Modelling Bionic Sweat Pores on Electronic Devices

***Abstract*—Thermal management plays an indispensable role in maintaining the normal operation of electronic devices. A proper management of heat produced by these devices is necessary, whilst not spend more than necessary for cooling. This is noticed in humans, where the body adaptively sweats, thus not losing unnecessary fluids. Motivated by this, we try to mimic this process in CPU and GPU cooling. Just like the human body, excess heat is produced only when they're put under the stress of computationally intensive tasks. Big data-centres have millions of these chips constantly cooled at the same rate, which could be re-established with this method to cut down cooling costs.**

I. Introduction

Perspiration is defined as the process by which the body releases liquid waste through the skin's pores. It plays a crucial role in regulating body temperature, as the evaporation of sweat from the skin helps cool the body down, particularly during physical activity or exposure to heat. The body's natural temperature regulation response allows for an optimal 36.0-37.4C operation. In this report, we will explore cutting-edge technologies in the field of silicon thermal management that allow for **bionic sweating** of high-power silicon surfaces. Our investigation will compare these advancements to traditional air and liquid alternatives to thermal management of System-on-Chip (SoC) architectures. To provide a comprehensive analysis, we will delve deeper into the design philosophy of **smart materials** employed in the paper, including their physical convolution that allows for optimal heat removal from the bulk of the system. This examination will be supported by simulations as well as insights derived from a synthesis of research papers and technical articles.

These proposals are grounded in both theoretical considerations and practical simulations, offering a holistic perspective on the latest developments in silicon thermals.

In the final sections of the paper, We present a self-simulated validation of the paper using simulation tools that compute the complex dependencies involved in cooling a chip. We set up a cooling solution based on the paper, giving special consideration to the unique mechanisms posed by it.

II. Inspiration

The proposed mechanism is founded at the core of biological thermal management. In a sedentary/low-activity state, the human body employs a largely convective and radiative heat dissipation. However, these fall short of the cooling demand during high energy activities, due to heat removal constraints. In response, the body **sweats** liquid water that spreads over its surface area and allows for evaporative heat dissipation. A feedback loop within the body controls the rate of release of sweat, via the opening of pores, until a threshold is reached and convective cooling is once again sufficient.

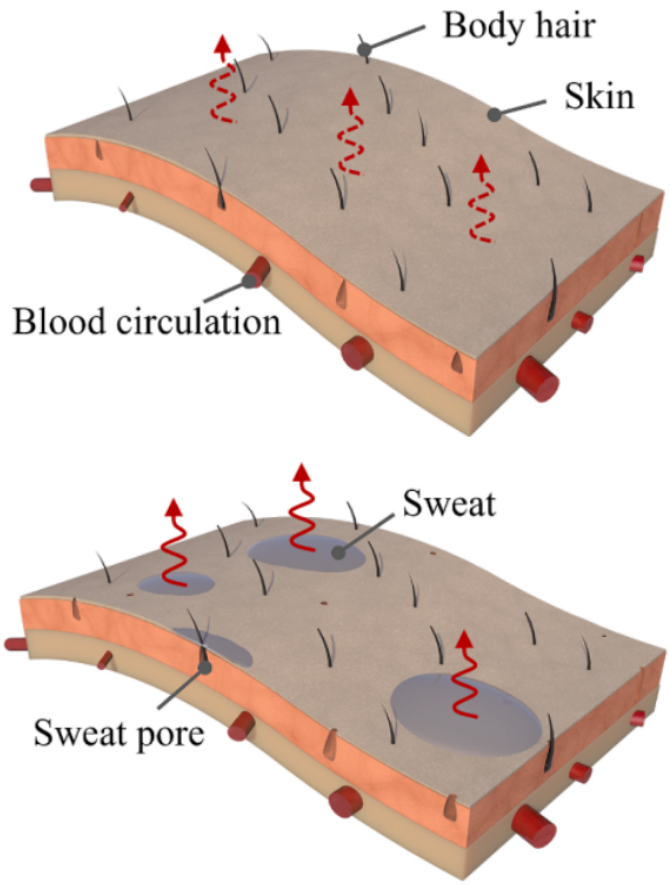

Fig. 1. Biological Sweating Mechanism

III. Existing Methods

A. Smart hydrogel valves

Dr. Gargava et al. [1] describe the design of hydrogels that can act as "smart" valves or membranes. Each hydrogel is engineered with a pore (about 1 cm long and ¡1 mm thick) that remains closed under ambient conditions but opens under specific conditions. The design is inspired by the stomatal valves in plant leaves, which regulate the movement of water and gases in and out of the leaves. The design features two different gels, active and passive, which are attached

concentrically to form a disc-shaped hybrid film. The pore is created in the central active gel, and the conditions for opening the pore can be tuned based on the chemistry of this gel.

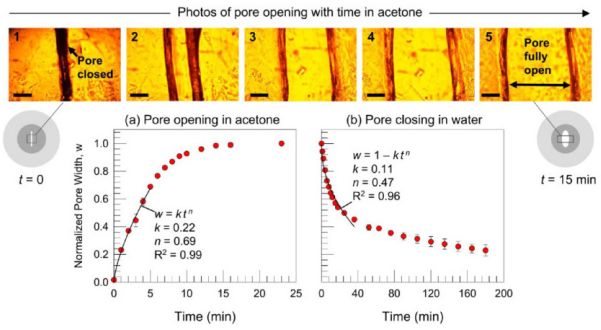

Fig. 2. Modelling pore opening with environmental conditions

B. Thermoelectric coolers

Park et al. [2] introduce a novel concept called the Adaptive Thermoelectric Cooling System (A-TECS). A-TECS utilizes an array of thermoelectric coolers (TECs) for both sensing and cooling purposes. It achieves this by employing a time-dependent sequence where each TEC alternates between temperature measurement and localized cooling.

Traditional methods rely on separate temperature sensors and TECs, leading to a more complex system design. A-TECS eliminates the need for additional sensors, simplifying the overall structure. The system operates in a four-step cycle:

- Heat Source Detection: Individual Seebeck voltages of each TEC are measured and analysed to identify localized heat generation.
- Cooling Location Determination: Based on the voltage analysis, A-TECS pinpoints the specific areas requiring cooling.
- Localized Cooling: The Peltier effect is utilized in the identified hot spots to achieve targeted cooling.
- Cycle Repetition: The entire process repeats continuously to maintain optimal temperature control.

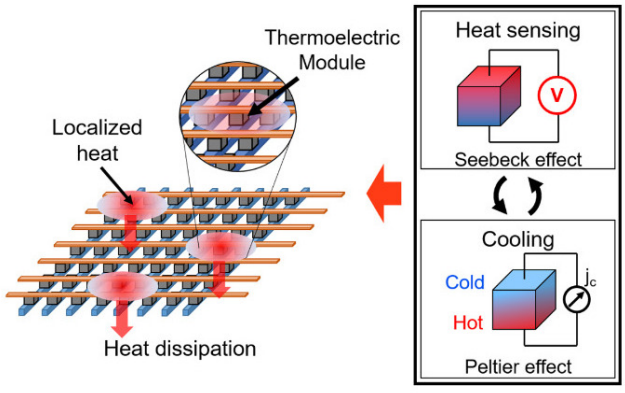

Fig. 3. Modelling pore opening with environmental conditions

In this paper, we focus on one particular such implementation:

IV. Bionic sweat pores

The paper [3] on the adaptive thermal management method via bionic sweat pores on electronic devices by Prof. Yu et al. will be the crux of our discussion.

A. An overview

The method employs shape memory alloys (SMAs) with martensite and austenite phases for adaptive state changes based on temperature variations. A millimetre-scale switch design incorporates shielding, deformation, and support structures to regulate bionic sweat pores in electronic devices. SMAs transition from martensite to austenite when temperatures exceed the phase transition point, returning to their initial state upon cooling. Differential scanning calorimetry verifies phase transition temperatures, crucial for achieving adaptive behaviour. The switch design's shielding structure has a diameter of 0.98 mm, and the deformation structure measures 7.81 mm in length. The SMA material's composition, including nickel, titanium, and hafnium, is adjusted to achieve a high phase transition temperature suitable for electronic device operation. Characterization via differential scanning calorimetry indicates phase transition temperatures during heating and cooling processes. The SMA switch demonstrates deformation, bending upward by a maximum of 2.8 ± 0.2 mm as temperature increases and returning to its initial state upon cooling. While thermal resistance and heat conduction affect deformation sensitivity, the focus remains on observing the SMA switch's deformation phenomenon.

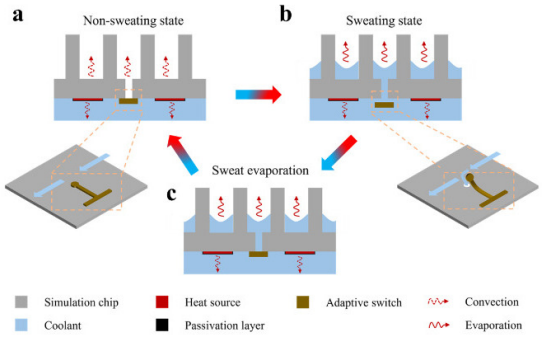

Fig. 4. The mechanism

B. The process

This paper also proposed a method to make a test bed. The SMA switch was affixed to the chip using acrylic tape, ensuring electrical characteristics remained unaffected by the passivation layer. Electrical connections were established via a printed circuit board-based interposer, bonded to the chip with high-temperature-resistant adhesive. Gold wire bonding facilitated interconnection, protected by light-curing adhesive. A water supply structure, constructed from transparent PMMA,

facilitated coolant provision for sweating and convection cooling. Its flow channel directed coolant to the chip's heat source, secured by acrylic tape to mitigate structural stress during experiments.

C. Modelling

Control Volume Definition:

- Our description of the control volume includes everything inside an infinitesimally small protruding surface, outside the concerned chip. This is a fixed control surface, with a macroscopic control volume inside it.

Underneath the chip coating, there are multiple bionic sweat pores inside, whose flow is allowed / blocked by a small Martensite strip, which on high temperatures, would change its shape by bending, thereby allowing underneath water to go upwards and evaporate, carrying the chip's heat with it. The temperature of the chip is estimated using a Platinum resistor, in front side of the chip.

Simplifying the governing equation using energy balance,

$$Q^{'} = hA_c \left(T_{\text{avg}} - T_{\text{in}}\right) + \dot{m}L$$

Constitutive Relations:

$$Q = V_{\text{chip}} \times I_{\text{chip}}$$

$$T_{\text{chip}} = \frac{1}{\alpha}\left(\frac{R_{Pt}}{R_0} - 1\right) + T_0$$

$$L = 2500 - 2.386T_l$$

Assumptions:

- The paper assumes that all the heat is dissipated through forced convection. This is a good approximation as heat transfer through other means: conduction through PCB, natural convection are assumed negligible compared to forced convection. Also, these means were present in the absence of sweat pores. So, it is justified to consider the effects of other predominant heat transfer modes.

V. Thermal Management

A. Background

The novel system of thermal management brings forth numerous compelling advantages for current System-on-Chip(SoCs). The most prominent is the dynamic design that allows for varied thermal management with maximized impact at critical temperatures. In contrast, air and liquid-cooled systems necessitate the use of inefficient power consumption, and highly resistive heat removal.

B. Simulation Tool

HotSpot v7.0 [4], a pre-RTL thermal simulator that supports the modelling of 2D, 2.5D and 3D integrated circuits (ICs) is used to demonstrate the same. Through LU Decomposition, it captures temperature traces of individual packages over time, relative to their power consumption.

HotSpot [4] divides the system into grids and utilizes finite difference methods to discretize the heat diffusion equation. This enables transient mapping of temperature changes. The discretized form of the heat diffusion equation can be represented as:

$$\frac{\partial T}{\partial t} = \alpha \cdot \frac{\partial^2 T}{\partial x^2}$$

where T is the temperature, t is time, x is the spatial coordinate, and α is the thermal diffusivity. The equation is solved iteratively over the grid to map temperature changes over time.

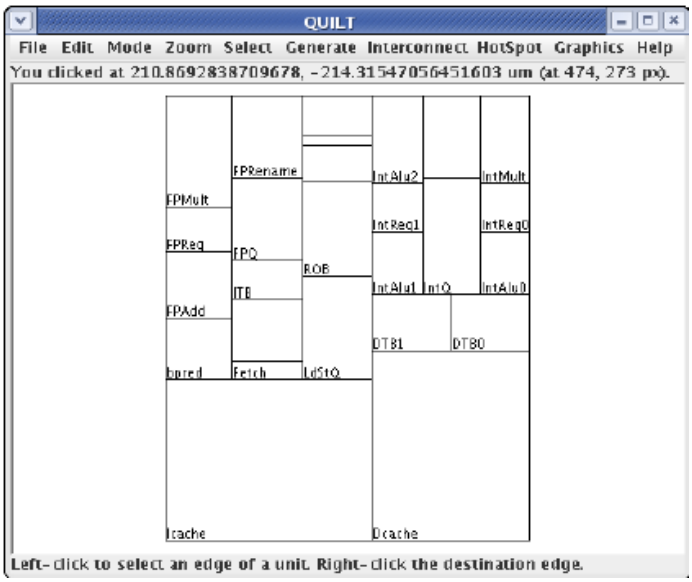

Fig. 5. Floorplan of Alpha Ev6 SoC

C. Setup

The simulation is set with the chosen SoC as the Alpha Ev6 processor thanks to its open-source and well-defined floorplan. The entire surface of the CPU is subdivided into a fine 64x64 grid for finite element analysis. Then, the tool is fed the constant-power heat load of each component on the package for time-variant analysis. A basic outline of the structure of the package is defined as a stack of multiple cuboidal elements with logged dimensions, and thermal properties.

D. Spec Information

We start our pipeline by creating an initial floor plan based on a set of given specifications, integrating the same with air, micro-fluidics [4] and the novel cooling circuit. To gain a basic specification and design baseline, we use the micro

architecture diagram of the system and then collate the area and power requirement for each specific component in the architecture. The design specifications were used to create the

TABLE I
MATERIAL PROPERTIES

Material	Type	Thermal Conductivity (W/(m-K))	Volumetric Heat Capacity (J/(m^3-K))
Silicon	Solid	130.0	1.63e6
Water	Fluid	2	3e6
Aluminum	Solid	237.0	2.422e6
Copper	Solid	400.0	3.55e6
Platinum	Solid	70	25.86e6
Martensite Steel	Solid	24.2	0.45e6
Austentite steel	Solid	45	0.51e6

custom configuration file required to construct and a heat map on Hotspot v7.0. A floor plan with the respective material and thermal properties was used for the simulations.

E. Package Analysis

[**?**] A multi-layered sandwich approach incorporated the

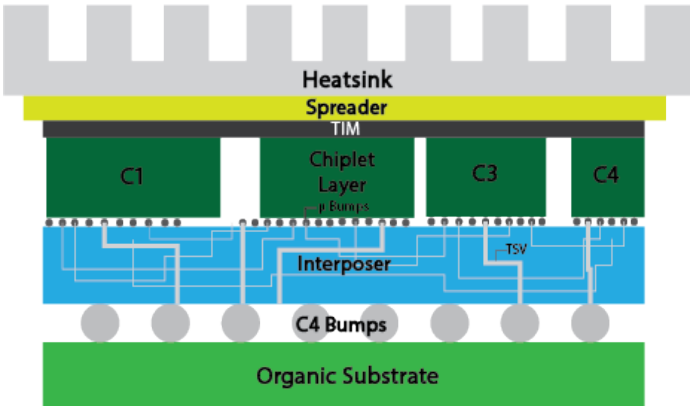

Fig. 6. Cross Section of Soc Package

[10]

following

[10]**Organic Substrate:** Provides structural support for the entire package and acts as a base for attaching various layers. **C4 Bumps (Controlled Collapse Chip Connection):** Facilitate electrical connections between the organic substrate and the interposer, enabling signal and power transmission between different layers. **Interposer with Through Silicon Vias (TSVs):** Serves as a bridge between corelets and facilitate communication. **Microbumps:** Enable fine-pitch connections between the interposer and chip layer, ensuring high-density, high-bandwidth intra-chip communication. **Chip Layer:** Contains the individual corelets (CPU, GPU, memory, etc.) and executes specific functions, contributing to the overall system functionality. **Thermal Interface Layer:** Manages and enhances thermal conductivity, ensuring efficient heat transfer from chiplets to subsequent layers. **Heat Spreader:** Disperses heat uniformly across the surface and enhances thermal performance by spreading heat generated by chiplets. **Heatsink:** Further dissipates heat into the surrounding environment, improving overall thermal management and preventing overheating. Provides an interface for interaction with fluid-cooling systems.

VI. RESULTS

A. Literature Results

[8]

- The effectiveness of the adaptive thermal management technique was proven through the modulation of power consumption to regulate chip temperature.
- The chip temperature stabilized at approximately 96.9°C under 6.2 W heating power and a forced convection flow rate of 20 mL/min. Upon increasing the heating power to 12 W, the chip temperature escalated to around 120.4°C, prompting the chip to enter the ”sweating” cooling phase.
- During the sweating phase, a sharp 64.8°C decline in chip temperature occurred due to rapid heat transfer facilitated by the substantial temperature disparity between the coolant and the chip.
- Equilibrium between heat transfer rate and water evaporation led to a stable evaporation state, maintaining a temperature of approximately 98.1°C.
- The sweating process terminated upon chip temperature reduction, transitioning to the dry-out stage, causing the chip temperature to rise.
- Analysis revealed a reduction in thermal resistance from 12.08 °C/W in the non-sweating state to 6.34°C/W in the stable evaporation state, denoting a 47.5% decrease compared to the non-sweating state, affirming the proactive cooling adjustment ability of the adaptive cooling method.
- **Influence of Forced Convection Cooling Capacity:** Cooling capacity during the stable evaporation stage decreased as forced convection cooling capacity increased. However, higher forced convection led to longer evaporation duration.
- **Impact of Evaporation Zone Interface State:** Plasma surface treatment reduced contact angle, covering more area for cooling. However, quicker evaporation times were observed, optimizing thermal management overall.
- **Influence of Sweat Volume:** Temperature reduction and duration of stable evaporation stage increased with higher sweat volumes. Larger droplets formed with increased sweat volumes, enhancing cooling performance.
- **Effect of Heating Power:** Higher chip power consumption increased chip temperature and sweat temperature. At small volumes, evaporation turned into boiling, increasing cooling capacity.

B. Simulation Results

1) Convective Air Cooled: With a purely air-cooled setup for the high-power(100W) die, temperatures very quickly exceeded 415K, exceeding the 398K **safe-operation** threshold set by the paper in less than 0.3s This very apparently highlights the limitations and inefficiencies of air cooling in high-performance setups.

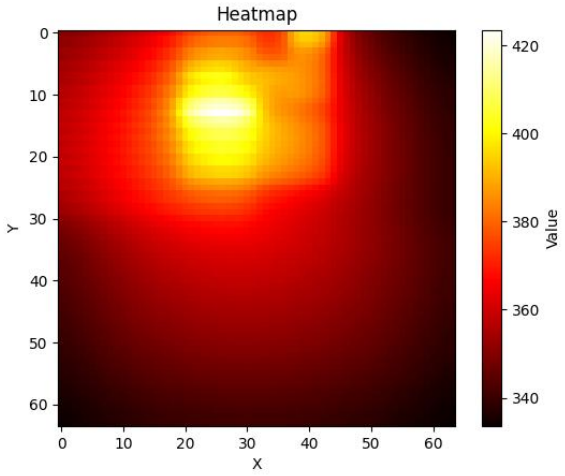

Fig. 7. Air Cooled Final Heatmap

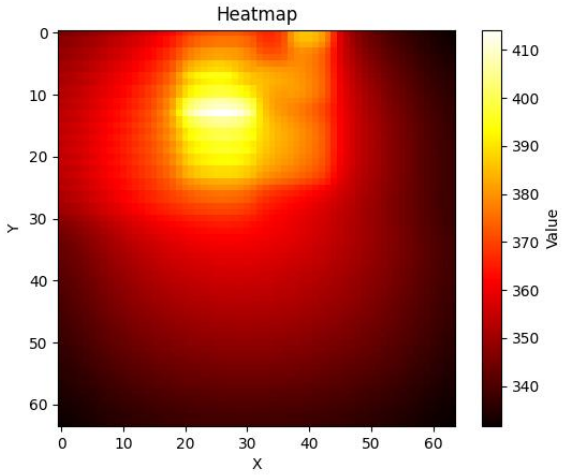

Fig. 8. Microfluidic Cooling Final Heatmap

2) Purely Microfluidic Setup: [10] Heat must be removed from the entire system outside the package, and transferred effectively and reliably to the ambient. While air cooling has proven to be a well-established low-cost option, it is inherently limited by surrounding conditions and low specific heat. Liquid cooling poses viable solutions for both these issues, but comes requires complex setups and necessitates adequate sealing and proofing. An additional layer that rests on top of the heat sink is established with a 32x32 grid of fine microfluidic channels. A simulated pump maintains a constant pressure at the entry and customizable channels run through the bulk of the system with water as the primary coolant. [10]

3) Bionic Sweat Pores: While the simulator is not designed for modelling the novel method of cooling, its code base was modified to accurately model the phase change, and in turn, the change in thermal properties of steel, and the fluid water.

TABLE II
MICROFLUIDIC COOLING PARAMETERS

Parameter	Value
Pumping Pressure (Pa)	52000
Pump Internal Resistance(Pa-S/m^3)	0
Inlet Coolant Temp(K)	298.15
Coolant Material	Water
Wall Material	Copper

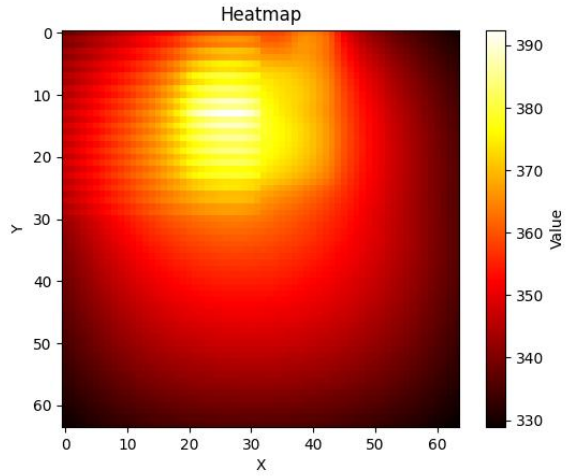

Fig. 9. Bionic Sweat Cooled Final Heatmap

A clever modification to the master shell script allowed for the alteration of material properties albeit a 'phase change' via a temperature cutoff. Parallelization of the base C code as well as optimization using the IBM Cplex solver [4] enabled the **Martensite-Austentite** shift to be represented in the model. As for water, modelling evaporation, accounting for latent heat, mass and pressure drop across the open area proved to be a daunting task in the limited time. Hence, a compromise was coded, accounting for an *average Cp* for the fluid.

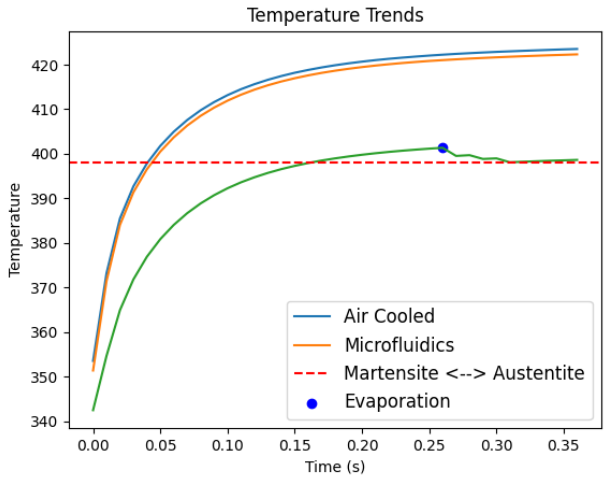

Fig. 10. Performance Comparison of Cooling Tech

As very apparent, at the high power output, conventional systems fall short of satisfying the needs of a high-density thermal load. The proposed bionic pores effortlessly shine through and allow for rapid **perspiration** through the surface. The blue point signifies the beginning of the evaporation process, amassing the largest heat-removal volume.

VII. Critique

A. Challenges in Practical Implementation

- Designing and engineering systems for bionic sweating demands expertise in multiple disciplines, including materials science, thermal engineering, and electronics.
- Cost and complexity may hinder widespread adoption, necessitating a balance between system design intricacies and practical considerations such as cost efficiency and integration into existing devices.

B. Reliability and Durability Evaluation

- Thorough evaluation of the long-term reliability and durability of bionic sweat pores and the liquid circulation system is essential to ensure consistent performance and prevent potential hazards such as overheating or fire incidents.

C. Scalability and Integration Challenges

- The paper should address the scalability of the bionic sweating method for diverse electronic devices and its integration into existing device designs to assess its practicality across various applications.
- Additionally, a more detailed exploration of chip integration with other devices is needed, considering factors influencing overall heating.

VIII. Conclusion

The increased integration density of electronic components and subsystems, including the nascent commercialization of 2.5D chip stack technology, has exacerbated the thermal management challenges facing electronic system developers. The confluence of chip power dissipation above 100 W, localized hot spots with fluxes above 1 kW/cm2, and package-level volumetric heat generation that can exceed 1 kW/cm3 has exposed the limitations of the current "remote cooling" paradigm and its inability to support continued enhancements in the performance of advanced silicon and compound semiconductor components. To overcome these limitations and remove a significant barrier to continued Moore's law progression in electronic components and systems, it is essential to "embed" aggressive thermal management in the chip, substrate, and/or package and directly cool the heat generation sites.

The cooling capacity achieved through forced convection of the coolant and bionic sweating behaviour suggests a promising outlook to the problems of the future-present:

- Bionic sweating behaviour boosts cooling in electronic devices, adding 80% of the original capacity and lowering the temperature by $22.3°C$.
- The flexibility of the system allows for thermal adjustment by varying evaporation zone properties, sweating volume, and phase change.
- Pool boiling with bionic sweat shows promise for greatly enhancing cooling, with potential maximum capacities of 208 W/cm^2 through structural optimizations like increased surface roughness and optimized micropillar spacing.

The system is designed around the sole purpose of deployment in high-performance environments that need the robustness to handle harsh life cycle conditions where boundary conditions and fundamental assumptions might fail (for example: assumption of available draft air or forced convection for passive heat sinks or cooling loops with radiators). An additional facet of the approach ensures maximum effectiveness of the system while minimizing power requirements for the same as the energy cost must be present in all considerations.

References

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