A Simple Approach to Design a Binary Coded Absolute Shaft Encoder

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A Simple Approach to Design a Binary Coded Absolute Shaft Encoder

Subir Das, Tuhin Subhra Sarkar, Badal Chakraborty, Himadri Sekhar Dutta

Abstract— **In this paper, an optical type absolute shaft encoder coding pattern is presented. Compared to conventional binary or gray code pattern resolution (2^n), proposed code exhibits two times more resolution (2^{n^2}). Even, to represent high density positional information of rotating object, it is required very less number of tracks. This pattern sequence is based on *n*-by-2 matrices of binary codes where consecutive two column of each code represented as high-low order bits. To retrieve the encoded position from these coding patterns, an extra pulse track was added at the outside of coded tracks. Moreover, it was used for providing a synchronized clock pulse into a simple photo-detector based sequential logic circuitry; is the decoding unit of this encoder. Thus depending on these synchronized pulses, proposed encoder is able to provide error free positional information for high speed rotating object. Eventually, in order to proof of this concept, a prototype is designed and tested, where a satisfactory performance was achieved.**

Index Terms—**optical sensor, absolute encoder, binary code, position sensor, encoder design.**

I. INTRODUCTION

ABSOLUTE shaft encoder is used in numerous applications such as precise position controlling of robotic arm, surveying instruments, astronomical apparatus etc. Traditionally, absolute shaft encoder consists of an encoded disc and a decoding unit. This encoded disc carries some positional information by using set of linear codes or mechanical pattern. During the rotation of disc with the object, a decoding unit decodes these codes or patterns and expressed the positional information in terms of analog or digital signals.

In article [1], authors presented a design of absolute angular position sensor based on the law of electromagnetic induction. This encoder consisted with two parts: six Hall ICs and a radial magnetizing ring. Here magnetizing ring acts as a mechanical pattern type encoded disc. Besides, six hall ICs used for measuring the intensity of the magnetic field around the magnetizing ring; is the basic phenomenon of this pattern. During the rotation of magnetizing ring with the object, a signal processing circuit used for process those Hall ICs output voltage and thus evaluated the object rotational angle in terms of magnetic field variation. Another mechanical pattern type absolute angular-position sensor is implemented by using the phenomenon of capacitive effect; is presented in [2]. Here, one plate of the capacitor is fixed and another plate rotates with the object; thus it acts as an encoded disc. Moreover, sometimes encoder disc designed with gradient gray color track and three RGB sensors. This sensor is used for identifying the polar co-ordinate of gray color track; is reported in [3].

The manufacturing cost of mechanical type absolute shaft encoder is high and not immune to environmental hazards viz. electromagnetic interference, dirt, dust and moisture etc. Also, its sensitivity and accuracy is mostly depending on physical structure of the disc. In contrast with mechanical structure, optical type shaft encoder is highly acceptable because its sensitivity and accuracy is not affected by the environmental hazards. Most of the commercially available optical type absolute encoder used linear code (2^n) pattern, because its accuracy and sensitivity is not effected by physical structure. Also, resolution of this pattern depends only on length of the code bits; is the major advantage of this pattern. For example, if code consists of *n*-binary bit then resolution will be 2^n and described 2^n positions. But *n*-separate tracks are required over the disc to represent each bit of this code. Thus, fabrication of small tracks over the disc makes the system costlier.

Many improvement of this coding pattern have been published in recent years [4]-[10] to reduce the fabrication cost and increase the resolution by limiting the track number. Here, a linear code is implemented within a single track. Mainly this single track code is based on De-Brujin sequence [7], [8] or Psedurandom coding patterns [9], [10]. By using these two coding patterns, Agrawal et.al [11], [12] and H. Wang et.al [13] developed a low cost absolute encoder for detecting the position of slow moving object. Both of these encoders decode these sequences by capturing the image of the code by using a CMOS camera and an image processing algorithm. Despite of its simplicity in terms track number and inexpensiveness, its output response time is too slow and unable to produce enough high resolution. Without use of single track code, Y. Sugiyama [14] et.al designed a rotary encoder module by implementing high speed 2D CMOS profile sensor and multi-track code disc. The disc has 64 indices and each index consists of a 6 bit code and one centre reference hole. The center reference hole is used to define the relative position of each index code area. Besides, Y axis profile data from the profile sensor are used for recognition of an index code on the disc and X axis profile data are used for position detection of this index code. This combination of

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two-axis image information provides high resolution (14-bit) positional information by using less amount of digital data. It is expensive but profile sensor can detect index position with the speed of 3.2 KHz. In this context, T. Dziwinski [15] proposed a novel multi- track, high resolution coding pattern. It is also based on the analysis of 2D images. The pattern is designed by finding a solution for Hamiltonian cycle problem in 2D matrices code. This pattern can encode 2^{n^2} unique positions by using *n* number of separate tracks (called as row) and 2^{n^2} separate columns. Here, the resolution of this code varies with the power-law factor. Hence it is advantageous over linear code that by using the same number of tracks this code allows more positional information. A Charge Coupled Device (CCD) and a processing unit with code memory are used for decoding this pattern. The high-speed CCD sensor captures the fragment of the pattern disc in respect to the current object position and sends it to the processing unit. Thus an appropriate position is directly determined after sorting the coding pattern in non-volatile memory.

In [11]-[15], designed encoder claims high resolution coding pattern by using limited number of tracks. But decoder unit's image capturing rate cannot synchronize with object speed while object rotational speed exceeds their limit. Thus it provides an error.

In this paper, an absolute shaft encoder coding pattern has been presented for detecting the angular position of high speed rotating object. This high resolution (2^{n^2}) coding pattern is based on binary combinational logic state and realized into a disc with *n* separate tracks and 2^{n^2} segments. The pattern sequence represents each unique position by considering two consecutive segment codes (called *n-by*-2 matrix) and resolution varies by the track numbers. For the purpose of synchronization with the object speed, the decoding unit is fabricated using a simple sequential logic circuit. The driving clock pulse for this circuit is provided by an extra track, which is added at the outside of the coded track. Thus during the rotation of the disc, this track supply a clock pulse to the circuit with the same speed of object. Also, it is used to retrieve the positional information from two consecutive segment codes. Thus, the decoding unit is free from any complex image processing algorithm. In order to proof of this concept a prototype has been fabricated and tested.

II. Implementation of Proposed Binary Coding Pattern

The conventional binary coded shaft encoder represents 2^n positions using *n* number of tracks. In this context, an attempt has been taken to increase the positional information using limited number of tracks. Here, proposed coding patterns exhibits 2^{n^2} positions by *n* numbers of tracks. Hence it is obvious that by using the same number of tracks, proposed binary code represents two times more positional information. In this design 2^{n^2} coding pattern is developed from two sets of 2^n binary coding information. For generating this *n* track pattern, a generalized algorithm has developed in MATLAB platform and each step illustrated by an example of two track (*n* = 2) code. But it can be extended further for the desired value of *n* by analyzing the each step of this algorithm.

Step 1: Two one dimensional arrays are created with 2^n *combinations of binary data elements. It is organized as column vector format of* H[i] *and* L[i] where i = 0 to $(2^n - 1)$

For *n = 2*, the elements of each array are {00,01,10,11}.

$$\begin{bmatrix} H_0 \\ H_1 \\ H_2 \\ H_3 \end{bmatrix} \quad \begin{bmatrix} L_0 \\ L_1 \\ L_2 \\ L_3 \end{bmatrix}$$

Fig.1. Representation of each array elements for *n* = 2. Here H[i] and L[i] array element are expressed as higher and lower order bits of proposed codeing patterns..

Step 2: From this two one dimensional array, 2^n *separate two dimensional (2D) arrays is made. The dimension of each array is* 2^n*-by-2. As an example the elements of first array are expressed bellow;*

A[m,0] = H[0]

A[m,1] = L[i] where, i = m and range starts from 0 to $(2^n - 1)$

$$A1 = \begin{bmatrix} H_0 & L_0 \\ H_0 & L_1 \\ H_0 & L_2 \\ H_0 & L_3 \end{bmatrix} \quad A2 = \begin{bmatrix} H_1 & L_0 \\ H_1 & L_1 \\ H_1 & L_2 \\ H_1 & L_3 \end{bmatrix} \quad A3 = \begin{bmatrix} H_2 & L_0 \\ H_2 & L_1 \\ H_2 & L_2 \\ H_2 & L_3 \end{bmatrix} \quad A4= \begin{bmatrix} H_3 & L_0 \\ H_3 & L_1 \\ H_3 & L_2 \\ H_3 & L_3 \end{bmatrix}$$

Fig.2. For *n* = 2, four separate array ($A_{4,2}$) is found. In these arrays, each elements of L[i] are combined with a single elements of H[i].

Step 3: A union operation performed sequentially in between of two consecutive 2D arrays. Here in accordance with the first array, the matching element of second array has been removed. Consequently $(2^n - 2)$ *separate 2D array is found. Where, the dimension of each array is* 2^n*-by-3.*

$$B1 = \begin{bmatrix} H_0 & L_0 & H_1 \\ H_0 & L_1 & H_1 \\ H_0 & L_2 & H_1 \\ H_0 & L_3 & H_1 \end{bmatrix} \quad B2 = \begin{bmatrix} H_2 & L_0 & H_3 \\ H_2 & L_1 & H_3 \\ H_2 & L_2 & H_3 \\ H_2 & L_3 & H_3 \end{bmatrix}$$

Fig.3. After performing union operation in between of A1∪A2 and A3∪ A4 two separate 2D arrays has been appeared viz. B1 and B2.

Step 4: From each 2D array two subarray are created. Consequently, 2^n *separate subarray is found. Here the first and second subarray has made with even and odd row element of 2D array. Therefore, each subarray will have* $(2^n/2)$ *separate rows and* $(2^n - 1)$ *separate columns.*

$$B11 = \begin{bmatrix} H_0 & L_0 & H_1 \\ H_0 & L_2 & H_1 \end{bmatrix} \quad B12 = \begin{bmatrix} H_0 & L_1 & H_1 \\ H_0 & L_3 & H_1 \end{bmatrix}$$

$$B21 = \begin{bmatrix} H_2 & L_0 & H_3 \\ H_2 & L_2 & H_3 \end{bmatrix} \quad B22 = \begin{bmatrix} H_2 & L_1 & H_3 \\ H_2 & L_3 & H_3 \end{bmatrix}$$

Fig.4. Here only four separate subarray has been found for n = 2. Subarray of B1 and B2 has been expressed as B11, B12, B21 and B22 respectively. Also, two numbers of row and three numbers of columns has been found in each array.

Step 5: A union operation completed sequentially in between of consecutive two sub array. Here in accordance with the first array, the matching element of second array has been

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removed. Thus, $(2^n - 2)$ *separate array are found with* $(2^n/2)$ *number of rows and* 2^n *number of columns.*

$$C1 = \begin{bmatrix} H_0 & L_0 & H_1 & L_1 \\ H_0 & L_2 & H_1 & L_3 \end{bmatrix} \quad C2 = \begin{bmatrix} H_2 & L_0 & H_3 & L_1 \\ H_2 & L_2 & H_3 & L_3 \end{bmatrix}$$

Fig.5. After completion of union operation in between of B11∪ B12 and B21∪ B22 two separate array of $C_{2,4}$ has found.

Step 6: Transpose of each array; noted as $C^T\,[2^n, \frac{2^n}{2}]$.

$$[C1]^T = \begin{bmatrix} H_0 & H_0 \\ L_0 & L_2 \\ H_1 & H_1 \\ L_1 & L_3 \end{bmatrix} \quad [C2]^T = \begin{bmatrix} H_2 & H_2 \\ L_0 & L_2 \\ H_3 & H_3 \\ L_1 & L_3 \end{bmatrix}$$

Fig.6. A Transpose operation performed in each array of $C_{2,4}$. Consequently, the dimension of each array is now changed to $C_{4,2}$.

Step 7: Finally a single array $D\,[2^n, 2^n]$ *is found after combining the each transpose array of* $C^T\,[2^n, \frac{2^n}{2}]$. *In this combining process a horizontally concatenate operation performed by considering the all matching element of these two arrays.*

$$D = \begin{bmatrix} H_0 & H_0 & H_2 & H_2 \\ L_0 & L_2 & L_0 & L_2 \\ H_1 & H_1 & H_3 & H_3 \\ L_1 & L_3 & L_1 & L_3 \end{bmatrix}$$

Fig.7. After completion of concatenation operation in between of $C1^T$ and $C2^T$ array a single 2D array is found. The dimension of presented array is 2^n-by-2^n. In this way, total 2^{n^2}numbers of element would be appeared in this array. For n = 2, we have got sixteen element in an array.

Step 8: one dimensional array (K) has made from $D\,[2^n, 2^n]$ *array element by sorting the elements as column major order. Hence the dimension of* "K" *array would be* 2^{n^2}.

$$K[16] = \{H_0, L_0, H_1, L_1, H_0, L_2, H_1, L_3, H_2, L_0, H_3, L_1, H_2, L_2, H_3, L_3\}$$

Fig.8. For n = 2, elements of K $[2^{n^2}]$ array are represents the proposed coding pattern sequence.

The elements of K-array represent the proposed coding sequence. Here, each element is a set of *n*-bit binary numbers represented as segment and consecutively two segments indicate *n*-by-*2* binary matrix code. Some selected code versus positional value is shown in Table I. In order to proof of this coding sequence validity, it could be represented as cycles in the undirected graph. The goal is to design a cyclic sequence, where all possible *n*-by-2 matrices code (2^{n^2}) would be appear exactly once. A generalized structure of this matrix code is shown in Fig.9, where first and second column indicates higher and lower order bits respectively.

$$C = \begin{bmatrix} d_{(2n-1)} & d_{(n-1)} \\ d_{(2n-2)} & d_{(n-2)} \\ \vdots & \vdots \\ d_n & d_0 \end{bmatrix}$$

Fig.9. *n*-by-2 Matrix Code bit format.

TABLE I
TRANSLATION BETWEEN 2×2 MATRIX CODES AND ANGULAR POSITION

Positional code	Code Matrices	Trackwise Code Higher & Lower order bits		Angle [^{0}]
		H	L	
C1	$[H_0\ L_0]$	0 0	0 0	0
C2	$[H_1\ L_0]$	0 1	0 0	22.5
C3	$[H_1\ L_1]$	0 1	0 1	45
C4	$[H_0\ L_1]$	0 0	0 1	67.5
⋮	⋮	⋮	⋮	⋮
C15	$[H_3\ L_3]$	1 1	1 1	337.5
C16	$[H_0\ L_3]$	0 0	1 1	360

Let *G = (V, E)* be the simple undirected graph composed of a set *V(G)* of vertices and a set *E(G)* of edges. Each *n*-by-2 matrix code represents a vertex of a set *V(G).* A set *E(G)* of edges defined by following consideration: There is an arc (edges) in between of different vertices *u* and *v* if a column element of *u* is present in vertex *v*. That means edge set *E(G)* is composed with pair of vertices; $(u,v) \in E(G) : u \neq v$. Hence, we can say that vertices *u* and *v* are adjacent to each other.

A. Properties of undirected graph

- Order (number of vertices) of the graph = 2^{n^2}
- Adjacency matrix of the graph should be symmetric.
- Diagonal elements of adjacency matrix should be containing zero, if the graph is simple (i.e. graph does not contain any loop).
- The graph said to be connected if every vertex has an even number of edges.

Let's consider the graph *G* for *n*=2. The set of 2-by-2 matrix (C) represents seed codes for 2^{n^2}=16 positions and constitutes the set of vertices *V (G).*

$$C_0 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \quad C_1 = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \quad C_2 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \quad C_3 = \begin{bmatrix} 0 & 1 \\ 0 & 1 \end{bmatrix}$$

$$C_4 = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \quad C_5 = \begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix} \quad C_6 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \quad C_7 = \begin{bmatrix} 0 & 1 \\ 1 & 1 \end{bmatrix}$$

$$C_8 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \quad C_9 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad C_{10} = \begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix} \quad C_{11} = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}$$

$$C_{12} = \begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix} \quad C_{13} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \quad C_{14} = \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix} \quad C_{15} = \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$$

The adjacency matrix *A* is the most convenient way in this case to represents the set of edges *E(G)* for the set of vertices *V(G)* = { C_0, C_1 .... C_{16}}.

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$$A = \begin{bmatrix} 0&1&1&1&1&0&0&0&1&0&0&0&1&0&0&0 \\ 1&0&1&1&0&1&0&0&0&1&0&0&0&1&0&0 \\ 1&1&0&1&0&0&1&0&0&0&1&0&0&0&1&0 \\ 1&1&1&0&0&0&0&1&0&0&0&1&0&0&0&1 \\ 1&0&0&0&0&1&1&1&1&0&0&0&1&0&0&0 \\ 0&1&0&0&1&0&1&1&0&1&0&0&0&1&0&0 \\ 0&0&1&0&1&1&0&1&0&0&1&0&0&0&1&0 \\ 0&0&0&1&1&1&1&0&0&0&0&1&0&0&0&1 \\ 1&0&0&0&1&0&0&0&0&1&1&1&1&0&0&0 \\ 0&1&0&0&0&1&0&0&1&0&1&1&0&1&0&0 \\ 0&0&1&0&0&0&1&0&1&1&0&1&0&0&1&0 \\ 0&0&0&1&0&0&0&1&1&1&1&0&0&0&0&1 \\ 1&0&0&0&1&0&0&0&1&0&0&0&0&1&1&1 \\ 0&1&0&0&0&1&0&0&0&1&0&0&1&0&1&1 \\ 0&0&1&0&0&0&1&0&0&0&1&0&1&1&0&1 \\ 0&0&0&1&0&0&0&1&0&0&0&1&1&1&1&0 \end{bmatrix}$$

From the earlier discussion, it can be said that the graph *G* is an undirected graph because the matrix *A* is symmetric (i.e. A = A^T) and contain no loops. Since, each row or column element of a matrix *A* represents edge of vertices. Hence sum of all edges of a vertex shows even numbers, hence the graph is connected.

B. *Hamiltonian Cycle*

Hamiltonian path in an undirected graph *G* is a path that goes through each vertex in a graph exactly once. If a path starts and end with a same vertex then it is called a Hamiltonian cycle. A graph which has at least one Hamiltonian cycle is called Hamiltonian graph. A Hamiltonian cycle exists in a graph if and only if an Eulerian cycle exists on that graph.

Lemma1: Euler's Theorem; an undirected graph has an Euler Cycle if and only if graph is connected and each vertex composed of even number of edges.

Based on the analysis of adjacent matrix *A* it is obvious that undirected graph *G* has at least one Euler cycle and there should be exists a Hamiltonian cycle. But there can be found more than once of Hamiltonian cycle in a graph *G*. Hence, at the time of travelling in a cycle from same start to end vertex, sequentially arrival of vertices is represent a sequence of code.

Since, in this proposed pattern *n*-by-*2* matrix sequence has organized as successive high-low ordered pair bits. Hence, in that case one such Hamiltonian cyclic vertex sequence is chosen by the following criterion: one vertex should follow the next one if two vertices second column (lower order bits) elements are equal and sequentially next vertex follows the other one if two vertices first column (higher order bits) elements are equal. Thus, sequence matrices are ordered on a disk by overlapping each of their matching columns. Hence, each matrix overlaps the previous by exactly all columns. The reported coding sequence for *n*=2 tracks is one of the example of high-low ordered Hamiltonian vertex sequence for the graph *G*. To identify the lower and higher order segment of this sequence as well as providing a pulse to the decoder unit an extra track is append outside the coded track. It is called as "CLK" track. Schematic diagram of this proposed pattern disc is shown in Fig.10.

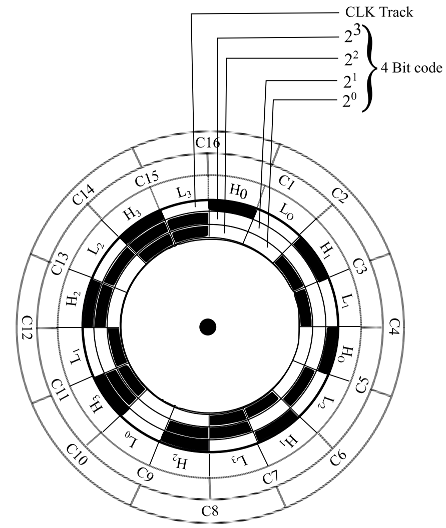

Fig.10. The 2 track, 4-bit code pattern disc

III. Working Principle Of Decoding Unit For Proposed Binary Code

Decoding unit for this proposed binary coding sequence is implemented by using a simple sequential logic circuitry. This unit is designed for decode only 4-bit track code. But it can be extended further for larger coded track by using the same stated principle. This circuitry comprises with series of D-Flip Flops (number of flip flops are depend on length of the code bits) and series of photo-detectors (as per the number of tracks). Photo-detectors are placed parallel over the disc tracks for optically sensing the track code bits through the flip flops and providing a clock pulse into the circuit. In this prototype, separate tracks as well as photo-detectors are identified as same notations: CLK (outer most track and detector), B1 and B0 (separate inner tracks and detectors), is shown in Fig.11 (a).

In the code disc each track slit represents a bit as shown in Fig.10. Here, opaque slit (noted as black) in between of source and detector is denoted as logic "1" and transparent slit in between of them denoted as logic "0". Hence, photo-detector detects each bit by conventional opto-interruption technique. Now, TTL level output from B1 and B0 photo-detectors are feed to the corresponding binary powered D-flip flop input ports and CLK photo-detector output is attached with clock input pin of all flip flops; shown in Fig.11(b). During the rotation of disc along with the object the CLK photo-detector supplies a continuous clock pulse into the flip flops. Therefore according to Fig.11(b), at any time instant two flip-flop gets direct pulse from CLK and the other two gets inverted pulse after converted through NOT gate. Now, if the CLK detector is detect an opaque slit, a high pulse will appear into the higher order (2^3, 2^2) filp-flops according to law of opto-interruption technique and its output will change according to the current output state of B1 and B0 but at the same time the lower order (2^1, 2^0) flip flops will receive a low clock pulse and will latch the previous output state of B1 and B0. This process will occur in reverse order when a low pulse appears

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from CLK detectors. The output state transition of flip-flops is shown in Table II.

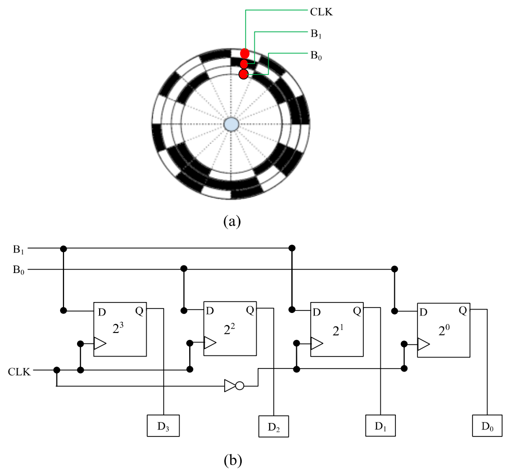

Fig.11. (a) Position of photo-detectors above the tracks. (b) Logical diagram of decoding unit.

TABLE II
TRUTH TABLE OF PROPOSED DECODING UNIT

CLK	D_3	D_2	D_1	D_0
HIGH	B_1	B_0	B_{1Prev}	B_{0Prev}
LOW	B_{1Prev}	B_{0Prev}	B_1	B_0

Thus, it is obvious from Table II that after shifting of every one segment a pulse will be inserted into the flip-flop circuit and a new code will appear by considering the previous latch segment code bits. Hence, without use of external source of clock pulse this design able to drive a sequential circuit and retrieve the encoded bits. Thus, it is fully synchronized with object speed and provides error free output for high speed rotating object.

IV. PROTOTYPE

The prototype is built to validate the applicability of presented method. Normally, encoders may provide either a serial or a parallel output for digital representation of absolute position. A common trend in industrial automation are encoders with serial output interfaces, i.e. PROFIBUS, DeviceNet or Synchronous Serial Interface (SSI). In this context, designed prototype is made with a low cost microcontroller (AT89S52) based processing unit with local display facilities. Also, it can be interfaced with other electronic measuring unit by SSI protocol. Graphical representation of this prototype is shown in Fig.12.

Based on the above mentioned sequence as shown in Fig.8, proposed encoder disc realized into a transparent fibre glass sheet. This patten is drawn using a INKSCAPE vector graphics software, where each column of this sequenced matrices represents a segment on the disc. Therefore according to the overlap column elements (bit) of two consequtive matrices, each segment are sliced by circular type multiple tracks. Now each slit of a segment are filled up by black (bit: “1”) and white (bit: “0”) color depends on column binary bits. CLK track is sliced and filled up by black and white color as per segment order. Subsequently, Print copy of this image is affixed over the glass sheet by cutting out the white color slits area.

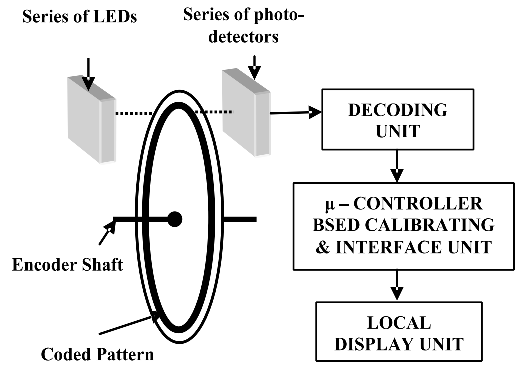

Fig.12. Graphical abstract of designed prototype.

For testing the performance of Prototype, a 100rpm motor coupled with this encoder disc shaft and as well as sensing the binary bits from encoded segment, disc is placed in between of miniature type IR LEDs (dimension of 5mm) and photo-transistors. A decoding unit retrieves the encoded bits from TTL output of photo-transistors by using the object speed oriented synchronized clock pulse and transmits the code bits to the processing unit for calibration with the rotational position information. Eventually, calibrated positional information is displayed on the local LCD panel. Some selected code versus rotational position (in degree) is shown in Table I.

V. CONCLUSION

Proposed coding pattern design is very simple and provides high resolution. Compared to conventional binary or gray code (2^n) pattern, it can present two times more positional information by the increase of track number (i.e. resolution varies with 2^{n^2}). Also instead of prior CMOS profile sensor [14] and CCD sensor [15], a simple sequential logic circuit is required for decode this coding pattern. In the prior art [15] binary coding matrix dimension is varied by the track numbers. Hence there is a limitation of CCD sensor based decoding unit that with the increase of track number, CCD sensor unable to focus on entire matrix pattern. In contrast with the variation of track number, proposed code matrix row number has been varies and column number remains unchanged. Therefore, only quantity of photo-transistor will be varied according to the track numbers. In terms of equipment cost and selection criteria, this design step is more significant because replacement/addition of photo-transistor is easier than CCD sensor. Moreover, major drawbacks of CMOS or CCD sensor based decoder unit is non synchronized scanning rate with respect to the object rotation and require high processing time to decode the coding pattern. Due to which decoder unit is unable to retrieve the coding information from the encoded disc with the increase of object speed. To resolve this issue, in the proposed pattern an extra track has been added outside the coded track. This track provides an object speed oriented synchronized clock pulse to the sequential circuit by which proposed decoder unit scanning time is fully dependent on object speed. Furthermore, photo-detector based sequential circuit able to present binary *n*-bit code directly, so it is free from any complex computation processing algorithm and require less processing time. This concept has been proved, verified and tested with laboratory prototype. Hence, we claim that propose method is the best choice for high speed rotating object position estimation applications. Also, propose coding pattern improves the resolution of the absolute encoder by using limited number of tracks.

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