音频解码芯片规格书

——AC309N 芯片

珠海市杰理科技有限公司

版本：V1.0

日期：2011.7.26

AC309N Features

High performance 8-bit MCU

- DC-48MHZ operation
- Compatible with 8051
- All instructions are single-cycle except branching instructions
- Two data pointer for indirect addressing

Program Memory

- 32K Bytes OTP program memory

Interrupt Feature

- 15 Vectored interrupts
- External wake up/interrupt on 4 GPIOs
- 4 Levels interrupt priority

Flexible I/O

- 29 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input

Digital Peripheral Feature

- Two multi-function 8-bit timers,support capture and PWM mode
- Two multi-function 16-bit timers, support Capture and PWM mode
- Watchdog
- One full-duplex UART
- MPEG-1, MPEG-2, MPEG-2.5 Audio Layer 1,2,3 decoder. Bit rate 8-448Kbps, CBR/VBR/ABR
- Support WMA format, data rate support 5kbps or above
- Support 9 sampling frequency:
  8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
- One SPI, support DMA
- One EMI
- SD Card Host controller
- Full speed USB 2.0 HOST/DEVICE controller

Analog Peripheral Features

- One 1~24MHz Crystal Oscillator
- An independent powered RTC with One 32KHz Crystal Oscillator
- One internal RC oscillator
- Full speed USB 2.0 PHY
- 48MHz PLL-based clock generator
- 24-bit Stereo DAC，SNR > 90dB

Confidential
The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

- Embedded headphone amplifier
- 2 channels Analog MUX
- 8 Channels 10-bit ADC
- 2 channels 4 levels Low Voltage Detector
- Power-on reset
- Two LDO: 5V to 1.8V, 5V to 3.3V

Power Supply

- VDDLDO is 3.2V to 5.5V
- VDDIO is 3.0V to 3.6V
- VDDCORE is 1.6V to 2.0V

Packages

- LQFP64
- LQFP48
- SSOP28
- DIE form

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Confidential
The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

二、引脚定义

2.1 引脚分配

图 1　AC309N_64PIN 引脚分配图

Confidential
The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

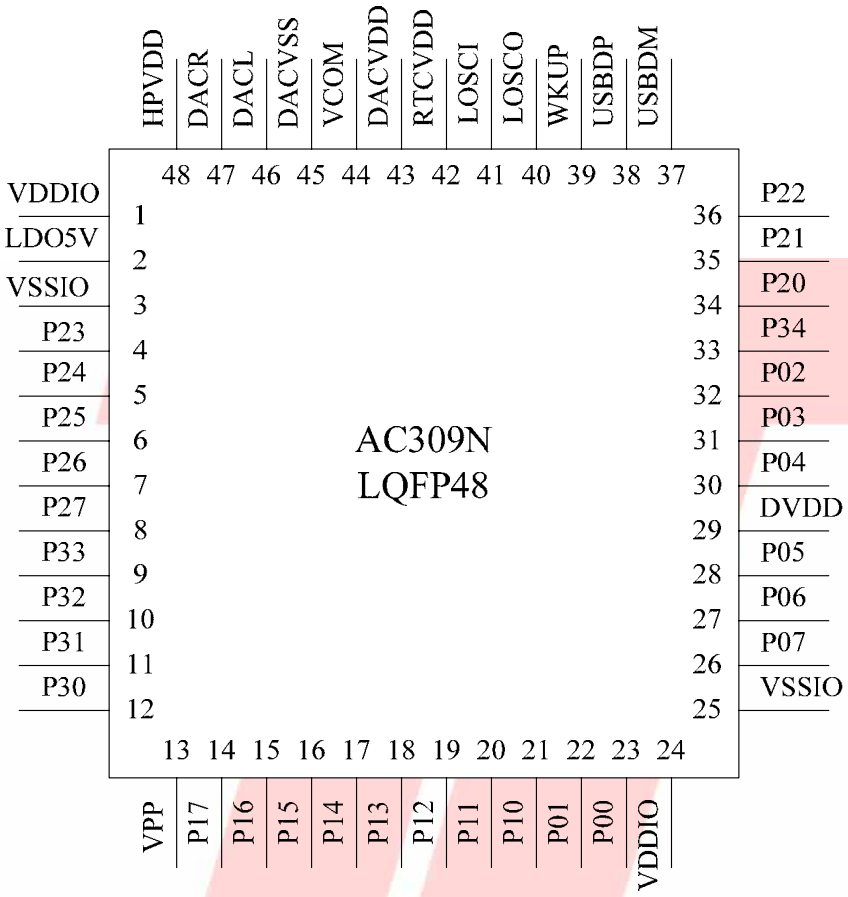

图 2　AC309N_48PIN 引脚分配图

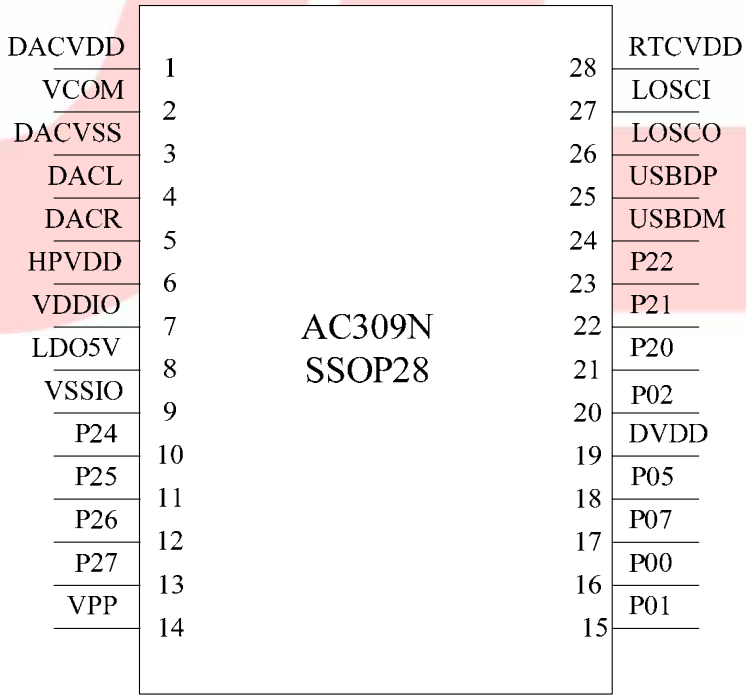

图 3　AC309N_28PIN 引脚分配图

Confidential
The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2.2 引脚描述

PIN#			Name	I/O Type	Drive (mA)	Function	Other Function
LQFP64	LQFP48	SSOP28					
1	48	6	HPVDD	P	/	Headphone Power 3.3V	
2			IR			IR Filter Input	
3	1	7	VDDIO	P	/	IO Power 3.3V	
4	2	8	LDO5V	P	/	LDO Power 5V	
5	3	9	VSSIO	P	/	IO Ground	
6	4		P23	I	24		T2CAP: Timer2 Capture Pin WKUP3:Port Interrupt/Wakeup MIC: MIC input
7	5	10	P24	I/O	24	GPIO	UARTTX1: UART Data Out(B) AUXL0: Analog MUX left channel input 0
8	6	11	P25	I/O	24	GPIO	UARTRX1: UART Data In(B) AUXR0: Analog MUX right channel input 0
9	7	12	P26	I/O	24	GPIO	IICK1: IIC Clock(B) AUXL1: Analog MUX left channel input 1
10	8	13	P27	I/O	24	GPIO	IICDA1: IIC Data(B) AUXR1: Analog MUX right channel input 1
11			P35	I/O	24	GPIO	ISD Clock Output
12	9		P33	I/O	24	GPIO	EMI_WR_: EMI Port Write enable UARTRX2: UART Data In(C) IICDA2: IIC Data(C)
13	10		P32	I/O	24	GPIO	SPIDIB: SPI Data In(B) UARTTX2: UART Data Out(C) IICK2: IIC Clock(C) SDDATB: SD Data(B)
14			P41	I/O	24	GPIO	ISD Data
15	11		P31	I/O	24	GPIO	SPIDOB: SPI Data Out(B) SDCMDB: SD Command(B)
16			P43	I/O	24	GPIO	ISD Data
17	12		P30	I/O	24	GPIO	SPICLKB: SPI Clock(B) SDCLKB: SD Clock(B)
18			MCLR	I	/	Master Clear, Low Active	MCLR
19	13	14	VPP	P	/	OTP Program Power	Additional Input Only Pin T3CAP: Timer3 Capture Pin
20	14		P17	I/O	16	GPIO	EMID7: EMI Data 7 SPIDOA: SPI Data Out(A)
21	15		P16	I/O	16	GPIO	EMID6: EMI Data 6 SPICLKA: SPI Clock(A)
22	16		P15	I/O	16	GPIO	EMID5: EMI Data 5 SPIDIA: SPI Data In(A)
23	17		P14	I/O	16	GPIO	EMID4: EMI Data 4
24			P42	I/O	24	GPIO	ISD Data
25	18		P13	I/O	16	GPIO	EMID3: EMI Data 3 T2CKIN: Timer2 Clock In
26	19		P12	I/O	16	GPIO	EMID2: EMI Data 2
27	20		P11	I/O	16	GPIO	EMID1: EMI Data 1
28	21		P10	I/O	16	GPIO	EMID0: EMI Data 0
29	22	15	P01	I/O	16	GPIO	High Frequency Oscillator Out ISP Data In
30	23	16	P00	I/O	16	GPIO	High Frequency Oscillator In ISP Clock In

Confidential
The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

31	24		VDDIO	P	/	IO Power 3.3V	
32	25		VSSIO	P	/	IO Ground	
33	26	17	P07	I/O	16	GPIO	ADC7: ADC Channel 7 Input UARTRX0: UART Data In(A) WKUP2:Port Interrupt/Wakeup CS7: Cap sense input7
34			P50	I/O	16	GPIO	JTAG: TCK CS0: Cap sense input0
35	27		P06	I/O	16	GPIO	ADC6: ADC Channel 6 Input UARTTX0: UART Data Out(A) CS6: Cap sense input6
36	28	18	P05	I/O	16	GPIO	ADC5: ADC Channel 5 Input T1CKIN: Timer1 Clock In WKUP1:Port Interrupt/Wakeup T2PWM: Timer2 PWM Output CLKOUT: Internal Clock Output CS5: Cap sense input5
37	29	19	DVDD	P	/	Core Power 1.8V	
38			P51	I/O	16	GPIO	JTAG: TMS CS1: Cap sense input1
39	30		P04	I/O	16	GPIO	ADC4: ADC Channel 4 Input T1CAP: Timer1 Capture Pin CS4: Cap sense input4
40			P52	I/O	16	GPIO	JTAG: TDI CS2: Cap sense input2
41	31		P03	I/O	24	GPIO	ADC3: ADC Channel 3 Input T0CKIN: Timer0 Clock In T1PWM: Timer1 PWM Output CS3: Cap sense input3
42	32	20	P02	I/O	24	GPIO	ADC2: ADC Channel 2 Input T0CAP: Timer0 Capture Pin WKUP0:Port Interrupt/Wakeup ISP Data Out
43	33		P34	I/O	24	GPIO	T3PWM: Timer3 PWM Output LVD: Low voltage detect input
44	34	21	P20	I/O	24	GPIO	SDCLKA: SD Clock(A)
45	35	22	P21	I/O	24	GPIO	SDCMDA: SD Command(A)
46			P40	I/O	24	GPIO	ISD Data
47	36	23	P22	I/O	24	GPIO	SDDATA: SD Data(A)
48			P47	I/O	24	GPIO	ISD Data
49			P46	I/O	24	GPIO	ISD Data
50	37	24	USBDM	I/O	/	USB Negative Data	UARTRX3: UART Data In(D) IICDA3: IIC Data(D)
51	38	25	USBDP	I/O	/	USB Positive Data	UARTTX3: UART Data Out(D) IICK3: IIC Clock(D)
52			P45	I/O	24	GPIO	SPI1CLK: SPI1 Clock
53			P44	I/O	24	GPIO	SPI0DOB: SPI0 Data Out(B)
54	39		WKUP	O	/	RTC WakeUp Input	
55	40	26	LOSCO	O	/	Low Frequency Crystal OSC Onput	
56	41	27	LOSCI	I	/	Low Frequency Crystal OSC Input	
57	42	28	RTCVDD	P	/	RTC Power 1.8V	
58			P53	I/O	16	GPIO	JTAG: TDO
59	43	1	DACVDD	P	/	DAC Power 3.0V	
60			VCOMO	P	/	DAC Reference Out	
61	44	2	VCOM	P	/	DAC Reference	
62	45	3	DACVSS	P	/	DAC Ground	

Confidential
The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

63	46	4	DACL	O	/	DAC Left Channel	
64	47	5	DACR	O	/	DAC Right Channel	

ZHUHAI JIELI TECHNOLOGY CO.,LTD

Confidential
The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.