EECS 3201 Lab 1: Introduction to the DE10-Lite

Objective

In this lab you will:

- Download and install the Quartus Prime Lite software;
- Use Quartus Lite to create a simple Verilog module;
- Configure the module for the DE10-Lite;
- Program the DE10-Lite with your module; and
- Demonstrate that the circuit works correctly.

Reference Material

Altera DE10 manual and resources, available from the course web site.

A. First Quartus project – A simple logic gate

Open Quartus and select the New Project Wizard.

- "What is the name of the project?" – type "lab1" (no space). To keep things organized, you might want to specify a directory for the project; this is optional. Click "Next".
- Select "Empty project" and click "Next"
- Add files – You don't want to add any files yet – just click "Next"
- Family, Device & Board settings:
    - At the top of the page, select the "Board" tab
    - From the "Family:" dropdown, select MAX 10
    - Under "Available boards:" select "MAX 10 DE10 – Lite"
    - Unselect 'Create Top Level Design File'
    - Click "Next"
- EDA Tool Settings – we won't use these settings in this lab – just click "Next"
- Click "Finish" on the summary page

At top left you will see the project navigator. Click the dropdown (it might say "Hierarchy") and select "Files". This should be empty. If you forgot to unselect 'Create Top Level Design File' then a file named "DE10_Lite_Golden_Top.v" will have been added to the project. We will see what this is later but don't need this file for this part, so if it is there right-click on it and select "Remove file from project".

Now we are ready to add a Verilog module to the project. From the menu select "File" -> "New", select "Verilog HDL File", and click OK. From here you can add whatever you want in Verilog; you can also organize your project into different

Verilog files. We are simply going to create a single NAND gate. Add the following Verilog code:

```
module lab1(a,b,c);

      input a,b;
      output c;

      assign c = ~(a & b);

endmodule
```

(What happens in this file? The tilde ~ means logical NOT, and the ampersand & means logical AND. The value of a & b is True if both a and b are True, and False otherwise. Thus, ~(a & b) inverts the result, i.e., False if both a and b are True, and True otherwise. This operation is Not-AND, or NAND.)

(Also notice that every line gets a semicolon except endmodule.)

Save the file. Module names should match the file name, so ensure this file is saved as “lab1.v”.

Now we need to designate the top-level entity in this project, kind of like the main() method in a Java program. In the project navigator, under “Files” right-click on lab1.v and select “Set as top-level entity”.

Finally, we can compile the design to ensure that our Verilog is correct. Below the project navigator you will see the “Tasks” window, which should have “Compilation” selected from the dropdown. (If not, select it.) Double-click on the blue triangle next to “Compile Design” to do a full compilation. If you get a green checkmark, hooray! If not, correct any errors.

Configuring the project for the DE10-Lite

The Verilog module you wrote has two inputs (a, b) and one output (c). Now you must assign them to input and output elements on the DE10-Lite board.

After compiling, Quartus will have found the input and output pins in your project, though they are not assigned to anything. We want to assign the inputs to two of the DE10-Lite’s switches, and the output to one of the DE10-Lite’s LEDs.

From the menu, select Assignments -> Pin Planner, which gives you a map of the MAX 10’s pins. At the bottom you should see a list. The pins a, b, and c should be at the top of this list, and they should not have any assignments. (If you can’t see them, go to the “Filter:” dropdown at the right, and select “Pins: unassigned”.)

The two rightmost switches on the DE10-Lite are labelled PIN_C10 and PIN_C11 (note, the pattern doesn't continue, the next switch isn't PIN_C12!). The rightmost LED on the DE10-Lite is labelled PIN_A8. For a complete list of pins for all accessories on the board, see the DE10-Lite user manual.

For pin a, double-click on the Location box. You can now type PIN_C10 as the location, or you can select it from the dropdown. (You might get an error that the pin is already assigned, or it might be missing from the dropdown list. In this case, go to Assignments -> Remove Assignments, check "Pin, Location & Routing Assignments", click OK, and try again.) Do the same to assign PIN_C11 to b, and PIN_A8 to c.

Re-compile the design. Again, you should get green checkmarks.

Program the DE10-Lite with your design

At the bottom of the Tasks window you should see "Program Device (Open Programmer)". Right-click on that and select "Open" to open the programmer.

Plug your board into any USB port, and click "Hardware Setup …". Under the "Hardware Settings" tab, you should see a list of "available hardware items", which should include "USB-Blaster". On the "Currently selected hardware" dropdown, select "USB-Blaster", then close the setup window.

You should now see a single line representing your output file, along with checkboxes for "Program/Configure", "Verify", etc. If the file is not "lab1.sof" then right-click on this line, select "Change file", navigate to the "output_files" directory, and select "lab1.sof".

Ensure the "Program/Configure" checkbox is checked, and then click "Start".

If the "Progress" bar reaches "100% (Successful)", the device should now be programmed.

Demonstrate the circuit by going through all four possible configurations of the rightmost two switches, showing that the LED only goes out when both switches are "on".

B. Our Logic Gate Version 2

This version will implement the same circuit but use the top-level file from Quartus.

Open Quartus and select the New Project Wizard as before with one exception.

- "What is the name of the project?" – type "lab1v2". A new folder is recommended but not required. Click "Next".
- Select "Empty project" and click "Next"
- Add files – You don't want to add any files yet – just click "Next"
- Family, Device & Board settings:
    - At the top of the page, select the "Board" tab
    - From the "Family:" dropdown, select MAX 10
    - Under "Available boards:" select "MAX 10 DE10 – Lite"
    - **This time select** 'Create Top Level Design File'
    - Click "Next"
- EDA Tool Settings – we won't use these settings in this lab – just click "Next"
- Click "Finish" on the summary page

This time in the hierarchy you will see a file named "DE10_Lite_Golden_Top.v" which will already be the top-level entity. This file is very convenient because it has definitions and assignments for all the pins to the DE10 Lite hardware. Open it and inspect it. You will see many definitions including

```
output    [9:0]   LEDR;
```

which are the 10 red LEDs. You can address the one on the corner as LED[0]. Very convenient and no pin planner needed!

To configure your circuit

- Copy your "lab1.v" file to the directory where you created the project (or confirm it is already there if you used the same directory).
- From the menu select "Project:Add/Remove Files in Project" and add "lab1.v"
- While you do not need to do pin assignment you do need to add your module to "DE10_Lite_Golden_Top.v" at the very bottom (but above `endmodule`) as follows:
-

```
//=======================================
//Structural Coding
//=======================================
      lab1(SW[0],SW[1],LEDR[0]; // add this line

endmodule
```

(What is going on in this file? Above this section are all the declarations of the hardware to be connected (you can comment out the enables for parts you do not use if you like). The line we added will create an instance of your circuit with inputs from SW[0] and SW[1] and output to LEDR[0].)

- Save the edited file, then compile (now two source files), program and test the system as in the previous section.

Deliverables and Evaluation

The implemented circuits must be demonstrated to the TA who will note a completed lab and may ask questions about your implementation. **When implementing the circuit be sure to use the switches and lights to make it easy to demonstrate your circuits.**

Scoring:

- You will receive full marks for submitting the deliverable. Grades might be deducted for minor errors.
- Grades may differ for lab partners if ability to explain and demo the implementation differs substantially

Value:
This lab is worth 2/20 of your total lab score