CS5300 Theory Assignment 2

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1) **True.** If thread A's `read()` call does not overlap any `write()` call to its location, then this call will return the most recently written value into `s_table[`A`]`. If it does, then it will return the new value or the old value since the component registers are regular, which is acceptable. Thus, the construction yields a regular Boolean MRSW register.
2) **True.** Since the SRSW registers are regular, no read call can return a value from either the future or the distant past. We only need to check if it is possible that $R^i \to R^j$ and R^i returns a value later than the value returned by R^j. Since the SRSW registers are regular, this can only happen when both reads overlap a single write.
   Suppose R^i returns the old value. Then, R^j can return either the old or new value, depending on whether the diagonal entry for that thread has been updated by the writer thread, which is acceptable.
   Otherwise, if R^i returned the new value, it would have also updated all the values in its column to reflect the newly read value. Then, R^j would scan its row to find this updated value written by R^i (if not written by the writer thread) and thus return the same value as it has the highest timestamp.
   Hence, the given construction still remains atomic even if SRSW regular registers are used.
3) Obviously, the reader thread cannot read values from the future since the entry in `r_bit` will not be set. Suppose $W^i \to W^j$, with values v_i and v_j being written. If $v_j \leq v_i$, then a read following W^j will return v_j. If $v_j > v_i$, then `r_bit[`v_j`]` is set and `r_bit[`v_i`]` is unset, so a read after W^j will return v_j.
   Suppose $R^i \to R^j$, and R^i returns v_i. Then, the first index with a set bit in `r_bit` is v_i. If no writes overlap with both these reads, then R^j will return v_i or a newly written value whose write overlaps only with R^j. Now, suppose a write W overlaps with both reads and writes a value v_j. If R^i returns v_j, it must mean that v_j is the smallest index with a set bit in `r_bit`. Hence, R^j will also return v_j. This analysis shows that the given construction is an atmoic MRSW register.
4) Clearly, this construction guarantees a safe register, since the returned value is also a 64-bit value. However, if a read operation overlaps with a write operation, then it can read the new upper 32 bits and the old lower 32 bits. This is characteristic of neither regular nor atomic registers. Thus, the strongest property satisfied by this construction is that of a safe register.