S.V. NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
End semester Examination April 2009
B.Tech -II Computer Engineering, IV Semester
Computer Organization

Time: 2 Hour **Max. Marks:** 50

Instruction:

a) Attempt all questions.
b) Support your answer with necessary block diagram.

Q.1 **Justify your Answer** **[8]**

1. If a greater number of devices are connected to the bus then bus performance will suffer.
2. Asynchronous communication interface is function as both transmitter and receiver.
3. For asynchronous data transfer strobe pulse method is batter than handshaking method.
4. The number line in cache is less than the number of main memory blocks.

Q.2 **[A]** Explain the structure of SRAM with diagram. **[3]**

[B] Write down the characteristics of memory system. And explain access methods and physical characteristics in detail. **[5]**

OR

Q.2 **[A]** Explain the structure of DRAM with diagram. **[3]**

[B] Write down the elements of cache design. And explain replacement algorithm and write policy in detail. **[5]**

Q.3 **[A]** What do you mean by Direct memory access? Explain one method for disable the buses. And explain the function of registers that are used in DMA Controller. **[5]**

[B] Explain the Snoopy protocol in detail. **[5]**

OR

Q.3 **[A]** What do you mean by asynchronous data transfer? Explain the methods that are used to achieve asynchronous data transfer in detail also draw required diagrams. **[5]**

[B] Explain Directory protocol in detail and also write down the drawbacks of it. **[5]**

Q.4 An instruction is stored at location 350 with its address filed at location 551.The address filed has the value 400.A processor register R1 contains number 200 .evaluate the effective address if the addressing mode of the instruction is :relative, register indirect, index with R1 as the index register **[3]**

Q.5 Divide (-9) by (-3) in binary two's complement notation using 5 bit word. **[4]**

Q.6 Explain Pentium operation type.

OR

Explain Pentium addressing mode.

Q.7 ADD R1,R2,R3
SUB R4,R5,R1
AND R6,R1,R7
OR R8,R1,R9
XOR R10,R1,R11
To execute this program by using five stage pipeline with 65 ns of each stage .Compare the speedup if we do not consider stall and if we consider stall.

Q.8 Explain register window with Appropriate diagram.

Q.9 **[A]** Explain register organization.

[B] Explain state diagram of instruction cycle

OR

Q.9 **[A]** Explain branch prediction Flow chart.

[B] Write down difference between RISC & CICS.

SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY

B. TECH. II (Semester 3)
Sept. 2011(Mid-Sem Exam)
Data Structures

Time: 1 Hr. **Total Marks: 30**

Q.1 **Answer the following questions:**

1. Explain row major ordering method to store two dimensional arrays. Evaluate the address for the element a[3][4] for the array a[10][10]. **[06]**
2. Write the overflow condition for the circular queue of size N.
3. Describe the advantages and disadvantages of dynamic implementation over static implementation of data structure.

Q.2 **Answer the following questions: [Any One]** **[04]**

1. Write an algorithm to convert postfix expression to the prefix expression.
2. Write an algorithm which reverses the order of elements on stack using the appropriate data structure.

Q.3 Write an algorithm to implement the ascending order stack of N elements. After each insertion of a new value, the lowest element is at the top and the highest element is at the bottom. **[05]**

Q.4 Design the node structure to identify the loop or cycle in the link list. Write the algorithm to identify the loop in the list. **[07]**

Q.5 The descending order link list is created, in which every node can store 3 numbers in descending order. The node can contain one/two/three number(s) but no empty nodes are allowed in the list.

a. Write an algorithm to insert the number in such a way that complete link list is maintained in descending order **[08]**

OR

a. Write an algorithm to delete the number from the link list **[08]**

SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY
B. TECH. II CO (Sem 4)
Feb-2010 (Test 1)
CO204: Computer Organization

Time: 1 Hr. Total Marks: 25

Q. 1 Answer the following: [05]

1) Complete the five classical components of a computer: i- Input Devices, ii - output Devices, iii - ..... , iv - ....., v - ..... .
2) What is the binding software layer between the hardware and application software?
3) Write the important two properties of the fifth generation computers.
4) Subtract (-24) from (-43) using signed-magnitude arithmetic.
5) Is the following a valid alternative definition of overflow in 2's complement arithmetic? "If the exclusive-OR of the carry bits into and out of the leftmost column is 1, then there is an overflow condition. Otherwise, there is not."

Q. 2 Answer the following: [08]

1) Complete the following instruction set design principles:
   i) ..... favors regularity
   ii) Smaller is .....
   iii) Good design demands .....
   iv) Make the ..... fast
2) Write down the equivalent MIPS codes for each of the following instructions.
   i) $8 = $11 – 1
   ii) $10 = 0
3) Write the equivalent C Code for the following MIPS Code. Let $20=x and $21=y.

```
slt $1,$21,$20
bne $1, $0, Loop
```

4) Convert $(02CA)_{16}$ to decimal using Double-Dabble method.

Q. 3 Answer the following: [12]

1) Explain all addressing modes in brief with the example.
2) Registers $10 and $11 contains two signed integers.

```
... # Start point of tracing
        add $4,$0,$10
        jal myproc
        add $12,$0,$2
        add $4,$0,$11
        jal myproc
        add $12,$12,$2
.... # Stop point of tracing
myproc: add $2,$4,$0
        slt $1,$4,$0
        beq $1,$0, pos
        sub $2,$0,$4
  pos: jr $ra
```

   i) Show the tracing of the given program for $10=0xFFFFFFF0 and $11= 0x02468ACE to find out what is calculated into the register $12.
   ii) Write the purpose of myproc function.
3) Draw the Flowchart for the Booth's Algorithm and using this algorithm multiply 23 (multiplicand) by 29 (multiplier) where each number is represented using 6 bits.

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S. V. National Institute of Technology, Surat

B.Tech(II)- CO, 4th Sem.

Exam : Second Mid-Sem , Feb-2008

Theoretical Computer Science

Time : 1 Hours

Q.1 Answer the following questions. Marks : 25

A. 6

	0	1
A	B	A
B	A	C
C	D	B
*D	D	A
E	D	F
F	G	E
G	F	G
H	G	D

DFA to be minimized

a. Draw the table of Distinguishabilities for this automaton.
b. Construct minimum-state equivalent DFA.

OR

A. 6

	0	1
A	B	E
B	C	F
*C	D	H
D	E	H
E	F	I
*F	G	B
G	H	B
H	I	C
*I	A	E

DFA to be minimized

a. Draw the table of Distinguishabilities for this automaton.
b. Construct minimum-state equivalent DFA.

B If $w = a_1a_2a_3\ldots a_n$ and $x = b_1b_2\ldots b_m$ are strings of the same length. Define alt(w,x) to be the string in which the symbol of w and x alternate, starting with w, that is, $a_1b_1a_2b_2\ldots a_nb_n$. If L an M are languages, define alt(L,M) to be the set of strings of the form alt(w,x), where w is any string in L and x is any string in M of the same length, Prove that if L and M are regular , so is alt(L,M). 2

OR

B For the following Expression use the distributive laws to develop two different, simpler, equivalent expressions. 2

$$(0+1)^*1(0+1)+(0+1)^*1(0+1)(0+1)$$

(PTO)

C Suppose h is the homomorphism from the alphabet {0,1,2) to the alphabet {a,b} defined by : h(0) = a, h(1) = ab, and h(2) = ba. 5

1. What is h(0120)
2. If L is the language L(01*2), what is h(L)?

Q.2 Answer The Following Questions **12**

a. Design DPDA for String of properly ended brackets. Eg. {{[ ] } [ ] }

b. Convert the CFG to PDA
S → AB | BC
A→ BA | 0
B→CC | 1
C→ AB | 0

c. Define N(P) for PDA P where N(P) is Acceptence by Empty stack. Prove , If L = $N(P_N)$ for some PDA $P_N = (Q;\sum,T,\partial_N, q_0,Z_0)$, then there is a PDA P_F , such that $L = L(P_F)$.

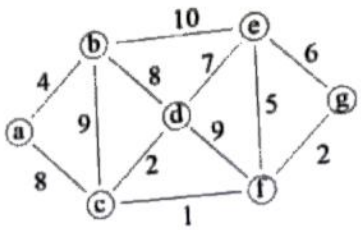
help of an example.

3) Write an algorithm to perform traversal of Binary search tree.

OR

3) Create a binary search tree by inserting following nodes in sequence.
68,85,23,38,44,80,30,108,26,5,92,60
Write inorder, preorder and post order traversal of the above generated Binary search tree.

4) What is a spanning tree? Find the minimum spanning tree for the graph shown in following figure.



5) Define AVL tree. Construct AVL tree for following data
10,20,30,40,50,60,70,80

Computer Engineering Department, S V N I T, Surat.
Mid-Semester Examinations, September 2016

B Tech II (CO) – 3rd semester
Course: Computer Organization (CO201)

Max Marks: 30

Time: 11:0 hrs to 12:30 hrs

Dated 20th Sep 2016

Instructions:
1. Write your B Tech Admission No/Roll No and other details clearly on the answer books while write your B Tech Admission No on the question paper, too.
2. Assume any necessary data but give proper justifications.
3. Be precise and clear in answering the questions.

Q. 1 Answer the following [Any Three]: [06]

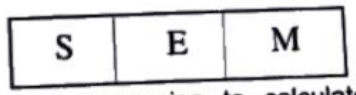
1) Enlist the six levels of computer.
2) Explain the type of 32-bit MIPS processor according to the storage order of data in memory.
3) Explain the need of ISA.
4) Justify the statement: "The number of registers affect the designing of the instruction code bits."
5) Explain how the memory operands affect the performance of the processor.

Q. 2 Answer the following [Any Three]: [09]

1) Write down equivalent MIPS instructions for the followings:
   Array1[1] = 0; //$s1=base address of array Array1
   Temp=1;
2) Enlist the MIPS instruction set principles. Explain the significance of any one design principle.
3) Enlist the different processor architectures type based on the type of operands. Explain advantages of one which is still utilized in present time.
4) Enlist the different types of instruction formats and explain any one of them.

Q. 3 Answer the followings:

1) Draw the hardware implementation and algorithmic diagrams for signed magnitude addition and subtraction in fixed point representation. [04]
2) Consider the following 16-bit register representing the floating point number with mantissa in normalized sign magnitude form, exponent in excess-64 form and base of the system is 2. [03]



   a. What is the relevant expression to calculate the value of the floating point representation?
   b. What is the 16-bit pattern that represent the value (-111.75)10?
   c. What is the second largest value stored in the above register?
3) Consider IEEE 754 single precision format register. What is the value interpreted with the following 32-bit number in the given format? [02]
   1100000111111000.....0
4) Compare for number of add, shift and subtract operations carried out for following numbers using conventional multiplication and Booth multiplication algorithms. [03]
   i) 011001101100 ii) 0111111011011 iii) 01111001
   iv) 111111100 v) 11110001111 vi) 001110011111
5) Perform the following multiplication using Booth Algorithm **[Any One]**: [03]
   i) (-13)*7 ii) (-12)*(-9)

• • •

Formulate the recursive solution and write an algorithm for this problem. Also find out the number of moves required for moving N disks.

a) Justify the need for Prefix or Postfix expressions in computer system. [5]
b) Show the progress of converting the infix expression "2+1-(4-3*1)*3" to its postfix expression.

Consider a process of generating Index from the document in several document processing softwares. Suggest suitable data structure for storing the section and subsection headings and later generate index from it. Explain your answer with illustration. (No need to write algorithm) [3]

A vertical scroll bar commonly located on the far right of a window that allows user to move the window viewing area up and down. Suggest a suitable data structure for simulating the functionality of a vertical scroll bar on the screen. (No need to write algorithm) [3]

Suggest a suitable node structure `struct node` for a Binary Search Tree for storing contents of a dictionary of words. Write a definition of `getnode()` function that creates a node with a given word using C language. [2]

The prototype of a function:

```
struct node *getnode(char *word);
```

Computer Engineering Department, S V N I T, Surat.
Suppl. Examinations, Jan - Feb 2017

B Tech II (CO) – 3rd semester
Course: Computer Organization (CO201)

Dated: 31st Jan 2017 Time: 14:00 hrs to 17:00 hrs Max Marks: 50

Instructions:
1. Write your B Tech Admission No/Roll No and other details clearly on the answer books while write your B Tech Admission No on the question paper, too.
2. Assume any necessary data but give proper justifications.
3. Be precise and clear in answering the questions.

Q. 1[A] Answer the following [Any Five]: **[10]**

1. Explain Computer organization and enlist the layers of the Computer Level Hierarchy.
2. Write Moore's law and explain its usage.
3. Write instructions for which the ALUSrcA control signal must set to 1.
4. What does the WB stage of the pipeline do and why?
5. Using 32-bit IEEE format with 1 sign bit, 8 exponent bits and 23 mantissa bits, show the representation of number -0.968.
6. Assuming single precision IEEE format, what decimal number is represent by this word:
   1 11111101 01100000000000000000000
7. Write the mechanism used by TLB.

Q. 2 Answer the following : [Any Four] **[20]**

1. Explain disadvantages of pipeline processor and describe the pipeline stages with RTL.
2. For the MIPS processor, write the MIPS instructions for the following C code segment:
   for (i=1; i != 10; i++)
   { A[i] = 2*A[i-1]; }
   The value in registers are the base address of arrays A in register $s0 and I in register $s1.
3. Consider the implementations of machine M. There are Four classes of instructions (A, B, C and D) in the instruction set. M has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M Cycles/Instruction Class	Frequency
A	1	50%
B	2	30%
C	3	10%
D	4	10%

   A) Calculate the average CPI for this machine.
   B) Calculate the average MIPS (Million Instructions Per Second) ratings for machine M.

i. Explain the bus types and also explain the handshaking protocol.
ii. Write and explain control hazard and its solutions.

Computer Engineering Department, S V N I T, Surat

Mid Semester Exam, September 2017

B. Tech II (CO) – 3rd semester

Course: Computer Organization (CO201)

Date: 19th September 2017 Time: 11:00 - 12:30 pm Total Marks: 30

Instructions:
1. Be precise and clear in answering the questions.
2. Assume any necessary data but give proper justifications.
3. Write your B. Tech Admission No/Roll No and other details clearly on the answer books while write your B. Tech Admission No on the question paper, too.

Q.1 Answer the following [Any Five]: **[05]**

1) Define computer organization. Describe the benefits of learning.
2) What features are considered by the compiler to compile the high level language program?
3) Describe ISA and explain the elements of instruction.
4) Justify the statement: One of the design principle states that smaller is faster.
5) Differentiate between register-register and load-store architecture.
6) Why registers are used for variables?

Q.2 Answer the following: **[10]**

1) Explain the stored program concept and its model. [02]
2) Explain how CISC processor achieves shorten execution time. [02]
3) Write instructions for 32-bits MIPS processor for the high level language instructions (consider $s0-base address of Ans, $s1-base address of No, $s2-i : [03]

```
for (i=5; i>=0; i--)    Ans[i]=No[i]*16;
```

4) For the Q.2(3), show 32-bits MIPS instruction mnemonics only on the memory location for PC=80000. Provide the calculated memory address component and target address calculation for branch instruction. Note: Ignore calculation of memory address component for jump instruction. [03]

Q.3 Answer the following: **[09]**

1) Perform the arithmetic operations (+42) + (-13) and (-42) – (-13) in binary using signed-2's complement representation for negative numbers using 8-bit. [02]
2) Design a 4-bit combinational circuit of Incrementer using half adders. [03]
3) Explain Booth multiplication algorithm with its flowchart. [04]

OR

3) Show stepwise execution of Booth Multiplication for the given numbers (-9) * (-13) with values of Q_nQ_{n+1}, AC and QR. Consider 5 bit registers for the signed numbers. [04]

Q.4 Answer the following [Any Two]: **[06]**

1) a) Perform Subtraction (20 – 100) by taking the 10's complement of the subtrahend.
   b) Explain overflow by performing the arithmetic operation (+70) + (+80) and (-70) + (-80).
2) If the values of j and k are 3 and 4 respectively. Design an array multiplier using AND gates and adders. Consider j = multiplier bit, k = multiplicand bit.
3) Draw and explain flowchart of signed magnitude data for addition and subtraction.

***

Q. 3 **Answer the following:**

1. For the 4-bit binary multiplication. Fill in the table for the Product, Multiplier and Multiplicand for each step. You need to provide the DESCRIPTION of the step being performed (shift left, shift right, add, no add). The value of M (Multiplicand) is 1010, Q (Multiplier) is initially 1011.

Product	Multiplicand	Multiplier	Description	Step
0000 0000	0000 1010	1011	Initial values	Step 0
.....	.....	.....	.....	.....

2. A) Explain Set Associative concept of Cache memory.

   B) A machine has the physical memory is 2 GB, word size is 32 bits, the block size is 32 bytes, and the cache is 4-way set associative. It can cache 32 KB of physical memory.

   1. How many bits are needed for the Tag, Index and Offset? Show your work.
   2. Describe how the different factors affect the performance of the cache.

3. A) Explain the terms: Virtual Pages, Physical Pages with reference to Virtual Memory.

   B) A machine has 4 GB of RAM for the 32-bit MIPS system and 32-bit virtual address space, 128 MB physical memory and a 8 KB page size. Based on this information, answer the following questions with required work.

   1. How many virtual pages and physical pages are there?
   2. What is the size of the page table, in bytes for one-level page-table design with each page table entry consuming 1 word.

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