Digital Electronics & Logic Design

(EC 207)

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Course Outline

- **PN DIODE AND TRANSITOR** **(04 Hours)**

  PN Diode Theory, PN Characteristic and Breakdown Region, PN Diode Application as Rectifier, Zener Diode Theory, Zener Voltage Regulator, Diode as Clamper and Clipper, Photodiode Theory, LED Theory, 7 Segment LED Circuit Diagram and Multi Colour LED, LASER Diode Theory and Applications, Bipolar Junction Transistor Theory, Transistor Symbols And Terminals, Common Collector, Emitter and Base Configurations, Different Biasing Techniques, Concept of Transistor Amplifier, Introduction to FET Transistor And Its Feature.

- **WAVESHAPING CIRCUITS AND OPERATIONAL AMPLIFIER** **(06 Hours)**

  Linear Wave Shaping Circuits, RC High Pass and Low Pass Circuits, RC Integrator and Differentiator Circuits, Nonlinear Wave Shaping Circuits, Two Level Diode Clipper Circuits, Clamping Circuits, Operational Amplifier OP-AMP with Block Diagram, Schematic Symbol of OP-AMP, The 741 Package Style and Pinouts, Specifications of Op-Amp, Inverting and Non-Inverting Amplifier, Voltage Follower Circuit, Multistage OP-AMP Circuit, OP-AMP Averaging Amplifier, OP-AMP Subtractor.

- **BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS** **(04 Hours)**

  Basic Logic Operation and Logic Gates, Truth Table, Basic Postulates and Fundamental Theorems of Boolean Algebra, Standard Representations of Logic Functions- SOP and POS Forms, Simplification of Switching Functions-K-Map and Quine-Mccluskey Tabular Methods, Synthesis of Combinational Logic Circuits.

- **COMBINATIONAL LOGIC CIRCUIT USING MSI INTEGRATED CIRCUITS** **(07 Hours)**

Course Outline

Binary Parallel Adder; BCD Adder; Encoder, Priority Encoder, Decoder; Multiplexer and Demultiplexer Circuits; Implementation of Boolean Functions Using Decoder and Multiplexer; Arithmetic and Logic Unit; BCD to 7-Segment Decoder; Common Anode and Common Cathode 7-Segment Displays; Random Access Memory, Read Only Memory And Erasable Programmable ROMS; Programmable Logic Array (PLA) and Programmable Array Logic (PAL).

- **INTRODUCTION TO SEQUENTIAL LOGIC CIRCUITS** **(04 Hours)**

  Basic Concepts of Sequential Circuits; Cross Coupled SR Flip-Flop Using NAND or NOR Gates; JK Flip-Flop Rise Condition; Clocked Flip-Flop; D-Type and Toggle Flip-Flops; Truth Tables and Excitation Tables for Flip-Flops; Master Slave Configuration; Edge Triggered and Level Triggered Flip-Flops; Elimination of Switch Bounce using Flip-Flops; Flip-Flops with Preset and Clear.

- **SEQUENTIAL LOGIC CIRCUIT DESIGN** **(06 Hours)**

  Basic Concepts of Counters and Registers; Binary Counters; BCD Counters; Up Down Counter; Johnson Counter, Module-N Counter; Design of Counter Using State Diagrams and Table; Sequence Generators; Shift Left and Right Register; Registers With Parallel Load; Serial-In-Parallel-Out (SIPO) And Parallel-In-Serial-Out(PISO); Register using Different Type of Flip-Flop.

- **REGISTER TRANSFER LOGIC** **(04 Hours)**

  Arithmetic, Logic and Shift Micro-Operation; Conditional Control Statements; Fixed-Point and Floating-Point Data; Arithmetic Shifts; Instruction Code and Design Of Simple Computer.

- **PROCESSOR LOGIC DESIGN** **(03 Hours)**

  Processor Organization; Design of Arithmetic Logic Unit; Design of Accumulator.

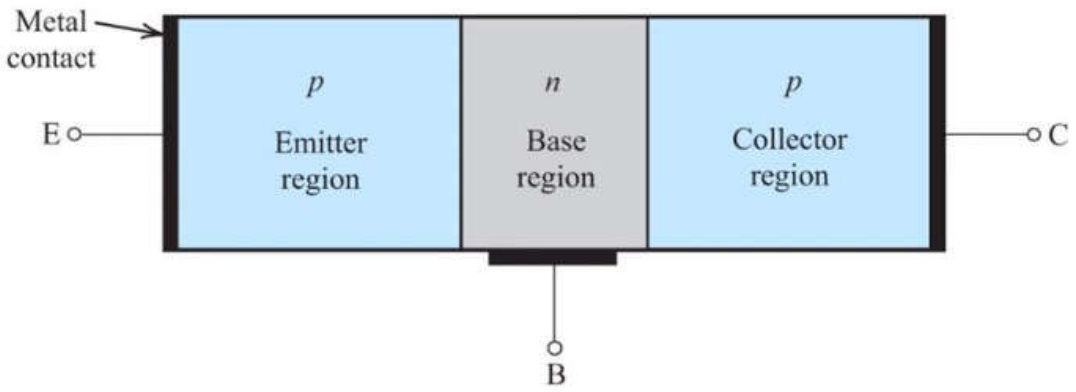
- **CONTROL LOGIC DESIGN** **(04 Hours)**

  Control Organization; Hard-Wired Control; Micro Program Control; Control Of Processor Unit; PLA Control.

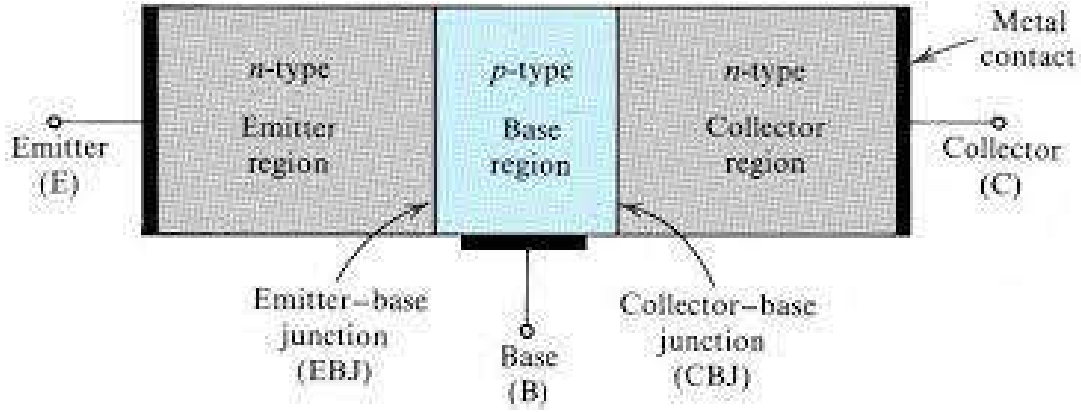
Course Text and Materials

1. Schilling Donald L. and Belove E., "Electronics Circuits- Discrete and Integrated", 3rd Ed., McGraw-Hill, 1989, Reprint 2008.
2. Millman Jacob, Halkias Christos C. and Parikh C., "Integrated Electronics", 2nd Ed., McGraw-Hill, 2009.
3. Taub H. and Mothibi Suryaprakash, Millman J., "Pulse, Digital and Switching Waveforms", 2nd Ed., McGraw-Hill, 2007.
4. Mano Morris, "Digital Logic and Computer Design", 5th Ed., Pearson Education, 2005.
5. Lee Samual, "Digital Circuits and Logic Design", 1st Ed., PHI, 1998.

Bipolar Junction Transistor



PNP



NPN

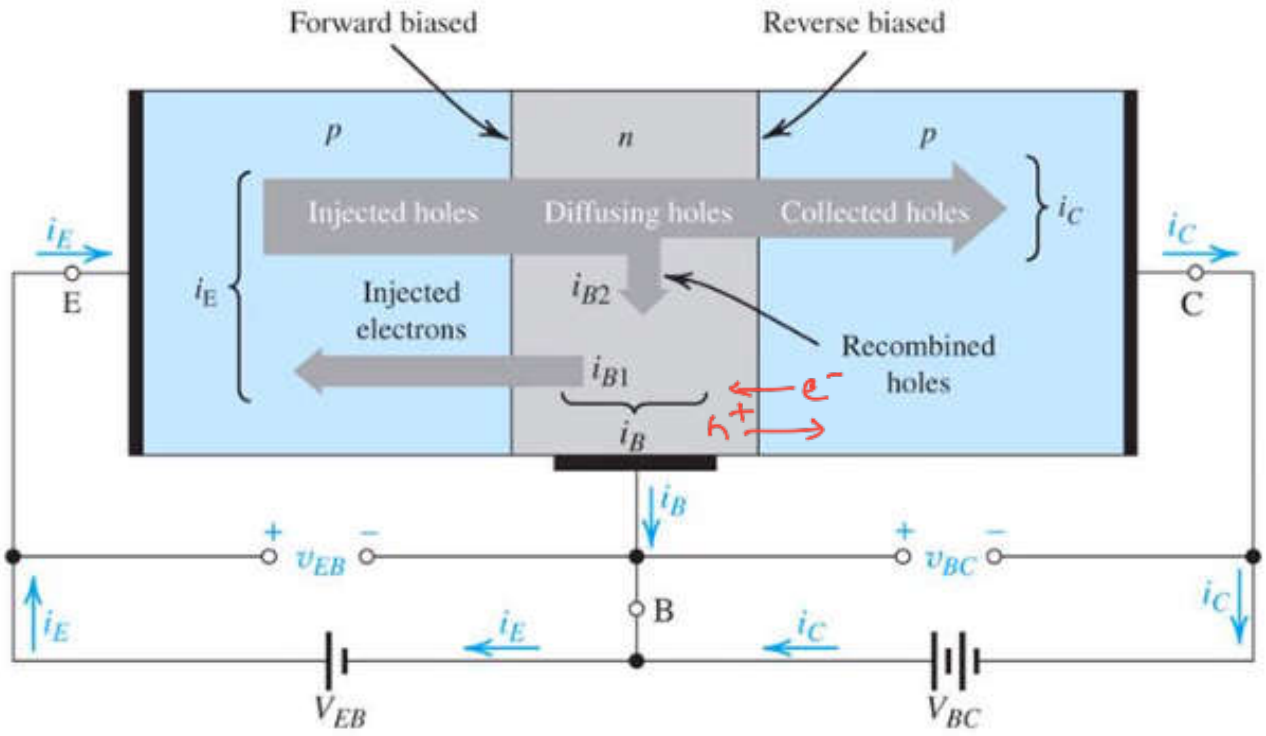
Modes of Operation

Mode	E-B Junction	C-B Junction
Active	Forward	Reverse
Saturation	Forward	Forward
Cut-off	Reverse	Reverse

Active Mode: Transistor as an amplifier

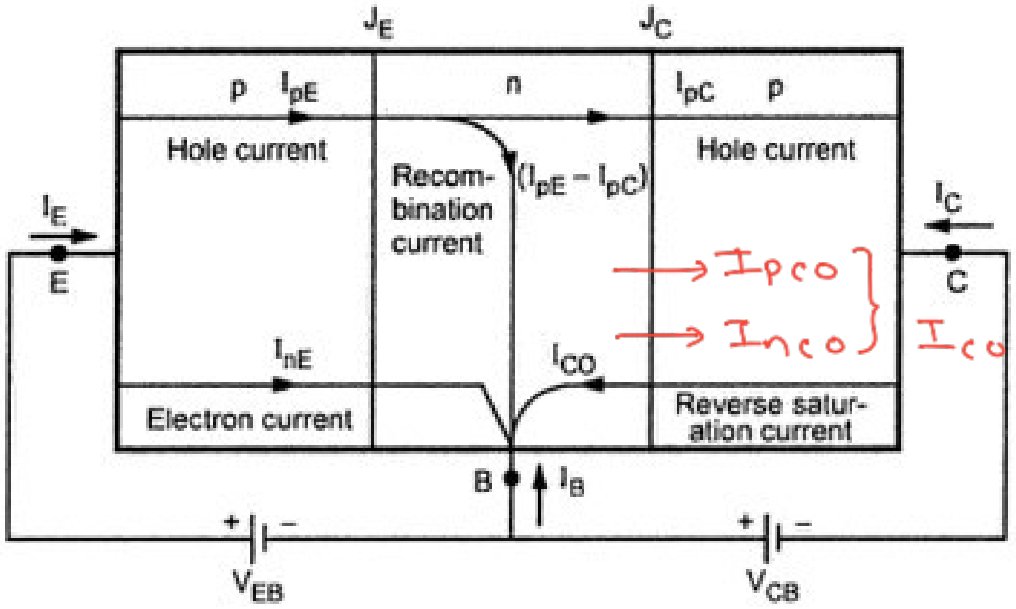
Cutoff, and Saturation: Switching Operation

Transistor Operation in Active Mode:



$$I_E = I_B + I_C$$

Transistor Operation in Active Mode:



Current Components:-

$I_{CO} = I_{pCO} + I_{nCO}$

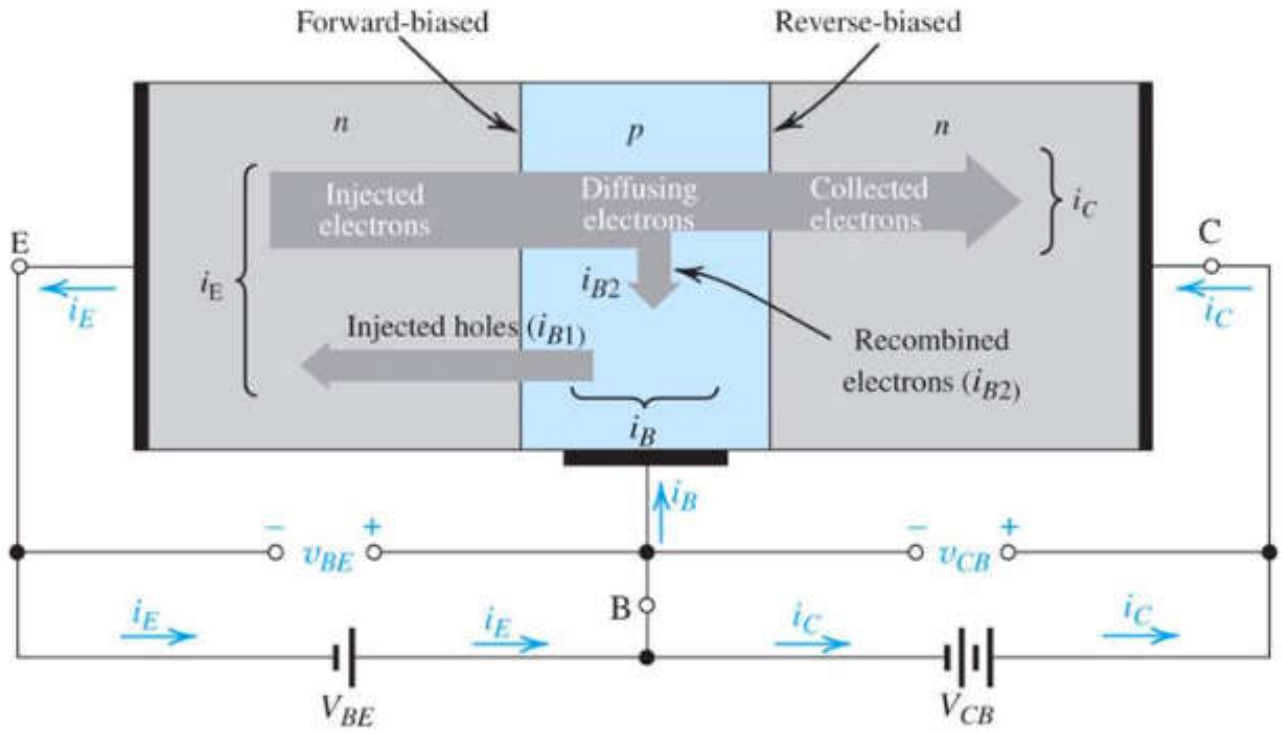
$I_E = I_B + I_C$

$I_C = \alpha I_E + I_{CO}$

$\alpha = \frac{I_C}{I_E}$ $I_{CO} \rightarrow$ Small

$\alpha \rightarrow (0.95 - 0.99)$

Transistor Operation in Active Mode:

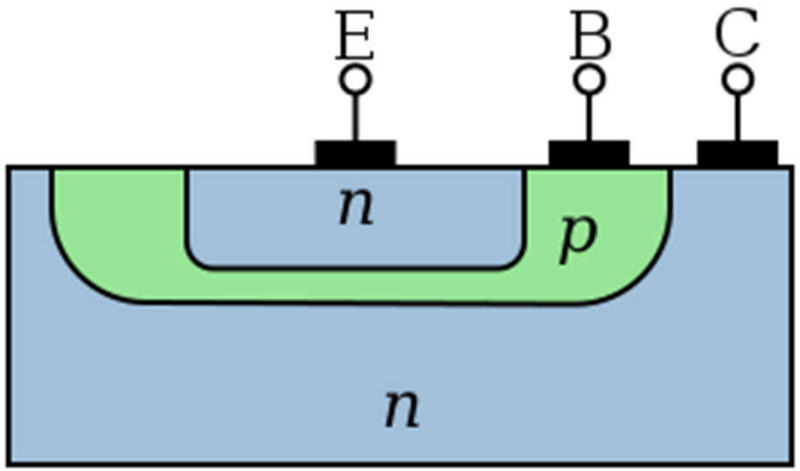


$I_E = I_B + I_C$

Direction of current is reversed.

Bipolar Junction Transistor

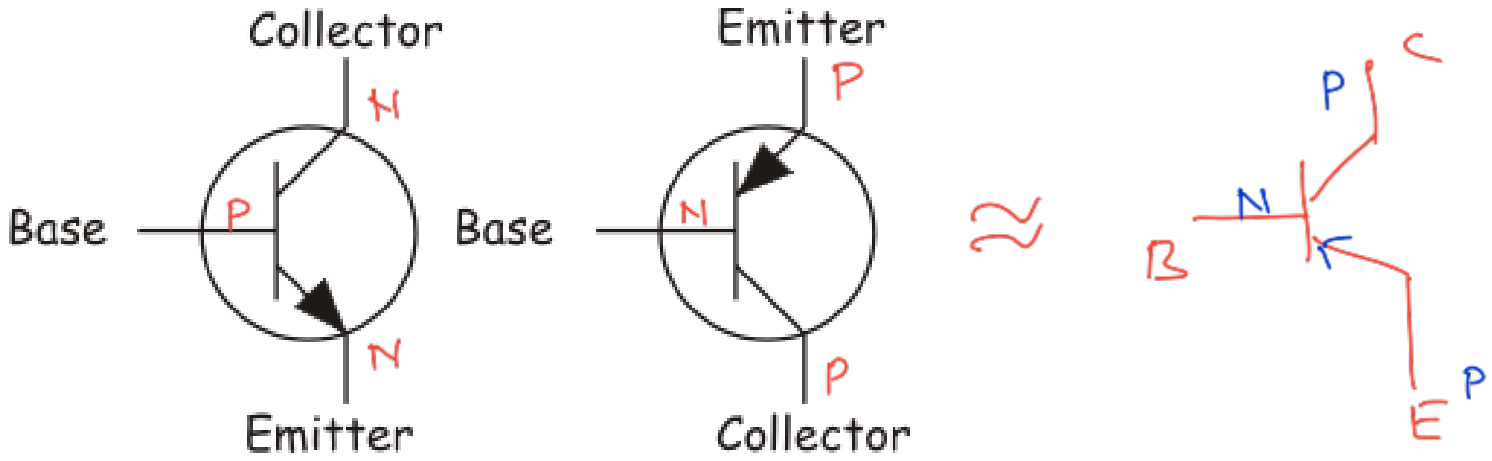
Physical Structure of Transistor:



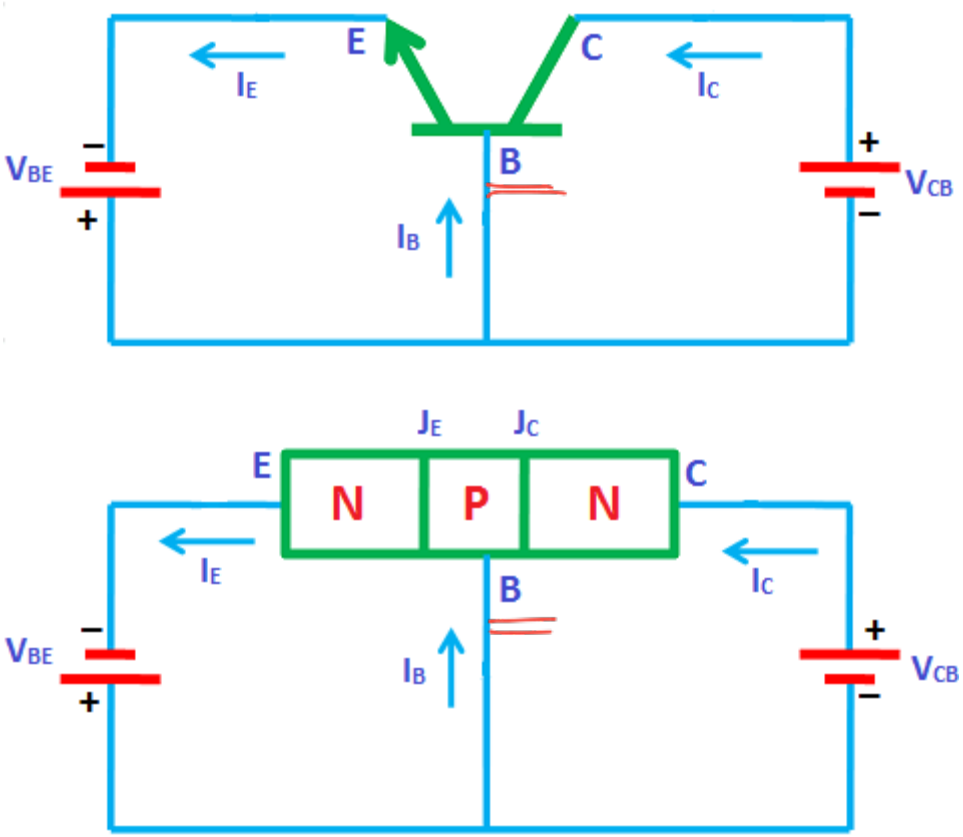
Planar Technology.

Bipolar Junction Transistor

Schematic Symbols of BJT:



Transistor Configuration: CB



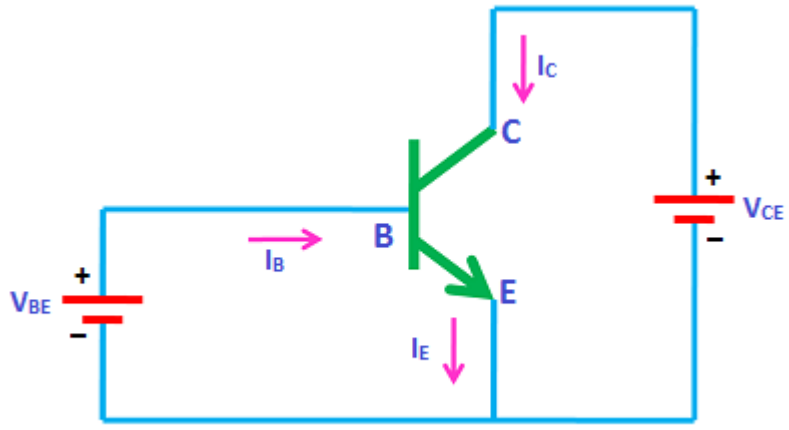
$$I_E = I_B + I_C$$

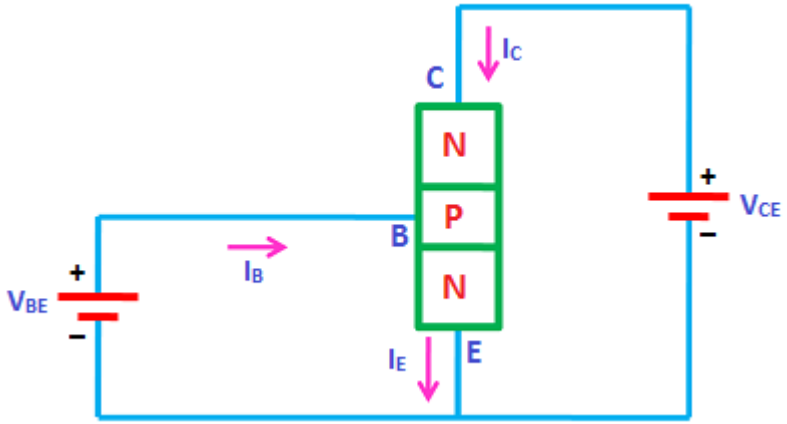
$$I_C = \alpha I_E + I_{CO}$$

$$\alpha = \frac{I_C}{I_E}$$

$\alpha \rightarrow (0.95 - 0.99)$

Transistor Configuration: CE





$$I_E = I_B + I_C \quad \text{—— (1)}$$

$$I_C = \alpha I_E + I_{CO} \quad \text{—— (2)}$$

from eqⁿ (1) & (2)

$$I_C = \alpha(I_B + I_C) + I_{CO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CO}$$

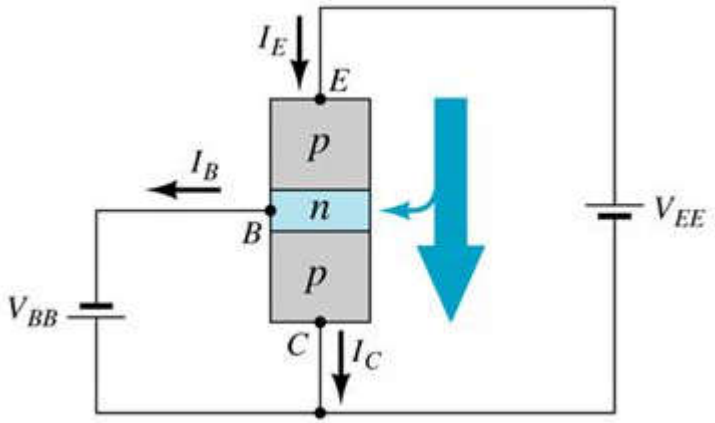
$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CO}$$

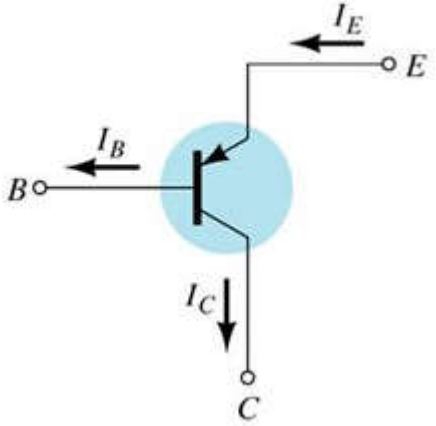
$$\boxed{I_C = \beta I_B + (1+\beta) I_{CO}}$$

$$\left\{ \beta = \frac{I_C}{I_B} = \left(\frac{\alpha}{1-\alpha}\right) \right.$$

$$\left. \beta + 1 = \left(\frac{1}{1-\alpha}\right) \right\}$$

Transistor Configuration: CC





$$I_E = I_B + I_C \quad \text{---} \quad (1)$$

$$I_C = \alpha I_E + I_{CBO} \quad \text{---} \quad (2)$$

from eqn (1) & (2)

$$I_E = I_B + (\alpha I_E + I_{CBO})$$

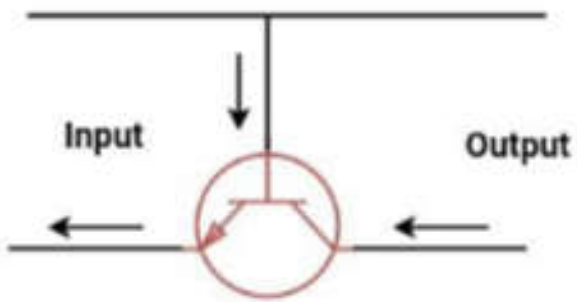
$$I_E(1-\alpha) = I_B + I_{CBO}$$

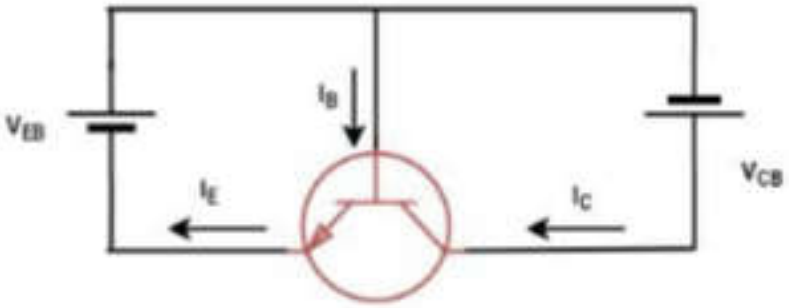
$$I_E = \left(\frac{1}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$$

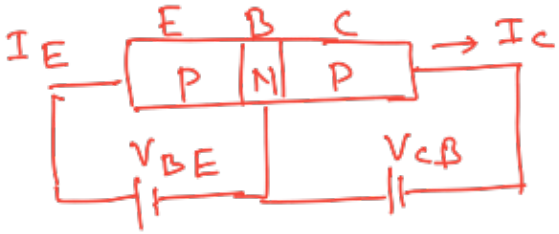
$$\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$$

$$\left\{\gamma = \frac{1}{1-\alpha}\right\}$$

Characteristics of BJT: CB







I/p characteristics:-

I_E Vs V_{EB} (V_{CB} → constant)

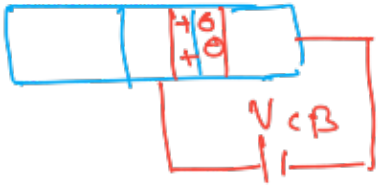
→ By varying V_{CB}, family of curves will be observed.

o/p. characteristics:-

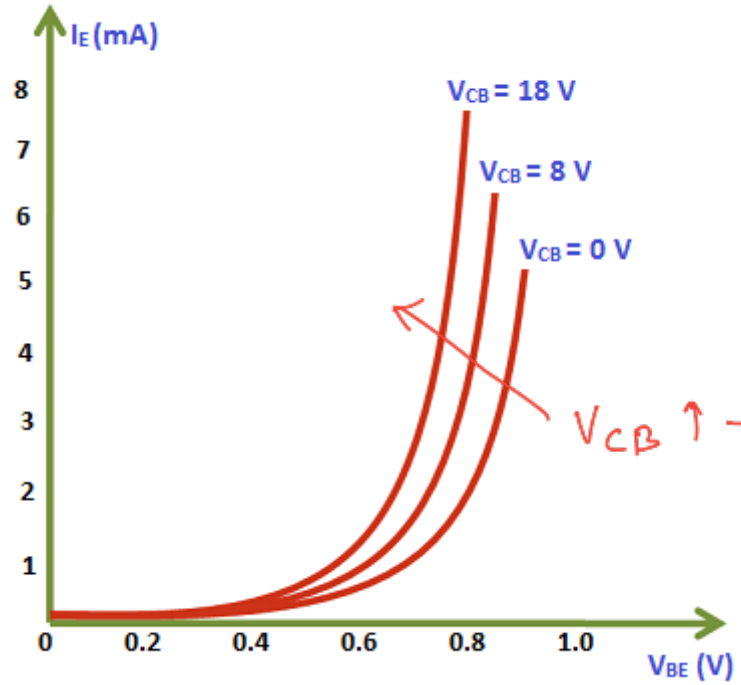
I_C Vs V_{CB} (I_E → Constant)

→ family of curves will be observed with varying I_E.

Input Characteristics: CB



{ Early effect (or) Base width modulation

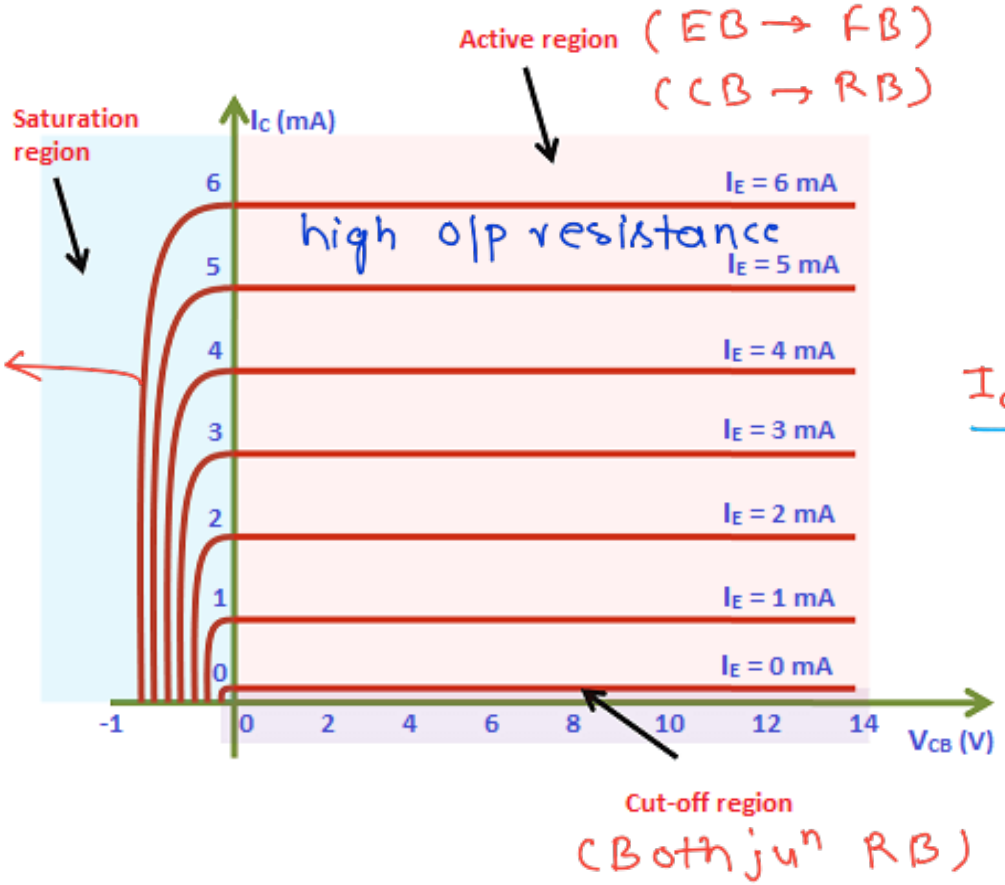


DKl → Depletion Klidth

V_{CB} ↑ → I_E ↑

V_{CB} ↑ → DKl ↑ → Concentration gradient ↑ → More diffusion current ↑

Output Characteristics: CB



As $V_{CB} \rightarrow$ FB
→ Reverse current w.r.t tradiational current will flow.
→ Makes $I_E \rightarrow$ zero for certain V_{CB}.

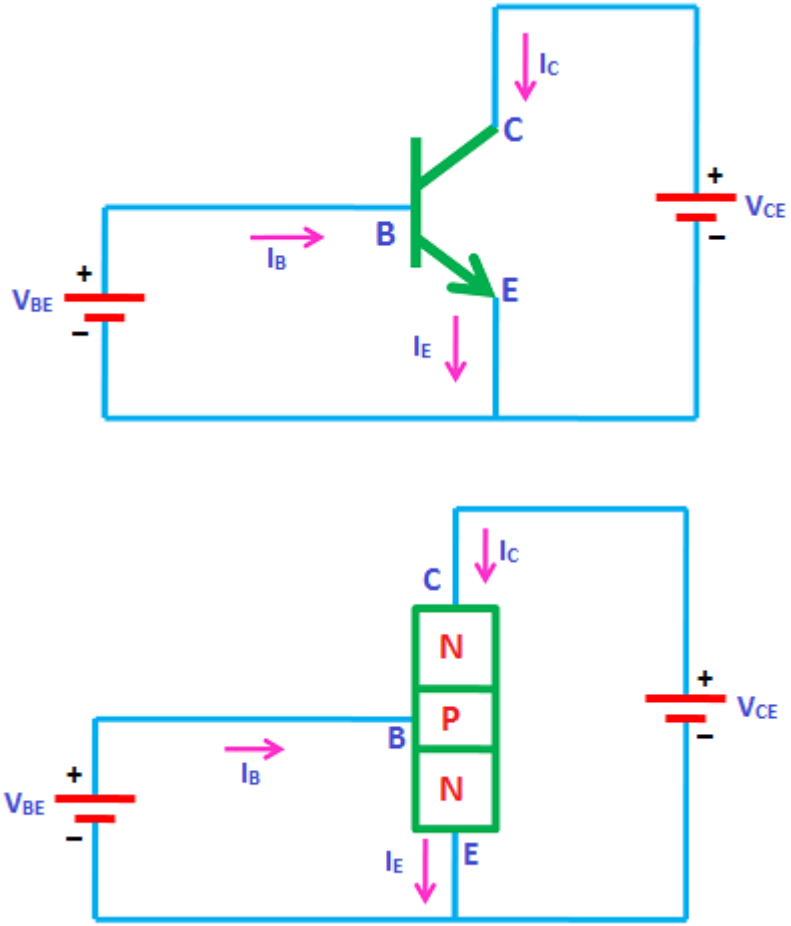
$\alpha = I_c / I_E$

$I_{CO} \rightarrow I_{CBO}$

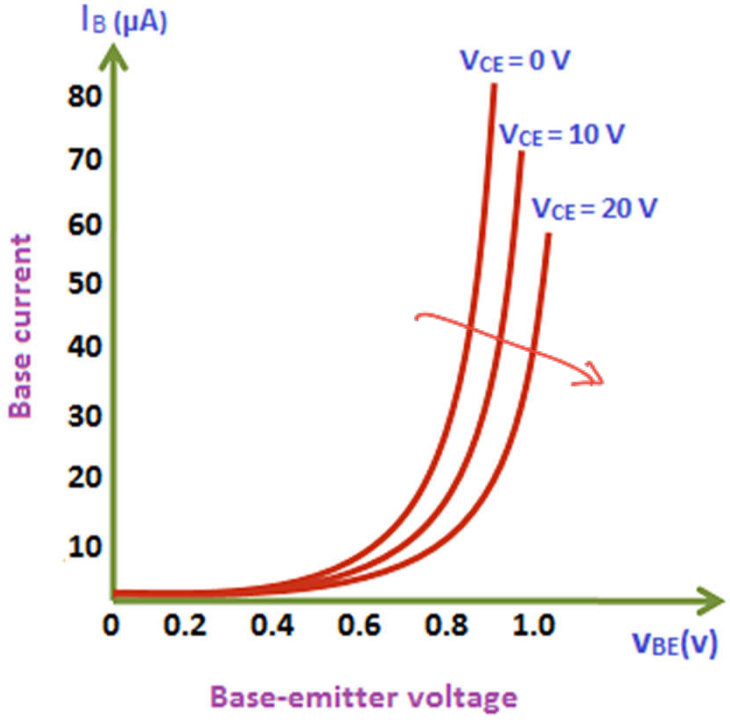
$I_c = \alpha I_E + I_{CBO}$

I_{CBO} → collector to base current when emitter is open.

Transistor Configuration: CE



Transistor Configuration: CE



I/P characteristics CE configuration

$V_{CE} = V_{CB} + V_{BE}$

→ As V_{CE} ↑ → V_{CB} ↑

→ V_{CB} ↑ → DW ↑ → I_B ↓

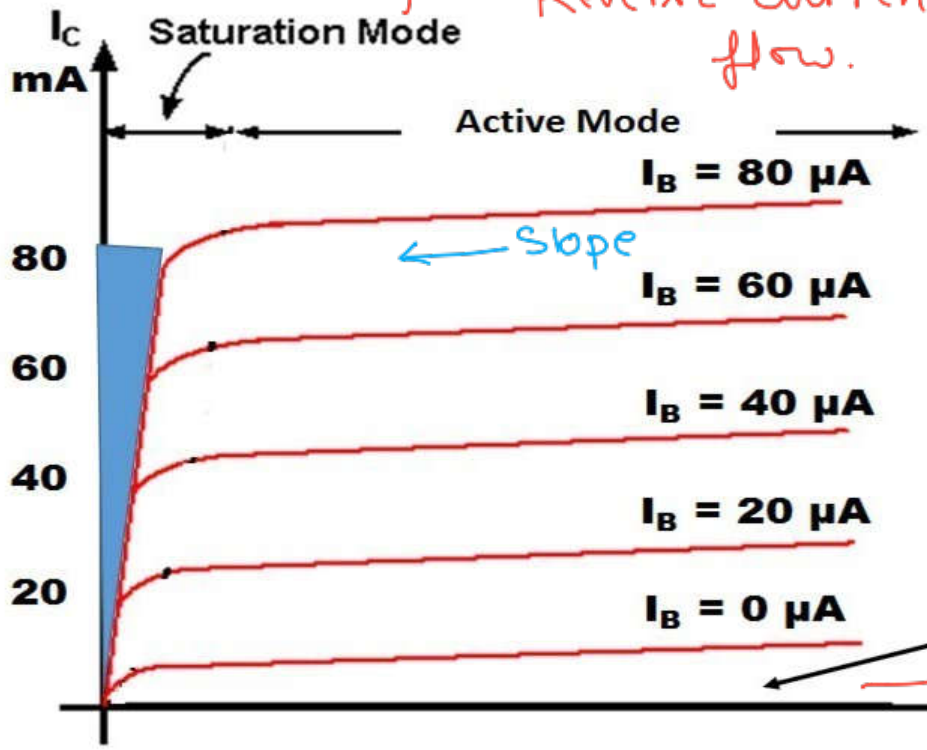
↓

Because of less recombination

→ As V_{CE} ↑ → I_B ↓

DW → Depletion Width.

Transistor Configuration: CE



→ $V_{CE} = V_{CB} + V_{BE}$
Reverse current will flow.

Slope

β is not constant
→ as V_{CE} ↑ → V_{CB} ↑ → I_B ↑ → β ↑

→ as V_{CE} ↑ → β ↑

$\beta = \frac{I_C}{I_B}$

→ large leakage current.

Transistor Configuration: CE

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$\rightarrow \quad (1+\beta) I_{CBO} = I_{CEO}$$

$$I_C = \beta I_B + I_{CEO}$$

$$\left\{ (1+\beta) I_{CBO} = \left(\frac{1}{1-\alpha}\right) I_{CBO} = I_{CEO} \right\}$$

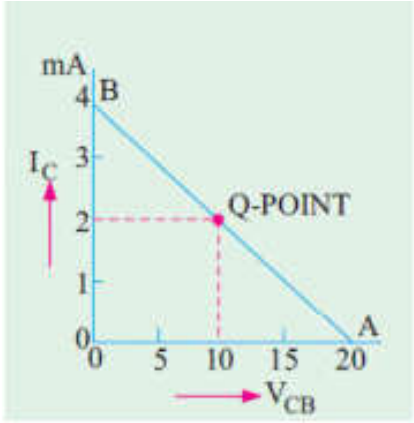
for $\alpha = 0.996 \rightarrow \beta = 249$

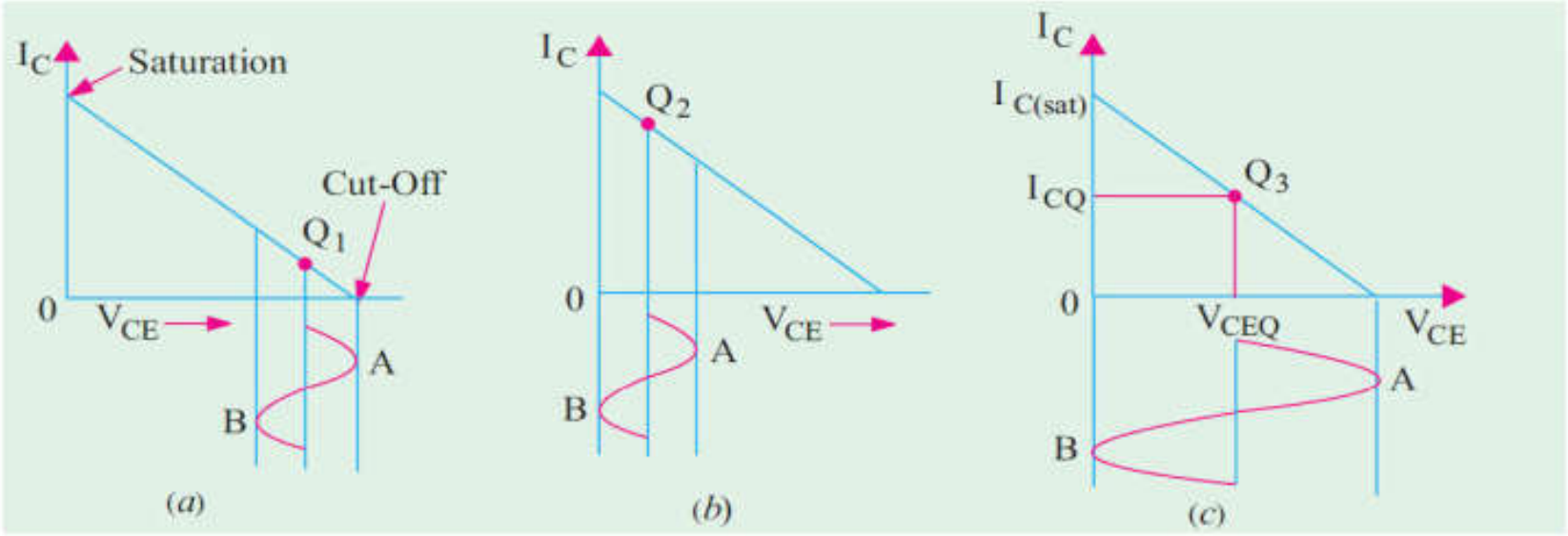
→ due to large value of β, leakage current is large in CE configuration.

Transistor Configuration: Comparison

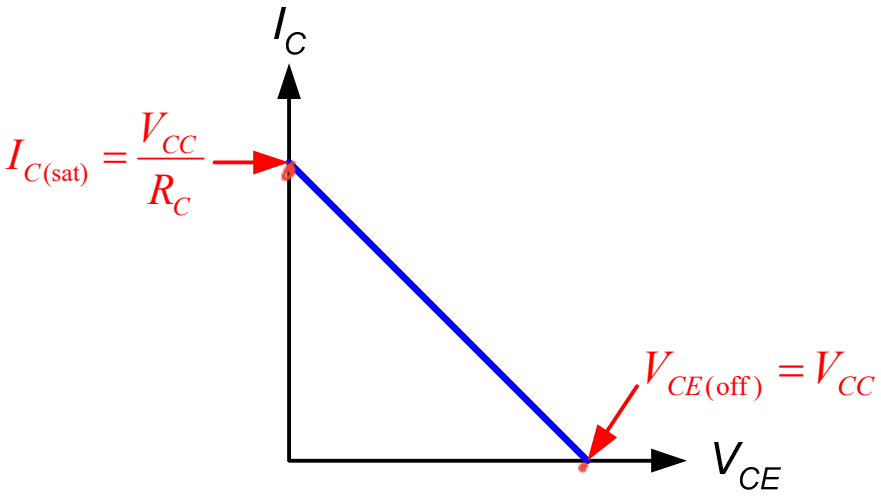
Transistor Configuration Summary Table			
Transistor Configuration	**Common Base**	**Common Collector (Emitter Follower)**	**Common Emitter**
Voltage Gain	High	Low	Medium
Current Gain	Low	High	Medium
Power Gain	Low	Medium	High
Input / Output Phase Relationship	0°	0°	180°
Input Resistance	Low	High	Medium
Output Resistance	High	Low	Medium

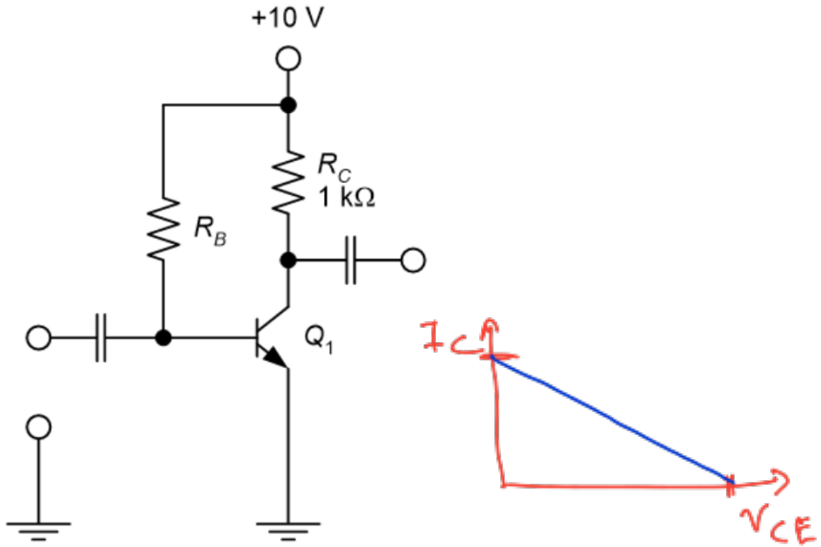
Transistor Biasing

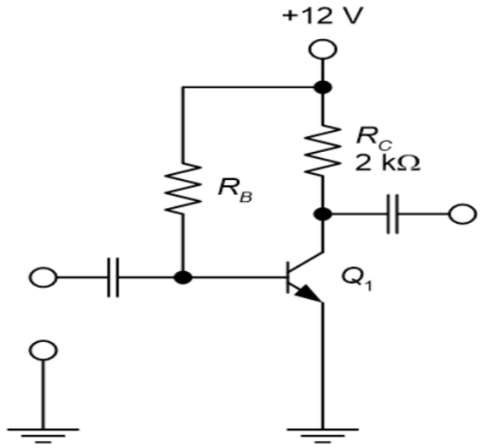


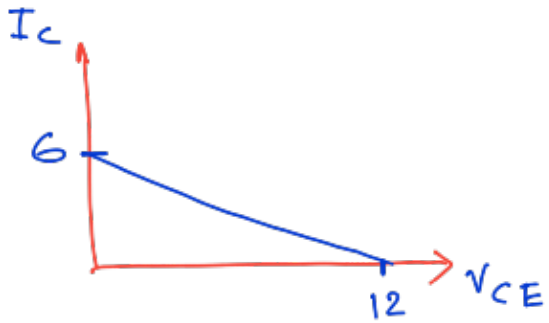


Transistor Biasing (Load Line)









Transistor Biasing (Stability Factor)

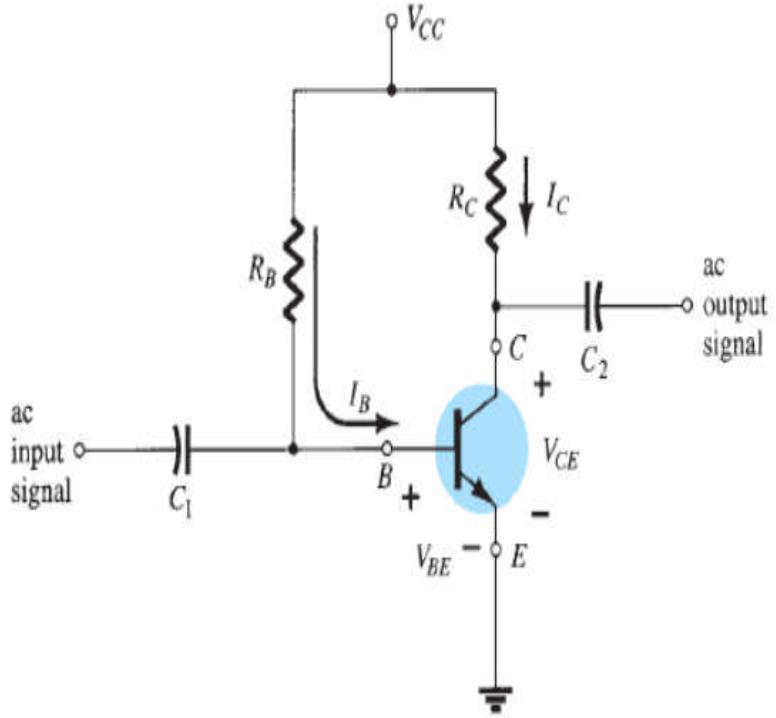
$$S = \frac{dI_C}{dI_{CO}}$$

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

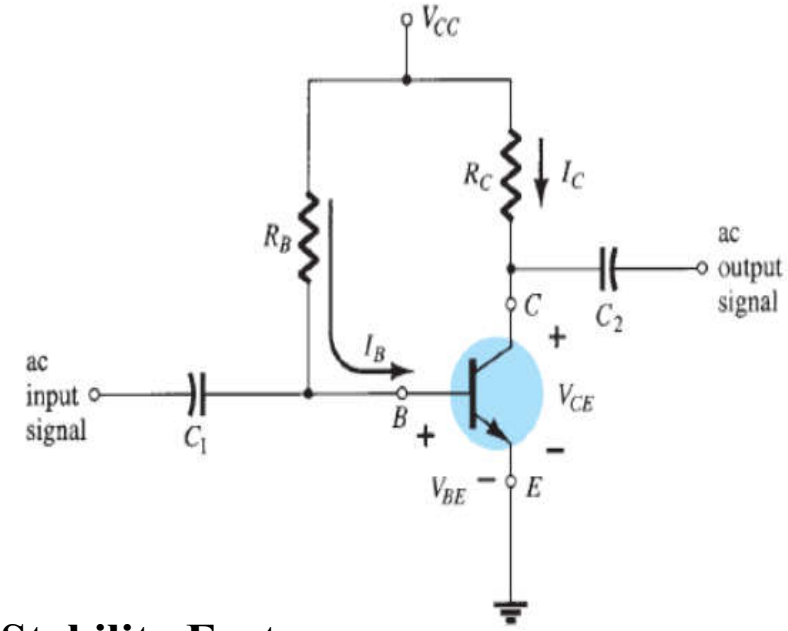
$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S}$$

$$S = \frac{\beta + 1}{1 - \beta \left(\frac{dI_B}{dI_C} \right)}$$



Since $\frac{dI_{CO}}{dI_C} = \frac{1}{S}$

Transistor Biasing (Fixed Biasing)



$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_C$$

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{BE} = V_B - V_E$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B$$

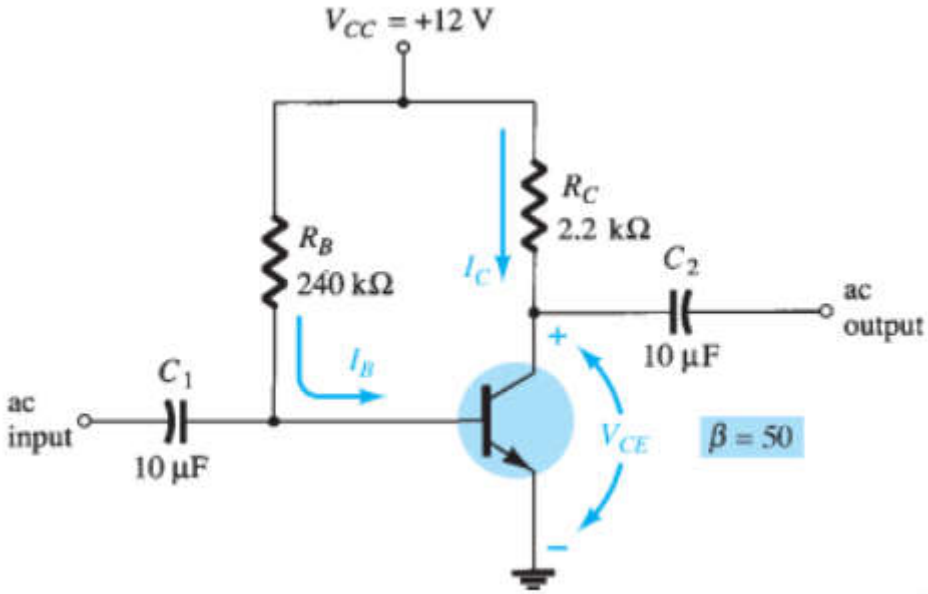
Stability Factor

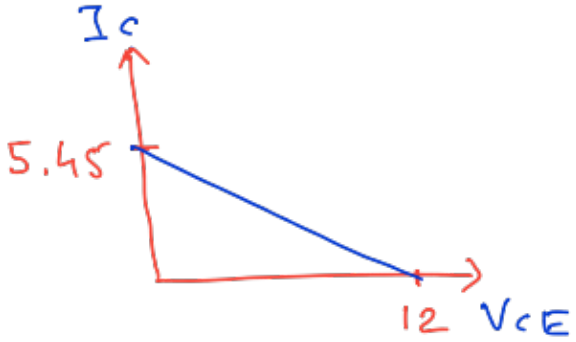
$$S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

$$S = \beta + 1$$

$$\frac{dI_B}{dI_C} = 0$$

Transistor Biasing (Fixed Biasing)





Draw the load line, and find:

a) I_B and I_C
b) V_{CE}
c) V_B and V_C
d) V_{BC}

Ans:- $I_B = 47.08\ \mu A$

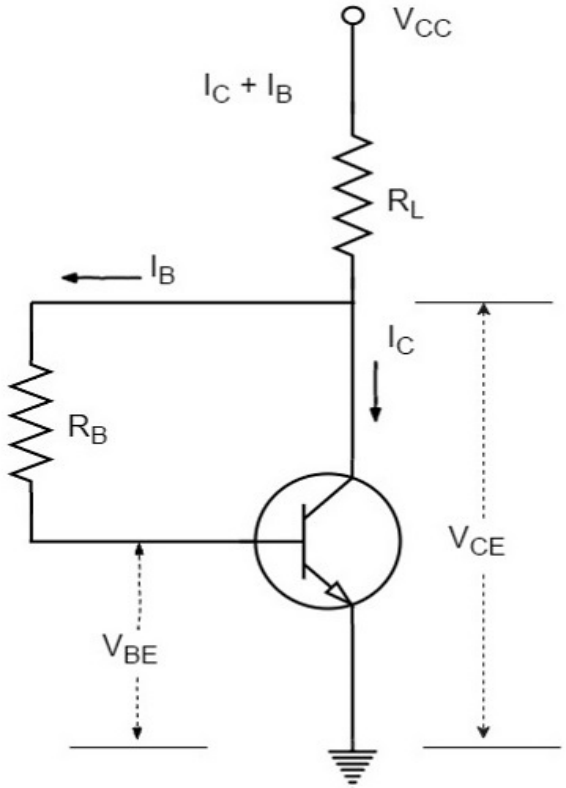
$I_c = 2.35\ mA$

$V_{CE} = 6.38\ V$

$V_c = 6.38\ V$

$V_{BC} = -6.13\ V$

Transistor Biasing (Collector to base bias)



eqn :- $V_{CC} - (I_B + I_C)R_L - I_B R_B - V_{BE} = 0$

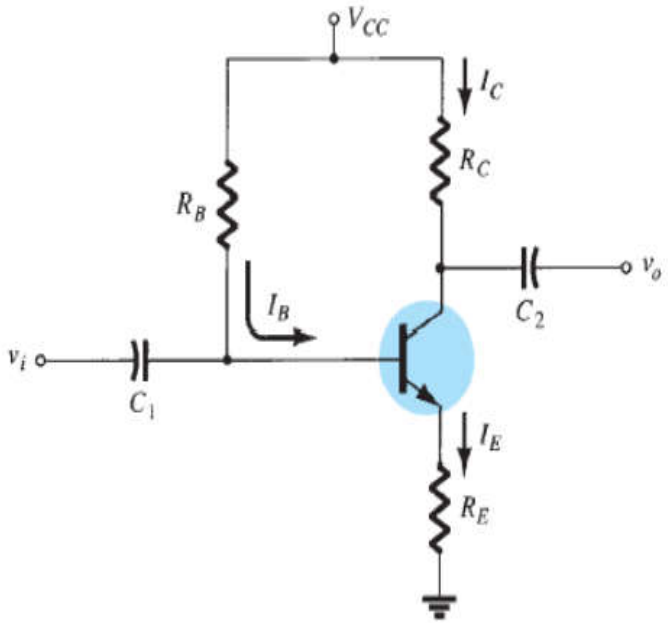
$$I_B = \frac{V_{CC} - V_{BE} - I_C R_L}{R_L + R_B}$$

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_L}{I_B}$$

$$\frac{dI_B}{dI_C} = -\frac{R_L}{R_L + R_B}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_L}{R_L+R_B}\right)}$$

Transistor Biasing (Emitter Bias)



$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}}$$

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

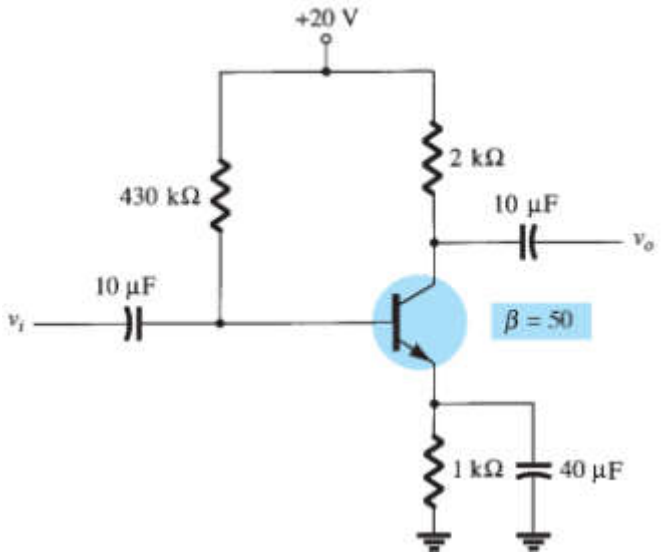
$$I_E \cong I_C$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

$$\boxed{V_E = I_E R_E}$$

$$V_{CE} = V_C - V_E$$

Transistor Biasing (Emitter Bias)



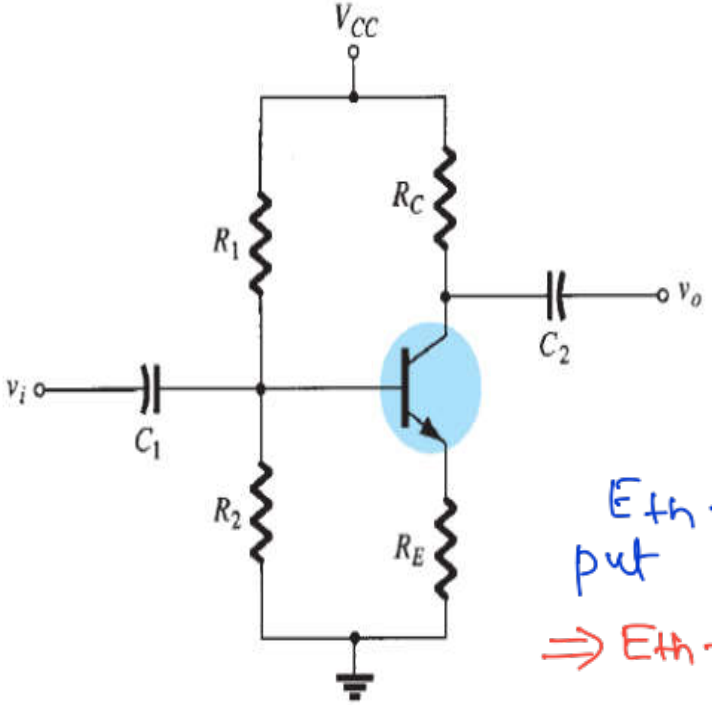
Ans:-

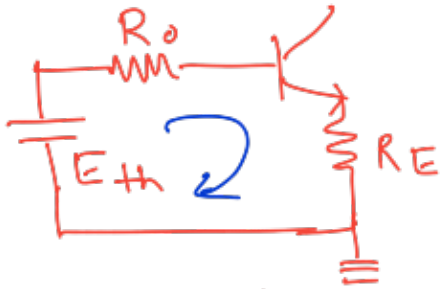
$I_B = 40.1\ \mu A$
$I_C = 2.01\ mA$
$V_{CE} = 13.97\ V$
$V_C = 15.98\ V$
$V_B = 2.01\ V$
$V_{BC} = -13.27\ V$

Draw the load line, and find:

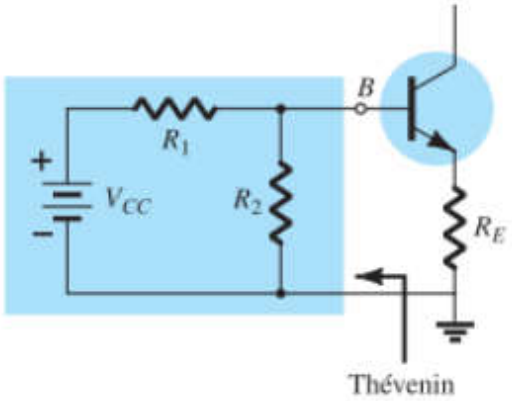
a) I_B and I_C
b) V_C, V_E, V_{CE}
c) V_B and V_C
d) V_{BC}

Transistor Biasing (Voltage Divider Bias)





$\approx$



$R_0 = R_1 \| R_2$

$E_{th} = V_{cc} \cdot \frac{R_2}{R_1 + R_2}$

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$E_{th} - I_B R_0 - V_{BE} - I_E R_E = 0$

put $I_E = I_B + I_c$, $I_c = \beta I_B$

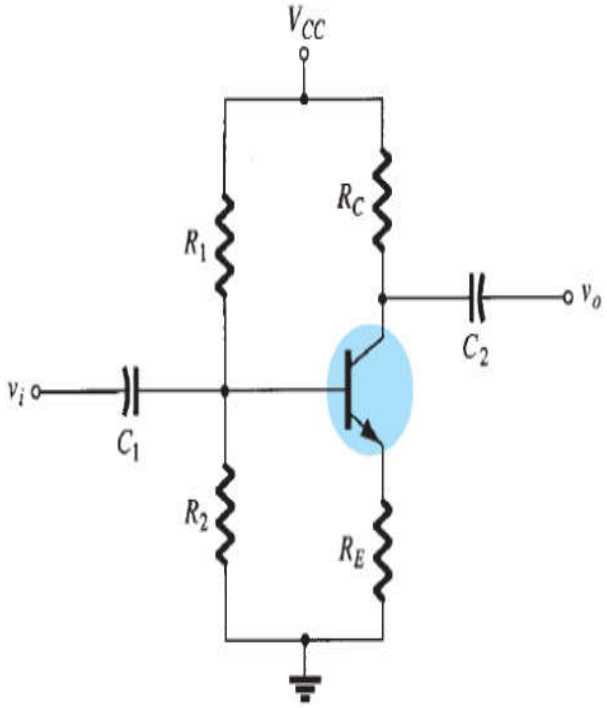
$\Rightarrow E_{th} - I_B R_0 - V_{BE} - I_B(\beta+1)R_E \Rightarrow$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$S = \frac{(\beta+1)(R_0+R_3)}{R_0+R_E+\beta R_E} = (\beta+1) \times \frac{1+\frac{R_0}{R_E}}{\beta+1+\frac{R_0}{R_E}} = (\beta+1) \times \frac{1}{\beta+1} = 1$$

Transistor Biasing (Voltage Divider Bias)



$$E_{th} - I_B R_0 - V_{BE} - (I_B + I_C) R_E = 0 \quad \text{—①}$$

taking derivative w.r.t. I_C

$$0 - \frac{dI_B}{dI_C} R_0 - 0 - \frac{dI_B}{dI_C} R_E - R_E = 0$$

$$\Rightarrow \left\{ \frac{dI_B}{dI_C} = \frac{-R_E}{R_0 + R_E} \right\}$$

$$S = \frac{1+\beta}{1 - \beta\left(\frac{-R_E}{R_0+R_E}\right)} = \frac{(1+\beta)\left[1 + (R_0/R_E)\right]}{1 + \beta + \frac{R_0}{R_E}}$$

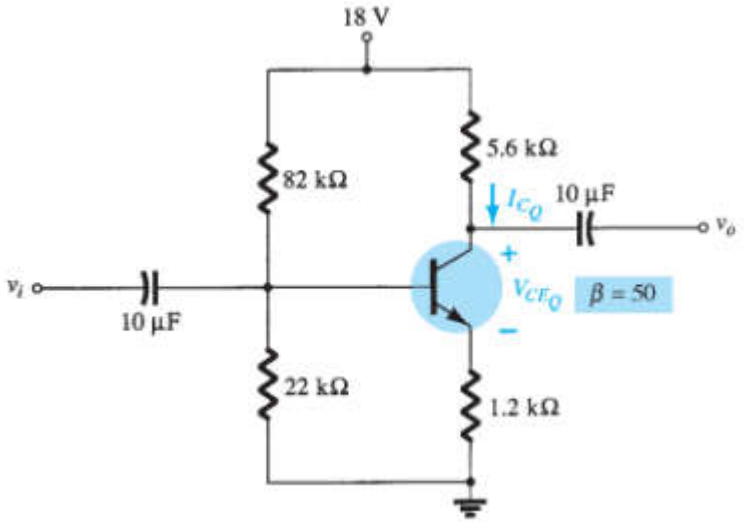
if $(R_0/R_E) \rightarrow$ small

$$S = \frac{(1+\beta)}{(1+\beta)} \simeq 1$$

$$S = \frac{(\beta+1)(R_0+R_3)}{R_0+R_E+\beta R_E} = (\beta+1) \times \frac{1+\frac{R_0}{R_E}}{\beta+1+\frac{R_0}{R_E}} = (\beta+1) \times \frac{1}{\beta+1} = 1$$

best stability factor.

Transistor Biasing (Voltage Divider Bias)



Ans:-

$I_B = 39.6\ \mu A$

$I_C = 1.98\ mA$

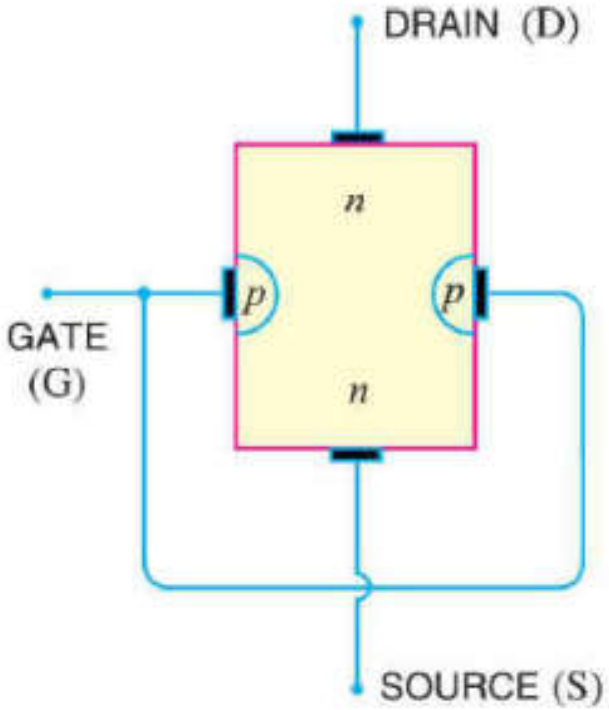
$V_{CE} = 5.45\ V$

Draw the load line, and find:

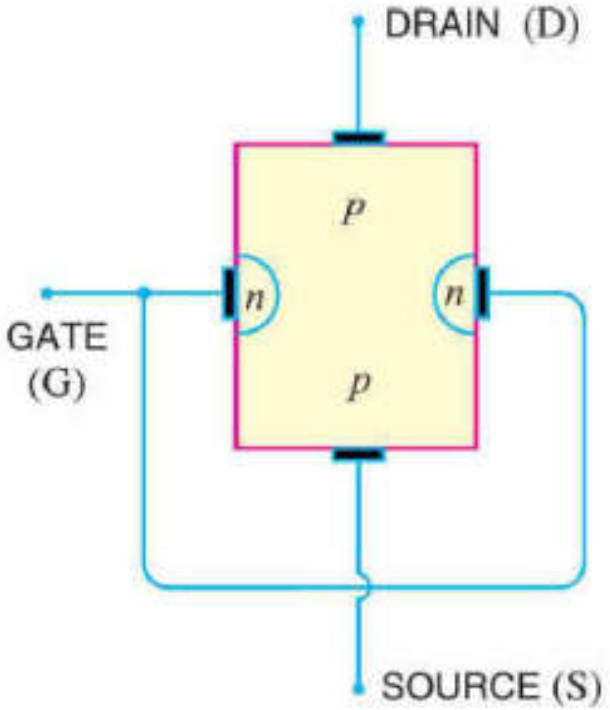
a) I_B and I_C
b) V_C, V_E, V_{CE}
c) V_B and V_C
d) V_{BC}

Field Effect Transistor

- It consists of a p-type or n-type silicon bar comprising of two pn-junctions
- Bar forms the conducting channel for the charge carriers
- If the bar is n-type: N-Channel JFET, if it is p-type: P-Channel JFET

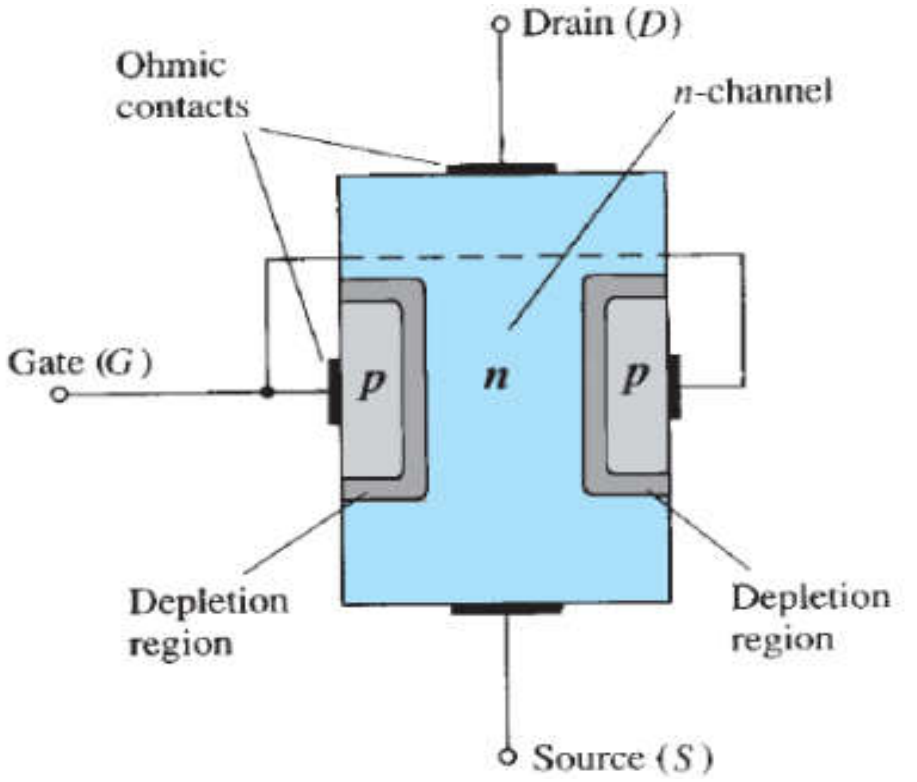


n-Channel JFET



p-Channel JFET

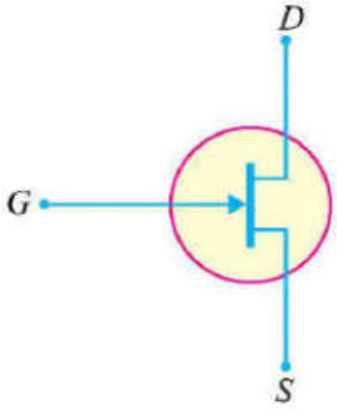
Field Effect Transistor



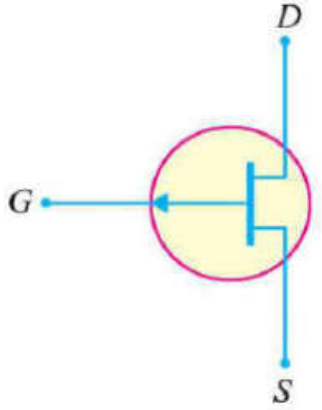
control variable

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

constants

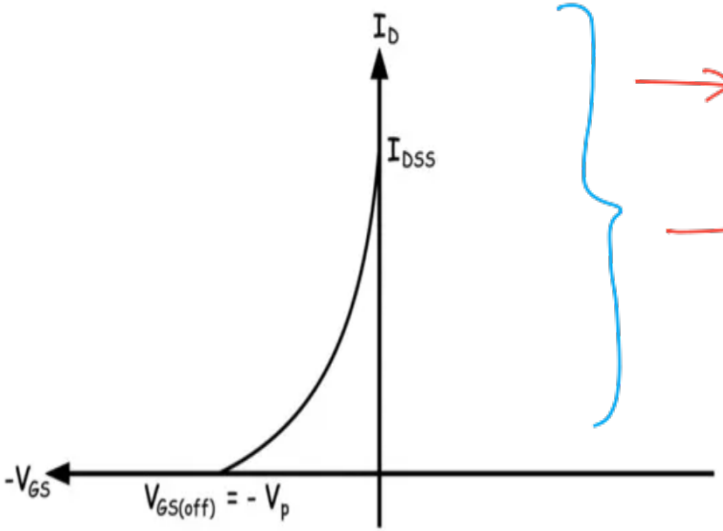


n-Channel *JFET*



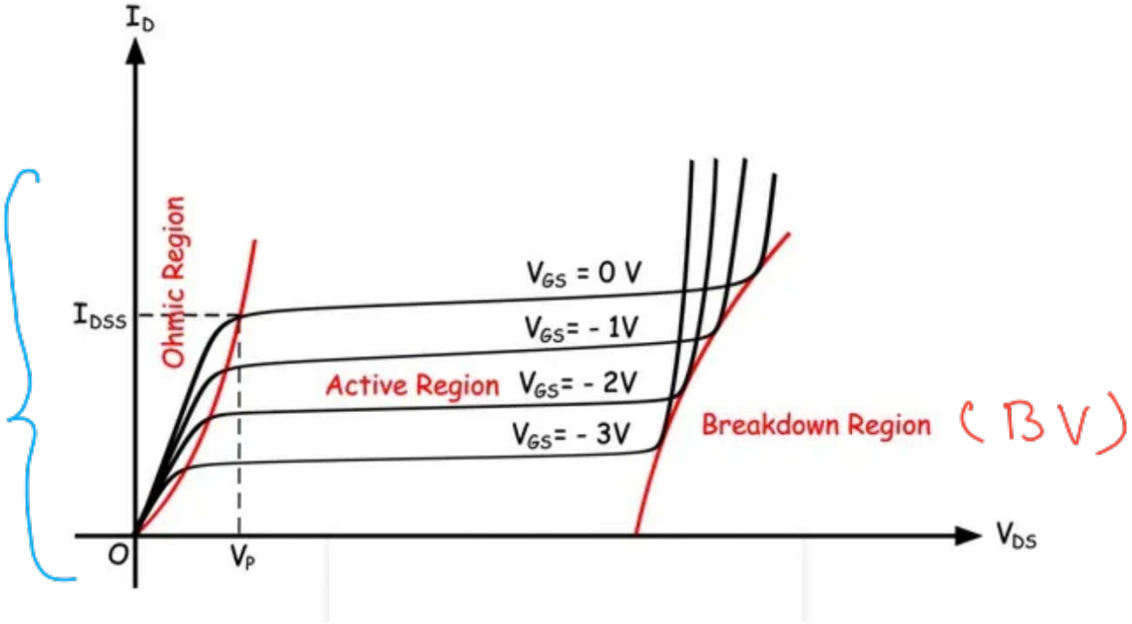
p-Channel *JFET*

Field Effect Transistor

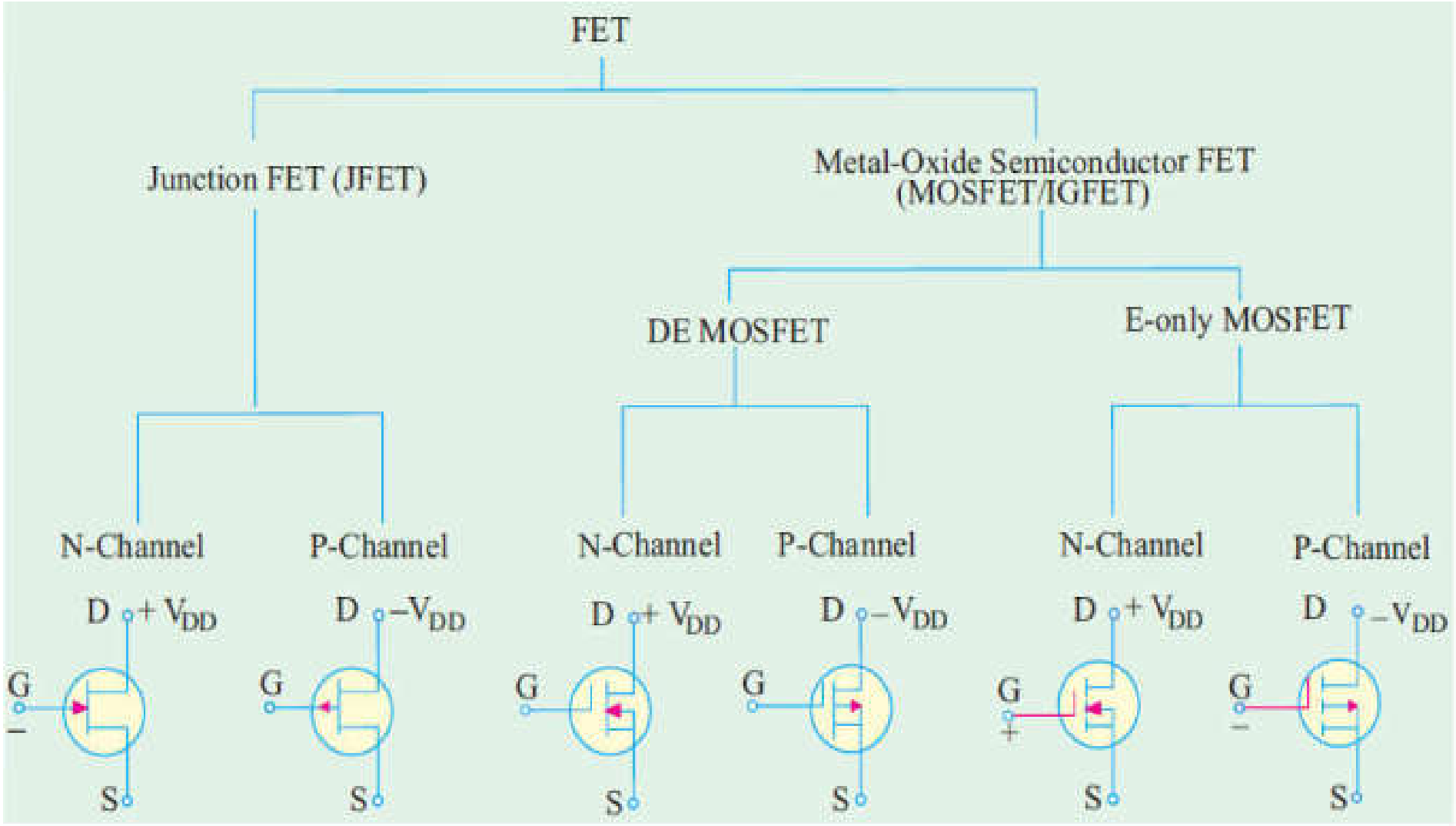


→ As V_{GS} becomes more negative
Id decreases
→ When $V_{GS} = V_P$, $I_D \to 0$

→ at $V_{GS} = 0$, $I_D = I_{DSS}$
→ As V_{GS} → applied
$I_D \downarrow \to V_P \downarrow \to BV \downarrow$



Field Effect Transistor



FET vs BJT Comparison

- FET is an unipolar device, while BJT is a bipolar device
- It has very high input impedance
- FET is voltage controlled device, BJT is current controlled device
- For amplification, BJT is operated in active region, while FET should be operated in saturation region