



#### Digital Electronics & Logic Design

(EC 207)



**Dr. Vivek Garg** 

Department of Electronics Engineering

S. V. National Institute of Technology (SVNIT)
Surat

email: vivekg@eced.svnit.ac.in; vivekgarg0101@gmail.com



#### **Course Outline**



#### PN DIODE AND TRANSITOR

(04 Hours)

PN Diode Theory, PN Characteristic and Breakdown Region, PN Diode Application as Rectifier, Zener Diode Theory, Zener Voltage Regulator, Diode as Clamper and Clipper, Photodiode Theory, LED Theory, 7 Segment LED Circuit Diagram and Multi Colour LED, LASER Diode Theory and Applications, Bipolar Junction Transistor Theory, Transistor Symbols And Terminals, Common Collector, Emitter and Base Configurations, Different Biasing Techniques, Concept of Transistor Amplifier, Introduction to FET Transistor And Its Feature.

#### WAVESHAPING CIRCUITS AND OPERATIONAL AMPLIFIER

(06 Hours)

Linear Wave Shaping Circuits, RC High Pass and Low Pass Circuits, RC Integrator and Differentiator Circuits, Nonlinear Wave Shaping Circuits, Two Level Diode Clipper Circuits, Clamping Circuits, Operational Amplifier OP-AMP with Block Diagram, Schematic Symbol of OP-AMP, The 741 Package Style and Pinouts, Specifications of Op-Amp, Inverting and Non-Inverting Amplifier, Voltage Follower Circuit, Multistage OP-AMP Circuit, OP-AMP Averaging Amplifier, OP-AMP Subtractor.

#### BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS

(04 Hours)

Basic Logic Operation and Logic Gates, Truth Table, Basic Postulates and Fundamental Theorems of Boolean Algebra, Standard Representations of Logic Functions- SOP and POS Forms, Simplification of Switching Functions-K-Map and Quine-Mccluskey Tabular Methods, Synthesis of Combinational Logic Circuits.

COMBINATIONAL LOGIC CIRCUIT USING MSI INTEGRATED CIRCUITS

(07 Hours)

9/10/2021



#### **Course Outline**



Binary Parallel Adder; BCD Adder; Encoder, Priority Encoder, Decoder; Multiplexer and Demultiplexer Circuits; Implementation of Boolean Functions Using Decoder and Multiplexer; Arithmetic and Logic Unit; BCD to 7-Segment Decoder; Common Anode and Common Cathode 7-Segment Displays; Random Access Memory, Read Only Memory And Erasable Programmable ROMS; Programmable Logic Array (PLA) and Programmable Array Logic (PAL).

#### INTRODUCTION TO SEQUENTIAL LOGIC CIRCUITS

(04 Hours)

Basic Concepts of Sequential Circuits; Cross Coupled SR Flip-Flop Using NAND or NOR Gates; JK Flip-Flop Rise Condition; Clocked Flip-Flop; D-Type and Toggle Flip-Flops; Truth Tables and Excitation Tables for Flip-Flops; Master Slave Configuration; Edge Triggered and Level Triggered Flip-Flops; Elimination of Switch Bounce using Flip-Flops; Flip-Flops with Preset and Clear.

#### SEQUENTIAL LOGIC CIRCUIT DESIGN

(06 Hours)

Basic Concepts of Counters and Registers; Binary Counters; BCD Counters; Up Down Counter; Johnson Counter, Module-N Counter; Design of Counter Using State Diagrams and Table; Sequence Generators; Shift Left and Right Register; Registers With Parallel Load; Serial-In-Parallel-Out (SIPO) And Parallel-In-Serial-Out(PISO); Register using Different Type of Flip-Flop.

#### REGISTER TRANSFER LOGIC

(04 Hours)

Arithmetic, Logic and Shift Micro-Operation; Conditional Control Statements; Fixed-Point and Floating-Point Data; Arithmetic Shifts; Instruction Code and Design Of Simple Computer.

#### PROCESSOR LOGIC DESIGN

(03 Hours)

Processor Organization; Design of Arithmetic Logic Unit; Design of Accumulator.

#### CONTROL LOGIC DESIGN

(04 Hours)

Control Organization; Hard-Wired Control; Micro Program Control; Control Of Processor Unit; PLA Control.



#### **Course Text and Materials**



- Schilling Donald L. and Belove E., "Electronics Circuits- Discrete and Integrated", 3rd Ed., McGraw-Hill, 1989, Reprint 2008.
- Millman Jacob, Halkias Christos C. and Parikh C., "Integrated Electronics", 2nd Ed., McGraw-Hill, 2009.
- Taub H. and Mothibi Suryaprakash, Millman J., "Pulse, Digital and Switching Waveforms", 2nd Ed., McGraw-Hill, 2007.
- Mano Morris, "Digital Logic and Computer Design", 5th Ed., Pearson Education, 2005.
- Lee Samual, "Digital Circuits and Logic Design", 1st Ed., PHI, 1998.



# Wave shaping Circuits and Operational Amplifier



# **Wave Shaping**

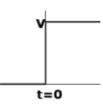
- ▶ A Signal may be of different shape such as Sinusoidal, Square, Triangular etc.
- ▶ It is the process of changing the shape of input signal with linear / non-linear circuits.
- ▶ Wave Shaping can be of two types:
  - ▶ Linear Wave Shaping: Linear elements like Resistors, Capacitors, Inductors etc are employed.
  - ▶ Non-Linear : Non-Linear Devices are used (e.g Diode) Clippers

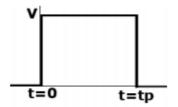


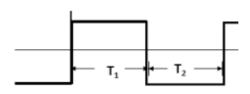


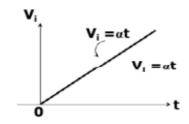
# **Linear Wave Shaping**

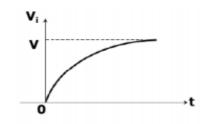
- ► The process where by the form of a non-sinusoidal signal is changed by transmission through a linear network is called Linear Wave Shaping
- ▶ Types:
  - ► High Pass RC Circuit.
  - ▶ Low Pass RC Circuit.
- Non-sinusoidal waveforms
  - ▶ Step
  - ▶ Pulse
  - ▶ Square Wave
  - ▶ Ramp
  - ▶ Exponential Wave















## **Filters**

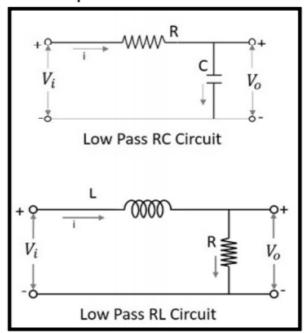
- A Filter is a circuit that is designed to pass the signals with desired frequencies and reject or attenuate the other frequencies.
- As a frequency-selective device, a filter can be used to limit the frequency spectrum of a signal to some specified band of frequencies.
- ▶ Filters are the circuits used in radio and TV receivers to allow us to select one desired signal out of a multitude of broadcast signals in the environment.
- ▶ A filter is a passive filter if it consists of only passive elements R, L, and C. It is said to be an active filter if it consists of active elements (such as transistors and operational amplifiers) in addition to passive elements R, L, and C.

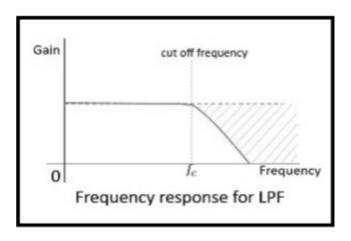




### **Low Pass Filter**

A Filter circuit which allows a set of frequencies that are below a specified value can be termed as a Low pass filter. This filter passes the lower frequencies.

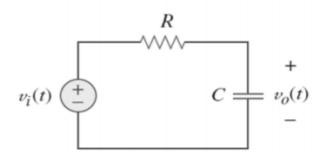


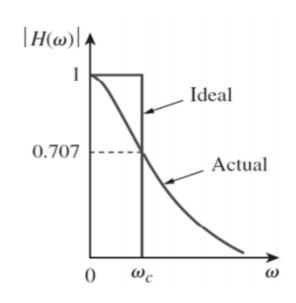






### **Low Pass Filter**





$$\mathbf{H}(\omega) = \frac{\mathbf{V}_o}{\mathbf{V}_i} = \frac{1/j\omega C}{R + 1/j\omega C}$$

$$\mathbf{H}(\omega) = \frac{1}{1 + j\omega RC}$$

$$|\mathbf{H}(\omega)| = \frac{1}{1 + \omega^2 R^2 C^2} = \frac{1}{\sqrt{2}}$$

when, 
$$\omega_c = \frac{1}{RC} \rightarrow \text{Resonance}$$
 freq.





**Prob 1**: A low pass filter has the following components:

input voltage source (10 V and 2kHz frequency), R: 1 k Ohm, C: 0.1µF.

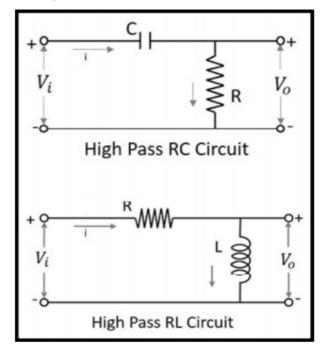
Find 3dB frequency, and the output voltage at 2kHz.

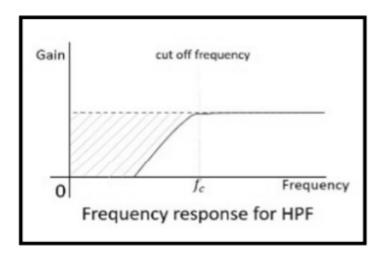




# **High Pass Filter**

A Filter circuit which allows a set of frequencies that are above a specified value can be termed as a High pass filter. This filter passes the higher frequencies.

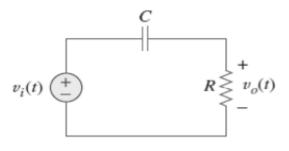


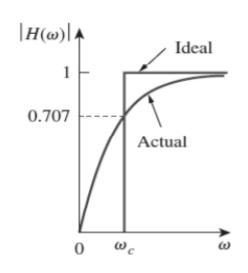






# **High Pass Filter**





$$\mathbf{H}(\omega) = \frac{\mathbf{V}_o}{\mathbf{V}_i} = \frac{R}{R + 1/j\omega C}$$

$$\mathbf{H}(\omega) = \frac{j\omega RC}{1 + j\omega RC} = \frac{1}{1 + (1/j\omega RC)}$$

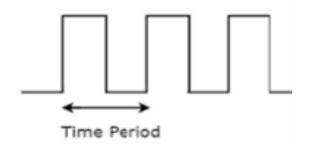
$$|\mathbf{H}(\omega)| = \frac{1}{\sqrt{1 + (1/\omega^2 R^2 C^2)}} = \frac{1}{\sqrt{2}}$$
when,  $\omega_c = \frac{1}{RC} \rightarrow \text{Resonance}$ 

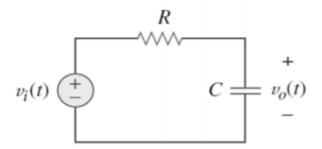




# **RC Integrator**

- ▶ If the time constant value is much greater than the time period of the input signal than the RC low pass circuit will act as an Integrator
- ▶ RC >> T



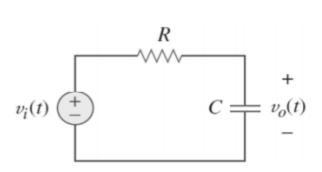






### **Derivation**

- ▶ If the time constant value is much greater than the time period of the input signal than the RC Low pass circuit will act as an Integrator
- ▶ RC >> T
- Under this circumstances the voltage drop across C will be very small in comparison to the drop across R



$$V_{i} = iR$$

$$i = \frac{V_{i}}{R}$$

$$V_{o} = \frac{1}{C} \int idt$$

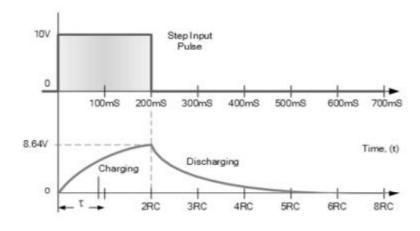
$$V_{o} = \frac{1}{C} \int \frac{V_{i}}{R} dt$$

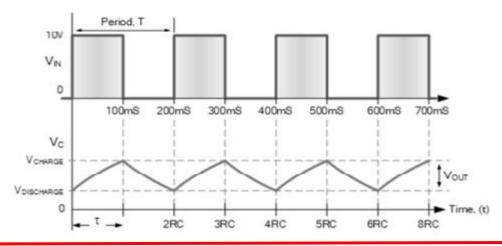
$$V_{o} = \frac{1}{RC} \int V_{i} dt$$





# **RC** Integrator

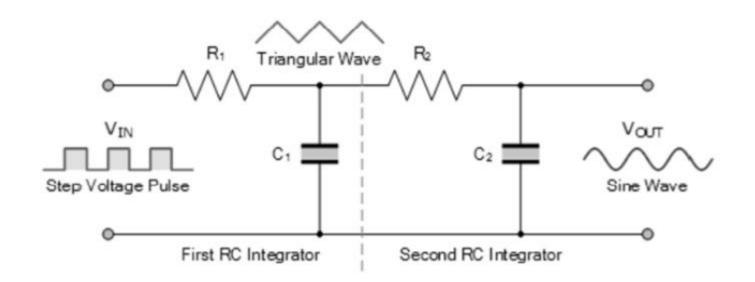








# **RC** Integrator

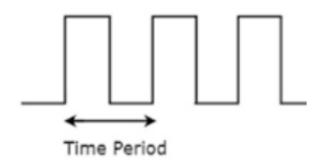


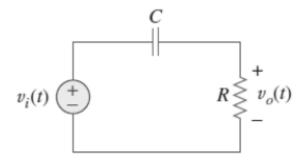




## RC Differentiator

- ▶ If the time constant value is much smaller than the time period of the input signal than the RC High pass circuit will act as an Differentiator
- ▶ RC << T</p>



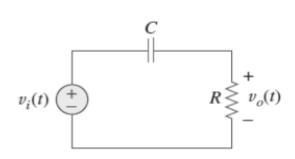






## **Derivation**

- ▶ If the time constant value is much smaller than the time period of the input signal than the RC High pass circuit will act as an Differentiator
- ▶ RC << T</p>
- ▶ Under this circumstances the voltage drop across R will be very small in comparison with the drop across C. Hence we may consider that the total input Vi appears across C, so that the current is determined entirely by the capacitance.



$$i = C \frac{dV_i}{dt}$$

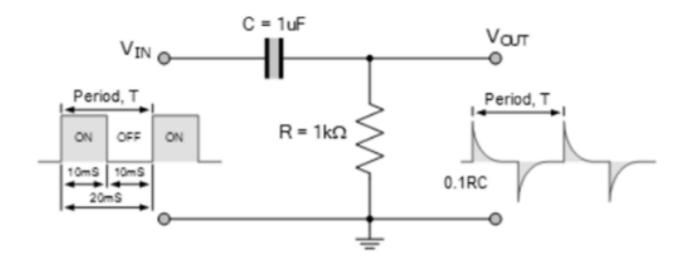
$$V_o = iR$$

$$V_o = RC \frac{dV_i}{dt}$$



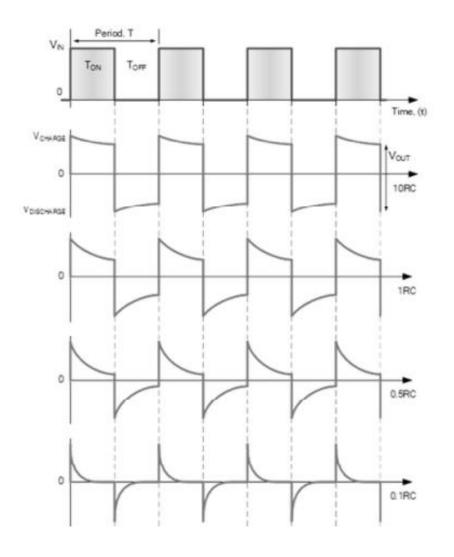


# **RC Differentiator**













## RC Integrator

- ► Sine (-Cosine)
- ▶ Triangular Sine
- ▶ Rectangular Wave Trianlge

#### **RC Differentiator**

- ▶ Sine Cosine
- ▶ Triangular Wave Square Wave
- ► Rectangular Wave Spikes



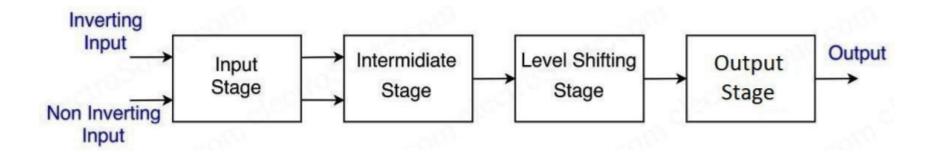


An ideal pulse of amplitude 10 V is fed to an RC low-pass integrator circuit. The width of the pulse is 3  $\mu$ s. Draw the output waveforms for the following upper 3-dB frequencies: (a) 30 MHz, (b) 3 MHz and (c) 0.3 MHz.



### **Operational Amplifier (OPAMP)**



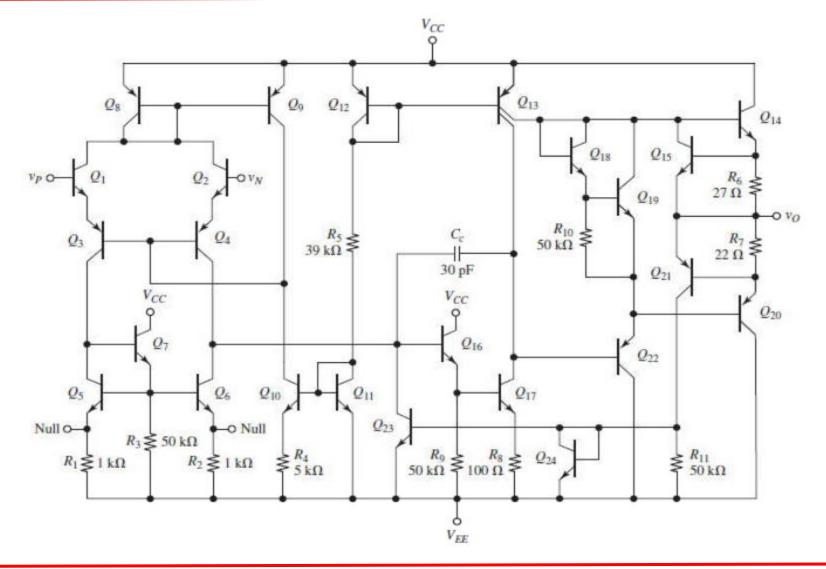


 An op amp is an active circuit element designed to perform mathematical operations of addition, subtraction, multiplication, division, differentiation, and integration, etc.



## **OPAMP** internal Circuit Diagram

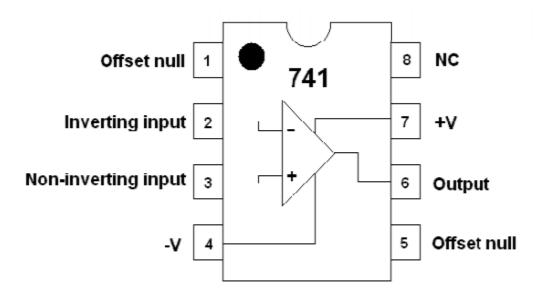






## 741 Package and Pin Details



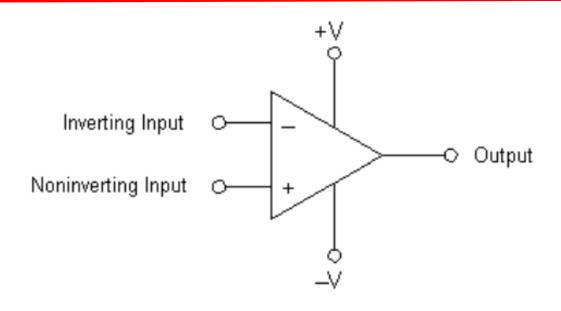






## **Schematic Symbol and Properties**



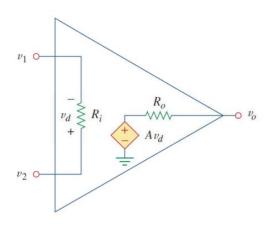


Parameter	Ideal Op-Amp	Real Op-Amp
Differential Voltage Gain	∞	10 <sup>5</sup> - 10 <sup>9</sup>
Gain Bandwidth Product (Hz)	∞	1-20 MHz
Input Resistance (R)	∞	10 <sup>6</sup> - 10 <sup>12</sup> Ω
Output Resistance (R)	0	100 - 1000 Ω



### Non Ideal Amplifier





- An op-amp amplifies the difference of the inputs V₁ and V₂ (known as the differential input voltage)
- This is the equation for an open loop gain amplifier:

$$V_{out} = A(V_{+} - V_{-})$$

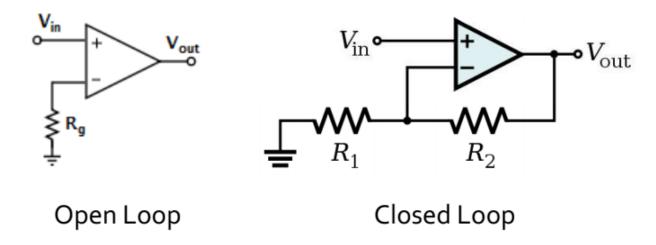
- K is typically very large at around 10,000 or more for IC Op-Amps
- This equation is the basis for all the types of amps we will be discussing



## **OPAMP Configurations**



 A closed loop op-amp has feedback from the output to the input, an open loop op-amp does not

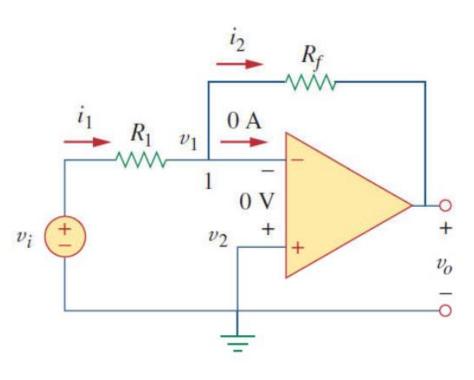


- Ideal Opamp
  - Opamp does not accepts any input current
  - Voltage at inverting Terminal = Voltage at noninverting terminal.



### **Inverting Amplifier**





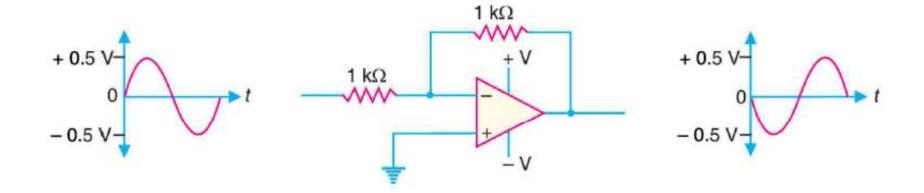
$$i_1 = i_2 \implies \frac{v_i - v_1}{R_1} = \frac{v_1 - v_o}{R_f}$$

$$v_o = -\frac{R_f}{R_1}v_i$$



### Example



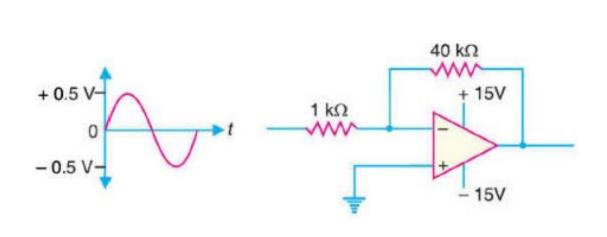


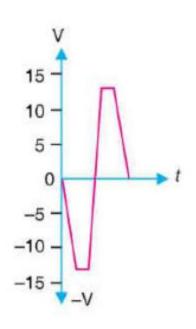
Voltage gain, 
$$A_{CL} = -\frac{R_f}{R_i} = -\frac{1 \text{ k}\Omega}{1 \text{ k}\Omega} = -1$$



### Example





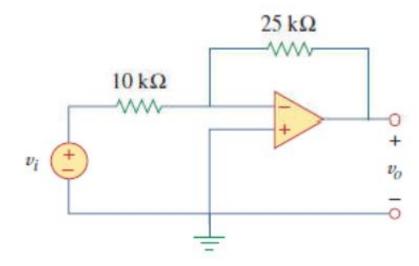


Voltage gain, 
$$A_{CL} = -\frac{R_f}{R_i} = -\frac{40 \text{ k}\Omega}{1 \text{ k}\Omega} = -40$$





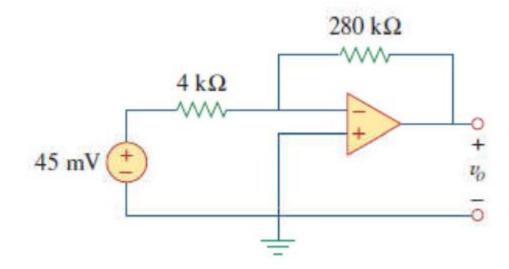
For the opamp in figure below. If vi is 0.5 V, calculate: (a) the output voltage vo, and (b) the current in the 10-k resistor.





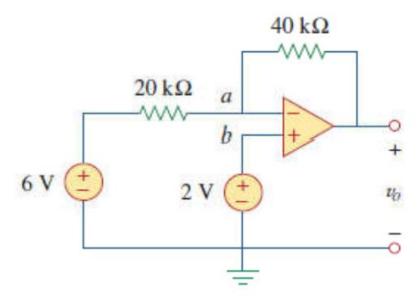


 Find the output of the opamp circuit shown below. Calculate the current through the feedback resistor.





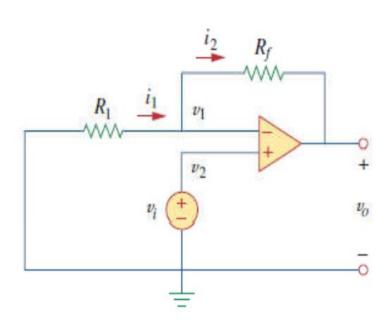






### **Non-Inverting Amplifier**





$$i_1 = i_2 \implies \frac{0 - v_1}{R_1} = \frac{v_1 - v_o}{R_f}$$

But  $v_1 = v_2 = v_i$ . Equation (5.10) becomes

$$\frac{-v_i}{R_1} = \frac{v_i - v_o}{R_f}$$

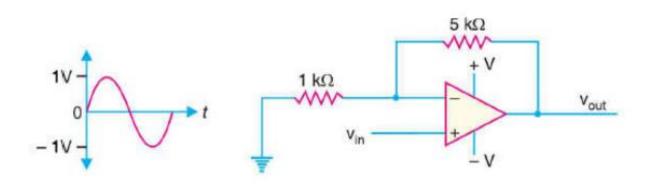
or

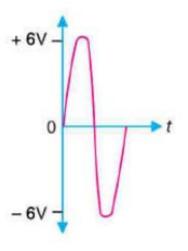
$$v_o = \left(1 + \frac{R_f}{R_1}\right) v_i$$



#### Example







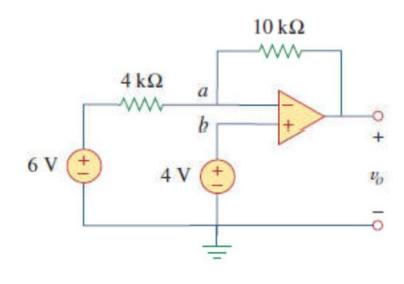
The input signal is 2 I' peak-to-peak.

Voltage gain, 
$$A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{5 \text{ k}\Omega}{1 \text{ k}\Omega} = 1 + 5 = 6$$

:. Peak-to-peak output voltage = 
$$A_{CL} \times v_{inpp} = 6 \times 2 = 12 \text{ V}$$







Determine Vo?

Applying KCL at node a,

$$\frac{6-v_a}{4}=\frac{v_a-v_o}{10}$$

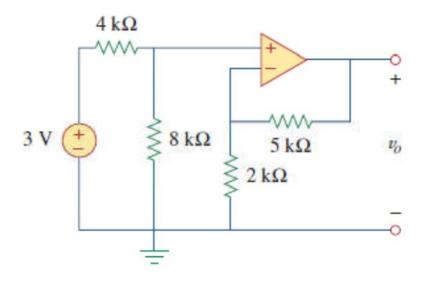
But  $v_a = v_b = 4$ , and so

$$\frac{6-4}{4} = \frac{4-v_o}{10} \quad \Rightarrow \quad 5 = 4-v_o$$

or  $v_o = -1$  V, as before.





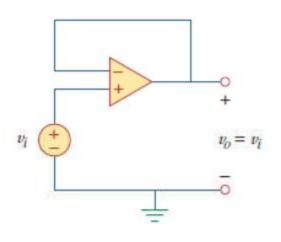


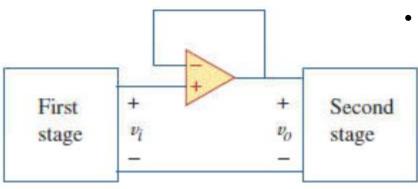
Determine Vo?



### **OPAMP** as Buffer





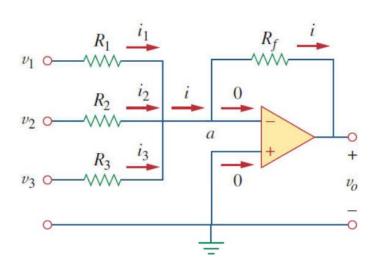


- Low input resistance of the load circuit results in large current sink at the load.
- This effect is called as Loading effect.
- High input resistance is required to tackle the loading effect.
- OPAMP is used as a buffer, which provides high
   input resistance at the load.



#### **OPAMP** as Adder





$$i = i_1 + i_2 + i_3$$

But

$$i_1 = \frac{v_1 - v_a}{R_1}, \quad i_2 = \frac{v_2 - v_a}{R_2}$$

$$i_3 = \frac{v_3 - v_a}{R_3}, \quad i = \frac{v_a - v_o}{R_f}$$

We note that  $v_a = 0$ 

$$v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3\right)$$

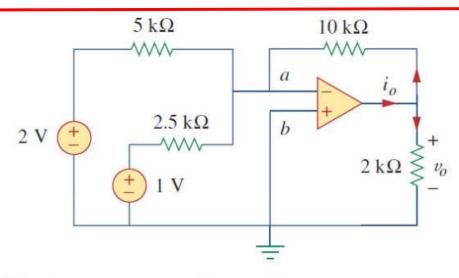
$$R_1 = R_2 = R_3$$

$$\frac{R_f}{R} = \frac{1}{n}$$

$$v_o = -\left(\frac{v_1 + v_2 + v_3}{3}\right)$$







This is a summer with two inputs.

$$v_o = -\left[\frac{10}{5}(2) + \frac{10}{2.5}(1)\right] = -(4+4) = -8 \text{ V}$$

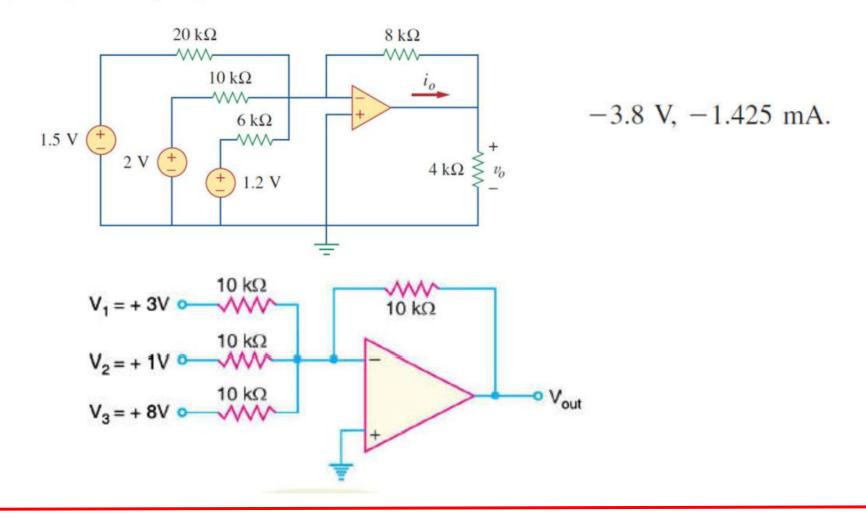
The current  $i_o$  is the sum of the currents through the  $10\text{-k}\Omega$  and  $2\text{-k}\Omega$  resistors. Both of these resistors have voltage  $v_o = -8 \text{ V}$  across them, since  $v_a = v_b = 0$ . Hence,

$$i_o = \frac{v_o - 0}{10} + \frac{v_o - 0}{2} \text{mA} = -0.8 - 4 = -4.8 \text{ mA}$$





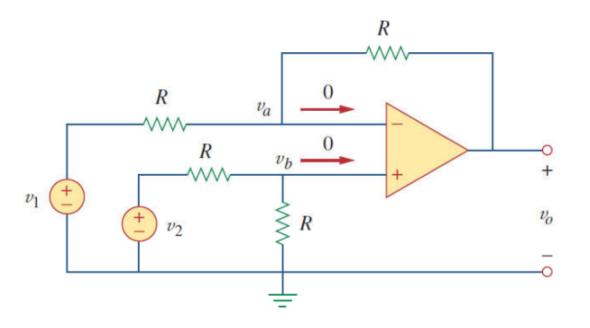
Find  $v_o$  and  $i_o$  in the op amp circuit shown





## **OPAMP** as **Subtractor**





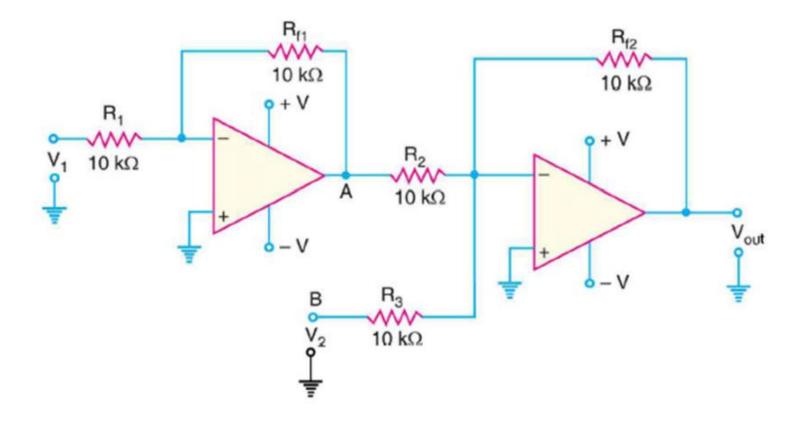
$$v_o = -\frac{R}{R}v_1 + \left(1 + \frac{R}{R}\right)v_b$$

$$v_b = \frac{R}{R+R}v_2$$

$$v_o = v_2 - v_1$$



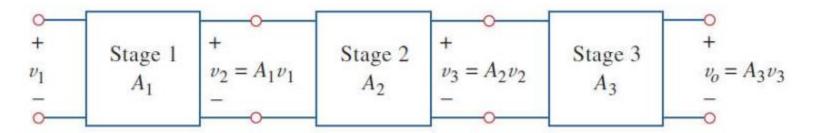


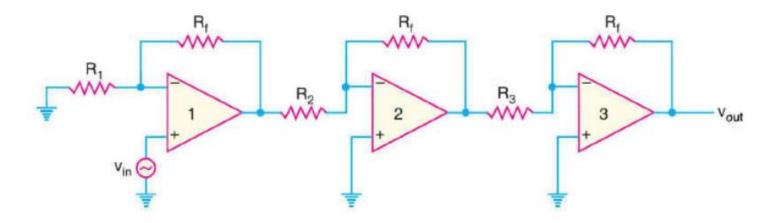




## **Multistage OPAMP Circuits**







The overall voltage gain A of this circuit is given by;

$$A = A_1 A_2 A_3$$
where  $A_1$  = Voltage gain of first stage =  $1 + (R_f/R_1)$ 

$$A_2$$
 = Voltage gain of second stage =  $-R_f/R_2$ 

$$A_3$$
 = Voltage gain of third stage =  $-R_f/R_3$ 



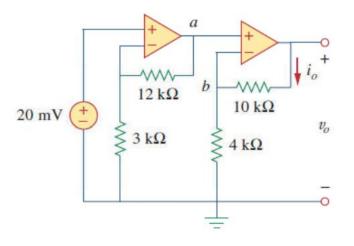


• In the previous circuit, if Rf = 470 k, R1=4.3 k, R2=33 k and R3=33 k. Determine the output voltage for an input voltage of 33 micro volts.





#### Find $v_o$ and $i_o$ in the circuit



This circuit consists of two noninverting amplifiers cascaded. At the output of the first op amp,

$$v_a = \left(1 + \frac{12}{3}\right)(20) = 100 \text{ mV}$$

At the output of the second op amp,

$$v_o = \left(1 + \frac{10}{4}\right)v_a = (1 + 2.5)100 = 350 \text{ mV}$$

The required current  $i_o$  is the current through the 10-k $\Omega$  resistor.

$$i_o = \frac{v_o - v_b}{10} \, \text{mA}$$

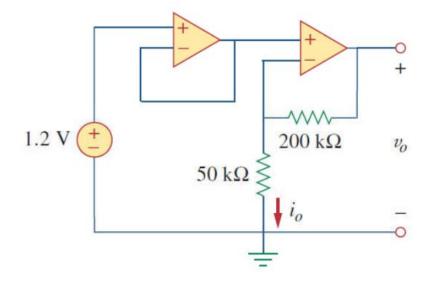
But 
$$v_b = v_a = 100$$
 mV. Hence,

$$i_o = \frac{(350 - 100) \times 10^{-3}}{10 \times 10^3} = 25 \,\mu\text{A}$$





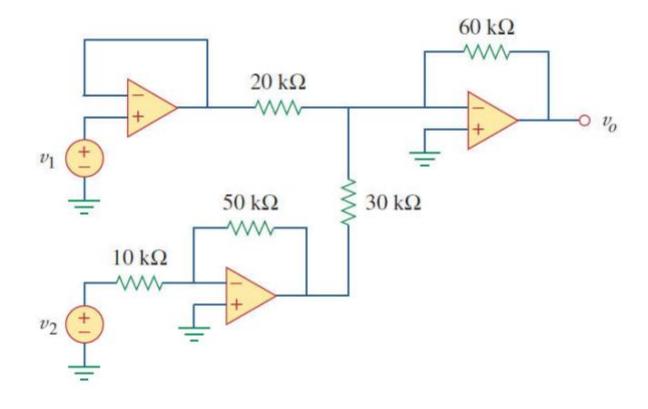
Determine  $v_o$  and  $i_o$  in the op amp circuit







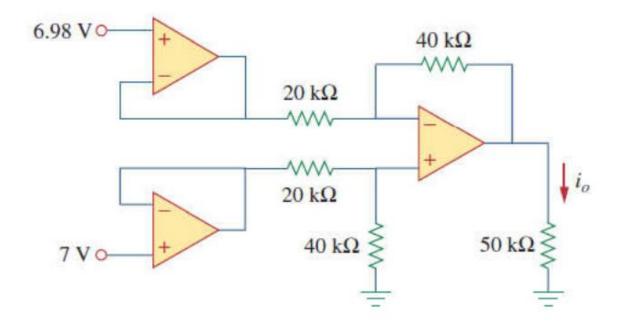
If  $v_1 = 7$  V and  $v_2 = 3.1$  V, find  $v_o$  in the op amp circuit







# Obtain io



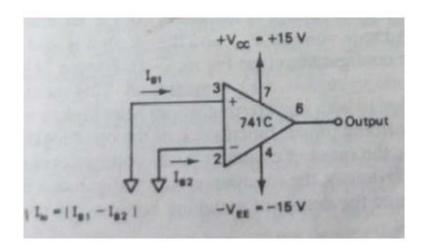


## **Input Offset Current**



 Algebric difference between the currents entering the inverting and non-inverting terminals.

$$I_{io} = \left| I_{B1} - I_{B2} \right|$$





## **Input Bias Current**



 Average of the currents that flow into the inverting an non-inverting terminals.

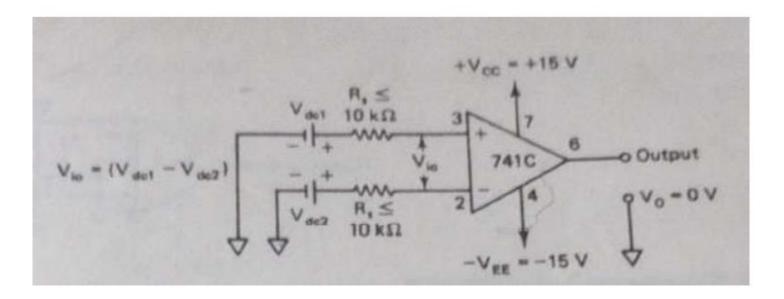
$$I_{B} = \frac{I_{B1} + I_{B2}}{2}$$



## **Input Offset Voltage**



It is the voltage that must be applied between the two input terminals of the opamp to nullify the output.





# Common Mode Rejection Ratio (CMRR)



 It is defined as the ratio of Differential Mode Gain to Common Mode Gain.

$$CMRR = \frac{A_d}{A_{cm}}$$

Change in the opamp's input offset voltage, caused by variation in supply voltages. It is also known as PSRR. Lower the value, better the opamp's performance.

$$SVRR / PSRR = \frac{\Delta V_{io}}{\Delta V}$$



#### **Slew Rate**



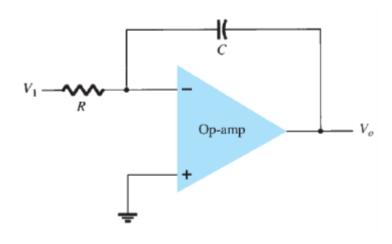
 Maximum rate of change of output voltage per unit of time and is expressed in volts per microseconds.

$$SR = \frac{dV_o}{dt} \bigg|_{\text{max}} V / \mu S$$

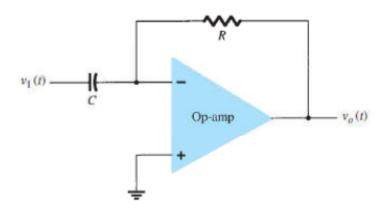


# **OPAMP** as Differentiator/Integrator





$$v_o(t) = -\frac{1}{RC} \int v_1(t) \, dt$$



$$v_o(t) = -RC \frac{dv_1(t)}{dt}$$



