Gobinath Jegannathan

Curriculum Vitae

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DOCTORAL RESEARCH

"CMOS based current-assisted detectors with avalanche gain: APDs, SPADs and SiPMs"

For the PhD research, I initially started with research focus on CMOS drivers that can drive a laser to emit very sharp (<1 ns) and high power (>10 W) pulses, which can be used in direct time-of-flight (dTOF) application. A few months later, due to new ideas and opportunities, I shifted the primary research focus towards Novel single-photon avalanche diode (SPAD) receivers for (dTOF). We came up with the concept of a "current-assisted" SPAD which promises enhanced near infrared sensitivity combined with high speed. Since then, I have been simulating, making variants and characterizing them. A few successful candidate structures for CA-SPADs have be already identified and have been published in peer-reviewed publications and presented in Single photon workshop 2019. My secondary research focus is on realizing high-performance CMOS avalanche photodiodes (APDs) and Silicon photomultipliers (SiPMs) using "current-assistance" technique.

WORK EXPERIENCE

SEPTEMBER 2016 – PRESENT (FT)

Vrije Universiteit Brussel
PhD researcher

Expected graduation: August 2021

JULY 2013 – AUGUST 2014 (1 YEAR PROJECT)

Tata institute of fundamental research, Mumbai
Junior research fellow

This position involved graphene and TMDC nanodevice fabrication and charcterization. During this time, I found a way to use monolayer /bilayer graphene as electrode contacts for WS2 nanotubes and the implementation involved complex trail and error fabrication attempts to realize the device. The end study resulted in a publication in Applied physics letters. *(see publication section).*

EDUCATION

2016 – PRESENT **Doctor of Philosophy**
EXPECTED GRADUATION: AUGUST 2021
Electronics engineering
Vrije Universiteit Brussel

2014-2016 **Master of Science**
Photonics Engineering
Ghent University and Vrije Universiteit Brussel

2009-2013 **Bachelor of Technology**
Nanotechnology
SRM University

SKILLSET

Full CMOS process pipeline: Device physics simulations for sensor pixel, SPICE simulations for readout circuitry, Layout, Test PCB design, Wirebonding, Design of experiments, Experiment automation using python, Device characterization, data analysis and reporting.

Programming: Python for data analysis for Measurement automation, MATLAB, Basic working knowledge of VHDL.

In addition, I have hands-on experience in working with nanodevice fabrication in a class-100 cleanroom during my time at TIFR. Some selected skills include e-beam lithography, electrode formation using physical vapor deposition, sputtering and atomic layer deposition.

PATENTS

2016 **CMOS VCSEL driver**
US10250011B2

2018 **Current-assisted SPAD**
US20200144436A1

SELECTED PUBLICATIONS

Jegannathan, G. et al (2019). Current assisted avalanche photo diodes (CAAPDs) with separate absorption and multiplication region in conventional CMOS. *Applied physics letters*, doi.org/10.1063/1.5116102

Jegannathan, G. et al (2020). Current-Assisted Single Photon Avalanche Diode (CASPAD) Fabricated in 350 nm Conventional CMOS. *Applied sciences*, doi.org/10.3390/app10062155

Jegannathan, G*. et al (2014).Light matter interaction in WS2 nanotube-graphene hybrid devices. *Applied physics letters*, doi.org/10.1063/1.4902983

**Two equal-contributing first authors*

CONFERENCE PRESENTATIONS

Jegannathan, G. et al (2019).Current-assisted single photon avalanche diode (CASPAD) in 350 nm CMOS *Single Photon Workshop 2019, Milan.*

REFERENCES

References available on request