DAYANANDA SAGAR UNIVERSITY

USN No:

III Semester B. Tech Backlog Examinations – January 2023

Course Title: Digital Electronics and Logic Design **Course Code:** 19CS2303
Duration: 03 Hours **Date:** 27-01-2023
Time: 1:30 pm to 04:30 pm **Max Marks:** 100

Note:
1. **Answer ALL 5 FULL Questions. All Questions are Compulsory**
2. **Each Full Question carries 20 Marks**
3. **Draw neat sketches wherever necessary**
4. **Missing Data may be suitably assumed**

1.a. Convert the following: (05 Marks)
i) 9AF to binary
ii) 1000 1100 to hexadecimal
iii) 2479 to hexadecimal
iv) 175 to octal
v) 1011 01101 to octal

1.b. Solve the following using K map by SOP method. Write the truth table and draw the circuit diagram using basic gates. (10 Marks)
F (A, B, C, D) = ∑m (0, 1, 3, 4, 5, 7, 10, 12, 13) + d (2, 14, 15)
F (W, X, Y, Z) = ∑m (0, 2, 3, 4, 6, 7, 8, 9, 13) + d (10, 12, 15)

1.c. Simplify the following using Boolean laws and also mention the law applied at each step. (05 Marks)
i) (AB)' (A' + B) (B' + B)
ii) P+(PQ)'

2.a. Implement the following Boolean function using 8x1 mux and table method. F (A, B, C, D) = ∑m (0,2,3,6,8,9,13,14) (05 Marks)

2.b. What is a Decoder? Write the truth table and Logic diagram of 3 to 8-line Decoder. (05 Marks)

2.c. Simplify the following Boolean function by using Quine McClusky method
F(A,B,C,D)= ∑m (2, 6, 8, 9, 10, 11, 14, 15) (10 Marks)

3.a. Illustrate how a PLA can be used for a combinational logic design with reference to the functions. (08 Marks)
F1(A,B,C)= ∑m(0,1,3,4)
F2(A,B,C)= ∑m(1,2,3,4,5)

3.b.	Implement the given Boolean expression using a PAL. $X(A,B,C)= \sum m(2,3,5,7)$ $Y(A,B,C)= \sum m(0,1,5)$ $Z(A,B,C)= \sum m(0,2,3,5)$	(08 Marks)
3.c.	With block diagram explain ROM and its types.	(04 Marks)
4.a.	Explain D flip flop along with its truth table, characteristic table and excitation table.	(08 Marks)
4.b.	Differentiate between combinational and sequential circuits.	(04 Marks)
4.c.	Briefly explain the SR latch using NAND & NOR gates along with their logic diagrams and truth tables with all cases.	(08 Marks)
5.a.	Design a MOD 5 counter using JK flip flop. Enumerate the steps in detail.	(10 Marks)
5.b.	Draw a 4 bit Parallel In Parallel Out (PIPO) shift register and explain its working.	(05 Marks)
5.c.	Differentiate between asynchronous and synchronous counters.	(05 Marks)