CODIGO

```
library IEEE;
 use IEEE.STD LOGIC 1164.ALL;
 use IEEE.NUMERIC STD.ALL;
 use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity alu is
      Port ( A : in STD LOGIC VECTOR (3 downto 0);
             B : in STD LOGIC VECTOR (3 downto 0);
             Sel : in STD LOGIC VECTOR (2 downto 0);
             Res : out STD_LOGIC_VECTOR (3 downto 0));
end alu;
architecture Behavioral of alu is
∃ --Signals
--SIGNAL Res temp: std logic vector (3 downto 0);
    process(Sel)
    begin
        case (Sel) is
             when "000" => Res <= A + B;
              when "001" => Res <= A - B;
             when "010" => Res <= A - "0001";
             when "011" => Res <= A + "0001";
             when "100" => Res <= (A AND B);
           when "101" => Res <= (A OR B);
              when "110" => Res <= (NOT A);
              when "111" => Res <= (A XOR B);
              when others => null;
         end case;
    end process;
end Behavioral;
```

TEST BENCH

```
library IEEE;
  use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
 use IEEE.STD LOGIC UNSIGNED.ALL;

    entity alu_tb is

 -- Port ();
end alu_tb;
architecture Behavioral of alu_tb is
    COMPONENT alu
        Port ( A : in STD LOGIC VECTOR (3 downto 0);
               B : in STD LOGIC VECTOR (3 downto 0);
               Sel : in STD_LOGIC_VECTOR (2 downto 0);
               Res : out STD LOGIC VECTOR (3 downto 0));
  END COMPONENT;
     --Signals
     SIGNAL A: STD LOGIC VECTOR (3 downto 0);
     SIGNAL B: STD_LOGIC_VECTOR (3 downto 0);
     SIGNAL Sel: STD LOGIC VECTOR (2 downto 0);
     SIGNAL Res: STD LOGIC VECTOR (3 downto 0);
begin
   -- Instance
                                 wait for 10 ns;
    DUT: alu
                                A <= "0101";
       PORT MAP (
                                Sel <= "010";
  A => A, wait for 10 ns;
           B \Rightarrow B,
                                --A + 1
                             A <= "1100";
Sel <= "011";
           Sel => Sel,
Res => Res
                                                               -- A XOR B
                                wait for 10 ns;
       );
                                                                A <= "0101";
                                 -- A AND B
                                                               B <= "0011";
                                A <= "0101";
     --Signals
    estimulos: process B <= "0110";
                                                               Sel <= "111";
        --A + B
                                                               wait for 10 ns;
                                Sel <= "100";
     begin
                                wait for 10 ns;
                                                         end process;
         A <= "1000";
                                --A OR B
                              A <= "0101";
B <= "0110";
        B <= "0100";
                                                       end Behavioral;
        Sel <= "000";
        wait for 10 ns; Sel <= "101";
                                -- NOT A
        --A - B
        A <= "1000";
                            Walt lol _.

A <= "0000";

Sel <= "110";

wait for 10 ns;
                                wait for 10 ns;
        B <= "0100";
        Sel <= "001";
        --A - 1
```