CODIGO

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity bin_bcd is
    Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
           u : out STD_LOGIC_VECTOR (3 downto 0);
           d : out STD_LOGIC_VECTOR (3 downto 0));
end bin_bcd;

architecture Behavioral of bin_bcd is
--Generar componente
--Generar señales
begin
--Instanciar componente
    process(a)
        -- crear variables internas del proceso
        variable z: STD_LOGIC_VECTOR(11 downto 0);
        begin
            z := "000000000000"; -- := Asignar valor a variable
            z(6 downto 3) := a; -- primeros 3 corrimientos
            for i in 0 to 0 loop
                --unidades
                if z(7 downto 4) > "0100"  then
                    z(7 downto 4) := z(7 downto 4) + "0011";
                end if;
                --decenas
                if z(11 downto 8) > "0100"  then
                    z(11 downto 8) := z(11 downto 8) + "0011";
                end if;
                z(11 downto 1) := z(10 downto 0);
            end loop;
            u <= z(7 downto 4);
            d <= z(11 downto 8);
    end process;
end Behavioral;
```

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity bcd_7seg is
    Port ( b : in STD_LOGIC_VECTOR (3 downto 0);
           s : out STD_LOGIC_VECTOR (6 downto 0));
end bcd_7seg;

architecture Behavioral of bcd_7seg is
--Generate component
--Generate signals
begin
--instance component
    process(b)
    begin
        case b is
            when "0000" => s <= "0111111";--0
            when "0001" => s <= "0000110";--1
            when "0010" => s <= "1011011";--2
            when "0011" => s <= "1001111";--3
            when "0100" => s <= "1100110";--4
            when "0101" => s <= "1101101";--5
            when "0110" => s <= "1111101";--6
            when "0111" => s <= "0000111";--7
            when "1000" => s <= "1111111";--8
            when "1001" => s <= "1101111";--9
            when others => s <= "0000000";--default
        end case;
    end process;
end Behavioral;
```

TEST BENCH

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity bin_7seg is
    Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
           seg_0 : out STD_LOGIC_VECTOR (6 downto 0);
           seg_1 : out STD_LOGIC_VECTOR (6 downto 0));
end bin_7seg;

architecture Behavioral of bin_7seg is
--Generate component
COMPONENT bin_bcd
    Port ( a : in   STD_LOGIC_VECTOR (3 downto 0);
           u : out  STD_LOGIC_VECTOR (3 downto 0);
           d : out  STD_LOGIC_VECTOR (3 downto 0));
END COMPONENT;
COMPONENT bcd_7seg
    Port ( b : in   STD_LOGIC_VECTOR (3 downto 0);
           s : out  STD_LOGIC_VECTOR (6 downto 0));
END COMPONENT;
--Generate signal
SIGNAL u: STD_LOGIC_VECTOR (3 downto 0);
SIGNAL d: STD_LOGIC_VECTOR (3 downto 0);

begin
    --Instance component
    C_bin_bcd: bin_bcd
        PORT MAP(
            a => a,
            u => u,
            d => d
        );
    C_tens: bcd_7seg
        PORT MAP(
            b => u,
            s => seg_0
        );
    C_units: bcd_7seg
        PORT MAP(
            b => d,
            s => seg_1
        );
end Behavioral;
```