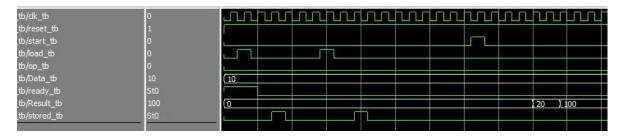
Tarea 5

Realizar el diseño, verificación e implementación de un multiplicador y divisor.

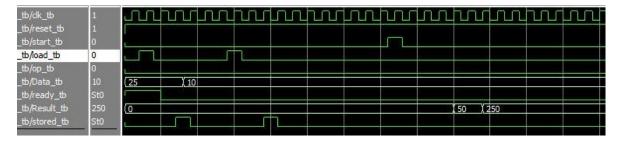
5x5

_tb/dk_tb	1	www			mmm	muluur	nununu	mmmmm
_tb/reset_tb	1							
_tb/start_tb	0			П				
_tb/load_tb	0							
_tb/op_tb	0							
_tb/Data_tb	5	(5						
_tb/ready_tb	St0							
_tb/Result_tb	25	(0			(5 (25			
_tb/stored_tb	St0							
			0.00	()				()

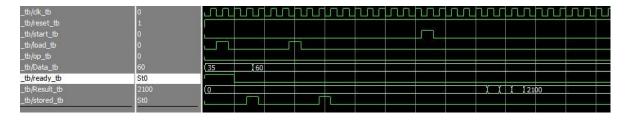
10x10



25x10



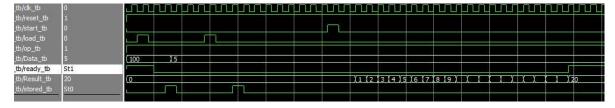
35x60



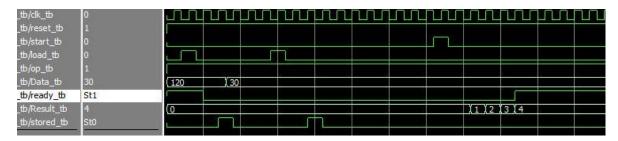
10/10

/Sequential_Multiplier_tb/dk_tb	0		M	M	M		ur		W	M.		TIT.	M	$\Box\Box$
/Sequential_Multiplier_tb/reset_tb	1													
/Sequential_Multiplier_tb/start_tb	0													
/Sequential_Multiplier_tb/load_tb	0			\vdash										
/Sequential_Multiplier_tb/op_tb	1													
/Sequential_Multiplier_tb/Data_tb	10	10												
/Sequential_Multiplier_tb/ready_tb	St1													
/Sequential_Multiplier_tb/Result_tb	1	(0					į.	1						
/Sequential_Multiplier_tb/stored_tb	St0													
	\$ S													

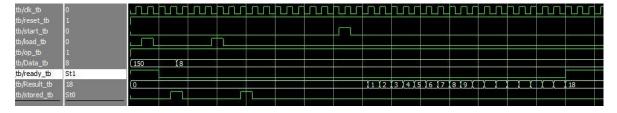
100/5



120/30

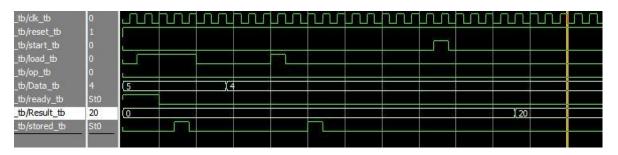


150/8



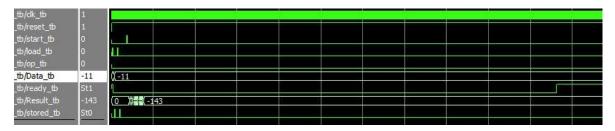
Load

Se observa que a pesar de que load permanezca en alto por un tiempo, eso no afecta el funcionamiento.



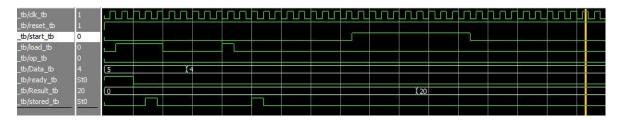
Ready

Se observa que la señal de ready se pone en alto una vez finaliza la operación.

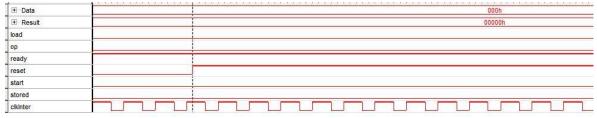


Start

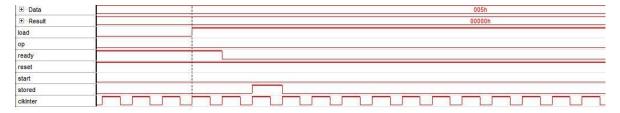
Se observa que a pesar de que start permanezca en alto por un tiempo, eso no afecta el funcionamiento.



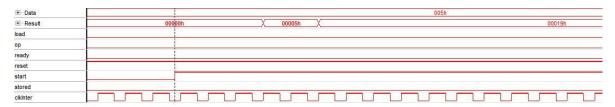
Signal Reset



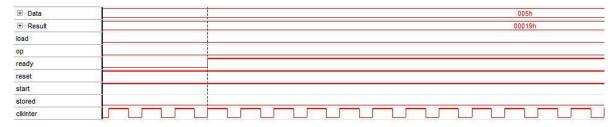
Signal Load y Stored



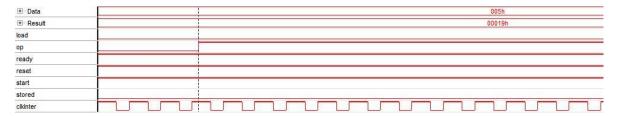
Signal Start



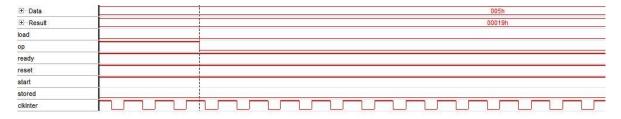
Signal Ready



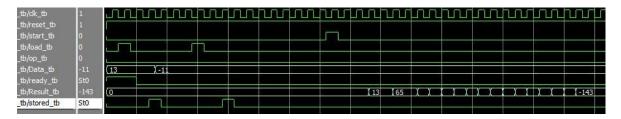
Signal OP=1



Signal OP=0



13x-11



-13x11

