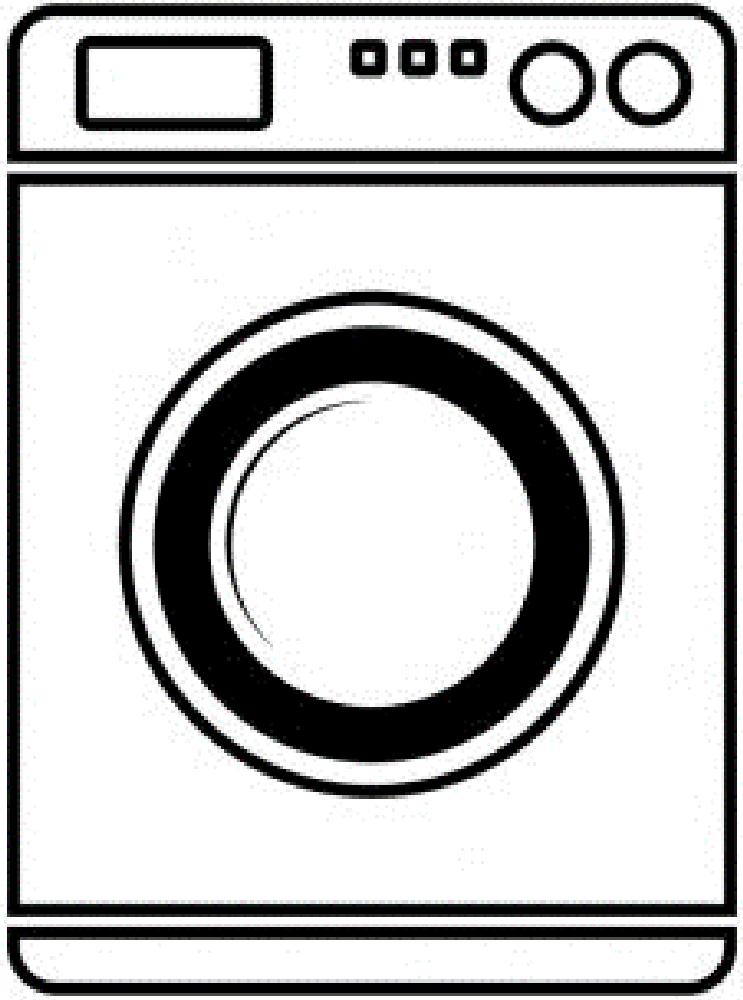
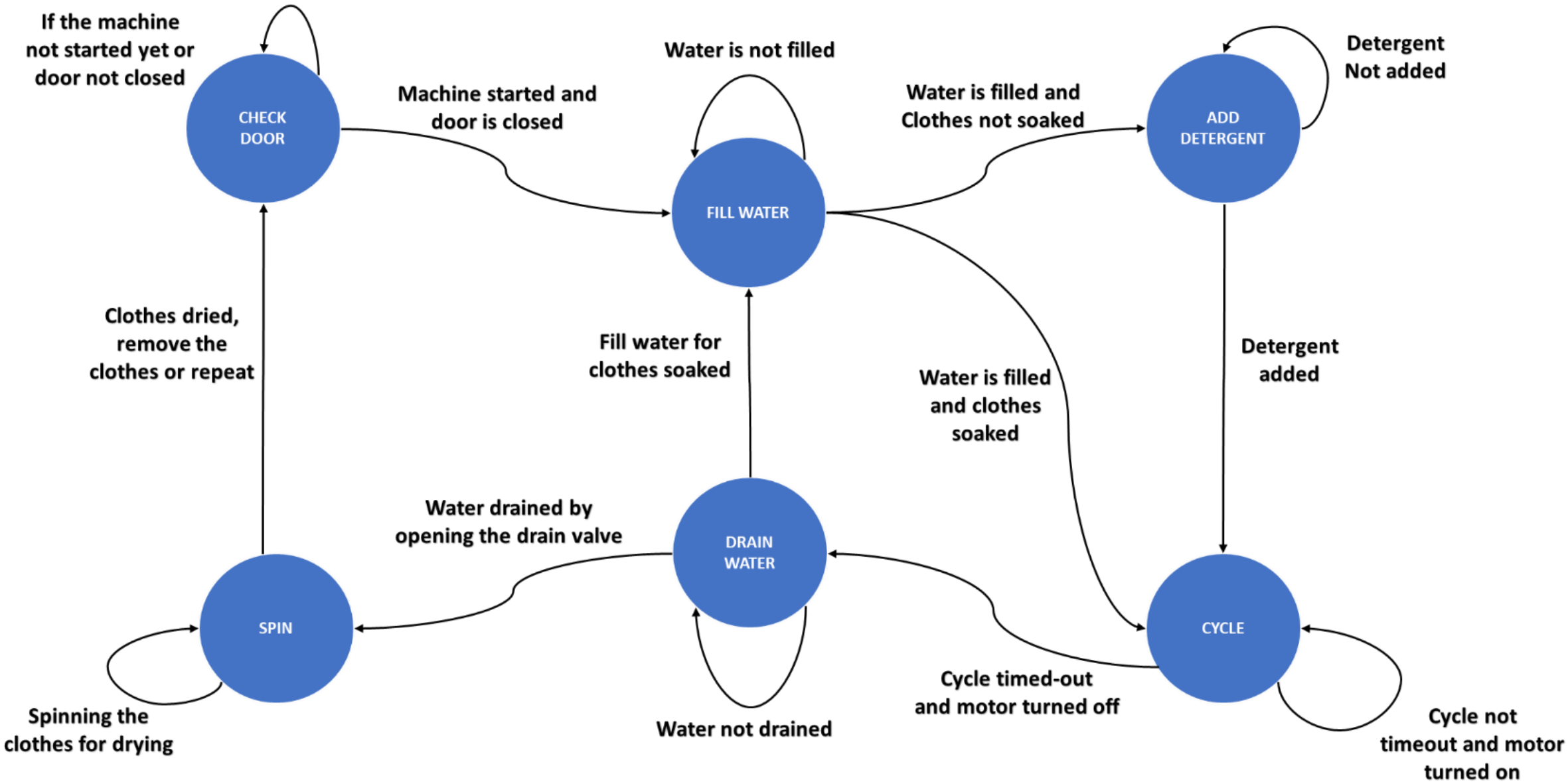
Automatic Washing Machine Control System Using Verilog HDL

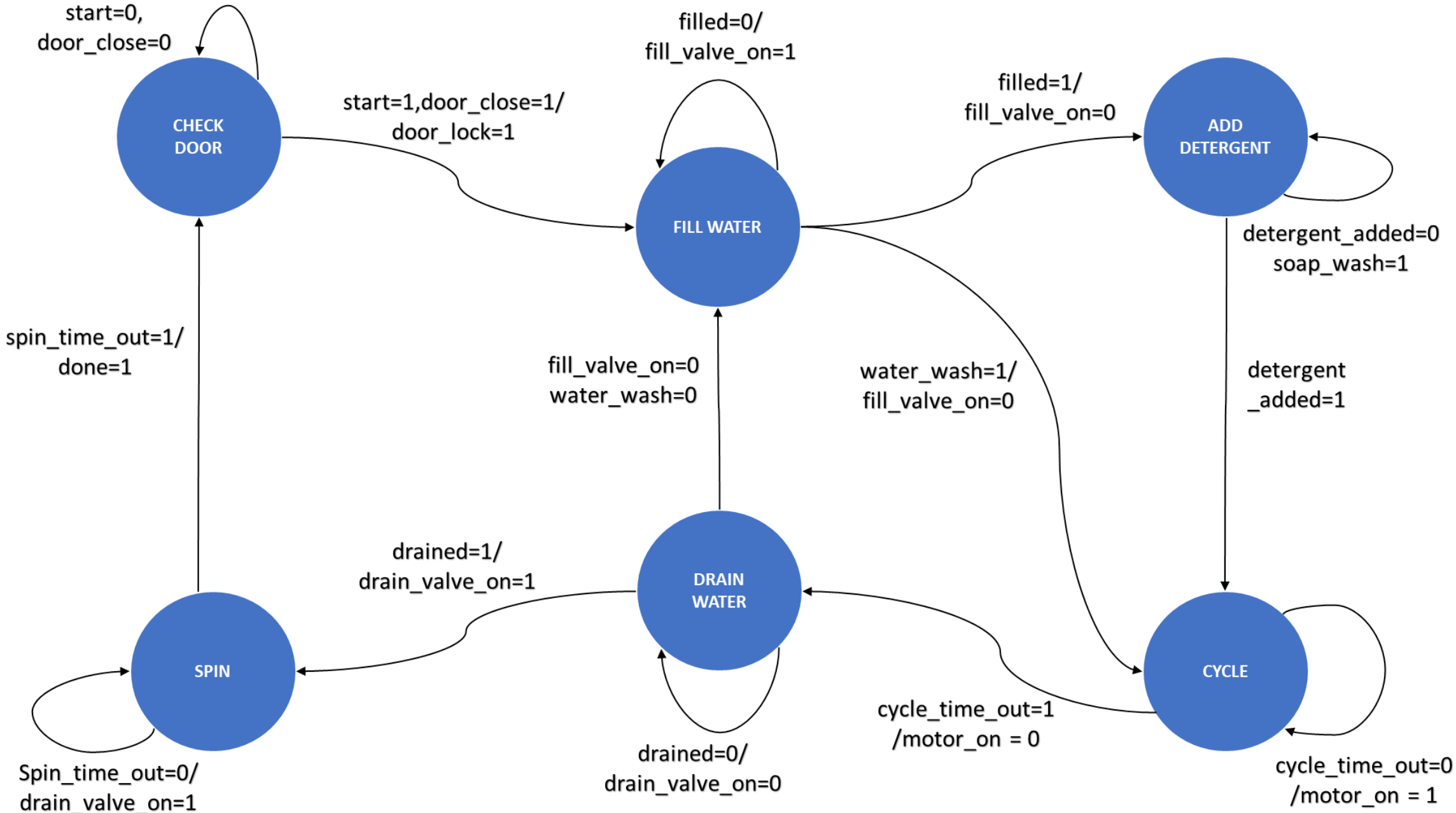


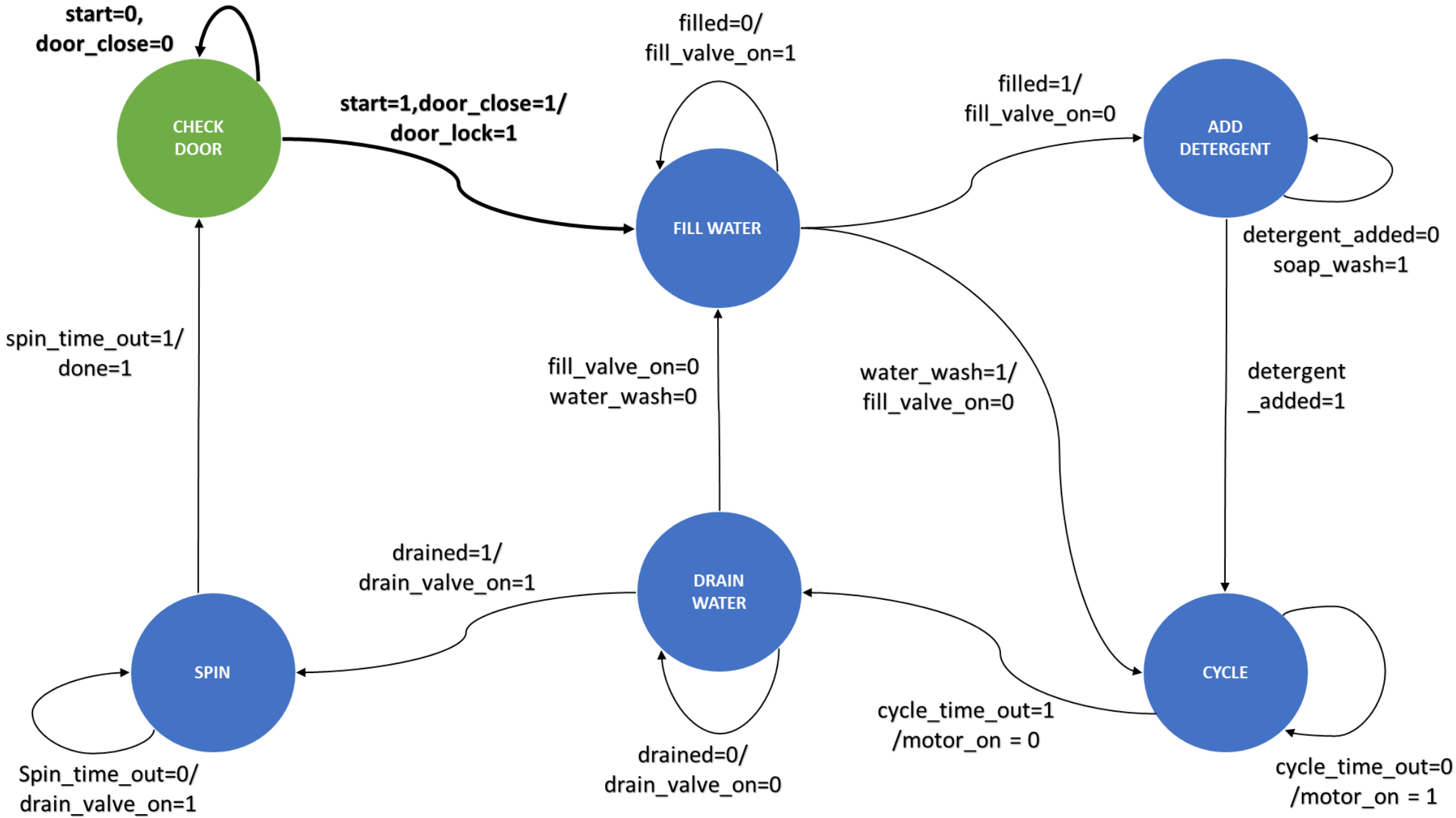
INTRODUCTION

- Various real life scenarios can be represented by Finite State Machines like control system of an automatic washing machine.
- Assigning the main stages of the process like Close door, fill water, add detergent, cycle, drain and spin various states that can be implemented as a State Machine.
- Writing a test bench to observe the working of the machine.
- Using Xilinx ISE 14.7 to implement the control system.

STATE DIAGRAM


If the machine not started yet or door not closed
CHECK DOOR
Machine started and door is closed
Water is not filled
FILL WATER
Water is filled and Clothes not soaked
ADD DETERGENT
Detergent Not added
Clothes dried, remove the clothes or repeat
Fill water for clothes soaked
Water is filled and clothes soaked
Detergent added
Water drained by opening the drain valve
DRAIN WATER
SPIN
CYCLE
Spinning the clothes for drying
Water not drained
Cycle timed-out and motor turned off
Cycle not timeout and motor turned on


start=0,
door_close=0
CHECK DOOR
start=1,door_close=1/
door_lock=1
filled=0/
fill_valve_on=1
FILL WATER
filled=1/
fill_valve_on=0
ADD DETERGENT
detergent_added=0
soap_wash=1
spin_time_out=1/
done=1
fill_valve_on=0
water_wash=0
water_wash=1/
fill_valve_on=0
detergent
_added=1
drained=1/
drain_valve_on=1
DRAIN WATER
SPIN
CYCLE
cycle_time_out=1
/motor_on = 0
Spin_time_out=0/
drain_valve_on=1
drained=0/
drain_valve_on=0
cycle_time_out=0
/motor_on = 1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Spin_time_out=0/
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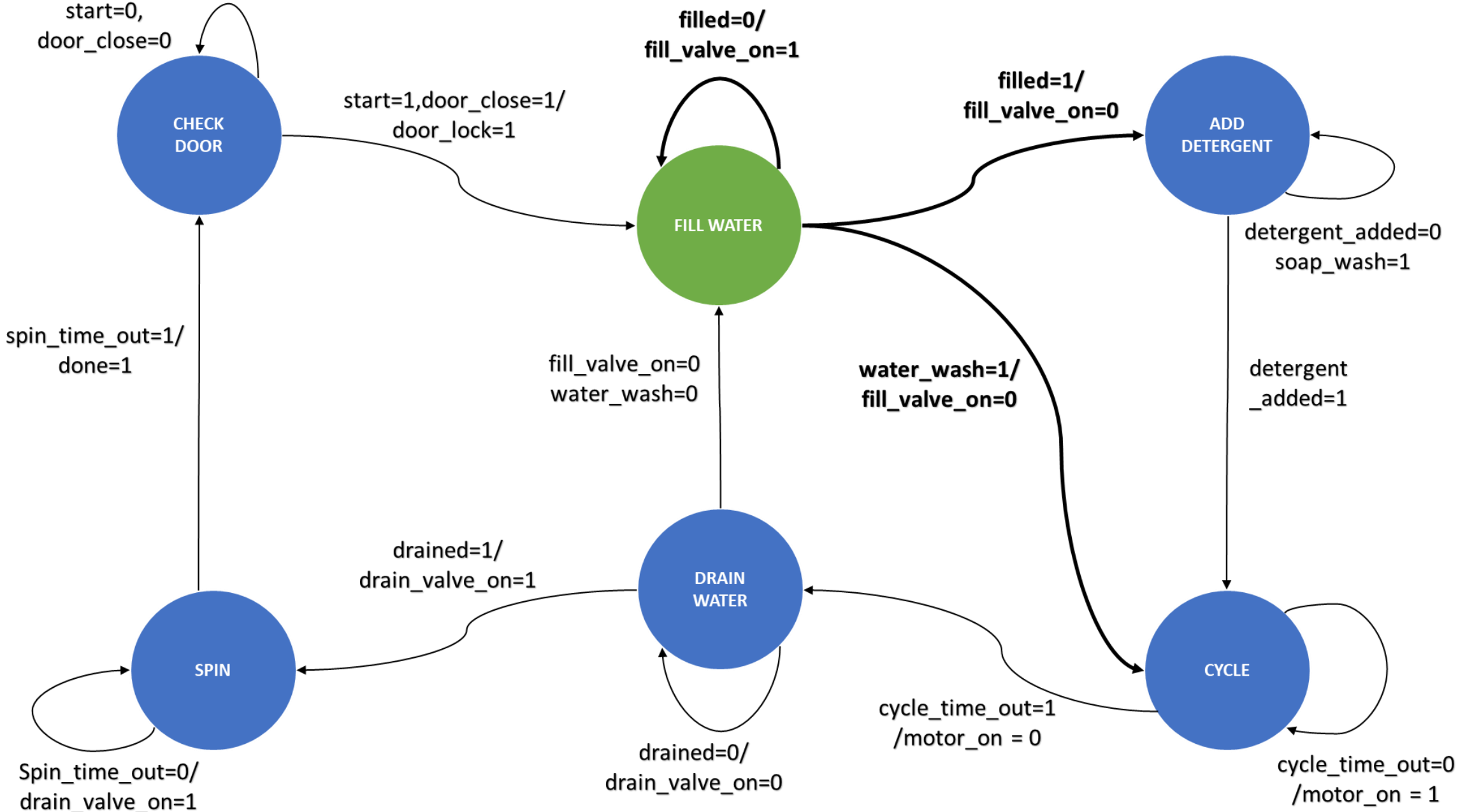
cycle_time_out=0
/motor_on = 1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detergent
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fill_valve_on=0
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water_wash=0
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DRAIN WATER
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CYCLE
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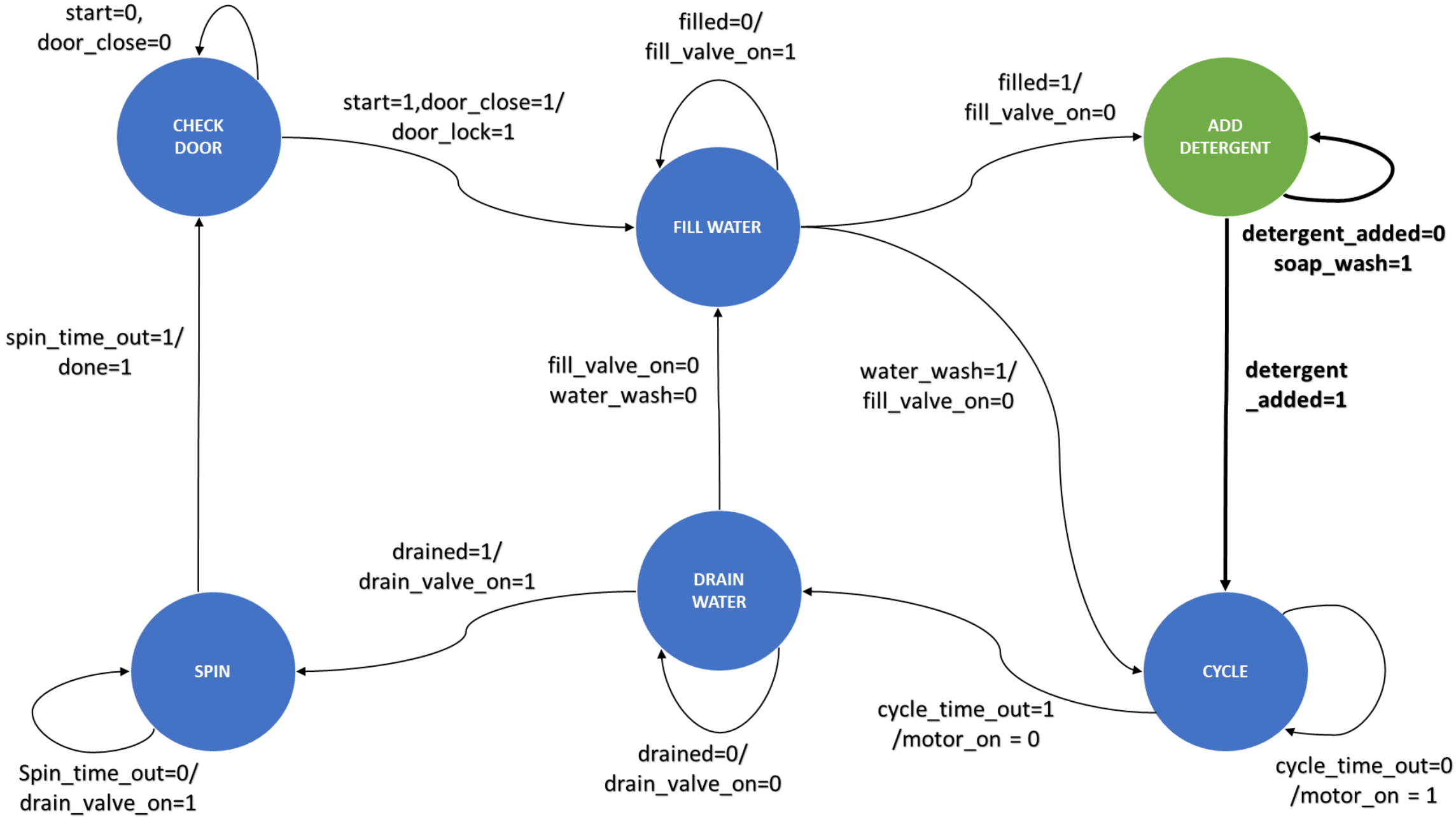
/motor_on = 0
cycle_time_out=0
/motor_on = 1
drained=0/
drain_valve_on=0
Spin_time_out=0/
drain_valve_on=1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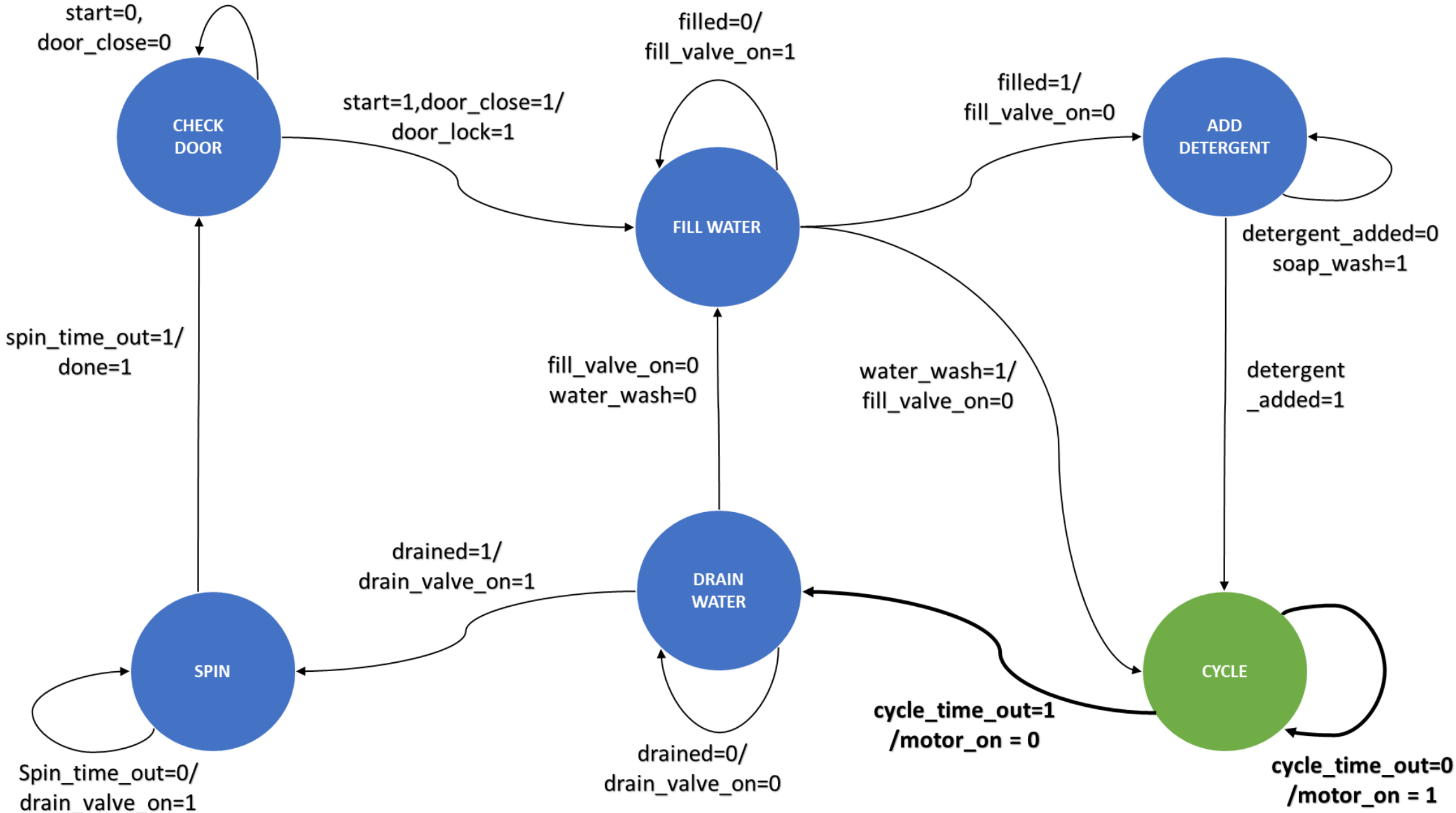
Spin_time_out=0/
drain_valve_on=1
drained=0/
drain_valve_on=0
cycle_time_out=0
/motor_on = 1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drain_valve_on=0
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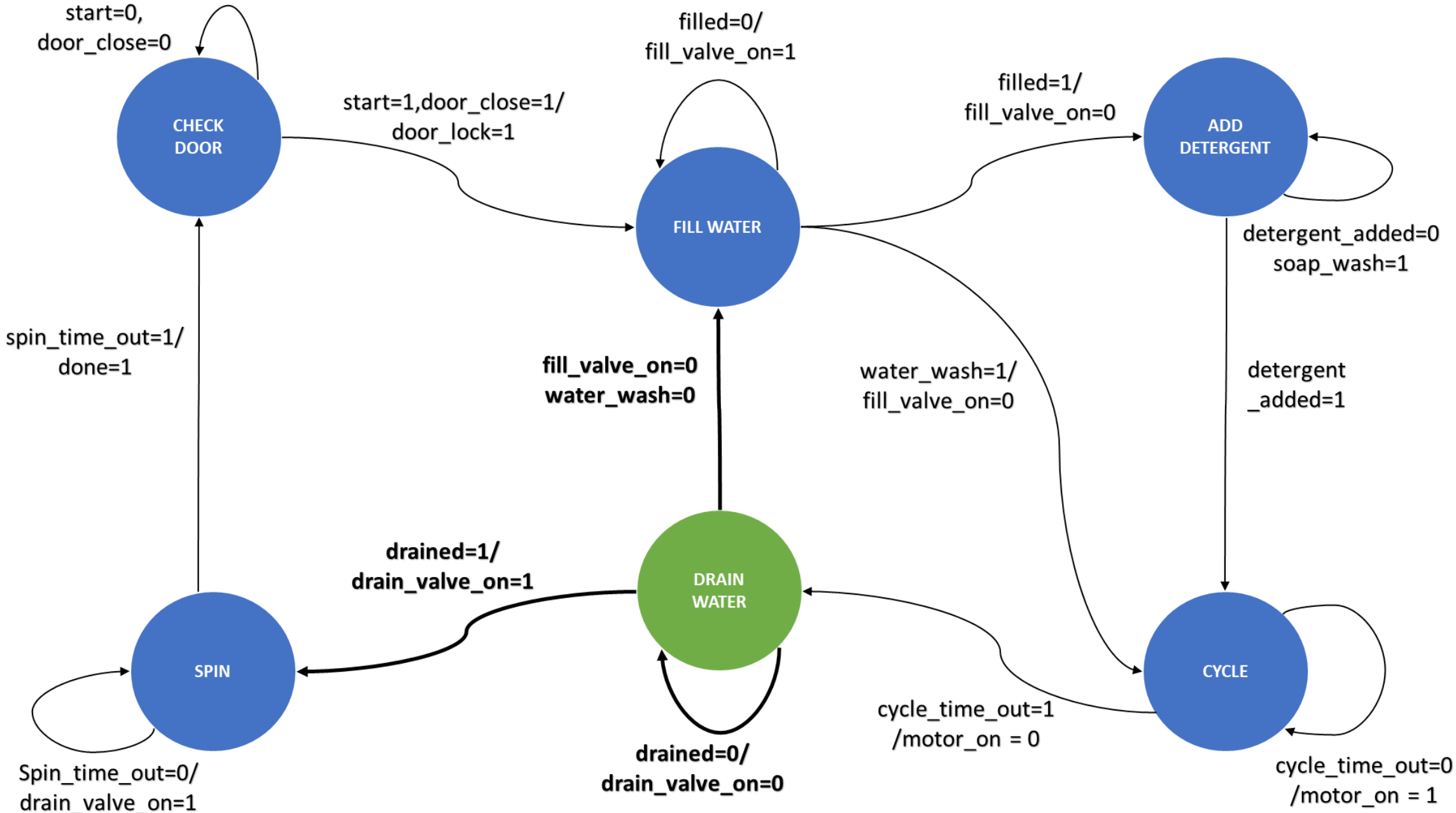
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soap_wash=1
spin_time_out=1/
done=1
fill_valve_on=0
water_wash=0
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detergent
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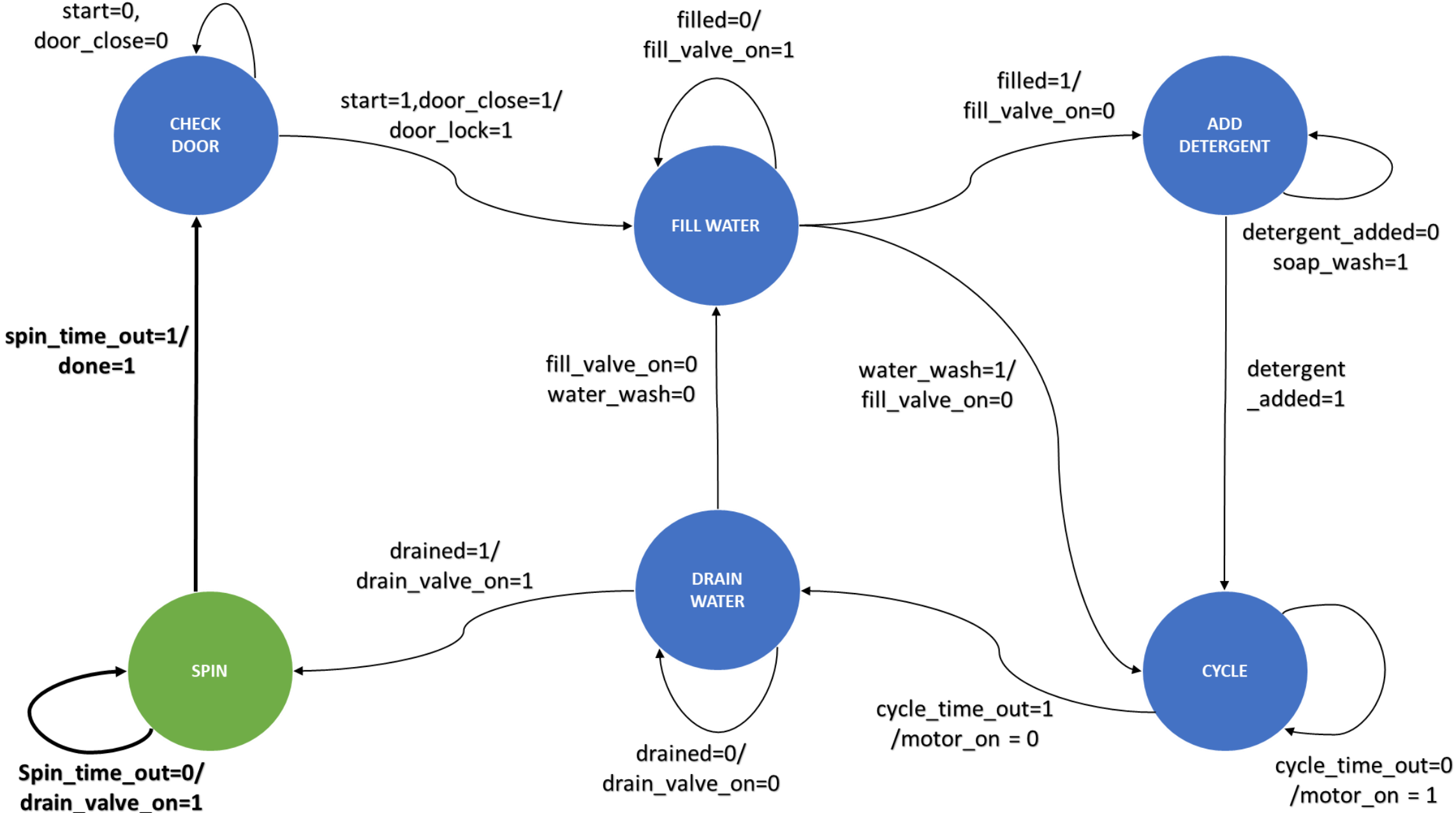
drain_valve_on=1
DRAIN WATER
SPIN
CYCLE
cycle_time_out=1
/motor_on = 0
Spin_time_out=0/
drain_valve_on=1
drained=0/
drain_valve_on=0
cycle_time_out=0
/motor_on = 1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soap_wash=1
detergent
_added=1
water_wash=1/
fill_valve_on=0
fill_valve_on=0
water_wash=0
spin_time_out=1/
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DRAIN WATER
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CYCLE
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/motor_on = 0
cycle_time_out=0
/motor_on = 1
drained=0/
drain_valve_on=0
Spin_time_out=0/
drain_valve_on=1

RESULTS

FUTURE SCOPE AND APPLICATIONS

1. The automatic washing machine has been implemented on Verilog HDL using Xilinx ISE.
2. The current project can be implemented on FPGA to demonstrate the code.
3. The project is based on Finite State Machine (FSM). Various other projects based on FSM can be implemented using the current project code as the basis.
4. More functionality may be included like different modes to wash the clothes based on the clothing material, temperature etc