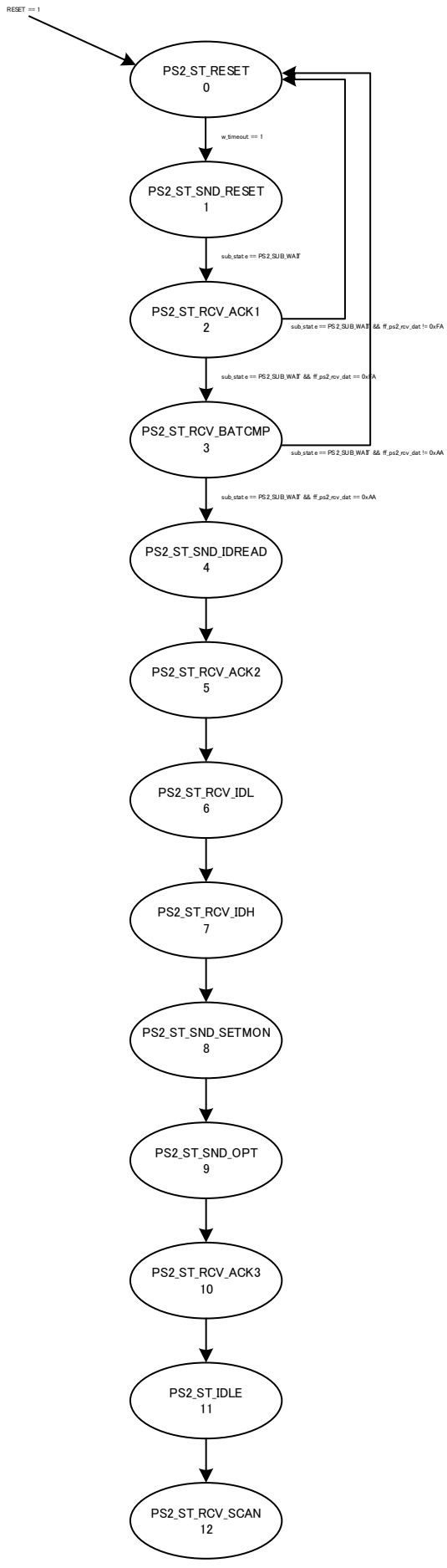
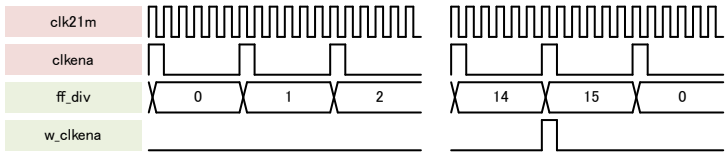

RESET == 1
PS2_ST_RESET
0
w_timeout == 1
PS2_ST_SND_RESET
1
sub_state == PS2_SUB_WAIT
PS2_ST_RCV_ACK1
2
sub_state == PS2_SUB_WAIT && ff_ps2_rcv_dat != 0xFA
sub_state == PS2_SUB_WAIT && ff_ps2_rcv_dat == 0xFA
PS2_ST_RCV_BATCMP
3
sub_state == PS2_SUB_WAIT && ff_ps2_rcv_dat != 0xAA
sub_state == PS2_SUB_WAIT && ff_ps2_rcv_dat == 0xAA
PS2_ST_SND_IDREAD
4
PS2_ST_RCV_ACK2
5
PS2_ST_RCV_IDL
6
PS2_ST_RCV_IDH
7
PS2_ST_SND_SETMON
8
PS2_ST_SND_OPT
9
PS2_ST_RCV_ACK3
10
PS2_ST_IDLE
11
PS2_ST_RCV_SCAN
12

信号の分周 (Signal division)



1st Gen OCM

clk21m
21.47727[MHz] : 46.56[nsec]

clkena
3.579578333[MHz] : 279.36[nsec]

w_clkena
4.469[usec]

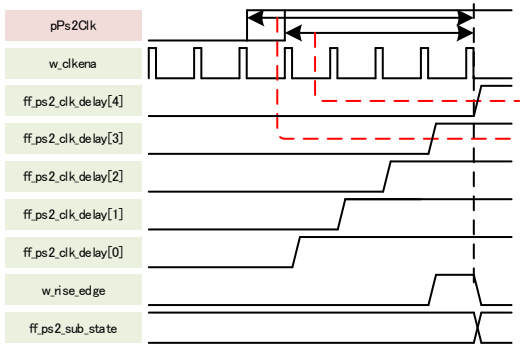
2nd Gen OCM

clk21m
21.484375[MHz] : 46.54[nsec]

clkena
3.5807292[MHz] : 279.27[nsec]

w_clkena
4.468[usec]

PS2CLKの検出 (PS2CLK detection)



1st Gen OCM

MINIMUM: rising edge 17.876[usec]

MAXIMUM: rising edge 22.345[usec]

Spec: 15[usec] .. 25[usec]

2nd Gen OCM

MINIMUM: rising edge 17.872[usec]

MAXIMUM: rising edge 22.340[usec]

Spec: 15[usec] .. 25[usec]