2.4G SOC
HW2171B

Data Sheet

- **Product Introduction**
- **Data Sheet**
- **Specifications**

Shanghai Neusoft carrier Microelectronics Co., Ltd.

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Ordering Information

Part NO.	Operating Voltage	OTP	SRAM	I / O	ADC	Timer	Package Type
HW2171BP4SD	2.1V ~ 3.6V	2K Words	64 Bytes	8 + 1INPUT	12-bit X 6ch	8-bit X 2	SOP16

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revise history

version	Modified Date	Change Summary
V1.0	2018-9-14 First edition.	
V1.1	2019-3-14	1. increase IAP Operation and interrupt enable bit GIE The supplement; 2. RF New register list PKG_RSSI Register Description; 3. change Logo .
V1.2	2019-4-22 change ACK Number of retransmissions will be described.	

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The first 1 Chapter chip Introduction

1.1 Outline

HW2171B It is a low cost, highly integrated 2.4GHZ ISM Band wireless SOC Chip, may be applied to the radio led Dimming, wireless HM, intelligent home, and other wireless data transmission and remote control and other fields. Integrated on-chip high-performance, low power consumption RF Transceivers and MCU .

a RF A peripheral circuit of the transceiver is simple, only few external passive components to form a complete 2.4G Wireless transceiver system.

RF Transceiver to transmit power up 8dBm , Receiver sensitivity can reach - 93dBm @ 250Kbps - 89dBm @ 1Mbps .

a MCU The low power consumption, comprising 2K Words of OTP Program memory space.

Chip features:

- **Working conditions**
  - Operating voltage range: 2.1V ~ 3.6V
  - range of working temperature:- 40 to 85 ℃
- **Package**
  - SOP16

MCU characteristic:

- Kernel
  - HR7P RISC CPU Kernel
  - 79 Article RISC
  - Machine cycle 2 System clock cycles
  - Reset vector is 000 H , Interrupt vector is located 004 H
  - Support for interrupt handling, 12 Interrupt sources
  - CPU Maximum operating frequency
    - 2MHz (VDD = 2.1 ~ 5.5V)
    - 20MHz (VDD = 3.0 ~ 5.5V)
- Storage resources
  - 2K Words OTP Program memory, 8 Level program stack
  - 64 Bytes SRAM Data Memory
  - Direct addressing the program memory, the relative addressing and read look-up table
  - Direct data memory addressing and indirect addressing support
- I / O port
  - Support for up to an available port 13 One (12 More I / O with 1 Input). Wherein the external ports are available 9 One (8 More I / O with 1 Inputs)
    - external PA port 6 One (PA0 ~ PA3 , PA5 , PA7)
    - external PB port 3 One (PB0 , PB1 , PB5)
    - Even within the port 4 One (PA6 , PB2 ~ PB4)
    - It is not a vacant internal port (PA4)
  - stand by 4 External interrupt port PINT0 ~ PINT3

- stand by 1 External key interrupt KINT Up support 8 Inputs (KIN0 ~ KIN7). Note: externally available 6 Input terminal, KIN4 with KIN6 unavailable.
- Arranged on a support independent internal weak / down input port
  - At room temperature, the matching accuracy ± 3% Within (VDD = 5V)
- It can be configured to support high-current ports

- Reset and Clock
  - A reset circuit embedded POR
  - The reset circuit embedded BOR
  - Embedded low voltage detection interrupt circuit
  - Support for external reset
  - Support independent hardware watchdog timer
    - stand by WDT Cycle Match Count register
  - Support internal high-frequency 16MHz RC Oscillation clock source
    - Frequency selection within the support section, the lowest frequency to be divided 32KHz
    - Factory calibrated accuracy of ± 2% (At room temperature 25 ℃)
  - Support internal low 32KHz RC Oscillator source (as WDT Clock source, and may be configured as a system clock source)
  - Support external oscillator
  - Supports clock frequency range 32KHz ~ 20MHz
  - Support system clock is switched high and low
- Peripherals
  - 2 road 8 Place PWM Base Timer T8P1 / T8P2
    - Timer Mode
    - After the support can be configured and configurable prescaler divider
    - The initial value of the counter may be arranged
    - It supports up to 9 Place PWM Output Accuracy
    - stand by PWM Complementary outputs and dead-time software configurable
    - Support interrupt generation
  - ADC ADC
    - stand by 12 Bit digital conversion accuracy
    - stand by 6 Analog input channels
    - Support supply voltage detection, an optional power supply voltage division ratio
    - Support for external reference source
    - Support internal reference source (reference source VDD / 4V / 3V / 2.1V Optional)
  - Support interrupt generation
- Low power consumption
  - IDLE Electric current
    - 3uA@5.0V , BOR / WDT Enable, 25 ℃, Typical Values
  - Dynamic current
    - 20uA @ 32KHz , 3.0V , 25 ℃, Typical Values

- 2mA @ 16MHz , 5.0V , 25 ℃, Typical Values

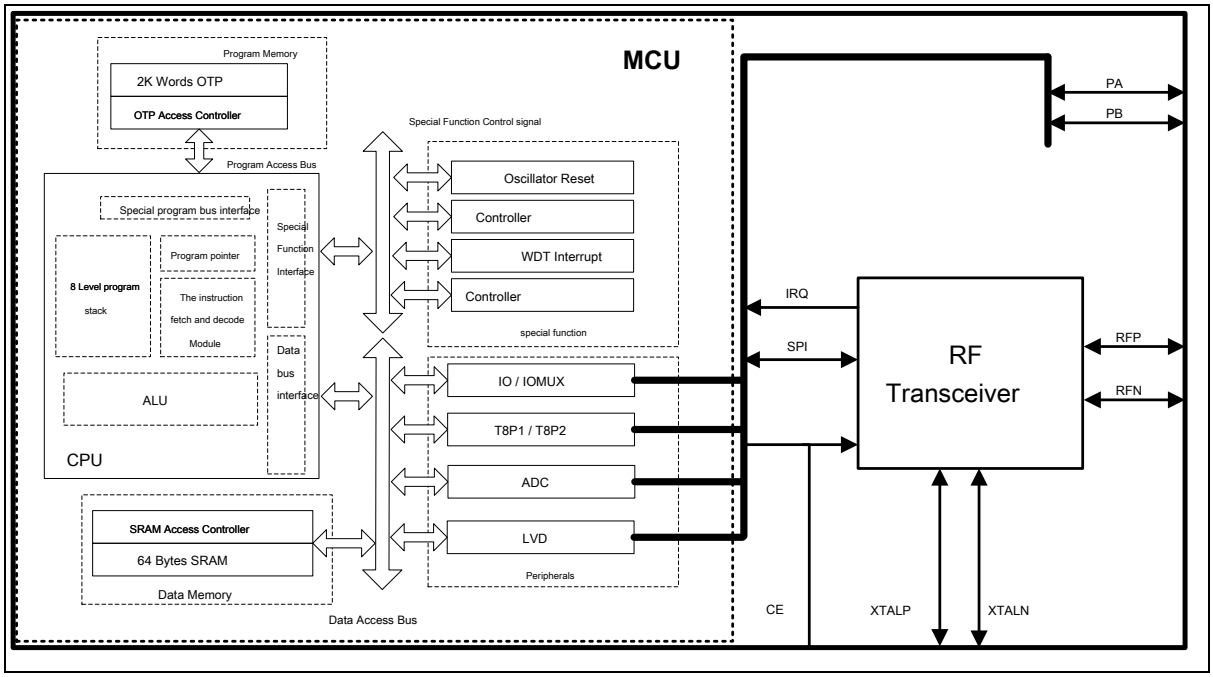
- Programming and debugging interface
  - Support online programming (ISP)interface
  - Support programming code encryption protection

RF Transceiver characteristics:

- Communication Features
  - The use of internationally accepted 2.4GHz ISM Working frequency 2402MHz ~ 2483MHz
  - stand by GFSK Modulation
  - stand by 250Kbps / 1Mbps Two data rates
  - Digital support RSSI measuring
  - stand by 4 PIPE Multiple logical channel transmission
- Receiver sensitivity (0.1% BER)
  - -89dBm @ 1Mbps
  - -9 3dBm @ 250Kbps
- Transmitter Output Power
  - Support transmitter output power controlled manually or automatically: - 40dBm ~ + 8dBm
- Power Features
  - Transmitter output power 0dBm When the chip power consumption is about 23mA
  - The receiver and the chip power consumption is about 20mA
  - IDLE Mode current is about 1.7mA
  - SLEEP Mode current is about 25uA
  - POWER DOWN Mode current is about 1.5uA
- Clock circuit
  - stand by 12 / 16MHz Crystal Oscillator

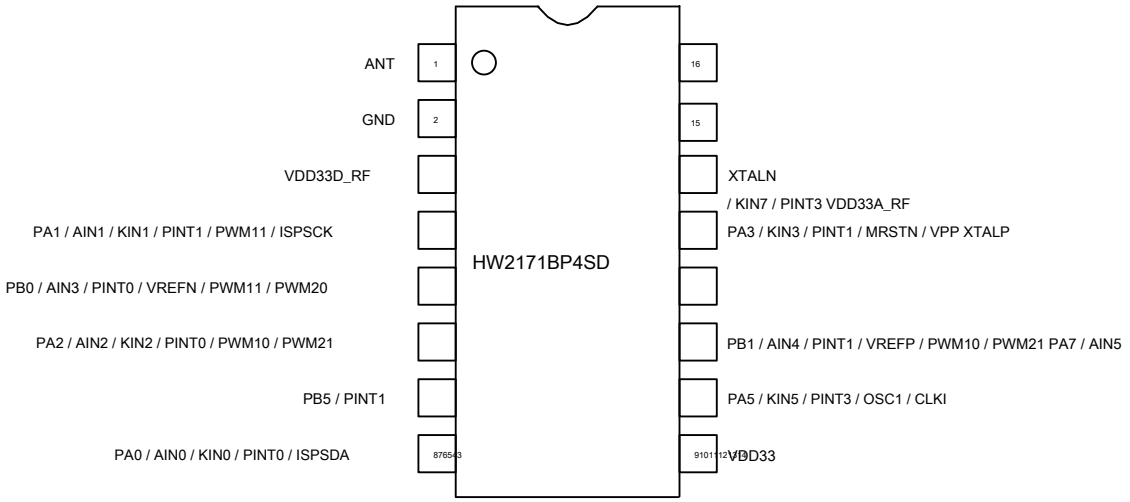
1.2 System Block Diagram

HW2171B The overall system diagram is shown below:



Map 1-1 System block diagram showing the internal structure

1.3 Pin allocation map



Map 1-2 Pin allocation map

1. 3.1 Pin Description

Pin Number	Pin Name	Pin Function	Pin Description
1	ANT	RF end	RF RF transceiver end interface, external RF Matching network
2	GND	Ground	Ground (0V)
3	VDD33D_RF	Digital Power Input RF Digital input power transceiver	
4	PA1 / AIN1 / KIN1 / PINT1 / PWM11 / ISPSCK General Purpose Input Output I SP Serial programming / debugging clock input, multiplexed with ADC Input, external interrupt input, PWM Output, etc.		
5	PB0 / AIN3 / PINT0 / VREFN / PWM11 / PWM20 General Purpose Input Output General IO , Reusable as ADC Input, external interrupt inputs In, PWM Output, etc.		
6	PA2 / AIN2 / KIN2 / PINT0 / PWM10 / PWM21 General Purpose Input Output General IO , Reusable as ADC Input, external interrupt inputs In, PWM Output, etc.		
7	PB5 / PINT1	General Purpose Input Output General IO , Reusable external interrupt inputs, etc.	
8	PA0 / AIN0 / KIN0 / PINT0 / ISPSDA	General Purpose Input Output ISP Serial programming / debugging data input and output, reusable for ADC Input, external interrupt input, etc.	
9	VDD33	Digital Power Input MCU Digital power input terminal	
10	PA5 / KIN5 / PINT3 / OSC1 / CLKI	General Purpose Input Output General IO , Can be used as an external interrupt input, input external crystal And so on into the	
11	PB1 / AIN4 / PINT1 / VREFP / PWM10 / PWM21 General Purpose Input Output General IO , Reusable as ADC Input, external interrupt inputs In, PWM Output, etc.		
12	PA7 / AIN5 / KIN7 / PINT3	General Purpose Input Output General IO Can be used for ADC Input, external interrupt input, Wait	
13	PA3 / KIN3 / PINT1 / MRSTN / VPP	Universal input Universal input, the reusable external reset input, ed Cheng high voltage input, an external interrupt input, etc.	
14	XTALN	Analog Output	RF The transceiver output of crystal oscillator

Pin Number	Pin Name	Pin Function	Pin Description
15	XTALP	Analog Input	RF Input of transceiver crystal oscillator
16	VDD33A_RF	Analog Power Input	RF Analog input power transceiver

table 1-1 Pin Description table

1.3.2 Pin Multiplexing description

Here are multiplexed pins Specific Multiplexing Happening:

Pin name	Input Output Pin	Multiplexing Type	Type A / D		Port Description	Remark
PA0 / AIN0 / KIN0 / PINT0 / ISPSDA	PA0	TTL	CMOS	D	Common I / O	Weak separately enabled / down
	AIN0	-	- A		ADC Analog channels 0	
	KIN0	TTL	- D		External key wake-up input 0	
	PINT0	TTL	- D		External interrupt input port 0	
	ISPSDA	TTL	CMOS	D	Serial data input and output programming	
PA1 / AIN1 / KIN1 / PINT1 / PWM11 / ISPSCK	PA1	TTL	CMOS	D	Common I / O	Weak separately enabled / down
	AIN1	-	- A		ADC Analog channels 1	
	KIN1	TTL	- D		External key wake-up input 1	
	PINT1	TTL	- D		External interrupt input port 1	
	PWM11	- CMOS		D	T8P1 PWM Export	
	ISPSCK	TTL	- D		Serial Programming Clock input	
PA2 / AIN2 / KIN2 / PINT0 / PWM10 / PWM21	PA2	TTL	CMOS	D	Common I / O	Weak separately enabled / down
	AIN2	-	- A		ADC Analog channels 2	
	KIN2	TTL	- D		External key wake-up input 2	
	PINT0	TTL	- D		External interrupt input port 0	
	PWM10	- CMOS		D	T8P1 PWM Complementary Output	
	PWM21	- CMOS		D	T8P2 PWM Export	
PA3 / KIN3 / PINT1 / MRSTN / VPP	PA3	TTL	CMOS	D	Common I	Can be individually enabled weak pull
	KIN3	TTL	- D		External key wake-up input 3	
	PINT1	TTL	- D		External interrupt input port 1	
	MRSTN	TTL	- D		Master reset input	
	VPP	Power	-	-	OTP Programming high voltage input	
	KIN4	TTL	- D		External key wake-up input 4	
	PINT2	TTL	- D		External interrupt input port 2	
	OSC2	- CMOS		A	Crystal / resonator output	
	CLKO	- CMOS		D	Fosc / 16 Reference clock output	
PA5 / KIN5 / PINT3 / OSC1 / CLKI	PA5	TTL	CMOS	D	Common I / O	Weak separately enabled / down
	KIN5	TTL	- D		External key wake-up input 5	
	PINT3	TTL	- D		External interrupt input port 3	
	OSC1	TTL	- A		Crystal / resonator input	
	CLKI	TTL	-	A / D	Clock input	

Pin name	Input Output Pin	Multiplexing Type	Type A / D		Port Description	Remark
PA7 / AIN5 / KIN7 / PINT3	PA7	TTL	CMOS	D	Common I / O	Weak separately enabled / down
	AIN5	-	- A		ADC Analog channels 5	
	KIN7	TTL	- D		External key wake-up input 7	
	PINT3	TTL	- D		External interrupt input port 3	
PB0 / AIN3 / PINT0 / VREFN / PWM11 / PWM20	PB0	TTL	CMOS	D	Common I / O	Weak separately enabled / down
	AIN3	-	- A		ADC Analog channels 3	
	PINT0	TTL	- D		External interrupt input port 0	
	VREFN	-	- A		ADC External negative reference voltage terminal	
	PWM11	- CMOS		D	T8P1 PWM Export	
	PWM20	- CMOS		D	T8P2 PWM Complementary Output	
PB1 / AIN4 / PINT1 / VREFP / PWM10 / PWM21	PB1	TTL	CMOS	D	Common I / O	Weak separately enabled / down
	AIN4	-	- A		ADC Analog channels 4	
	PINT1	TTL	- D		External interrupt input port 1	
	VREFP	-	- A		ADC External reference voltage positive terminal	
	PWM10	- CMOS		D	T8P1 PWM Complementary Output	
	PWM21	- CMOS		D	T8P2 PWM Export	
	PINT1	TTL	- D		External interrupt input port 1	
PB5 / PINT1	PB5	TTL	CMOS	D	Common I / O	Weak separately enabled / down
	PINT1	TTL	- D		External interrupt input port 1	
VDD	VDD	Power	-	-	power supply	-
VSS	VSS	Power	-	-	, The 0V Reference Point	-

table 1-2 Pin Description

Note 1 : A = simulation, D = digital; MRSTN It represents active low; Note 2 :except PA3 In addition, all common data I / O Are TTL Schmitt input and CMOS Output drive, PA3 for TTL Input; Note 3 : T8P1 , T8P2 of PWM Output and complementary output ports can be configured to output;

1. 3.3 Interconnector

MCU with RF Digital Transceiver Interface is a direct Internal connection, internal connection relation shown in the following table:

No. RF transceiver(I / O)		MCU (I / O)	Explanation
1	CSN (I)	PA6 (O)	RF transceiver SPI The chip select input (active low), and internal MCU of PA6 Connected, PA6 Should be set to the output port.
2	SCK (I)	PB2 (O)	RF transceiver SPI A clock input port, and an internal MCU of PB2 Connected, PB2 Should be se to the output port.
3	MOSI (I)	PB3 (O)	RF transceiver SPI Input port, and an internal MCU of PB3 Connected, PB3 Should be set to the output port.
4	MISO (O)	PB4 (I)	RF transceiver SPI Output port, and an internal MCU of PB4 Connected, PB4 Should be set to the input port.
5	IRQ (O)	-	RF Transceiver internal interrupt output floating, so the interrupt can not be used, with the only access query.
6	CE (I)	-	RF Transceiver chip enable input terminal, connected to the internal 3.3V Power supply terminal, i.e., enabled by default.

table 1-3 Interconnector

1. 3. 4 MCU Note dangling feet

requires attention MCU Internal floating foot initial programming, the output should be set to a low level, in order to ensure the normal operation of the chip.

DESCRIPTION floating foot the following table:

No. MCU The extending Name Set status Special register < bit>			
1	PA4	Output low	PBT <4>

table 1-4 MCU The extending table Description

1. 3. 5 HW2171B with HW2171 Differences pin control

HW2171B Connected to the upper portion of a pin plate HW2171 Different, need to pay attention when in use. Differences control pin given below,

The following table Below:

Pin name	HW2171B	HW2171
PA4	Internal floating	External connections
PB5	External connections	Internal floating
CE	An internal power source terminal connected	The external connection may be connected GPIO Port or a power supply termina.

table 1-5 Differences in the two versions of the chip pins comparison table

The first 2 chapter MCU - Core Features

2. 1 CPU Core Overview

- Core Features
  - Harvard-type high-performance RISC CPU Kernel
  - 79 Article RISC
  - The system clock frequency of up to 20MHz
  - Machine cycle 2 System clock cycles
  - Support for interrupt handling, a total of 12 Interrupt sources

twenty two The system clock cycle and machine

System clock frequency (Fosc) Up to 20MHz . Two system clock cycles to generate two quadrature clocks do not overlap within the chip by the clock generator phase1 (p1), phase2 (p2).

Two non-overlapping quadrature clock cycles one machine cycle. If the system clock frequency is 4MHz , A machine cycle time 500ns .

twenty three Instruction Set Overview

use HR7P series 79 Article RISC system.

Apart from some conditional jump instructions and program flow control is bis (machine) cycle instruction, other instructions are single (machine) cycle instruction.

Specific Instruction set details, see " 9 chapter MCU- Instruction Set".

twenty four Special Function Register

CPU Related register comprising 11-bit Program Counter PCRL / PCRH Program status word register PSW And accumulators A register AREG . Wherein the program status register PSW For storing various status flags, including a program pop / push overflow, negative flag, overflow flag, a zero flag, Digit carry / borrow bit half and full carry or borrow bit full like.

PSW : Program status word register

Bit	7	6	5	4	3	2	1	0
Name	-	UF	OF	N	OV	Z	DC	C
R / W	-	R	R	R / W	R / W	R / W	R / W	R / W
POR	x	0	0	x	x	x	x	x "x" :unknown

Bit 7 Reserved for future use

Bit 6 UF : Program Stack Overflow flag

0 : The program does not overflow the stack

1 : Program Stack Overflow

Bit 5 OF : Program push-out flag

0 : The program does not overflow onto the stack

1 : Overflow program push

Bit 4 N : Negative flag

0 : Signed arithmetic or logic operation result is positive

1 : The result is negative

Bit 3 OV : Overflow flag

0 : Signed arithmetic overflow does not occur

1 : Overflow

Bit 2 Z : Zero flag

0 : Arithmetic or logic operation result is not zero

1 : Result of arithmetic or logic operation is zero

Bit 1 DC : Half Carry or Borrow flag

0 : Low nibble Carry or borrow from the low nibble

1 : Low nibble bits or lower four no borrow

Bit 0 C : All carry or borrow bit full

0 : Carry or borrow

1 : There is no carry or borrow

Note 1 : Only part of the instruction PSW Write to a register, comprising JDEC , JINC , SWAP , BCC , BSS , BTT , MOVA with SETR . Other instructions PSW Write register operation, affects only the corresponding status flag according to the operation result. Note 2 : OF with UF Flag bit is read, only the power-on reset, reset command, and MRSTN Reset will be cleared, reset does not affect the other two flag.

AREG :accumulator A register								
Bit	7	6	5	4	3	2	1	0
Name	AREG <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	x	x	x	x	x	x	x	x "x" :unknown

Bit 7 ~ 0 AREG <7: 0> : The value of the accumulator

PCRL : Program Counter Low 8 Place								
Bit	7	6	5	4	3	2	1	0
Name	PCR <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 PCR <7: 0> : Program Counter Low 8 Place

PCRH : Program Counter High 3 Place								
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	P CR <10: 8 >		
R / W	-	-	-	-	- R / W		R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 3 Reserved for future use

Bit 2 ~ 0 PCR <10: 8> : Program Counter High 3 Place

The first 3 chapter MCU - Storage Resource

3.1 Outline

This chip bus Harvard architecture, the program address space and the data address spaces independent of each other.

Chip memory resources include:

- 2K Words OTP A program memory;
- 64 byte SRAM

among them OTP The program memory is mapped into the address space of the program, SRAM Data memory is mapped into the data address space.

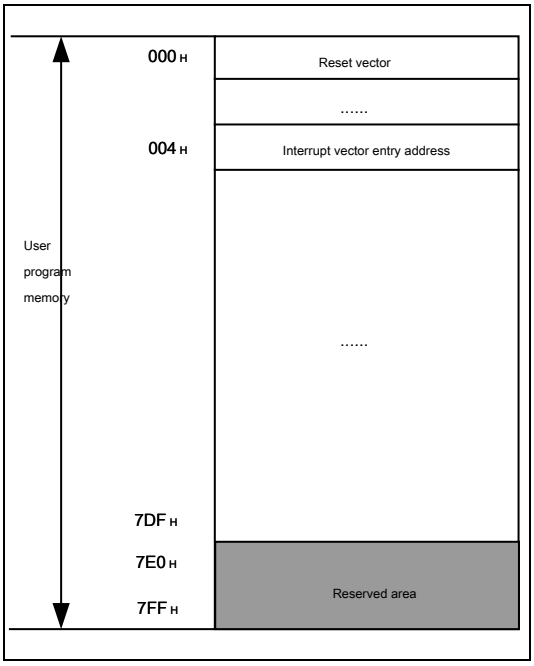
3.2 Program Memory

3. 2.1 Outline

OTP A program memory for storing a user program. Since the bit width of the chip instruction 16 Bit (2 Bytes), thus 2K Words OTP The program memory is mapped into the address space of the program 000 H - 7FF H ,among them 7E0 H - 7FF H Reserved area. Each address corresponds access 16 Bits wide (2 Bytes) of the memory cell. by 11 Bit program counter PC Procedural addressing.

Reset vector is 000 H Interrupt vector address is located 004 H ,stand by 8 Level hardware stack.

3. 2.2 Program address map schematic



Map 3-1 Program address map

3. 2.3 Program Counter (PC)

The program counter is stored in the address of the next instruction to be executed. PC Are automatically added to each instruction cycle 1 ,unless PC Value is rewritten exception or an interrupt. 11 Bit program counter PC <10: 0> No actual physical address, can not be read, addressable 2K Program memory space 000 H - 7FF H Beyond the address range can cause PC Cycle (and from 000 H Began a visit).

PC <7: 0> accessible PCRL Register read / write operation for reading / writing, and PC <10: 8> by PCRH Register indirect (e.g. RCALL , CALL , GOTO And other instructions) assignment.

When the chip is reset, PCRL , PCRH with PC It will be cleared. PC Hardware stack operation does not affect PCRH Value.

Note: all kinds of instructions PC Impact:

1. Modified by direct instruction PC When the value of PCRL Is the destination, the operation can be directly modified PC <7: 0> , which is PC <7: 0> = PCRL <7: 0> ;
   The operation PC <7: 0> But also the implementation of PC <10: 8> = PCRH <2: 0> Therefore, modifications PC When, should be modified PCRH <2: 0> , And then modify PCRL <7: 0> .
2. carried out RCALL Instruction, PC <7: 0> To register R The value; and PC <10: 8> = PCRH <2: 0> .
3. carried out CALL , GOTO Instruction, PC <10: 0> For the instruction 11 Bit immediate I (Operand).
4. carried out LCALL When the instruction, which is a two-word instructions Total 16 Bit immediate I (Operand). PC <10: 0> Modified to the 16 Bit immediate I Low value 11 Bit; at the same time PCRH <2: 0> It is modified I <10: 8> Value.
5. carried out AJMP When the instruction, which is a two-word instructions Total 16 Bit immediate I (Operand). PC <10: 0> Modified to the 16 Bit immediate I Low value 11 Bits, while PCRH <2: 0> change into I <10: 8> Value.
6. carried out PAGE Instruction, PCRH <7: 3> The value is the number of the instruction immediately I replace. (The size of this chip program memory is 2K Words , therefore PCRH <7: 3> Is fixed to all zeros, execute PAGE After instruction PC Values are not affected)
7. The implementation of other instructions, PC Automatic value 1 .

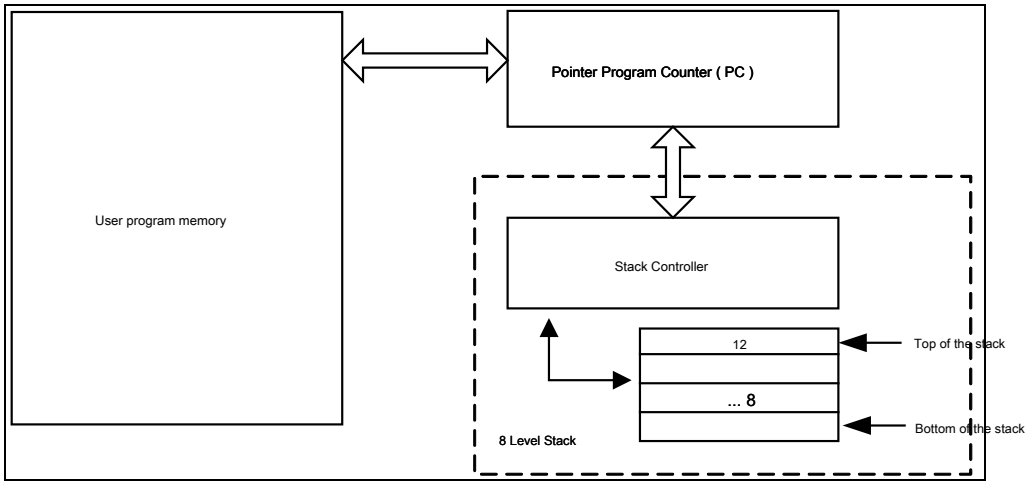
Application examples: The PCRL Instructions for the application target register

```
..... MOVI
                pageaddr
MOVA    PCRH    ; Set the table page address
MOVI    tableaddr   ; Offset is set to A register
CALL    TABLE   ; Subroutine call mode look-up table
.....
TABLE:
ADD     PCRL, F ; PC Plus the offset, the address of the access point
RETIA   0X01
RETIA   0X02
RETIA   0X03
.....
```

3. 2.4 Program stack

There chip 8 Level program stack (hardware stack), and the stack bit wide PC Equal bits wide, for PC The push and pop. carried out CALL , LCALL with RCALL After interruption of instructions or in response, PC Automatically pushed onto the stack; when performed RET , RETIA or RETIE Instruction, the stack will push the value of a recent return to PC .

Program stack only supports 8 Level buffer operation, that only saves the last program stack 8 PUSH value, for continuously for more than 8 Second push operation, the first 9 Data so that the first push times 1 Times push data loss. Similarly, more than 8 Times in a row out of the stack, the first 9 Ci pop operations, so that the program flow may be uncontrollable. After reset, the stack pointer points to the top of the stack again.



Map 3-2 Stack schematic

3. 3 IAP access OTP operating

3. 3. 1 OTP Memory

OTP The memory is a programmable memory, in VPP Multiplexing application of high pressure port 8.45V When, by IAP For unprogrammed off OTP Address unit control programming software. IAP Word write operation (Word) As a unit, by FRA (FRAH , FRAL) Addressing. when OTP Memory IAP When a write operation CPU Core suspended, the software needs to close the global interrupt enable bit GIE (INTG <7>), And judges GIE Whether the register is cleared successfully, if not cleared, you need software to perform clear operation again until cleared successfully, peripherals can be preset state to continue running, peripheral interrupt request will set the corresponding interrupt flag. when IAP When the writing operation is completed, CPU Core resumes execution, the software then enables the global interrupt enable bit GIE , The corresponding interrupt handling.

3. 3.2 Table read instruction

HR7P 79 Instruction set includes 8 Article table read instructions.

Look-up table read instructions:

Table look-up read command for FRA (FRAH , FRAL) Pointed OTP A cell address word (Word) Read ROMD (ROMDH , ROMDL)in.

- TBR
- TBR # 1
- TBR_1
- TBR1 #

Look-up table write instructions: This chip look-up table write instruction reserved for future use.

- TBW
- TBW # 1
- TBW_1
- TBW1 #

The specific operation may refer to the table read instruction "on 9 chapter MCU- Instruction Set"

3. 3. 3 IAP program

IAP By programming operation IAPC Control register ROMD (ROMDH , ROMDL Content) is written FRA (FRAH , FRAL) Points OTP Address unit. IAP Programmatic access to address space 200H ~ 7DFH . Recommends that each address programming is complete, look-up table read verification is successful, if unsuccessful needs to return to the program operation until the read verification is successful then the follow-up program address space. Single address programming, programming for at least 2ms .

Application routines 1 : IAP program

```
MOVI    0x02            ;will 55AAH Write OTP of 0210H Address unit
MOVA    FRAH
MOVI    0x10
MOVA    FRAL
MOVI    0xAA
MOVA    ROMDL
MOVI    0x55
MOVA    ROMDH
BCC     INTG, GIE       ; Close the global interrupt
JBC     INTG, GIE       ; Determine whether the global interrupt cleared
GOTO    $ -2
BSS     IAPC, IAPEN     ;Enable IAP operating
BSS     IAPC, IAPGO     ;trigger IAP operating
WAIT:
JBC     IAPC, IAPGO
GOTO WAIT BSS
        INTG, GIE       ; Open global interrupt
……
```

Application routines 2 : IAP Read look-up table

```
MOVI    0x02            ; Read a data memory 0210H unit
MOVA    FRAH
MOVI    0X10
MOVA    FRAL
TBR                     ; Table look-up read command to read data ROMDH / L register
MOV     ROMDH, 0 ...
... MOV
        ROMDL, 0 ...
...
```

3. 3.4 Special Function Register

FRAL : Low lookup table address register 8 Place

Bit	7	6	5	4	3	2	1	0
Name	FRA <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	x	x	x	x	x	x	x	x

" x ":unknown

Bit 7 ~ 0 FRA <7: 0> : Low address look-up table 8 Place

FRAH : Look-up table address register high 8 Place								
Bit	7	6	5	4	3	2	1	0
Name	FRA <15: 8>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	x	x	x	x	x	x	x	x

" x ":unknown

Bit 7 ~ 0 FRA <15: 8> : High Address look-up table 8 Place

ROMDL : Low lookup data register 8 Place								
Bit	7	6	5	4	3	2	1	0
Name	ROMD <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	x	x	x	x	x	x	x	x

" x ":unknown

Bit 7 ~ 0 ROMD <7: 0> : Low data look-up table 8 Place

ROMDH : High lookup data register 8 Place								
Bit	7	6	5	4	3	2	1	0
Name	ROMD <15: 8>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	x	x	x	x	x	x	x	x

" x ":unknown

Bit 7 ~ 0 ROMD <15: 8> : High data look-up table 8 Place

IAPC : IAP Control register								
Bit	7	6	5	4	3	2	1	0
Name	IAPEN	-	-	-	-	-	IAPGO	-
R / W	R / W	-	-	-	-	-	R / W	-
POR	0	0	0	0	0	0	0	0 "x" :unknown

Bit 7 **IAPEN : IAP Enable**

0 :shut down

1 : Enable (in only VPP And when the input high voltage)

Bit 6 ~ 2 Reserved for future use

Bit 1 **IAPGO : IAP Start bit programming**

0 : Programming operation does not start, or the operation has been completed

1 : Start the programming operation (set by software 1 Start-up operation, the operation is completed automatically cleared by hardware) (in only VPP And when the input high voltage)

Bit 0 Reserved for future use

3.4 Data Memory

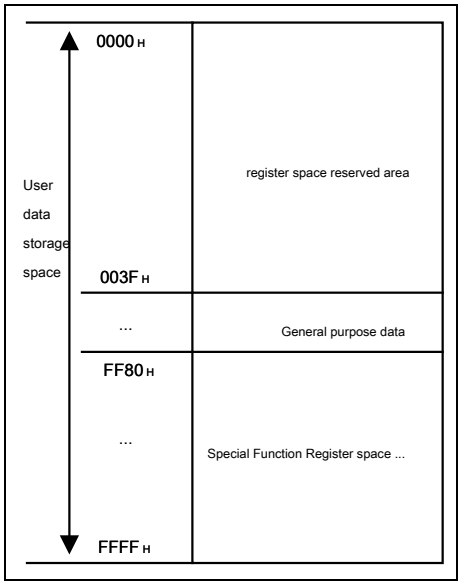
3. 4.1 Outline

- The data memory 2 Parts
  - Universal Data Memory GPR
  - Special Function Register SFR
- Universal Data Memory GPR
  - Altogether 1 Bank groups

  –64 Byte address range 00_H - $3F_H$
- Special Function Register SFR

  –128 Special registers
  - Address range $FF80_H$ - $FFFF_H$
- stand by 2 Addressing modes
  - Direct addressing
  - Indirect addressing

3. 4.2 Data address map



Map 3-3 A schematic view of a data address map

3. 4.3 Universal Data Memory

General data memory is used for temporary storage of data and control information, read and write operations may be performed under program control.

This chip is a general-purpose data memory space 64 Bytes With an address range 0000_H - $003F_H$. The contents of general data memory after a power-on reset is uncertain, the reset level is not at the other, to save the contents before reset.

3. 4.4 Special Function Register

Chip special function registers for controlling the setting of the operation of the peripherals. This chip supports 128 Special register, an address range $FF80_H$ - $FFFF_H$. Most registers are readable and writable, only a few part of the registers is not open. Related functions used are described in the respective register sections.

FF80H	IAD	FFA0H	INTG	FFC0H	T8P1PEX
FF81H	IAAL	FFA1H	LVDC	FFC1H	T8P2PEX
FF82H	IAAH	FFA2H	INTF1	FFC2H	-
FF83H	-	FFA3H	INTE1	FFC3H	-
FF84H	PSW	FFA4H	OSCCAL	FFC4H	-
FF85H	AREG	FFA5H	WDTCAL	FFC5H	-
FF86H	IAPC	FFA6H		FFC6H	ADCCL
FF87H	FRAL	FFA7H	PWRC	FFC7H	ADCCH
FF88H	FRAH	FFA8H	OSCC	FFC8H	ADCRL
FF89H	ROMDL	FFA9H	WKDC	FFC9H	ADCRH
FF8AH	ROMDH	FFAAH	OSCP	FFCAH	ADCTR
FF8BH	PCRL	FFABH	WDTC	FFCBH	-
FF8CH	PCRH	FFACH	PWEN	FFCCH	-
FF8DH	-	FFADH	-	FFCDH	-
FF8EH	PA	FFAEH	-	FFCEH	-
FF8FH		FFAFH	-	FFCFH	CALPROT
FF90H		FFB0H	WDTP	FFD0H	-
FF91H		FFB1H	-	FFD1H	-
FF92H	-	FFB2H	T8P1	FFD2H	-
FF93H	-	FFB3H	T8P1C	FFD3H	-
FF94H	N_PAD	FFB4H	T8P1P	FFD4H	-
FF95H	N_PBD	FFB5H	T8P1PMC	FFD5H	-
FF96H	N_PAU	FFB6H		.....	.....
FF97H	N_PBU	FFB7H	T8P1OC		
FF98H	-	FFB8H	T8P2	FFF8H	-
FF99H	-	FFB9H	T8P2C	FFF9H	-
FF9AH	-	FFBAH	T8P2P	FFFAH	-
FF9BH	PINTS	FFBBH	T8P2R	FFFBH	-
FF9CH	ANS	FFBCH	T8P2PMC	FFFCH	-
FF9DH	INTF0	FFBDH	T8P2OC	FFFDH	-
FF9EH	INTE0	FFBEH	T8P1PDT	FFFEH	-
FF9FH	INTC0	FFBFH	T8P2PDT	FFFFH	-

Note: "-" Reserved space, unused

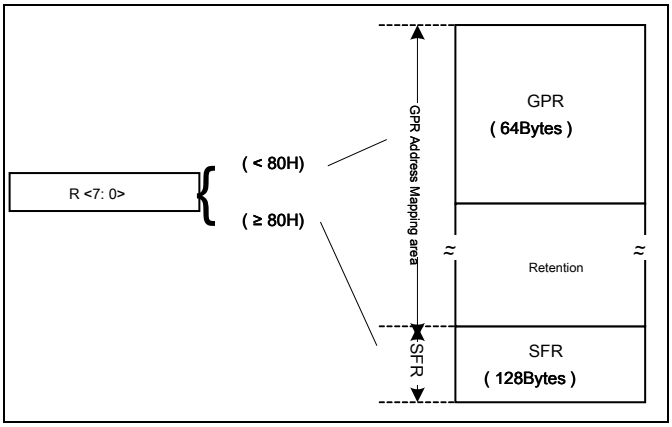
Map 3-4 Special Function Register space

3. 4.5 Addressing

SRAM Data memory addressing modes support direct addressing and indirect addressing.

3. 4. 5.1 Direct addressing

In direct addressing, the instruction 8 Bit address information GPR with SFR Addressing. When the instruction 8 Bit address information R <7: 0> Less than 80H When direct addressing GPR Mapping area. when R <7: 0> greater than or equal to 80H When direct addressing SFR Mapping area.



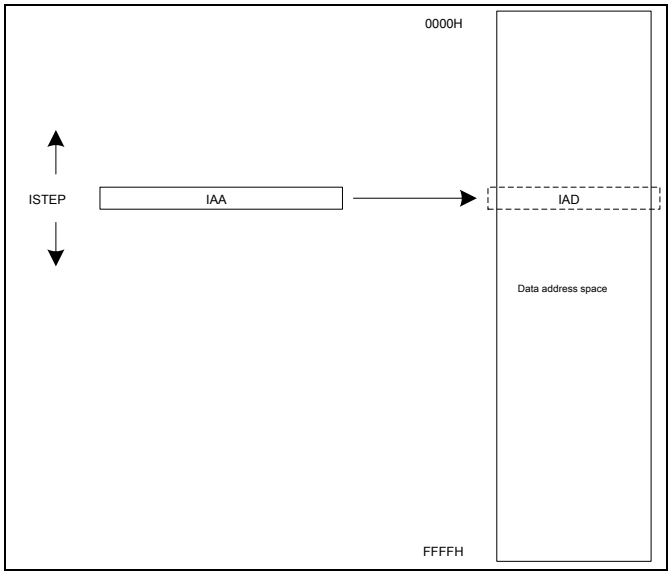
Map 3-5 Direct addressing schematic general

3. 4. 5.2 Indirect addressing

Indirect addressing is by 16 Indirect Address Register Bit IAA (by 2 More 8 Bit register IAAH with IAAL Composition) and 8 Bit virtual data register IAD Access the data address space of the memory cell, the address space 0000H ~ FFFFH . First access destination address stored in address register indirect IAA , Through the instruction IAD Read / write operations, the actual read / write operation is subject IAA Pointed object unit address data addressing space.

due to IAD Registers itself is mapped into the data address space FF80H Address, so when IAA Address stored value FF80H , The read / write IAD It corresponds to a virtual register indirect addressing IAD Itself, this time a read operation will always read as 00H , The write operation is a no-operation (likely to affect the status bits).

ISTEP Command used to 16 Indirect Register Bit Addressing IAAH / IAAL Offset operation. When the instruction is executed, the first instruction word 8 Bit signed immediate sign extension is 16 Digits, then IAA The result of this value plus the number of stored back IAA register. ISTEP Offset range can be achieved is - 128 to 127 . Although only 8 Bit immediate, but the instruction of the whole IAA (IAAL with IAAH) get on 16 Bit computing. The result of the calculation remains stored in IAAL with IAAH in.



Map 3-6 Indirect schematic

Application Example: The use of indirect addressing (020H ~ 02FH) The register is cleared.

```
..... CLR
      IAAH
      MOVI 0X20          ; Pointer initialization
      MOVA IAAL          ; IAA direction RAM
NEXT1:
      CLR   IAD          ; Clear IAD register
      ISTEP 0X01         ;pointer IAA Add content 1
      JBS   IAAL, 4      ;
      GOTO NEXT1         ; Is not complete, the next cell cycle to clear
CONTINUE:                ; It has been completed, continue following program is executed
      .....
```

3. 4.6 Special Function Register

IAD : Data register indirect addressing

Bit	7	6	5	4	3	2	1	0
Name	IAD <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 **IAD <7: 0> : Indirect Data**

IAAL : Low index register indirect addressing 8 Place

Bit	7	6	5	4	3	2	1	0
Name	IAA <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 **IAA <7: 0> : Indirect low index 8 Place**

IAAH : High index register indirect addressing 8 Place

Bit	7	6	5	4	3	2	1	0
Name	IAA <15: 8>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 **IAA <15: 8> : Indirect High Index 8 Place**

The first 4 chapter MCU - input / output port

4.1 Outline

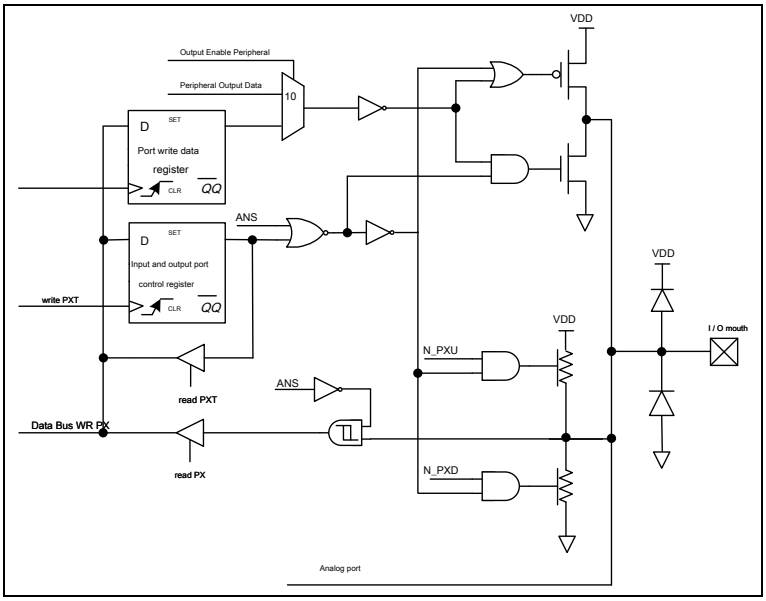
Input / output port MCU The most basic part MCU Supports up 13 Available in I / O Port and 1 Input ports. An input port PA3 Yes TTL Inputs, all other I / O Ports are TTL / SMT Input and CMOS

Output driver. among them, 4 More I / O Port and RF Even within a I / O Internal port vacant, is not available.

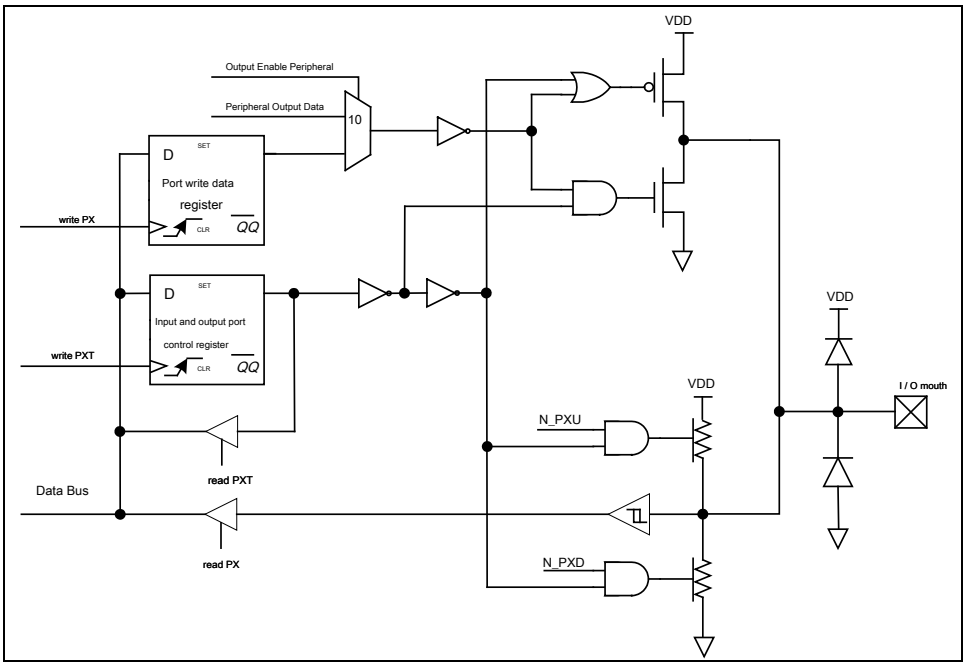
- PA Input / output ports functional components
  - 7 Bit bidirectional input / output and 1 Bit input port
  - TTL / SMT Input and CMOS Output Driver
  - Port I / O control register (PAT)
  - Weak pull port control register (N_PAU)
  - Port weak pull-down control register (N_PAD)
  - PA0 ~ PA7 Support for external interrupt function keys
  - PA0 ~ PA2 , PA7 I / O Digital to analog port selection register (ANS)
- PB Input / output ports functional components
  - 6 Bit bidirectional input / output port
  - TTL / SMT Input and CMOS Output Driver
  - Port I / O control register (PBT)
  - Weak pull port control register (N_PBU)
  - Port weak pull-down control register (N_PBD)
  - PB0 ~ PB5 Support for external port interrupt function
  - PB0 ~ PB1 I / O Digital to analog port selection register (ANS)

Note 1 : When the port is set to output port when the external oscillator clock, internal weak / pull-down is automatically disabled.

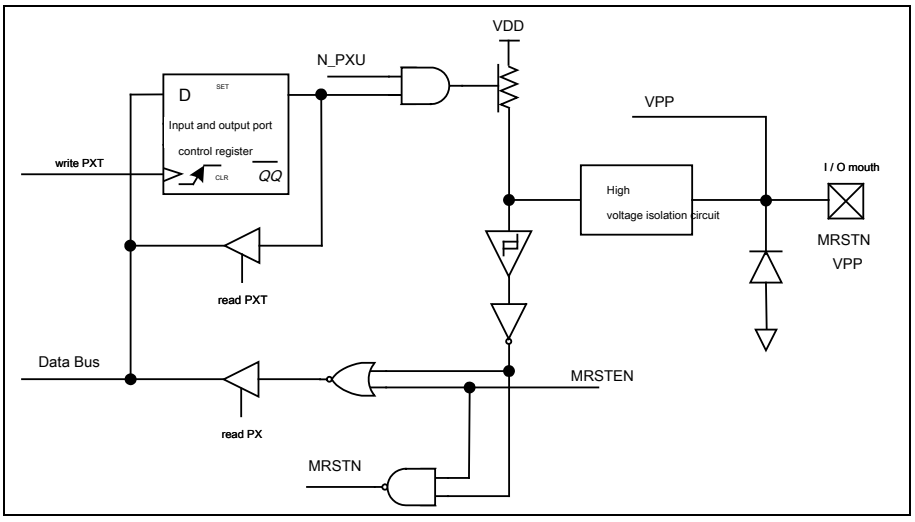
4.2 Structure diagram



Map 4-1 Input / output port configuration diagram - PA0 ~ PA2, PA7, PB0 ~ PB1



Map 4-2 Input / output port configuration diagram - PA4 ~ PA6, PB2 ~ PB5



Map 4-3 FIG input port structure - PA3

Note 1 : PA3 Corresponding port PAT Control bits are always 1 , which is PA3 Only for input. Note 2 :except ISP / IAP Operation outside, PA3 / MRSTN / VPP Pin voltage is higher than the chip supply voltage can not.

4. 3 I / O Port feature set

4. 3. 1 I / O Port Input / Output Control

All chips I / O Capacity having an input port / output port control register PxT An input or output port selected for the respective function. when I / O When the port is set to the digital output, I / O Output port Px Register contents, i.e., the corresponding I / O

Level of the port state, reading Px Register operation actually read the corresponding I / O Port state level. when I / O When set to the digital input port state, reading Px Register operation actually read the corresponding I / O Port state level.

4. 3. 2 I / O Weak pull-up on the port, the weak pull-down

Application of many products requires port pullup or pulldown resistor, so that the port is fixed at a stable level state against external interference, and other effects. This chip only PA3 The default pull-up enable port, all other ports are provided on a separate weak, pull-down function, it can be independently configured by software weak.

Pin	0	1	2	3	4	5	6	7
PA stand by	stand by	stand by	Support	Support	Support	support		
PB stand by	stand by	Support	Support	Support	stand by		-	-

table 4-1 I / O Port weak pull

Pin	0	1	2	3	4	5	6	7
PA stand by	stand by	stand by		-	support	support		
PB stand by	stand by	Support	Support	Support		-	-	-

table 4-2 I / O Weak Pull-Down

4. 3. 3 I / O Port Large current control function

register N_PBD <5> (PLCS) Can control port PA (PA7-4 , PA2-0), PB (PB5-0) Current drive capability.

4. 3. 4 I / O Port analog / digital type selection function

When the digital signal and the analog signal common pin, prior to use of the corresponding port function digital or analog signals, shall be provided with the correct type of a port, it may not achieve the desired results. This chip PA0 ~ PA2, PA7, PB0 ~ PB1 Ports having separate analog / digital signal selection function, by the ANS Register selection control. When the port is configured as an analog port, a respective read Px Always read register "0" .

4. 3. 5 I / O Port multiplexing function

In order to optimize the rational use of resources, most of this chip I / O Port has alternate functions. When the port for multiplexing function, the pin level determined by the multiplexing function.

4.4 Port Interrupt

4.4.1 Key interrupt (KINT)

This chip supports external port 1 Set of external key interrupt. Key interrupt support up 8 Input keys KIN <7: 0> , 8 Shared keys a key interrupt enable bit KIE (INTE0 <0>) And Key interrupt flag KIF (INTF0 <0>), Each input can be masked by respective key bits KMSKx (INTC0 <7: 0>) Shielding, any one of the buttons will affect interrupt interrupt flag KIF . (Note, KIN4 with KIN6 unavailable.)

when KINn Multiplexing port is configured as a digital input port, and 1 Any change in the level of the input port of a signal generating group, the key interrupt is generated KINT . When using an external key interrupt shall configure the control register, and to enable the external interrupt key internal port pull-up resistor. External button level comparison, the comparison is the last key input port of the input value at the level of the latches. Before clearing key interrupt flag must first read the corresponding multiplexing port / write operation, or the key interrupt flag can not be cleared. In the key interrupt enable (KMSKn = 1 , KIE = 1) Before the first port register read or write operation, clear the interrupt flag, so as to avoid an interrupt is generated. This interrupt can wake up from sleep state.

Pin name	Port input Key shielded interrupt enable interrupt flag			
PA0	KIN0	KMSK0	KIE	KIF
PA1	KIN1	KMSK1		
PA2	KIN2	KMSK2		
PA3	KIN3	KMSK3		
PA4	KIN4	KMSK4		
PA5	KIN5	KMSK5		
PA6	KIN6	KMSK6		
PA7	KIN7	KMSK7		

table 4-3 Key interrupt

(Note, KIN4 with KIN6 unavailable.)

4. 4.2 External port interrupt (PINT)

This chip supports external port 4 External port interrupt, external interrupt sources are external interrupt selection bit PINT3S ~ PINT0S (PINTS <7: 0>)select. Interrupted by the corresponding external port PIE3 ~ PIE0 (INTE1 <3: 0>) Enabled by PEG3 ~ PEG0 (INTC1 <3: 0>) Selects the rising edge or falling edge. when PINTn Multiplexing port is configured as a digital input port, the input signal changes and the trigger condition is met, it will produce PINTn External port interrupt, the interrupt will cause a corresponding interrupt flags PIFn (INTF1 <3: 0>). This interrupt can wake up from sleep state.

Pin name Interrupt Source Selection Enter the name of the port interrupt edge selection Interrupt Enable interrupt flag						
PA0 PA2 PB0 PB4	PINT0S <1: 0>	PINT0	PEG0	PINT0	PIE0	PIF0
PA1 PA3 PB1 PB5	PINT1S <1: 0>	PINT1	PEG1	PINT1	PIE1	PIF1
PA6 PA4 PB2	PINT2S <1: 0>	PINT2	PEG2	PINT2	PIE2	PIF2
PA7 PA5 PB3	PINT3S <1: 0>	PINT3	PEG3	PINT3	PIE3	PIF3

table 4-4 External interrupt port

4. 5 I / O Port Handling Precautions

When performing operations (except bit manipulation instructions) to the port register is the target, the actual implementation of the chip read - modify - write process, i.e., all the read first set I / O Level ports, modified, and written back to the register. Bit manipulation instructions I / O The modification affects only the selected bit, the same group will not affect other I / O port. It is recommended that a single user I / O Changes using bit manipulation instructions. In addition to the user I / O Port multiplexing function is enabled and when closed, should take full account of the current I / O Output port of register values, and determines whether these need to I / O Port initialization assignment.

4.6 Special Function Register

Input / output port set control register includes a series, PX Register for displaying PX Port level state, PXT Register sets PX Input and output port status, N_PXU / N_PXD For setting PX Weak pull port / Weak pull-down resistor is connected condition. ANS For setting PX Data type of the port.

PA : PA Level of the port status register								
Bit	7	6	5	4	3	2	1	0
Name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	x	x	x	x	x	x	x	x

" x ":unknown

Bit 7 ~ 0 PA <7: 0> : PA Port state level

0 : Low

1 : High

PAT : PA Input and output port control register								
Bit	7	6	5	4	3	2	1	0
Name	PAT7	PAT6	PAT5	PAT4	PAT3	PAT2	PAT1	PAT0
R / W	R / W	R / W	R / W	R / W	R	R / W	R / W	R / W
POR	1	1	1	1	1	1	1	1

Bit 7 ~ 6 PAT <7: 6> : PA <7: 6> State selection bit input and output ports

0 : Output state

1 : Input status

Bit 5 ~ 4 PAT <5: 4> : PA <5: 4> State selection bit input and output ports (external oscillator is multiplexed port, analog ports, this hardwired to two 1)

0 : Output state

1 : Input status

Bit 3 PAT3 : Hardwired to 1 The port can only be used as an input

Bit 2 ~ 0 PAT <2: 0> : PA <2: 0> State selection bit input and output ports

0 : Output state

1 : Input status

PB : PB Level of the port status register								
Bit	7	6	5	4	3	2	1	0
Name	-	-	PB5	PB4	PB3	PB2	PB1	PB0
R / W	-	-	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	x	x	x	x	x	x

" x ":unknown

Bit 7 ~ 6 Reserved for future use

Bit 5 ~ 0 PB <5: 0> : PB Port state level

0 : Low

1 : High

PBT : PB Input and output port control register								
Bit	7	6	5	4	3	2	1	0
Name	-	-	PBT5	PBT4	PBT3	PBT2	PBT1	PBT0
R / W	-	-	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	1	1	1	1	1	1

Bit 7 ~ 6 Reserved for future use

Bit 5 ~ 0 **PBT <5: 0> : PB State selection bit input and output ports**

0 : Output state

1 : Input status

N_PAU : PA Weak pull-port control register								
Bit	7	6	5	4	3	2	1	0
Name	N_PAU7	N_PAU6	N_PAU5	N_PAU4	N_PAU3	N_PAU2	N_PAU1	N_PAU0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	1	1	1	1	0	1	1	1

Bit 7 ~ 0 **N_PAU <7: 0> : PA Up control bit of a weak internal port**

0 :Enable

1 : Prohibition

N_PBU : PB Weak pull-port control register								
Bit	7	6	5	4	3	2	1	0
Name	-	-	N_PBU5	N_PBU4	N_PBU3	N_PBU2	N_PBU1	N_PBU0
R / W	-	-	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	1	1	1	1	1	1

Bit 7 ~ 6 Reserved for future use

Bit 5 ~ 0 **N_PBU <5: 0> : PB Up control bit of a weak internal port**

0 :Enable

1 : Prohibition

N_PAD : PA Port weak pull-down control register								
Bit	7	6	5	4	3	2	1	0
Name	N_PAD7	N_PAD6	N_PAD5	N_PAD4	-	N_PAD2	N_PAD1	N_PAD0
R / W	R / W	R / W	R / W	R / W	-	R / W	R / W	R / W
POR	1	1	1	1	1	1	1	1

Bit 7 ~ 4 **N_PAD <7: 4> : PA Weak pull-down control bit internal port**

0 :Enable

1 : Prohibition

Bit 3 Reserved for future use

Bit 2 ~ 0 **N_PAD <2: 0> : PA Weak pull-down control bit internal port**

0 :Enable

1 : Prohibition

N_PBD : PB Weak Pull-Down / large-current control register								
Bit	7	6	5	4	3	2	1	0
Name	-	-	PLCS	N_PBD4	N_PBD3	N_PBD2	N_PBD1	N_PBD0
R / W	-	-	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	1	1	1	1	1	1

Bit 7 ~ 6 Reserved for future use

Bit 5 **PLCS : High current drive ports PA (PA7-4 , PA2-0) / PB (PB5-0) Control bit**

0 : Prohibition

1 :Enable

Bit 4 ~ 0 **N_PBD <4: 0> : PB Weak pull-down control bit internal port**

0 :Enable

1 : Prohibition

Note: PB5 Weak Pull-Down hardwired to prohibit.

ANS : I / O Digital to analog port selection register								
Bit	7	6	5	4	3	2	1	0
Name	PWM20NS	PWM10NS	ANPA7	ANPB1	ANPB0	ANPA2	ANPA1	ANPA0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 **PWM20NS : PWM20 Output polarity Control**

0 :with PWM21 Inverting output

1 :with PWM21 Output in phase

Bit 6 **PWM10NS : PWM10 Output polarity Control**

0 :with PWM11 Inverting output

1 :with PWM11 Output in phase

Bit 5 **ANPA7 : PA7 Port select bit digital to analog (AIN5) 0 : Analog**

port

1 : Digital port

Bit 4 **ANPB1 : PB1 Port select bit digital to analog (AIN4) 0 : Analog**

port

1 : Digital port

Bit 3 **ANPB0 : PB0 Port select bit digital to analog (AIN3) 0 : Analog**

port

1 : Digital port

Bit 2 **ANPA2 : PA2 Port select bit digital to analog (AIN2) 0 : Analog**

port

1 : Digital port

Bit 1 **ANPA1 : PA1 Port select bit digital to analog (AIN1) 0 : Analog**

port

1 : Digital port

Bit 0 **ANPA0 : PA0 Port select bit digital to analog (AIN0) 0 : Analog**

port

1 : Digital port

The first 5 chapter MCU - special features and operating characteristics

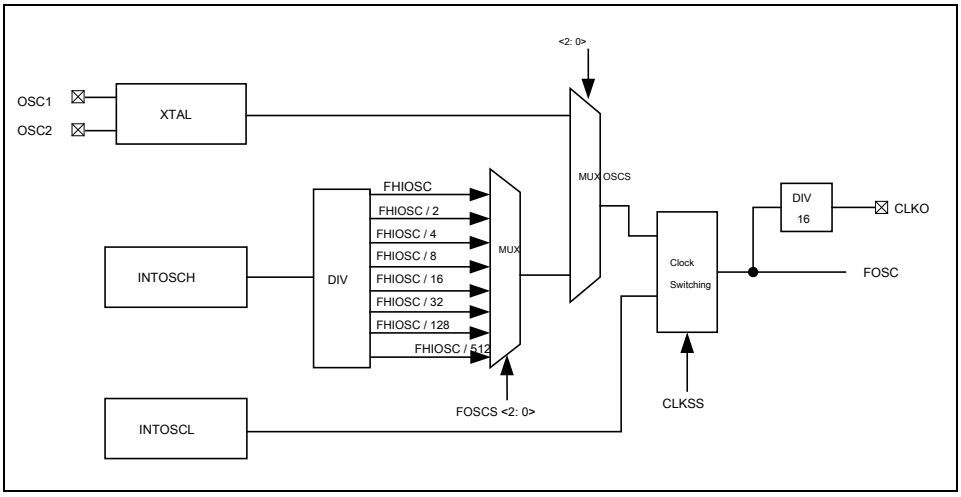
5.1 The system clock oscillator

5. 1.1 Outline

Chips needed to run the clock oscillator source is provided, different oscillator options offer the user a wide range of functions in various application requirements. Chip oscillator provided in this paragraph, there are three: external crystal / ceramic resonator XTAL , Internal high-speed RC Oscillator (16MHz) And internal low speed RC Oscillator (32KHz) . The flexibility to choose oscillator, making products in the speed and power consumption can be optimized. external LP And low-speed internal oscillator RC Oscillator In addition, as the system clock source, the watchdog timer can also provide the desired clock source.

- Oscillator mode
  - External oscillator (HS / XT / LP)
  - internal 16MHz RC Oscillator (configurable as INTOSC with INTOSCO)
  - internal 32KHz RC Oscillator
- internal 16MHz RC Oscillator
  - 8 Bit calibration register (OSCCAL)
  - Factory, at room temperature has been calibrated to an accuracy of ± 2%
  - Support for multiple clock divider
- internal 32KHz RC Oscillator
  - 8 Bit calibration register (WDTCAL)
- Switching system clock
  - HS / XT / INTOSCH 16MHz And internal low-speed oscillation clock INTOSCL 32KHz Clock Switching
  - External low speed LP Internal high-speed clock oscillation INTOSCH 16MHz Clock Switching
- Oscillation and pause
  - in IDLE0 Mode, the oscillator oscillating suspension
  - in IDLE1 Mode, the oscillator is oscillating system clock is suspended

5. 1.2 Clock Source



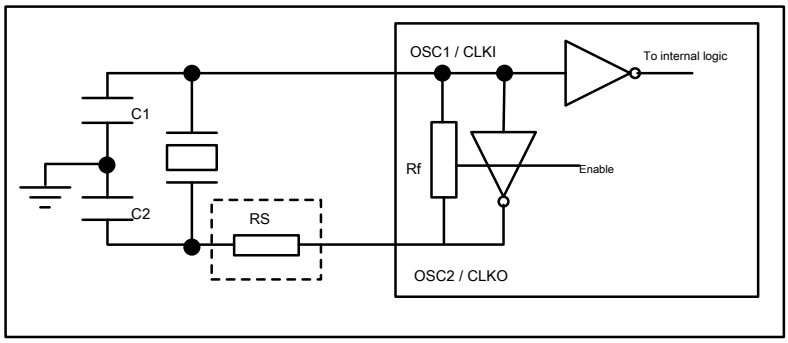
Map 5-1 The system clock internal structure of FIG.

5. 1. 2.1 External Clock

External clock includes a crystal / ceramic resonator mode (HS / XT / LP). For a crystal / ceramic oscillator, the crystal simply connected to the OSC1 with OSC2 Between the pin, it will produce the desired phase shift and oscillation feedback. To ensure more accurate oscillation frequency, to be connected to two small capacitor C1 with C2 To VSS , Crystal and specific values used / ceramic oscillator related to the range of the reference capacitor 15 ~ 33pF . The selected oscillator frequency can be divided into three modes:

HS mode, XT Mode and LP mode. When the chip configuration word OSCS <2: 0> = 000 When selecting LP Mode; when OSCS <2: 0> = 010 When selecting HS Mode; when the chip configuration word OSCS <2: 0> = 100 When selecting XT mode. Chip configuration word OSCS <2: 0> Customer choice through the programming interface.

- Crystal / resonator mode (HS , XT , LP mode)
  - HS / XT Crystal Start-up time is stable 512 System clock. LP Designed for low power oscillator crystal, vibrating stabilization time of about one second.



Map 5-2 Crystal / resonator mode (HS , XT , LP mode)

Note: RS It is optional.

Osc Type	Crystal frequency	C1	C2
LP	32KHz	33pF	33pF
XT	1MHz	15 ~ 33pF	15 ~ 33pF
	4MHz		
HS	8MHz		
	20MHz	15pF	15pF

table 5-1 Crystal Oscillator capacitance parameter reference table

Note: This data may be different from the size of fine tuning frequency from the crystal, the peripheral circuit.

5. 1. 2.2 Internal high-speed 16MHz RC Oscillator mode (INTOSCH)

Chip built 16MHz RC Clock oscillator, no external other external devices. When the configuration word OSCS <2: 0> = 000/110/111 And register OSCC middle CLKSS = 1 , The internal selection 16MHz RC Source as the system clock, this time PA2 with PA3 Pin Multiplexing is common I / O port. INTOSCH 16MHz The lowest frequency to be divided 32KHz , The factory built 16MHz RC Clock oscillator is calibrated at room temperature. On power chip, automatically loads calibration value, the calibration does not need to register the client OSCCAL Anything.

5. 1. 2. 3 Internal low 32kHz RC Oscillator mode (INTOSCL)

Chip built 32KHz RC Clock oscillator, no external other external devices, may be used WDT Count clock source, it may be configured as the primary system clock source. When the configuration word OSCS <2: 0> = 010/100/110/111 And register OSCC middle

CLKSS = 0 , The internal selection 32KHz RC Source as the system clock, this time PA2 with PA3 Pin Multiplexing is common I / O port. On power chip, automatically loads calibration value, the calibration does not need to register the client WDTCAL Anything.

5. 1.3 Switching system clock

High-frequency clock can provide higher performance of the system, low frequency clock to provide lower power consumption. Thus, according to user needs, flexibility to arrange high-frequency clock switching, the system can be optimized in terms of execution speed and power consumption. System software can register bit CLKSS (OSCC <7>), High selectivity, low-speed system clock. When the system is powered on, the register CLKSS The default value is 0 , The system operates at low speed clock mode.

The system supports four clock switch:

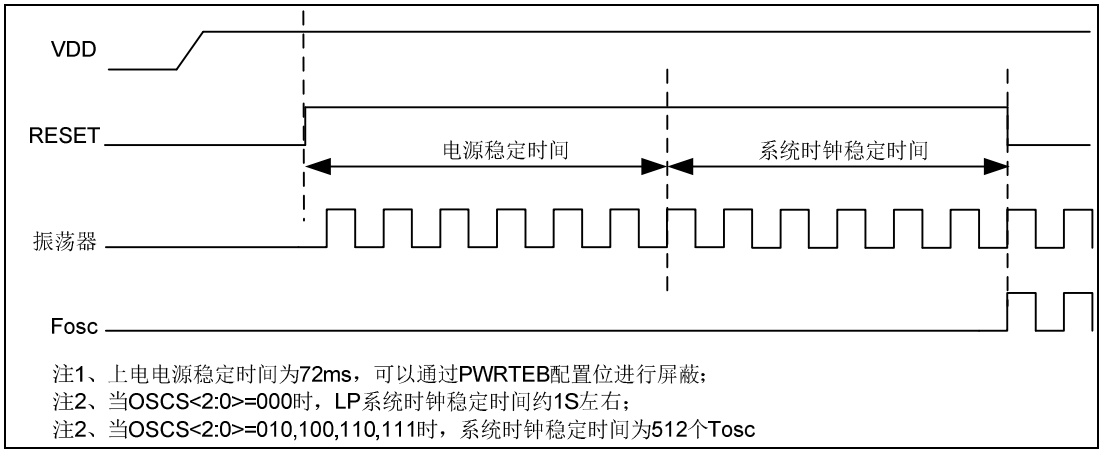
- Internal low INTOSCL 32KHz Internal high-speed clock is switched to INTOSCH / External high-speed HS / XT clock
  - Setting chip configuration word CFG_WD middle OSCS <2: 0> = 010/100/110/111 ;
  - Set up OSCC Register CLKSS = 1 ;
  - Detect OSCC Register HSOSCF Position, until it is detected HSOSCF = 1 ;
  - Wait a NOP instruction;
  - Detect PWEN Register SW_HS Position, until it is detected SW_HS = 1 ;
- Internal high-speed INTOSCH / External high-speed HS / XT The internal clock is switched to a low speed INTOSCL clock
  - Setting chip configuration word CFG_WD middle OSCS <2: 0> = 010/100/110/111 ;
  - Set up OSCC Register CLKSS = 0 ;
  - Detect OSCC Register WDTOSCF Position, until it is detected WDTOSCF = 1 ;
  - Wait a NOP instruction;
  - Detect PWEN Register SW_WDT Position, until it is detected SW_WDT = 1 ;
- External low speed LP Clock is switched to INTOSCH Clock Clock
  - Setting chip configuration word CFG_WD middle OSCS <2: 0> = 000 ;
  - Set up OSCC Register CLKSS = 1 ;
  - Detect OSCC Register HSOSCF Position, until it is detected HSOSCF = 1 ;
  - Wait a NOP instruction;
  - Detect PWEN Register SW_HS Position, until it is detected SW_HS = 1 ;
- Internal high-speed INTOSCH External clock is switched to a low speed LP clock
  - Setting chip configuration word CFG_WD middle OSCS <2: 0> = 000 ;
  - Set up OSCC Register CLKSS = 0 ;
  - Detect OSCC Register LPOSCF Position, until it is detected LPOSCF = 1 ;
  - Wait a NOP instruction;
  - Detect PWEN Register SW_LP Position, until it is detected SW_LP = 1 ;

The system clock source	OSCS <2: 0> Place	CLKSS Place
LP	000	0
HS	010	1
XT	100	1
INTOSCH	000	1
	110	1
	111	1
INTOSCL	010	0
	100	0

Clock Source System Clock Source OSCS<2:0> Bit	Bit CLKSS Place	Bit
	110	0
	111	0

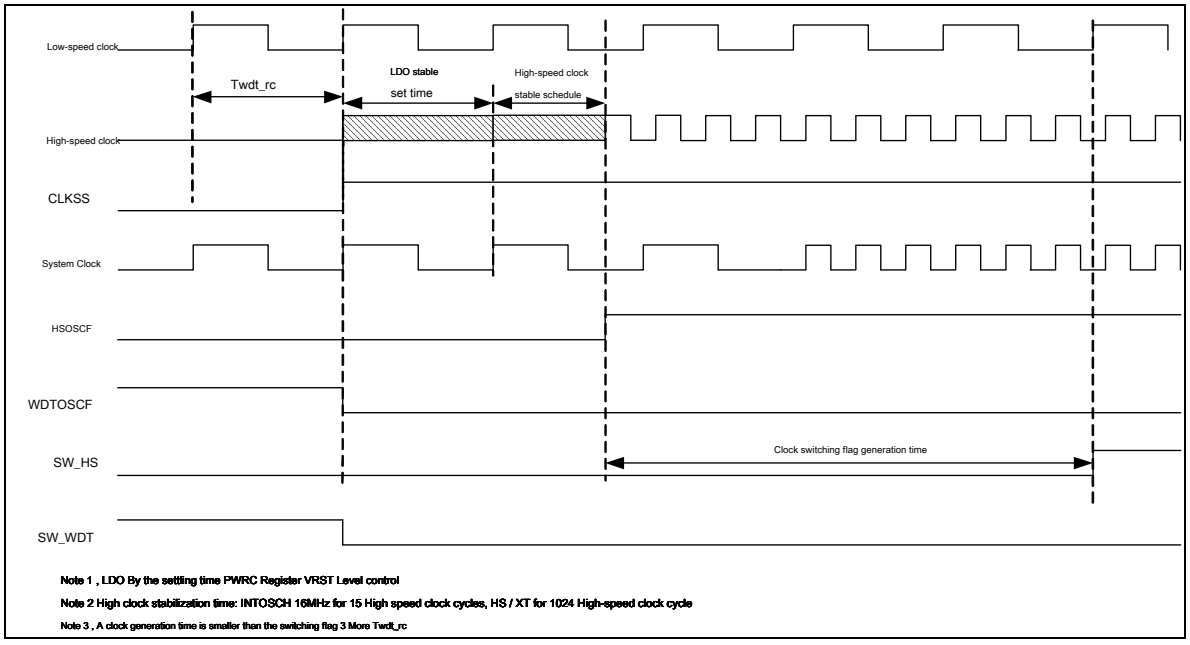
table 5-2 Oscillation mode select switch

5. 1. 3.1 System power-on timing on the system

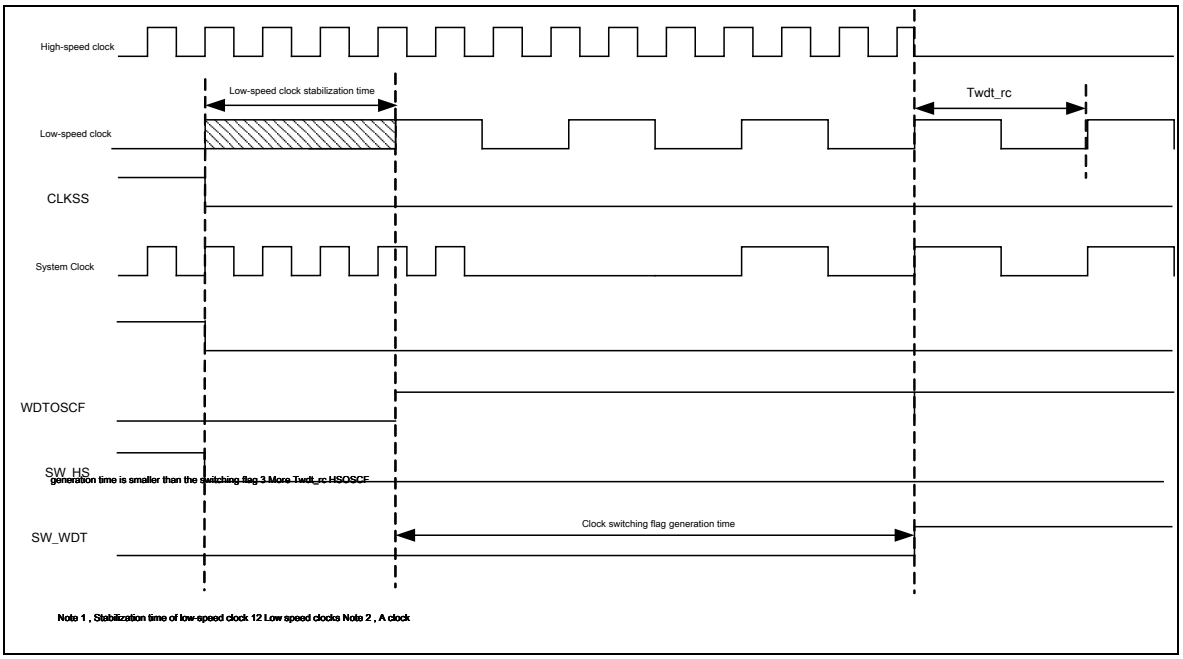


Map 5-3 System power timing chart

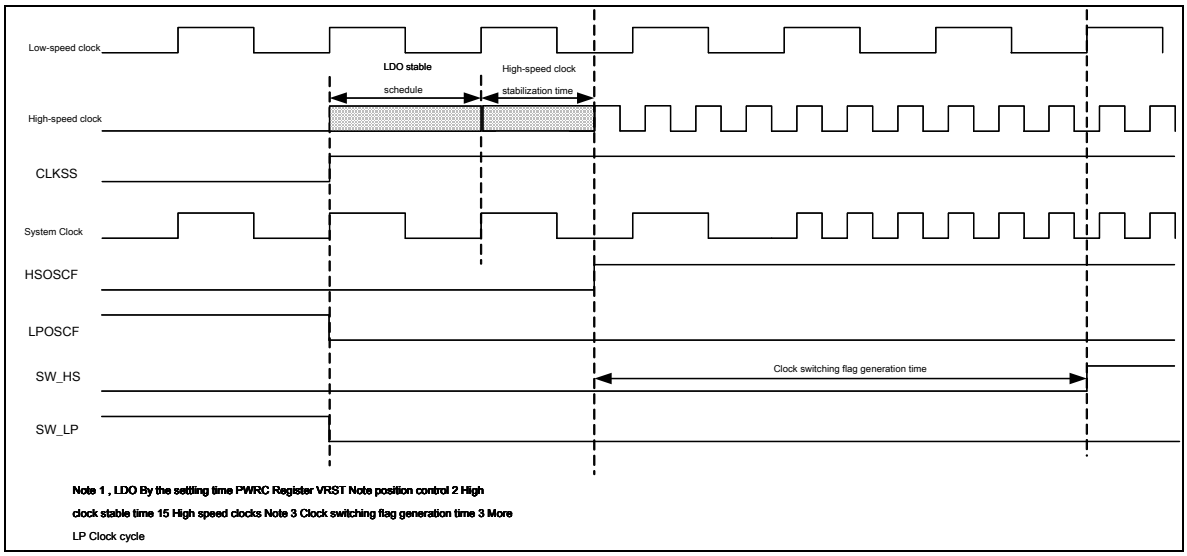
5. 1. 3.2 Switching system clock timing of the system clock



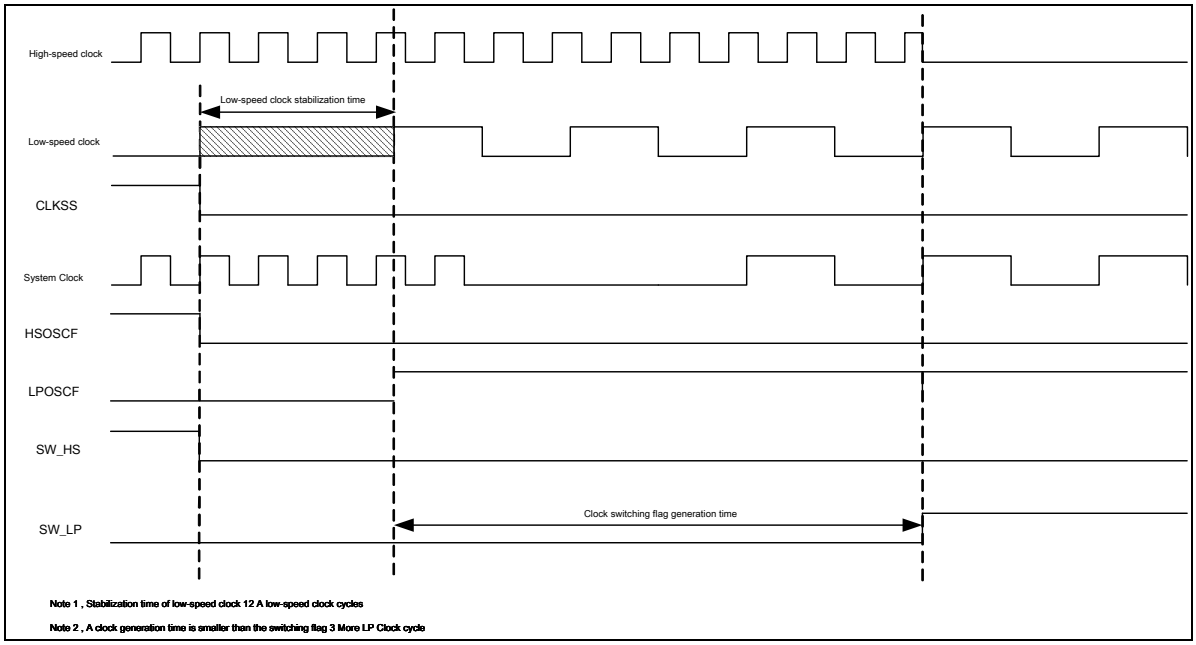
Map 5-4 INTOSCL Clock is switched to INTOSCH / HS / XT clock



Map 5-5 INTOSCH / HS / XT Clock is switched to INTOSCL clock



Map 5-6 Low Speed LP Clock is switched to INTOSCH clock



Map 5-7 INTOSCH Clock is switched to a low speed LP clock

5. 1.4 The system [illegible] dividing the system clock

When the system clock is derived from an internal clock frequency INTOSCH 16MHz When the system clock support 1 Largest division ratio is

1: 512 Divider, the lowest frequency to be divided 32KHz ,accessible OSSC Register FOSCS <2: 0> Bit

Selecting the division ratio.

5. 1.5 Special Fu[illegible] Registers

CALPROT : [illegible] register

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	CALPROT0
R / W	-	-	-	-	-	-	-	R / W
POR	0	0	0	0	0	0	0	1

Bit 7 ~ 1 Reserved for future use

Bit 0 CALPROT0 : Protection bit calibration value

1 : Calibration value is protected

0 : Removing the calibration value is protected

when CALPROT Write register 55 H When removing the protection bits, any other bit write protection is enabled.

Note: CALPROT Protected calibration value register OSCCAL , WDTCAL .

OSCCAL : Inte[illegible] register

Bit	7	6	5	4	3	2	1	0
Name	OSC CAL <7: 0>							
R / W	R / W	R / W	R / WR / W		R / W	R / W	R / W	R / W
POR	1	0	1	0	1	0	0	1

Bit 7 ~ 0 OSCCAL <7: 0> :internal 16MHz Clock frequency adjustment bits

Note: This register is CALPROT Register protection. OSCCAL Mainly to adjust the internal register 16MHz Accuracy of the clock. Under normal conditions, the factory calibrated to 16MHz . If there is no special needs, the user need not set this register, so as to cover the chip clock default calibration value.

OSCC : Clock control register

Bit	7	6	5	4	3	2	1	0
Name	CLKSS	FOSCS <2: 0>			-	WDTOSCF	HSOSCF	LPOSCF
R / W	R / W	R / W	R / W	R / W	-	R	R	R
POR	0	1	1	0	0	1	0	x

Bit 7 CLKSS : High speed and low speed clock when the bit clock switching OSCS

<2: 0> = 000 Time:

0 : External low LP 32KHZ Clock Source

1 : Internal high-speed INTOSCH 16MHz When the clock source OSCS

<2: 0> = 010/100/110/111 Time:

0 : Internal low INTOSCL 32KHZ Clock Source

1 : Internal high-speed INTOSCH 16MHz Or external high-speed HS / XT Clock Source

Bit 6 ~ 4 FOSCS <2: 0> : Internal system clock frequency select bit

000 : 32KHZ 001 : 125KHZ

010 : 500KHz 011 : 1MHz

100 : 2MHz 101 : 4MHz

110 : 8MHz 111 : 16MHz

Bit 3 Reserved for future use

Bit 2 WDTOSCF :internal 32KHz Stable Flag bit

0 : Not stable

1 :stable

Bit 1 HSOSCF : High-speed clock stable flag

0 : Not stable

1 :stable

Bit 0 LPOSCF :external LP Crystal stable flag

0 : Not stable

1 :stable

OSCP : Clock control register write protection

Bit	7	6	5	4	3	2	1	0
Name	OSCP <7: 0>							
R / W	R / W	R / W	R / WR / W		R / W	R / W	R / W	R / W
POR	1	1	1	1	1	1	1	1

Bit 7 ~ 0 OSCP <7: 0> : Clock controls write protection bits

OSCP for 55H , You can change FOSCS with CLKSS Bit. when FOSCS with CLKSS When it is written,

OSCP Automatic reset FFH .

OSCP It is not 55H When, for FOSCS with CLKSS The write operation will be ignored.

PWEN : Power Control Register								
Bit	7	6	5	4	3	2	1	0
Name	-	SW_WDT	SW_HS	SW_LP	-	-	RCEN	-
R / W	-	R	R	R	-	-	R / W	-
POR	0	1	0	0	0	0	1	1

Bit 7,3 ~ 2 Reserved for future use

Bit 6 SW_WDT : Switch to the low speed internal 32KHz Clock flag

0 : Switch unfinished

1 : Handover is completed

Bit 5 SW_HS : Switch to HS / XT / INTOSCH 16MHz High-speed clock flag

0 : Switch unfinished

1 : Handover is completed

Bit 4 SW_LP : Switch to the low speed external LP Crystal clock flag

0 : Switch unfinished

1 : Handover is completed

Bit 1 RCEN : WDT internal RC Clock Enable bit (software settings RCEN for 1 Enable) When CLKSS = 1 And in IDLE Mode:

0 :shut down WDT internal RC clock

1 :Enable WDT internal RC Clock (non IDLE Mode, and RCEN Nothing to do, RC Clock has been enabled) when CLKSS = 0 Time:

RCEN Fixed 1 , And write

Bit 0 Reserved for future use

Note 1 : It is recommended client software settings RCEN for 1 ,Enable WDT internal RC clock. Note 2 : If frequent high-low speed switching system clock, must be appropriately handover completion flag SW_LP , SW_HS with SW_WDT of

Judgment.

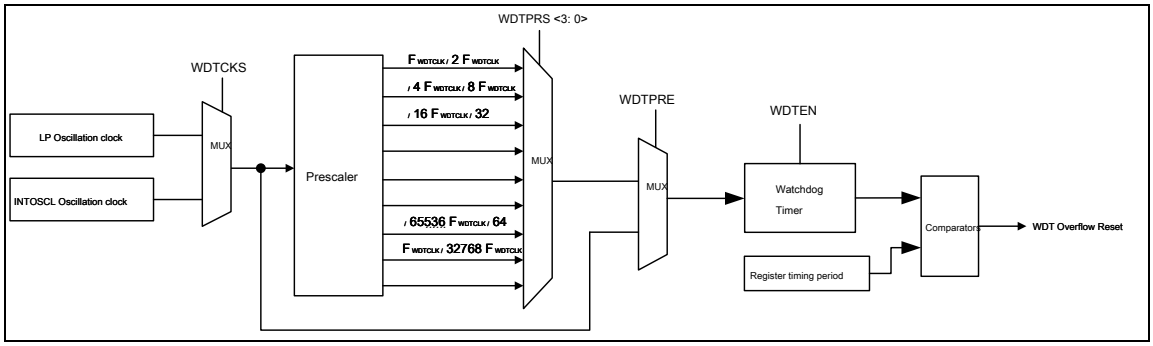
5.2 Watchdog Timer

5. 2.1 Outline

The watchdog timer is an integral part of the chip, its function is that in the event of a software failure, the resetting device resets the chip. If the system entered the wrong operation state, so that the chip can reset the watchdog within a reasonable time frame. When enabled, the watchdog, if the user program clears the watchdog timer failure, then within a predetermined time, the system will reset the watchdog.

- WDT Timer
  - 8 Place WDT Timing counter (no actual physical address, can not be read)
  - 8 Bit prescaler (no actual physical address, can not be read)
  - WDT Control Register (WDTC)
  - WDT Counting period match register (WDTP)
  - Wake-up function
  - Reset function
- internal WDT RC Oscillator
  - Internal timer clock source 32KHz RC Or an external clock LP Oscillation clock
  - 8 Place WDT Clock calibration register (WDTCAL)
  - Factory, at room temperature has been calibrated frequency ± 15% Within its high and low frequency offset WDT Influence The overflow cycle, as described in "Electrical Characteristics" section

5. 2.2 e



Map 5-8 Watchdog timer internal structure

5. 2. 3 WDT Timer

Chip offers 8 Place WDT Timing counter, through a chip configuration word WDTEN It enables the hardware watchdog WDT . When the chip configuration word WDTEN When enabled, WDT Enable timer count; when WDTEN When closed, WDT The timer counts prohibited. Customer choice through the programming interface.

When the configuration word OSCS <2: 0> Bit configuration to LP When mode, WDT Count clock source has two options: internal 32KHz RC And external clock LP Oscillation clock. in case WDTCKS = 0 Time, WDT The count clock is WDT RC Clock; when WDTCKS = 1 Time, WDT The count clock is LP Oscillation clock.

WDT Support a prescaler, by WDTC Register WDTPRS <3: 0> Bit Set WDT Prescaler clock source, and then the frequency divided clock signal as WDT Counting of the timer clock. when WDTPRE
(WDTC <4>) Cleared, Disabled Prescaler, WDT Clock 32KHz ;when WDTPRE (WDTC <4>) Set 1 Enable prescaler.

WDT It supports a set of read / write timing cycle register WDTP When the timing cycle of the watchdog count, timeout. in IDLE Mode, WDT The overflow will wake CPU ; In addition, WDT The overflow will reset the chip. To avoid unnecessary reset, may be used CWDT Timely clear instructions WDT counter.

In prescaler divide ratio is 1: 2 And the period register WDTP Set as FF$_H$ Time, WDT Internal use WDT Counting clock, the clock frequency of about room temperature 32KHz Counting the overflow time is about 16ms . When disabled prescaler,
WDT The overflow time is about the 8ms . Under other operating conditions, WDT The overflow of time in the section " 22.2 MCU FIG characteristic parameter "related chapters illustrated.

It is noteworthy that when WDT internal RC Clock Enable bit RCEN = 0 , The only IDLE Watchdog mode is prohibited, under other modes WDT of RC The clock has been turned on, not RCEN Impact.

Note 1 : WDT When the timer operation, RCEN (PWEN <1>) Must be set 1 .

5. 2.4 Special Function Register

WDT The function is controlled by WDTC Configuration registers and chip together to complete words. WDT Function is enabled by a chip configuration control word, and WDT Clock source selection, WDT Prescaler and enable control WDT Prescaler division ratio selection by WDTC Register settings. In addition, WDTP Register sets WDT Period count value,
WDTCAL Internal register 32KHz Clock calibration.

WDTCAL :internal 32KHz Clock calibration register								
Bit	7	6	5	4	3	2	1	0
Name	WDTCAL <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	1	0	0	0	0	1	0	0

Bit 7 ~ 0 WDTCAL <7: 0> :internal 32KHz Clock frequency adjustment bits

Note: This register is CALPROT Register protection. WDTCAL Mainly to adjust the internal register 32KHz Accuracy of the clock. In the former chip factory calibration values have been set up to prohibit the user program to rewrite the register, otherwise it will lead to a corresponding function module chip not working.

WDTC : WDT Control register								
Bit	7	6	5	4	3	2	1	0
Name	WDTCKS	-	-	WDTPRE	WDTP RS <3: 0>			
R / W	R / W	-	- R / W		R / W	R / W	R / W	R / W
POR	0	0	0	1	0	1	1	1

Bit 7 WDTCKS : WDT Count clock source selection
0 :internal WDT RC clock
1 :external LP Oscillation clock

Bit 6 ~ 5 Reserved for future use

Bit 4 WDTPRE : WDT Prescaler enable bit

0 : Prohibition

1 :Enable

Bit 3 ~ 0 **WDTPRS <3: 0> : WDT Prescaler division ratio selection bits**

0000 : 1: 20001 : 1: 40010 : 1:

80011 : 0100 1:16 : 0101 1:32 : 0110

1:64 : 1: 1,280,111 : 1: 256 (default)

1000 : 1: 5,121,001 : 1:

10,241,010 : 1:

20,481,011 : 1:

40,961,100 : 1:

81,921,101 : 1:

163841110 : 1:

327681111 : 1: 65536

WDTP : WDT Cycle Match Count register

Bit	7	6	5	4	3	2	1	0
Name	WDTP <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	1	1	1	1	1	1	1	1

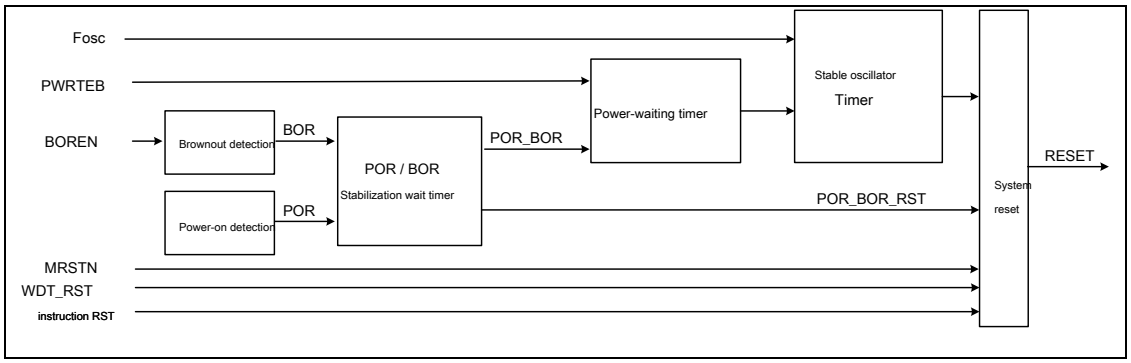
Bit 7 ~ 0 **WDTP <7: 0> : WDT Cycle count values**

5.3 Reset module

5. 3.1 Outline

Reset function is a fundamental part of all the chips, the chip supports five reset:

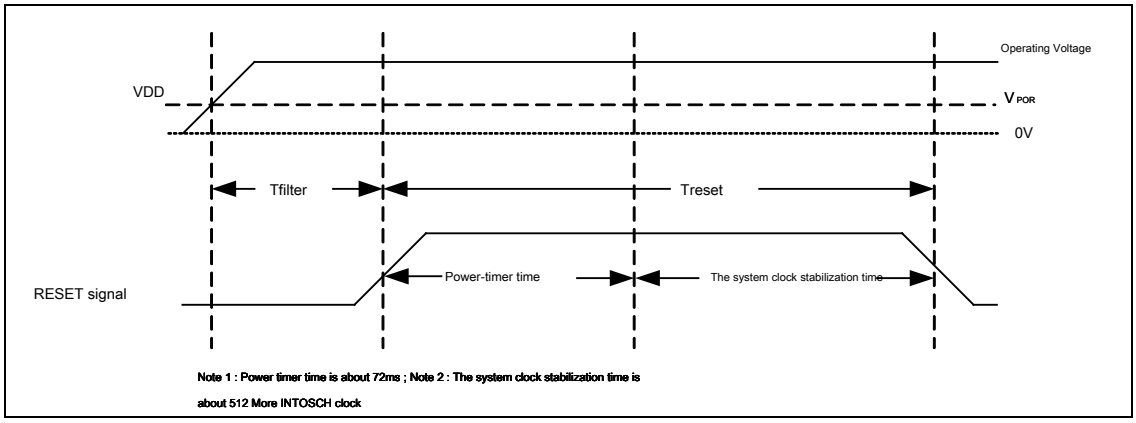
- Power-On Reset POR
- Under power-on reset BOR
- External ports MRSTN Reset, active low reset
- Watchdog Timer WDT Overflow Reset
- Software executing instructions RST Reset



Map 5-9 Schematic chip reset

5. 3.2 Power-On Reset

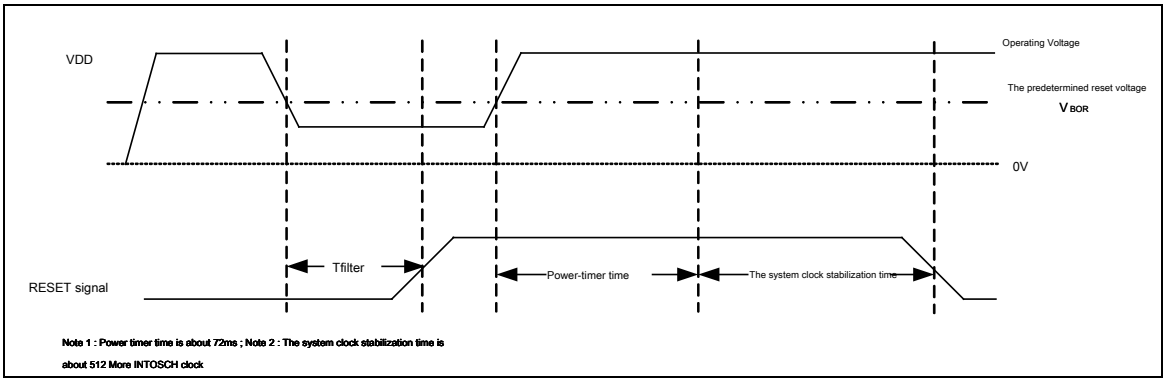
During power on the chip will produce POR Reset, and the reset signal will remain until the supply voltage rises to the voltage of the chip can operate properly. During power on the system as a rising curve, and it takes time to reach a normal level value. Power on reset sequence is as follows:



Map 5-10 Timing diagram of power-on reset

5. 3.3 Under power-on reset

Under power-on reset caused by external factors power dropping condition (for example: battery replacement), under the power-on reset may cause the system not working properly or state program execution errors.



Map 5-11 Timing diagram of the power-on reset

Note 1 : 72ms Waiting time can be stabilized by PWRTEB shield. Note 2 : When configured as HS / XT / INTOSCH 16MHz Mode, the

oscillation stabilization time 512 x Tosc ;

When configured as LP Mode, the oscillation stabilization time is about 1S about.

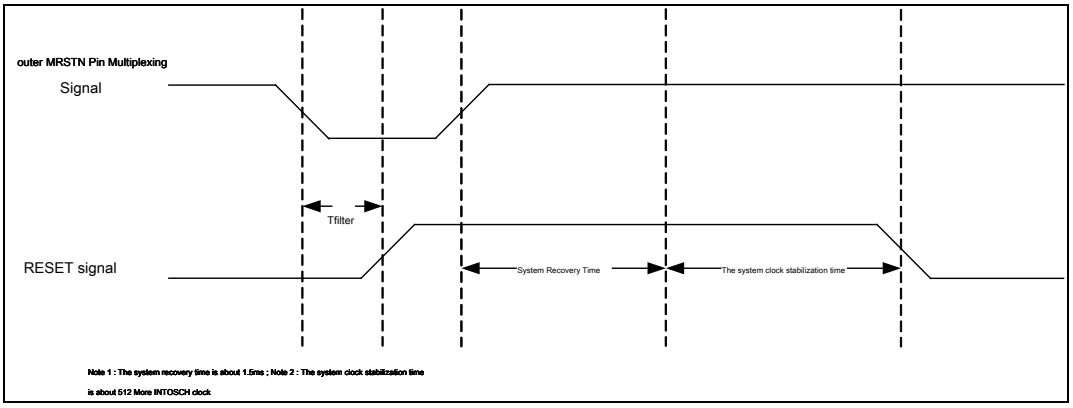
Chip can reset the lower voltage and the reset point may be configured Word BORVS <1: 0> Bit configuration.

BORVS <1: 0>	The reset voltage point configuration	The reset enable
11	Lower than 3.4V When the chip is reset	Enable
10	Lower than 2.7V When the chip is reset	Enable
01	Lower than 2.2V When the chip is reset	Enable
00	-	Ban

table 5-3 The reset voltage point configuration table

5. 3.4 external MRSTN Reset pin

Providing an external chip MRSTN Pin, when CFG_WD <5> (MRSTEN)for 1 When, for a system reset. When the reset pin input a low level signal, the system reset. When the reset pin is at high level, the normal operation of the system. Note that, after the completion of power on the system, the external reset input pin **must be high, otherwise the system will remain in the reset state. In addition, special attention is prohibited MRSTN Pin is connected directly to the VDD On; prohibited MRSTN Higher than the voltage on pin VDD Voltage.**

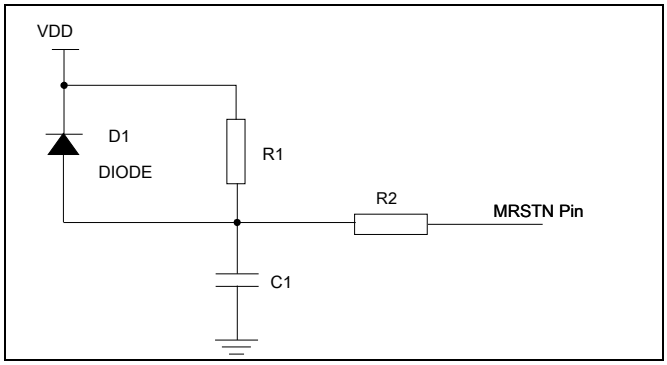


Map 5-12 external MRSTN Reset pin

external MRSTN There are a variety of pin reset circuit, the following describes two typical connection circuit.

1. RC Reset

RC External reset circuit MRSTN Reset circuit pin simplest one, of a case where less demanding ambient conditions, this connection may be employed.

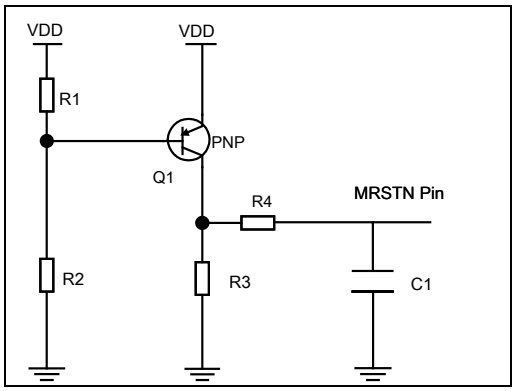


Map 5-13 MRSTN Reset circuit diagram of a reference 1

Note: Sampling RC Reset, wherein 47KΩ≤R1≤100KΩ ,capacitance C1 (0.1μF), R2 Current limiting resistor, 0.1KΩ≤R2≤1KΩ .

2. PNP Reset transistor

PNP Transistor power on reset circuit suitable for the case where a strong interference.

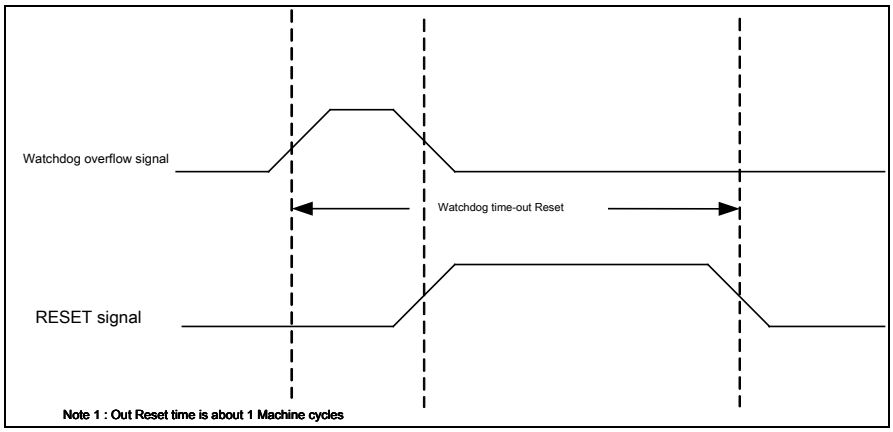


Map 5-14 MRSTN Reset circuit diagram of a reference 2

Note: The PNP Reset transistor, by R1 (2KΩ)with R2 (10KΩ) Partial pressure as a base input, an emitter connected VDD Collector all the way through R3 (20KΩ) Ground, another way by R4 (1KΩ)with C1 (0.1μF) Ground, C1 As the other end MRSTN Input.

5. 3.5 Watchdog timer overflow reset

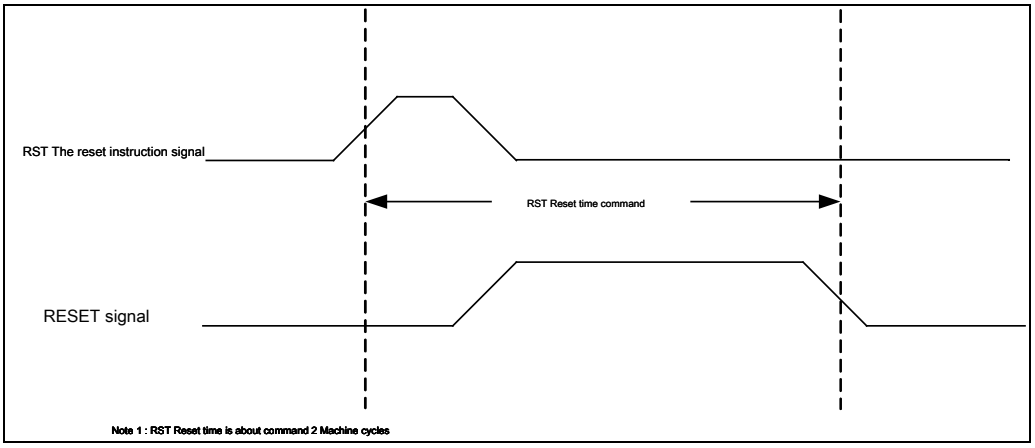
The watchdog reset is a system protection. Under normal conditions, the watchdog timer is cleared by the program. If the error, the system is in an unknown state, the program can not clear the watchdog, and therefore the watchdog timer overflow, then the system is reset. Watchdog overflow reset, reboot the system into the normal state.



Map 5-15 Watchdog Time-out Reset

5. 3. 6 RST Reset command

The entire chip by performing RST Reset command, reset, all status bits are affected.



Map 5-16 RST Reset command

5. 3.7 Special Function Register

PWRC : Power Control Register								
Bit	7	6	5	4	3	2	1	0
Name	LPM	VRST <1: 0>		N_RSTI	N_TO	N_PD	N_POR	N_BOR
R / WR / W		R / W	R / W	R / W	R	R	R / W	R / W
POR	0	1	0	1	1	1	0	x "x" :unknown

Bit 7 LPM : Sleep Mode Select Bits

0 : IDLE0 mode

1 : IDLE1 mode

Bit 6 ~ 5 VRST <1: 0> : LDO When the settling time of the control register CLKSS

= 1 Time:

00 : LDO Settling time 16 Internal 32KHz Clock cycle

01 : LDO Settling time 32 Internal 32KHz Clock cycle

10 : LDO Settling time 64 Internal 32KHz Clock cycle

11 : LDO Settling time 128 Internal 32KHz When the clock cycle CLKSS = 0 Time

:

11 : LDO Settling time 128 Internal 32KHz Other clock cycle: LDO Settling time 64 Internal 32KHz Clock cycle

Bit 4 N_RSTI : Flag reset instruction

0 : Reset instruction (must be set by software)

1 : Reset instruction is not executed

Bit 3 N_TO : WDT Overflow flag

0 : WDT It is cleared counter overflows

1 : Power-on reset or execution CWDT , IDLE Instruction set after 1

Bit 2 N_PD : Power Down Flag

0 :carried out IDLE After the instruction clears

1 : Power-on reset or execution CWDT Command post 1

Bit 1 N_POR : On Reset Status bit

0 : Power on reset occurs (after power-on reset, the software must be set)

1 : Supreme Power-on Reset occurred

Bit 0 N_BOR : Reset Status bit

0 : The power reset occurs (after the power-on reset, the software must be set)

1 : No next power-on reset occurs

Note: LDO To-chip power module, power module internal circuitry to the chip.

5.4 Low-power operation

5. 4. 1 MCU Low-power mode

This chip supports two low-power sleep mode: IDLE0 Mode or IDLE1 Mode, by setting PWRC Register Bit LPM (PWRC <7>) To select it.

- stand by IDLE0 mode
  - when LPM = 0 When executed IDLE Command, the device enters IDLE0 mode:
  - Clock source to stop vibration (32KHz RC Excluding clock source), the main system clock is suspended
  - Program pause, pause synchronization module, the module runs asynchronously, reduce device power consumption
  - Support low-power wake-up time can be equipped, at the same time need to consider LDO stable schedule
  - all I / O Enter the port will remain IDLE0 State before mode
  - If enabled WDT ,then WDT It will be cleared but keeps running
  - N_PD Bit is cleared, N_TO Bit is set 1
- stand by IDLE1 mode
  - when LPM = 1 When executed IDLE Command, the device enters IDLE1 mode:
  - Source clock keeps running, the main system clock is suspended
  - Program pause, pause synchronization module, the module runs asynchronously, reduce device power consumption
  - Support low-power wake-up time can be equipped with a minimum 1 Machine cycles
  - all I / O Enter the port will remain IDLE1 Former state
  - If enabled WDT ,then WDT It will be cleared but keeps running
  - N_PD Bit is cleared, N_TO Bit is set 1

5. 4.2 Low-power mode configuration

Two low-power mode IDLE0 with IDLE1 Select mode by PWRC Register LPM Position control. when LPM = 0 When executed IDLE Command, the device enters IDLE0 Mode; when LPM = 1 When executed IDLE Command, the device enters IDLE1 mode.

Low-power mode	LPM
IDLE0 mode	0
IDLE1 mode	1

table 5-4 Low power mode configuration table

To reduce power consumption, all I / O Pin should be kept VDD or VSS . In order to avoid floating input pin switching currents, should the external impedance inputs I / O Pulling the pin high or low, MRSTN Pin must be at a logic high.

5. 4.3 IDLE Wake-up configuration

When the system enters a low power mode, the program is paused, the following ways can wake up the system.

No.	Wake-up source	Interrupt Mask	Interrupt Enable	interrupt mode		Remark
1	MRSTN	-	-	-		External reset
2	WDT	-	-	-		WDT overflow
3	KINT0	KMSK0	KIE	default		External Key interrupt
	KINT1	KMSK1				
	KINT2	KMSK2				
	KINT3	KMSK3				
	KINT4	KMSK4				
	KINT5	KMSK5				
	KINT6	KMSK6				
	KINT7	KMSK7				
4	PINT0	-	PIE0	The default port		external interrupt 0
5	PINT1	-	PIE1	The default port		external interrupt 1
6	PINT2	-	PIE2	The default port		external interrupt 2
7	PINT3	-	PIE3	The default port		external interrupt 3

table 5-5 Wake-up table

Note 1 : Low-power wake-up has nothing to do with global interrupts are enabled, only the corresponding interrupt source enable bit is set "1" It can be. In the low power mode, the interrupt signal is generated when the peripheral, even if the global interrupt enable GIE for 0 Low-power mode will still wake up, wake up after just will not execute the interrupt routine. Note 2 : About using external key interrupt, when open interrupt enable and interrupt mask bits before it is enabled, the first port register read or write operation, and then clear the interrupt flag, so as to avoid an interrupt is generated. Note 3 : KINT6 unavailable.

5. 4.4 Wake timing diagram

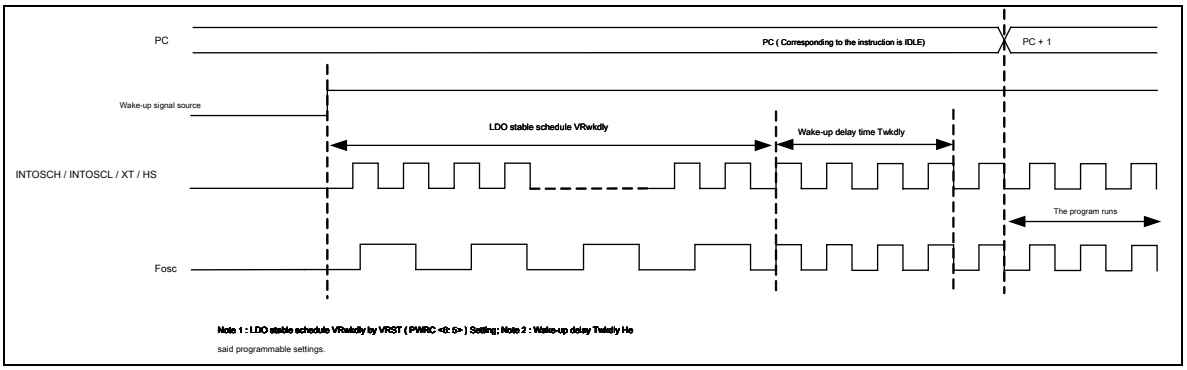
When the wake-up event, according to the chip configuration word OSCS <2: 0> Configuration performs the following operations:

- when OSCS <2: 0> Configured to HS / XT / INTOSCO / INTOSC Mode:
  - in IDLE0 mode(LPM = 0 Under), the chip will need to wait VRwkdly Time (by the VRST (PWRC <6: 5>) Set), this time called LDO Stabilization time, after a period of operation of the master clock chip Twkdly Time after execution IDLE The next instruction, Twkdly Called Wake-up delay, wake-up delay by WKDC Register set;
  - in IDLE1 mode(LPM = 1), The chip only wait Twkdly Time after execution IDLE The next instruction, no VRwkdly time.

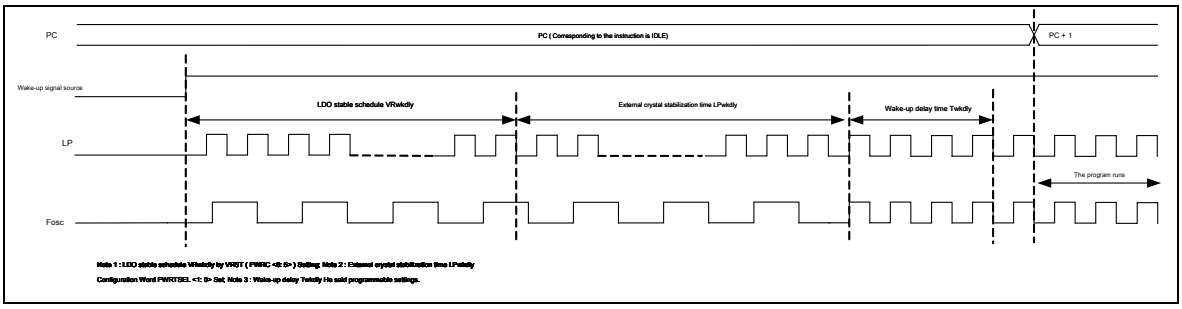
- when OSCS <2: 0> Configured to LP Mode:
  - in IDLE0 mode(LPM = 0 Under), the chip will need to wait VRwkdly Time (by the VRST (PWRC <6: 5>) Set), this time called LDO Settling time, and then wait for the chip LPwkdly Time, after a period of operation of the master clock chip Twkdly Time after execution IDLE The next instruction, Twkdly Called Wake-up delay, wake-up delay by WKDC Register set;
  - in IDLE1 mode(LPM = 1), The chip only wait Twkdly Time after execution IDLE The next instruction, no VRwkdly with LPwkdly time.

OSCS Configuration	Low-power mode	The formula
All modes	IDLE1 mode	(WKDC [7: 0] +1) × 2 Tosc
non- LP mode	IDLE0 mode	VRwkdly + (WKDC [7: 4] + 1) × 16 × 2 Tosc
LP mode		VRwkdly + LPwkdly + (WKDC [7: 4] + 1) × 16 × 2 Tosc

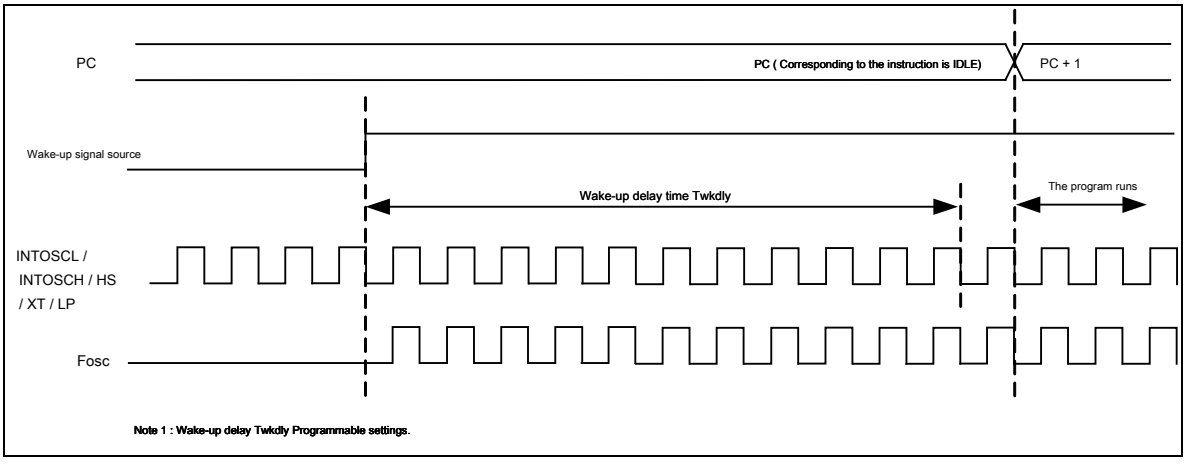
table 5-6 Wake-up schedule



Map 5-17 HS / XT / INTOSCO / INTOSC Mode, the system wake-up IDLE0 Timing diagram



Map 5-18 LP Mode, the system wake-up IDLE0 Timing diagram



Map 5-19 HS / XT / INTOSCO / INTOSC / LP Mode, the system wake-up IDLE1 Timing diagram

5. 4.5 Special Function Register

WKDC : Wake-up delay control register								
Bit	7	6	5	4	3	2	1	0
Name	WKDC <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	1	1	1	1	1	1	1	1

Bit 7 ~ 0 WKDC <7: 0> : Wake-up delay time setting position

00 H : The shortest delay

..... FF H : Longest

delay

The first 6 chapter MCU - Peripheral

6. The 18 Place PWM Base Timer (T8P1 / T8P2)

6. 1.1 Outline

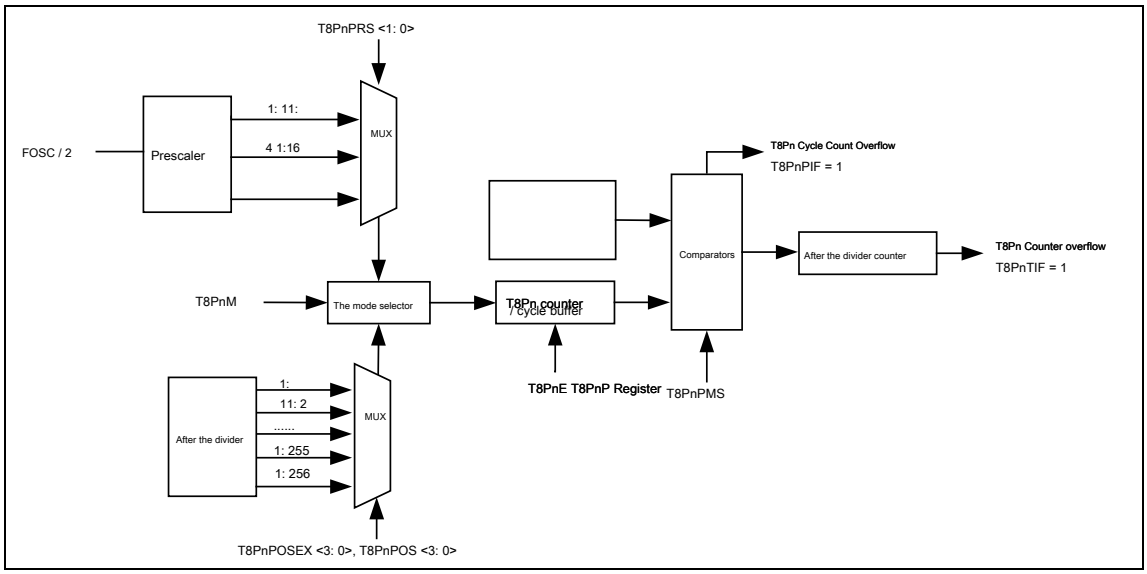
This chip contains 2 group PWM Base Timer (T8P1 / T8P2), Supports two modes, timer mode and PWM mode. Timing according to the timing timer mode time register established, the timer can selectively generate interrupt requests or perform other operations. PWM Mode is used PWM Output.

- T8Pn It supports two modes of operation (clock source for the system clock 2 Divider (Fosc / 2))
  - Timer Mode
  - PWM Mode, the maximum support 11 Place PWM The average output accuracy, support PWM With dead complementary outputs and dead-time software configurable
- T8Pn It supports the following functional components

–4 Bit prescaler and 8 After bit divider (no actual physical address, the software can not read and write)

- 8 Bit counter (T8Pn)
- 8 Bit precision registers (T8PnR)
- 8 Bit period register (T8PnP)
- 8 Bit period buffer (PRDBUF No actual physical address, the software can not read and write)
- 8 Bit precision buffer (RESBUF No actual physical address, the software can not read and write)
- 8 Place T8Pn PWM Dead time control register (T8PnPDT)
  - Control Register (T8PnC)
  - T8PnPEX After the division ratio extension register (T8P1PEX / T8P2PEX)
  - T8Pn Cycle Match Control Register (T8P1PMC / T8P2PMC)
  - T8Pn Output control register (T8P1OC)
- Interruption and suspension
  - Support match interrupt flag (T8PnTIF) And periodic interrupt (T8PnPIF)
  - Support interrupt handling
  - in IDLE Mode, T8Pn Suspend work

6. 1.2 e



Map 6-1 T8P1 / T8P2 e

6. 1.3 Operating mode

8 Place PWM There are two time-base timer mode: Timer mode and PWM Mode, T8PnM Mode selection register. Both modes support prescaler and divider. In both modes, T8Pn The system clock source clock counter are 2 Divider (Fosc / 2).

T8PnM	Operating mode
0	Timer Mode
1	PWM mode

table 6-1 T8Pn Working Mode Configuration Table

6.1.4 Prescaler and divider

Prescaler and divider can provide a longer time-out and break the cycle. T8Pn Block counter support configurable

4 Bit prescaler and configurable 8 Bits divider. Prescaler count value after divider can not read and write, modify

T8Pn A control register or counter is the prescaler and prescaler are cleared, without changing the division ratio setting. Prescaler

division ratio by T8PnC Register T8PnPRS <1: 0> Bit is set, the range of prescaler

1: 1 to 1:16 . After the division ratio divider by T8PnC Register T8PnPOS <3: 0> Bits and the frequency division ratio of the extension register T8PnPEX middle T8PnPOSEX <3: 0> Setting, after the frequency division ratio in the range 1: 1 to 1: 256 .

T8PnPRS <1: 0>	T8PnPOSEX <3: 0>, T8PnPOS <3: 0>	T8Pn Interrupted match
00	00000000	And the period counter register match 1 Secondary
00	00000001	And the period counter register match 2 Secondary
00	00000010	And the period counter register match 3 Secondary
00	00000011	And the period counter register match 4 Secondary

T8PnPRS <1: 0> T8PnPOSEX <3: 0>, T8PnPOS <3: 0>		T8Pn Interrupted match
00	.....	.....
00	11111110	And the period counter register match 255 Secondary
00	11111111	And the period counter register match 256 Secondary
Other values	-	-

table 6-2 T8P1 / T8P2 After the divider configuration table

6. 1.5 Timer Mode

when T8PnM = 0 And T8PnE = 1 Time, T8Pn Work in timer mode.

In timer mode, T8Pn The counter clock source for the system clock 2 Divider (Fosc / 2), Select the count clock prescaler for frequency-dividing the clock counter after counting the frequency-divided clock.

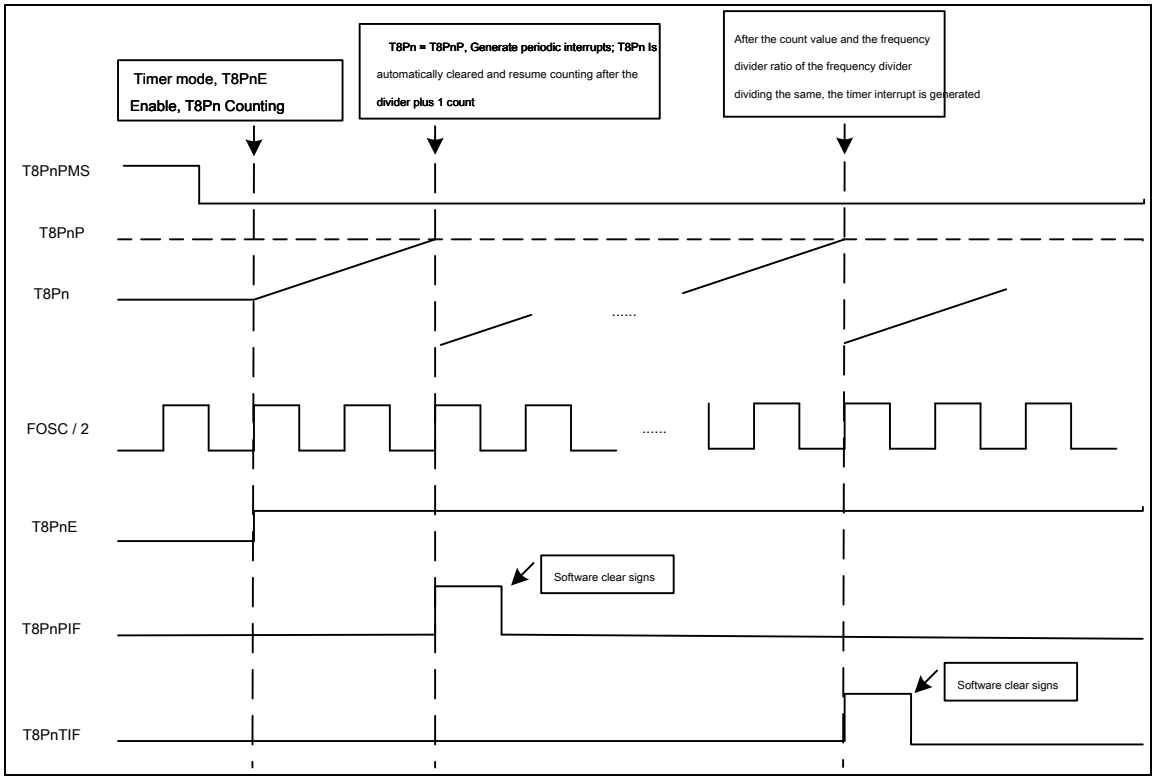
In timer mode, when T8PnPMS = 0 When not update cycle buffer PRDBUF , T8Pn The cycle count value register T8PnP Comparing match; when T8PnPMS = 1 When the update cycle register T8PnP Value to the cycle buffer PRDBUF , T8Pn Cycle buffer count value and PRDBUF Compare match.

when T8Pn The cycle count value register T8PnP (when T8PnPMS = 0) Or cycle buffer PRDBUF (when T8PnPMS = 1) Match equal, the cycle interrupt flag T8PnPIF Put 1 The flag needs to be cleared by software. Simultaneously T8Pn Is automatically cleared and resume counting Meanwhile divider plus 1 count. When the count value after the divider ratio of the frequency divider are the same frequency, the frequency divider is reset, and the timer interrupt flag T8PnTIF Put 1 The flag needs to be cleared by software.

In timer mode, cycle buffer PRDBUF Update:

In the timer mode starting period, in order to be able to register period T8PnP It updates the value to cycle buffer PRDBUF , Subject to the following order: first set T8PnM = 0 And T8PnPMS = 1 Before enabling T8PnE = 1 .

After the initial period, each T8Pn Cycle buffer count value and PRDBUF After matching equal, it will automatically update cycle buffer.



Map 6-2 T8Pn Timer Mode Timing Chart

6. 1. 6 PWM Output Mode

when T8PnM = 1 And T8PnE = 1 Time, T8Pn work at PWM mode.

Count clock source as the system clock divided by two Fosc / 2 And supports prescaler. After the divider settings do not affect PWM Output and duty cycle, affects only match interrupted T8PnTIF Interrupt flag, see " T8Pn After the divider configuration table. "

in PWM Mode, PWM Output from the register T8PnTRN Position control.

when T8PnTRN = 1 Time, PWM Output is always 0 And will not update T8PnP with T8PnR Value of the buffer register to cycle PRDBUF Buffer and precision RESBUF .

when T8PnTRN = 0 Time, PWM The output waveform to start and PWM Output start of 1 , Respectively, while T8PnP with T8PnR To update the contents of register cycle buffer PRDBUF Buffer and precision RESBUF (Software can not read and write buffer), followed by T8Pn Scratch counts, when T8Pn versus RESBUF Of equal value, PWM Output is changed 0 And continues to count up. when T8Pn The count value PRDBUF Equal, PWM Output is restored 1 ,Simultaneously PRDBUF with RESBUF Were loaded again T8PnP with T8PnR Value of the register, and generates an interrupt period T8PnPIF Interrupt flag, the flag needs to be cleared by software. Simultaneously T8Pn Is automatically cleared and resume counting after the divider plus 1 count. At this point a complete PWM Cycle is complete, the new cycle then continues PWM cycle. When the count value after the divider ratio of the frequency divider are the same frequency, the frequency divider is reset, and the timer interrupt flag

T8PnTIF Put 1 The flag needs to be cleared by software.

in PWM Mode, accuracy buffer RESBUF And cycle buffer PRDBUF Update:

in PWM Mode starting period, in order to be able to T8PnP with T8PnR Value of the buffer register to cycle PRDBUF Buffer and precision RESBUF , Subject to the following order: first set T8PnM = 1 , T8PnPMS = 1 with T8PnE = 1 ,

Then set PWM Output Enable T8PnTRN = 0 .

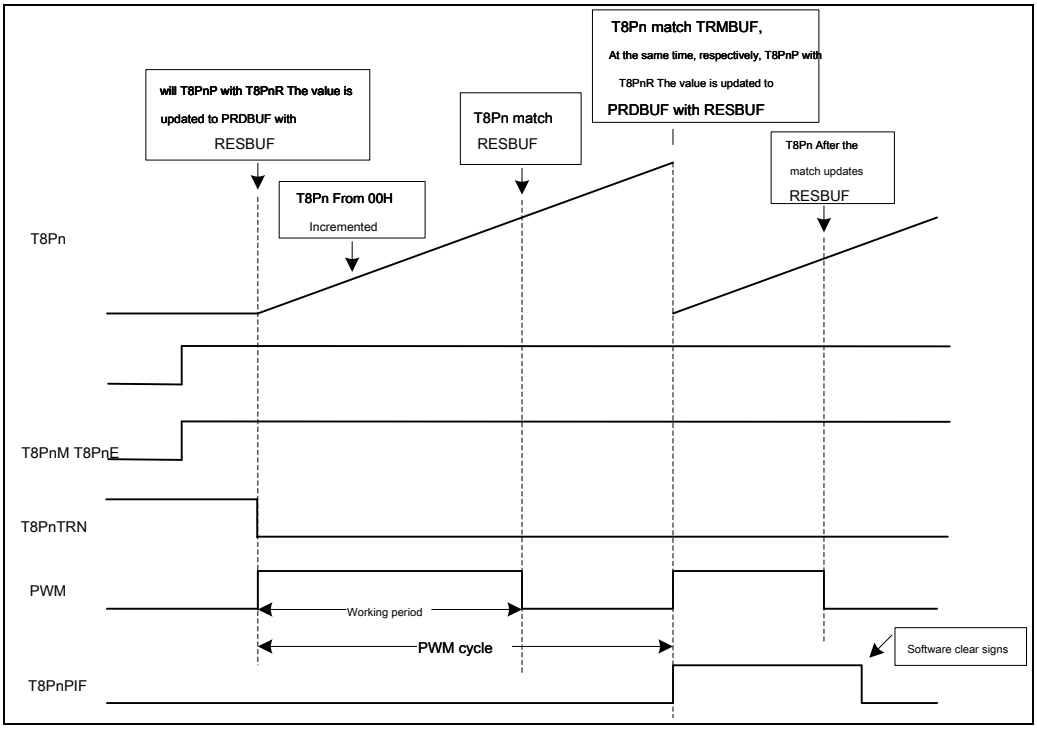
After the initial period, each T8Pn Cycle buffer count value and PRDBUF After the match equal, and it will automatically update cycle buffer precision registers.

Note 1 : If the accuracy buffer RESBUF Value 0 , The current PWM Cycle PWM Output is always 0 ;

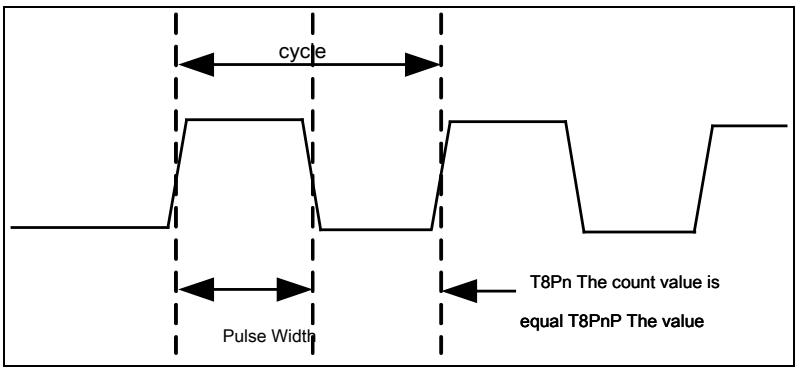
If the accuracy of the buffer register RESBUF Value is not less than PRDBUF , The current PWM Cycle PWM Output is always 1 . Note 2 : Reading T8PnTRN State bits, read the bit is written to this bit inverse logic value, i.e., when this bit is written 0 When the read value 1 ;

When this bit is written 1 When the read value 0 . Note 3 : If T8PnTRN = 1 ,then PWM Export 0 And the cycle buffer is not updated (either holds the initial value 0xFF Either as T8PnTRN = 0 Time,

Last updated value).



Map 6-3 T8Pn PWM Schematic model



Map 6-4 PWM Output schematic

PWM Calculated as follows:

PWM Cycle = [(T8PnP) +1] × 2 × Tosc × (T8Pn Prescale factor)

PWM Frequency = 1 / (PWM cycle)

When you select 9 Place PWM Output accuracy:

PWM Width = (T8PnR × 2 +1 + T8PnREX) × Tosc × (T8Pn Prescale factor)

PWM Precision registers T8PnR for 8 Bit registers, while increasing 1 Place T8PnREX As a T8PnR The lowest bit extensions, the pulse width control based on the system clock Fosc Prescaler.

When you select 8 Place PWM Output accuracy:

PWM Width = (T8PnR +1) × 2 × Tosc × (T8Pn Prescale factor)

PWM Duty Cycle = [PWM Pulse width] / [PWM cycle]

PWM The maximum resolution of the formula:

$$\text{Resolution} = \frac{\log\left(\frac{Fosc}{Fpwm * [\text{Multiple prescaler}}\right)]}{\log 2}$$

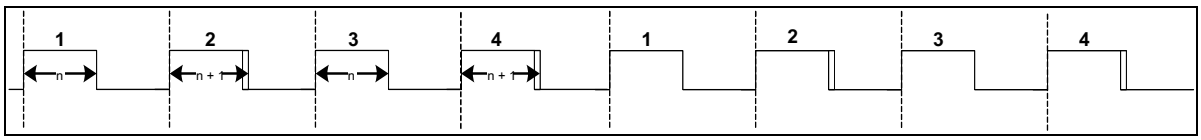
Note 1 : Tosc = 1 / Fosc , Fpwm = 1 / (PWM cycle)

6. 1. 7 PWM Average precision extension

PWM The maximum resolution of up to 9 Bit further refine PWM Precision output, by setting bit extended precision T8PxRE <1: 0> (T8PxOC <5: 4>)get on PWM Average accuracy extension. Application of this principle is continuous pattern output waveform for the pulse width interval plus 1 (plus 1 More LSB That increases the pulse width 1 More Tosc × [Prescaler multiples] (see PWM Formula)), to achieve PWM The average duty cycle waveform thinning.

Extended precision bit may be set 0 , 1/4 , 2/4 , 3/4 Altogether 4 An extended-precision values, equivalent to PWM Average precision extension 2 Bit.

For example, when the extension is set to the precision 2/4 , which is 4 More PWM There pulse width 2 A pulse width increases 1 More LSB And increase 1 More LSB Evenly distributed in the pulse width 4 A pulse width, as shown in FIG assumed as pulse width n ,then 4 Switching cycle (PWM Cycle) average pulse width n + 1/2 So that without increasing the clock frequency to achieve the equivalent of a high resolution PWM .



Map 6-5 PWM Extended precision schematic

6. 1.8 PWM Multiplexed output port

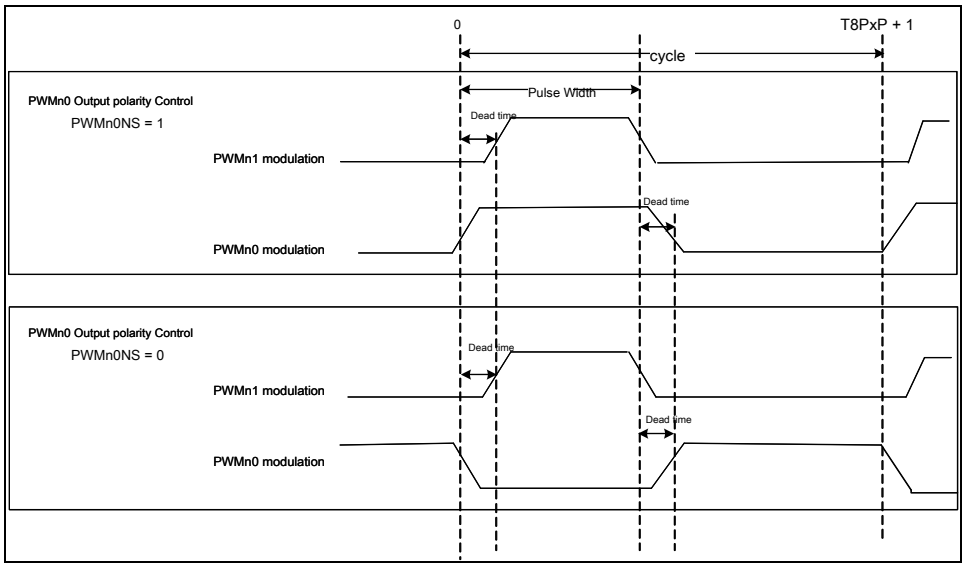
T8Pn Each supporting a pair of complementary PWM Output port, PWMn0 with PWMn1 , Supports adjustable dead-time configuration, the dead time can be T8PnPDT Register settings.

PWM Dead-band delay time calculation formula: T8PnPDT <7: 0> x Tosc .

By setting T8PnOC Register T8PnPEN <1: 0> with T8PnNEN <1: 0> ,select T8Pn of PWMn0 with PWMn1 versus I / O Complex output pins used.

PWMn0 Register output polarity by ANS <7: 6> (PWM20NS , PWM10NS) To be set.

It is worth noting that in the can PWM Before output, and to be first PWM Multiplexing corresponding I / O Port control register bit PxT Set to output state, otherwise there will be no PWM Waveform output.



Map 6-6 With dead complementary PWM Output schematic

6. 1.9 Special Function Register

T8Pn : T8Pn counter(T8P1 / T8P2)								
Bit	7	6	5	4	3	2	1	0
Name	T8Pn <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 **T8Pn <7: 0> : 8 Place T8Pn Count value, 00 H - FF H**

T8PnP : T8Pn Period register (T8P1P / T8P2P)								
Bit	7	6	5	4	3	2	1	0
Name	T8PnP <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	1	1	1	1	1	1	1	1

Bit 7 ~ 0 **T8PnP <7: 0> : PWM Period value**

T8PnR : T8Pn Precision registers (T8P1R / T8P2R)								
Bit	7	6	5	4	3	2	1	0
Name	T8PnR <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 **T8PnR <7: 0> : 8 Bit precision registers**

T8PnC : T8Pn Control Register (T8P1C / T8P2C)								
Bit	7	6	5	4	3	2	1	0
Name	T8PnM	T8PnPOS <3: 0>				T8PnE	T8PnPRS <1: 0>	
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 T8PnM : T8Pn Operating Mode Select bits

0 : Timer mode

1 : PWM mode

Bit 6 ~ 3 T8PnPOS <3: 0> : T8Pn After the frequency divider ratio selection bits

0000 : Dividing ratio 1: 10001 :

Dividing ratio 1: 20010 :

Dividing ratio 1: 3

...

1111 : Dividing ratio 1:16 8 After bit divider division ratio of the frequency division ratio by the extension register T8PnPEX After the division ratio 4 Bit extension bit T8PnPOSEX <3: 0> And the frequency division ratio lower 4 Bit Selection bit T8PnPOS <3: 0> Setting the frequency division ratio in the range 1: 1 to 1: 256 .

Bit 2 T8PnE : T8Pn Module Enable bit

0 :shut down

1 :Enable

Bit 1 ~ 0 T8PnPRS <1: 0> : T8Pn Prescaler division ratio selection bits

00 : Dividing ratio 1: 101 :

Dividing ratio 1: 4 1x :

Dividing ratio 1:16

T8PnPEX : T8Pn After the frequency divider ratio of extended registers (T8P1PEX / T8P2PEX)								
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	T8PnPOSEX <3: 0>			
R / W	-	-	-	-	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 4 Reserved for future use

Bit 3 ~ 0 T8PnPOSEX <3: 0> : The frequency division ratio 4 Bit extension bit

T8PnPMC : T8Pn Cycle Match Control Register (T8P1PMC / T8P2PMC)								
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	T8PnRS	T8PnPMS
R / W	-	-	-	-	-	-	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 2 Reserved for future use

Bit 1 T8PnRS : PWM Select bit output accuracy

1 : 9 Place PWM Output Accuracy

0 : 8 Place PWM Output Accuracy

Bit 0 T8PnPMS : Cycle timer mode select bit Match

0 : T8Pn Period count value register T8PnP Match

1 : T8Pn Cycle buffer count value PRDBUF Match

T8P1OC : T8P1 Output control register								
Bit	7	6	5	4	3	2	1	0
Name	T8P1TRN	T8P1REX	T8P1RE <1: 0>		T8P1NEN <1: 0>		T8P1PEN <1: 0>	
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 T8P1TRN : PWM Output Enable bit

1 : Stopped (reset waveform, the counter is reset)

0 : Enable (waveform generation)

Bit 6 T8P1REX : PWM Bit extended precision mode

Bit 5 ~ 4 T8P1RE <1: 0> : T8P1 of PWM1 The average accuracy extension bit

00 : 001 : 1/4

10 : 2/4 11 : 3/4

Bit 3 ~ 2 T8P1NEN <1: 0> : T8P1 of PWM1 Complementary output pin select bit

00 : PWM10 Output Close

01 : PA2 Export PWM10 10 : PB1 Export

PWM10 11 : PB3 Export PWM10

Bit 1 ~ 0 T8P1PEN <1: 0> : T8P1 of PWM1 Output pin select bit

00 : PA1 Export PWM11 01 : PB0

Export PWM11 10 : PA6 Export PWM11

11 : PB2 Export PWM11

T8P2OC : T8P2 Output control register								
Bit	7	6	5	4	3	2	1	0
Name	T8P2TRN	T8P2REX	T8P2RE <1: 0>	T8P2NEN <1: 0>			T8P2PEN <1: 0>	
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 T8P2TRN : PWM Output Enable bit

1 : Stopped (reset waveform, the counter is reset)

0 : Enable (waveform generation)

Bit 6 T8P2REX : PWM Bit extended precision mode

Bit 5 ~ 4 T8P2RE <1: 0> : T8P2 of PWM2 The average accuracy extension bit

00 : 001 : 1/4

10 : 2/4 11 : 3/4

Bit 3 ~ 2 T8P2NEN <1: 0> : T8P2 of PWM2 Complementary output pin select bit

00 : PWM20 Output Close

01 : PB0 Export PWM20 10 : PA6 Export

PWM20 11 : PB2 Export PWM20

Bit 1 ~ 0 **T8P2PEN <1: 0> : T8P2 of PWM2 Output pin select bit**

00 : PA2 Export PWM21 01 : PB1 Export

PWM21 10 : PB3 Export PWM21

11 : PWM21 Output Close

T8PnPDT : T8Pn PWM Dead time control register								
Bit	7	6	5	4	3	2	1	0
Name	T8PnPDT <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 **T8PnPDT <7: 0> : PWM Dead-time delay T8PnPDT x Tosc**

6.2 A / D converter module (ADC)

6. 2.1 Outline

Analog to digital converter for converting the analog signal into a set of digital signals composed of binary code. Analog signal input via the multiplexer input pin, through a sample - and-hold circuit is connected to the input of the converter. The chip supports 12-bit 6 + 2

Channels A / D Converter, after A / D Converter converts 12-bit The binary data stored ADC Data register

ADCRH , ADCRL in.

- A / D Converter Characteristics

  --12 Place ADC Sampling accuracy

  - 6 Analog inputs + 2 Power supply voltage detecting passage optional

  --12 Bit conversion, placed in alignment support high or low placed in alignment

  - Support external or internal reference voltage selectable
  - Support supply voltage detection, an optional power supply voltage division ratio
  - **Support configurable A / D Conversion clock**
  - **Clock from the system clock source Fosc**

- The main functional components

  - ADC Conversion value register (ADCRL , ADCRH)

  - ADC Control Register (ADCCL , ADCCH)

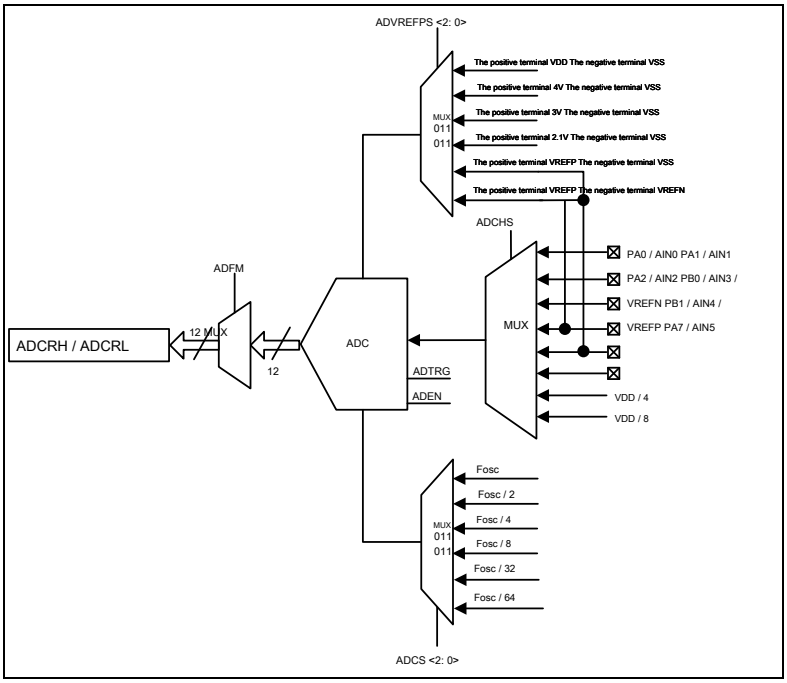
  - Port type selection register (ANS)

  - ADC Automatically trigger register (ADCTR)

- Interruption and suspension

  - **stand by A / D Conversion interrupt (ADIE / ADIF)**

6. 2.2 ADC e



Map 6-7 ADC e

6. 2. 3 ADC Configuration

ADC Circuit before use, need to be properly configured for the following aspects needed before correct desired conversion results.

Clock Select

ADC The clock circuit are required 7 Optional group, Fosc ~ Fosc / 64 ,accessible ADCCH Select the desired register clocks.

Reference voltage selection

ADC Circuits using a positive reference voltage and a negative reference voltage, the reference voltage corresponding to the external input pin, respectively VREFP with VREFN . Since the two external input pins, respectively PB1 / AIN4 , PB0 / AIN3 Multiplexing, when using the two external reference voltage input, must first pass ANS Register set correctly multiplexing port type. Positive reference voltage by ADVREFS <2: 0> Choice VDD , 4V , 3V , 2.1V or it could be VREFP Multiplexing port, a negative reference voltage corresponding to the selected VSS or it could be VREFN Port Multiplexed. The positive terminal of the reference voltage selection in 2.1V When, in accordance with the need to VDD Voltage by AD2VCALS Bit (ADCTR <0>) Set correctly A / D 2.1V The reference voltage adjustment information.

Sample time

This chip supports ADC Alternatively the sampling time of the circuit, by ADCCH Register ADST <3: 0> About Choice 1 to 15 More Tadclk Altogether 15 Kinds of options.

Multiplexing port type selected

This chip ADC All analog input channels circuit AINn , The reference voltage of the external input pins and are PA / PB Port multiplexing, using ADC Before conversion circuit, the pin must first be used by ANS Register is set to the analog type.

Analog input channel

ADC Before the circuit is enabled, you must first select A / D Analog channels. This chip ADC Circuit support 6 And external channel 2 Power supply voltage detecting passage Alternatively, the outer channel respectively, AIN0 ~ AIN5 , Two detection channels are the power supply voltage VDD / 4 with VDD / 8 . A / D Analog channel through which channel to select ADCCL Register ADCHS <2: 0> Bit.

Alignment options

This chip ADC The results of the conversion circuit supports two alignment, low and high alignment aligned by ADCCH Register ADFM Bit selection.

ADC Module conversion trigger mode selection

This chip ADC Module supports two A / D Conversion Trigger: software trigger and PWM Automatic trigger.

in ADC Enable bit conversion module ADEN (ADCCL <0>) When enabled, the software will ADC Conversion Status bit ADTRG (ADCCL <1>) Is set to " 1 " ADC Module begins converting, this software trigger A / D Conversion; in ADC Enable bit conversion module ADEN (ADCCL <0>)with PWM Automatically trigger ADC Enable TRIGEN (ADCTR <4>) Are able to make after by PWM Edge trigger signal causes ADTRG Bit is automatically set to " 1 " ADC Modules start the conversion, such as PWM Automatic trigger.

PWM Alternatively automatically trigger source from PWMn1 Signal, by automatically trigger source selection TRIGS (ADCTR <6>) Selection, PWM Edge triggered automatically by TRIGPEG Bit (ADCTR <5>)select PWM Rising or falling edge trigger.

It is worth noting that, in the use PWM Automatically trigger ADC It is recommended to inquiry ADTRG The current state of the bit. If the

Queried ADTRG Bit " 1 "When, in this period PWM Edge automatically trigger signals are ignored until ADTRG

Status bit is reset to " 0 "After the system is detected again PWM Automatic edge trigger signal, will respond PWM Automatically trigger ADC Module conversion.

6. 2. 4 ADC Conversion step

Overview achieve the following ADC Each step of the conversion process.

Step 1 :select ADC Conversion clock, by ADCCH Register ADCS <2: 0> select ADC Conversion clock.

Step 2 : Select the negative reference voltage by ADCCL Register ADVREFNS Bit selection.

Step 3 : ADC Sample time, by ADCCH Register A / D Sampling time select bits ADST <3: 0> set up.

Step 4 : Multiplex port is provided to an analog type, i.e. which is selected as the pin ADC Converting an input pin, the port type selection register ANS Control options.

Step 5 : Analog input is selected channels AINx ,by ADCCL Register ADCHS <2: 0> select ADC Analog channels.

Step 6 : Setting the conversion result alignment, by ADCCH Register ADFM Bit selects the high or low placed in alignment is properly aligned.

Step 7 : If you are using an interrupt, the interrupt control registers must be correctly configured to ensure the A / D Interrupt function is activated correctly. In interrupt mode, the global need to interrupt enable bit GIE Set to "1" with ADC Interrupt enable bit "1" .

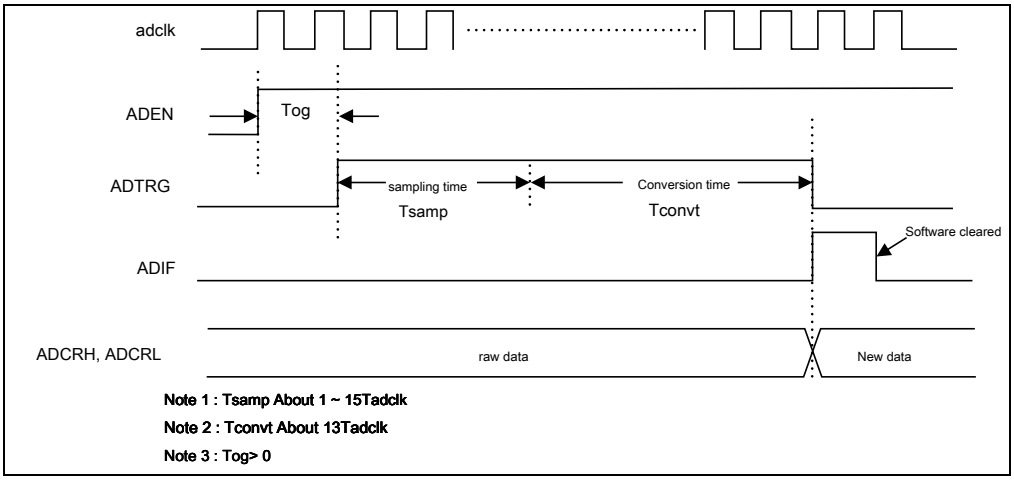
Step 8 :Enable ADC Circuit, the ADCCL Register ADC Enable ADEN Set as "1" .

Step 9 :select ADC Module conversion software trigger or trigger PWM Automatic trigger. If you select software trigger, the ADCCL Register ADC Start bit conversion ADTRG Bit is set to "1" To begin ADC Conversion; if you choose PWM Automatic trigger, you must first set TRIGS Choice and automatic trigger source TRIGPEG Choice PWM Automatically trigger edge setting PWM Automatically trigger ADC Enable TRIGEN for" 1 ".in PWM Automatically trigger ADC
After complete conversion setting module, automatic edge trigger signal will automatically ADTRG Location " 1 "Started ADC Conversion.

Step 10 :polling ADCCL Conversion status bit register ADTRG Place, determine the A / D The conversion is complete.

Step 11 : Read ADCRH with ADCRL Conversion result register.

6. 2. 5 AD Timing Characteristics schematic



Map 6-8 ADC Timing Characteristics schematic

6. 2. 6 ADC Application routines

Application Example: analog input channels 0 (AIN0 Analog to digital conversion)

```
        BCC     ANS, 0          ; AIN0 Where the port is configured as an analog port
        BCC     ADCCH, ADFM     ; High conversion results placed in alignment
        MOVI    0X01
        MOVA    ADCCL           ;Enable ADC Converter, the selected channel 0
        BSS     ADCCL, ADTRG    ;trigger ADC Change
AD_WAIT:
        JBC     ADCCL, ADTRG    ;wait ADC The conversion is complete
        GOTO AD_WAIT MOV
                ADCRH, 0        ; High reading 8 Bit conversion result
        ... ... MOV
                ADCRL, 0        ; Low reading 4 Bit conversion result
        ... ...
```

6. 2.7 Special Function Register

ADFM	ADCRH : ADC High conversion value register 8 Place								ADCRL : ADC Low conversion value register 8 Place							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	-	-	-	-	ADCR <11: 8>				ADCR <7: 0>							
0	ADCR <11: 4>												ADCR <3: 0>		-	-	-	-

ADCR <11: 0> : A / D Conversion results

ADCCL : ADC Control Register Low 8 Place								
Bit	7	6	5	4	3	2	1	0
Name	AD VREFS <2: 0 >			A DCHS <2: 0 >			ADTRG	ADEN
R / W	R / W	R / W	R / WR / W		R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 5 ADVREFS <2: 0> : Select bit reference voltage source

000 : ADC The positive terminal of the reference voltage VDD , Negative end as VSS 001 : ADC The positive terminal of the reference voltage 4.0V , Negative end as VSS 010 : ADC The positive terminal of the reference voltage 3.0V , Negative end as VSS 011 : ADC The positive terminal of the reference voltage 2.1V , Negative end as VSS 100 : ADC Reference voltage at the positive terminal of the external VREFP , Negative end as VSS 101 : ADC Reference voltage at the positive terminal of the external VREFP , Negative end as VREFN

Others: Reserved

Bit 4 ~ 2 ADCHS <2: 0> : A / D Channel selection bits

000 :aisle 0 (AIN0)

001 :aisle 1 (AIN1)

010 :aisle 2 (AIN2)

011 :aisle 3 (AIN3)

100 :aisle 4 (AIN4)

101 :aisle 5 (AIN5)

110 : VDD / 4 111 : VDD / 8

Bit 1 ADTRG : ADC Conversion Status bit

0 : ADC Conversion is not performed, or A / D Conversion has been completed

1 : ADC Conversion is in progress, this position 1 start up A / D Change

Bit 0 ADEN : ADC Enable

0 :shut down

1 :Enable

ADCCH : ADC Control Register High 8 Place								
Bit	7	6	5	4	3	2	1	0
Name	ADFM	A DCS <2: 0>			ADST <3: 0>			
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	1	0	0	0

Bit 7 ADFM : ADC Converts the data format selection bit

0 : High-aligned (ADCRH <7: 0>, ADCRL <7: 4>)

1 : Low alignment (ADCRH <3: 0>, ADCRL <7: 0>)

Bit 6 ~ 4 ADCS <2: 0> : ADC Clock select bits

000 : Fosc 001 : Fosc

/ 2 010 : Fosc / 4

011 : Fosc / 8 100 : Fosc

/ 16 101 : Fosc / 32

110 : Fosc / 64 111 :

Reserved

Bit 3 ~ 0 ADST <3: 0> : A / D Sampling time select bits

0000 : Do not use

0001 to 1111 : ADC Respectively corresponding to sampling time 1 to 15 More ADC Clock (default value 8)

ADCTR : ADC Automatically trigger register

Bit	7	6	5	4	3	2	1	0
Name -		TRIGS	TRIGPEG	TRIGEN	-	-	-	AD2VCALS
R / W -		R / W	R / W	R / W	-	-	-	R / W
POR	0	0	0	0	0	0	0	0

Bit 7, 3 ~ 1 Reserved for future use

Bit 6 TRIGS : Automatically trigger source selection

0: PWM11 1:

PWM21

Bit 5 TRIGPEG : PWM Automatically trigger ADC Edge selection bit

0 : PWM Rising

1 : PWM Falling

Bit 4 TRIGEN : PWM Automatically trigger ADC Enable

0 : Prohibition

1 :Enable

Bit 0 AD2VCALS : A / D The positive terminal of the reference voltage 2.1V Calibration Select bit

0 : VDD = 5V When A / D The positive terminal of the reference voltage 2.1V Calibration value

1 : VDD = 3V When A / D The positive terminal of the reference voltage 2.1V Calibration value

6.3 Low voltage detection module (LVD)

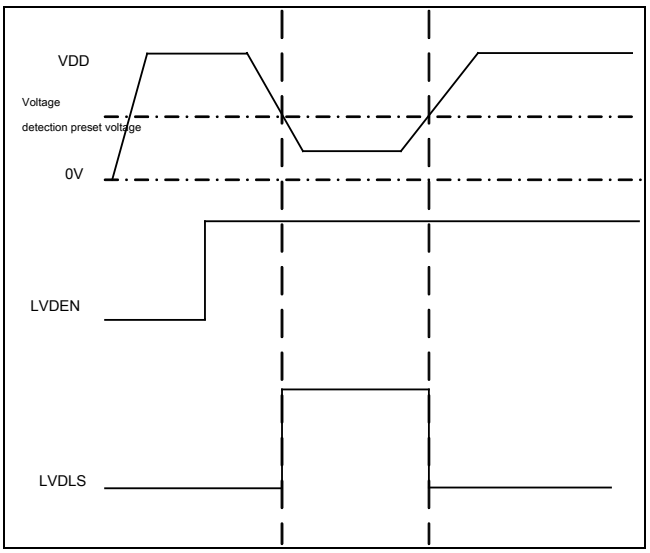
6. 3.1 Outline

A set of low-chip voltage detecting module, to support low-voltage detecting function, i.e., LVD This feature enables the device to monitor the supply voltage VDD . In the case of unstable power supply, external power supply as noise or crosstalk EMS Under the conditions tested, will power vigorous shaking. When the target voltage is not stable, it will likely lower than the operating voltage. If the detected voltage is below a certain value required to provide a warning signal. Low-voltage detection signal can generate an interrupt.

6.3.2 LVD operating

LVD Enable the disable function LVDC Register LVDEN Control bits. when LVDEN Bit is cleared, LVD Function disabled. when LVDEN High position, LVD Feature enabled. LVD Module power supply voltage VDD Compared with the preset voltage, the comparison results LVDC Register LVDLS Bit query. A preset voltage threshold LVDC Register LVDV <1: 0> Configuration, preset voltage range 2.1V ~ 3.6V . When the target voltage is lower than a preset voltage value, LVDLS

Bit is set high, indicating the detection of a low voltage generator, generating LVD Interrupt flag. when LVD An interrupt is generated when the enable on LVD Interrupt request.



Map 6-9 LVD Operation Timing Chart

6. 3.3 Special Function Register

LVDC : LVD Detection Register								
Bit	7	6	5	4	3	2	1	0
Name LVDLS		-	-	LVDEN - -			LVDV <1: 0>	
R / W	R	-	-	R / W	-	-	R / W	R / W
POR	0	0	0	1	0	0	0	0

Bit 7 LVDLS : LVD Voltage detection status bit

0 : Supply voltage is higher than the preset voltage

1 : Supply voltage is below the predetermined voltage

Bit 6 ~ 5,3 ~ 2 Reserved for future use

Bit 4 **LVDEN : LVD Enable**

0 : Prohibition

1 :Enable

Bit 2 ~ 0 **LVDV <1: 0> : LVD Voltage detection selection bit**

00 : 2.1V 01 : 2.4V

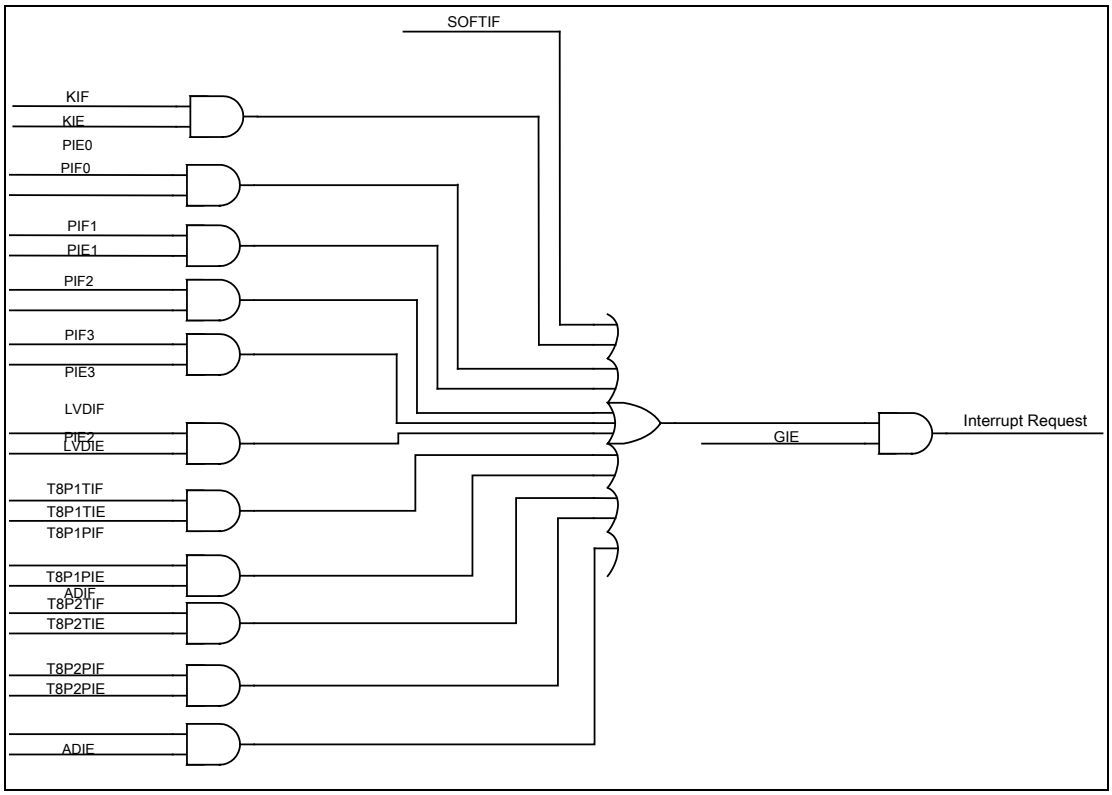
10 : 3.0V 11 : 3.6V

The first 7 chapter MCU - interrupt handling

7.1 Outline

Interrupts are an important function of the chip. It will wake up from sleep mode, you can also make the system response during normal operation of emergency, suspend and save the currently running program, jump to the entry address of the interrupt request, execute the corresponding interrupt service routine, handling emergencies. This chip supports only the default interrupt mode, it can support up to 12 Interrupt sources, 1 Software interrupts and 11 A hardware interrupt.

7.2 Internal structure



Map 7-1 Interrupt control logic

7. 2.1 The default interrupt mode

This chip supports only the default interrupt mode, all entry address of the interrupt vectors are located 004H. Each user must interrupt source flag and enable bit to distinguish which is the interrupt source caused the interrupt by interrupt subroutine determines to execute the corresponding interrupt service routine.

No.	Interrupt name	Interrupt Flag	Interrupt Mask	interrupt enable	global enable	interrupt entry address
1	Soft interrupt	SOFTIF	-	-	GIE	004H
2	KINT0	KIF	KMASK0	KIE	GIE	
	KINT1		KMASK1			
	KINT2		KMASK2			
	KINT3		KMASK3			
	KINT4		KMASK4			

No.	Interrupt name	Interrupt Flag	Interrupt Mask	interrupt enable	global enable interrupt	entry address	
	KINT5		KMSK5				
	KINT6		KMSK6				
	KINT7		KMSK7				
3	PINT0	PIF0	-	PIE0	GIE		
4	PINT1	PIF1	-	PIE1	GIE		
5	PINT2	PIF2	-	PIE2	GIE		
6	PINT3	PIF3	-	PIE3	GIE		
7	LVDINT	LVDIF	-	LVDIE	GIE		
8	T8P1TINT	T8P1TIF	-	T8P1TIE	GIE		
9	T8P1PINT	T8P1PIF	-	T8P1PIE	GIE		
10	T8P2TINT	T8P2TIF	-	T8P2TIE	GIE		
11	T8P2PINT	T8P2PIF	-	T8P2PIE	GIE		
12	ADINT	ADIF	-	ADIE	GIE		

table 7-1 The default mode interrupt logic interrupt table

(Note: KINT6 unavailable.)

7.3 Interrupt Context

Interrupt Context interrupt program is a very important part. Command system has PUSH (Push) and POP (Stack) instruction can be used to implement data storage interrupt. You can save the data include: Accumulator A Register, a program status word register PSW , IAA Register and PCRH register. Protect other data registers need to use other instructions. Can be continuous 2 Secondary PUSH The first 3 Secondary PUSH

It will make the first time PUSH Data loss. Similarly, more than 2 Times in a row POP The first 3 Secondary POP Data recovery can not be expected.

7.4 Interrupt operation

7. 4.1 Interrupt enable bit GIE Operations

Each hardware interrupt source has its own interrupt enable and interrupt flag bits, initialize the corresponding hardware interrupt, you need to clear the interrupt flag before enabling the current interrupt. If enabled before does not clear the interrupt flag, there may be circumstances incursion into the interrupt occurred. In addition to support each interrupt interrupt enable herein, this chip also provides a global interrupt. Therefore, after all the initialization needed break, please enable global interrupts.

If the interrupt event condition occurs, the related interrupt flag will be set "1" . After the interrupt flag generating program to jump to the address corresponding service execution must meet the following conditions:

1. When the corresponding interrupt enable bit "1" When, continues to determine a second condition is met; when the corresponding interrupt enable bit "0" , Even if the interrupt flag "1" , It will not interrupt occurs, the program does not jump to interrupt service address execution.

2. When the global interrupt enable bit GIE for "0" It will block all interrupt requests. When the global interrupt enable bit GIE for "1" , The program jumps to execute the interrupt service address.

To ensure register GIE Software write operation is successful, adjustment shall be as follows:

Correct GIE Bit software cleared 0 Operation, you must first turn off all peripheral interrupts enabled, then GIE Cleared 0 ; Or GIE Place

clear 0 After the operation, inquiry GIE Bit is set 0 , Is not 0 Proceed to clean 0 Operation until it is successful; for GIE Bit software set 1 Operation, no special requirements, it is recommended to open the desired peripheral interrupt enable, and then GIE position 1 .

7. 4.2 External Interrupt

when PINTn Multiplexing port is configured as a digital input port, the input signal changes and the trigger condition is met, it will produce PINTn External port interrupt, the corresponding interrupt flag PIFn It is set "1" . When the global interrupt control bit GIE And interrupt control bit external port PIEn They are set to "1" , Then to CPU issue PINTn External port interrupt request. When the interrupt conditions permit, the system will enter the entry address of the interrupt service routine, the interrupt program processing.

It is noteworthy that the corresponding interrupt flag PIFn And interrupt enable bits PIEn We had to go through software removal, INTC1 Register PEGn Bits for configuring the trigger condition, are arranged to be rising or falling edge triggered.

7. 4.3 External Key interrupt

when KINn Multiplexing port is configured as a digital input port, a port of any change in the level of the input signal is not masked keys occurs, the interrupt flag bit KIF Set to "1" , When the external interrupt control bit key KIE for "1" And global interrupt control bit GIE After the bit is enabled, then the CPU External interrupt request issued keys. When the external interrupt conditions permit key, the system will enter the entry address of the interrupt service routine, the interrupt program processing.

When using an external key interrupt shall configure the control register, and to enable the external interrupt key internal port pull-up resistor.

In the key interrupt enable (KMSKn = 1 , KIE = 1) Before the first port register read or write operation, clear the interrupt flag, so as to avoid an interrupt is generated.

Clear the interrupt flag KIF Steps:

1) Port register read or write operation, the conditions do not match the level of the end of the port latch value;

2) Software clear interrupt flag KIF . Interrupt enable bit KIE Also you need to be cleared by software.

7. 4. 4 T8Pn (T8P1 / T8P2) Timer interrupt

8 Place PWM Base Timer T8Pn In timer mode and PWM Mode, the counting clock counts, when T8Pn After the count value and the frequency divider ratio of the frequency divider dividing the same, the interrupt flag T8PnTIF position "1" . when T8Pn Timer interrupt enable bit T8PnTIE Set to "1" And global interrupt control bit GIE When enabled, then the CPU issue T8Pn Timer interrupt request. when T8Pn When the timer interrupt conditions permit, the system will enter the entry address of the interrupt service routine, the interrupt program processing. It is worth noting that, T8Pn Timer interrupt flag T8PnTIF And interrupt enable bits T8PnTIE They are required to be cleared by software.

7. 4. 5 T8Pn (T8P1 / T8P2) Periodic interrupt

8 Place PWM Base Timer T8Pn In timer mode and PWM When mode, it can generate periodic interrupts. when T8Pn Counter with T8PnP When the value of the register is equal to (PWM When mode, T8Pn Counting up from scratch), generated T8Pn Periodic interrupt, the interrupt flag T8PnPIF It is set "1" . If the interrupt enable bit T8PnPIE Set to "1" And global interrupt control bit GIE When enabled, then the CPU issue T8Pn Periodic interrupt requests. when T8Pn When conditions permit periodic interrupt, the system will enter the entry address of the interrupt service routine, the interrupt program processing. It is worth noting that, T8Pn Periodic Interrupt Flag T8PnPIF And interrupt enable bits T8PnPIE They are required to be cleared by software.

7. 4. 6 ADC Interrupt

ADC Interrupted by ADC Conversion operation control, when ADC When the conversion is complete, the generated ADC Interruption, ADC Interrupt flag ADIF It is set "1" . when ADC Interrupt control bit ADIE Set to "1" And global interrupt control bit GIE When enabled, then the CPU issue ADC Interrupt request. when ADC Interrupt conditions permit, the system will enter the entry address of the interrupt service routine, interrupt procedures. It is worth noting that, ADC Interrupt flag ADIF And interrupt enable bits ADIE They are required to be cleared by software.

7. 4. 7 LVD Interrupt

when VDD Voltage is less than LVDC A register set threshold voltage, a low voltage is generated, LVDLS After rising or falling edge trigger interrupt flag LVDIF Bit is set "1" . If the interrupt enable bit LVDIE Set to "1" And global interrupt control bit GIE When enabled, then the CPU issue LVD Interrupt request. when LVD Interrupt conditions permit, the system will enter the entry address of the interrupt service routine, interrupt procedures. It is worth noting that, LVD Interrupt flag LVDIF And interrupt enable bits LVDIE They are required to be cleared by software.

7. 4.8 Interrupt Handling Precautions

Before the user can interrupt must first clear the corresponding interrupt flag to avoid interruption of false triggering.

In addition to the read-only interrupt flag (cleared by hardware), the rest must be cleared by software.

7.5 Special Function Register

INTF0 : Interrupt flag register 0								
Bit	7	6	5	4	3	2	1	0
Name	T8P2PIF	T8P1PIF	ADIF	LVDIF	-	T8P2TIF	T8P1TIF	KIF
R / W	R / W	R / W	R / W	R / W	-	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 T8P2PIF : T8P2 Periodic Interrupt Flag

0 : T8P2 No counter match occurs

1 : T8P2 Counter match occurred (to be cleared)

Bit 6 T8P1PIF : T8P1 Periodic Interrupt Flag

0 : T8P1 No counter match occurs

1 : T8P1 Counter match occurred (to be cleared)

Bit 5 ADIF : ADC Interrupt flag

0 :not initiated ADC Conversion or conversion in progress

1 : ADC Conversion completed (must be cleared in software)

Bit 4 LVDIF : LVD Interrupt flag

0 : Never detected voltage is lower than a preset value

1 : Detection voltage is lower than the preset value (must be cleared in software)

Bit 3 Reserved for future use

Bit 2 T8P2TIF : T8P2 Timer interrupt flag

0 : T8P2 No counter match occurs

1 : T8P2 Counter match occurred (to be cleared)

Bit 1 T8P1TIF : T8P1 Timer interrupt flag

0 : T8P1 No counter match occurs

1 : T8P1 Counter match occurred (to be cleared)

Bit 0 KIF : External key interrupt flag

0 : External key port without a level change

1 : There are changes in the level of external key port (must be cleared in software)

INTE0 : Interrupt Enable register 0								
Bit	7	6	5	4	3	2	1	0
Name	T8P2PIE	T8P1PIE	ADIE	LVDIE	-	T8P2TIE	T8P1TIE	KIE
R / W	R / W	R / W	R / W	R / W	-	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 T8P2PIE : T8P2 Periodic interrupt enable bit

0 : Prohibition T8P2 Interrupt

1 :Enable T8P2 Interrupt

Bit 6 T8P1PIE : T8P1 Periodic interrupt enable bit

0 : Prohibition T8P1 Interrupt

1 :Enable T8P1 Interrupt

Bit 5 ADIE : ADC Interrupt enable bit

0 : Prohibition ADC Interrupt

1 :Enable ADC Interrupt

Bit 4 LVDIE : LVD Interrupt enable bit

0 : Prohibition LVD Interrupt

1 :Enable LVD Interrupt

Bit 3 Reserved for future use

Bit 2 T8P2TIE : T8P2 Timer interrupt enable bit

0 : Prohibition T8P2 Interrupt

1 :Enable T8P2 Interrupt

Bit 1 T8P1TIE : T8P1 Timer interrupt enable bit

0 : Prohibition T8P1 Interrupt

1 :Enable T8P1 Interrupt

Bit 0 KIE : External key interrupt enable bit

0 : Prohibition KIN0-7 Key interrupt

1 :Enable KIN0-7 Key interrupt

INTF1 : Interrupt flag register 1

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	PIF3	PIF2	PIF1	PIF0
R / W	-	-	-	-	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 4 Reserved for future use

Bit 3 PIF3 : PINT3 Port interrupt flag

0 : PINT3 No interrupt signal port

1 : PINT3 An interrupt signal (must be cleared in software) on port

Bit 2 PIF2 : PINT2 Port interrupt flag

0 : PINT2 No interrupt signal port

1 : PINT2 An interrupt signal (must be cleared in software) on port

Bit 1 PIF1 : PINT1 Port interrupt flag

0 : PINT1 No interrupt signal port

1 : PINT1 An interrupt signal (must be cleared in software) on port

Bit 0 PIF0 : PINT0 Port interrupt flag

0 : PINT0 No interrupt signal port

1 : PINT0 An interrupt signal (must be cleared in software) on port

INTE1 : Interrupt Enable register 1

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	PIE3	PIE2	PIE1	PIE0
R / W	-	-	-	-	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 4 Reserved for future use

Bit 3 PIE3 : PINT3 Port interrupt enable bit

0 : Prohibition PINT3 Port Interrupt

1 :Enable PINT3 Port Interrupt

Bit 2 PIE2 : PINT2 Port interrupt enable bit

0 : Prohibition PINT2 Port Interrupt

1 :Enable PINT2 Port Interrupt

Bit 1 PIE1 : PINT1 Port interrupt enable bit

0 : Prohibition PINT1 Port Interrupt

1 :Enable PINT1 Port Interrupt

Bit 0 PIE0 : PINT0 Port interrupt enable bit

0 : Prohibition PINT0 Port Interrupt

1 :Enable PINT0 Port Interrupt

INTC0 : Interrupt Control Register 0

Bit	7	6	5	4	3	2	1	0
Name	KMSKn <7: 0>							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 KMSKn <7: 0> : KINn Key input mask bits

0 :shield

1 : Not shield

INTC1 : Interrupt Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	PEG3	PEG2	PEG1	PEG0
R / W	-	-	-	-	R / W	R / W	R / W	R / W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 4 Reserved for future use

Bit 3 PEG3 : PINT3 Edge Select bit

0 : PINT3 Falling edge

1 : PINT3 Rising edge triggered

Bit 2 PEG2 : PINT2 Edge Select bit

0 : PINT2 Falling edge

1 : PINT2 Rising edge triggered

Bit 1 PEG1 : PINT1 Edge Select bit

0 : PINT1 Falling edge

1 : PINT1 Rising edge triggered

Bit 0 PEG0 : PINT0 Edge Select bit

0 : PINT0 Falling edge

1 : PINT0 Rising edge triggered

PINTS : External Interrupt selection register

Bit	7	6	5	4	3	2	1	0
Name	PINT3S <1: 0>		PINT2S <1: 0>		PINT1S <1: 0>		PINT0S <1: 0>	
R / W	W	W	W	W	W	W	W	W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 6 PINT3S <1: 0> : PINT3 Interrupt Source Selection

00 : PA7 01 : PA5

10 : PB3 11 :

Reserved

Bit 5 ~ 4 PINT2S <1: 0> : PINT2 Interrupt Source Selection

00 : PA6 01 : PA4

10 : PB2 11 :

Reserved

Bit 3 ~ 2 PINT1S <1: 0> : PINT1 Interrupt Source Selection

00 : PA1 01 : PA3

10 : PB1 11 : PB5

Bit 1 ~ 0 PINT0S <1: 0> : PINT0 Interrupt Source Selection

00 : PA0 01 : PA2

10 : PB0 11 : PB4

Note: This register is only writable and readable; therefore, need to use this register assignment MOVA , MOVAR instruction.

INTG : Global interrupt register

Bit	7	6	5	4	3	2	1	0
Name	GIE	-	-	-	-	-	SOFTIF	-
R / W	R / W	-	-	-	-	-	R / W	-
POR	0	0	0	0	0	0	0	0

Bit 7 GIE : Global Interrupt Enable bit

0 : Disable all interrupts

1 : Enables all unmasked interrupts

Bit 6 ~ 2 Reserved for future use

Bit 1 SOFTIF : Software interrupt flag

0 : No software interrupt

1 : Start the software interrupt

Bit 0 Reserved for future use

Note: Cleared by software GIE When the bit need determination GIE Clear whether the success, if not cleared, you need software to perform clear operation again until cleared success.

The first 8 chapter MCU - chip configuration word

Register Name	Chip configuration word (CFG_WD)	
address	7F2 H	
OSCS <2: 0>	bit2-0	Oscillator Selection bits 000 : LP Crystal / resonator is connected to PA4 with PA5 001 : Reserved for future use 010 : HS Mode: the crystal oscillator connected to the PA4 with PA5 011 : Reserved for future use 100 : XT Mode: the crystal oscillator connected to the PA4 with PA5 101 : Reserved for future use 110 : INTOSCO mode: CLKO From PA4 Output, PA5 for I / O 111 : INTOSC mode: PA4 for I / O , PA5 for I / O
WDTEN	bit3	Hardware watchdog enable bit 0 : Prohibition 1 :Enable
PWRTEB	bit4	Power-up Timer Enable bit 0 :Enable 1 : Prohibition
MRSTEN	bit5	MRSTN Pin function select bit 0 : For digital input pin 1 : Pin for external reset
-	bit7-6 Reservations, by default 1	
BORVS <1: 0>	bit9-8	The enable and reset voltage point selection bits 00 : Prohibition 01 : Enabled, the reset voltage 2.2V 10 : Enabled, the reset voltage 2.7V 11 : Enabled, the reset voltage 3.4V
-	bit10 Reservations, by default 1	
-	bit15-11 Reservations, by default 0	

Note 1 : CLKO System clock 16 Frequency output.

The first 9 chapter MCU -Instruction Set

9.1 Outline

This chip provides 79 Article reduced instruction.

Assembly instructions for the convenience of programmers use, mostly by command name abbreviation instruction function thereof. Program consisting of instructions after compiling the connector compiler, will be converted to the corresponding instruction code. Can be converted into the instruction code opcode (OP Code) Operand (Operand) In two parts. Portion corresponding to the instruction opcode itself. Chip runs 4MHz When the system clock, a machine cycle time 500ns . Machine-cycle instruction execution according to the number of instructions can be divided into two-cycle instruction and single-cycle instruction, wherein CALL , LCALL ,

RCALL , GOTO , JUMP , RET , RETIA , RETIE Two-cycle instruction; jump conditions are satisfied, JBC , JBS ,

JDEC , JINC Instruction for the two-cycle instruction, otherwise single-cycle instruction; other instructions as a single instruction cycle.

9.2 Operation instruction register

No.	instruction		Affect the status of the machine cycle		operating
1	SECTION	I <7: 0>	-	1	This chip does not support this instruction
2	PAGE	I <8: 0>	-	1	This chip does not support this instruction
3	ISTEP	I <7: 0>	-	1	**IAA + i-> IAA (-128 ≤ i ≤ 127)**
4	MOVI	I <7: 0>	-	1	I <7: 0> -> (A)
5	MOV	R <7: 0>, F Z, N		1	(R) -> (aims)
6	MOVA	R <7: 0>	-	1	(A) -> (R)
7	MOVAR	R <10: 0> -		1	(A) -> (R)
8	MOVRA	R <10: 0> -		1	(R) -> (A)

table 9-1 Register operation instruction table

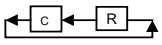
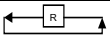
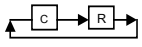
9.3 Program Control Instructions

No.	instruction		Affect the status of the machine cycle		operating
9	JUMP	I <7: 0>	-	2	PC + 1 + i <7: 0> -> PC (-128≤i≤127)
10	AJMP	I <19: 0>	-	2	I <9: 0> -> PC <9: 0> I <9: 8> -> PCRH <1: 0>
11	GOTO	I <10: 0>	-	2	I <9: 0> -> PC <9: 0>,
12	CALL	I <10: 0>	-	2	PC + 1-> TOS, I <9: 0> -> PC <9: 0>
13	LCALL	I <19: 0>	-	2	PC + 1-> TOS, I <9: 0> -> PC <9: 0> I <9: 8> -> PCRH <1: 0>
14	RCALL	R <7: 0>	-	2	**PC + 1 → TOS, (R) → PC <7: 0>, PCRH <1: 0> → PC <9: 8>,**
15	JBC	R <7: 0>, B <2: 0>	-	**2 or 1 when**	**R <B> = 0 When Skip**
16	JBS	R <7: 0>, B <2: 0>	-	**2 or 1 when**	**R <B> = 1 When Skip**

No.	instruction		Affect the status of the machine cycle		operating
17	JCAIE	I <7: 0>	-	2 or 1 when	(A) = I When Skip
18	JCAIG	I <7: 0>	-	2 or 1 when	(A)> I When Skip
19	JCAIL	I <7: 0>	-	2 or 1 when	(A) <I When Skip
20	JCRAE	R <7: 0>	-	2 or 1 when	(R) = (A) When Skip
twenty one	JCRAG R <7: 0>		-	2 or 1 when	(R)> (A) When Skip
twenty two	JCRAL	R <7: 0>	-	2 or 1 when	(R) <(A) When Skip
twenty three	JCCRE R <7: 0>,	B <2: 0>	-	2 or 1 when	C = R (B) When Skip
twenty four	JCCRG R <7: 0>,	B <2: 0>	-	2 or 1 when	C> R (B) When Skip
25	JCCRL	R <7: 0>, B <2: 0>	-	2 or 1 when	C <R (B) When Skip
26	JDEC	R <7: 0>, F	-	2 or 1	(R-1) -> (Destination), when the target register is 0 When the next instruction is skipped
27	JINC	R <7: 0>, F	-	2 or 1	(R + 1) -> (Destination), when the target register is 0 When the next instruction is skipped
28 NOP		-	-	1	No operation
29 POP		-	-	1	AS-> A, PSWS-> PSW, PCRHS-> PCRH
30 PUSH		-	-	1	A-> AS, PSW-> PSWS, PCRH-> PCRHS
31 RET		-	-	2	TOS-> PC
32 RETIA		I <7: 0>	-	2	I -> (A), TOS-> PC
33 RETIE		-	-	2	TOS-> PC, 1-> GIE
34 RST		-	All status bits are affected	1	Software reset command
35 CWDT		-	N_TO, N_PD	1	00 H-> WDT, 0-> WDT Prescaler, 1-> N_TO, 1-> N_PD
36	IDLE	-	N_TO, N_PD	1	00 H-> WDT, 0-> WDT Prescaler, 1-> N_TO, 0-> N_PD

table 9-2 Program control instructions table

9.4 Arithmetic / logic operation instructions

No.	instruction		Affect the status of the machine cycle		operating
37	ADD	R <7: 0>, F	C, DC, Z, OV, N	1	(R) + (A) -> (aims)
38	ADDC	R <7: 0>, F	C, DC, Z, OV, N	1	(R) + (A) + C -> (aims)
39	ADDCI	I <7: 0>	C, DC, Z, OV, N	1	I + (A) + C -> (A)
40	ADDI	I <7: 0>	C, DC, Z, OV, N	1	I + (A) -> (A)
41	AND	R <7: 0>, F	Z, N	1	(A) .AND (R) -.> (aims)
42	ANDI	I <7: 0>	Z, N	1	I.AND (A) -.> (A)
43	BCC	R <7: 0>, B <2: 0>	-	1	0-> R <B>
44	BSS	R <7: 0>, B <2: 0>	-	1	1-> R <B>
45	BTT	R <7: 0>, B <2: 0>	-	1	(~ R <B>) -> R <B>
46	CLR	R <7: 0>	Z	1	(R) = 0
47	SETR	R <7: 0>	-	1	FF_{H} -> (R)
48	NEG	R <7: 0>	C, DC, Z, OV, N	1	~ (R) + 1-> (R)
49	COM	R <7: 0>, F	Z, N	1	(~ R) -> (aims)
50	DAR	R <7: 0>, F	C	1	Correct(R) Decimal adjust -> (target)
51	DAA	-	C	1	Correct(A) Decimal adjust -> (A)
52	DEC	R <7: 0>, F	C, DC, Z, OV, N	1	(R-1) -> (aims)
53	INC	R <7: 0>, F	C, DC, Z, OV, N	1	(R + 1) -> (aims)
54	IOR	R <7: 0>, F	Z, N	1	(A) .OR (R) -.> (aims)
55	IORI	I <7: 0>	Z, N	1	I.OR. (A) -> (A)
56	RLB	R <7: 0>, F, B <2: 0> C, Z, N		1	 C << R <7: 0> (R band C Cyclic shift to the left)
57	RLBNC	R <7: 0>, F, B <2: 0> Z, N		1	 R <7> << R <7: 0> (R Without C Cyclic shift to the left)
58	RRB	R <7: 0>, F, B <2: 0> C, Z, N		1	 C >> R <7: 0> (R band C Right rotation)
59	RRBNC	R <7: 0>, F, B <2: 0> Z, N		1	 R <7: 0> >> R <0> (R Without C Right rotation)

No.	instruction	Affect the status of the machine cycle		operating
60 SUB	R <7: 0>, F	C, DC, Z, OV, N	1	(R) - (A) -> (aims)
61 SUBC	R <7: 0>, F	C, DC, Z, OV, N	1	(R) - (A) - (~ C) -> (aims)
62 SUBCI	I <7: 0>	C, DC, Z, OV, N	1	I- (A) - (~ C) -> (A)
63 SUBI	I <7: 0>	C, DC, Z, OV, N	1	I- (A) -> (A)
64 SSUB	R <7: 0>, F	C, DC, Z, OV, N	1	(A) - (R) -> (aims)
65 SSUBC	R <7: 0>, F	C, DC, Z, OV, N	1	(A) - (R) - (~ C) -> (aims)
66 SSUBCI	I <7: 0>	C, DC, Z, OV, N	1	(A) -I- (~ C) -> (A)
67 SSUBI	I <7: 0>	C, DC, Z, OV, N	1	(A) -I -> (A)
68 SWAP	R <7: 0>, F	-	1	R <3: 0> -> (Target) < 7: 4>, R <7: 4> -> (Target) < 3: 0>
69 TBR	-	-	2	Pmem (FRA) -> ROMD
70 TBR # 1	-	-	2	Pmem (FRA) -> ROMD, FRA + 1-> FRA
71 TBR_1	-	-	2	Pmem (FRA) -> ROMD, FRA-1-> FRA
72 TBR1 #	-	-	2	FRA + 1-> FRA, Pmem (FRA) -> ROMD
73 TBW	-	-	2	This chip does not support this instruction
74 TBW # 1	-	-	2	This chip does not support this instruction
75 TBW_1	-	-	2	This chip does not support this instruction
76 TBW1 #	-	-	2	This chip does not support this instruction
77 XOR	R <7: 0>, F	Z, N	1	(A) .XOR (R) -.> (aims)
78 XORI	I <7: 0>	Z, N	1	I.XOR (A) -.> (A)

table 9-3 Arithmetic / logic operation instruction list

Note: The instruction set

1 . i - immediate, F - flag A -register A , R -register R , B -register R First B Bit.

2 . C - Carry / borrow, DC - Digit carry / borrow from, Z - Zero flag, OV - overflow flag, N - Negative.

3 . TOS - Top stack.

4 . in case F = 0 , The destination is file register A ;in case F = 1 , The destination is file register R .

5 . 79 Otherwise an instruction NOP Instruction is not described in the above table.

6 . In some instructions, PC Bits and PCRU Register, depending on the actual chip set. for HW2171B , PC The median 11 Bit, no PCRU register.

The first 10 chapter MCU - Special Function Registers Summary Table

address	name	Function Description	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value at POR
FF80 H	IAD	Data register indirect addressing	IAD <7: 0>								0000 0000
FF81 H	IAAL	Low index register indirect addressing 8 Place	IAA <7: 0>								0000 0000
FF82 H	IAAH	High index register indirect addressing 8 Place	IAA <15: 8>								0000 0000
FF83 H	-	-	-								-
FF84 H	PSW	Program status word register	-	UF	OF	N	OV	Z	DC	C	x00x xxxx
FF85 H	AREG	A register	AREG <7: 0>								xxxx xxxx
FF86 H	IAPC	IAP Control register	IAPEN	-	-	-	-	-	IAPGO	-	0000 0000
FF87 H	FRAL	Program Memory look-up table address register low 8 Place	FRA <7: 0>								xxxx xxxx
FF88 H	FRAH	Program Memory look-up table address register high 8 Place	FRA <15: 8>								xxxx xxxx
FF89 H	ROMDL	Low program memory look-up table data register 8 Place	ROMD <7: 0>								xxxx xxxx
FF8A H	ROMDH	Program memory check	ROMD <15: 8>								xxxx

address	name	Function Description	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value at POR
		High data register, 8 Place									xxxx
FF8B H	PCRL	Program Counter Low 8 Place	PCR <7: 0>								0000 0000
FF8C H	PCRH	Program Counter High 3 Place	-	-	-	-	-	PCR <10: 8>			0000 0000
FF8D H	-	-	-								-
FF8E H	PA	PA Level of the port status register	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	xxxx xxxx
FF8F H	PAT	PA Input and output port control register	PAT7	PAT6	PAT5	PAT4	PAT3	PAT2	PAT1	PAT0	1111 1111
FF90 H	PB	PB Level of the port status register	-	-	PB5	PB4	PB3	PB2	PB1	PB0	00xx xxxx
FF91 H	PBT	PB Input and output port control register	-	-	PBT5	PBT4	PBT3	PBT2	PBT1	PBT0	0011 1111
FF92 H	-	-	-								-
FF93 H	-	-	-								-
FF94 H	N_PAD	PA Port weak pull-down control register	N_PAD7	N_PAD6	N_PAD5	N_PAD4	-	N_PAD2	N_PAD1	N_PAD0	1111 1111
FF95 H	N_PBD	PB Port weak pull-down control register	-	-	PLCS	N_PBD4	N_PBD3	N_PBD2	N_PBD1	N_PBD0	0011 1111
FF96 H	N_PAU	PA Weak pull control register	N_PAU7	N_PAU6	N_PAU5	N_PAU4	N_PAU3	N_PAU2	N_PAU1	N_PAU0	1111 0111
FF97 H	N_PBU	PB Weak pull control register	-	-	N_PBU5	N_PBU4	N_PBU3	N_PBU2	N_PBU1	N_PBU0	0011 1111

address	name	Function Description	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value at POR
FF98 H	-	-	-								-
FF99 H	-	-	-								-
FF9A H	-	-	-								-
FF9B H	PINTS	External Interrupt selection register	PINT3S <1: 0>		PINT2S <1: 0>		PINT1S <1: 0>		PINT0S <1: 0>		0000 0000
FF9C H	ANS	IO Digital to analog port selection register	PWM20NS	PWM10NS	ANPA7	ANPB1	ANPB0	ANPA2	ANPA1	ANPA0	0000 0000
FF9D H	INTF0	Interrupt Flag Register 0	T8P2PIF	T8P1PIF	ADIF	LVDIF	-	T8P2TIF	T8P1TIF	KIF	0000 0000
FF9E H	INTE0	Interrupt enable register 0	T8P2PIE	T8P1PIE	ADIE	LVDIE	-	T8P2TIE	T8P1TIE	KIE	0000 0000
FF9F H	INTC0	Interrupt Control Register 0	KMSK7	KMSK6	KMSK5	KMSK4	KMSK3	KMSK2	KMSK1	KMSK0	0000 0000
FFA0 H	INTG	The global interrupt register	GIE	-	-	-	-	-	SOFTIF	-	0000 0000
FFA1 H	LVDC	LVD Detection Register	LVDLS	-	-	LVDEN	-	-	LVDV <1: 0>		0001 0000
FFA2 H	INTF1	Interrupt Flag Register 1	-	-	-	-	PIF3	PIF2	PIF1	PIF0	0000 0000
FFA3 H	INTE1	Interrupt enable register 1	-	-	-	-	PIE3	PIE2	PIE1	PIE0	0000 0000
FFA4 H	INTC1	Interrupt Control Register 1	-	-	-	-	PEG3	PEG2	PEG1	PEG0	0000 0000
FFA5 H	OSCCAL	internal 16MHz Clock calibration register	OSCCAL <7: 0>								1010 1001

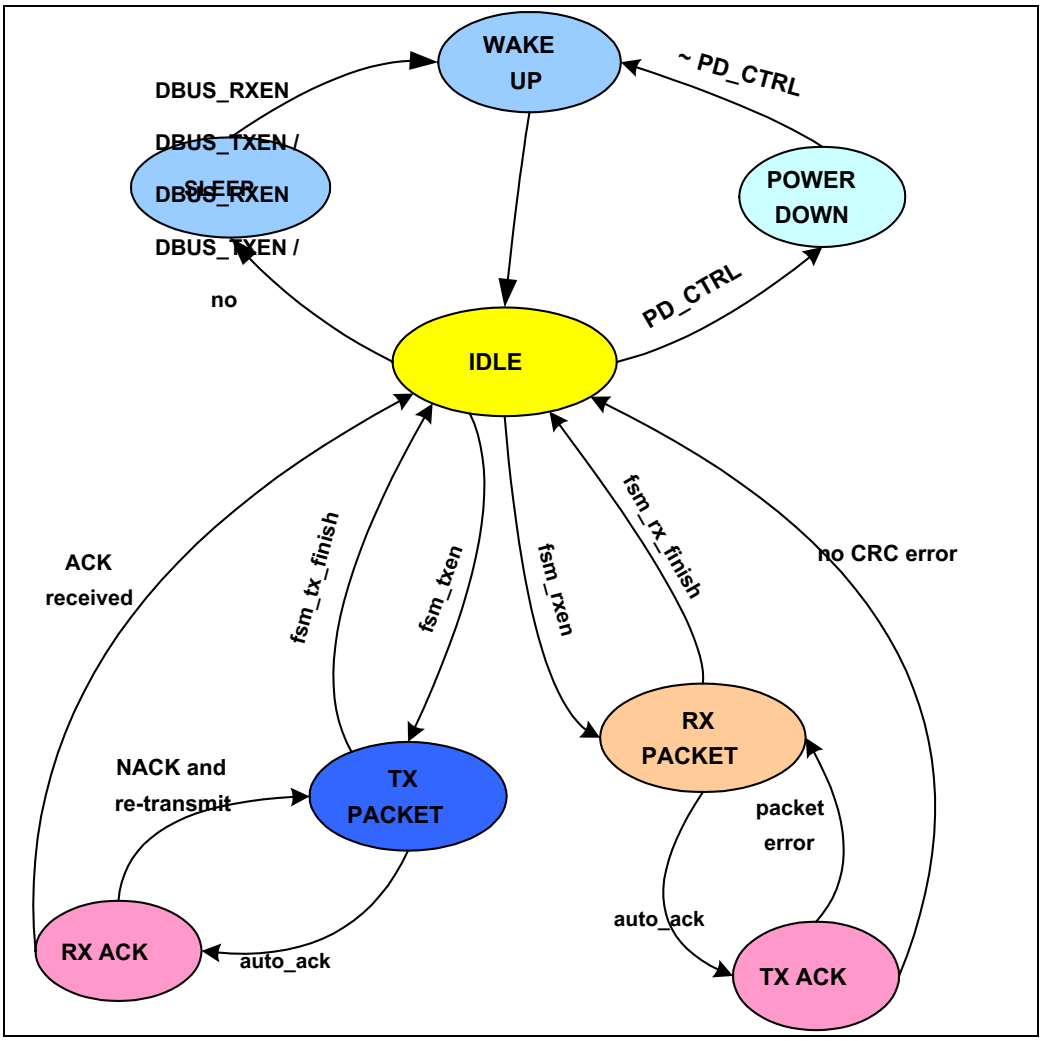
address	name	Function Description	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value at POR
FFA6H	WDTCAL	internal 32KHz Clock calibration register	WDTCAL <7: 0>								1000 0100
FFA7H	PWRC	Power Control Status Register	LPM	VRST <1: 0>		N_RSTI	N_TO	N_PD	N_POR	N_BOR	0101 110x
FFA8H	OSCC	Clock control register	CLKSS	FOSCS <2: 0>			-	WDTOSCF	HSOSCF	LPOSCF	0110 010x
FFA9H	WKDC	Wake-up delay control register	WKDC <7: 0>								1111 1111
FFAAH	OSCP	Clock Control Register write protection	OSCP <7: 0>								1111 1111
FFABH	WDTC	WDT Control register	WDTCKS	-	-	WDTPRE	WDTPRS <3: 0>				0001 0111
FFACH	PWEN	Power Control Register	-	SW_WDT	SW_HS	SW_LP	-	-	RCEN	-	0100 0011
FFADH	-	-	-								-
FFAEH	-	-	-								-
FFAFH	-	-	-								-
FFB0H	WDTP	WDT Cycle Match Count register	WDTP <7: 0>								1111 1111
FFB1H	-	-	-								-
FFB2H	T8P1	T8P1 counter	T8P1 <7: 0>								0000 0000
FFB3H	T8P1C	T8P1 Control register	T8P1M	T8P1POS <3: 0>				T8P1E	T8P1PRS <1: 0>		0000 0000
FFB4H	T8P1P	T8P1 Cycle Storage	T8P1P <7: 0>								1111

address	name	Function Description	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value at POR
		Device									1111
FFB5 H	T8P1R	T8P1 Precision registers	T8P1R <7: 0>								0000 0000
FFB6 H	T8P1PMC	T8P1 Cycle Match Control Registers	-	-	-	-	-	-	T8P1RS	T8P1PMS	0000 0000
FFB7 H	T8P1OC	T8P1 Output control register	T8P1TRN	T8P1REX	T8P1RE <1: 0>		T8P1NEN <1: 0>		T8P1PEN <1: 0>		0000 0000
FFB8 H	T8P2	T8P2 counter	T8P2 <7: 0>								0000 0000
FFB9 H	T8P2C	T8P2 Control register	T8P2M	T8P2POS <3: 0>				T8P2E	T8P2PRS <1: 0>		0000 0000
FFBA H	T8P2P	T8P2 Cycle register	T8P2PL <7: 0>								1111 1111
FFBB H	T8P2R	T8P2 Precision registers	T8P2RL <7: 0>								0000 0000
FFBC H	T8P2PMC	T8P2 Cycle Match Control Registers	-	-	-	-	-	-	T8P2RS	T8P2PMS	0000 0000
FFBD H	T8P2OC	T8P2 Output control register	T8P2TRN	T8P2REX	T8P2RE <1: 0>		T8P2NEN <1: 0>		T8P2PEN <1: 0>		0000 0000
FFBE H	T8P1PDT	T8P1 PWM Dead time control register	T8P1PDT <7: 0>								0000 0000
FFBF H	T8P2PDT	T8P2 PWM Dead time control register	T8P2PDT <7: 0>								0000 0000
FFC0 H	T8P1PEX	T8P1 After the division ratio of the extension register	-	-	-	-	T8P1POSEX <3: 0>				0000 0000

address	name	Function Description	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value at POR
FFC1 H	T8P2PEX	T8P2 After the division ratio of the extension register	-	-	-	-	T8P2POSEX <3: 0>				0000 0000
FFC2 H	-	-	-								-
FFC3 H	-	-	-								-
FFC4 H	-	-	-								-
FFC5 H	-	-	-								-
FFC6 H	ADCCL	ADC Control register	ADVREFS <2: 0>			ADCHS <2: 0>			ADTRG	ADEN	0000 0000
FFC7 H	ADCCH	ADC Control register	ADFM	ADCS <2: 0>			ADST <3: 0>				0000 1000
FFC8 H	ADCRL	ADC Conversion result register < 7: 0>	ADCRL <7: 0>								xxxx xxxx
FFC9 H	ADCRH	ADC Conversion result register < 15: 8>	ADCRH <7: 0>								xxxx xxxx
FFCA H	ADCTR	ADC Automatically trigger register	-	TRIGS	TRIGPEG	TRIGEN	-	-	-	AD2VCALS 0000	0000
FFCB H	-	-	-								-
FFCC H	-	-	-								-
FFCD H	-	-	-								-
FFCE H	-	-	-								-
FFCF H	CALPROT Send calibration values protection	Register	-	-	-	-	-	-	-	CALPROT0	0000 0001
FFD0 H ~ FFFF H	-	-	-								-

The first 11 chapter RF Transceiver - the operating mode control

RF Switching between operation mode transceiver control as shown below:



Map 11-1 RF A schematic view of the operating mode control Transceiver

11. 1 POWER DOWN mode

In this mode in addition to low-power digital LDO External power supply, all analog modules are closed and can read the register state maintained (but FIFO Inoperable, interrupt flag can not be cleared), RF The transceiver overall power consumption of about 1.5uA .

Setting register PD_CTRL (register MISC0 of Bit15) High can enter POWER DOWN Mode, if Set to low exit POWER DOWN Mode (pin CE The need to maintain a high level). RF Transceiver from POWER DOWN Mode Exit to enter IDLE Without the transceiver mode will be automatically entered in claim SLEEP mode.

11. 2 SLEEP mode

In this low-power mode, the digital LDO Crystal oscillator with power, but the crystal oscillator buffer is not enabled, no clock chip digital circuitry, and read and write registers should be saved (but FIFO Inoperable, interrupt flag can not be cleared), use

12MHz When the crystal oscillator, RF The transceiver overall power consumption of about 25uA .

when RF Transceiver The transceiver is not required to close DBUS_TXEN (register TRCTL of Bit8) / DBUS_RXEN (register TRCTL of Bit7 When) automatically from IDLE Mode entry SLEEP Mode, the transceiver is turned on when a request DBUS_TXEN / DBUS_RXEN , RF Transceiver from SLEEP Mode to recovery IDLE After entering the pattern TX / RX Operating mode.

11. 3 IDLE mode

In this mode number LDO Power supply is enabled in the normal mode, the crystal oscillator, crystal oscillator buffer circuit has a digital-chip system clock, but PLL And the transceiver circuit is not operating, using 12MHz When the crystal oscillator, RF The transceiver overall power consumption is less than 2mA .

RF After the transceiver from the transceiver to complete the automatic TX / RX Mode entry IDLE mode.

11. 4 TX mode

When enabled RF transceiver DBUS_TXEN And send FIFO After active, RF Transceiver enters TX mode. After completion of transmission, RF Transceiver enters IDLE Mode, turn off DBUS_TXEN Rear, RF Transceiver enters SLEEP mode.

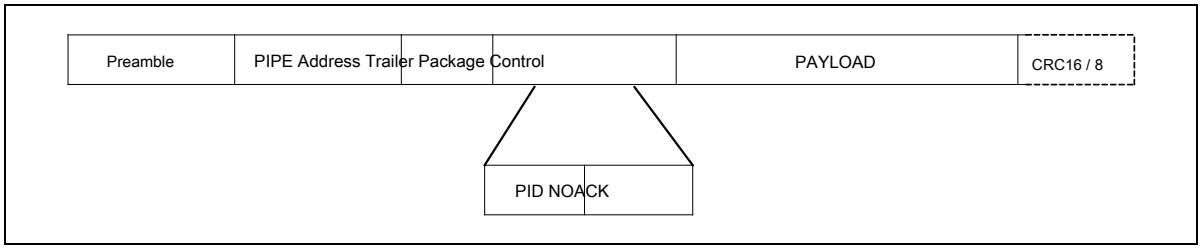
11. 5 RX mode

When enabled RF transceiver DBUS_RXEN And receiving FIFO After active, RF Transceiver enters RX mode. If the FIFO Upon receipt of state does not satisfy the conditions for the occupation, RF Transceiver enters IDLE Mode, turn off DBUS_RXEN Rear, RF Transceiver enters SLEEP mode.

Note: FIFO Is active finger FIFO Configuration Register FIFO0CTRL / FIFO1CTRL Filled in PIPE (PRX_FIFOn_PIPE) With the current Fee package PIPE And address match PRX_FIFOn_OCPY = '1' .

The first 12 chapter RF Transceivers - packet structure

12. 1 PTX Transmission packet structure



Map 12-1 PTX A schematic view of the transmission packet structure

- **Preamble**

  stand by 2,4,6 ... 16bytes, Length register by PREAMBLE_LEN (PKTCTRL Register

  Bit15-Bit13) Configuration.

- **PIPE Address (Syncword)**

  stand by 16/32 / 48bits, Length register by SYNCWORD_LEN (PKTCTRL Register

  Bit12-Bit11) Configuration. stand by 4 Way data channel, PIPE Address Register by 0x40 ~ 0x47 Configuration.

- **Trailer**

  stand by 4 ~ 18bits, Length is defined by TRAILER_LEN (PKTCTRL Register Bit10-Bit8) Configuration.

- **PID**

  PID Length of 2bits When the automatic transmission is generated by hardware.

  PTX Each time a new packet transmission PID Will automatically add '1' .

  PRX Received for the current PIPE Address, in accordance with PID versus CRC Determining the current value of the received packet as a new packet

  or a retransmission packet (retransmission packet is dropped).

  PTX If the retransmission timeout, the next re-transmission PID Not cumulative.

- **NOACK**

  This bit is used to indicate when ACK When the function is enabled, PTX inform PRX The current package do not need ACK The exceptional cases.

  able to pass PTX_FIFOn_NOACK (FIFOnCTRL Register Bit4) To be set.

- **PAYLOAD**

  Under hardware control link, each stage FIFO Maximum support 63bytes of PAYLOAD Non-fixed-length mode FIFO First byte representative PAYLOAD

  Length, fixed length mode PAYLOAD Length of the register FIX_PLD_LEN

  Configuration.

  Link under software control, PAYLOAD The length of the master MCU Chip decision.

- **CRC**

  Hardware link under control, to support CRC16 versus CRC8 Modes, by CRC_SEL (MISC1 Register Bit14) Configuration.

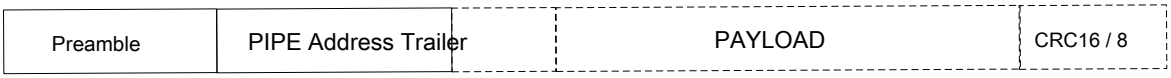
  CRC16 Generating polynomial: x ^ 16 + x ^ 12 + x ^ 5 + 1 CRC8 Generating

  polynomial: x ^ 8 + x ^ 2 + x + 1

Link does not support hardware under software control CRC Features.

12. 2 PRX send ACK Packet structure

PRX Sent ACK Packet structure diagram is shown below:



Map 12-2 PRX send ACK Packet structure diagram

If the ACK band ACK PAYLOAD Feature is not enabled, PRX Only return Preamble versus PIPE Address Two parts.

If the ACK band ACK PAYLOAD Function enabled, PRX return Preamble , PIPE Address , Trailer , PAYLOAD versus CRC .

Preamble , PIPE Address , Trailer , PAYLOAD versus CRC See the configuration 12.1 Festival PTX Transmission structure described in the packet.

The first 13 chapter RF Transceiver - Link Control mode

RF The transceiver supports communication link control hardware and software communication link control, through the register

PACK_LENGTH_EN (MISC1 Register Bit12) Configuration. Details transceiver processes and operations, please refer " AN1000_ Application Note_ HW2000B_User_Guide "Contents of the packet transceiver section.

13.1 Hardware link control

When set PACK_LENGTH_EN for '1' Time, RF The transceiver is in communication mode link control hardware. Hardware link control includes two modes of operation, a non-staple mode and the staple mode, by 0x31 Register FIX_PLD_LEN_EN Bits to configure, set ' 1 'Enable the fixed length mode, set to' 0 'Non-staple mode, the default mode of the non-fixed length.

Non-fixed-length mode support two transceivers FIFO Each grade FIFO Maximum support 63bytes PAYLOAD And has PAYLOAD Automatic hardware CRC Check function. stand by ACK Features, ACK Whether with package ACK PAYLOAD Function can be equipped.

Non-fixed-length filled under FIFO First byte On behalf of the class FIFO middle PAYLOAD The length (must be greater than 0) , PRX May be charged according to the store PAYLOAD of FIFO The first byte Determining a desired value read PAYLOAD length.

Fixed-length mode supports two transceivers FIFO Each grade FIFO Maximum support 63bytes PAYLOAD ,not support ACK and ACKPAYLOAD Features. The fixed length mode PAYLOAD Length register by FIX_PLD_LEN Register configuration.

13.2 Software Link Control mode

When set PACK_LENGTH_EN for '0' Time, RF Software in the transceiver mode communication link control.

This mode only supports FIFO0 One FIFO ,not support ACK And hardware CRC Check function.

Software Link mode is suitable for longer needs to be sent PAYLOAD Length (> 63 bytes) The occasion, the master MCU Chip based on need FIFO The half-empty and half-full mark with the transceiver process.

By configuring FW_HW_TERM_EN Control bit (MISC1 Register Bit11), You can select different PTX Stop sending condition:

FW_HW_TERM_EN = '1' Time, FIFO0 The read and write pointers same state machine automatically stops sending data;

FW_HW_TERM_EN = '0' Time, PTX Send cycle FIFO0 Internal data, the main control MCU Chip Close DBUS_TXEN To determine when to stop sending data, the test mode is convenient for PTX Performance in continuous transmission mode.

The first 14 chapter RF Transceivers - and more PIPE Logical Channel

RF Transceiver supports 4 Data PIPE Logical channel, i.e., PIPE0 ~ PIPE3 Each PIPE It has its own physical address, default PIPE0 / PIPE1 Enable. each PIPE See address configuration register 0x40 ~ 0x47 description. each PIPE Enable, ACK

Function ACK band PAYLOAD See feature enable PIPECTRL Register description.

To use PIPE0 Logical channel communications, for example, PIPECTRL Register is configured as follows:

- If Enable ACK Features

  P0_EN = '1' ; P0_ACK_EN = '0' ; P0_ACKPAYLOAD_EN = '0' .

- If enabled ACK Without PAYLOAD Features

  P0_EN = '1' ; P0_ACK_EN = '1' ; P0_ACKPAYLOAD_EN = '0' .

- If enabled ACK band PAYLOAD Features

  P0_EN = '1' ; P0_ACK_EN = '1' ; P0_ACKPAYLOAD_EN = '1' .

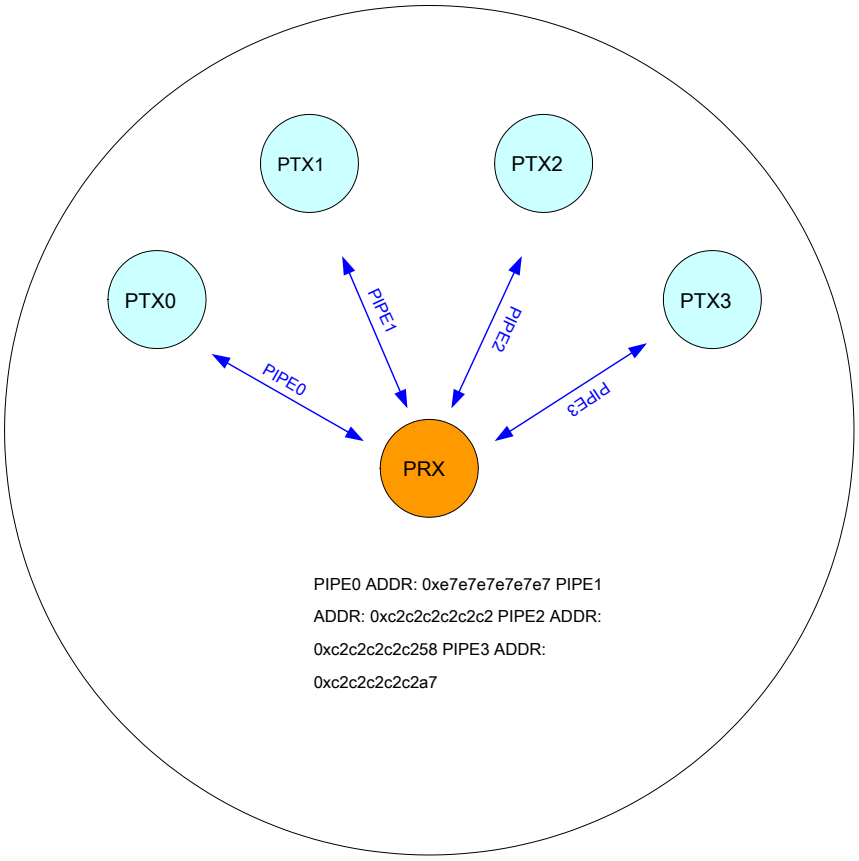
PRX Support and 4 Different PIPE Address PTX communication. To ensure that PRX You can reply to ACK To correct PTX ,

PRX After receiving the data packet received is saved PIPE Address and Reply ACK When used as PIPE sending address.

Map 14-1 Shows 4 road PIPE Communication diagram 4 road PIPE They have independent PIPE address. PRX Sharing may be different PIPE Related communications, but in the way PIPE Before a full send and receive process is complete, PRX Not the other way PIPE

Address PTX communication. When the multi-channel PTX versus 1 road PRX When communication, set each PTX of AUTO_RX_ACK_TIME

Register value (MISC2 Register Bit7-Bit0) Can effectively prevent the various PIPE Interference between.



Map 14-14 road PIPE Communication schematic

The first 15 chapter RF Transceiver - Automatic Response ACK And automatic retransmission ART

15. 1 ACK Without ACK PAYLOAD

- when PTX versus PRX While enabling the current communication PIPE of ACK After the function (PIPECTRL Register Pn_EN = '1' and Pn_ACK_EN = '1'), PRX Receiving CRC After the completion of the RX Mode is automatically TX Send mode ACK package, PTX In sending CRC After the completion of the TX Mode is automatically RX Mode waiting to receive ACK
  package. PTX Receiving ACK carry out, PRX In sending ACK After completion of the set their respective FIFO The interrupt flag bit (see Figure 16-3).

- PTX If the AUTO_RX_ACK_TIME Not successfully received within the time PRX Sent ACK signal,
  PTX It will automatically retransmit the packet. As the number of retransmissions exceeds the preset number of times RE_TX_TIMES plus 1 (MISC0 Register Bit11-Bit8), INT Register INTn And interrupt flag FIFO Send indication bit PTX_FIFOn_FAIL (FIFOnCTRL Register Bit15) Are both set '1' Indicating transmission failure (see FIG. 16-4 To 16-6).

- PRX Receiving CRC Upon completion If there CRC Error will not switch RX Waiting for the automatic re-entry mode (see FIG. 16-7).

in ACK When the function is enabled by configuring PTX_FIFOn_NOACK Control bits may inform PRX Do not automatically send the current packet ACK .

15. 2 ACK band ACK PAYLOAD

- when PTX versus PRX While enabling the current communication PIPE of ACK band ACK PAYLOAD After the function (Pn_EN = '1' , Pn_ACK_EN = '1' and Pn_ACKPAYLOAD_EN = '1'), PRX In sending ACK The process conditions are automatically satisfied from ACK FIFO Remove the ACK PAYLOAD Sending. ACK FIFO First
  byte representative ACK PAYLOAD Length must be greater than the value of fill 0 . PTX Upon receipt ACK PAYLOAD After data into the meet the conditions ACK FIFO In from the juxtaposed ACK FIFO Respective status indication bit (INT Register ACKINTn , FIFOn_ACK_POS with ACKINTn_W_ACKPAY , ACKFIFOnCTRL Register PTX_ACKFIFOn_PIPE). ACK FIFO Operating procedures and DATA FIFO Basically the same process.

- If the PRX Not meet the conditions ACK FIFO In sending ACK Automatically sent when the packet ignored ACK PAYLOAD
  versus CRC Link, PTX Receiving ACK It detects packet length is 0 of ACK PAYLOAD And automatically ignore reception CRC Link.

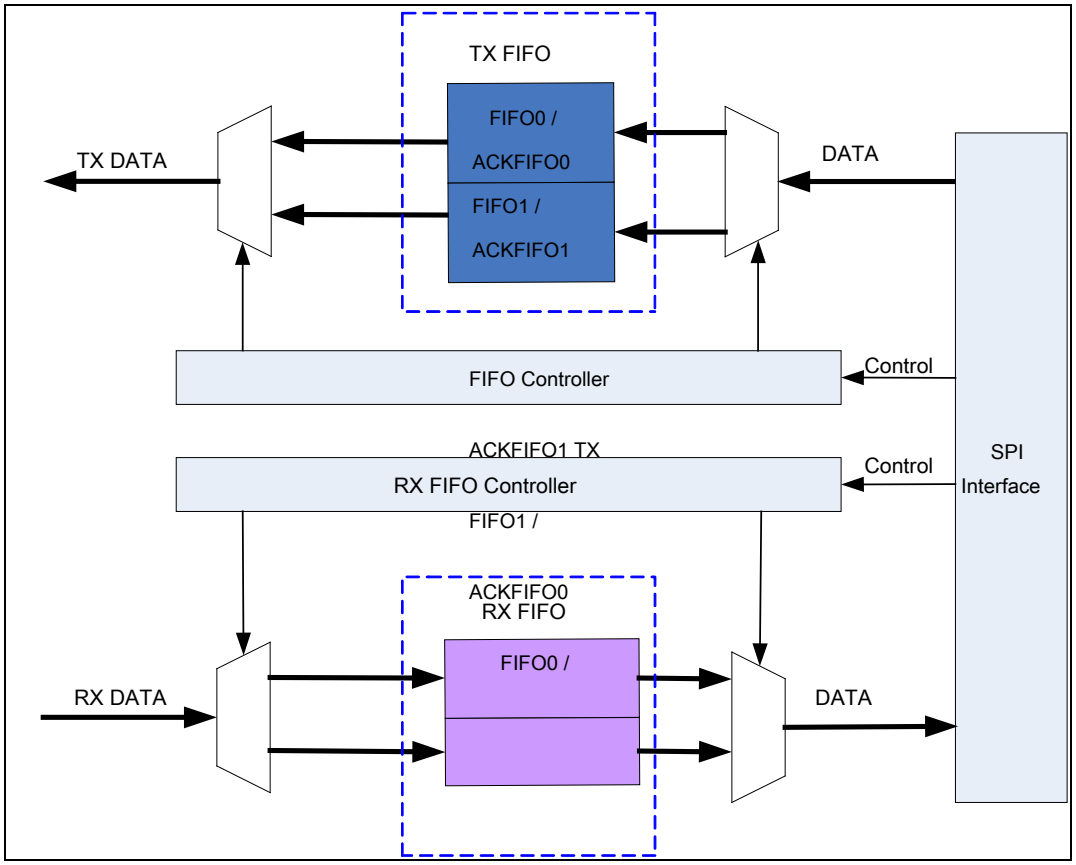
- PTX If the detected charge ACK PAYLOAD Have CRC Error by RX Transfer mode TX Retransmission mode. As the number of retransmissions exceeds the preset number of times RE_TX_TIMES + 1 , PTX_FIFOn_FAIL Will set '1' It failed to send instructions.

Note: to meet the conditions ACK FIFO Finger ACK FIFO Configuration Register ACKFIFO0CTRL / ACKFIFO1CTRL Filled in PIPE (PRX_ACKFIFOn_PIPE) , Charged with the current package PIPE And address match PRX_ACKFIFOn_OCPY = '1' .

The first 16 chapter RF Transceivers - Data and control interface

16. 1 FIFO

RF Transceiver supports two DATA FIFO (Each level 64bytes) And two ACK FIFO (Each level 32bytes) . DATA FIFO For storing transceiving PAYLOAD Data, its access address 0x32 versus 0x33 , ACK FIFO For storing transceiving ACK PAYLOAD Data, its access address 0x34 versus 0x35 .



Map 16-1 FIFO Control schematic

for PTX In sending PAYLOAD Ago by SPI to DATA FIFO Fill in the data transmission process DATA FIFO Read permission to cross the internal state machine, during a transmission prohibition SPI Interface Read DATA FIFO operating;

for PRX In reception PAYLOAD Process DATA FIFO The cross-write access to the internal state machine, is prohibited in the process SPI Write Interface DATA FIFO operating.

Similarly, if enabled ACK band PAYLOAD Function for PRX ,in ACK PAYLOAD Before sending through SPI to ACK FIFO Fill in the data transmission process ACK FIFO Read permission to cross the internal state machine, during a transmission prohibition SPI Interface Read ACK FIFO operating;

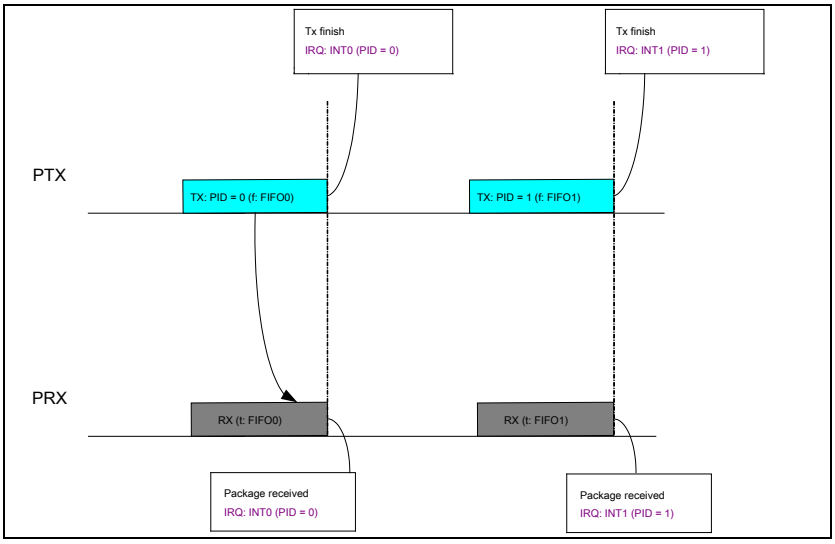
for PTX In reception ACK PAYLOAD Process ACK FIFO The cross-write access to the internal state machine, is prohibited in the process SPI Write Interface ACK FIFO operating.

16.2 Interrupt

16. 2.1 Link control hardware interrupts

- **ACK Not to interrupt**

in ACK Can not make the next case, PTX After the completion of the transmission to set their respective transmit FIFO Interrupt flag INTn ,same PRX Upon receiving the reception completion to set their respective FIFO Interrupt flag (Figure 16-2 Shown).

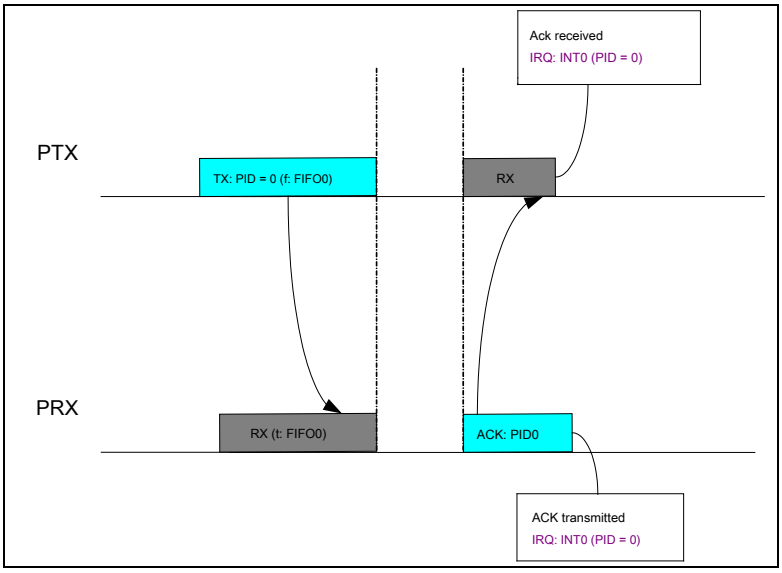


Map 16-2 ACK Not enable interruption schematic

- **ACK Enable without ACK PAYLOAD Interrupt**

in ACK Enable without ACK PAYLOAD Case, if PTX Send from FIFOn of PAYLOAD In reception ACK After the success of the corresponding interrupt flag INTn Will set '1' .

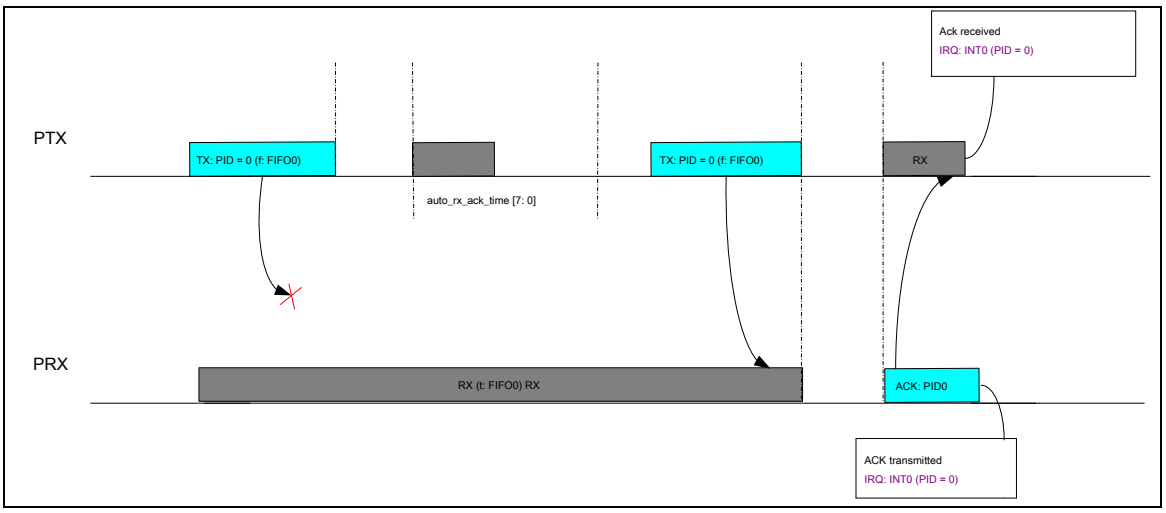
If the PRX After successful reception PAYLOAD Fill FIFOn , PRX In return ACK The corresponding interrupt flag after completion INTn Will set '1' . (Figure 16-3 Shown).



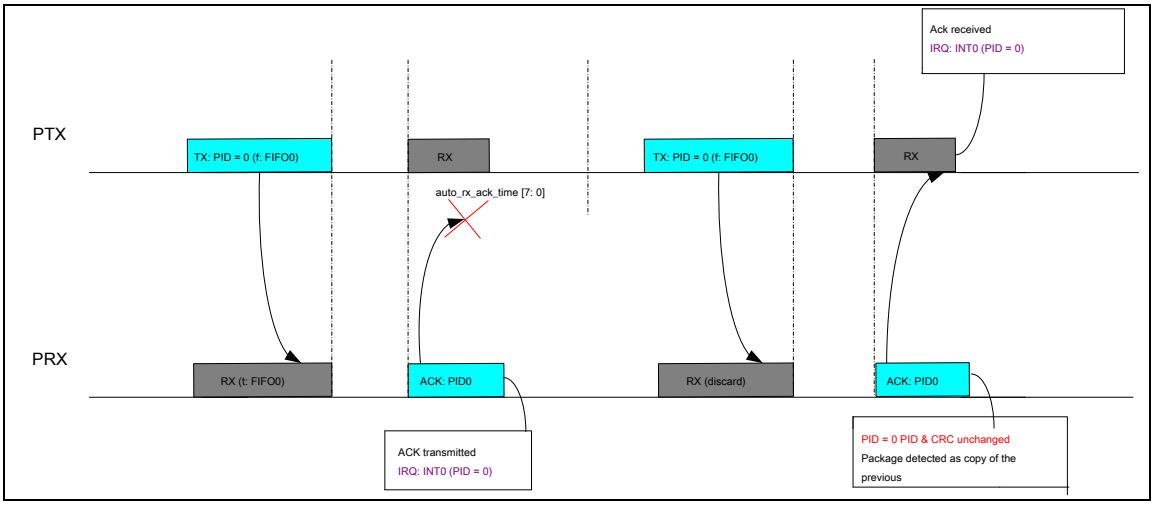
Map 16-3 ACK Enable without ACK PAYLOAD Interrupt schematic

Map 16-4 To 16-6 Shown as a transceiver unsuccessful possible scenarios, PTX After switching to receive a transmission completion ACK State, if the wait ACK in time(AUTO_RX_ACK_TIME) Did not receive effective ACK Signal, switches back automatic retransmission.

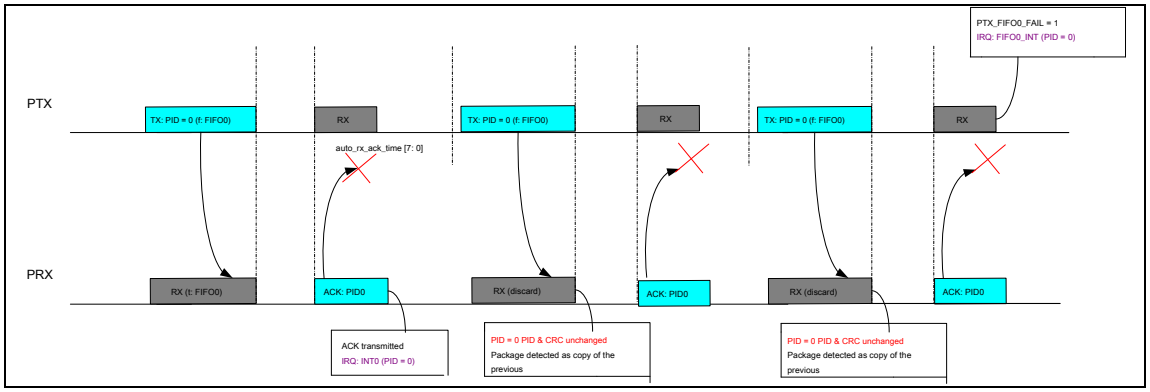
PRX After receiving the success will judge charged PID If charged PID versus CRC The same as the previous one, will be treated as re-entry package, not a break (only return ACK).



Map 16-4 PTX Automatic retransmission situation 1 Interrupt schematic

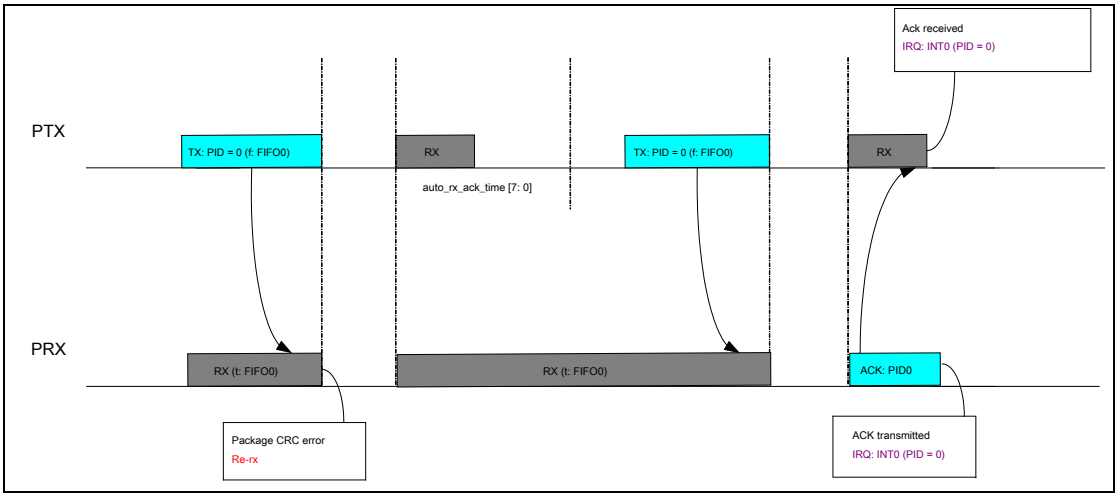


Map 16-5 PTX Automatic retransmission situation 2 Interrupt schematic



Map 16-6 PTX Automatic retransmission situation 3 Interrupt schematic (retransmission timeout, the number of retransmissions of 2)

Note 1 : Automatic retransmission is set RE_TX_TIMES Must be greater than '1' . Note 2 : If PTX in RE_TX_TIMES The number is not received ACK , PTX In the home from break INTn Meanwhile PTX_FIFOn_FAIL Will set '1' . Note 3 : If PTX Retransmission timeout, when sending the next packet PID Compared with the previous remains unchanged. Note 4 : Re-entry feature is only discarded packets ACK The situation can lower effective.



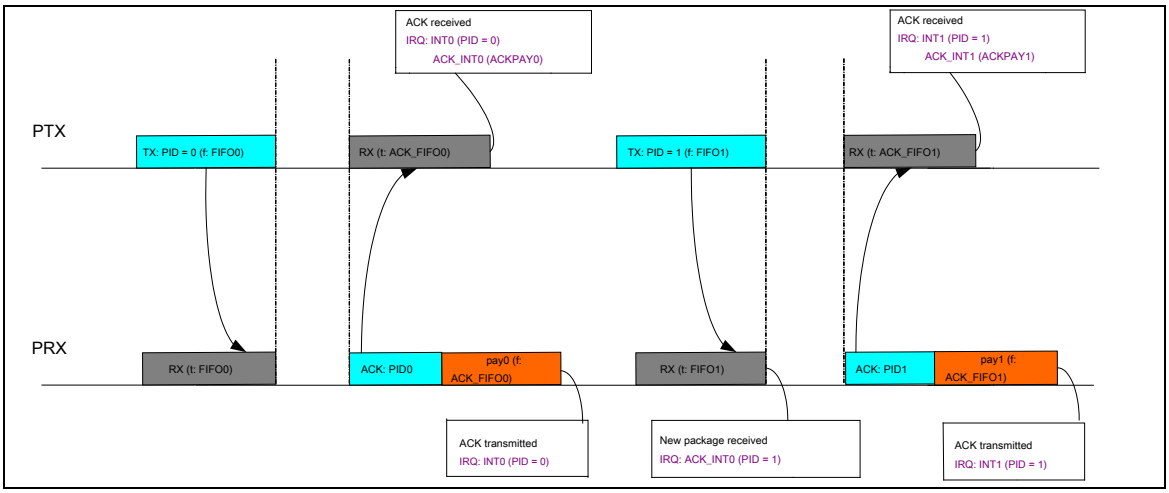
Map 16-7 PRX Automatic Re-entry interrupt schematic

Map 16-7 Shows PRX In the case of automatic re-closing, PRX After receiving the data packet if it is detected CRC There are not mistakenly return ACK It switched to the automatic re-entry until it receives the correct data packets and returns ACK After starting the interrupt flag is set. PTX in AUTO_RX_ACK_TIME Can not receive effective time ACK The automatic retransmission.

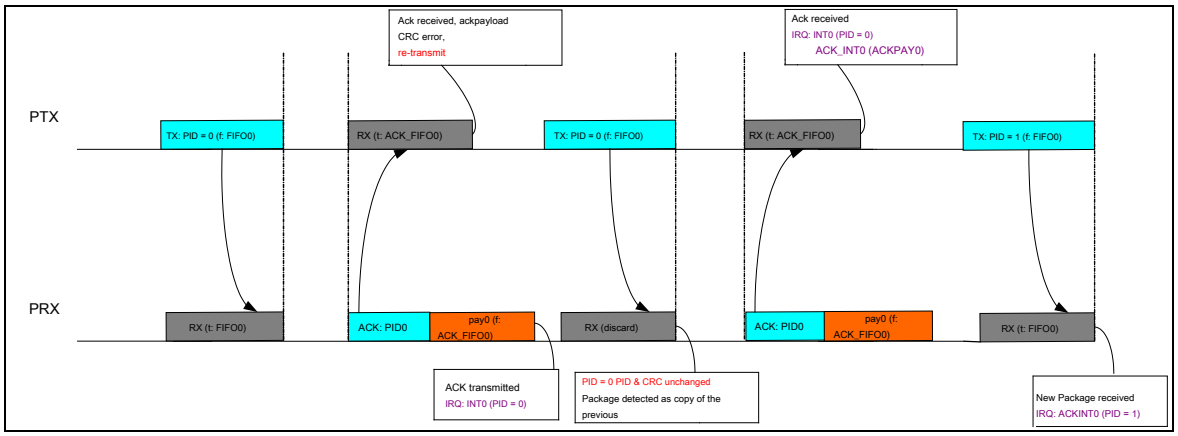
- **ACK The band ACK PAYLOAD Interrupt**

  in ACK band ACK PAYLOAD Case, if PTX From FIFOn Sent PAYLOAD After a successful reception ACK PAYLOAD After fill ACK_FIFOn , The corresponding interrupt flag INTn versus ACK_INTn Will set '1' .

  If the PRX From ACKFIFOn Return ACK PAYLOAD After the next time you receive a new package (the same PIPE PID Changes), the corresponding interrupt flag ACK_INTn Will set '1' (Figure 16-8 Shown).

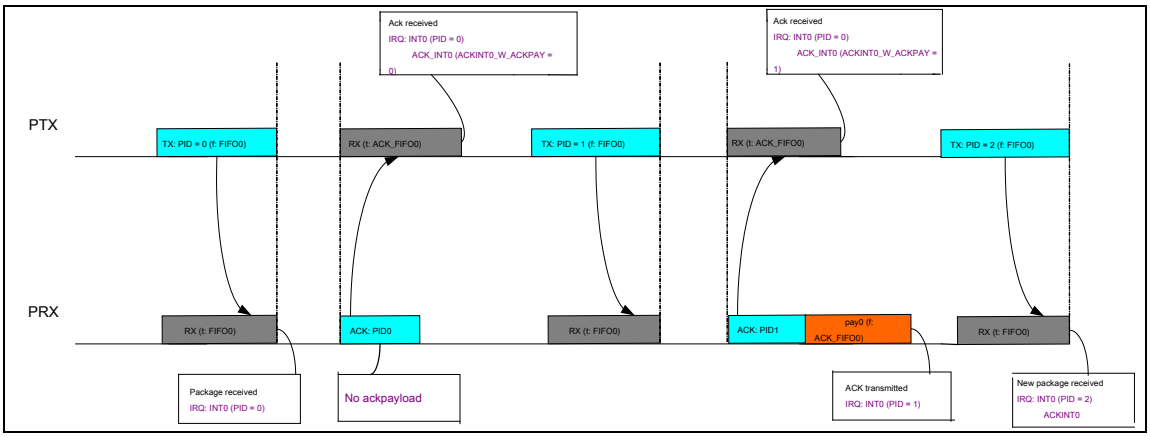


Map 16-8 ACK band ACK PAYLOAD Interruption schematic



Map 16-9 PTX receive ACK CRC ERROR Interruption schematic

PTX received ACK PAYLOAD If detected after CRC Error, retransmission, did not mention since interrupt (Figure 16-9 Shown).



Map 16-10 PRX No satisfy the conditions ACK PAYLOAD Send interruption schematic

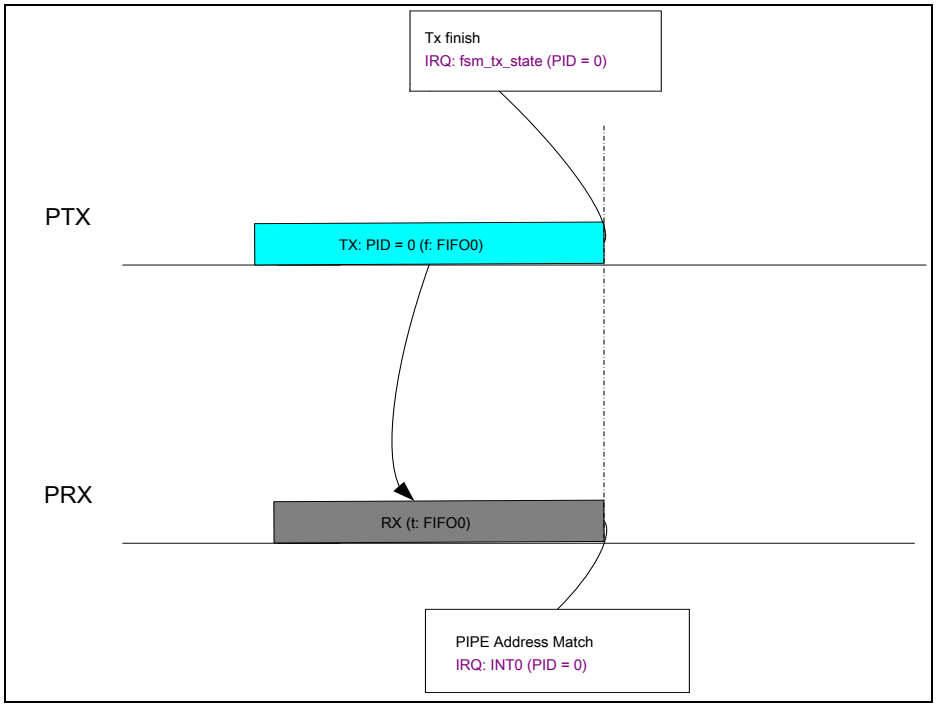
PRX If not meet the conditions ACK FIFO Ignored Send ACK PAYLOAD , PTX Detecting the length of 0 of ACK PAYLOAD , From home ACK_INT0 (Assuming that ACK FIFO0 Meet the receiving state) while the

ACKINT0_W_ACKPAY State position '0' Indicating that the interruption no ACK PAYLOAD . PRX Even if the next received PID Changes nor to set their ACKINT0 Interrupt (Figure 16-10 Shown).

16. 2.2 Link Control software interrupt

Under software control of link PTX of IRQ Pin indicates the transmit mode, after the completion of IRQ Level flip.

PRX It can be received in the associated PIPE Address Post interrupt flag INTn , Can be cleared by the interrupt flag or register SPI Read reception FIFOn Automatic Clearing corresponding interrupt INTn (Figure 16-11 Shown).

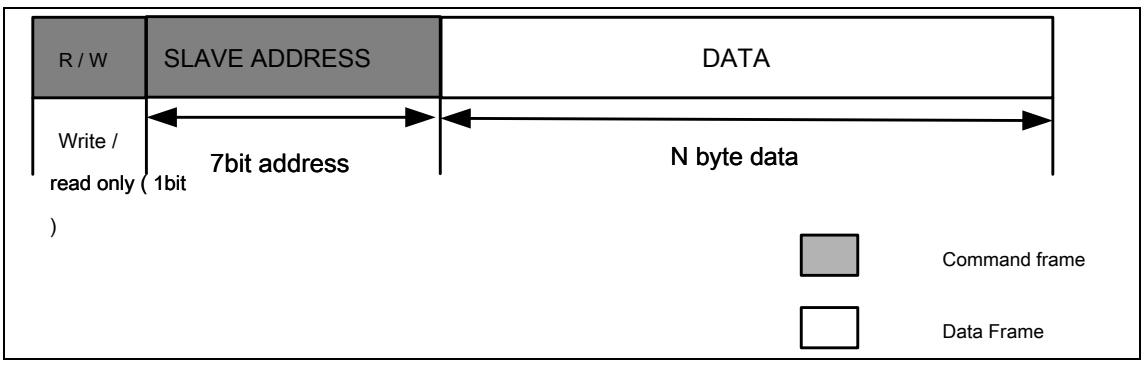


Map 16-11 Illustration software interrupt link control

16. 3 SPI Communication Interface

RF Transceiver supports 4 line SPI Communication interface, support SLEEP Mode register read and write operations support FIFO Tonal ligatures.

16. 3. 1 SPI Frame format



Map 16-12 SPI Frame format

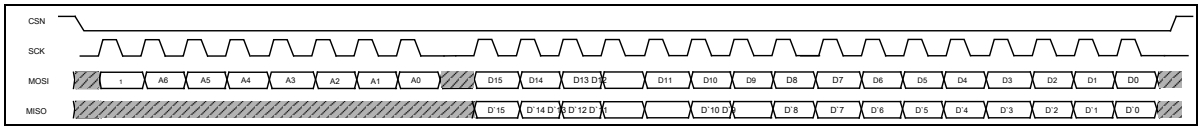
among them 8bit Write command frame to the first control bit, '0' Read-only operation, '1' For the read and write operations (to read a register value can be written simultaneously value), after 7 Bit read and write address bits.

SPI According to the data frame SPI Different differ interface to access the object, if SPI Access to internal registers of the data frame is fixed 2bytes ,in case SPI access FIFO (Register Address: 0x32 , 0x33 , 0x34 , 0x35), In the case of non-tonal ligatures 1byte (internal FIFO Data width), the data read through the length of the lower case cursive access length is determined by the master device.

Data format is high (MSB) First, low (LSB)is behind.

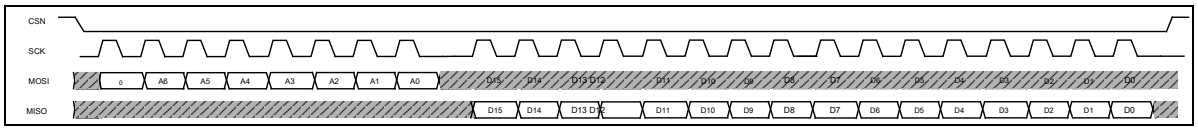
16. 3.2 Register Access Timing

SPI Interface register read and write operation timing in FIG. 16-13 FIG. 16-14 Fig.



Map 16-13 SPI Write register Timing

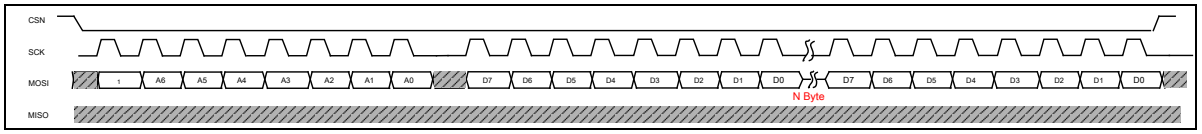
Note: When you write register MISO Sent D'x The access register to the original value.



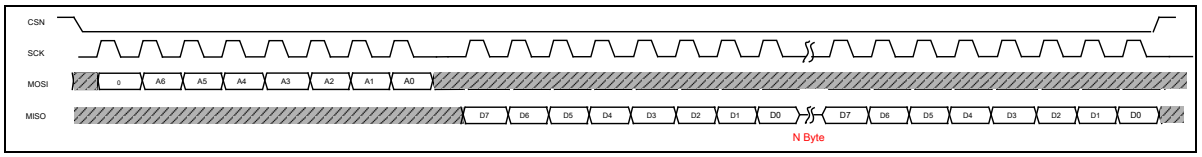
Map 16-14 SPI Read register Timing

16. 3. 3 FIFO Access Timing

FIFO Support continuous read and write operations, the minimum unit of 1byte , SPI Interface to read and write FIFO Operation timing in FIG. 16-15 FIG. 16-16 Fig.

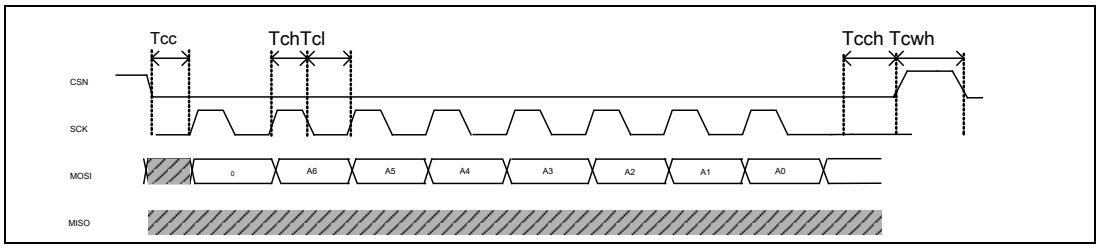


Map 16-15 SPI write FIFO Timing



Map 16-16 SPI read FIFO Timing

16. 3. 4 SPI Timing Parameters



Map 16-17 SPI Diagram of timing parameters

Symbol	Parameter	Min.	Units
Tcc	CSN to SCK setup time	20	ns
Tch	SCK high time	62.5	ns
Tcl	SCK low time	62.5	ns
Tcch	SCK to CSN hold time	40	ns
Tcwh	CSN inactive time	125	ns

table 16-1 SPI Timing Parameters

The first 17 chapter RF Transceiver - Other functions provided

17. 1 RF Transceiver Reset

RF The transceiver provides a total of three reset sources, respectively, the power POR Reset chip select pin CE Reset SFT_RST Software reset.

Power-on POR Reset chip select pin CE Reset to full-chip reset, software reset only resets the status signal of each chip, while maintaining the internal register.

It should be noted that, due to MCU Reset wake-up time than RF Reset Wake-up time is short, so, MCU The need for proper wake-up delay after reset, and then the RF Transceivers SPI operating.

17.2 Frequency settings

When data transceiver, sending and receiving ends frequency must be the same. Frequency range may be used are 2402MHz ~ 2483MHz , Frequency interval 1MHz A total of 82 Available frequency. Frequency channel number register by PLL_CH_NO Set frequency is finally transmitted or received RF_FREQ_BASE + PLL_CH_NO (MHz) .

Note: The complete frequency point provided before enabling sending or receiving.

17.3 Automatic offset correction (AFC)

Across the wireless transceiver, due to the factors of the crystal, work environment, such that the frequency of sending and receiving ends there will be some deviation. RF The transceiver provides automatic offset correction function when data is received (AFC),register AFC_MCTRL (MISC2 Register Bit14)for AFC Functions enable control bit.

17.4 Software offset correction

In addition to providing the hardware itself AFC Features, RF Providing the transceiver back to the frequency offset correction software interface.

register RF_FREQ_FRACTION (FOCCFG Register Bit11-Bit0) Used to complete frequency offset compensation value, calculated the particular register set as follows:

RF_FREQ_FRACTION = round (f_{dev} / 10^6 * 2048) , Frequency compensation accuracy of about 250Hz . among them f_{dev} = Target frequency - the actual frequency (Hz)

For the receiving end, RF The transceiver provides an indication hardware evaluation of the frequency offset register FREQ_ESTIMATION (STATUS0 Register Bit9-Bit0 , Twos complement), the data register and the actual frequency offset f_{dev} The correspondence is as follows:

when 250kbps Data rate: f_{dev} = FREQ_ESTIMATION / 1024 * 10^6 (Hz)

when 1Mbps Data rate: fdev = FREQ_ESTIMATION / 256 * 106 (Hz)

The user may indicate a frequency offset based on the register FREQ_ESTIMATION The estimated value f_{dev} , Complete offset compensation register RF_FREQ_FRACTION Configuration.

17.5 The preamble instructions

Data packets " 0101 "As the leader sequence of the entire packet, RF The transceiver can be continuously detected by the received " 01 "Number of data packets indicated as a leader sequence specific needs detected" 01 "Number of data registers can be provided PREAMBLE_NUM (FOCCFG Register Bit15-Bit12)determine. in case RF The transceiver detects a valid preamble sequence, the register PQT (STATUS0 register Bit11) Indicates a high level.

17. 6 RSSI Features

In the receive mode, the chip evaluation signal energy received at the antenna size will be, it will be the value stored in the register RSSI in. RSSI The unit is reading dBm Format data into twos complement signed number. Recommended latched read data packet received after completion RSSI The values latched RSSI register PKG_RSSI It is reserved on a data packet RSSI value. If the reading environment RSSI Value, after receiving the required enabled, a few milliseconds after read delay RSSI register.

RSSI Corresponding relationship between the input power value described in "Application Note _ HW2000B_User_Guide " RSSI Content section.

17.7 Carrier detect indication (Carrier Detect) Features

RF The transceiver supports carrier detection, i.e., when in receive mode, RF Received signal energy in the band transceiver monitors, when the received signal energy is greater than the set threshold, and maintain a certain time (> 8us) Rear, RF The transceiver will be given carrier detect indication signal.

Carrier energy threshold indicated by CDTH Register setting, when the input signal exceeds the energy CD_TH1 Setting and maintaining more than 8us After the carrier sense indication bit CD It will be set high, if the signal energy is reduced and less than CD_TH2 Setting the carrier sense indication bit is reset immediately.

CD_TH1 with CD_TH2 When set to specific units dBm Data format symbols twos complement form.

CD_TH1 versus CD_TH2 Setting method:

1 . Reads the reception sensitivity point RSSI Register value;

2 . CD_TH1 It is provided RSSI - 2dBm ;

3 . CD_TH2 It is provided RSSI - 5dBm . Recommended "Application Notes _ HW2000B_User_Guide "Register is initialized to a given set chapters CD Threshold.

17. 8 FEC , CRC , SCRAMBLE Features

RF The transceiver supports data automatically FEC Error Correction Code, rate R for 2/3 . use FEC Can correct transmission errors in transmission, the transmission system can improve the success rate in low SNR environment, but FEC Redundant data increases, the data packet transfer time increases.

Through configuration register FEC_TYPE (PKTCTRL register Bit5-Bit4)Enable FEC .

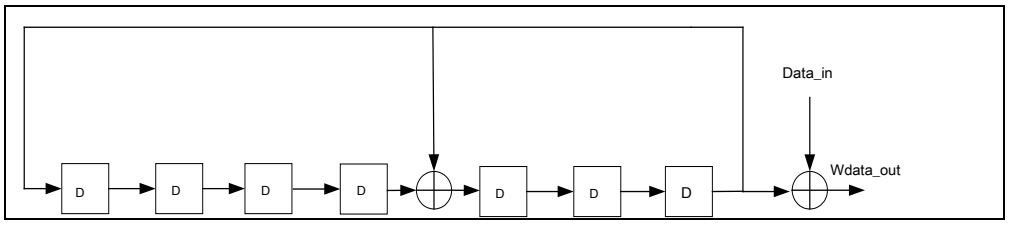
In hardware link control mode CRC Algorithm implemented in hardware, CRC The initial value of the shift register by register CRC_INIT_DATA (MISC1 register Bit7-Bit0) Setting.

stand by CRC16 versus CRC8 Modes, by CRC_SEL Configuration.

CRC16 Generating polynomial: $x^{16} + x^{12} + x^5 + 1$ CRC8 Generating polynomial: $x^8 + x^2 + x + 1$ RF The transceiver supports data scrambling function, in order to enhance long '0' Or long '1' Type of data transmission capability. Can register

SCRAMBLE_ON (MISC1 register Bit13) Open scrambling function, the scrambler seed can register SCRAMBLE_DATA (MISC0 register Bit6-Bit0) Setting.

Scrambling region PAYLOAD-CRC . The basic data stream:



Map 17-1 Data scrambler generator

The first 18 chapter RF Transceivers - Register

18.1 Register List

Register list below, it is marked in purple HW2171B With respect HW2171 The latest addition, three registers.

address	Register Name	Function Description	Reset value
0x20	**PKTCTRL**	Packet Configuration Register	0x5000
0x21	**TRCTL**	Transmission and reception enable register	0x0000
0x22	**CHANNR**	Channel Setting register	0x1830
0x23	**MISC0**	Configuration Register 0	0x0300
0x24	**FOCCFG**	Frequency offset compensation register	0x4000
0x25	**FREQBASE**	Starting frequency setting register	0x0962
0x26	**DS_PE**	**Pull current drive and Enable Control Register**	**0x000F**
0x28	**THRES**	Threshold value setting register	0x2103
0x29	**MISC1**	Configuration Register 1	0x1800
0x2A	**MISC2**	Configuration Register 2	0xC07E
0x2B	**PKG_RSSI**	**Received packet signal energy indication register**	**-**
0x2C	**CDTH**	CD Threshold value setting register	0x8883
0x2D	**RSSI**	Received signal energy indication register	-
0x2E	**STATUS0**	Status Register 0	-
0x30	**STATUS1**	Status Register 1	-
0x31	**FIX_LEN_EN**	**Transceiver fixed length control register**	**0x0F01**
0x32	**FIFO0DATA**	FIFO0 Access Register	-
0x33	**FIFO1DATA**	FIFO1 Access Register	-
0x34	**ACKFIFO0DATA**	ACKFIFO0 Access Register	-
0x35	**ACKFIFO1DATA**	ACKFIFO1 Access Register	-
0x36	**FIFO0CTRL**	FIFO0 Configuration Register	0x008E
0x37	**FIFO1CTRL**	FIFO1 Configuration Register	0x008E
0x38	**ACKFIFO0CTRL**	ACKFIFO0 Configuration Register	0x0E80
0x39	**ACKFIFO1CTRL**	ACKFIFO1 Configuration Register	0x0E80
0x3A	**FIFOSTATUS**	FIFO Status Register	-
0x3B	**CLEAR**	FIFO Pointer register	-
0x3C	**PIPECTRL**	PIPE Setting register	0x3000
0x3D	**INT**	Interrupt Register	-
0x40	**P0ADDR0**	PIPE0 Address Low 16bits	0xE7E7
0x41	**P0ADDR1**	PIPE0 Intermediate address 16bits	0xE7E7
0x42	**P0ADDR2**	PIPE0 Address High 16bits	0xE7E7
0x43	**P1ADDR0**	PIPE1 Address Low 16bits	0xC2C2
0x44	**P1ADDR1**	PIPE1 Intermediate address 16bits	0xC2C2
0x45	**P1ADDR2**	PIPE1 Address High 16bits	0xC2C2
0x46	**P2ADDR**	PIPE2 Address Low 8bits	0xxx58
0x47	**P3ADDR**	PIPE3 Address Low 8bits	0xxxA7

table 18-1 Register List

18.2 Register Description

register	Packet Configuration Register PKTCTRL				
address	0x20				
Reset value	0x5000				
Bit Name	Place	Read and write	Bit Description	1	0
PREAMBLE_LEN	15:13	R / W	Preamble Length setting	000: 2bytes 001: 4bytes 010: 6 bytes … 111: 16 bytes	
SYNCWORD_LEN	12:11	R / W	Syncword Length setting	00: 16 bits 01: 32 bits 10: 48 bits 11: reserved	
TRAILER_LEN	10: 8	R / W	Trailer Length setting	000: 4bits 001: 6bits ... 111: 18 bits Trailer Length = setting value * 2 + 4 (bits)	
PACK_TYPE	7: 6	R / W	Data encoding selection	00: NRZ law data 01: Manchester data type 10: 8bit / 10bit line code 11: Interleave data type	
FEC_TYPE	5: 4	R / W	FEC Function enable bit	00: NO FEC 10: FEC23 others: reserved	
-	3: 0	-		-	

table 18-2 PKTCTRL Register Description

register	Transmission and reception enable register TRCTL				
address	0x21				
Reset value	0x0000				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 9	-	-	-	
DBUS_TXEN	8	R / W	Transmit Enable (And the reception are not simultaneously enabled '1')	Enable	Not enabled
DBUS_RXEN	7	R / W	Receive enable (And can send the same time '1')	Enable	Not enabled
-	6: 0	-	-	-	

table 18-3 TRCTL Register Description

register	Channel Setting register CHANNR				
address	0x22				
Reset value	0x1830				
Bit Name	Place	Read and write	Bit Description	1	0
-	15:14	-	-		
REF_FQ	13: 9	R / W	The frequency of the reference clock (MHz)	12M Crystal: 01100 16M Crystal: 10000 20M Crystal: 10100	
-	8: 7	-	-	-	
PLL_CH_NO	6: 0	R / W	RF channel number	The on-air frequency: F = RF_FREQ_BASE + PLL_CH_NO	

table 18-4 CHANNR Register Description

register	Configuration Register MISC0				
address	0x23				
Reset value	0x0300				
Bit Name	Place	Read and write	Bit Description	1	0
PD_CTRL	15	R / W	POWER DOWN Mode enable signal (RF Transceiver enters POWER DOWN After the mode register state can be held reader, but FIFO Do not Operational, interrupt flag can not be cleared.)	Enable	Not enabled
SFT_RST	14	R / W	Software reset enable signal (not reset register values)	Enable	Not enabled
-	13:12	-	-	-	
RE_TX_TIMES	11: 8	R / W	PTX Automatic number of retransmissions (ACK Function enable effective post)	NOTE: Setting range 0 ~ 0xE Retransmission times Number setting value plus 1	
MISO_TRI_OPT	7	R / W	SPI Sheet preferably at a high level, MISO Pin Configuration status	MISO Pin output Enable	MISO Pin output is not enabled for High impedance state
SCRAMBLE_DATA	6: 0	R / W	Scrambling seed	-	

table 18-5 MISC0 Register Description

register	Frequency offset compensation register FOCCFG				
address	0x24				
Reset value	0x4000				
Bit Name	Place	Read and write	Bit Description	1	0
PREAMBLE_NUM 15:12 R / W	Receiving detection Preamble length			Detecting a length of preamble_num * 2 (bits)	
RF_FREQ_FRACTION 11: 0 R / W	Frequency offset compensation register			See 17.4 Festival	

table 18-6 FOCCFG Register Description

register	Starting frequency setting register FREQBASE				
address	0x25				
Reset value	0x0962				
Bit Name	Place	Read and write	Bit Description	1	0
-	15:12	-	-	-	
RF_FREQ_BASE 11: 0 R / W			The initial frequency setting (MHz)	RF operating frequency range of 2402 ~ 2483MHz , Must comply with the set value PLL_CH_NO Register set value, the working frequency is in the frequency range support.	

table 18-7 FREQBASE Register Description

register	Pull current drive and Enable Control Register DS_PE			
address	0x26			
Reset value	0x000F			
Bit Name	Bit read and write	Bit Description	1	0
CE_DS	15	R / W CE PAD large current drive enable	1 : enable , 0 : disable	
CSN_DS	14	R / W CSN PAD enable high-current drive	1 : enable , 0 : disable	
SCK_DS	13	R / W SCK PAD enable high-current drive	1 : enable , 0 : disable	
IRQ_DS	12	R / W IRQ PAD enable high-current drive	1 : enable , 0 : disable	
MOSI_DS	11	R / W MOSI PAD enable high-current drive 1 : enable , 0 : disable		
MISO_DS	10	R / W MISO PAD enable high-current drive 1 : enable , 0 : disable		
CE_PE	9	R / W Pull enable CE PAD	1 : enable , 0 : disable	
CSN_PE	8	R / W CSN PAD pull-enabled	1 : enable , 0 : disable	
SCK_PE	7	R / W SCK PAD pull-enabled	1 : enable , 0 : disable	
IRQ_PE	6	R / W Pull-up enabled IRQ PAD	1 : enable , 0 : disable	
MOSI_PE	5	R / W MOSI PAD pull-enabled	1 : enable , 0 : disable	
MISO_PE	4	R / W MISO PAD pull-enabled	1 : enable , 0 : disable	
CE_SONOF	3	R / W CE FILTER enable	1 : enable , 0 : disable	
CSN_SONOF	2	R / W CSN FILTER enable	1 : enable , 0 : disable	
SCLK_SONOF	1	R / W SCLK FILTER enable	1 : enable , 0 : disable	
MOSI_SONOF	0	R / W MOSI FILTER enable	1 : enable , 0 : disable	

table 18-8 DS_PE Register Description

register	Threshold value setting register THRES				
address	0x28				
Reset value	0x2103				
Bit Name	Place	Read and write	Bit Description	1	0
EMPTY_THRES	15:11	R / W	FIFO0 Half-empty threshold (Link Control mode using software)	-	
FULL_THRES	10: 6	R / W	FIFO0 Half-full threshold (Link Control mode using software)	-	
SYNC_THRES	5: 0	R / W	Allow sync word error threshold number	-	

table 18-9 THRES Register Description

register	Configuration Register MISC1				
address	0x29				
Reset value	0x1800				
Bit Name	Place	Read and write	Bit Description	1	0
-	15	-	-	-	
CRC_SEL	14	R / W	CRC Select Control	CRC8	CRC16
SCRAMBLE_ON	13	R / W	Scrambling function enable bit	Enable	Not enabled
PACK_LENGTH_EN	12	R / W	Link control mode selection	Hardware Link Control	Software Link Control
FW_HW_TERM_EN	11	R / W	In hardware link control mode PTX Send stop mode configuration	when FIFO0 The read and write pointers are equal automatic stop send	By the master MCU Decision sent Close time
PKT_HINT_PORITY	10	R / W	Active level interrupt pin configuration	Active Low	Active High
-	9: 8	-	-	-	
CRC_INIT_DATA	7: 0	R / W	CRC Shift Register The initial value	-	

table 18-10 MISC1 Register Description

register	Configuration Register MISC2				
address	0x2A				
Reset value	0xC07D				
Bit Name	Place	Read and write	Bit Description	1	0
RATE	15	R / W	Select the transmission rate	1Mbps	250Kbps
AFC_MCTRL	14	R / W	AFC Function Control	Enable	Not enabled
DCOC_ENABLE	13	R / W	DCOC Calibration enable	Enable	Not enabled
DCOC_CTRL	12:10	R / W	DCOC Calibration control bits	Enable	Not enabled
-	9	-	-	-	-
ACKTIME_ADJUST_ON	8	R / W	AUTO_RX_ACK_TIME Take time to register settings 2	Enable	Not enabled
AUTO_RX_ACK_TIME	7: 0	R / W	in ACK Enable case, PTX Transmitted is received by the switch to@ 1Mbps	wait ACK The time register set value * 1us	

			After waiting ACK time. The register set value * 4us @ 250Kbps Recommended setting value preamble_length (bits) + 100 @ 1Mbps preamble_length (bits) + 52 @ 250Kbps	

table 18-11 MISC2 Register Description

register	Received packet signal energy indication register PKG_RSSI				
address	0x2B				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	
PKG_RSSI	7: 0	R	data pack RSSI value(dBm)	See 17.6 Festival	

table 18-12 PKG_RSSI Register Description

register	CD Threshold value setting register CDTH				
address	0x2C				
Reset value	0x8883				
Bit Name	Place	Read and write	Bit Description	1	0
CD_TH1	15: 8	R / W	CD The high threshold	See 17.7 Festival	
CD_TH2	7: 0	R / W	CD Low threshold		

table 18-13 CDTH Register Description

register	Received signal energy indication register RSSI				
address	0x2D				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	
RSSI	7: 0	R	RSSI value(dBm)	See 17.6 Festival	

table 18-14 RSSI Register Description

register	Status Register STATUS0				
address	0x2E				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15:12	-	-	-	
PQT	11	R	Preamble Detection flag	Found to be effective Preamble	No valid Preamble
CD	10	R	carrier detect Mark	Found to be effective carriers	No effective carrier
FREQ_ESTIMATION 9: 0		R	Estimated values of the frequency deviation	See 17.4 Festival	

table 18-15 STATUS0 Register Description

register	Status Register STATUS1				
address	0x30				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	
PIPE_ADDR_MATCH	7	R	Sync word is received successfully completed flag after receiving hardware clear '0'	Synchronization successfully	synchronized unsuccessful
-	6	-	-	-	
FSM_TX_STATE	5	R	The current state of the state machine transmits Indicator bit	The state machine is in the Send state	The state machine is not in send status
-	4: 0	-	-	-	

table 18-16 STATUS1 Register Description

register	Fixed length register FIX_LEN_EN				
address	0x31				
Reset value	0x0F01				
Bit Name	Bit	read and write	Bit Description	1	0
FIX_PLD_LEN	15: 8	R / W	Fixed-length mode payload length	-	
FIX_PLD_LEN_EN	7	R / W	Fixed length mode enable	Enable	Not enabled
-	6: 0	-	-	-	

table 18-17 FIX_LEN_EN Register Description

register	FIFO0 Access Register FIFO0DATA				
address	0x32				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	
FIFO0DATA	7: 0	R / W	FIFO0 Access Register (MCU Chip byte As a unit access FIFO)	FIFO Read and write operations see 16.3.3 chapter	

table 18-18 FIFO0DATA Register Description

register	FIFO1 Access Register FIFO1DATA				
address	0x33				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	
FIFO1DATA	7: 0	R / W	FIFO1 Access Register (MCU Chip byte As a unit access FIFO)	FIFO Read and write operations see 16.3.3 chapter	

table 18-19 FIFO1DATA Register Description

register	ACKFIFO0 Access Register ACKFIFO0DATA				
address	0x34				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	-
ACKFIFO0DATA	7: 0	R / W	ACKFIFO0 Access Register (MCU Chip byte As a unit access ACKFIFO)	FIFO Read and write operations see 16.3.3 chapter	

table 18-20 ACKFIFO0DATA Register Description

register	ACKFIFO1 Access Register ACKFIFO1DATA				
address	0x35				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	-
ACKFIFO1DATA	15: 0	R / W	ACKFIFO1 Access Register (MCU Chip byte As a unit access ACKFIFO)	FIFO Read and write operations see 16.3.3 chapter	

table 18-21 ACKFIFO1DATA Register Description

register	FIFO0 Configuration Register FIFO0CTRL				
address	0x36				
Reset value	0x008E				
Bit Name	Place	Read and write	Bit Description	1	0
PTX_FIFO0_FAIL	15	R	Retransmission timeout signal, distinguishing between the transmission interrupt is set for starting PTX status(PTX clear INT0 Automatically cleared by hardware '0')	No retransmission timeout	retransmission timeout
-	14	-	-	-	
PRX_CRC_ERR0	13	R	PRX Stored in the receiver FIFO0 middle PAYLOAD CRC Bit error indication	CRC error	CRC correct
PRX_FEC23_ERR0	12	R	Stored in the FIFO0 Reception PAYLOAD FEC2 / 3 Bit error indication	FEC error	FEC correct
PRX_FIFO0_PIPE	11: 9	R	PRX Stored in the receiver FIFO0 middle PAYLOAD Data belongs PIPE	000: PIPE0 001: PIPE1 010: PIPE2 011: PIPE3 Others: invalid	
			PRX FIFO0 Data filled out PRX FIFO0		PRX FIFO0

PRX_FIFO0_OCPY	8	R	Signal (interrupt clear INT0 After the hardware clear '0')	Occupied	Unoccupied
FIFO0_EN	7	R / W	FIFO0 Enable	Enable	Not enabled
-	6: 5	-	-	-	
PTX_FIFO0_NOACK	4	R / W	inform PRX From FIFO0 Sent PAYLOAD No need ACK Control bit (ACK Function active when enabled)	NOACK	ACK
PTX_FIFO0_PIPE	3: 1	R / W	PTX FIFO0 middle PAYLOAD Data belongs PIPE	000: PIPE0 001: PIPE1 010: PIPE2 011: PIPE3 Others: invalid	
PTX_FIFO0_OCPY	0	R / W	PTX FIFO0 Data filled out Signal (Software cleared '0')	PTX FIFO0 Occupied	PTX FIFO0 Unoccupied

table 18-22 FIFO0CTRL Register Description

register	FIFO1 Configuration Register FIFO1CTRL				
address	0x37				
Reset value	0x008E				
Bit Name	Place	Read and write	Bit Description	1	0
PTX_FIFO1_FAIL	15	R	Retransmission timeout signal, distinguishing between the transmission interrupt is set for starting PTX status(PTX clear INT1 Automatically cleared by hardware '0')	No retransmission timeout	retransmission timeout
-	14	-	-	-	
PRX_CRC_ERR1	13	R	PRX Stored in the receiver FIFO1 middle PAYLOAD CRC Bit error indication	CRC error	CRC correct
PRX_FEC23_ERR1	12	R	Stored in the FIFO1 Reception PAYLOAD FEC2 / 3 Bit error indication	FEC error	FEC correct
PRX_FIFO1_PIPE	11: 9	R	PRX Stored in the receiver FIFO1 middle PAYLOAD Data belongs PIPE	000: PIPE0 001: PIPE1 010: PIPE2 011: PIPE3 Others: invalid	
PRX_FIFO1_OCPY	8	R	PRX FIFO1 Fill complete data signal (clear interrupt INT1 After clearing the hardware '0')	PRX FIFO1 Occupied	PRX FIFO1 Unoccupied
FIFO1_EN	7	R / W	FIFO1 Enable	Enable	Not enabled
-	6: 5	-	-	-	
PTX_FIFO1_NOACK	4	R / W	inform PRX From FIFO1 Sent PAYLOAD No need ACK control NOACK		ACK

			Bit (ACK Function active when enabled)		
PTX_FIFO1_PIPE	3: 1	R / W	PTX FIFO1 middle PAYLOAD Data belongs PIPE	000: PIPE0 001: PIPE1 010: PIPE2 011: PIPE3 Others: invalid	
PTX_FIFO1_OCPY	0	R / W	PTX FIFO1 Data filled out Signal (Software cleared '0')	PTX FIFO1 Occupied	PTX FIFO1 Unoccupied

table 18-23 FIFO1CTRL Register Description

register	ACKFIFO0 Configuration Register ACKFIFO0CTRL				
address	0x38				
Reset value	0x0E80				
Bit Name	Place	Read and write	Bit Description	1	0
-	15:12	-	-	-	
PRX_ACKFIFO0_PIPE	11: 9	R / W	PRX ACKFIFO0 in ACK PAYLOAD Data belongs PIPE	000: PIPE0 001: PIPE1 010: PIPE2 011: PIPE3 Others: invalid	
PRX_ACKFIFO0_OCPY	8	R / W	PRX ACKFIFO0 Fill complete data signal (by software '0')	PRX ACKFIFO0 Occupied	PRX ACKFIFO0 Unoccupied
ACKFIFO0_EN	7	R / W	ACKFIFO0 Enable	Enable	Not enabled
-	6: 5	-	-	-	
PTX_ACKCRC_ERR0	4	R	PTX Stored in the receiver ACKFIFO0 of ACK PAYLOAD CRC Bit error indication	CRC error	CRC correct
PTX_ACKFIFO0_PIPE	3: 1	R	PTX Stored in the receiver ACKFIFO0 in ACK PAYLOAD Data belongs PIPE	000: PIPE0 001: PIPE1 010: PIPE2 011: PIPE3 Others: invalid	
PTX_ACKFIFO0_OCPY	0	R	PTX ACKFIFO0 Fill complete data signal (clear interrupt ACK_INT0 Rear Hardware clear '0')	PTX ACKFIFO0 Occupied	PTX ACKFIFO0 Unoccupied

table 18-24 ACKFIFO0CTRL Register Description

register	ACKFIFO1 Configuration Register ACKFIFO1CTRL				
address	0x39				
Reset value	0x0E80				
Bit Name	Place	Read and write	Bit Description	1	0
-	15:12	-	-	-	
PRX_ACKFIFO1_PIPE 11: 9 R / W			PRX ACKFIFO1 in ACK PAYLOAD Data belongs PIPE	000: PIPE0 001: PIPE1 010: PIPE2 011: PIPE3 Others: invalid	
PRX_ACKFIFO1_OCPY	8	R / W	PRX ACKFIFO1 Fill complete data signal (by software '0')	PRX ACKFIFO1 Occupied	PRX ACKFIFO1 Unoccupied
ACKFIFO1_EN	7	R / W	ACKFIFO1 Enable	Enable	Not enabled
-	6: 5	-	-	-	
PTX_ACKCRC_ERR1	4	R	PTX Stored in the receiver ACKFIFO1 of ACK PAYLOAD CRC Bit error indication	CRC error	CRC correct
PTX_ACKFIFO1_PIPE	3: 1	R	PTX Stored in the receiver ACKFIFO1 in PAYLOAD Data belongs PIPE	000: PIPE0 001: PIPE1 010: PIPE2 011: PIPE3 Others: invalid	
PTX_ACKFIFO1_OCPY	0	R	PTX ACKFIFO1 Fill complete data signal (clear interrupt ACK_INT1 Rear Hardware clear '0')	PTX ACKFIFO1 Occupied	PTX ACKFIFO1 Unoccupied

table 18-25 ACKFIFO1CTRL Register Description

register	FIFO Status Register FIFOSTATUS				
address	0x3A				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
-	15:10	-	-	-	
FIFO0_HALF_FULL	9	R	receive FIFO0 Half-full indicator bit	Half-full	Not half full
FIFO0_HALF_EMPTY	8	R	send FIFO0 Half-empty indicator bit	Mid-air	Not half empty
-	7: 6	-	-	-	
ACKFIFO1_ OCPY	5	R	ACKFIFO1 Status Indicators	ACKFIFO1 Occupied	ACKFIFO1 Unoccupied
ACKFIFO0_ OCPY	4	R	ACKFIFO0 Status Indicators	ACKFIFO0 Occupied	ACKFIFO0 Unoccupied

FIFO1_ OCPY	3	R	FIFO1 Status Indicators	FIFO1 Occupied	FIFO1 Unoccupied
FIFO0_ OCPY	2	R	FIFO0 Status Indicators	FIFO0 Occupied	FIFO0 Unoccupied
-	1: 0	-	-	-	

table 18-26 FIFOSTATUS Register Description

register	FIFO Pointer register CLEAR				
address	0x3B				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
CLR_W_PTR	15	W	FIFO Write pointer clear '0' signal (Not in reception PAYLOAD When you use)	FIFO Write pointer clear '0'	Invalid operation
CLR_W_ACKPTR 14		W	ACKFIFO Write pointer clear '0' signal (Not in reception ACK PAYLOAD When you use)	ACK FIFO Write pointer clear '0'	Invalid operation
FIFO0_WR_PTR 13: 8		R	FIFO0 Write pointer	-	
CLR_R_PTR	7	W	FIFO Read pointer clear '0' signal (Not sent PAYLOAD When you use)	FIFO Read pointer clear '0'	Invalid operation
CLR_R_ACKPTR	6	W	ACK FIFO Read pointer clear '0' signal (Not sent ACK PAYLOAD When you use)	ACK FIFO Read pointer clear '0'	Invalid operation
FIFO0_RD_PTR	5: 0	R	FIFO0 Read pointer	-	

table 18-27 CLEAR Register Description

register	PIPE Setting register PIPECTRL				
address	0x3C				
Reset value	0x3000				
Bit Name	Place	Read and write	Bit Description	1	0
P3_EN	15	R / W	PIPE3 Enable signal	Enable	Not enabled
P2_EN	14	R / W	PIPE2 Enable signal	Enable	Not enabled
P1_EN	13	R / W	PIPE1 Enable signal	Enable	Not enabled
P0_EN	12	R / W	PIPE0 Enable signal	Enable	Not enabled
-	11: 8	-			
P3_ACKPAYLOAD_EN	7	R / W	PIPE3 ACK band PAYLOAD Enable signal	Enable	Not enabled
P2_ACKPAYLOAD_EN	6	R / W	PIPE2 ACK band PAYLOAD Enable signal	Enable	Not enabled
P1_ACKPAYLOAD_EN	5	R / W	PIPE1 ACK band	Enable	Not enabled

			PAYLOAD Enable signal		
P0_ACKPAYLOAD_EN	4	R / W	PIPE0 ACK band PAYLOAD Enable signal	Enable	Not enabled
P3_ACK_EN	3	R / W	PIPE3 ACK Enable signal	Enable	Not enabled
P2_ACK_EN	2	R / W	PIPE2 ACK Enable signal	Enable	Not enabled
P1_ACK_EN	1	R / W	PIPE1 ACK Enable signal	Enable	Not enabled
P0_ACK_EN	0	R / W	PIPE0 ACK Enable signal	Enable	Not enabled

table 18-28 PIPECTRL Register Description

register	Interrupt Register INT				
address	0x3D				
Reset value	-				
Bit Name	Place	Read and write	Bit Description	1	0
ACKINT1_CLR	15	W	ACKINT1 Flag clear '0' signal	clear '0'	Invalid operation
ACKINT1_PID	14:13	R	ACKINT1 for '1' Time PID Indicator bit	PTX: When instructions ACKINT1 for '1' Time, ACKFIFO1 Received ACK PAYLOAD Corresponding PID . PRX: When instructions ACKINT1 for '1' Time, ACKFIFO1 The last successful transmission of ACK PAYLOAD Corresponding PID .	
ACKINT1	12	R	ACKFIFO1 Interrupt flag PTX: ACKFIFO1 Meet ACK PAYLOAD Postposition '1' . PRX: PRX Upon receiving a new packet PID When set to change '1' . A show from the front ACKFIFO1 Sent ACK PAYLOAD Sent successfully. (See specific 16.2 Section)	Interrupt occurs not interrupted	
ACKINT0_CLR	11	W	ACKINT0 Flag clear '0' signal	clear '0'	Invalid operation
ACKINT0_PID	10: 9	R	ACKINT0 for '1' Time PID Indicator bit	PTX: When instructions ACKINT0 for '1' Time, ACKFIFO0 Received ACK PAYLOAD Corresponding PID . PRX: When instructions ACKINT0 for '1' Time, ACKFIFO0 The last successful transmission of ACK PAYLOAD Corresponding PID .	
			ACKFIFO0 Interrupt flag PTX: ACKFIFO0 Meet ACK PAYLOAD Postposition '1' .		

ACKINT0	8	R	PRX: PRX Upon receiving a new packet PID When set to change '1' . A show from the front ACKFIFO0 Sent ACK PAYLOAD Sent successfully. (See specific 16.2 Section)	Interrupt occurs not interrupted	
INT1_CLR	7	W	INT1 Flag will be cleared '0' signal	clear '0'	Invalid operation
FIFO1_ACK_POS	6	R	PTX From FIFO1 After receiving the contract ACK PAYLOAD Stored ACK FIFO (Only for PTX And ACKINT1 = '1' , ACKINT1_W_ACKPAY = '1' Valid)	ACKFIFO1	ACKFIFO0
ACKINT1_W_ACKPAY	5	R	ACKINT1 Whether with ACK PAYLOAD Indicator bit (Only for PTX And ACKINT1 = '1' Valid)	ACK band PAYLOAD	ACK Without PAYLOAD
INT1	4	R	FIFO1 Interrupt flag PTX: Send completed or send timeout PRX: Reception completion, transmission ACK Completed or Syncword match. (See specific 16.2 Section)	Interrupt occurs not interrupted	
INT0_CLR	3	W	INT0 Flag will be cleared '0' signal	clear '0'	Invalid operation
FIFO0_ACK_POS	2	R	PTX From FIFO0 After receiving the contract ACK PAYLOAD Stored ACK FIFO (Only for PTX ,and ACKINT0 = '1', ACKINT0_W_ACKPAY = '1' Valid)	ACKFIFO1	ACKFIFO0
ACKINT0_W_ACKPAY	1	R	ACKINT0 Whether with ACK PAYLOAD Indicator bit (Only for PTX And ACKINT0 = '1' Valid)	ACK band PAYLOAD	ACK Without PAYLOAD
INT0	0	R	FIFO0 Interrupt flag PTX: Send completed or send timeout PRX: Reception completion, transmission ACK Completed or Syncword match. (See specific 16.2 Section)	Interrupt occurs not interrupted	

table 18-29 INT Register Description

Register Name	PIPE0 Address register P0ADDR0				
address	0x40				
Reset value	0xE7E7				
Bit Name	Place	Read and write	Bit Description	1	0
P0_ADDR [15: 0]	15: 0	R / W	PIPE0 syncword address	-	

table 18-30 P0ADDR0 Register Description

Register Name	PIPE0 Address register P0ADDR1				
address	0x41				
Reset value	0xE7E7				
Bit Name	Place	Read and write	Bit Description	1	0
P0_ADDR [31:16]	15: 0	R / W	PIPE0 syncword address	-	

table 18-31 P0ADDR1 Register Description

Register Name	PIPE0 Address register P0ADDR2				
address	0x42				
Reset value	0xE7E7				
Bit Name	Place	Read and write	Bit Description	1	0
P0_ADDR [47:32]	15: 0	R / W	PIPE0 syncword address	-	

table 18-32 P0ADDR2 Register Description

Register Name	PIPE1 Address register P1ADDR0				
address	0x43				
Reset value	0xC2C2				
Bit Name	Place	Read and write	Bit Description	1	0
P1_ADDR [15: 0]	15: 0	R / W	PIPE1 syncword address	-	

table 18-33 P1ADDR0 Register Description

Register Name	PIPE1 Address register P1ADDR1				
address	0x44				
Reset value	0xC2C2				
Bit Name	Place	Read and write	Bit Description	1	0
P1_ADDR [31:16]	15: 0	R / W	PIPE1 syncword address	-	

table 18-34 P1ADDR1 Register Description

Register Name	PIPE1 Address register P1ADDR2				
address	0x45				
Reset value	0xC2C2				
Bit Name	Place	Read and write	Bit Description	1	0
P1_ADDR [47:32]	15: 0	R / W	PIPE1 syncword address	-	

table 18-35 P1ADDR2 Register Description

Register Name	PIPE2 Address register P2ADDR				
address	0x46				
Reset value	0xxx58				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	
P2_ADDR [7: 0]	7: 0	R / W	PIPE2 syncword Address Low 8 Bit. PIPE2 The total length of the address register by SYNCWORD_LEN Configuration: 16bit: {P1_ADDR [15: 8], P2_ADDR} 32bit: {P1_ADDR [31: 8], P2_ADDR} 48bit: {P1_ADDR [47: 8], P2_ADDR}	-	

table 18-36 P2ADDR Register Description

Register Name	PIPE3 Address register P3ADDR				
address	0x47				
Reset value	0xxxA7				
Bit Name	Place	Read and write	Bit Description	1	0
-	15: 8	-	-	-	
P3_ADDR [7: 0]	7: 0	R / W	PIPE3 syncword Address Low 8 Bit. PIPE3 The total length of the address register by SYNCWORD_LEN Configuration: 16bit: {P1_ADDR [15: 8], P3_ADDR} 32bit: {P1_ADDR [31: 8], P3_ADDR} 48bit: {P1_ADDR [47: 8], P3_ADDR}	-	

table 18-37 P3ADDR Register Description

The first 19 chapter RF Transceivers - Explanation of terms

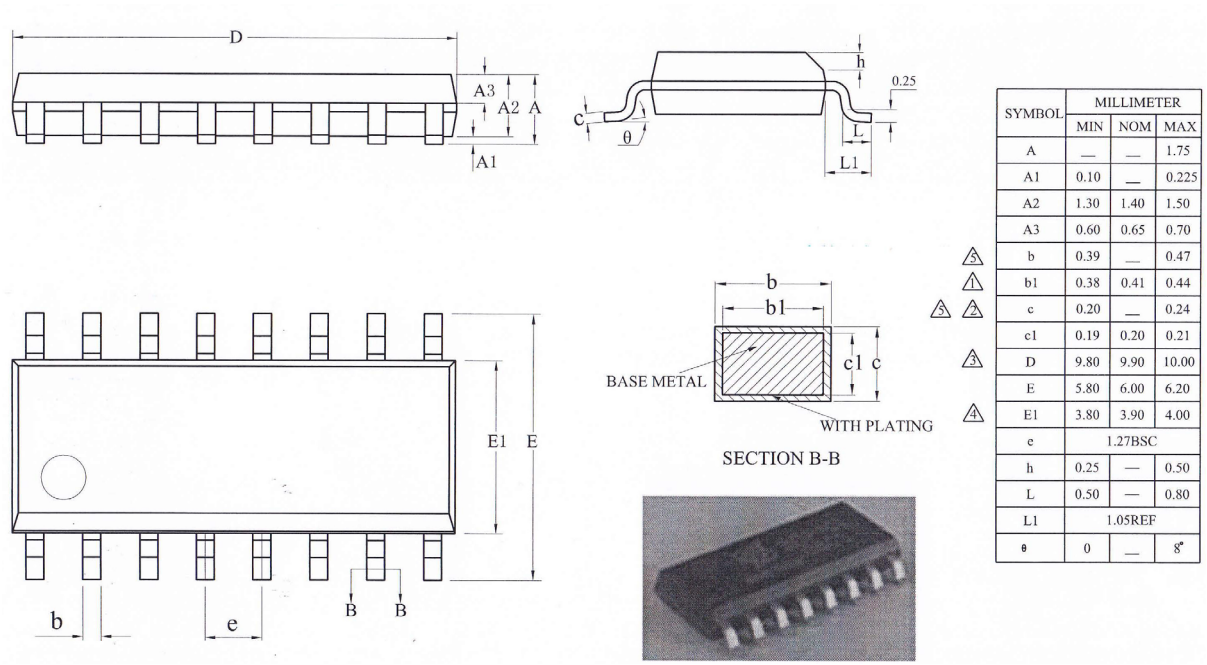
RF The term transceiver, please refer to the following table:

Term	Description
ACK	Acknowledgement
ART	Auto Re-Transmit
PTX	Primary TX
PRX	Primary RX
TX	Transmit
RX	Receive
ISM	Industrial-Scientific-Medical
GFSK	Gaussian Frequency Shift Keying
PID	Packet Identity Bits
CE	Chip Enable
IRQ	Interrupt Request
CSN	Chip Select NOT
SCK	Serial Clock
MOSI	Master Out Slave In
MISO	Master In Slave Out

table 19-1 Explanation of Terms

The first 20 Cap package dimension

20.1 FIG package size



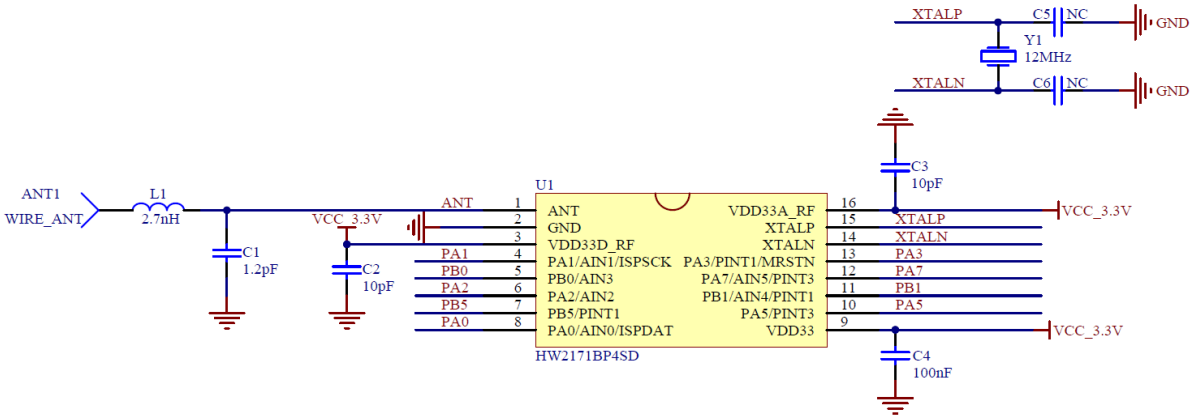
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
5 b	0.39	—	0.47
1 b1	0.38	0.41	0.44
5 2 c	0.20	—	0.24
c1	0.19	0.20	0.21
3 D	9.80	9.90	10.00
E	5.80	6.00	6.20
4 E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Map 20-1 SOP16 FIG package size

The first twenty one Chapter Application Reference Design

21.1 Typical Application Reference PCB design

21. 1.1 reference SCH design diagram



Map 21-1 Typical Application Reference Design SCH Map

have to be aware of is RF Matching parameters, there are two options, as shown in the following table:

Program	L1	C1	Explanation
Inductance program	2.7nH	1.2pF	Only support wire antenna, emission power
Capacitance program	100pF	1.5pF	Support wire and PCB Antenna, transmission power smaller

21. 1.2 Reference Design SCH Considerations

1) Of particular note is ANT foot(PIN1) DC output voltage, can not be grounded. So, if you want to pick up some PCB Inverted antenna (if ground feeding point F type PCB Antenna), capacitive scheme must be used, but the transmission power smaller. If the performance requirements are relatively high, and does not use earthed PCB The antenna, inductors scheme may be used.

2) Chip RF Power supply pins are PIN3 , PIN16 , MCU Power feet PIN9 They are not internally connected, Therefore, the need to connect to an external power supply.

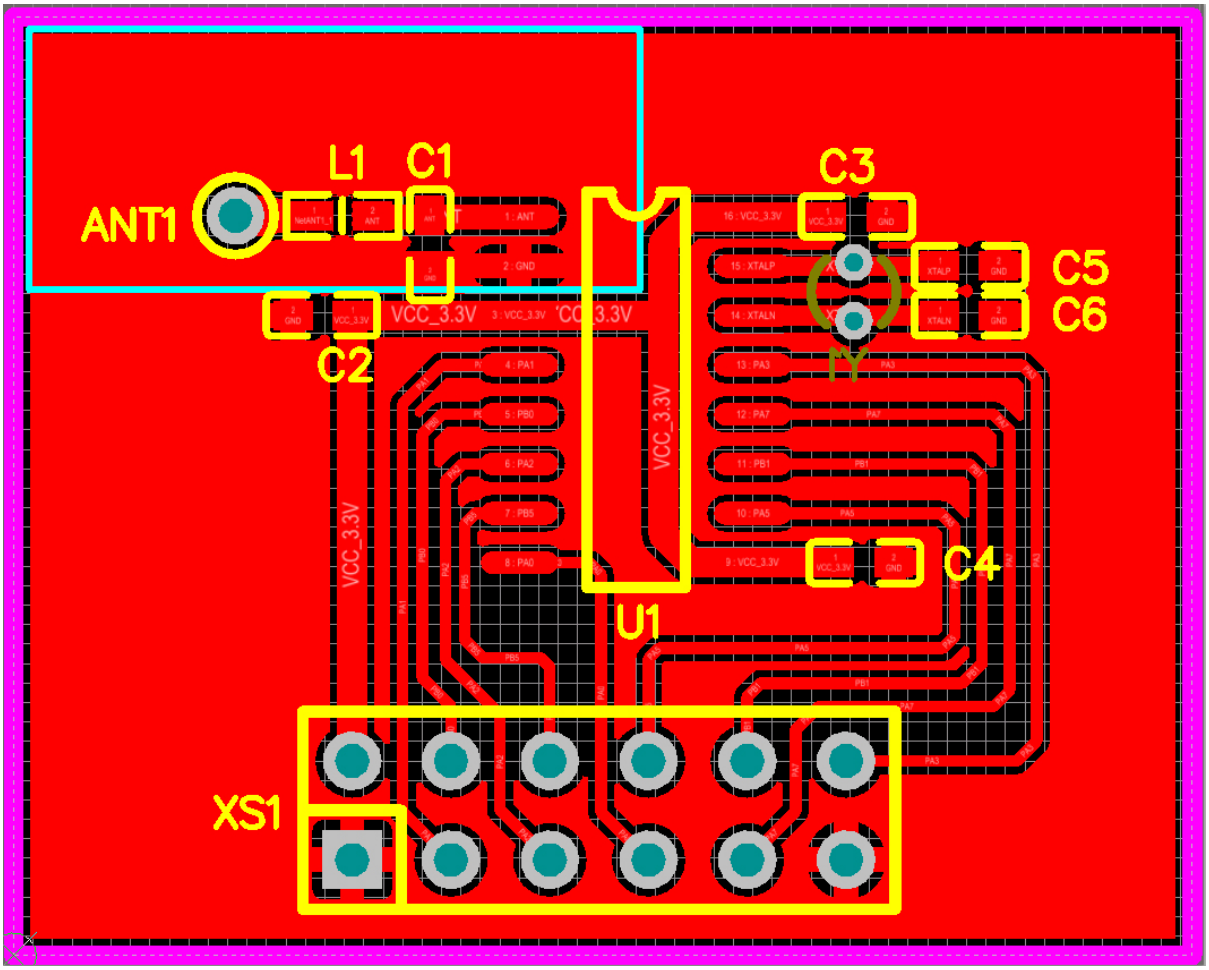
3) capacitance C3 The value of 10pF In favor of harmonic suppression it is very important for the application of certified, must be retained. C2 with C4 Capacitors, respectively, for internal chip RF Digital Power and MCU Filtering power, the reliability of the chip plays an important role.

4) Both sides of the crystal capacitance C5 with C6 Generally do not need to add, use only when necessary to adjust the oscillator frequency, but it is recommended in PCB Board placeholder.

21.2 reference PCB design

21. 2.1 Single panel PCB

Referring single panel design is given.



Map 21-2 Reference design of a single panel PCB Map

21. 2.2 Single panel PCB Design Considerations

1) Require special attention, RF components ANT1 , L1 with C1 Alignment between the straight line as much as possible and as short as possible, it is recommended A direction along the pin, not perpendicular to the pin direction. chip ANT foot(PIN1) Traces must go through C1 Before connecting L1 . C1 Chip capacitor as close as possible ANT foot(PIN1)with GND foot(PIN2).

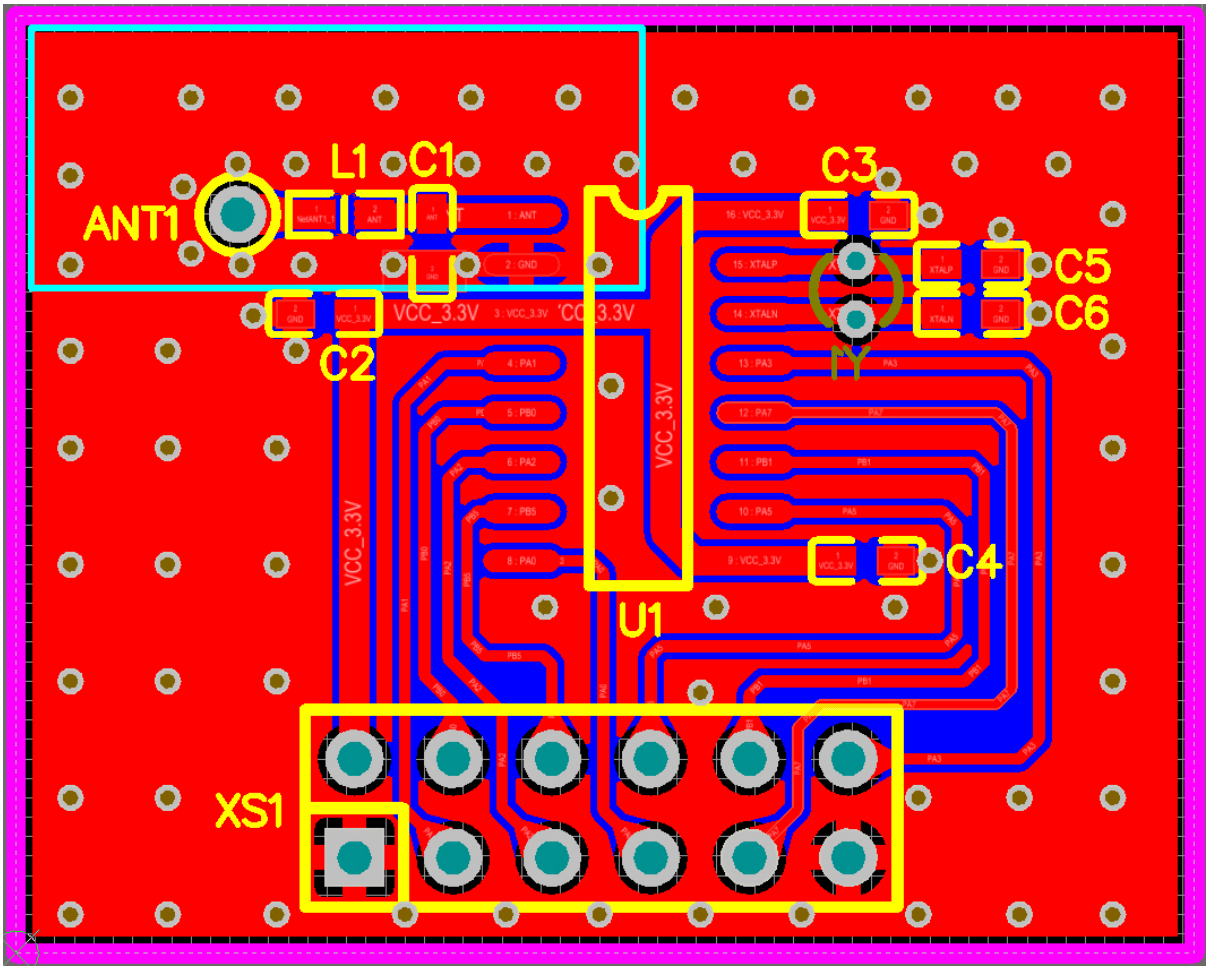
2) Since only one single-sided wiring layer, no separate ground plane, the ground plane of the area should be increased as much as possible, in particular, Chip GND foot(PIN2 Between the ground plane) and the RF circuit. Special attention is required, the RF ground plane (blue border region) need to maintain integrity in this region can only be paved, traces prohibited.

3) As far away from the crystal oscillation circuit and the digital RF circuit.

4) Filter capacitor C2 , C3 , C4 As close to the power pins.

21. 2.3 Double panel PCB

Referring dual-panel design is given.



Map 21-3 Reference Design double panel PCB Map

21. 2.4 Double panel PCB Design Considerations

1) Require special attention, RF components ANT1 , L1 with C1 Alignment between the straight line as much as possible and as short as possible, it is recommended

A direction along the pin, not perpendicular to the pin direction. chip ANT foot(PIN1) Traces must go through C1 Before connecting

L1 . C1 To close as possible 1 Feet and 2 foot.

2) To ensure that the bottom of the RF circuit is complete ground plane (blue border region), the top and bottom in this zone is prohibited

Traces, only paved ground, the area should be as large as possible. Further, the RF circuit should be around "the bag", and placed a number of ground vias to reduce the impedance ground plane. If the power of the digital portion of the bottom have to travel, to consider the alignment of the split ground plane should be as small as possible, and as far away from the RF circuit.

3) As far away from the crystal oscillation circuit and the digital RF circuit.

4) Filter capacitor C2 , C3 , C4 As close to the power pins.

The first twenty two Electrical Characteristics chapter

22.1 MCU Electrical Characteristics

Test Conditions: The following data, unless otherwise marked, are in the temperature range - 40 ℃ ~ 85 ℃.

22. 1.1 The maximum nominal value

parameter	symbol	condition	Nominal value	unit
voltage	VDD	-	-0.3 to 7.5	V
Input voltage	V_{IN}	-	-0.3 ~ VDD + 0.3	V
The output voltage	V_{OUT}	-	-0.3 ~ VDD + 0.3	V
storage temperature	T_{STG}	-	- 55 - 125	℃
Operating temperature	T_{OPR}	VDD : 2.1 ~ 5.5V	- 40 to 85	℃

22. 1.2 Power Parameters

parameter	symbol	Min	Typ	Max	Units		Working conditions
Chip Supply Voltage	VDD	2.1	-	5.5 V			F_{osc} ≤ 2MHz ; - 40 ℃ ~ 85 ℃
		3.0	-	5.5 V			F_{osc} ≤ 20MHz ; - 40 ℃ ~ 85 ℃
Chip quiescent current	I_{DD}	- 200		- μA			25 ℃, VDD = 5V The internal clock mode, all I / O Port input low, MRSTN = 0 , OSC1 = 0 , OSC2 = 0 .
IDLE0 Chip current sleep mode	I_{PD1}	- 2		- μA	25 ℃, VDD = 5V ,		BOR with WDT Enable.
		--3		- μA	25 ℃, VDD = 5V ,		BOR with WDT , LVD Enable.
IDLE1 Current chip (high-speed clock mode) Sleep Mode	I_{PD2}	- 400		- μA			25 ℃, VDD = 5V , BOR with WDT , LVD Enable.
IDLE1 Current chip (low-speed clock mode) Sleep mode	I_{PD3}	--25		- μA			25 ℃, VDD = 5V , BOR with WDT Enable
Current chip normal operating mode (high-speed clock mode)	I_{OP1}	- 2		- mA			25 ℃, VDD = 5V Normal operation mode, the internal 16MHz RC clock, I / O Fixed port output level, no load, ADC shut down.
Current chip normal operating mode (high-speed clock mode)	I_{OP2}	--610		- uA			25 ℃, VDD = 5V Normal operation mode, the internal 2MHz RC Clock (Internal 16MHz RC Clock 8 Divider), I / O Fixed port output level, no load, ADC shut down.

parameter	symbol	Min	Typ	Max	Units		Working conditions
Current chip normal operating mode (low-speed clock mode)	I_{OP3}	--20		- uA			25 ℃, VDD = 5V Normal operation mode, the internal 32KHz RC clock, BOR with LVD Enable, I / O Fixed port output level, no load, ADC shut down.
VDD Maximum input current pin	I_{MAXVDD}	-	-	55	mA	25 ℃, VDD = 5V	
VSS Maximum output current pin	I_{MAXVSS}	-	- 120		mA	25 ℃, VDD = 5V	
Non-high-current I / O Port sink	I_{OL2}	- 8		- mA	25 ℃, VDD = 5V V_{OL} = 0.6V		
Non-high-current I / O Pull current	I_{OH2}	- 8		- mA	25 ℃, VDD = 5V V_{OH} = 4.4V		
High Current I / O Port sink	I_{OL2}	--30		- mA	25 ℃, VDD = 5V V_{OL} = 0.6V		
High Current I / O Pull current	I_{OH2}	--16		- mA	25 ℃, VDD = 5V V_{OH} = 4.4V		

22. 1.3 Input port parameters

parameter	Symbol	Min	Typ	Max	Units		Test Conditions
PA , PB High input port (Schmitt input characteristics)	V_{IH}	0.8VDD		- VDD		V	2.1V ≤ VDD ≤ 5.5V
MRSTN High master reset input port (Schmitt input characteristics)		0.8VDD		- VDD		V	
PA , PB Port input low	V_{IL}	VSS		-	0.18VDD	V	
MRSTN Master reset port input low		VSS		-	0.20VDD	V	
PA , PB Port Input leakage current	I_{IL}	-		-	± 1	μA	2.1V ≤ VDD ≤ 5.5V VSS ≤ Vpin ≤ VDD (Port in high impedance state)
MRSTN Leakage current master reset port		-		--5		μA	VSS ≤ Vpin ≤ VDD
PA , PB Weak pull-up current input port	I_{WPU1}	-		50	- μA		25 ℃, VDD = 5.0V Vpin = VSS
PA , PB Weak pull-down current input port	I_{WPD1}	-		50	- μA		25 ℃, VDD = 5.0V Vpin = VDD
MRSTN Pull-up current master reset input port weak	I_{WPU2}	-		50	- μA		25 ℃, VDD = 5.0V Vpin = VSS

22. 1.4 Output port parameters

parameter	symbol	Min	Typ	Max	Units		Test Conditions
I / O High output port	V_{OH}	VDD-0.7	-	-	V		2.1V ≤ VDD ≤ 5.5V I_{OH} = 2mA
I / O Port output low	V_{OL}	-	-	0.6	V		2.1V ≤ VDD ≤ 5.5V I_{OL} = 3 mA

22. 1.5 System clock parameters

parameter	symbol	Min	Typ	Max	Units		Test Conditions
System clock frequency	F_{OSC}	-	- 2M		Hz		2.1V ≤ VDD ≤ 5.5V
		-	- 8M		Hz		2.7V ≤ VDD ≤ 5.5V
		-	- 20M		Hz		3.0V ≤ VDD ≤ 5.5V
The system clock cycle	T_{OSC1}	500	-	-	ns		2.1V ≤ VDD ≤ 5.5V
		125	-	-	ns		2.7V ≤ VDD ≤ 5.5V
		50	-	-	ns		3.0V ≤ VDD ≤ 5.5V
High and low external clock time	T_{OSL} , T_{OSH}	15	-	-	ns		-
External clock rise and fall times	T_{OSR} , T_{OSF}	-	-	15	ns		-
WDT Overflow time	T_{WDT}	2.4 (9.6KHz)	8 (32K Hz)	13.6 (54K Hz)	ms		VDD = 5V , - 40 ℃ ~ 85 ℃

22. 1.6 internal 16MHz RC Clock calibration parameters

Calibration conditions	Working conditions	Min	Typ	Max	Units
5V , 25 The frequency calibration to ℃ 16MHz	25 ℃, VDD = 5V	15.68	16	16.32	MHz
	- 40 ℃ ~ 85 ℃, VDD = 2.1V ~ 5.5V	15.52	16	16.48	MHz

22. 1. 7 ADC AC parameters

parameter name	symbol	Explanation	Min	Typ	Max	Units
Resolution	RR	25 ℃, VDD = 5V ,internal VDD reference, f_{ADCCLK} = 1MHz The sampling time 8 More ADCCLK	-	11	-	bit
Differential linearity	DNL		- ± 1		- LSB	
Integral linearity	INL		- ± 2		- LSB	
Offset Error Voffset 25 ℃, VDD = 5V , f_{ADCCLK} = 1MHz , Sampling time 8 More ADCCLK			- ± 2		- mV	
The reference voltage	Vref1 25 ℃, VDD = 5V External reference VREFP		2	- VDD		V
	Vref2 25 ℃, VDD = 5V ,internal VDD reference		-	VDD	- V	

parameter name	symbol	Explanation	Min	Typ	Max	Units
	Vref3	25 ℃, VDD = 5V ,internal 4.0V reference	3.92		4.0	4.08 V
	Vref4	25 ℃, VDD = 5V ,internal 3.0V reference	2.94		3.0	3.06 V
	Vref5	25 ℃, VDD = 5V ,internal 2.1V reference	2.05		2.1	2.15 V
ADC Work the chip supply voltage	Vpow	internal VDD Or external reference VREFP reference	2.5	-	-	V
		Internal Reference 2.1V	3	-	-	V
		Internal Reference 3.0V	3.5	-	-	V
		Internal Reference 4.0V	4.5	-	-	V
Analog voltage Input range	VIN	-	0	-	Vref1-5	V
Input capacitance	CIN	-	-	40	-	Pf
Analog input input impedance is recommended	RIN	-	--10		-	KΩ

Note: Here the design parameters for the theoretical value.

22. 1. 8 ADC Conversion time parameters

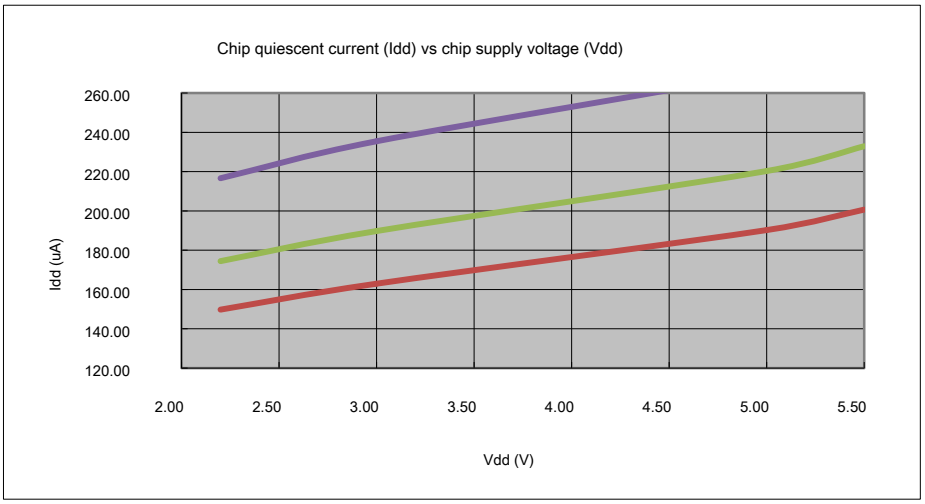
A / D Clock Source select	working frequency			
	16M	8M	4M	1M
Fosc	Not recommended	Not recommended	Not recommended	T_{ADCCLK} = 1us
Fosc / 2	Not recommended	Not recommended	T_{ADCCLK} = 0.5us	T_{ADCCLK} = 2us
Fosc / 4	Not recommended T_{ADCCLK} = 0.5us		T_{ADCCLK} = 1us	T_{ADCCLK} = 4us
Fosc / 8	T_{ADCCLK} = 0.5us	T_{ADCCLK} = 1us	T_{ADCCLK} = 2us	T_{ADCCLK} = 8us
Fosc / 16	T_{ADCCLK} = 1us	T_{ADCCLK} = 2us	T_{ADCCLK} = 4us	T_{ADCCLK} = 16us
Fosc / 32	T_{ADCCLK} = 2us	T_{ADCCLK} = 4us	T_{ADCCLK} = 8us	T_{ADCCLK} = 32us
Fosc / 64	T_{ADCCLK} = 4us	T_{ADCCLK} = 8us	T_{ADCCLK} = 16us	T_{ADCCLK} = 64us

Note: Tad Value does not meet the design requirements of accuracy, not recommended.

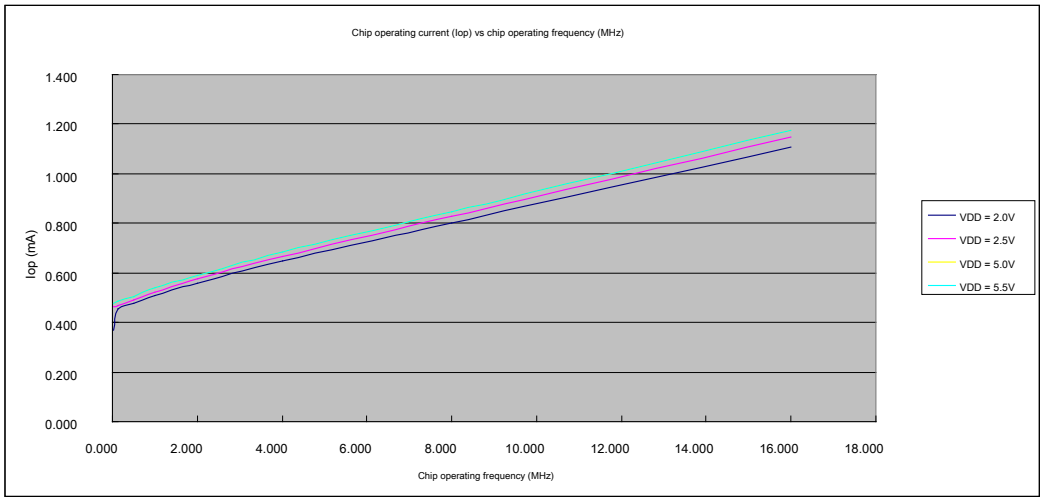
22.2 MCU FIG characteristic parameter

Listed in this section are shown in the test sample, merely as a design reference. Wherein the data listed in section illustrating the operation has exceeded the specified range, this information also for reference only, the chip only guaranteed to operate properly within the specified range.

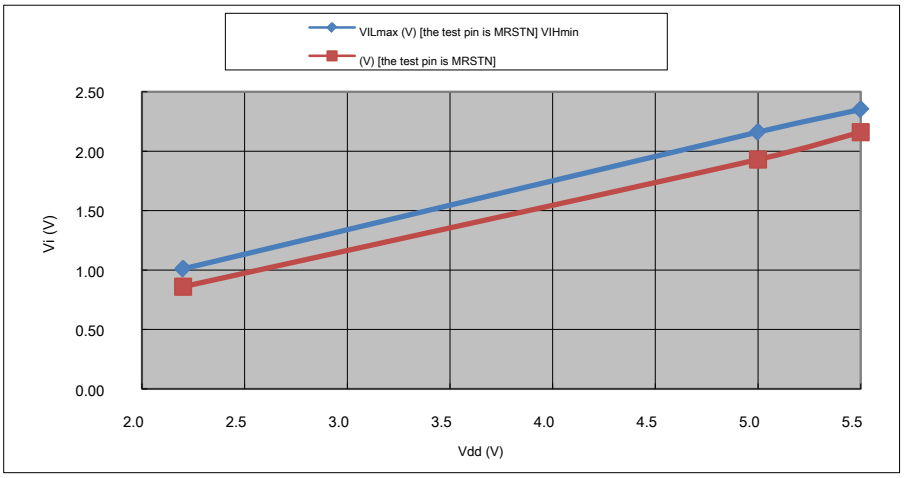
- It accounts for the IC chip with the voltage variation characteristic of FIG.



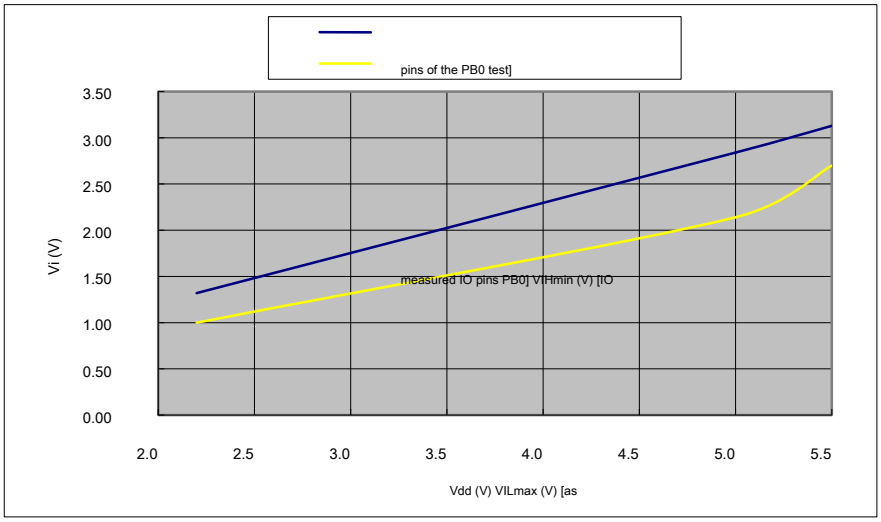
- **Current chip clocked the normal operation mode frequency display (Fosc Internal clock source 16MHz RC Different frequency divided clock, room temperature 25 ℃)**



- External reset input characteristic diagram (rt 25 ℃)

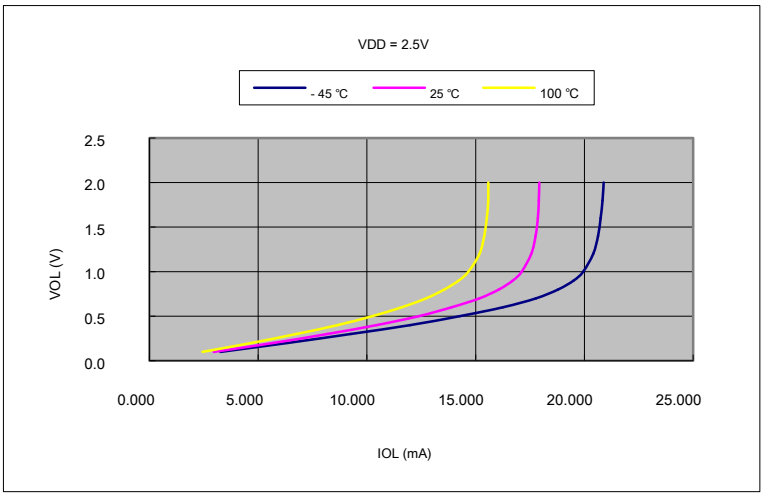


- I / O FIG characteristic signal input port (rt 25 ℃)

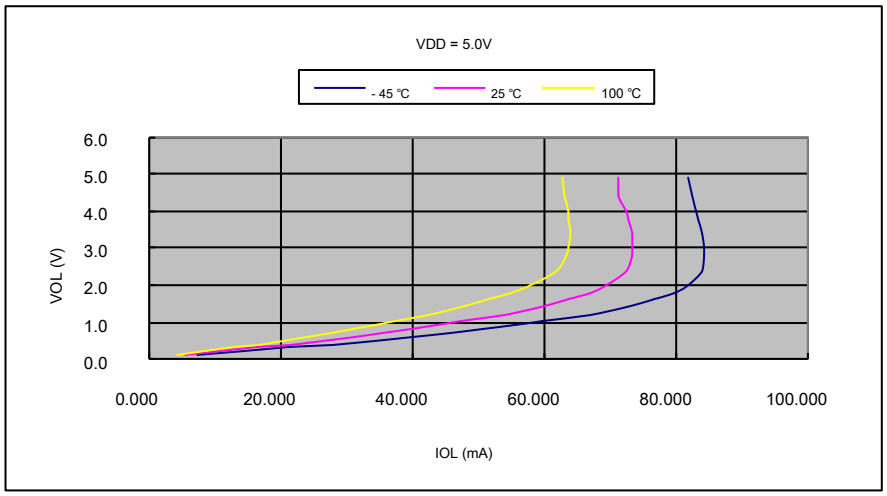


- I / O Port output characteristics of FIG.

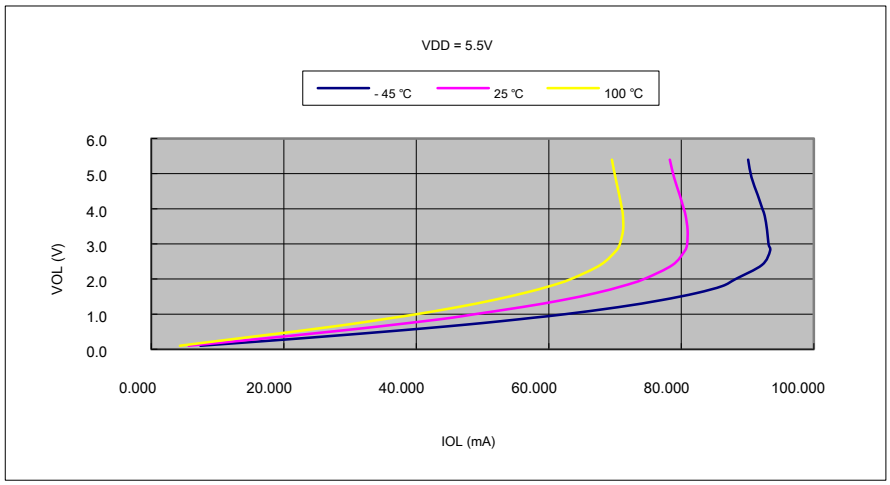
A: V_{OL} vs I_{OL} @ VDD = 2.5V



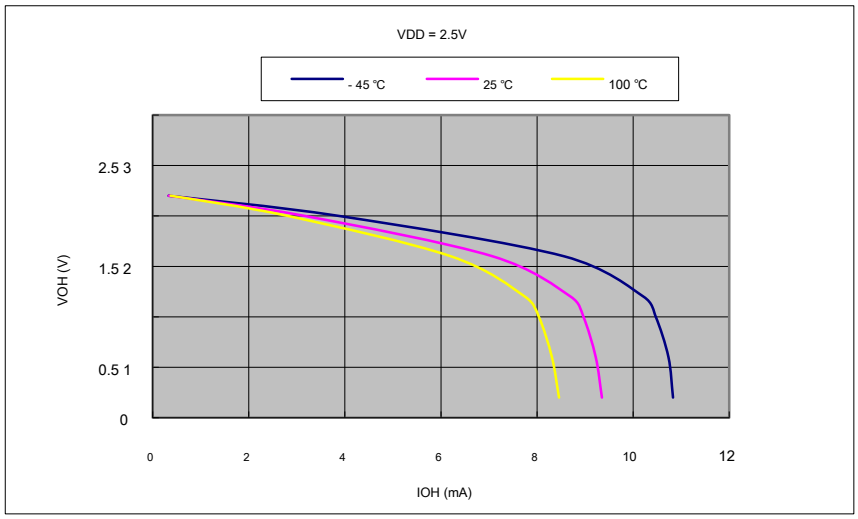
B: V_{OL} vs I_{OL} @ VDD = 5.0V



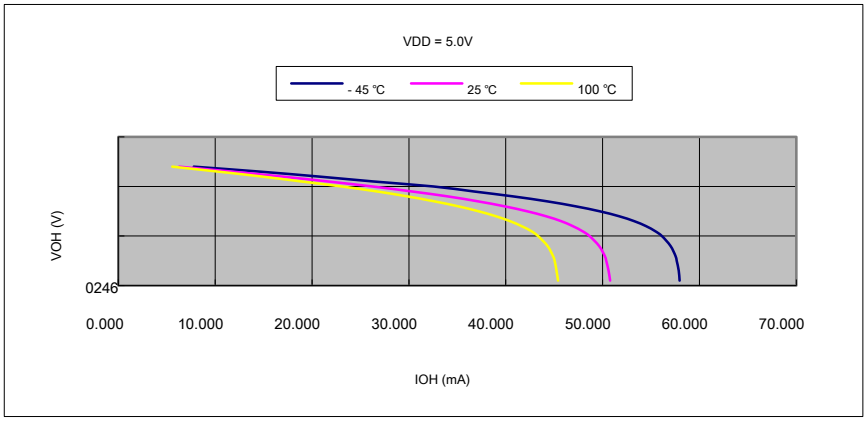
C: V_{OL} vs I_{OL} @ VDD = 5.5V



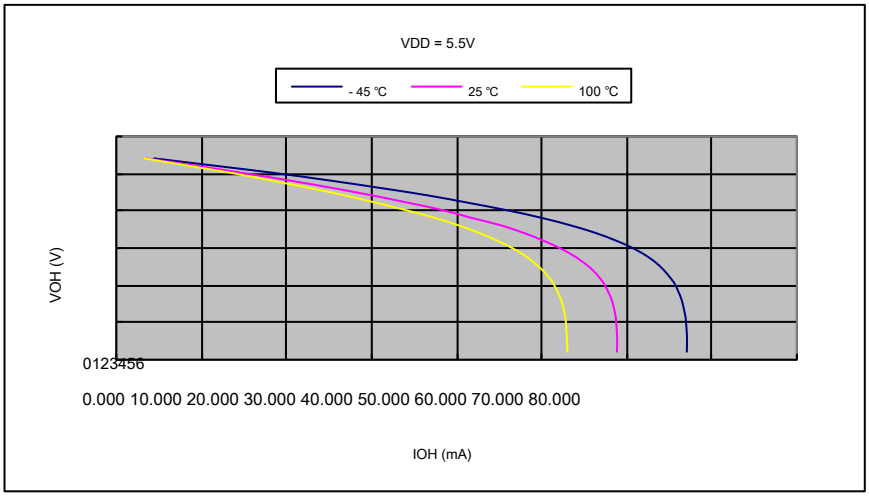
D: V_{OH} vs I_{OH} @ VDD = 2.5V



E: V_{OH} vs I_{OH}@ VDD = 5V



F: V_{OH} vs I_{OH}@ VDD = 5.5V



22.3 RF Transceiver Electrical Characteristics

22. 3.1 Power Parameters

symbol	parameter	Min.	Typ.	Max.	Units
VDDRF	VDDRF Supply voltage	2.0	3.0	3.6	V
	Low-power mode				
I_{VDD_PD}	POWER DOWN Chip current mode	-	1.5	-	uA
I_{VDD_Sleep}	SLEEP Chip current mode	--25		-	uA
I_{VDD_Idle}	IDLE Chip current mode	-	1.7	-	mA
	TX mode				
I_{VDD_TX8}	Output power 8dBm Current at	- 40		-	mA
I_{VDD_TX5}	Output power 5dBm Current at	--28		-	mA
I_{VDD_TX0}	Output power 0dBm Current at	- twenty three		-	mA
I_{VDD_TX5N}	Output power - 5dBm Current at	--18		-	mA
I_{VDD_TX15N}	Output power - 15dBm Current at	--15		-	mA
I_{VDD_TX20N}	Output power - 20dBm Current at	--14		-	mA
I_{VDD_TX25N}	Output power - 25dBm Current at	--13		-	mA
	RX mode				
I_{VDD}	When the current high sensitivity receiver @ 1M / 250Kbps	--20		-	mA
I_{VDD}	Receiver sensitivity when low current @ 1M / 250Kbps Decreased sensitivity (about this mode 6dB)	--16		-	mA

Note: Typ. Data measured at room temperature; Min. with Max. Temperature for the whole, full voltage range was measured minimum and maximum values.

22. 3.2 The basic parameters of Communications

symbol	parameter	Min.	Typ.	Max.	Units
F_{OP}	Working frequency	2300	-	2500	MHz
PLL_{RES}	PLL Configurable frequency	2300	-	2500	MHz
F_{XTAL}	Oscillator frequency	12	12	16	MHz
Δf_{1M}	Offset @ 1Mbps	-	250	-	KHz
Δf_{250K}	Offset @ 250Kbps	-	250	-	KHz
R_{GFSK}	Baseband data rate	250	-	1000	Kbps
F_{CH1M}	Pitch with non-overlapping @ 1Mbps	- 1		-	MHz
F_{CH250K}	Pitch with non-overlapping @ 250Kbps	-	0.25	-	MHz

22. 3.3 Transmitter parameters

symbol	parameter	Min.	Typ.	Max.	Units
P_{RF}	Maximum output power	- 8		-	dBm
P_{RFC}	RF Transmitter output power adjustable range	- 40	- 8		dBm
P_{RFCR}	RF Precision adjustable transmitter output power	- 1		2	dB

22. 3.4 Receiver parameters

symbol	parameter	Min.	Typ.	Max.	Units
RX_{max}	BER <0.1% When the maximum received signal energy	--10	--10		dBm
RX_{SENS}	Sensitivity (0.1% BER) @ 1Mbps	-	- 89	- dBm	
RX_{SENS}	Sensitivity (0.1% BER) @ 250Kbps	-	--93	- dBm	
C / I_{CO}	The same frequency signal C / I (@ 1Mbps)	-	--10		dB
C / I_{1ST}	1st Adjacent channel rejection C / I 1MHz	--25	-	- dB	
C / I_{2ND}	2nd Adjacent channel rejection C / I 2MHz	--27	-	- dB	
C / I_{3RD}	3rd Adjacent channel rejection C / I 3MHz	- 36	-	- dB	
C / I_{CO}	The same frequency signal C / I (@ 250Kbps)	-	- 6		dB
C / I_{1ST}	1st Adjacent channel rejection C / I 1MHz	--25	-	- dB	
C / I_{2ND}	2nd Adjacent channel rejection C / I 2MHz	--27	-	- dB	
C / I_{3RD}	3rd Adjacent channel rejection C / I 3MHz	- 41	-	- dB	

22. 3.5 Parametric oscillator

symbol	parameter	Min.	Typ.	Max.	Units
F_{xo}	Crystal frequency	12	12	16	MHz
ΔF	Crystal frequency offset	-	± 10 ± 60		ppm

22. 3. 6 IO port DC parameter

symbol	parameter	Min.	Typ.	Max.	Units
V_{IH}	IO High input port	0.7VDD	-	- V	
V_{IL}	IO Port input low	-	-	0.4VDD	V
V_{OH}	IO Port output high (IOH = 4.0mA)	VDD-0.6	-	- V	
V_{OL}	IO Port output low (IOL = 6.0mA)	-	-	0.7	V

22. 3.7 State switching time parameter

symbol	parameter	Min.	Typ.	Max.	Units
T_{Stol}	From chip SLEEP Mode entry IDLE Mode Time	--5		-	μs
T_{Ptol}	From chip POWER DOWN Mode entry IDLE Mode Time	- 900		-	μs
T_{AFEset}	RF front-end chip enable setup time after transmitting or receiving	- 250		-	μs
T_{TxtoRx}	After completion of the chip is switched to send packets received ACK RF front-end state setup time (ACK Enable)	- 250		-	μs
T_{RxtoTx}	After completion of the chip is switched to receive data packets transmitted ACK RF front-end state setup time (ACK Enable)	- 250		-	μs