

Digital Design and Computer Organization Lab

WEEK 2

1 Sept 2021

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Q1) Full Adder

b.v file:

```
module invert(input wire i, output wire o1);
    assign o1 = !i;
endmodule

module and2(input wire i0, i1, output wire o2);
    assign o2 = i0 & i1;
endmodule

module or2(input wire i0, i1, output wire o3);
    assign o3 = i0 | i1;
endmodule

module xor2(input wire i0, i1, output wire o4);
    assign o4 = i0 ^ i1;
endmodule

module nand2(input wire i0, i1, output wire o5);
    wire t;
    and2 and2_0 (i0, i1, t);
    invert invert_0 (t, o5);
endmodule
```

c.v file:

```
module fulladd(input wire a, b, cin, output wire sum, cout);
    wire [4:0] t;

    xor2 x0(a, b, t[0]);
    xor2 x1(t[0], cin, sum);

    and2 a0(a, b, t[1]);
    and2 a1(a, cin, t[2]);
    and2 a2(b, cin, t[3]);

    or2 o0(t[1], t[2], t[4]);
    or2 o1(t[3], t[4], cout);
endmodule
```

c1testbench.v:

```
module TB;
  reg aa,bb,cc;
  wire ss,cy;
  fulladd add1(.a(aa), .b(bb), .cin(cc), .sum(ss), .cout(cy));
  initial
  begin
    $dumpfile("dump.vcd");
    $dumpvars(0, TB);
  end

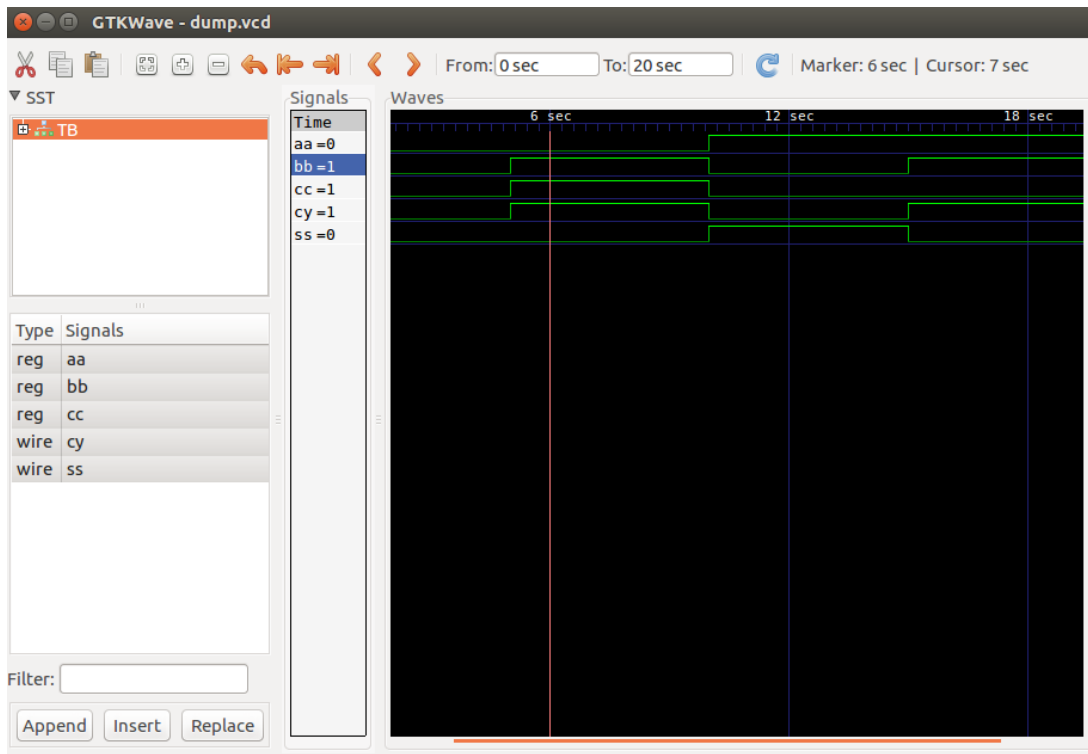
  initial begin $monitor(aa,bb,cc,ss,cy);
    aa = 1'b0;
    bb = 1'b0;
    cc=1'b0;
    #5
    aa = 1'b0;
    bb = 1'b1;
    cc=1'b1;
    #5
    aa = 1'b1;
    bb = 1'b0;
    cc=1'b0;
    #5
    aa = 1'b1;
    bb = 1'b1;
    cc=1'b0;
    #5
    aa = 1'b0;
    bb = 1'b0;
    cc=1'b1;
  end
endmodule
```

Output:

```
student@pessat196: ~/Desktop/PES1UG20CS484/Lab2
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ iverilog -o aout b.v c.v c1testb
ench.v
c1testbench.v: No such file or directory
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ iverilog -o aout b.v c.v c1testB
ench.v
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ vvp aout
VCD info: dumpfile dump.vcd opened for output.
00000
01101
10010
11001
00110
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ gtkwave dump.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[20] end time.
```



Q2) Ripple Carry Adder

d1.v file:

```
module invert(input wire i, output wire o1);
    assign o1 = !i;
endmodule

module and2(input wire i0, i1, output wire o2);
    assign o2 = i0 & i1;
endmodule

module or2(input wire i0, i1, output wire o3);
    assign o3 = i0 | i1;
endmodule

module xor2(input wire i0, i1, output wire o4);
    assign o4 = i0 ^ i1;
endmodule

module nand2(input wire i0, i1, output wire o5);
    wire t;
    and2 and2_0 (i0, i1, t);
    invert invert_0 (t, o5);
endmodule

//Module full adder.
module fulladd(input wire a, b, cin, output wire sum, cout);
    wire [4:0] t;
    xor2 x0(a, b, t[0]);
    xor2 x1(t[0], cin, sum);

    and2 a0(a, b, t[1]);
    and2 a1(a, cin, t[2]);
    and2 a2(b, cin, t[3]);

    or2 o0(t[1], t[2], t[4]);
    or2 o1(t[3], t[4], cout);
endmodule
```

d2.v file:

```
module fulladdR(input wire [3:0] a, b, input wire cin, output wire [3:0] sum, output wire cout);
// Instantiate full adder modules here.
wire [2:0] c;

fulladd F1(a[0],b[0],cin,sum[0],c[0]);
fulladd F2(a[1],b[1],c[0],sum[1],c[1]);
fulladd F3(a[2],b[2],c[1],sum[2],c[2]);
fulladd F4(a[3],b[3],c[2],sum[3],cout);

endmodule
```

dtestbench.v file:

```
`timescale 1 ns / 100 ps
`define TESTVECS 8

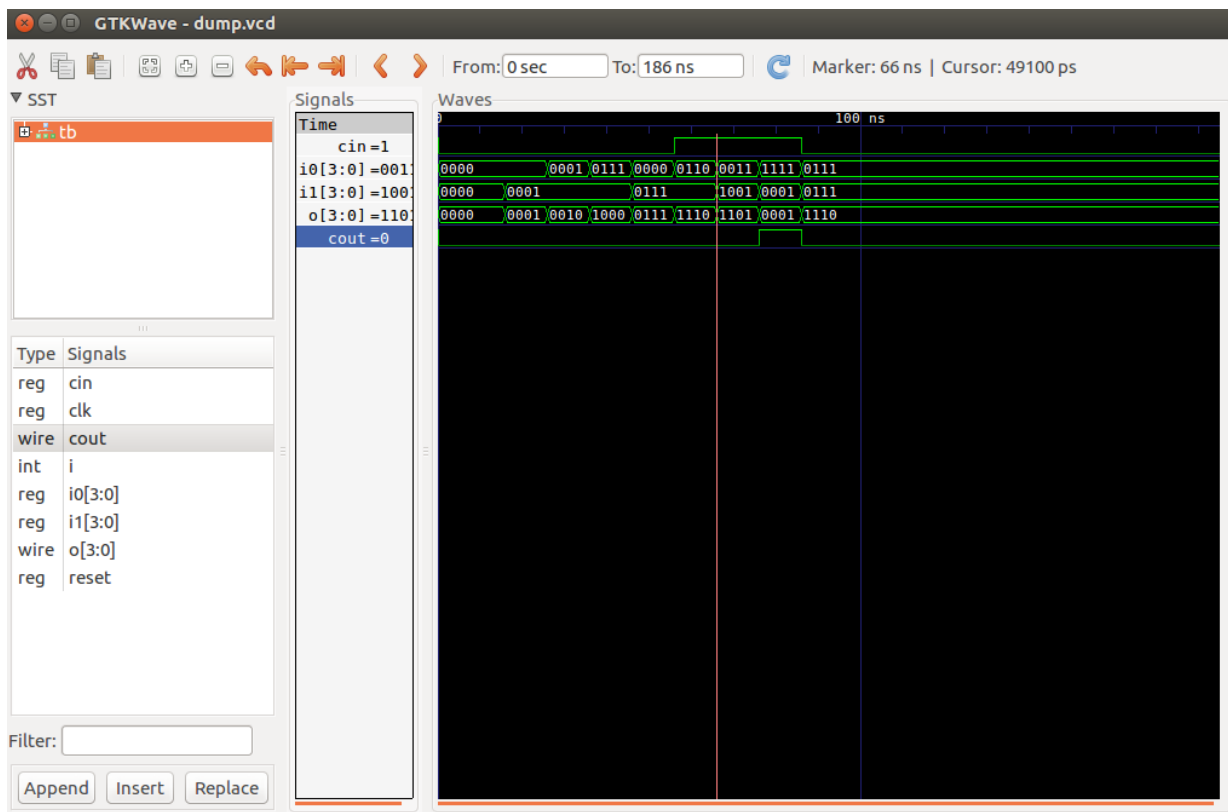
module tb;
    reg clk, reset;
    reg [3:0] i0, i1; reg cin;
    wire [3:0] o; wire cout;
    reg [8:0] test_vecs [0:(`TESTVECS-1)];
    integer i;
    initial begin $dumpfile("dump.vcd");
    $dumpvars(0,tb);
    end
    initial begin reset = 1'b1; #12.5 reset = 1'b0; end
    initial clk = 1'b0; always #5 clk =~ clk;
    initial begin
        test_vecs[0] = 9'b000000010;
        test_vecs[1] = 9'b000100010;
        test_vecs[2] = 9'b011100010;
        test_vecs[3] = 9'b000001110;
        test_vecs[4] = 9'b011001111;
        test_vecs[5] = 9'b001110011;
        test_vecs[6] = 9'b111100011;
        test_vecs[7] = 9'b011101110;
    end
    initial {i0, i1, cin, i} = 0;
    fulladdR u0 (i0, i1, cin, o, cout);
    initial begin
        #6 for(i=0;i<`TESTVECS;i=i+1)
            begin #10 {i0, i1, cin}=test_vecs[i]; end
        #100 $finish;
    end
endmodule
```

Output:

```
student@pessat196: ~/Desktop/PES1UG20CS484/Lab2
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ iverilog -o aout d1.v d2.v dtest
bench.v
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ vvp aout
VCD info: dumpfile dump.vcd opened for output.
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ gtkwave dump.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[186] end time.
```



Q3) 2 to 1 MUX

MUX2to1.v file:

```
module mux2(input wire i0,i1,j, output wire o);
    assign o = (j==0)?i0:i1;
endmodule
```

testBench2to1.v file:

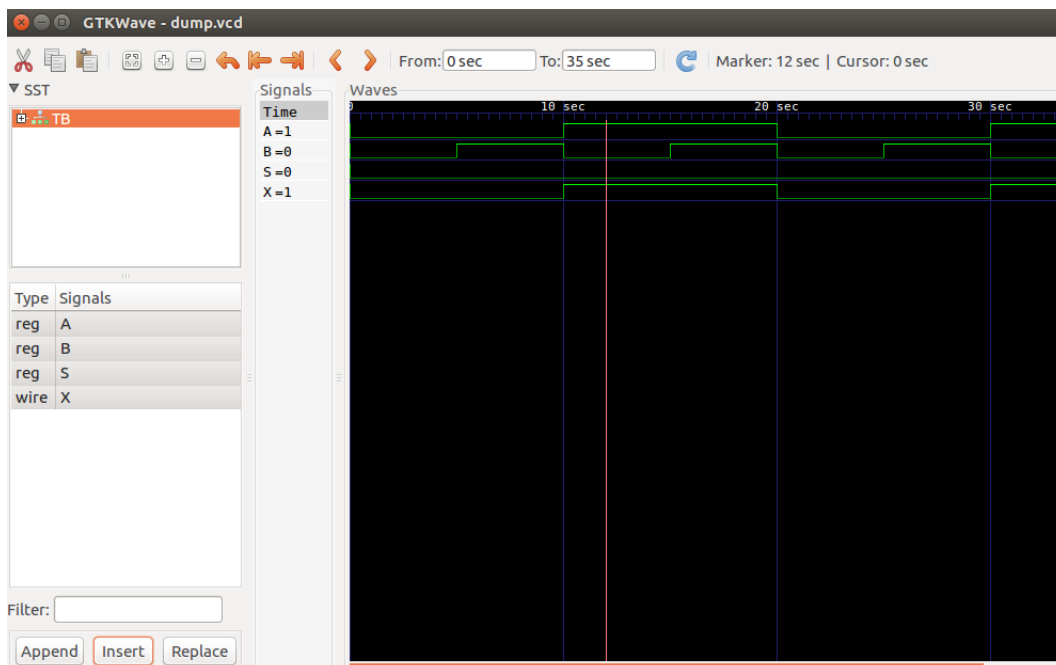
```
module TB;
    reg A,B,S;
    wire X;
    initial
    begin
        $dumpfile("dump.vcd");
        $dumpvars(0,TB);
    end
    mux2 newMUX(.i0(A), .i1(B), .j(S), .o(X));
    initial
    begin
        S = 1'b0;
        A = 1'b0;
        B = 1'b0;
        #5
        A = 1'b0;
        B = 1'b1;
        #5
        A = 1'b1;
        B = 1'b0;
        #5
        A = 1'b1;
        B = 1'b1;
        #5
        S = 1'b0;
        A = 1'b0;
        B = 1'b0;
        #5
        A = 1'b0;
        B = 1'b1;
        #5
        A = 1'b1;
        B = 1'b0;
        #5
        A = 1'b1;
        B = 1'b1;
        end
    endmodule
```

Output:

```
student@pessat196: ~/Desktop/PES1UG20CS484/Lab2
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ iverilog -o aout MUX2to1.v testBench2to1.v
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ vvp aout
VCD info: dumpfile dump.vcd opened for output.
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ gtkwave dump.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[35] end time.
```



Q3) 4 to 1 MUX

MUX2to1.v

```
module mux2(input wire i0,i1,j, output wire o);
    assign o = (j==0)?i0:i1;
endmodule
```

MUX4to1.v

```
module mux4 (input wire [0:3] i, input wire j1, j0, output wire o);
    wire t0, t1;
    mux2 m1(i[0],i[1],j0,t0);
    mux2 m2(i[2],i[3],j0,t1);
    mux2 m3(t0,t1,j1,o);

endmodule
```

testBench4to1.v

```
module TB;
reg [0:3]ii;
reg s0;
reg s1;
wire yy;
initial
begin
$dumpfile("dump.vcd");
$dumpvars(0, TB);
end
mux4 newMUX(.i(ii), .j0(s0),.j1(s1),.o(yy));
initial
begin
ii = 4'b0001;
s0=1'b0;
s1=1'b0;
#5
ii = 4'b1000;
#5
ii = 4'b0001;
s0=1'b1;
s1=1'b1;
#5
ii = 4'b0000;
s0=1'b1;
s1=1'b0;
end
endmodule
```

Output:

```
student@pessat196: ~/Desktop/PES1UG20CS484/Lab2
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ iverilog -o aout MUX4to1.v testB
ench4to1.v
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ vvp aout
VCD info: dumpfile dump.vcd opened for output.
student@pessat196:~/Desktop/PES1UG20CS484/Lab2$ gtkwave dump.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[15] end time.
```

