Digital Design and Computer Organization Lab

WEEK 1

25 Aug 2021

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(Performed on own laptop due to technical issues in lab)

Q1) AND and OR gates

a.v file

```
module and1(input wire a,b,output wire x, y);
assign y=a&b;
assign x=a|b;
endmodule
```

atestbench.v file

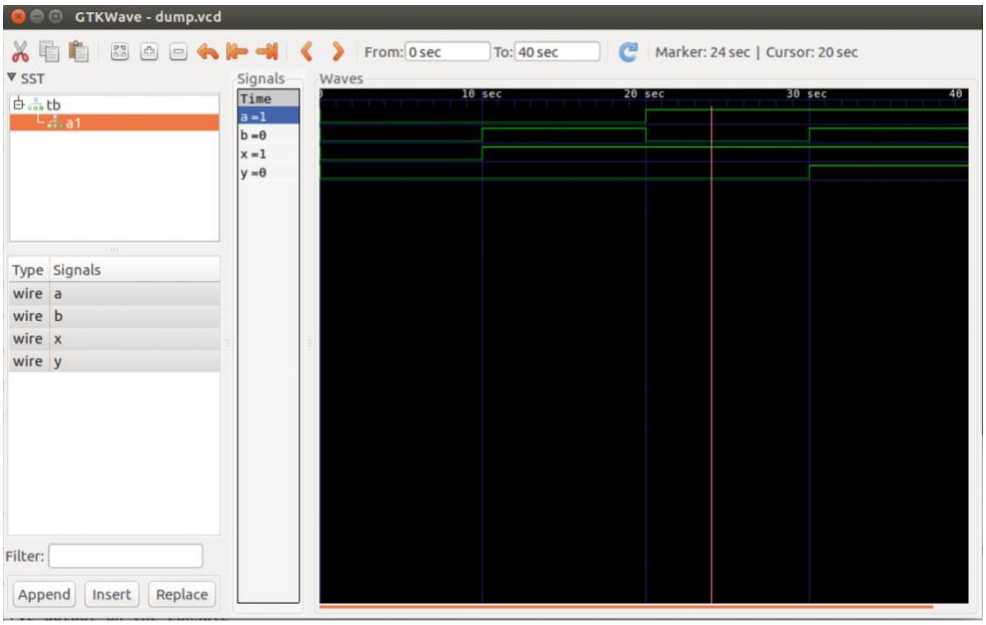
```
module tb;
reg t_a;
reg t_b;
wire t_x,t_y;
//instatiate
and1 a1(.a(t_a),.b(t_b),.y(t_x),.x(t_y));
initial begin $dumpfile("dump.vcd");
$dumpvars(0,tb);
end
initial begin $monitor(t_a,t_b,t_x,t_y); //displays the content of the register
t_a=1'b0;//1 bit input
t_b=1'b0;
#10 //time nanosecs
t_a=1'b0;//1 bit input
t_b=1'b1;
#10 //time nanosecs
t_a=1'b1;//1 bit input
t_b=1'b0;
#10 //time nanosecs
t_a=1'b1;//1 bit input
t_b=1'b1;
#10 //time nanosecs
t_a=0;//inorder to see the last input
t_b=0;
end
endmodule
```

Output:

```
student@pessat196: ~/Desktop/PES1UG20CS484/Lab1
student@pessat196:~/Desktop/PES1UG20CS484/Lab1$ iverilog -o aout a.v atestbench.
v
student@pessat196:~/Desktop/PES1UG20CS484/Lab1$ vvp aout
VCD info: dumpfile dump.vcd opened for output.
0000
0101
1001
1111
0000
student@pessat196:~/Desktop/PES1UG20CS484/Lab1$ gtkwave dump.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[40] end time.
```



Q2) XOR and NAND gates

b.v file

```
module invert(input wire i, output wire o1);
    assign o1 = !i;
endmodule

module and2(input wire i0, i1, output wire o2);
    assign o2 = i0 & i1;
endmodule

module or2(input wire i0, i1, output wire o3);
    assign o3 = i0 | i1;
endmodule

module xor2(input wire i0, i1, output wire o4);
    assign o4 = i0 ^ i1;
endmodule

module nand2(input wire i0, i1, output wire o5);
    assign o5 = !(i0&i1);
endmodule
```

btestbench.v file

```
module tb;
reg t_a;
reg t_b;
wire P,Q,R,S,T;
//instantiate
invert a1(.i(t_a),.o1(P));
and2 a2(.i0(t_a),.i1(t_b),.o2(Q));
or2 a3(.i0(t_a),.i1(t_b),.o3(R));
xor2 a4(.i0(t_a),.i1(t_b),.o4(S));
nand2 a5(.i0(t_a),.i1(t_b),.o5(T));
initial begin $dumpfile("dmp1.vcd");
$dumpvars(0,tb);
end
initial begin $monitor(t_a,t_b,P,Q,R,S,T); //displays the content of the register
t_a=1'b0;//1 bit input
t_b=1'b0;
#10 //time nanosecs
t_a=1'b0;//1 bit input
t_b=1'b1;
#10 //time nanosecs
t_a=1'b1;//1 bit input
t_b=1'b0;
#10 //time nanosecs
t_a=1'b1;//1 bit input
t_b=1'b1;
#10 //time nanosecs
t_a=0;//inorder to see the last input
t_b=0;
end
endmodule
```

Output:

```
student@pessat196: ~/Desktop/PES1UG20CS484/Lab1
student@pessat196:~/Desktop/PES1UG20CS484/Lab1$ iverilog -o aout b.v btestbench.
v
student@pessat196:~/Desktop/PES1UG20CS484/Lab1$ vvp aout
VCD info: dumpfile dmp1.vcd opened for output.
0010001
0110111
1000111
1101100
0010001
student@pessat196:~/Desktop/PES1UG20CS484/Lab1$ gtkwave dump.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[40] end time.
```