**Digital Design and Computer Organization Lab**

**WEEK 7**

**27 Oct 2021**

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| Vanshika Goel | **PES1UG20CS484** | H Section | Roll No: 40 |

**Implementation of Control Unit**

**Input:**

module ir (input wire clk, reset, load, input wire [15:0] din, output wire [15:0] dout);

dfrl dfrl\_0 (clk, reset, load, din['h0], dout['h0]);

dfrl dfrl\_1 (clk, reset, load, din['h1], dout['h1]);

dfrl dfrl\_2 (clk, reset, load, din['h2], dout['h2]);

dfrl dfrl\_3 (clk, reset, load, din['h3], dout['h3]);

dfrl dfrl\_4 (clk, reset, load, din['h4], dout['h4]);

dfrl dfrl\_5 (clk, reset, load, din['h5], dout['h5]);

dfrl dfrl\_6 (clk, reset, load, din['h6], dout['h6]);

dfrl dfrl\_7 (clk, reset, load, din['h7], dout['h7]);

dfrl dfrl\_8 (clk, reset, load, din['h8], dout['h8]);

dfrl dfrl\_9 (clk, reset, load, din['h9], dout['h9]);

dfrl dfrl\_a (clk, reset, load, din['ha], dout['ha]);

dfrl dfrl\_b (clk, reset, load, din['hb], dout['hb]);

dfrl dfrl\_c (clk, reset, load, din['hc], dout['hc]);

dfrl dfrl\_d (clk, reset, load, din['hd], dout['hd]);

dfrl dfrl\_e (clk, reset, load, din['he], dout['he]);

dfrl dfrl\_f (clk, reset, load, din['hf], dout['hf]);

endmodule

module control\_logic (input wire clk, reset, input wire [15:0] cur\_ins, output wire [2:0] rd\_addr\_a, rd\_addr\_b, wr\_addr, output wire [1:0] op, output wire pc\_inc, load\_ir, wr\_reg);

assign rd\_addr\_a[0] = cur\_ins[0];

assign rd\_addr\_a[1] = cur\_ins[1];

assign rd\_addr\_a[2] = cur\_ins[2];

assign rd\_addr\_b[0] = cur\_ins[3];

assign rd\_addr\_b[1] = cur\_ins[4];

assign rd\_addr\_b[2] = cur\_ins[5];

assign wr\_addr[0] = cur\_ins[6];

assign wr\_addr[1] = cur\_ins[7];

assign wr\_addr[2] = cur\_ins[8];

assign op[0] = cur\_ins[9];

assign op[1] = cur\_ins[10];

wire t1,t2,t3;

or3 o1(cur\_ins[11],cur\_ins[12],cur\_ins[13],t1);

or3 o2(cur\_ins[14],cur\_ins[15],t1,t2);

invert o3(t2,t3);

dfsl g1(clk,reset,1'b1,pc\_inc,load\_ir);

dfrl g2(clk,reset,1'b1,load\_ir,pc\_inc);

and2 o4(pc\_inc, t3,wr\_reg);

endmodule

module mproc (input wire clk, reset, input wire [15:0] ins, output wire [15:0] addr);

wire pc\_inc, cout; wire [2:0] rd\_addr\_a, rd\_addr\_b, wr\_addr; wire [1:0] op; wire [15:0] cur\_ins, d\_out\_a, d\_out\_b;

pc pc\_0 (clk, reset, pc\_inc, 1'b0, 1'b0, 16'b0, addr);

ir ir\_0 (clk, reset, load\_ir, ins, cur\_ins);

control\_logic control\_logic\_0 (clk, reset, cur\_ins, rd\_addr\_a, rd\_addr\_b, wr\_addr, op, pc\_inc, load\_ir, wr\_reg);

reg\_alu reg\_alu\_0 (clk, reset, 1'b1, wr\_reg, op, rd\_addr\_a, rd\_addr\_b, wr\_addr, 16'b0, d\_out\_a, d\_out\_b, cout);

endmodule

**Output:**

**Text

Description automatically generated**

**Graphical user interface

Description automatically generated**