CSE 100/L Logic Design
Fall 2025

Lab Assignment 1

Code Submission deadlines:

- 100% Before the end of your section Thursday, October 2nd.
- 95% after the end of your section until 11:59 PM Thursday, October 2nd.
- 80% after 11:59PM Thursday, October 2nd.
- 60% after 11:59PM Sunday, October 5th.
- 40% after 11:59PM Monday, October 6th.
- 20% after 11:59PM Tuesday, October 7th.
- 0% after 11:59PM Wednesday, October 8th.

Demo deadline:

- Code may be demonstrated until the end of the next lab assignment. You must submit before you demo, and the code you submit must be the code you demo. You may be required to download the code from Canvas to demo.

Write-Up deadline:

- There is no write-up submission for this lab assignment.

Academic Integrity Policy:

The Academic Integrity Policy is stated in the syllabus on Canvas. Students are responsible for reading the syllabus. Not reading the syllabus is not an excuse for academic misconduct.

- Work submitted in CSE 100 must be yours alone. Sharing/sending code, submitting code written by others, and submitting (any) code from generative AI **are all violations of academic integrity**.
- Working together on a whiteboard, on paper, debugging waveforms, explaining concepts and/or examples, is encouraged, **as long as no solution code is shared**.

Verilog Operator Constraints:

In this lab you can use any of the following combinational operators:

- All combinational logic must be implemented using only `assign` statements.
- Bit-wise Operators: &, |, $\sim$, $\wedge$, and $\sim \wedge$
- Concatenation and Replication: {} and {{}}

All other operators will be considered behavioral and will result in a **score of 0**!

Overview

You should have already completed the prelab tutorial before proceeding with this lab assignment. In this lab, you will display an octal digit on the rightmost digit of the 7-segment display of the Basys 3 board. The octal digit will correspond to the rightmost three switches. A pushbutton will provide the value of DP (the decimal point).

Procedure

1. Read about the 7-Segment Displays in the Basys3 Board Reference Manual. The FPGA pin names used for the 7-segment display controls in this manual are **CA**, **CB**, **CC**, **CD**, **CE**, **CF**, **CG**, **DP**, **AN3**, **AN2**, **AN1**, and **AN0**

2. From the prelab you should have equations for the 7-segment controls **CA**, **CB**, **CC**, **CD**, **CE**, **CF**, and **CG**. Figure out what the values should be for **AN3**, **AN2**, **AN1**, and **AN0**.

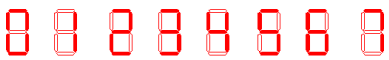

Figure 1: Octal digit on a 7-segment display.

1. Follow these steps to create a project. If you are working on a lab computer, **make sure the project is created on the desktop.**

2. Follow the steps below to enter and implement your design. For this project, your

   inputs should be: **d2,d1,d0, btnD**

   outputs should be: **CA, CB, CC, CD, CE, CF, CG, DP, AN3, AN2, AN1,** and **AN0**

   (a) Using the equations you obtained in the pre-lab, add assign statements to your module for

   CA, CB, CC, CD, CE, CF, and **CG**

   Then, add:

   ```
   assign DP = btnD;
   ```

   and assign statements for **AN3**, **AN2**, **AN1**, and **AN0**.

   (b) As described in the "Entering and Implementing a Design in Vivado Tutorial" on Canvas, you will need to modify the constraints file Basys3_Master.xdc to edit the pin names so that they match the inputs/outputs of your module. There are two lines for each pin. Uncomment the lines for the pins used in this project and replace the pin name with the corresponding input/output name in your module according to the tables below.

Input	btnD	d0	d1	d2
PIN	btnD	sw[0]	sw[1]	sw[2]

Table 1: Design input pins.

Output	CA	CB	CC	CD	CE	CF	CG	DP	AN0	AN1	AN2	AN3
PIN	seg[0]	seg[1]	seg[2]	seg[3]	seg[4]	seg[5]	seg[6]	dp	an[0]	an[1]	an[2]	an[3]

Table 2: Design output pins.

(c) Implement your design as described in steps. There may be an error that you need to fix. Check the console window. When it successfully generates the bitfile, do not select "Open Implemented Design".

3. Download the bitfile to the Basys3 board by following the same steps as in the Prelab (but if you already have Vivado open you can just open the Hardware Manager). The bit file will have the same name as your top level module (top_module.bit).

4. ***Demonstrate your design to the TA. Ahead of your demonstration, make sure that all combinations of d2,d1,d0, and btnD result in the correct 7-segment output. The TA will verify that the output of your design is valid under arbitrary input combinations.***

5. Archive your project by following the "Archiving your Vivado Project" tutorial in Canvas. Files left on the PC are not protected. Should it become necessary to re-image that PC, its disks will be wiped clean.

6. ***Submit your archived project on canvas to the "Lab Assignment 1: Demo and Code Submission" assignment. The code contained in your archive submission must be the same code that was used for demonstration credit.***

7. **Important** Please remember to turn off the Basys3 board when you are done.

Rubric

There is no partial credit for this lab. All students must completely satisfy the lab description, as many components are used in later labs.