VIT®

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ASIC DESIGN LAB – MVLD505P

SLOT: L33+L34

DIGITAL ASSIGNMENT -2

Synthesis of Digital Architecture

SUBMITTED BY:

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Aim:

The objective of this work is to perform logical synthesis on an RTL design, optimize it for timing, power, and area constraints, and generate a gate-level netlist that meets the design specifications.

TOOLS USED:

Synopsys Design Compiler

Technology Library

Linux Environment – For running scripts and managing design files

For every synthesis, one **SDC** file and one **TCL** file are required, and it generates a **netlist** and updated **SDC** files.

First, enable the **dc-shell** file using the command

dc_shell –topo

source the **TCL** file with the command

source <file_name>.

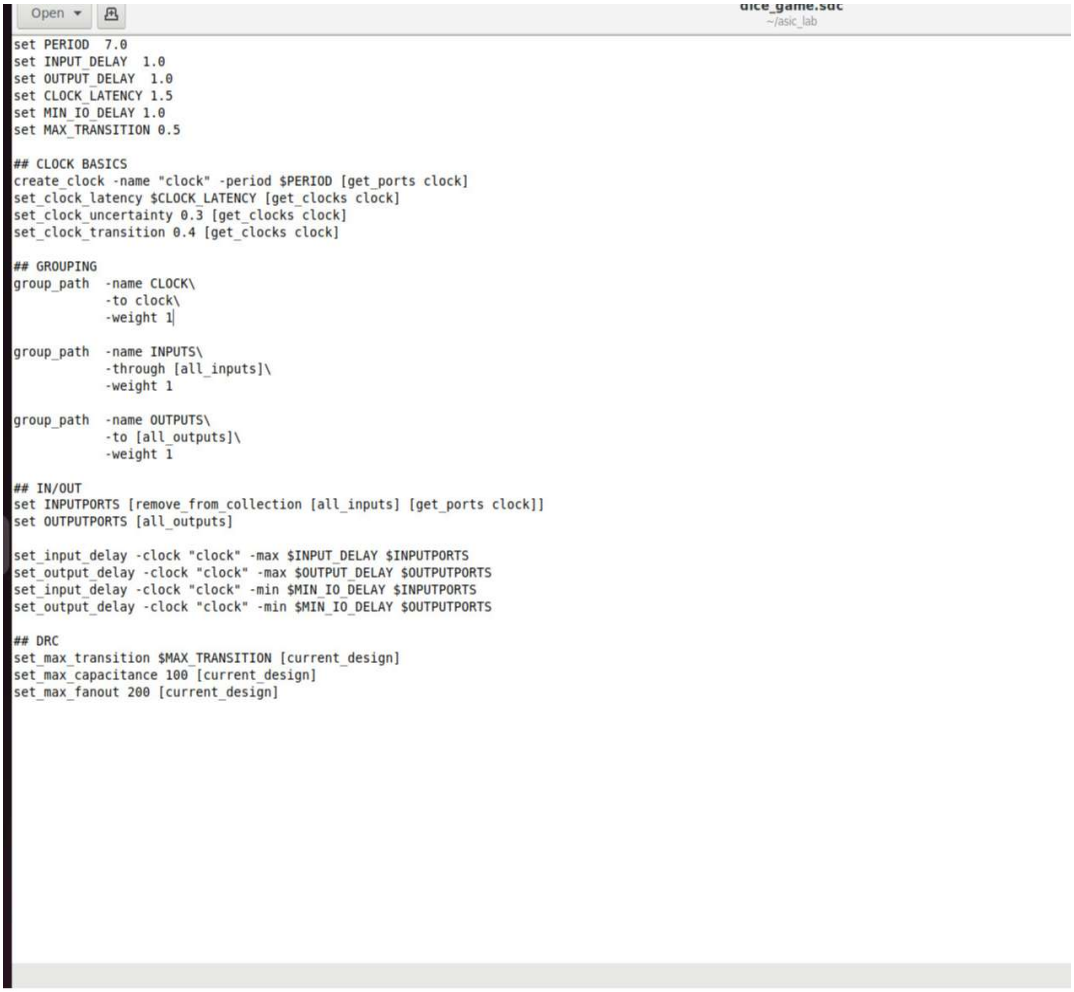
report_timing→to get timing analysis

report_area→to get area details

report_power → to get power analysis

1. LOGICAL SYNTHESIS

.sdc file




```
set PERIOD  7.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.5
set MIN_IO_DELAY 1.0
set MAX_TRANSITION 0.5

## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports clock]
set_clock_latency $CLOCK_LATENCY [get_clocks clock]
set_clock_uncertainty 0.3 [get_clocks clock]
set_clock_transition 0.4 [get_clocks clock]

## GROUPING
group_path  -name CLOCK\
            -to clock\
            -weight 1

group_path  -name INPUTS\
            -through [all_inputs]\
            -weight 1

group_path  -name OUTPUTS\
            -to [all_outputs]\
            -weight 1

## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

## DRC
set_max_transition $MAX_TRANSITION [current_design]
set_max_capacitance 100 [current_design]
set_max_fanout 200 [current_design]
```

- **.tcl file**

Open dice_game.tcl

```
set_host_options -max_cores 4

#source ../../../common_setup.tcl

set DESIGN_REF_PATH "/home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/"

set LINK_LIBRARY_FILES    "* \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_tt0p8v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ss0p72v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ff0p88v25c.db"


set TARGET_LIBRARY_FILES   "\
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_tt0p8v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ss0p72v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ff0p88v25c.db"


set link_library  $LINK_LIBRARY_FILES
set target_library $TARGET_LIBRARY_FILES


#set_app_var search_path "$SEARCH_PATH"
#set_app_var target_library "$TARGET_LIBRARY_FILES"
#set_app_var link_library " $LINK_LIBRARY_FILES "

# SET DONT USE ############################################################
#set_dont_use [get_lib_cells -quiet */SAEDRVT14_AO21_U_0P5]

analyze -library WORK -format verilog {./dice_game.v}

read_file -format verilog {./dice_game.v}

# check design quality
check_design

link

source -echo ./dice_game.sdc

check_timing

set auto_wire_load_selection false
set_wire_load_model -name "8000"
set_wire_load_mode top
```

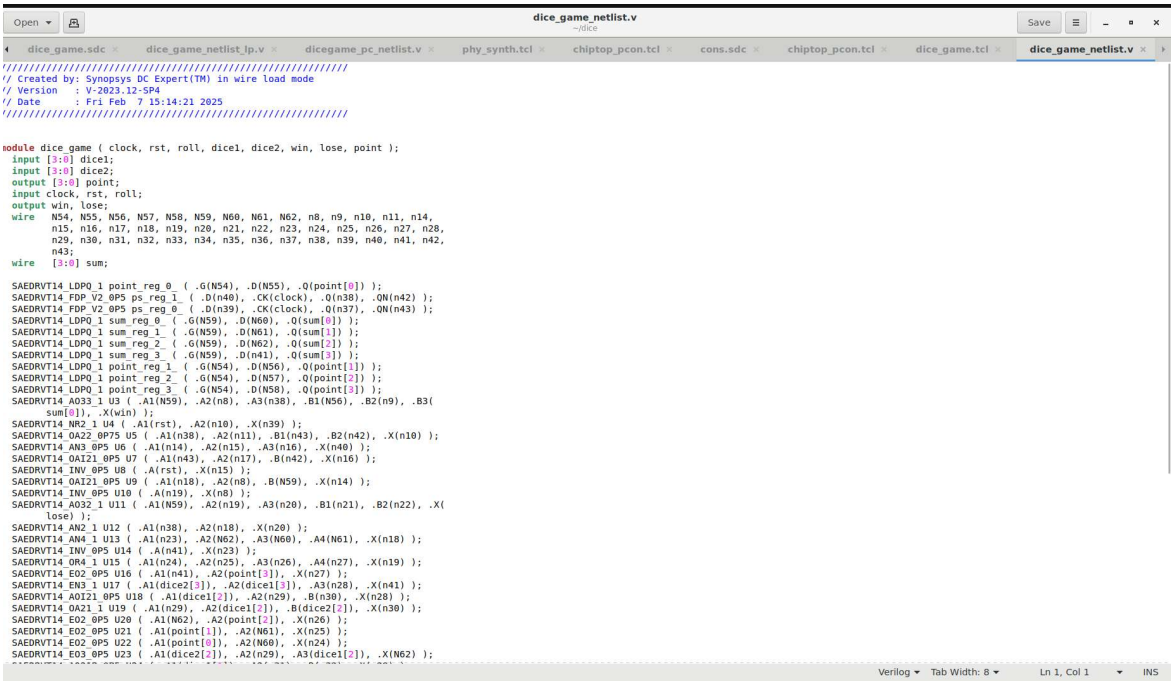
Open

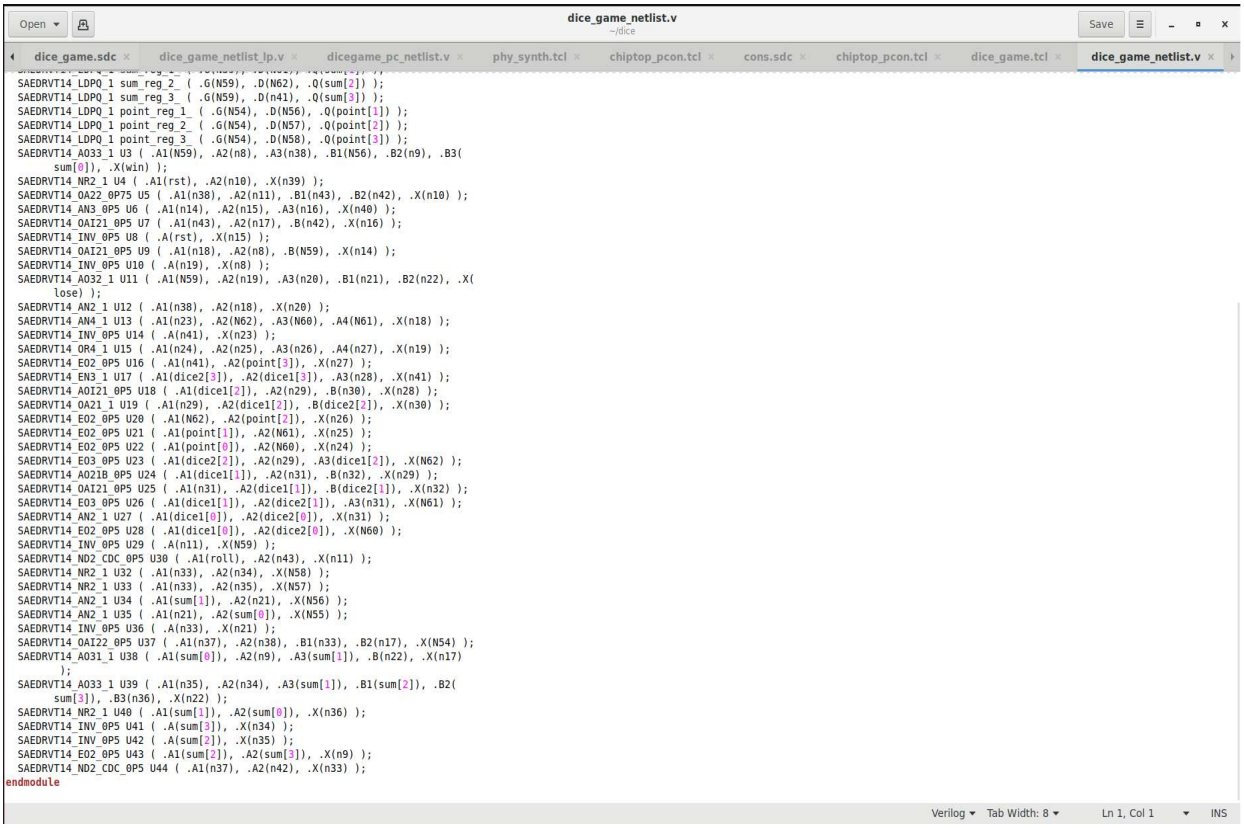
dice_game.tcl
~/asic_lab

dice_game.tcl | phy_synth.tcl | dicegame_

```
# SET DONT USE ###########################################################
#set_dont_use [get_lib_cells -quiet */SAEDRVT14_AO21_U_0P5]

analyze -library WORK -format verilog {./dice_game.v}

read_file -format verilog {./dice_game.v}

# check design quality
check_design

link

source -echo ./dice_game.sdc

check_timing

set auto_wire_load_selection false
set_wire_load_model -name "8000"
set_wire_load_mode top

#set_clock_gating_registers -include_instances [remove_from_collection  [all_registers -clock clock] [get_cells "MemYHier/MemXb MemYHier/MemXa MemXHier/MemXb MemXHier/MemXa"]]

set_operating_conditions -min ff0p88v25c -max ss0p72v25c


set_fix_multiple_port_nets -all -buffer_constants [get_designs ChipTop]


compile -exact_map -gate_clock

change_names -rules verilog -verbose -hier
report_clock_gating


#set_fix_hold [all_clocks]
#report_constraints  -min_delay
#compile -incremental -only_design

##########reports#########################
report_area
report_timing
report_power


write -f verilog -h -out   ./reports/dice_game_netlist.v
write -f ddc -h -out       ./reports/dice_game.ddc
write_sdc ./reports/dice_game.sdc
```

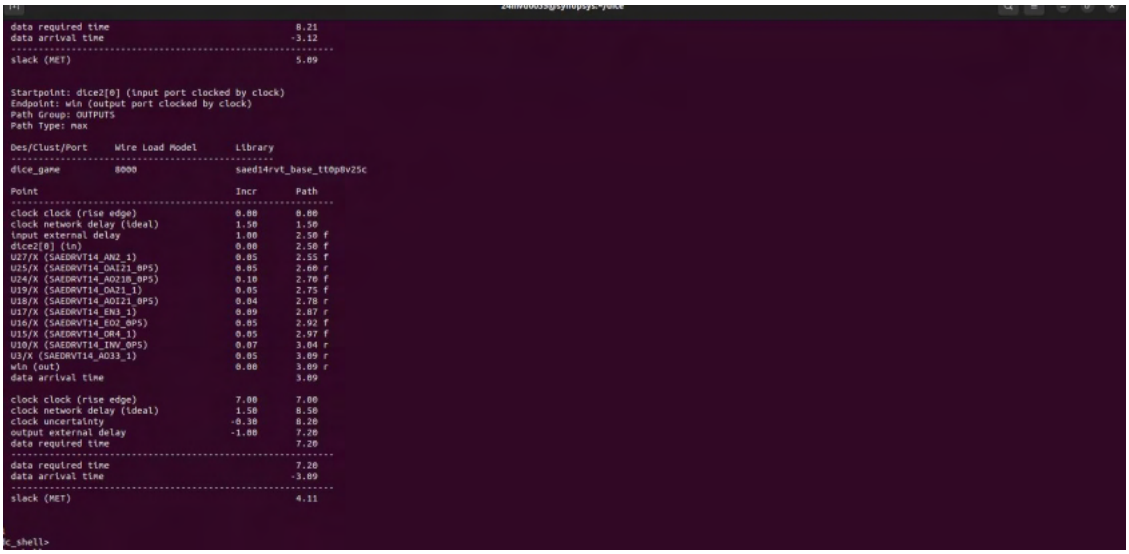
- **Generated netlist file (.v)**





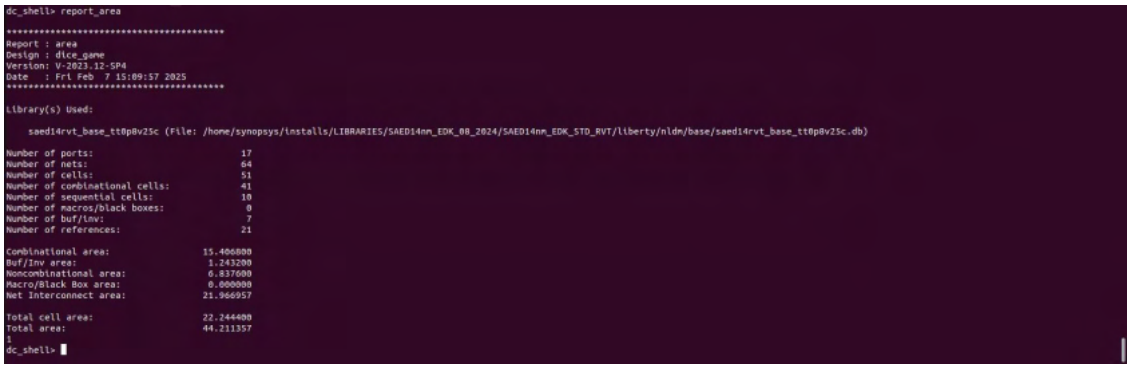
REPORTS:

Timing report:



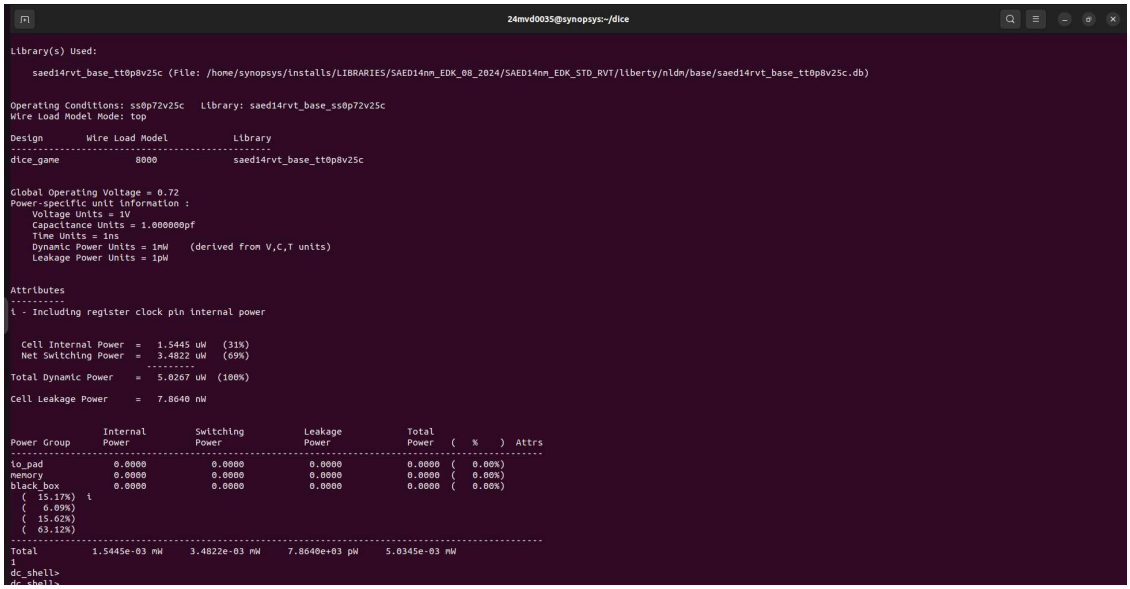
```
data required time                                 8.21
data arrival time                                 -3.12
---------------------------------------------------------
slack (MET)                                        5.09


Startpoint: dice2[0] (input port clocked by clock)
Endpoint: win (output port clocked by clock)
Path Group: OUTPUTS
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
dice_game          8000                  saed14rvt_base_tt0p8v25c

Point                                    Incr       Path
---------------------------------------------------------
clock clock (rise edge)                  0.00       0.00
clock network delay (ideal)              1.50       1.50
input external delay                     1.00       2.50 f
dice2[0] (in)                            0.00       2.50 f
U27/X (SAEDRVT14_AN2_1)                  0.05       2.55 f
U25/X (SAEDRVT14_OAI21_0P5)              0.05       2.60 r
U24/X (SAEDRVT14_AOI18_0P5)              0.10       2.70 f
U19/X (SAEDRVT14_OA21_1)                 0.05       2.75 f
U18/X (SAEDRVT14_AOI21_0P5)              0.04       2.78 r
U17/X (SAEDRVT14_EN3_1)                  0.09       2.87 r
U16/X (SAEDRVT14_EOI_0P5)                0.05       2.92 f
U15/X (SAEDRVT14_OR4_1)                  0.05       2.97 f
U10/X (SAEDRVT14_INV_0P5)                0.07       3.04 r
U3/X (SAEDRVT14_AO33_1)                  0.05       3.09 r
win (out)                                0.00       3.09 r
data arrival time                                   3.09

clock clock (rise edge)                  7.00       7.00
clock network delay (ideal)              1.50       8.50
clock uncertainty                       -0.30       8.20
output external delay                   -1.00       7.20
data required time                                  7.20
---------------------------------------------------------
data required time                                  7.20
data arrival time                                  -3.09
---------------------------------------------------------
slack (MET)                                        4.11


dc_shell>
```

Area report:



```
dc_shell> report_area
****************************************
Report : area
Design : dice_game
Version: V-2023.12-SP4
Date   : Fri Feb  7 15:09:57 2025
****************************************

Library(s) Used:

    saed14rvt_base_tt0p8v25c (File: /home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db)

Number of ports:                           17
Number of nets:                            64
Number of cells:                           51
Number of combinational cells:             41
Number of sequential cells:                10
Number of macros/black boxes:               0
Number of buf/inv:                          7
Number of references:                      21

Combinational area:                15.466800
Buf/Inv area:                       1.243200
Noncombinational area:              6.837600
Macro/Black Box area:               0.000000
Net Interconnect area:             21.966957

Total cell area:                   22.244400
Total area:                        44.211357
1
dc_shell>
```

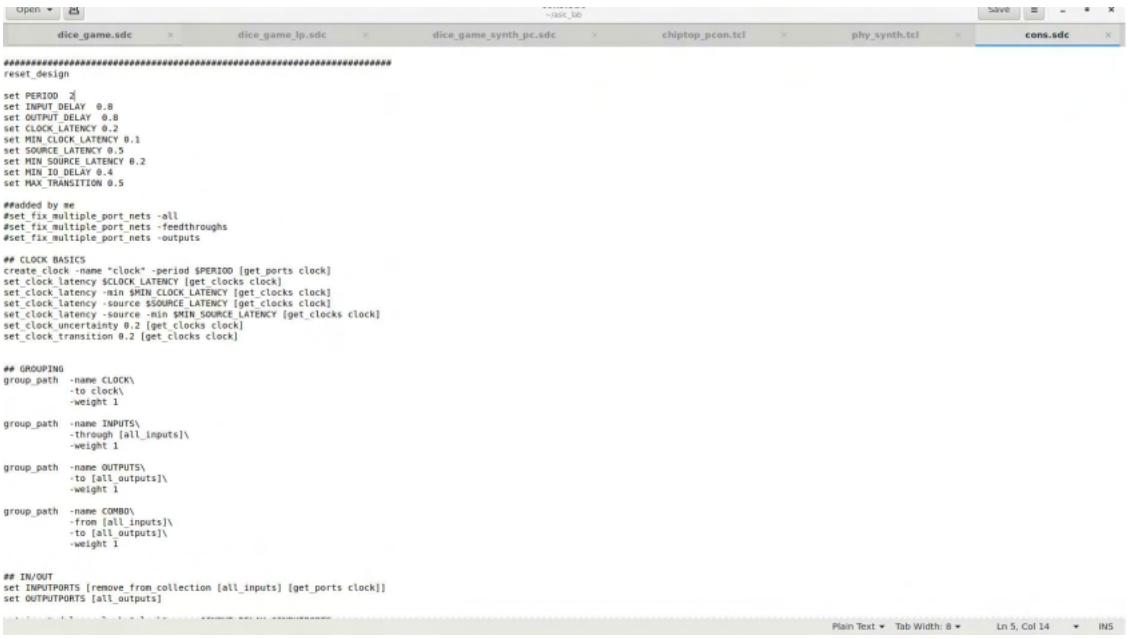
Power report:



```
24mvd0035@synopsys:~/dice

Library(s) Used:

    saed14rvt_base_tt0p8v25c (File: /home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db)


Operating Conditions: ss0p72v25c   Library: saed14rvt_base_ss0p72v25c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
dice_game             8000              saed14rvt_base_tt0p8v25c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1nW    (derived from V,C,T units)
    Leakage Power Units = 1pW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   1.5445 uW   (31%)
  Net Switching Power  =   3.4822 uW   (69%)
                         --------
Total Dynamic Power    =   5.0267 uW  (100%)

Cell Leakage Power     =   7.8640 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
  (  15.17%)  i
  (   6.09%)
  (  15.62%)
  (  63.12%)
--------------------------------------------------------------------------------------------------
Total          1.5445e-03 mW     3.4822e-03 mW     7.8640e+03 pW     5.0345e-03 mW
i
dc_shell>
dc_shell>
```

PHYSICAL SYNTHESIS

- **.sdc file**



dice_game.sdc | dice_game_lp.sdc | dice_game_synth_pc.sdc | chiptop_pcon.tcl | phy_synth.tcl | cons.sdc

```
##########################################################################
reset_design

set PERIOD  2
set INPUT_DELAY  0.8
set OUTPUT_DELAY  0.8
set CLOCK_LATENCY 0.2
set MIN_CLOCK_LATENCY 0.1
set SOURCE_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.2
set MIN_IO_DELAY 0.4
set MAX_TRANSITION 0.5

##added by me
#set_fix_multiple_port_nets -all
#set_fix_multiple_port_nets -feedthroughs
#set_fix_multiple_port_nets -outputs

## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports clock]
set_clock_latency $CLOCK_LATENCY [get_clocks clock]
set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]
set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]
set_clock_uncertainty 0.2 [get_clocks clock]
set_clock_transition 0.2 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
            -to clock\
            -weight 1

group_path  -name INPUTS\
            -through [all_inputs]\
            -weight 1

group_path  -name OUTPUTS\
            -to [all_outputs]\
            -weight 1

group_path  -name COMBO\
            -from [all_inputs]\
            -to [all_outputs]\
            -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports clock]]
set OUTPUTPORTS [all_outputs]
```

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```
## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

- **.tcl file**

Open

phy_synth.tcl
~/asic_lab

```
set_svf "ChipTop.svf"

## Point to the 32nm SAED libs
set DESIGN_REF_PATH "/home/synopsys/installs/LIBRARIES/ref"

set SEARCH_PATH      " \
${DESIGN_REF_PATH}/milkyway/saed32nm_lvt_1p9m \
${DESIGN_REF_PATH}/milkyway/saed32nm_hvt_1p9m \
${DESIGN_REF_PATH}/milkyway/saed32nm_rvt_1p9m \
${DESIGN_REF_PATH}/milkyway/saed32sram_lp "

set LINK_LIBRARY_FILES   "* \
${DESIGN_REF_PATH}/DBs/saed32hvt_ff1p16v125c.db \
${DESIGN_REF_PATH}/DBs/saed32hvt_ff1p16vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32rvt_ff1p16v125c.db \
${DESIGN_REF_PATH}/DBs/saed32rvt_ff1p16vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32lvt_ff1p16v125c.db \
${DESIGN_REF_PATH}/DBs/saed32lvt_ff1p16vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32hvt_ss0p75v125c.db \
${DESIGN_REF_PATH}/DBs/saed32hvt_ss0p75vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32rvt_ss0p75v125c.db \
${DESIGN_REF_PATH}/DBs/saed32rvt_ss0p75vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32lvt_ss0p75v125c.db \
${DESIGN_REF_PATH}/DBs/saed32lvt_ss0p75vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32sramlp_ff1p16v125c_i1p16v.db \
${DESIGN_REF_PATH}/DBs/saed32sramlp_ff1p16vn40c_i1p16v.db \
${DESIGN_REF_PATH}/DBs/saed32sramlp_ss0p75v125c_i0p75v.db \
${DESIGN_REF_PATH}/DBs/saed32sramlp_ss0p75vn40c_i0p75v.db "

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/DBs/saed32hvt_ff1p16v125c.db \
${DESIGN_REF_PATH}/DBs/saed32hvt_ff1p16vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32rvt_ff1p16v125c.db \
${DESIGN_REF_PATH}/DBs/saed32rvt_ff1p16vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32lvt_ff1p16v125c.db \
${DESIGN_REF_PATH}/DBs/saed32lvt_ff1p16vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32hvt_ss0p75v125c.db \
${DESIGN_REF_PATH}/DBs/saed32hvt_ss0p75vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32rvt_ss0p75v125c.db \
${DESIGN_REF_PATH}/DBs/saed32rvt_ss0p75vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32lvt_ss0p75v125c.db \
${DESIGN_REF_PATH}/DBs/saed32lvt_ss0p75vn40c.db \
${DESIGN_REF_PATH}/DBs/saed32sramlp_ff1p16v125c_i1p16v.db \
${DESIGN_REF_PATH}/DBs/saed32sramlp_ff1p16vn40c_i1p16v.db \
${DESIGN_REF_PATH}/DBs/saed32sramlp_ss0p75v125c_i0p75v.db \
${DESIGN_REF_PATH}/DBs/saed32sramlp_ss0p75vn40c_i0p75v.db "

##########################################################################################
# User-defined variables for physical library setup in dc_setup.tcl
##########################################################################################

set MW_DESIGN_LIB        MY_DESIGN_LIB    ;# User-defined Milkyway design library name
```

Open

phy_synth.tcl
~/asic_lab

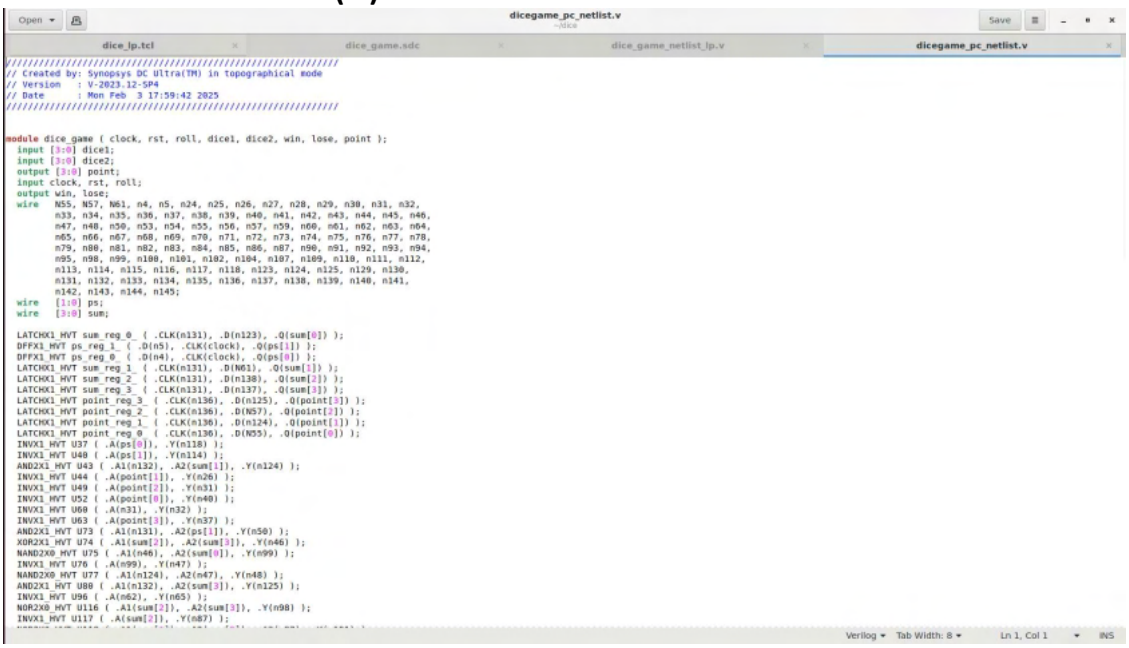
```
##############################################################################################

set MW_DESIGN_LIB        MY_DESIGN_LIB    ;# User-defined Milkyway design library name

# Milkyway reference libraries
set MW_REFERENCE_LIB_DIRS "${SEARCH_PATH} "

set TECH_FILE "${DESIGN_REF_PATH}/tech/saed32nm_1p9m.tf" ;#  Milkyway technology file

set TLUPLUS_MAX_FILE  "${DESIGN_REF_PATH}/tech/saed32nm_1p9m_Cmax.lv.tluplus" ;#Max TLUPlus file

set TLUPLUS_MIN_FILE  "${DESIGN_REF_PATH}/tech/saed32nm_1p9m_Cmin.lv.tluplus" ;#Min TLUPlus file

set MAP_FILE   "${DESIGN_REF_PATH}/tech/saed32nm_tf_itf_tluplus.map" ;#  Mapping file for TLUplus

##########################################################################
# Logical Library Settings
##########################################################################
set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "
##########################################################################
# Physical Library Settings
##########################################################################

set_app_var mw_reference_library $MW_REFERENCE_LIB_DIRS
set_app_var mw_design_library $MW_DESIGN_LIB

# create new Milkyway design library

#create_mw_lib   -technology $TECH_FILE \
#                     -mw_reference_library $mw_reference_library \
#                      $mw_design_library

# Only create new Milkyway design library if it doesn't already exist
    if {![file isdirectory $mw_design_library ]} {
      create_mw_lib   -technology $TECH_FILE \
                      -mw_reference_library $mw_reference_library \
                      -hier_separator {/} \
                      -bus_naming_style {[%d]} \
                      $mw_design_library
    } else {
# If Milkyway design library already exists, continue by opening the existing library
    }

open_mw_lib     $mw_design_library
check_library
set_tlu_plus_files -max_tluplus $TLUPLUS_MAX_FILE -min_tluplus $TLUPLUS_MIN_FILE \
-tech2itf_map $MAP_FILE

check_tlu_plus_files

analyze -library WORK -format verilog {./dice_game.v \

}
read_file -format verilog {./dice_game.v}
```

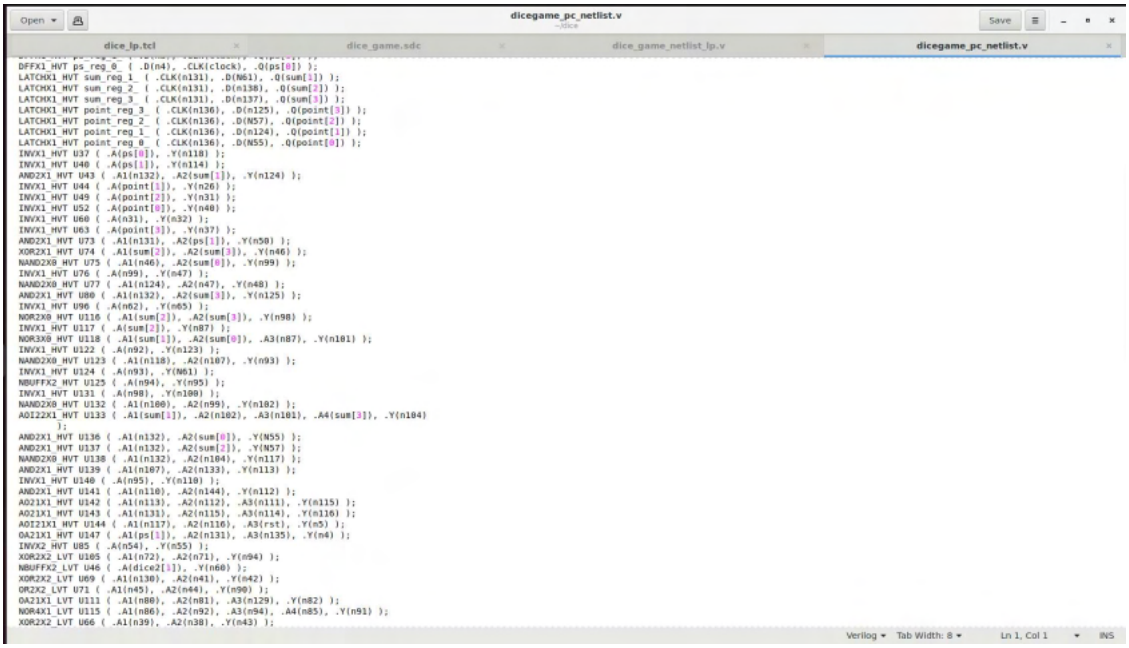
Open

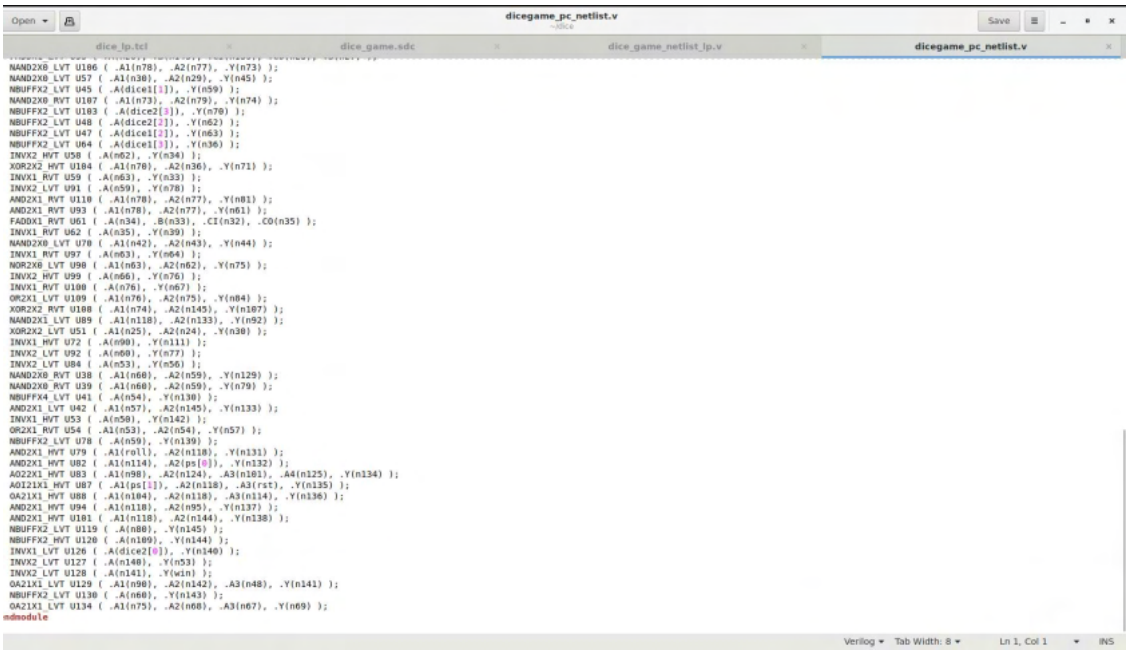
phy_synth.tcl
~/asic_lab

```
}
read_file -format verilog {./dice_game.v}

link
## Generating intermediate technology independet (GTECH) design ###########
write_file -format verilog -output ./dice_game_gtech.vs

# check design quality
check_design

source ./cons.sdc

check_timing

source ./chiptop_pcon.tcl
#extract_physical_constraints ./floorplan/floorplan.def

#set_operating_conditions ss0p95v125c
set_operating_conditions -max ss0p75v125c -min ff1p16vn40c


#set auto_wire_load_selection false
#set_wire_load_model -name "16000"
#set_wire_load_mode top

set REFLIB saed32hvt_ss0p75v125c
set BUFFER "IBUFFX8_HVT"
set BUFFER1 "IBUFFX2_HVT"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "Y"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER1 -pin $BUF_OUT_PIN $INPUTPORTS

#set_load -max 0.025 [get_ports Cout*]
set_fix_multiple_port_nets -all -buffer_constants [get_designs dice_game]

#compile_ultra
compile_ultra -no_autoungroup -exact_map
report_area
report_power
report_timing
report_timing -delay_type min
report_constraint -verbose
report_qor


change_names -rule verilog -hier
write -hierarchy -format verilog -output ./dice_game_pc_netlist.v
write_sdc ./dice_game_synth_pc.sdc
```

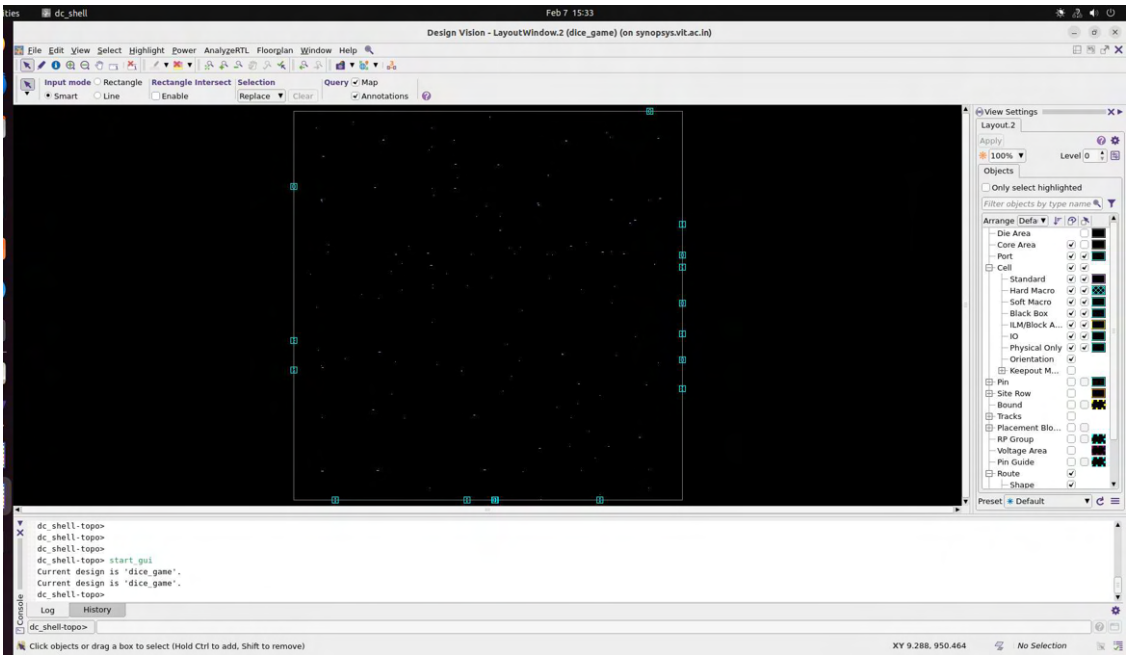
- **Generated netlist file(.v)**



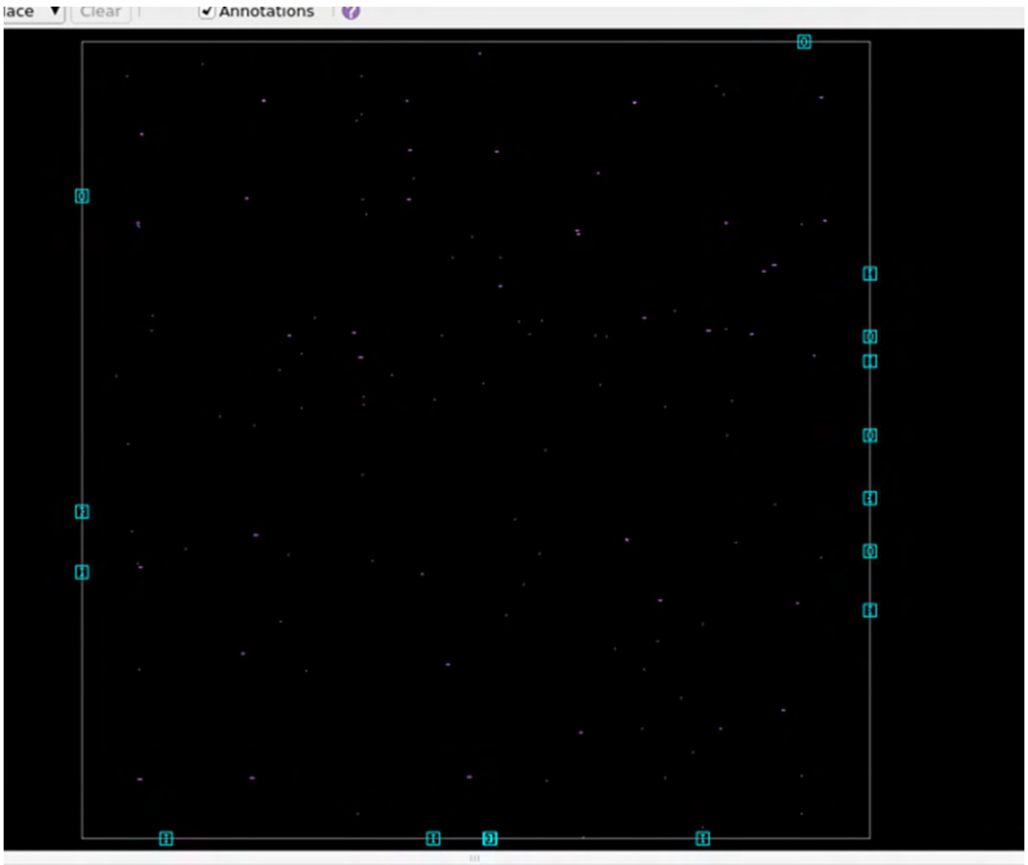

Open
dicegame_pc_netlist.v
~/dice
Save
dice_lp.tcl
dice_game.sdc
dice_game_netlist_lp.v
dicegame_pc_netlist.v
DFFX1_HVT ps_reg_0_ (.D(n4), .CLK(clock), .Q(ps[0]));
LATCHX1_HVT sum_reg_1_ (.CLK(n131), .D(N61), .Q(sum[1]));
LATCHX1_HVT sum_reg_2_ (.CLK(n131), .D(n138), .Q(sum[2]));
LATCHX1_HVT sum_reg_3_ (.CLK(n131), .D(n137), .Q(sum[3]));
LATCHX1_HVT point_reg_3_ (.CLK(n136), .D(n125), .Q(point[3]));
LATCHX1_HVT point_reg_2_ (.CLK(n136), .D(N57), .Q(point[2]));
LATCHX1_HVT point_reg_1_ (.CLK(n136), .D(n124), .Q(point[1]));
LATCHX1_HVT point_reg_0_ (.CLK(n136), .D(N55), .Q(point[0]));
INVX1_HVT U37 (.A(ps[0]), .Y(n118));
INVX1_HVT U40 (.A(ps[1]), .Y(n114));
AND2X1_HVT U43 (.A1(n132), .A2(sum[1]), .Y(n124));
INVX1_HVT U44 (.A(point[1]), .Y(n26));
INVX1_HVT U49 (.A(point[2]), .Y(n31));
INVX1_HVT U52 (.A(point[0]), .Y(n40));
INVX1_HVT U60 (.A(n31), .Y(n32));
INVX1_HVT U63 (.A(point[3]), .Y(n37));
AND2X1_HVT U73 (.A1(n131), .A2(ps[1]), .Y(n50));
XOR2X1_HVT U74 (.A1(sum[2]), .A2(sum[3]), .Y(n46));
NAND2X0_HVT U75 (.A1(n46), .A2(sum[0]), .Y(n99));
INVX1_HVT U76 (.A(n99), .Y(n47));
NAND2X0_HVT U77 (.A1(n124), .A2(n47), .Y(n48));
AND2X1_HVT U80 (.A1(n132), .A2(sum[3]), .Y(n125));
INVX1_HVT U96 (.A(n62), .Y(n65));
NOR2X0_HVT U116 (.A1(sum[2]), .A2(sum[3]), .Y(n98));
INVX1_HVT U117 (.A(sum[2]), .Y(n87));
NOR3X0_HVT U118 (.A1(sum[1]), .A2(sum[0]), .A3(n87), .Y(n101));
INVX1_HVT U122 (.A(n92), .Y(n123));
NAND2X0_HVT U123 (.A1(n118), .A2(n107), .Y(n93));
INVX1_HVT U124 (.A(n93), .Y(N61));
NBUFFX2_HVT U125 (.A(n94), .Y(n95));
INVX1_HVT U131 (.A(n98), .Y(n100));
NAND2X0_HVT U132 (.A1(n100), .A2(n99), .Y(n102));
AOI22X1_HVT U133 (.A1(sum[1]), .A2(n102), .A3(n101), .A4(sum[3]), .Y(n104)
);
AND2X1_HVT U136 (.A1(n132), .A2(sum[0]), .Y(N55));
AND2X1_HVT U137 (.A1(n132), .A2(sum[2]), .Y(N57));
NAND2X0_HVT U138 (.A1(n132), .A2(n104), .Y(n117));
AND2X1_HVT U139 (.A1(n107), .A2(n133), .Y(n113));
INVX1_HVT U140 (.A(n95), .Y(n110));
AND2X1_HVT U141 (.A1(n110), .A2(n144), .Y(n112));
AO21X1_HVT U142 (.A1(n113), .A2(n112), .A3(n111), .Y(n115));
AO21X1_HVT U143 (.A1(n131), .A2(n115), .A3(n114), .Y(n116));
AOI21X1_HVT U144 (.A1(n117), .A2(n116), .A3(rst), .Y(n5));
OA21X1_HVT U147 (.A1(ps[1]), .A2(n131), .A3(n135), .Y(n4));
INVX2_HVT U85 (.A(n54), .Y(n55));
XOR2X2_LVT U105 (.A1(n72), .A2(n71), .Y(n94));
NBUFFX2_LVT U46 (.A(dice2[1]), .Y(n60));
XOR2X2_LVT U69 (.A1(n130), .A2(n41), .Y(n42));
OR2X2_LVT U71 (.A1(n45), .A2(n44), .Y(n90));
OA21X1_LVT U111 (.A1(n80), .A2(n81), .A3(n129), .Y(n82));
NOR4X1_LVT U115 (.A1(n86), .A2(n92), .A3(n94), .A4(n85), .Y(n91));
XOR2X2_LVT U66 (.A1(n39), .A2(n38), .Y(n43));
Verilog
Tab Width: 8
Ln 1, Col 1
INS


Open
dicegame_pc_netlist.v
~/dice
Save
dice_lp.tcl
dice_game.sdc
dice_game_netlist_lp.v
dicegame_pc_netlist.v
NAND2X0_LVT U106 (.A1(n78), .A2(n77), .Y(n73));
NAND2X0_LVT U57 (.A1(n38), .A2(n29), .Y(n45));
NBUFFX2_LVT U45 (.A(dice1[1]), .Y(n59));
NAND2X0_RVT U107 (.A1(n73), .A2(n79), .Y(n74));
NBUFFX2_LVT U103 (.A(dice2[3]), .Y(n70));
NBUFFX2_LVT U48 (.A(dice2[2]), .Y(n62));
NBUFFX2_LVT U47 (.A(dice1[2]), .Y(n63));
NBUFFX2_LVT U64 (.A(dice1[3]), .Y(n36));
INVX2_HVT U58 (.A(n62), .Y(n34));
XOR2X2_HVT U104 (.A1(n70), .A2(n36), .Y(n71));
INVX1_RVT U59 (.A(n63), .Y(n33));
INVX2_LVT U91 (.A(n59), .Y(n78));
AND2X1_RVT U110 (.A1(n78), .A2(n77), .Y(n81));
AND2X1_RVT U93 (.A1(n78), .A2(n77), .Y(n61));
FADDX1_RVT U61 (.A(n34), .B(n33), .CI(n32), .CO(n35));
INVX1_RVT U62 (.A(n35), .Y(n39));
NAND2X0_LVT U70 (.A1(n42), .A2(n43), .Y(n44));
INVX1_RVT U97 (.A(n63), .Y(n64));
NOR2X0_LVT U98 (.A1(n63), .A2(n62), .Y(n75));
INVX2_HVT U99 (.A(n66), .Y(n76));
INVX1_RVT U100 (.A(n76), .Y(n67));
OR2X1_LVT U109 (.A1(n76), .A2(n75), .Y(n84));
XOR2X2_RVT U108 (.A1(n74), .A2(n145), .Y(n107));
NAND2X1_LVT U89 (.A1(n118), .A2(n133), .Y(n92));
XOR2X2_LVT U51 (.A1(n25), .A2(n24), .Y(n30));
INVX1_HVT U72 (.A(n90), .Y(n111));
INVX2_LVT U92 (.A(n60), .Y(n77));
INVX2_LVT U84 (.A(n53), .Y(n56));
NAND2X0_RVT U38 (.A1(n60), .A2(n59), .Y(n129));
NAND2X0_RVT U39 (.A1(n60), .A2(n59), .Y(n79));
NBUFFX4_LVT U41 (.A(n54), .Y(n130));
AND2X1_LVT U42 (.A1(n57), .A2(n145), .Y(n133));
INVX1_HVT U53 (.A(n50), .Y(n142));
OR2X1_RVT U54 (.A1(n53), .A2(n54), .Y(n57));
NBUFFX2_LVT U78 (.A(n59), .Y(n139));
AND2X1_HVT U79 (.A1(roll), .A2(n118), .Y(n131));
AND2X1_HVT U82 (.A1(n114), .A2(ps[0]), .Y(n132));
AO22X1_HVT U83 (.A1(n98), .A2(n124), .A3(n101), .A4(n125), .Y(n134));
AOI21X1_HVT U87 (.A1(ps[1]), .A2(n118), .A3(rst), .Y(n135));
OA21X1_HVT U88 (.A1(n104), .A2(n118), .A3(n114), .Y(n136));
AND2X1_HVT U94 (.A1(n118), .A2(n95), .Y(n137));
AND2X1_HVT U101 (.A1(n118), .A2(n144), .Y(n138));
NBUFFX2_LVT U119 (.A(n80), .Y(n145));
NBUFFX2_HVT U120 (.A(n109), .Y(n144));
INVX1_LVT U126 (.A(dice2[0]), .Y(n140));
INVX2_LVT U127 (.A(n140), .Y(n53));
INVX2_LVT U128 (.A(n141), .Y(win));
OA21X1_LVT U129 (.A1(n90), .A2(n142), .A3(n48), .Y(n141));
NBUFFX2_LVT U130 (.A(n60), .Y(n143));
OA21X1_LVT U134 (.A1(n75), .A2(n68), .A3(n67), .Y(n69));
endmodule
Verilog
Tab Width: 8
Ln 1, Col 1
INS

- **Layout view**

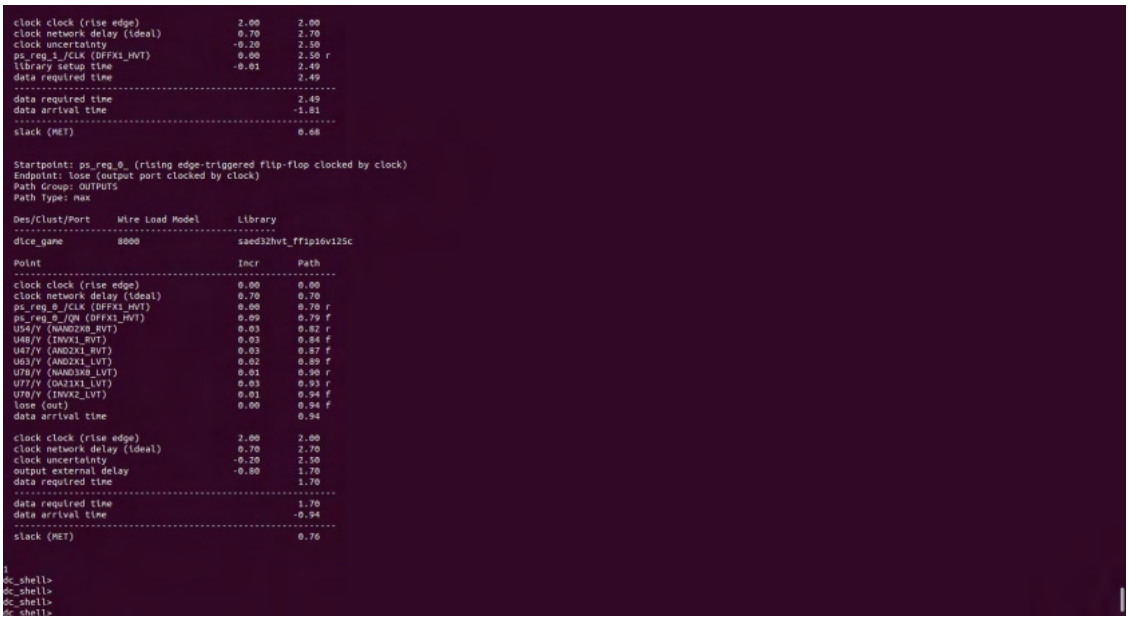


Layout with standard cells:



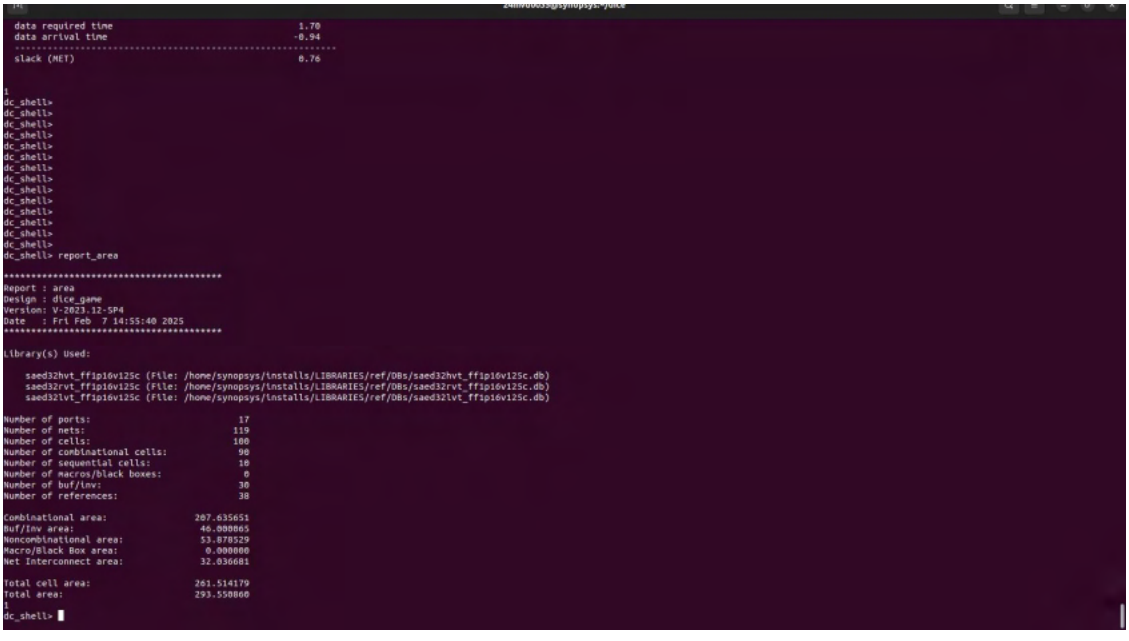
- **REPORTS:**

Timing::



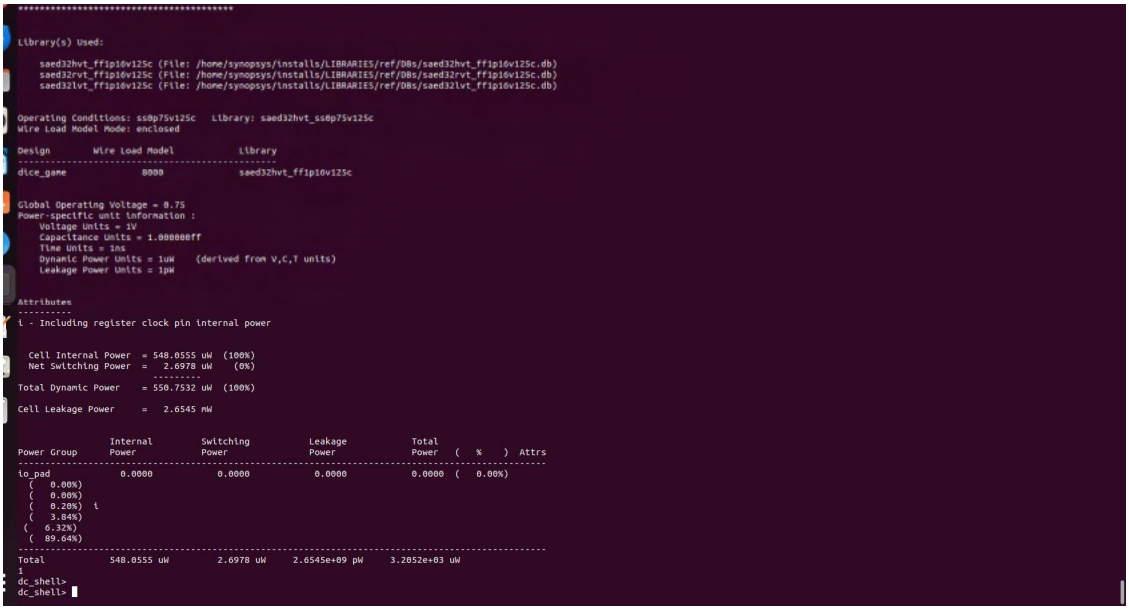
```
  clock clock (rise edge)                  2.00       2.00
  clock network delay (ideal)              0.70       2.70
  clock uncertainty                       -0.20       2.50
  ps_reg_1_/CLK (DFFX1_HVT)                0.00       2.50 r
  library setup time                      -0.01       2.49
  data required time                                  2.49
  ----------------------------------------------------------
  data required time                                  2.49
  data arrival time                                  -1.81
  ----------------------------------------------------------
  slack (MET)                                         0.68


  Startpoint: ps_reg_0_ (rising edge-triggered flip-flop clocked by clock)
  Endpoint: lose (output port clocked by clock)
  Path Group: OUTPUTS
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  dice_game          8000                  saed32hvt_ff1p16v125c

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock clock (rise edge)                  0.00       0.00
  clock network delay (ideal)              0.70       0.70
  ps_reg_0_/CLK (DFFX1_HVT)                0.00       0.70 r
  ps_reg_0_/QN (DFFX1_HVT)                 0.09       0.79 f
  U54/Y (NAND2X0_RVT)                      0.03       0.82 r
  U48/Y (INVX1_RVT)                        0.03       0.84 f
  U47/Y (AND2X1_RVT)                       0.03       0.87 f
  U63/Y (AND2X1_LVT)                       0.02       0.89 f
  U78/Y (NAND3X0_LVT)                      0.01       0.90 r
  U77/Y (OA21X1_LVT)                       0.03       0.93 r
  U79/Y (INVX2_LVT)                        0.01       0.94 f
  lose (out)                               0.00       0.94 f
  data arrival time                                   0.94

  clock clock (rise edge)                  2.00       2.00
  clock network delay (ideal)              0.70       2.70
  clock uncertainty                       -0.20       2.50
  output external delay                   -0.80       1.70
  data required time                                  1.70
  ----------------------------------------------------------
  data required time                                  1.70
  data arrival time                                  -0.94
  ----------------------------------------------------------
  slack (MET)                                         0.76


1
dc_shell>
dc_shell>
dc_shell>
```

Area:



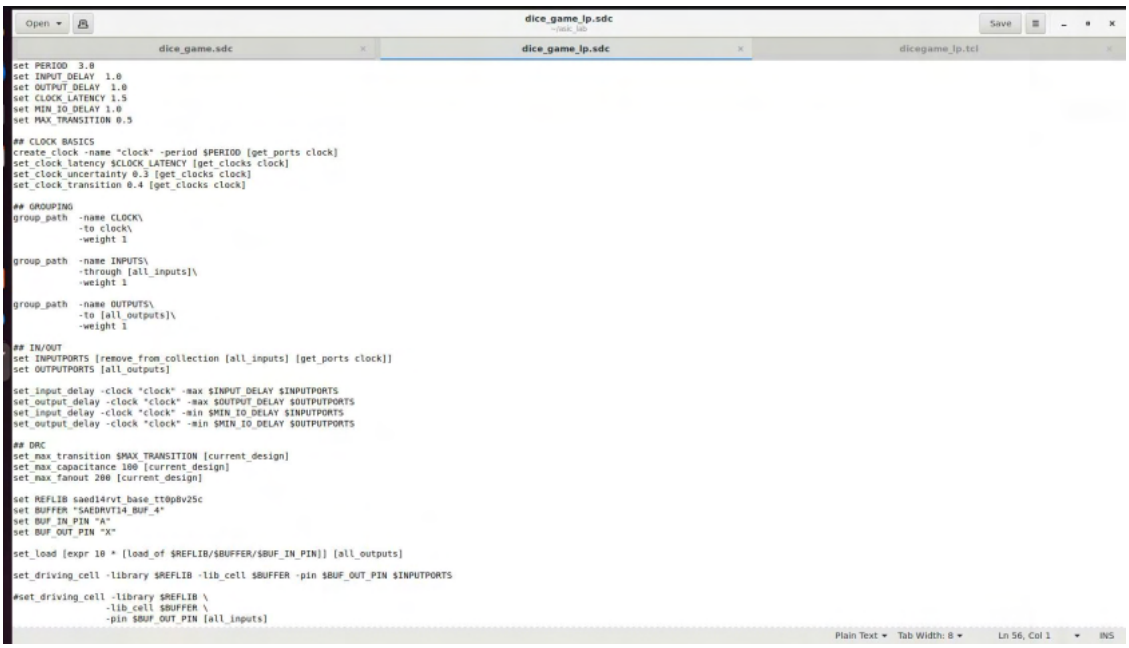
```
  data required time                                  1.70
  data arrival time                                  -0.94
  ----------------------------------------------------------
  slack (MET)                                         0.76


1
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell>
dc_shell> report_area

****************************************
Report : area
Design : dice_game
Version: V-2023.12-SP4
Date   : Fri Feb  7 14:55:40 2025
****************************************

Library(s) Used:

    saed32hvt_ff1p16v125c (File: /home/synopsys/installs/LIBRARIES/ref/DBs/saed32hvt_ff1p16v125c.db)
    saed32rvt_ff1p16v125c (File: /home/synopsys/installs/LIBRARIES/ref/DBs/saed32rvt_ff1p16v125c.db)
    saed32lvt_ff1p16v125c (File: /home/synopsys/installs/LIBRARIES/ref/DBs/saed32lvt_ff1p16v125c.db)

Number of ports:                           17
Number of nets:                           119
Number of cells:                          100
Number of combinational cells:             90
Number of sequential cells:                10
Number of macros/black boxes:               0
Number of buf/inv:                         30
Number of references:                      38

Combinational area:              207.635651
Buf/Inv area:                     46.080865
Noncombinational area:            53.878529
Macro/Black Box area:              0.000000
Net Interconnect area:            32.036681

Total cell area:                 261.514179
Total area:                      293.550860
1
dc_shell>
```

Power:

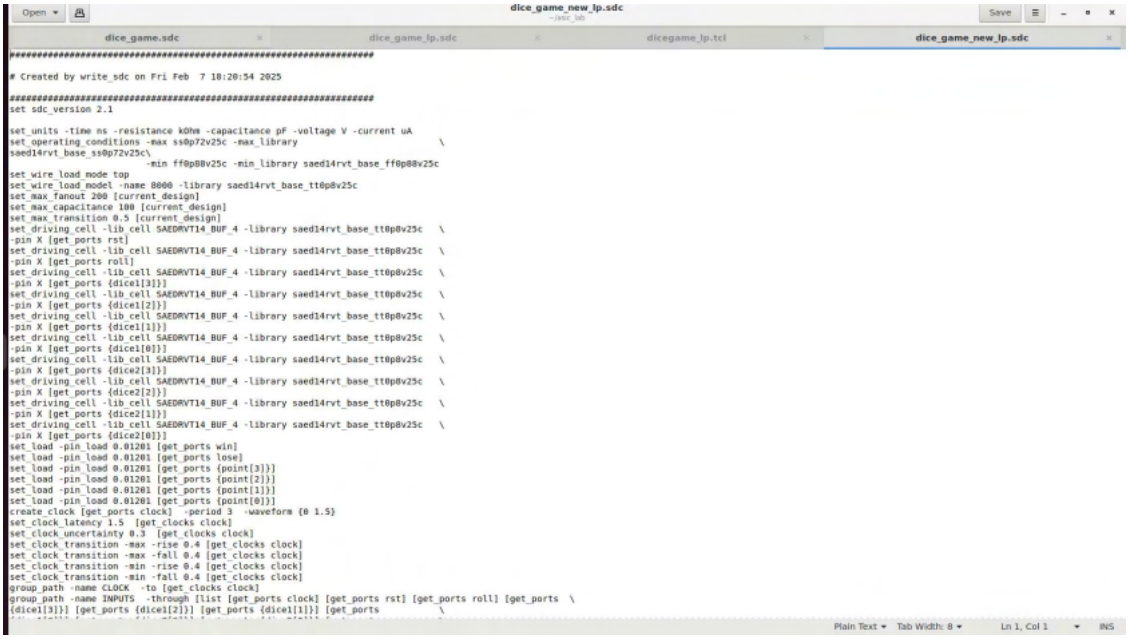


2. LOW POWER SYNTHESIS

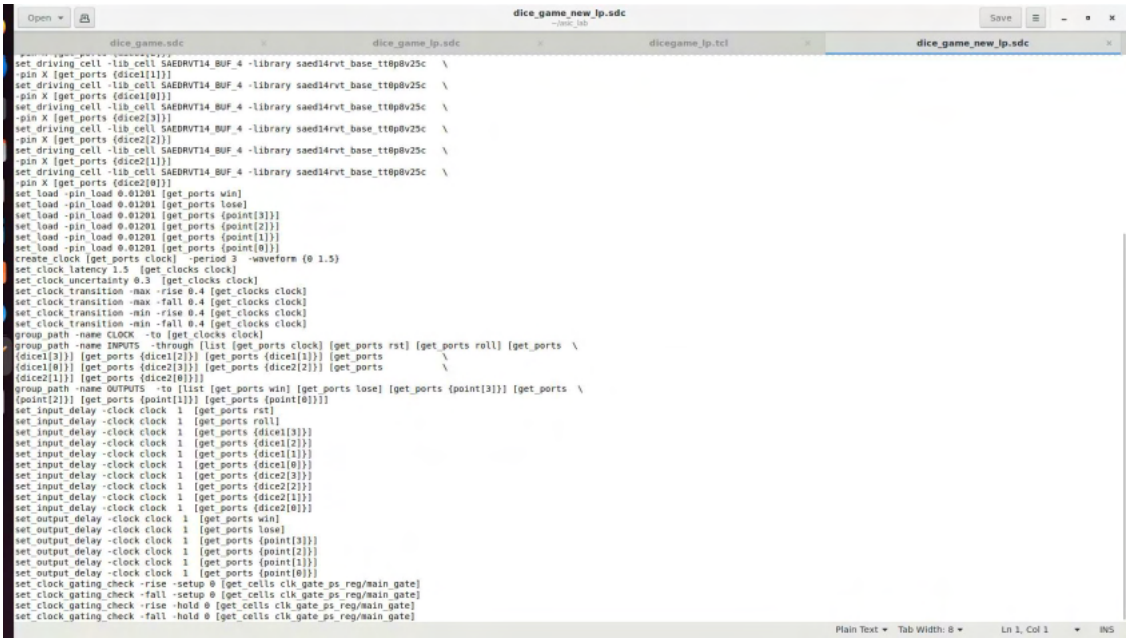
- **.sdc file**



Generated Sdc



```
dice_game_new_lp.sdc
dice_game.sdc | dice_game_lp.sdc | dicegame_lp.tcl | dice_game_new_lp.sdc
################################################################################

# Created by write_sdc on Fri Feb  7 18:20:54 2025

###############################################################################
set sdc_version 2.1

set_units -time ns -resistance kOhm -capacitance pF -voltage V -current uA
set_operating_conditions -max ss0p72v25c -max_library                    \
saed14rvt_base_ss0p72v25c\
                         -min ff0p88v25c -min_library saed14rvt_base_ff0p88v25c
set_wire_load_mode top
set_wire_load_model -name 8000 -library saed14rvt_base_tt0p8v25c
set_max_fanout 200 [current_design]
set_max_capacitance 100 [current_design]
set_max_transition 0.5 [current_design]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports rst]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports roll]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[3]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[2]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[1]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[0]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[3]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[2]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[1]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[0]}]
set_load -pin_load 0.01201 [get_ports win]
set_load -pin_load 0.01201 [get_ports lose]
set_load -pin_load 0.01201 [get_ports {point[3]}]
set_load -pin_load 0.01201 [get_ports {point[2]}]
set_load -pin_load 0.01201 [get_ports {point[1]}]
set_load -pin_load 0.01201 [get_ports {point[0]}]
create_clock [get_ports clock]  -period 3  -waveform {0 1.5}
set_clock_latency 1.5  [get_clocks clock]
set_clock_uncertainty 0.3  [get_clocks clock]
set_clock_transition -max -rise 0.4 [get_clocks clock]
set_clock_transition -max -fall 0.4 [get_clocks clock]
set_clock_transition -min -rise 0.4 [get_clocks clock]
set_clock_transition -min -fall 0.4 [get_clocks clock]
group_path -name CLOCK  -to [get_clocks clock]
group_path -name INPUTS  -through [list [get_ports clock] [get_ports rst] [get_ports roll] [get_ports  \
{dice1[3]}] [get_ports {dice1[2]}] [get_ports {dice1[1]}] [get_ports           \
Plain Text  Tab Width: 8  Ln 1, Col 1  INS
```



```
dice_game_new_lp.sdc
dice_game.sdc | dice_game_lp.sdc | dicegame_lp.tcl | dice_game_new_lp.sdc
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[1]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[0]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[3]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[2]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[1]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[0]}]
set_load -pin_load 0.01201 [get_ports win]
set_load -pin_load 0.01201 [get_ports lose]
set_load -pin_load 0.01201 [get_ports {point[3]}]
set_load -pin_load 0.01201 [get_ports {point[2]}]
set_load -pin_load 0.01201 [get_ports {point[1]}]
set_load -pin_load 0.01201 [get_ports {point[0]}]
create_clock [get_ports clock]  -period 3  -waveform {0 1.5}
set_clock_latency 1.5  [get_clocks clock]
set_clock_uncertainty 0.3  [get_clocks clock]
set_clock_transition -max -rise 0.4 [get_clocks clock]
set_clock_transition -max -fall 0.4 [get_clocks clock]
set_clock_transition -min -rise 0.4 [get_clocks clock]
set_clock_transition -min -fall 0.4 [get_clocks clock]
group_path -name CLOCK  -to [get_clocks clock]
group_path -name INPUTS  -through [list [get_ports clock] [get_ports rst] [get_ports roll] [get_ports  \
{dice1[3]}] [get_ports {dice1[2]}] [get_ports {dice1[1]}] [get_ports           \
{dice1[0]}] [get_ports {dice2[3]}] [get_ports {dice2[2]}] [get_ports           \
{dice2[1]}] [get_ports {dice2[0]}]]
group_path -name OUTPUTS  -to [list [get_ports win] [get_ports lose] [get_ports {point[3]}] [get_ports  \
{point[2]}] [get_ports {point[1]}] [get_ports {point[0]}]]
set_input_delay -clock clock  1  [get_ports rst]
set_input_delay -clock clock  1  [get_ports roll]
set_input_delay -clock clock  1  [get_ports {dice1[3]}]
set_input_delay -clock clock  1  [get_ports {dice1[2]}]
set_input_delay -clock clock  1  [get_ports {dice1[1]}]
set_input_delay -clock clock  1  [get_ports {dice1[0]}]
set_input_delay -clock clock  1  [get_ports {dice2[3]}]
set_input_delay -clock clock  1  [get_ports {dice2[2]}]
set_input_delay -clock clock  1  [get_ports {dice2[1]}]
set_input_delay -clock clock  1  [get_ports {dice2[0]}]
set_output_delay -clock clock  1  [get_ports win]
set_output_delay -clock clock  1  [get_ports lose]
set_output_delay -clock clock  1  [get_ports {point[3]}]
set_output_delay -clock clock  1  [get_ports {point[2]}]
set_output_delay -clock clock  1  [get_ports {point[1]}]
set_output_delay -clock clock  1  [get_ports {point[0]}]
set_clock_gating_check -rise -setup 0 [get_cells clk_gate_ps_reg/main_gate]
set_clock_gating_check -fall -setup 0 [get_cells clk_gate_ps_reg/main_gate]
set_clock_gating_check -rise -hold 0 [get_cells clk_gate_ps_reg/main_gate]
set_clock_gating_check -fall -hold 0 [get_cells clk_gate_ps_reg/main_gate]
Plain Text  Tab Width: 8  Ln 1, Col 1  INS
```

.tcl file

Open

dicegame_lp.tcl
~/asic_lab

```
set_host_options -max_cores 4

#source ../../../common_setup.tcl

set DESIGN_REF_PATH "/home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/"

set LINK_LIBRARY_FILES    "* \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_tt0p8v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ss0p72v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ff0p88v25c.db"


set TARGET_LIBRARY_FILES   "\
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_tt0p8v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ss0p72v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ff0p88v25c.db"


set link_library  $LINK_LIBRARY_FILES
set target_library $TARGET_LIBRARY_FILES


#set_app_var search_path "$SEARCH_PATH"
#set_app_var target_library "$TARGET_LIBRARY_FILES"
#set_app_var link_library " $LINK_LIBRARY_FILES "


# SET DONT USE ############################################################
#set_dont_use [get_lib_cells -quiet */SAEDRVT14_AO21_U_0P5]

analyze -library WORK -format verilog {./dice_game.v \

}
read_file -format verilog {./dice_game.v}
```

Open

dicegame_lp.tcl
~/asic_lab

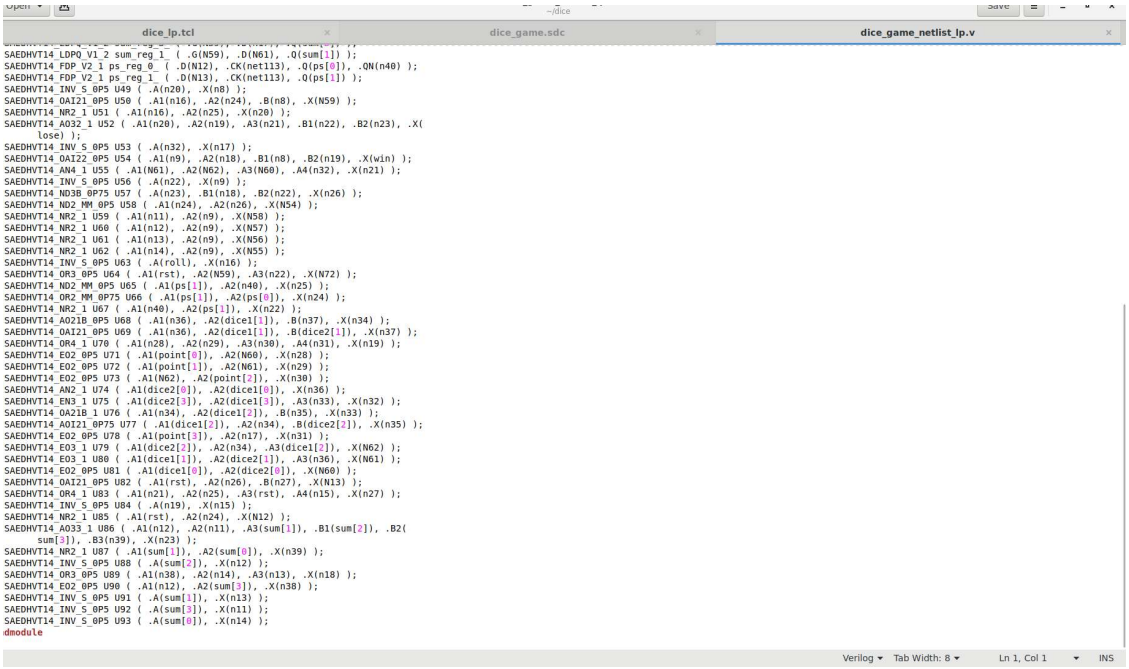
```
# SET DONT USE ###########################################################
#set_dont_use [get_lib_cells -quiet */SAEDRVT14_AO21_U_0P5]

analyze -library WORK -format verilog {./dice_game.v \

}
read_file -format verilog {./dice_game.v}

# check design quality
check_design

link

source -echo ./dice_game_lp.sdc

check_timing

set auto_wire_load_selection false
set_wire_load_model -name "8000"
set_wire_load_mode top

set_clock_gating_registers -include_instances [remove_from_collection  [all_registers -clock clock] [get_cells "MemYHier/MemXb MemYHier/MemXa MemXHier/MemXb MemXHier/MemXa"]]

set_operating_conditions -min ff0p88v25c -max ss0p72v25c

set_leakage_optimization true
set_dynamic_optimization true

set_fix_multiple_port_nets -all -buffer_constants [get_designs dice_game]


compile -exact_map -gate_clock

change_names -rules verilog -verbose -hier
report_clock_gating


#set_fix_hold [all_clocks]
#report_constraints  -min_delay
#compile -incremental -only_design

###########reports#############################
report_area
report_timing
report_power


write -f verilog -h -out    ./dice_game_netlist_lp.v
write -f ddc -h -out        ./dice_game_lp.ddc
write_sdc ./dice_game_new_lp.sdc
```

- **Generated netlist file(.v)**

dice_lp.tcl | dice_game.sdc | dice_game_netlist_lp.v

```
////////////////////////////////////////////////////////////////////
// Created by: Synopsys DC Expert(TM) in wire load mode
// Version   : V-2023.12-SP4
// Date      : Fri Feb  7 14:28:56 2025
////////////////////////////////////////////////////////////////////


module SNPS_CLOCK_GATE_HIGH_dice_game ( CLK, EN, ENCLK );
  input CLK, EN;
  output ENCLK;
  wire   net107;

  SAEDHVT14_LDNQ_V1_2 latch ( .D(EN), .G(CLK), .Q(net107) );
  SAEDHVT14_AN2_1 main_gate ( .A1(net107), .A2(CLK), .X(ENCLK) );
endmodule


module dice_game ( clock, rst, roll, dice1, dice2, win, lose, point );
  input [3:0] dice1;
  input [3:0] dice2;
  output [3:0] point;
  input clock, rst, roll;
  output win, lose;
  wire   N12, N13, N54, N55, N56, N57, N58, N59, N60, N61, N62, N72, net113,
         n8, n9, n11, n12, n13, n14, n15, n16, n17, n18, n19, n20, n21, n22,
         n23, n24, n25, n26, n27, n28, n29, n30, n31, n32, n33, n34, n35, n36,
         n37, n38, n39, n40;
  wire   [1:0] ps;
  wire   [3:0] sum;

  SNPS_CLOCK_GATE_HIGH_dice_game clk_gate_ps_reg ( .CLK(clock), .EN(N72),
        .ENCLK(net113) );
  SAEDHVT14_LDPQ_V1_2 point_reg_2_ ( .G(N54), .D(N57), .Q(point[2]) );
  SAEDHVT14_LDPQ_V1_2 point_reg_0_ ( .G(N54), .D(N55), .Q(point[0]) );
  SAEDHVT14_LDPQ_V1_2 point_reg_1_ ( .G(N54), .D(N56), .Q(point[1]) );
  SAEDHVT14_LDPQ_V1_2 point_reg_3_ ( .G(N54), .D(N58), .Q(point[3]) );
  SAEDHVT14_LDPQ_V1_2 sum_reg_2_ ( .G(N59), .D(N62), .Q(sum[2]) );
  SAEDHVT14_LDPQ_V1_2 sum_reg_0_ ( .G(N59), .D(N60), .Q(sum[0]) );
  SAEDHVT14_LDPQ_V1_2 sum_reg_3_ ( .G(N59), .D(n17), .Q(sum[3]) );
  SAEDHVT14_LDPQ_V1_2 sum_reg_1_ ( .G(N59), .D(N61), .Q(sum[1]) );
  SAEDHVT14_FDP_V2_1 ps_reg_0_ ( .D(N12), .CK(net113), .Q(ps[0]), .QN(n40) );
  SAEDHVT14_FDP_V2_1 ps_reg_1_ ( .D(N13), .CK(net113), .Q(ps[1]) );
  SAEDHVT14_INV_S_0P5 U49 ( .A(n20), .X(n8) );
  SAEDHVT14_OAI21_0P5 U50 ( .A1(n16), .A2(n24), .B(n8), .X(N59) );
  SAEDHVT14_NR2_1 U51 ( .A1(n16), .A2(n25), .X(n20) );
  SAEDHVT14_AO32_1 U52 ( .A1(n20), .A2(n19), .A3(n21), .B1(n22), .B2(n23), .X(
        lose) );
  SAEDHVT14_INV_S_0P5 U53 ( .A(n32), .X(n17) );
  SAEDHVT14_OAI22_0P5 U54 ( .A1(n9), .A2(n18), .B1(n8), .B2(n19), .X(win) );
  SAEDHVT14_AN4_1 U55 ( .A1(N61), .A2(N62), .A3(N60), .A4(n32), .X(n21) );
  SAEDHVT14_INV_S_0P5 U56 ( .A(n22), .X(n9) );
  SAEDHVT14_ND3B_0P75 U57 ( .A(n23), .B1(n18), .B2(n22), .X(n26) );
```

Verilog | Tab Width: 8 | Ln 1, Col 1 | INS



REPORTS:

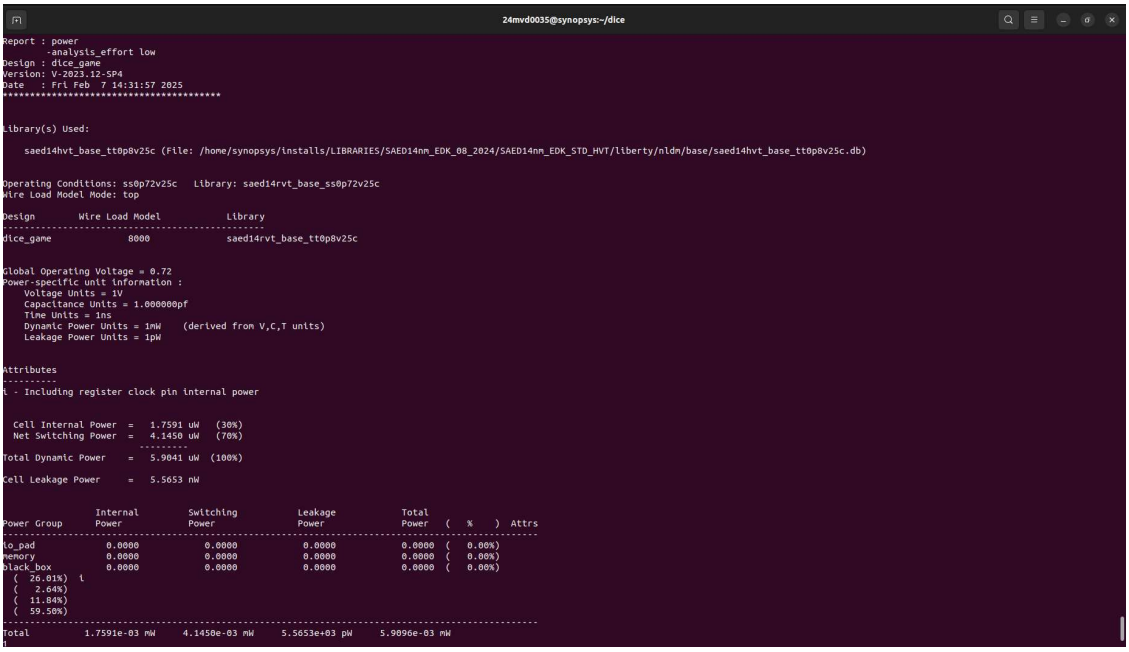
Timing:

```
slack (MET)                                                    1.68

Time Borrowing Information
-----------------------------------------------------------------
clock nominal pulse width                                  3.50
library setup time                                         0.00
-----------------------------------------------------------------
max time borrow                                            3.50
actual time borrow                                         0.00
-----------------------------------------------------------------


Startpoint: dice1[0] (input port clocked by clock)
Endpoint: win (output port clocked by clock)
Path Group: OUTPUTS
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
dice_game          8000                  saed14rvt_base_tt0p8v25c

Point                                    Incr       Path
-----------------------------------------------------------
clock clock (rise edge)                  0.00       0.00
clock network delay (ideal)              1.50       1.50
input external delay                     1.00       2.50 r
dice1[0] (in)                            0.00       2.50 r
U74/X (SAEDHVT14_AN2_1)                  0.05       2.55 r
U69/X (SAEDHVT14_OAI21_0P5)              0.05       2.61 f
U68/X (SAEDHVT14_AO21B_0P5)              0.12       2.72 r
U77/X (SAEDHVT14_AOI21_0P75)             0.07       2.79 f
U76/X (SAEDHVT14_OA21B_1)                0.04       2.84 r
U75/X (SAEDHVT14_EN3_1)                  0.08       2.91 f
U53/X (SAEDHVT14_INV_S_0P5)              0.07       2.99 r
U78/X (SAEDHVT14_EO2_0P5)                0.07       3.06 r
U70/X (SAEDHVT14_OR4_1)                  0.07       3.13 r
U54/X (SAEDHVT14_OAI22_0P5)              0.07       3.20 f
win (out)                                0.00       3.20 f
data arrival time                                   3.20

clock clock (rise edge)                  7.00       7.00
clock network delay (ideal)              1.50       8.50
clock uncertainty                       -0.30       8.20
output external delay                   -1.00       7.20
data required time                                  7.20
-----------------------------------------------------------
data required time                                  7.20
data arrival time                                  -3.20
-----------------------------------------------------------
slack (MET)                                         4.00
```

Area:

```
dc_shell> report_area

****************************************
Report : area
Design : dice_game
Version: V-2023.12-SP4
Date   : Fri Feb  7 14:31:33 2025
****************************************

Library(s) Used:

    saed14hvt_base_tt0p8v25c (File: /home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_tt0p8v25c.db)

Number of ports:                           20
Number of nets:                            72
Number of cells:                           58
Number of combinational cells:             46
Number of sequential cells:                11
Number of macros/black boxes:               0
Number of buf/inv:                          9
Number of references:                      22

Combinational area:                16.250400
Buf/Inv area:                       1.598400
Noncombinational area:              8.258400
Macro/Black Box area:               0.000000
Net Interconnect area:             22.633049

Total cell area:                   24.508800
Total area:                        47.141849
1
```

Power:



```
24mvd0035@synopsys:~/dice

Report : power
        -analysis_effort low
Design : dice_game
Version: V-2023.12-SP4
Date   : Fri Feb  7 14:31:57 2025
****************************************


Library(s) Used:

    saed14hvt_base_tt0p8v25c (File: /home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_tt0p8v25c.db)


Operating Conditions: ss0p72v25c   Library: saed14rvt_base_ss0p72v25c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
dice_game              8000              saed14rvt_base_tt0p8v25c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   1.7591 uW   (30%)
  Net Switching Power  =   4.1450 uW   (70%)
                         ---------
Total Dynamic Power    =   5.9041 uW  (100%)

Cell Leakage Power     =   5.5653 nW


                 Internal         Switching           Leakage           Total
Power Group      Power            Power               Power             Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
  (  26.81%)  i
  (   2.64%)
  (  11.84%)
  (  59.50%)
--------------------------------------------------------------------------------------------------
Total          1.7591e-03 mW     4.1450e-03 mW     5.5653e+03 pW     5.9096e-03 mW
1
```

INFERENCE:

The synthesis process successfully transformed the RTL code into a gate-level netlist optimized for timing, area, and power. The synthesized design meets the required constraints and is ready for further physical implementation stages.