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ASIC DESIGN LAB – MVLD505P

SLOT:L33+L34

DIGITAL ASSIGNMENT -3

Pre STA

SUBMITTED BY:

GOGULA SIVA SHANKAR – 24MVD0035

Aim:

- To perform STA for the dice_game module
- Identify and analyze hold violations
- Use GUI based buffer insertion to resolve violations

Tools used:

- Synopsys primetime
- Design compiler

Procedure:

- Use **pt_shell** command to activate the primetime tool
- Use **source pt_scripts.tcl** to source the tcl file

Pt_script.tcl file

```
## Point to the 32nm SAED libs
set DESIGN_REF_PATH "/home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/"

set SEARCH_PATH       " ./ \
          ${DESIGN_REF_PATH} "

set LINK_LIBRARY_FILES    "* \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_tt0p8v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ss0p72v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ff0p88v25c.db"


set TARGET_LIBRARY_FILES   "\
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ss0p72v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_tt0p8v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ss0p72v25c.db \
${DESIGN_REF_PATH}//SAED14nm_EDK_SRAM/liberty/nldm/saed14sram_ff0p88v25c.db"

#################################################################
# Logical Library Settings
#################################################################
set_app_var search_path "$SEARCH_PATH"
set app var target library "$TARGET LIBRARY FILES"
```

```
#####################################################################
# Logical Library Settings
#####################################################################
set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

read_file -format verilog ./dice_gamenetlist_lp_up.v
current_design dice_game
link

source ./dice_game_new_lp.sdc
check_timing

#set_max_transition 0.1 [current_design]
#set_max_capacitance 100 [current_design]
#set_max_fanout 200 [current_design]

update_timing -full

report_timing
report_timing -delay_type min
report_analysis_coverage

report_timing -from [all_inputs] -max_paths 20 -to [all_registers -data_pins]  > reports/timing.rpt
report_timing -from [all_register -clock_pins] -max_paths 20 -to [all_registers -data_pins] > reports/su.timing.rpt
report_timing -from [all_register -clock_pins] -max_paths 20 -to [all_registers -data_pins] -delay_type min > reports/hold.timing.rpt
report_timing -from [all_registers -clock_pins] -max_paths 20 -to [all_outputs] >> reports/timing.rpt
report_timing -from [all_inputs] -to [all_outputs] -max_paths 20 >> reports/timing.rpt
report_timing -from [all_registers -clock_pins] -to [all_registers -data_pins] -delay_type max  >> reports/timing.rpt
report_timing -from [all_registers -clock_pins] -to [all_registers -data_pins] -delay_type min  >> reports/timing.rpt


report_timing -transition_time -capacitance -nets -input_pins -from [all_registers -clock_pins] -to [all_registers -data_pins]  > reports/timing.tran.cap.rpt
```

Dice_game_new_lp.sdc file:

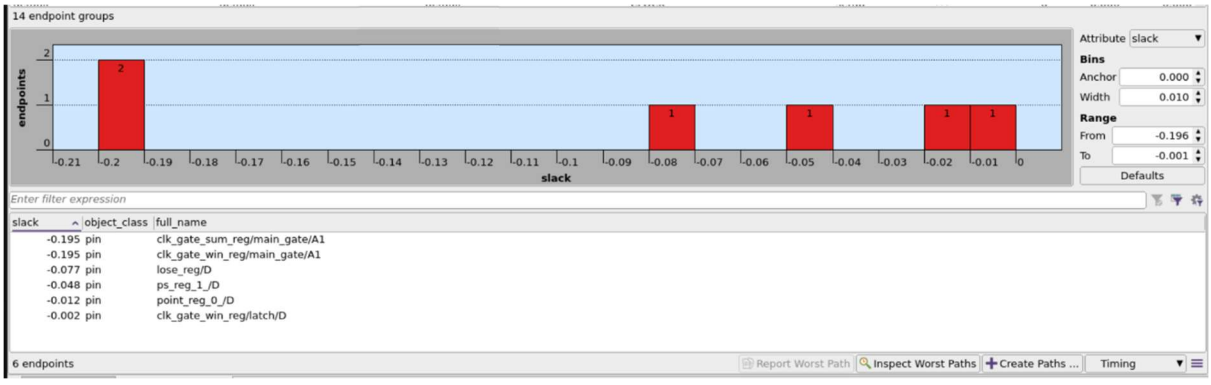
```
#####################################################################
set sdc_version 2.1

set_units -time ns -resistance kOhm -capacitance pF -voltage V -current uA
set_operating_conditions -max ss0p72v25c -max_library                          \
saed14rvt_base_ss0p72v25c\
                         -min ff0p88v25c -min_library saed14rvt_base_ff0p88v25c
set_wire_load_mode top
set_wire_load_model -name 8000 -library saed14rvt_base_tt0p8v25c
set_max_fanout 200 [current_design]
set_max_capacitance 100 [current_design]
set_max_transition 0.5 [current_design]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports rst]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports roll]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[3]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[2]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[1]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice1[0]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[3]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[2]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[1]}]
set_driving_cell -lib_cell SAEDRVT14_BUF_4 -library saed14rvt_base_tt0p8v25c   \
-pin X [get_ports {dice2[0]}]
set_load -pin_load 0.01201 [get_ports win]
set_load -pin_load 0.01201 [get_ports lose]
set_load -pin_load 0.01201 [get_ports {point[3]}]
set_load -pin_load 0.01201 [get_ports {point[2]}]
set_load -pin_load 0.01201 [get_ports {point[1]}]
set_load -pin_load 0.01201 [get_ports {point[0]}]
create_clock [get_ports clock]  -period 3  -waveform {0 1.5}
set_clock_latency 1.5  [get_clocks clock]
set_clock_uncertainty 0.3  [get_clocks clock]
```

```
set_clock_uncertainty 0.3  [get_clocks clock]
set_clock_transition -max -rise 0.4 [get_clocks clock]
set_clock_transition -max -fall 0.4 [get_clocks clock]
set_clock_transition -min -rise 0.4 [get_clocks clock]
set_clock_transition -min -fall 0.4 [get_clocks clock]
group_path -name CLOCK  -to [get_clocks clock]
group_path -name INPUTS  -through [list [get_ports clock] [get_ports rst] [get_ports roll] [get_ports  \
{dice1[3]}] [get_ports {dice1[2]}] [get_ports {dice1[1]}] [get_ports           \
{dice1[0]}] [get_ports {dice2[3]}] [get_ports {dice2[2]}] [get_ports           \
{dice2[1]}] [get_ports {dice2[0]}]]
group_path -name OUTPUTS  -to [list [get_ports win] [get_ports lose] [get_ports {point[3]}] [get_ports  \
{point[2]}] [get_ports {point[1]}] [get_ports {point[0]}]]
set_input_delay -clock clock  1  [get_ports rst]
set_input_delay -clock clock  1  [get_ports roll]
set_input_delay -clock clock  1  [get_ports {dice1[3]}]
set_input_delay -clock clock  1  [get_ports {dice1[2]}]
set_input_delay -clock clock  1  [get_ports {dice1[1]}]
set_input_delay -clock clock  1  [get_ports {dice1[0]}]
set_input_delay -clock clock  1  [get_ports {dice2[3]}]
set_input_delay -clock clock  1  [get_ports {dice2[2]}]
set_input_delay -clock clock  1  [get_ports {dice2[1]}]
set_input_delay -clock clock  1  [get_ports {dice2[0]}]
set_output_delay -clock clock  1  [get_ports win]
set_output_delay -clock clock  1  [get_ports lose]
set_output_delay -clock clock  1  [get_ports {point[3]}]
set_output_delay -clock clock  1  [get_ports {point[2]}]
set_output_delay -clock clock  1  [get_ports {point[1]}]
set_output_delay -clock clock  1  [get_ports {point[0]}]
set_clock_gating_check -rise -setup 0 [get_cells clk_gate_sum_reg/main_gate]
set_clock_gating_check -fall -setup 0 [get_cells clk_gate_sum_reg/main_gate]
set_clock_gating_check -rise -hold 0 [get_cells clk_gate_sum_reg/main_gate]
set_clock_gating_check -fall -hold 0 [get_cells clk_gate_sum_reg/main_gate]
set_clock_gating_check -rise -setup 0 [get_cells clk_gate_win_reg/main_gate]
set_clock_gating_check -fall -setup 0 [get_cells clk_gate_win_reg/main_gate]
set_clock_gating_check -rise -hold 0 [get_cells clk_gate_win_reg/main_gate]
set_clock_gating_check -fall -hold 0 [get_cells clk_gate_win_reg/main_gate]
```

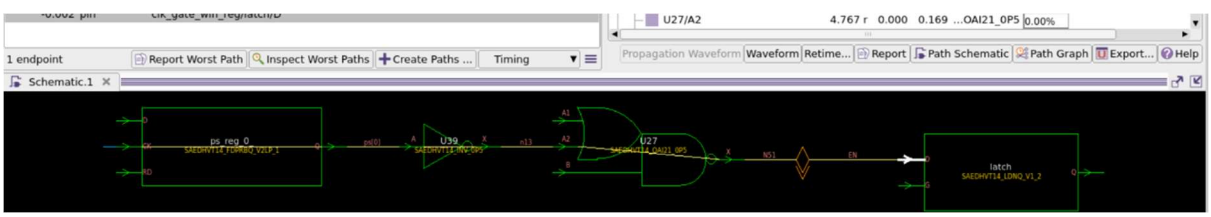
- Use **start_gui** command to activate the gui

Violations:

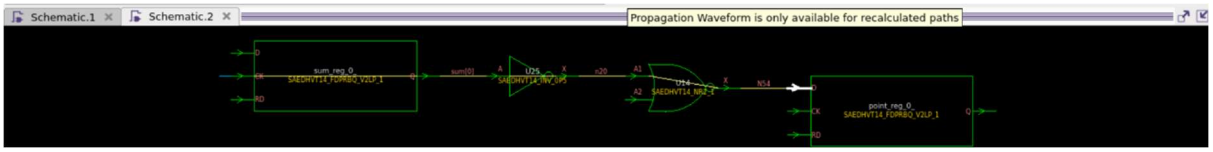


6 hold violations in the design

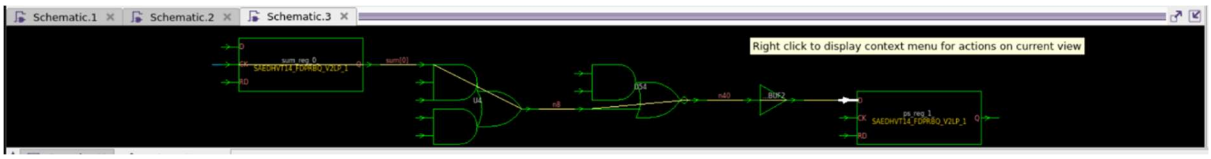
Violated Path1:



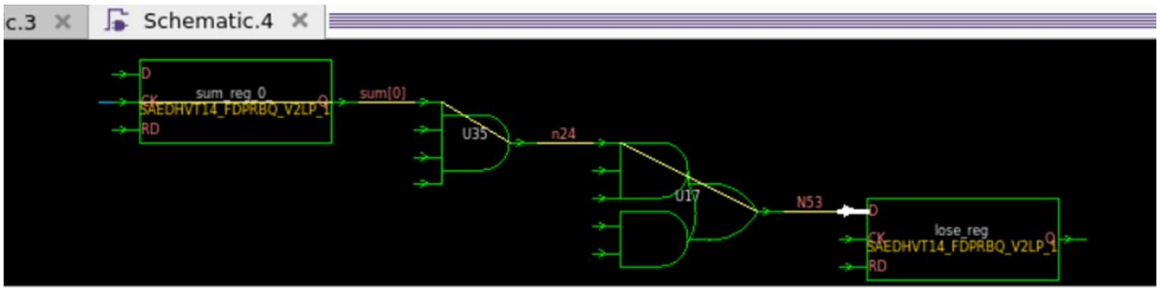
Violated Path2:



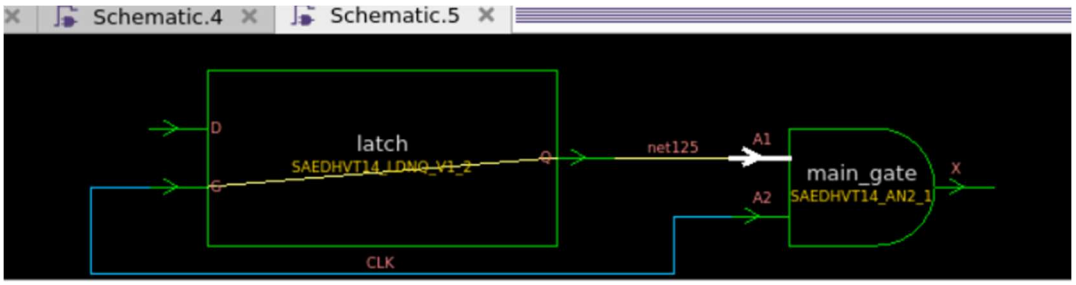
Violated Path3:



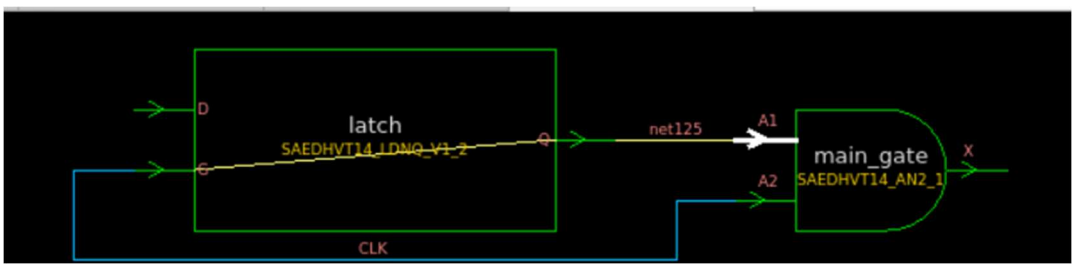
Violated Path4:



Violated Path5:

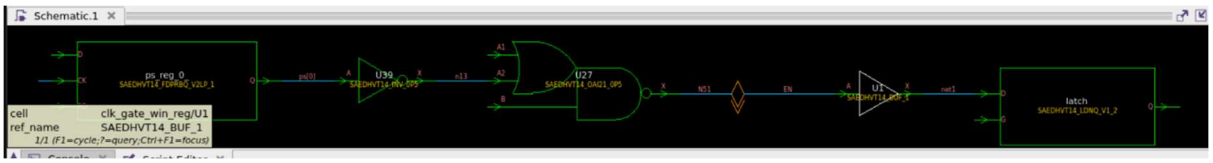


Violated Path6:

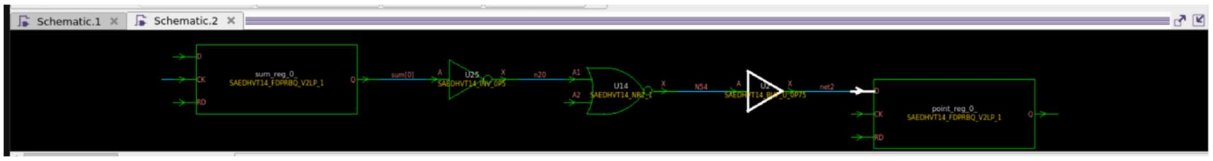


Paths after buffer Insertion:

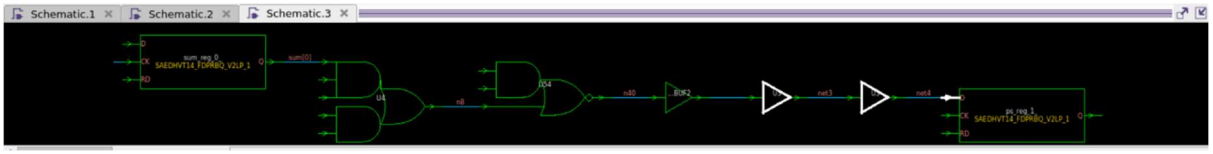
Path1:



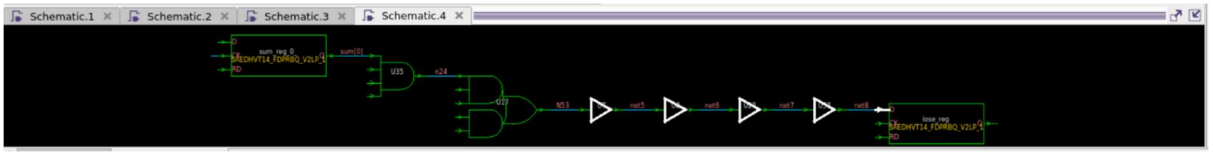
Path2:



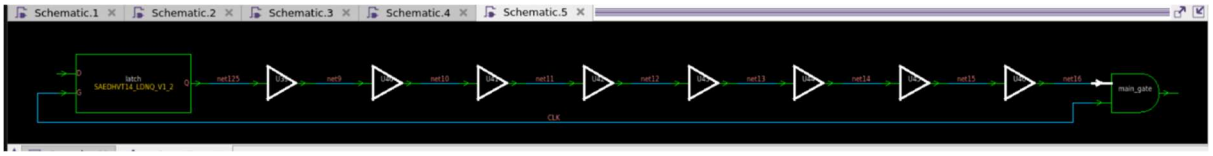
Path3:



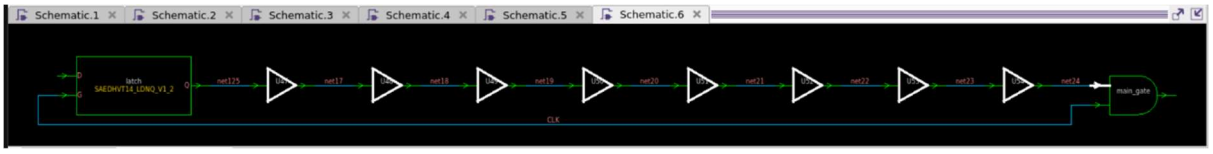
Path4:



Path5:



Path6:



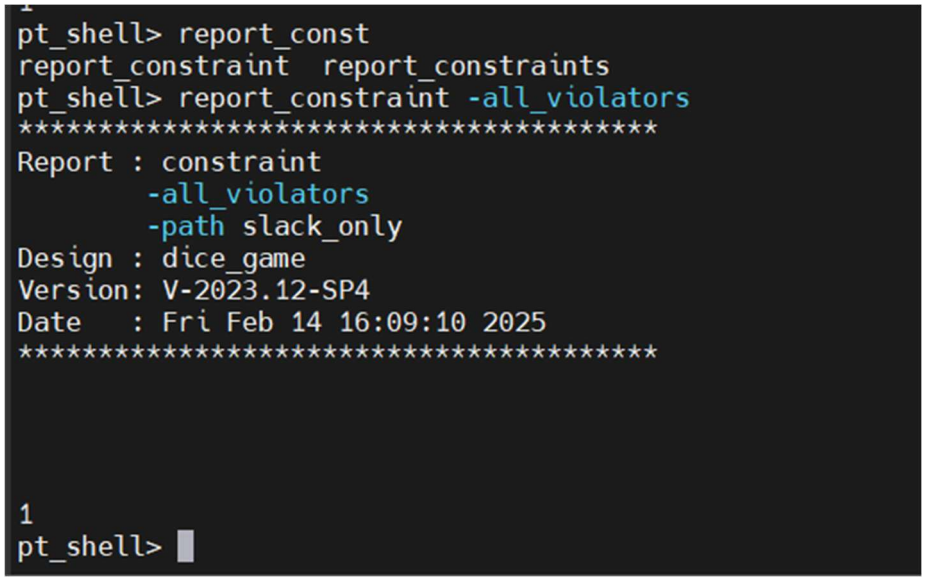
- Use **write_changes -format dctcl -output holdfix.tcl** command to save the changes made into a tcl file.

holdfix.tcl file

dice_lp.tcl

```
# Change list, formatted for dc_shell -tcl
#
# NOTE - Assumes dc_shell is already in incremental mode
#
#
#
#
##########################################################################
current_instance
current_instance {clk_gate_win_reg}
insert_buffer [get_pins {latch/D}] SAEDHVT14_BUF_1 -new_net_names {net1} -new_cell_names {U1}
current_instance
insert_buffer [get_pins {point_reg_0_/D}] SAEDHVT14_BUF_U_0P75 -new_net_names {net2} -new_cell_names {U2}
insert_buffer [get_pins {ps_reg_1_/D}] SAEDHVT14_BUF_U_0P75 -new_net_names {net3} -new_cell_names {U3}
insert_buffer [get_pins {ps_reg_1_/D}] SAEDHVT14_BUF_U_0P75 -new_net_names {net4} -new_cell_names {U5}
insert_buffer [get_pins {lose_reg/D}] SAEDHVT14_BUF_U_0P75 -new_net_names {net5} -new_cell_names {U7}
insert_buffer [get_pins {lose_reg/D}] SAEDHVT14_BUF_1 -new_net_names {net6} -new_cell_names {U8}
insert_buffer [get_pins {lose_reg/D}] SAEDHVT14_BUF_U_0P75 -new_net_names {net7} -new_cell_names {U28}
insert_buffer [get_pins {lose_reg/D}] SAEDHVT14_BUF_1 -new_net_names {net8} -new_cell_names {U38}
current_instance
current_instance {clk_gate_sum_reg}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P75 -new_net_names {net9} -new_cell_names {U39}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P75 -new_net_names {net10} -new_cell_names {U40}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_1 -new_net_names {net11} -new_cell_names {U41}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P5 -new_net_names {net12} -new_cell_names {U42}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_1 -new_net_names {net13} -new_cell_names {U43}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P75 -new_net_names {net14} -new_cell_names {U44}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P75 -new_net_names {net15} -new_cell_names {U45}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_1 -new_net_names {net16} -new_cell_names {U46}
current_instance
current_instance {clk_gate_win_reg}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_1 -new_net_names {net17} -new_cell_names {U47}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_1 -new_net_names {net18} -new_cell_names {U48}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P75 -new_net_names {net19} -new_cell_names {U49}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P75 -new_net_names {net20} -new_cell_names {U50}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P75 -new_net_names {net21} -new_cell_names {U51}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_U_0P5 -new_net_names {net22} -new_cell_names {U52}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_1 -new_net_names {net23} -new_cell_names {U53}
insert_buffer [get_pins {main_gate/A1}] SAEDHVT14_BUF_1 -new_net_names {net24} -new_cell_names {U54}
current_instance
```

- use **report_constrains -all_violations** to list all the violations in the design.



This figure shows that there are no violated paths in the design.

- Use **dc_shell** to activate the design compiler tool
- Use **source dicegame_lp.tcl** to source the tcl file. The tcl file includes the holdfix.tcl file. So it source the file and updates the netlist .v file

Updated netlist file:

```
////////////////////////////////////////////////////////////
// Created by: Synopsys DC Expert(TM) in wire load mode
// Version   : V-2023.12-SP4
// Date      : Fri Feb 14 16:06:32 2025
////////////////////////////////////////////////////////////


module SNPS_CLOCK_GATE_HIGH_dice_game_0 ( CLK, EN, ENCLK );
  input CLK, EN;
  output ENCLK;
  wire   net125, net1, net17, net18, net19, net20, net21, net22, net23, net24;

  SAEDHVT14_LDNQ_V1_2 latch ( .D(net1), .G(CLK), .Q(net125) );
  SAEDHVT14_AN2_1 main_gate ( .A1(net24), .A2(CLK), .X(ENCLK) );
  SAEDHVT14_BUF_1 U1 ( .A(EN), .X(net1) );
  SAEDHVT14_BUF_1 U47 ( .A(net125), .X(net17) );
  SAEDHVT14_BUF_1 U48 ( .A(net17), .X(net18) );
  SAEDHVT14_BUF_U_0P75 U49 ( .A(net18), .X(net19) );
  SAEDHVT14_BUF_U_0P75 U50 ( .A(net19), .X(net20) );
  SAEDHVT14_BUF_U_0P75 U51 ( .A(net20), .X(net21) );
  SAEDHVT14_BUF_U_0P5 U52 ( .A(net21), .X(net22) );
  SAEDHVT14_BUF_1 U53 ( .A(net22), .X(net23) );
  SAEDHVT14_BUF_1 U54 ( .A(net23), .X(net24) );
endmodule


module SNPS_CLOCK_GATE_HIGH_dice_game_1 ( CLK, EN, ENCLK );
  input CLK, EN;
  output ENCLK;
  wire   net125, net9, net10, net11, net12, net13, net14, net15, net16;

  SAEDHVT14_LDNQ_V1_2 latch ( .D(EN), .G(CLK), .Q(net125) );
  SAEDHVT14_AN2_1 main_gate ( .A1(net16), .A2(CLK), .X(ENCLK) );
  SAEDHVT14_BUF_U_0P75 U39 ( .A(net125), .X(net9) );
  SAEDHVT14_BUF_U_0P75 U40 ( .A(net9), .X(net10) );
  SAEDHVT14_BUF_1 U41 ( .A(net10), .X(net11) );
  SAEDHVT14_BUF_U_0P5 U42 ( .A(net11), .X(net12) );
  SAEDHVT14_BUF_1 U43 ( .A(net12), .X(net13) );
  SAEDHVT14_BUF_U_0P75 U44 ( .A(net13), .X(net14) );
  SAEDHVT14_BUF_U_0P75 U45 ( .A(net14), .X(net15) );
```

```
  SAEDHVT14_BUF_1 U46 ( .A(net15), .X(net16) );
endmodule


module dice_game ( clock, rst, roll, dice1, dice2, win, lose, point );
  input [3:0] dice1;
  input [3:0] dice2;
  output [3:0] point;
  input clock, rst, roll;
  output win, lose;
  wire   N24, N25, N26, N27, N28, N51, N52, N53, N54, N55, N56, N57, net131,
         net136, n7, n8, n9, n10, n11, n12, n13, n14, n15, n16, n17, n18, n19,
         n20, n21, n22, n23, n24, n25, n26, n27, n28, n29, n30, n31, n32, n33,
         n34, n35, n36, n37, n38, n39, n40, n41, n42, net2, net3, net4, net5,
         net6, net7, net8, net1, net9, net10, net11, net12;
  wire   [1:0] ps;
  wire   [3:0] sum;

  SNPS_CLOCK_GATE_HIGH_dice_game_0 clk_gate_win_reg ( .CLK(clock), .EN(N51),
        .ENCLK(net131) );
  SNPS_CLOCK_GATE_HIGH_dice_game_1 clk_gate_sum_reg ( .CLK(clock), .EN(N28),
        .ENCLK(net136) );
  SAEDHVT14_AO32_1 U4 ( .A1(sum[0]), .A2(n9), .A3(sum[1]), .B1(n10), .B2(n11),
        .X(n8) );
  SAEDHVT14_OAI22_0P5 U6 ( .A1(sum[2]), .A2(ps[1]), .B1(sum[3]), .B2(n14), .X(
        n9) );
  SAEDHVT14_OAI22_0P5 U9 ( .A1(n11), .A2(n13), .B1(ps[1]), .B2(n15), .X(n42)
        );
  SAEDHVT14_INV_0P5 U10 ( .A(ps[1]), .X(n11) );
  SAEDHVT14_NR2_1 U11 ( .A1(n16), .A2(n17), .X(N57) );
  SAEDHVT14_NR2_1 U12 ( .A1(n18), .A2(n17), .X(N56) );
  SAEDHVT14_NR2_1 U13 ( .A1(n19), .A2(n17), .X(N55) );
  SAEDHVT14_NR2_1 U14 ( .A1(n20), .A2(n17), .X(N54) );
  SAEDHVT14_OR3_0P5 U15 ( .A1(n21), .A2(n22), .A3(n12), .X(n17) );
  SAEDHVT14_INV_0P5 U16 ( .A(n23), .X(n21) );
  SAEDHVT14_AO32_1 U17 ( .A1(n24), .A2(ps[1]), .A3(n25), .B1(n23), .B2(n12),
```

dice_lp.tcl × holdfix.tcl ×

```
        .X(N53) );
  SAEDHVT14_AO33_1 U18 ( .A1(n18), .A2(n16), .A3(sum[1]), .B1(sum[3]), .B2(
        sum[2]), .B3(n26), .X(n12) );
  SAEDHVT14_NR2_1 U19 ( .A1(sum[1]), .A2(sum[0]), .X(n26) );
  SAEDHVT14_INV_0P5 U20 ( .A(sum[2]), .X(n18) );
  SAEDHVT14_NR2_1 U21 ( .A1(n7), .A2(n15), .X(n25) );
  SAEDHVT14_AO32_1 U22 ( .A1(ps[1]), .A2(N28), .A3(n7), .B1(n22), .B2(n23),
        .X(N52) );
  SAEDHVT14_NR3_1 U23 ( .A1(n27), .A2(n20), .A3(n19), .X(n22) );
  SAEDHVT14_INV_0P5 U24 ( .A(sum[1]), .X(n19) );
  SAEDHVT14_INV_0P5 U25 ( .A(sum[0]), .X(n20) );
  SAEDHVT14_EO2_0P5 U26 ( .A1(n16), .A2(sum[2]), .X(n27) );
  SAEDHVT14_OAI21_0P5 U27 ( .A1(ps[1]), .A2(n13), .B(n23), .X(N51) );
  SAEDHVT14_OA21B_1 U29 ( .A1(n24), .A2(n7), .B(n15), .X(n28) );
  SAEDHVT14_NR4_0P75 U30 ( .A1(n29), .A2(n30), .A3(n31), .A4(n32), .X(n7) );
  SAEDHVT14_EO2_0P5 U31 ( .A1(sum[2]), .A2(point[2]), .X(n32) );
  SAEDHVT14_EO2_0P5 U32 ( .A1(sum[3]), .A2(point[3]), .X(n31) );
  SAEDHVT14_EO2_0P5 U33 ( .A1(sum[0]), .A2(point[0]), .X(n30) );
  SAEDHVT14_EO2_0P5 U34 ( .A1(sum[1]), .A2(point[1]), .X(n29) );
  SAEDHVT14_AN4_1 U35 ( .A1(sum[0]), .A2(sum[1]), .A3(n16), .A4(sum[2]), .X(
        n24) );
  SAEDHVT14_INV_0P5 U36 ( .A(sum[3]), .X(n16) );
  SAEDHVT14_INV_0P5 U37 ( .A(n15), .X(N28) );
  SAEDHVT14_INV_0P5 U39 ( .A(ps[0]), .X(n13) );
  SAEDHVT14_EN3_1 U40 ( .A1(dice2[3]), .A2(dice1[3]), .A3(n33), .X(N27) );
  SAEDHVT14_OAI21_0P5 U41 ( .A1(dice1[2]), .A2(n34), .B(n35), .X(n33) );
  SAEDHVT14_AO21B_0P5 U42 ( .A1(n34), .A2(dice1[2]), .B(n36), .X(n35) );
  SAEDHVT14_EN3_1 U43 ( .A1(n36), .A2(n34), .A3(dice1[2]), .X(N26) );
  SAEDHVT14_OAI21_0P5 U44 ( .A1(n37), .A2(n38), .B(n39), .X(n34) );
  SAEDHVT14_AO21B_0P5 U45 ( .A1(n37), .A2(n38), .B(dice2[1]), .X(n39) );
  SAEDHVT14_INV_0P5 U46 ( .A(dice1[1]), .X(n38) );
  SAEDHVT14_INV_0P5 U47 ( .A(dice2[2]), .X(n36) );
  SAEDHVT14_EN3_1 U48 ( .A1(dice2[1]), .A2(dice1[1]), .A3(n37), .X(N25) );
  SAEDHVT14_EO2_0P5 U50 ( .A1(dice2[0]), .A2(dice1[0]), .X(N24) );
  SAEDHVT14_FDPRBQ_V2LP_1 ps_reg_1_ ( .D(net9), .CK(clock), .RD(n41), .Q(ps[1]) );
  SAEDHVT14_FDPRBQ_V2LP_1 point_reg_1_ ( .D(N55), .CK(net131), .RD(n41), .Q(
        point[1]) );
  SAEDHVT14_FDPRBQ_V2LP_1 point_reg_0_ ( .D(net2), .CK(net131), .RD(n41), .Q(
        point[0]) );
  SAEDHVT14_FDPRBQ_V2LP_1 point_reg_3_ ( .D(N57), .CK(net131), .RD(n41), .Q(
```

```
dice_lp.tcl                                    holdfix.tcl
SAEDHVT14_FDPRBQ_V2LP_1 point_reg_0_ ( .D(net2), .CK(net131), .RD(n41), .Q(
      point[0]) );
SAEDHVT14_FDPRBQ_V2LP_1 point_reg_3_ ( .D(N57), .CK(net131), .RD(n41), .Q(
      point[3]) );
SAEDHVT14_FDPRBQ_V2LP_1 point_reg_2_ ( .D(N56), .CK(net131), .RD(n41), .Q(
      point[2]) );
SAEDHVT14_FDPRBQ_V2LP_1 sum_reg_0_ ( .D(N24), .CK(net136), .RD(n41), .Q(
      sum[0]) );
SAEDHVT14_FDPRBQ_V2LP_1 sum_reg_1_ ( .D(N25), .CK(net136), .RD(n41), .Q(
      sum[1]) );
SAEDHVT14_FDPRBQ_V2LP_1 sum_reg_2_ ( .D(N26), .CK(net136), .RD(n41), .Q(
      sum[2]) );
SAEDHVT14_FDPRBQ_V2LP_1 sum_reg_3_ ( .D(N27), .CK(net136), .RD(n41), .Q(
      sum[3]) );
SAEDHVT14_FDPRBQ_V2LP_1 ps_reg_0_ ( .D(net1), .CK(clock), .RD(n41), .Q(ps[0]) );
SAEDHVT14_FDPRBQ_V2LP_1 win_reg ( .D(net12), .CK(net131), .RD(n41), .Q(win)
      );
SAEDHVT14_FDPRBQ_V2LP_1 lose_reg ( .D(net8), .CK(net131), .RD(n41), .Q(lose)
      );
SAEDHVT14_INV_S_1 U51 ( .A(rst), .X(n41) );
SAEDHVT14_ND2_MM_0P5 U52 ( .A1(roll), .A2(n13), .X(n15) );
SAEDHVT14_ND2_MM_0P5 U53 ( .A1(n28), .A2(ps[1]), .X(n23) );
SAEDHVT14_AOI21_0P75 U54 ( .A1(n7), .A2(N28), .B(n8), .X(n40) );
SAEDHVT14_OR2_MM_0P75 U55 ( .A1(n12), .A2(n13), .X(n10) );
SAEDHVT14_AOI21_0P75 U56 ( .A1(sum[2]), .A2(N28), .B(n11), .X(n14) );
SAEDHVT14_ND2_MM_0P5 U57 ( .A1(dice2[0]), .A2(dice1[0]), .X(n37) );
SAEDHVT14_BUF_U_0P75 U2 ( .A(N54), .X(net2) );
SAEDHVT14_BUF_U_0P75 U3 ( .A(n40), .X(net3) );
SAEDHVT14_BUF_U_0P75 U5 ( .A(net3), .X(net4) );
SAEDHVT14_BUF_U_0P75 U7 ( .A(N53), .X(net5) );
SAEDHVT14_BUF_1 U8 ( .A(net5), .X(net6) );
SAEDHVT14_BUF_U_0P75 U28 ( .A(net6), .X(net7) );
SAEDHVT14_BUF_1 U38 ( .A(net7), .X(net8) );
SAEDHVT14_BUF_1 U1 ( .A(n42), .X(net1) );
SAEDHVT14_BUF_1 U49 ( .A(net4), .X(net9) );
SAEDHVT14_BUF_U_0P75 U58 ( .A(N52), .X(net10) );
SAEDHVT14_BUF_U_0P5 U59 ( .A(net10), .X(net11) );
SAEDHVT14_BUF_U_0P5 U60 ( .A(net11), .X(net12) );
endmodule
```

REPORTS:

- **check_timing report:**

```
pt_shell> check_timing
Information: Checking 'no_input_delay'.
Information: Checking 'no_driving_cell'.
Information: Checking 'unconstrained_endpoints'.
Information: Checking 'unexpandable_clocks'.
Information: Checking 'latch_fanout'.
Information: Checking 'no_clock'.
Information: Checking 'partial_input_delay'.
Information: Checking 'generic'.
Information: Checking 'loops'.
Information: Checking 'generated_clocks'.
Information: Checking 'pulse_clock_non_pulse_clock_merge'.
Information: Checking 'pll_configuration'.
Information: Checking 'voltage_level'.
check_timing succeeded.
1
pt_shell>
```

- **hold timing report:**

```
****************************************
Report : timing
         -path_type full
         -delay_type min
         -slack_lesser_than 0.00
         -max_paths 20
         -sort_by slack
Design : dice_game
Version: V-2023.12-SP4
Date   : Fri Feb 14 16:08:30 2025
****************************************

No paths with slack less than 0.00.

1
```

- **setup timing report:**

```
****************************************
Report : timing
         -path_type full
         -delay_type max
         -slack_lesser_than 0.00
         -max_paths 20
         -sort_by slack
Design : dice_game
Version: V-2023.12-SP4
Date   : Fri Feb 14 16:08:30 2025
****************************************

No paths with slack less than 0.00.

1
```

By adding buffers, the hold violations in the design were fixed while keeping the circuit working correctly. The updated TCL script helps repeat these changes easily.