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Submitted to
School of Electronics Engineering

MVLD502L – DIGITAL INTEGRATED CIRCUIT DESIGN

COURSE PROJECT

SUBMITTED BY

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IMPLEMENTATION OF A BOOLEAN FUNCTION USING CMOS , PASS TRANSISTOR AND TRANSMISSION GATE DESIGN STYLES AND COMPARING THEM BY MAINTAINING A CONSTANT AREA

AIM : To implement a boolean function using cmos, pass transistor and transmission gate design styles and comparing delay and average power dissipation by maintaining a constant area.

SOFTWARE TOOL USED : CADENCE , UMC 180 nm technology .

INTRODUCTION :

Very Large Scale Integrated circuits are consequential for designing high performance and portable devices. The performance parameters like delay, area and power are the main parameters that play an important role in the VLSI technology. The basic logic gates are fundamental components and accommodate as the building blocks to VLSI digital logic circuits utilising combinational logic.The principle of operation on basic gates is that the circuit operation on two voltage levels considered in to logic levels as logic 0 and logic 1.When applied inputs either logic 0 or logic 1 will get a output gate replication depends upon the particular logic of the gate. A boolean function is defined by an algebraic expression consisting of binary variables, constants such as 0 and 1, and logic operation symbols. Where as a variable or symbol which is generally an alphabet that depicts the logical quantities such as 0 or 1. Here we consider the boolean function $F = A'B + A'C + BC$.

CMOS DESIGN STYLE

CMOS is the most commonly used technique in digital circuits. It's a combination of pull-up PMOS network, it will set the output as logic 1 and pull-down NMOS network, it will set the output as logic 0. Both the network cannot be activated and deactivated at a time.

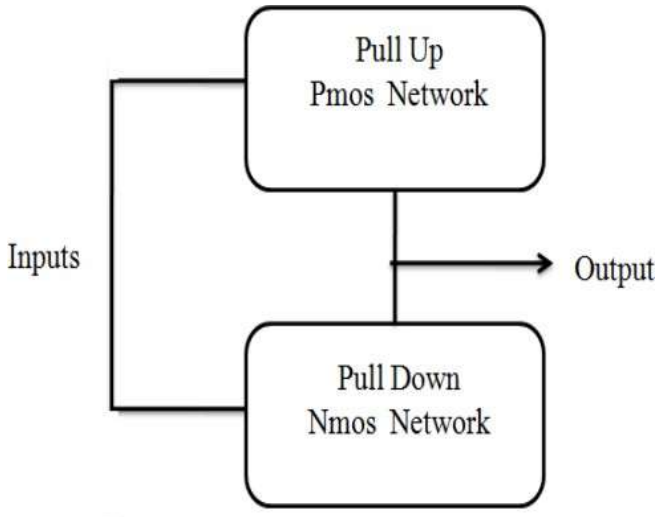

Figure 1: CMOS representation

By using this design technique for boolean function, the output level is not degraded (full swing output), the operation speed is increased (delay has been reduced) and more power and area are consumed, since there are more transistors to design.

PASS TRANSISTOR DESIGN STYLE

A popular and widely-used alternative to complementary CMOS is pass-transistor logic, which attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source/drain terminal.

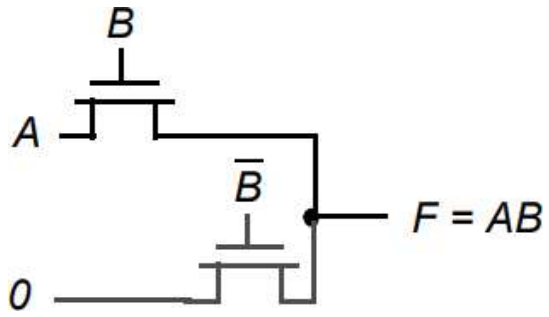

Figure 2: AND gate implementation using pass transistor

TRANSMISSION GATE DESIGN STYLE

A transmission gate can conduct in both directions or block by a control signal with almost any voltage potential analogous to that of relay. It is CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously. Unlike traditional discrete field effect transistors, in a transmission gate the substrate terminal (Bulk) is not connected internally to the source terminal.In transmission gates, static power dissipation and on resistance are reduced.

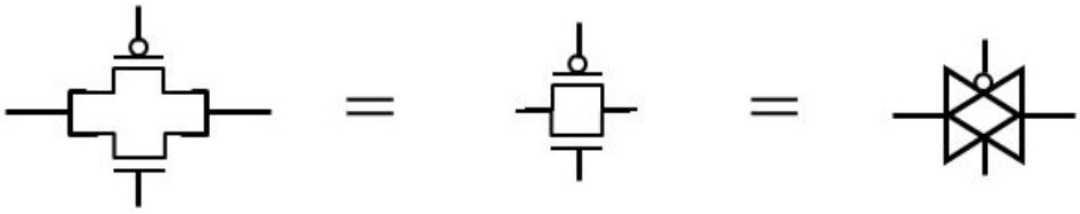

Figure 3: Transmission gate representation

IMPLEMENTATION :

Boolean function being implemented is $F = A'B + A'C + BC$.

CMOS DESIGN STYLE

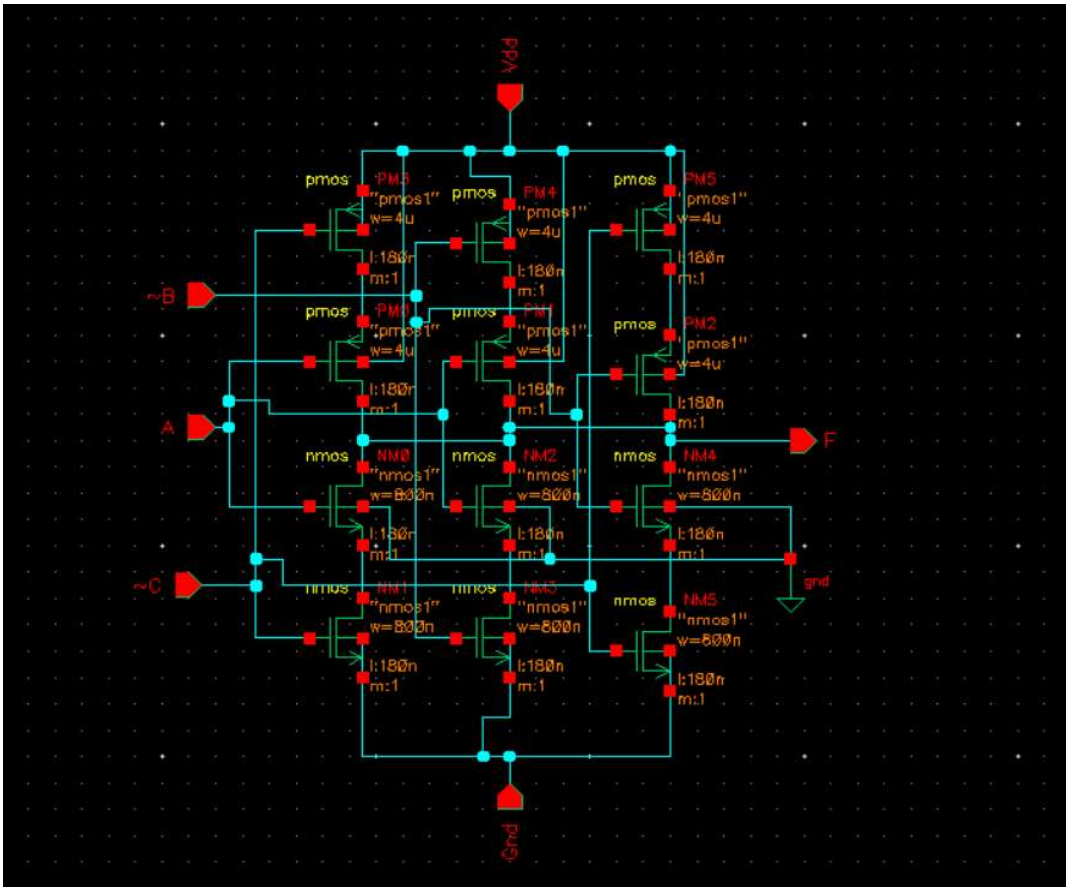

Figure 4: CMOS Schematic

While implementing complementary CMOS logic, NMOS transistors are connected in series in the Pull Down Network, while PMOS transistors are connected in parallel in the Pull Up Network, and vice versa. We have taken a special function in which if we put inverted inputs into the boolean expression, then we get the inverted output. So here, Pull Up Network and Pull Down Network are mirror images of each other. First, we implement the PDN, and then we mirror the PDN with PMOS transistors to implement PUN.

As a result, PMOS stack and PMOS sizes in the Pull-up network are reduced than in the normal implementation.

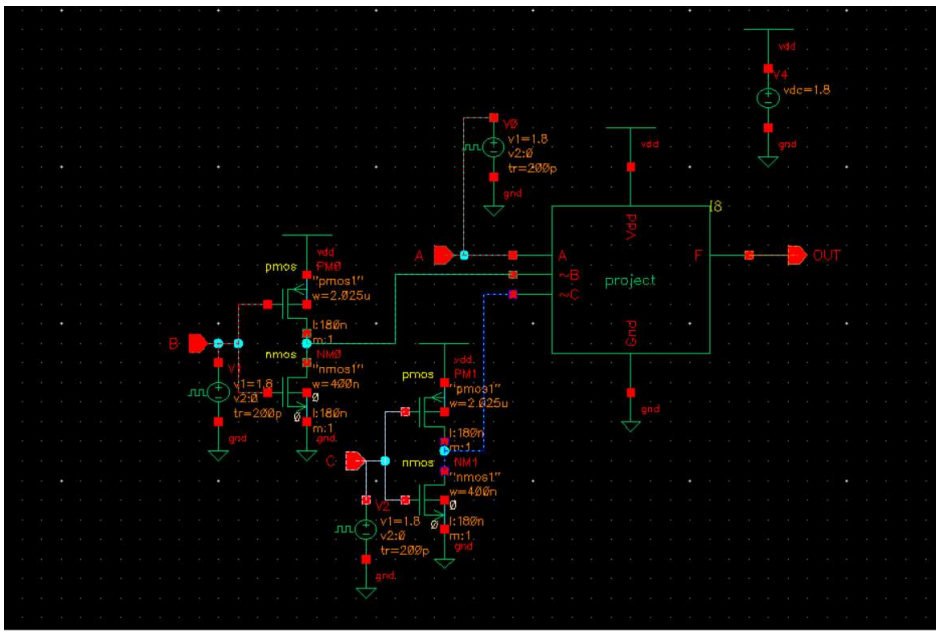

Figure 5: Symbol of CMOS schematic

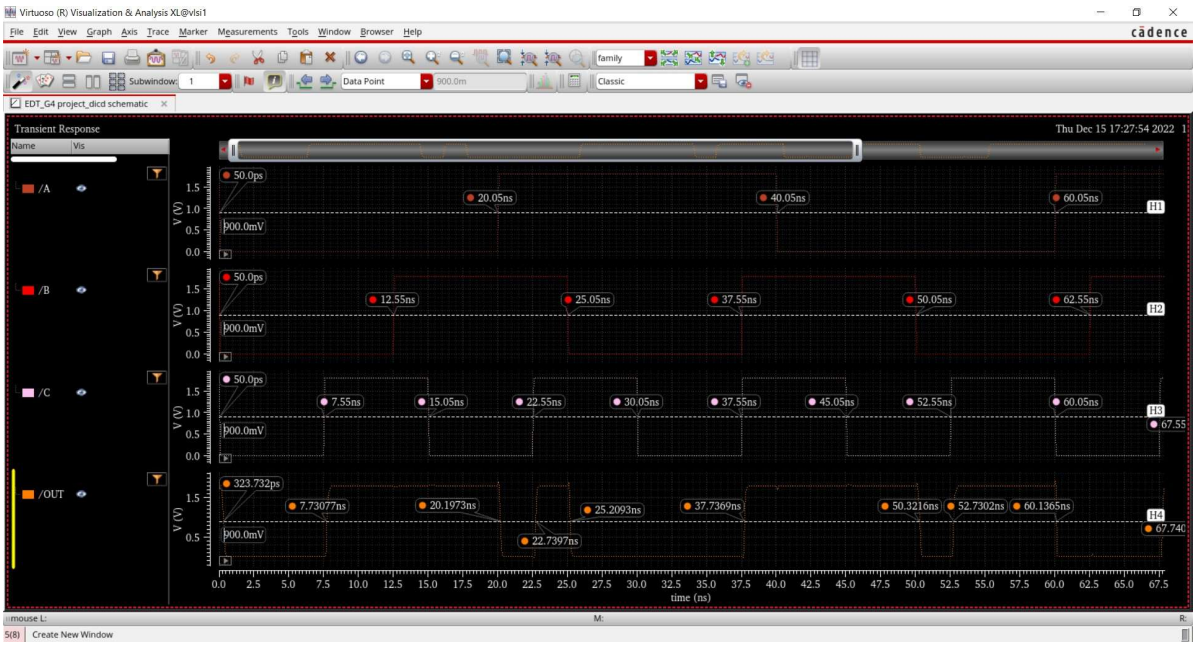

Figure 6: Output of CMOS logic design

PASS TRANSISTOR DESIGN STYLE

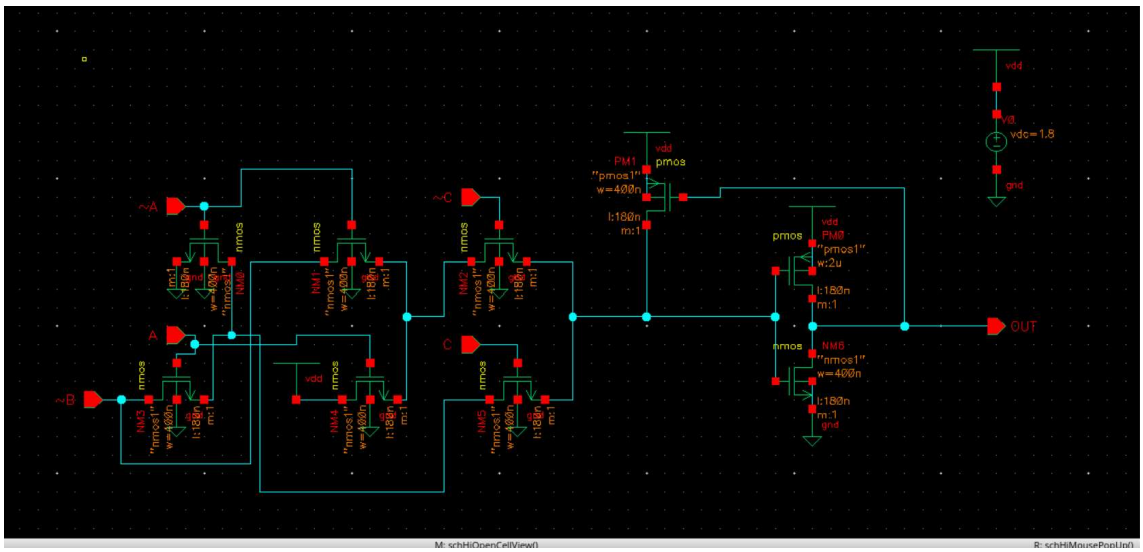

Figure 7: Pass transistor schematic

Here we use level restoring circuit to form a low impedance path from output to Vdd whenever output is high. This eliminates any static power dissipation.

Using parametric analysis, the size of level restorer pmos is determined

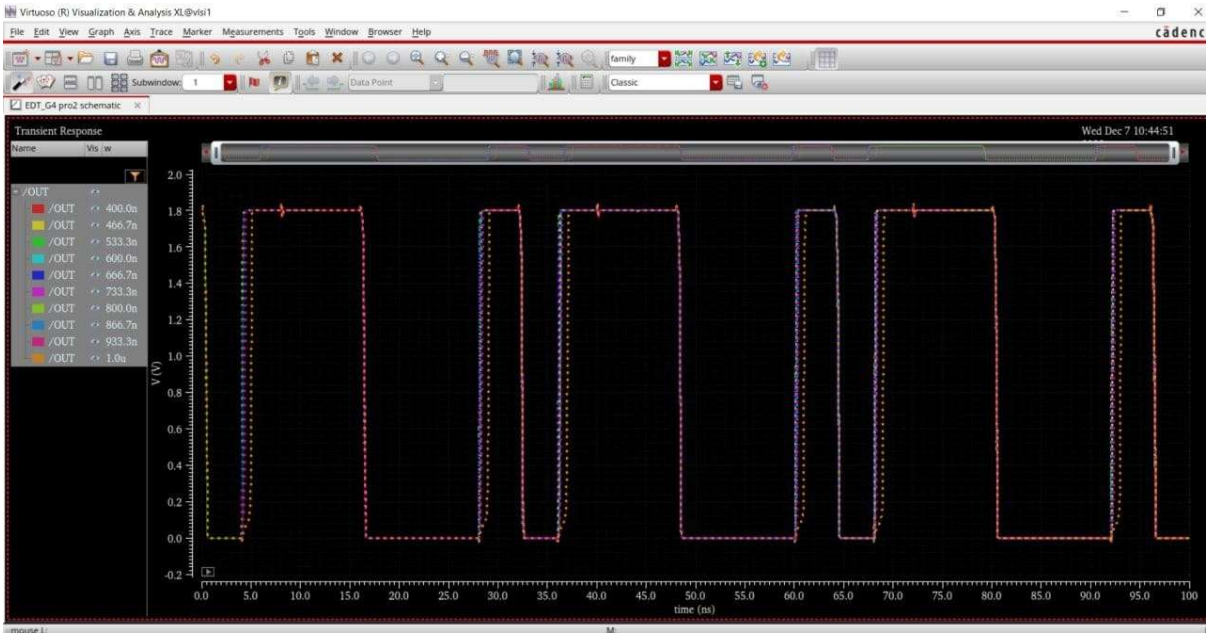

Figure 8 : Outputs with respect to different widths of pmos

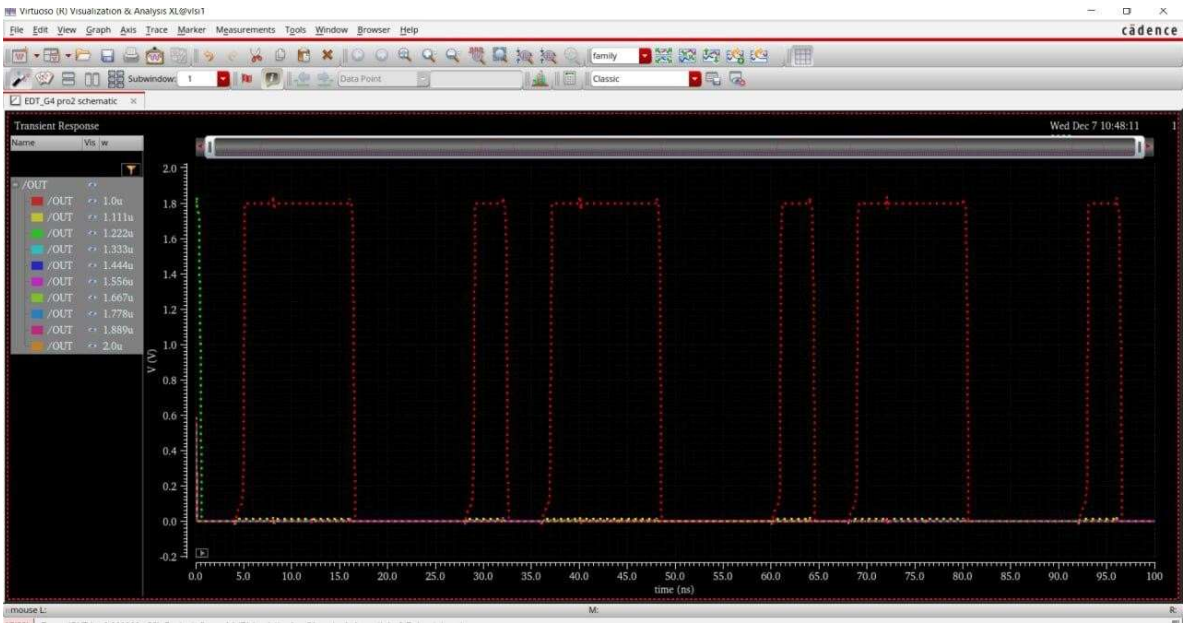

Figure 9 : Outputs with respect to different widths of pmos

Here we have taken minimum size of pmos width as 400 nm

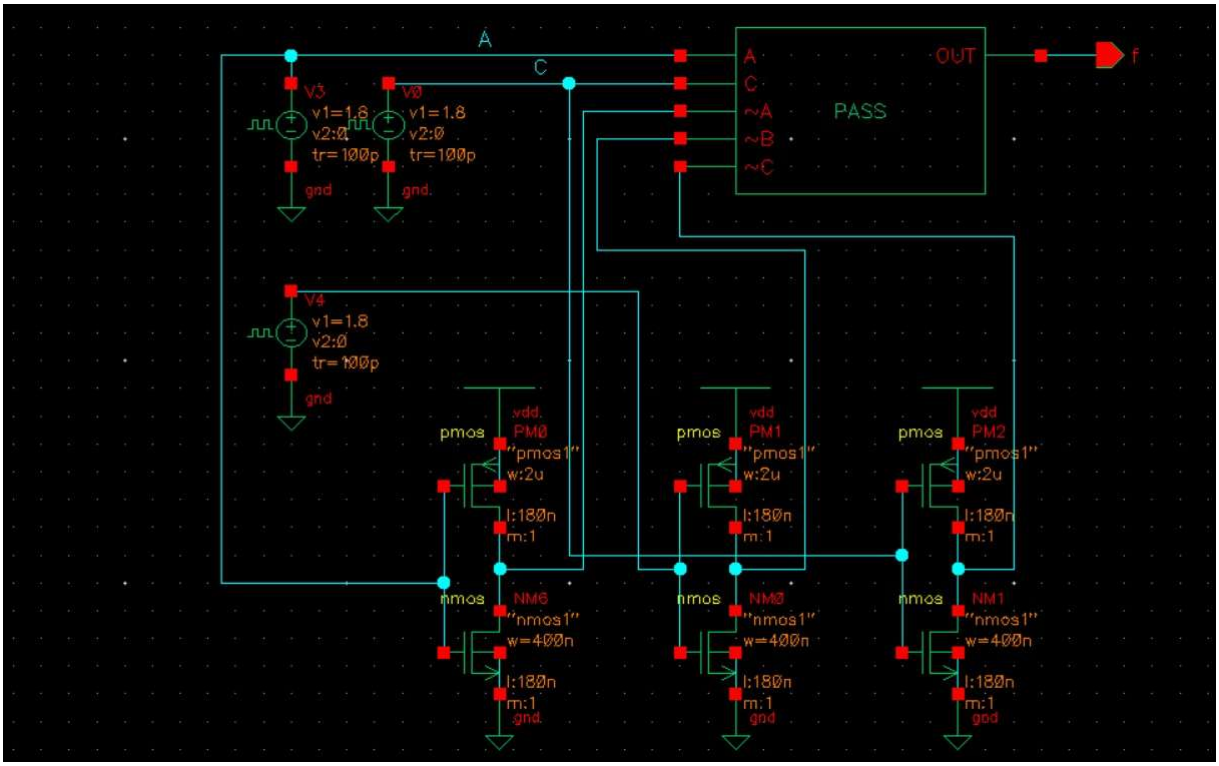

Figure 9: Symbol of pass transistor schematic

Figure 10 : Output of pass transistor logic design

TRANSMISSION GATE DESIGN STYLE

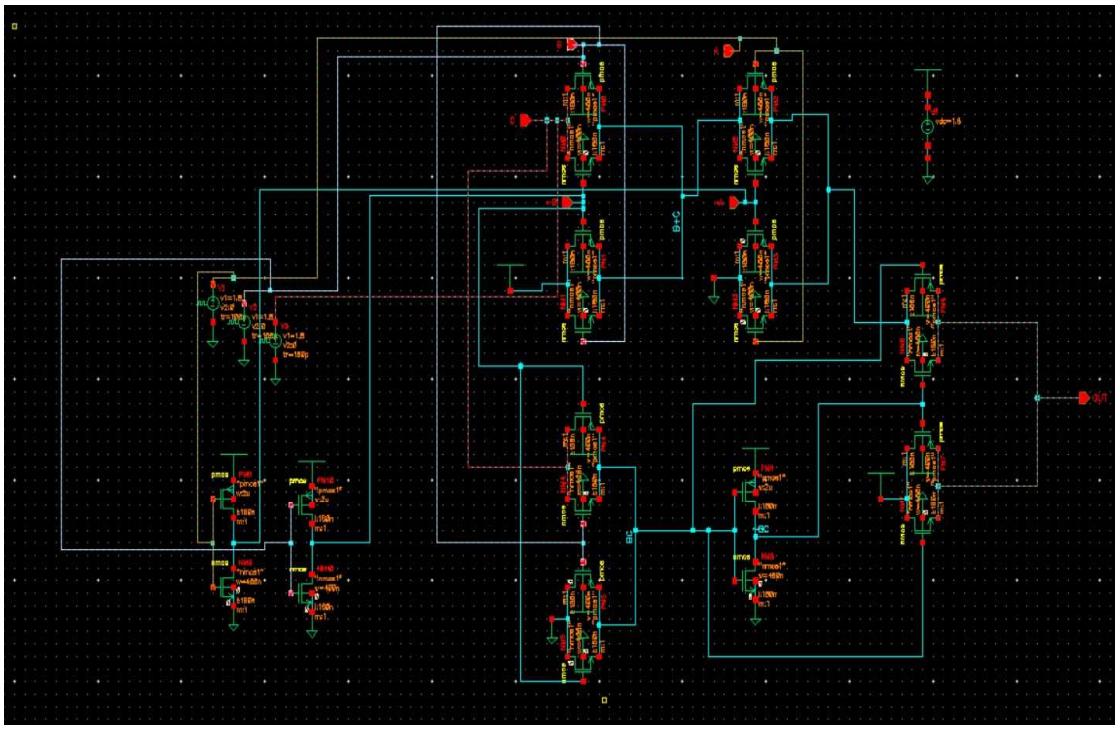

Figure 11: Transmission gate schematic

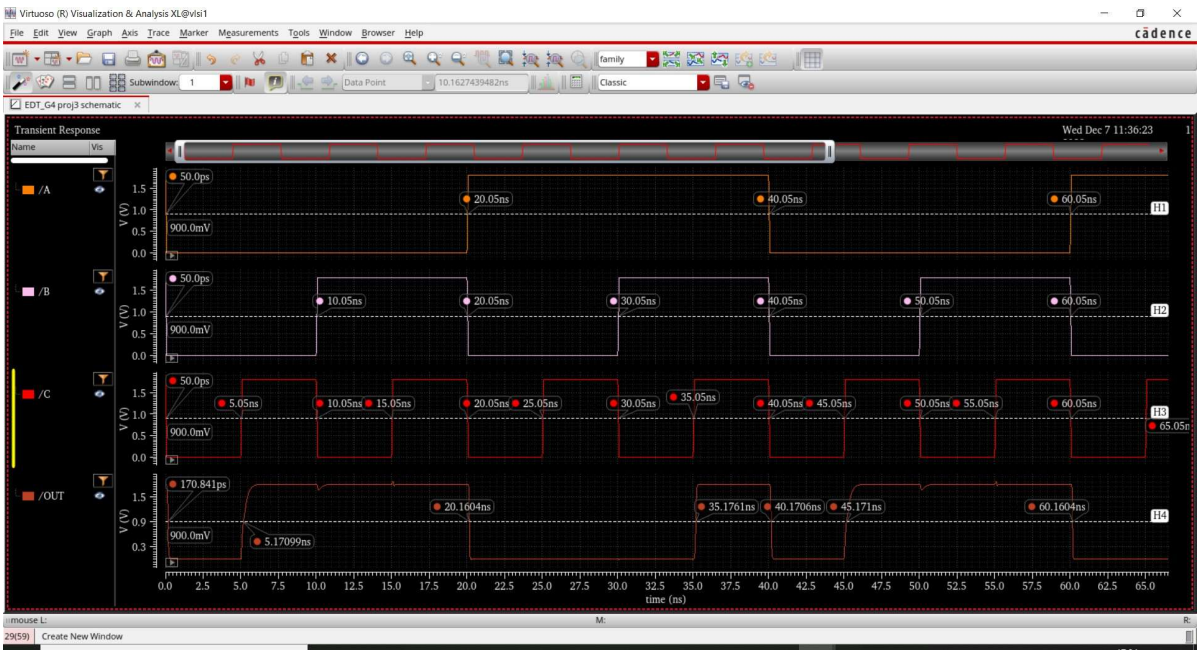

Figure 12 : Output of transmission gate logic design

COMPARISON :

Here we are comparing delay and average power dissipation by maintaining a constant area. The area of all designs is 6 p sq.metres and rise time , fall time of inputs are 100 p sec. Length of pmos and nmos of all logic design styles are 180 nm.

CMOS DESIGN STYLE

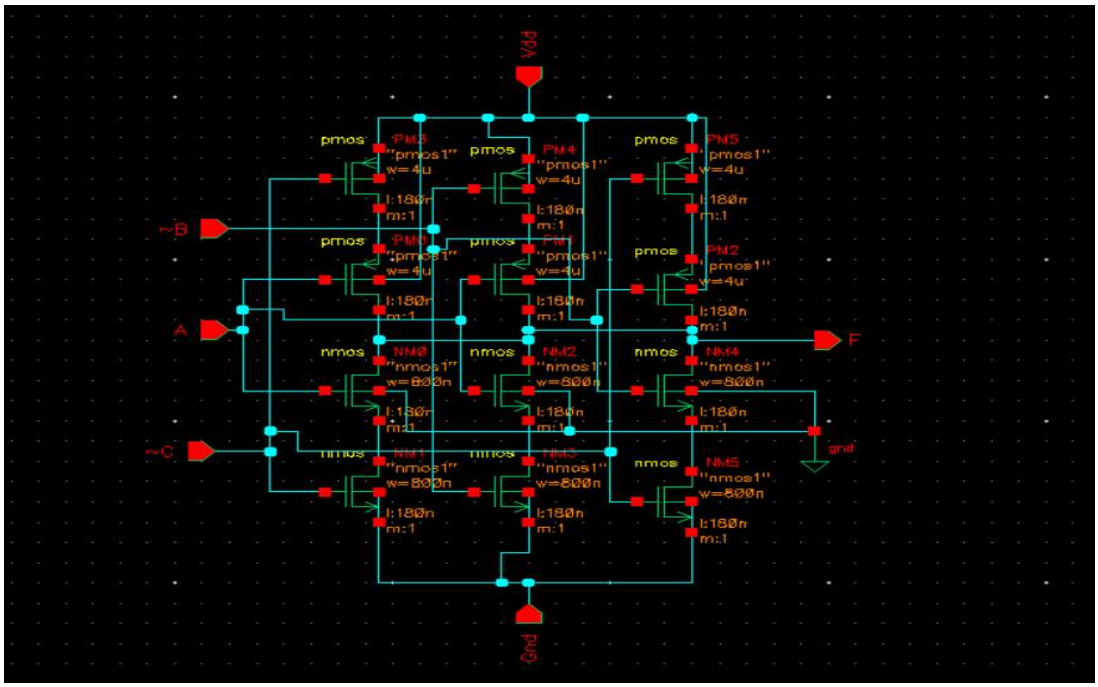

Figure 13: CMOS schematic

The width of pmos and nmos of the CMOS logic design are 4 µm and 800 nm respectively.

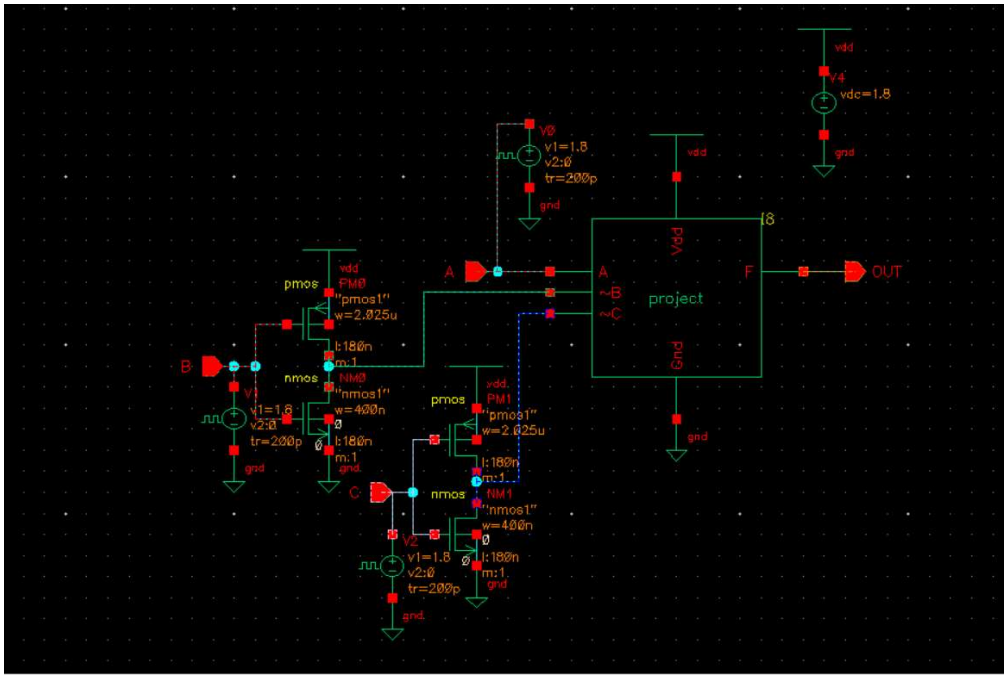

Figure 14 : Symbol of cmos schematic

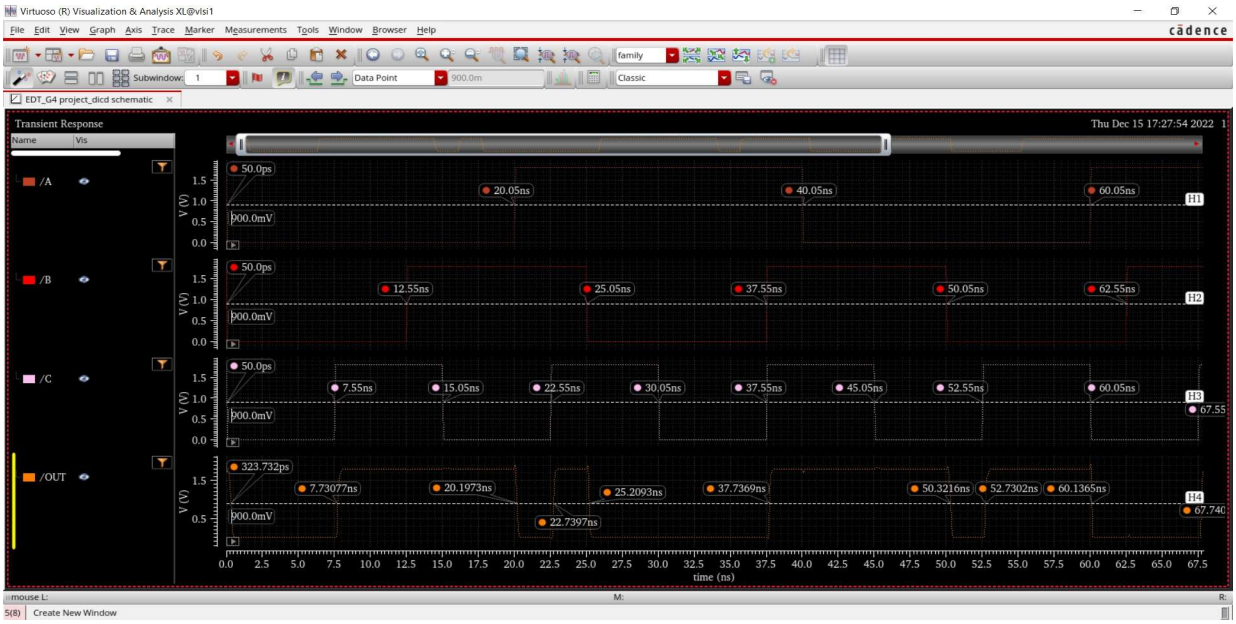

Figure 15 : Obtained outputs with delays of cmos logic design

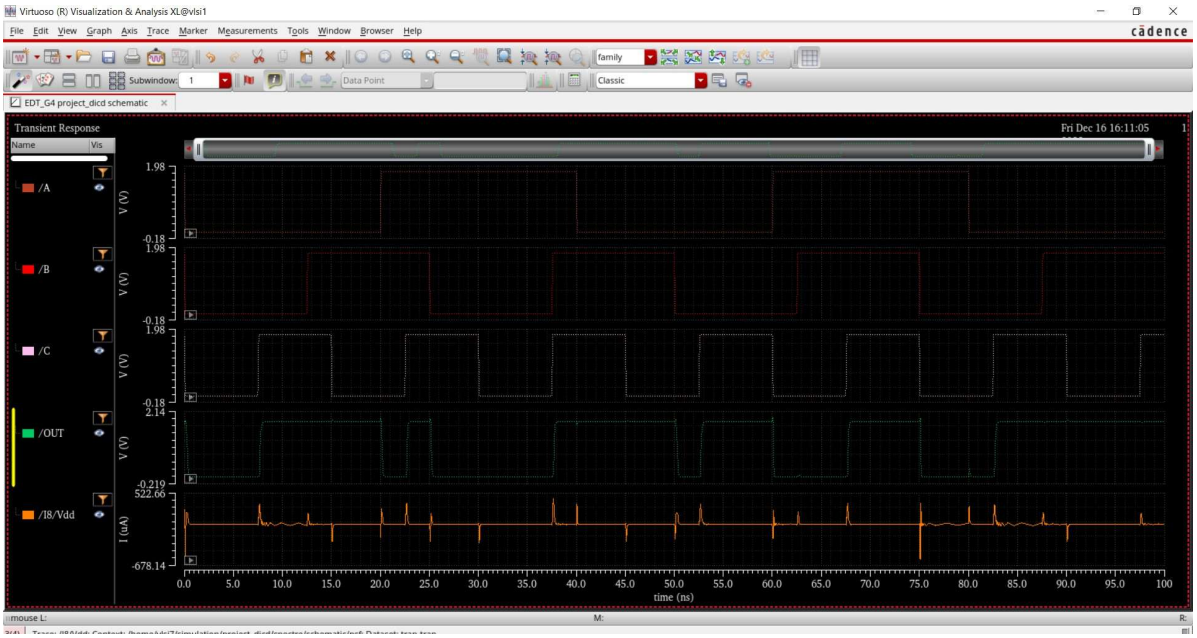

Figure 16: Transition current of cmos logic design

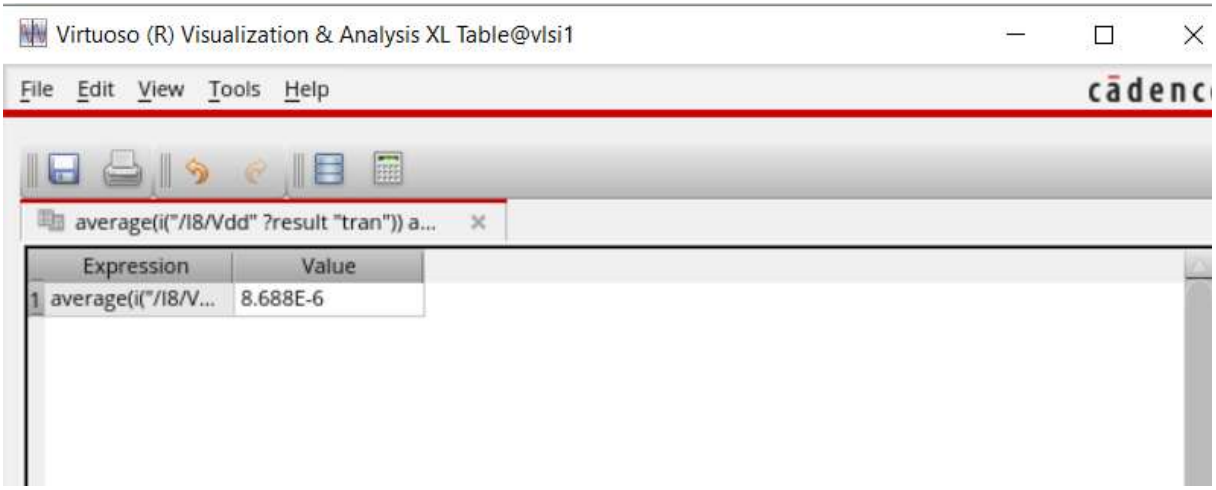

Figure 17 : Cmos average power dissipation

PASS TRANSISTOR DESIGN STYLE

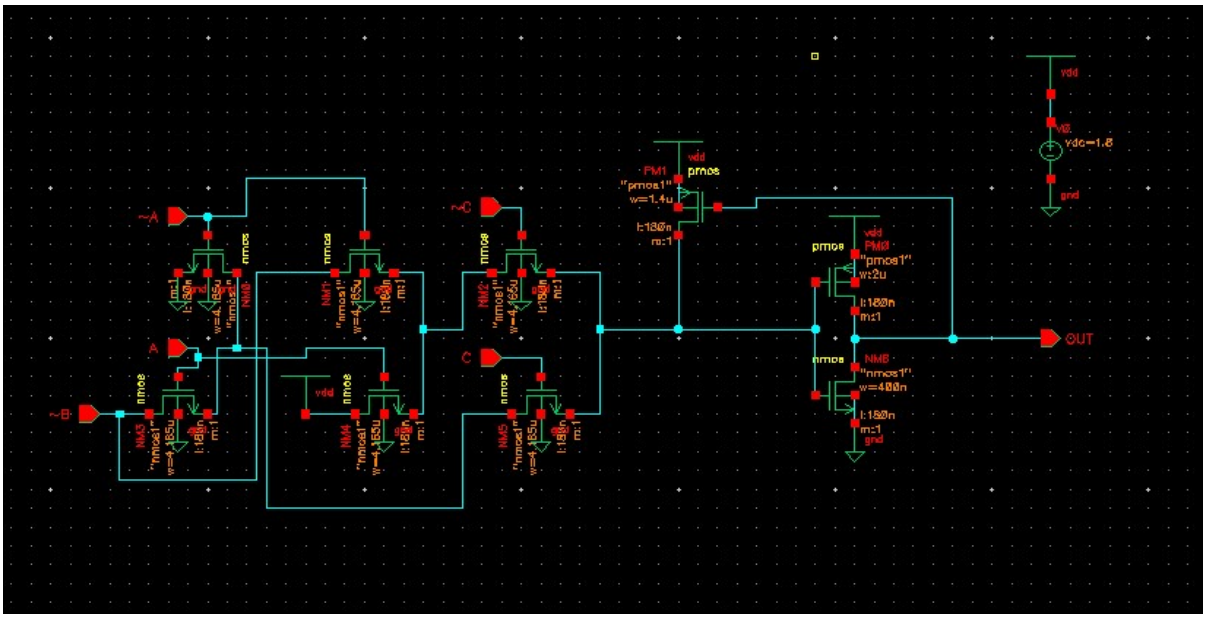

Figure 18 : Pass transistor schematic

In pass transistor logic design, the width of nmos is 1.65 µm and level restorer pmos width is 1.4 µm

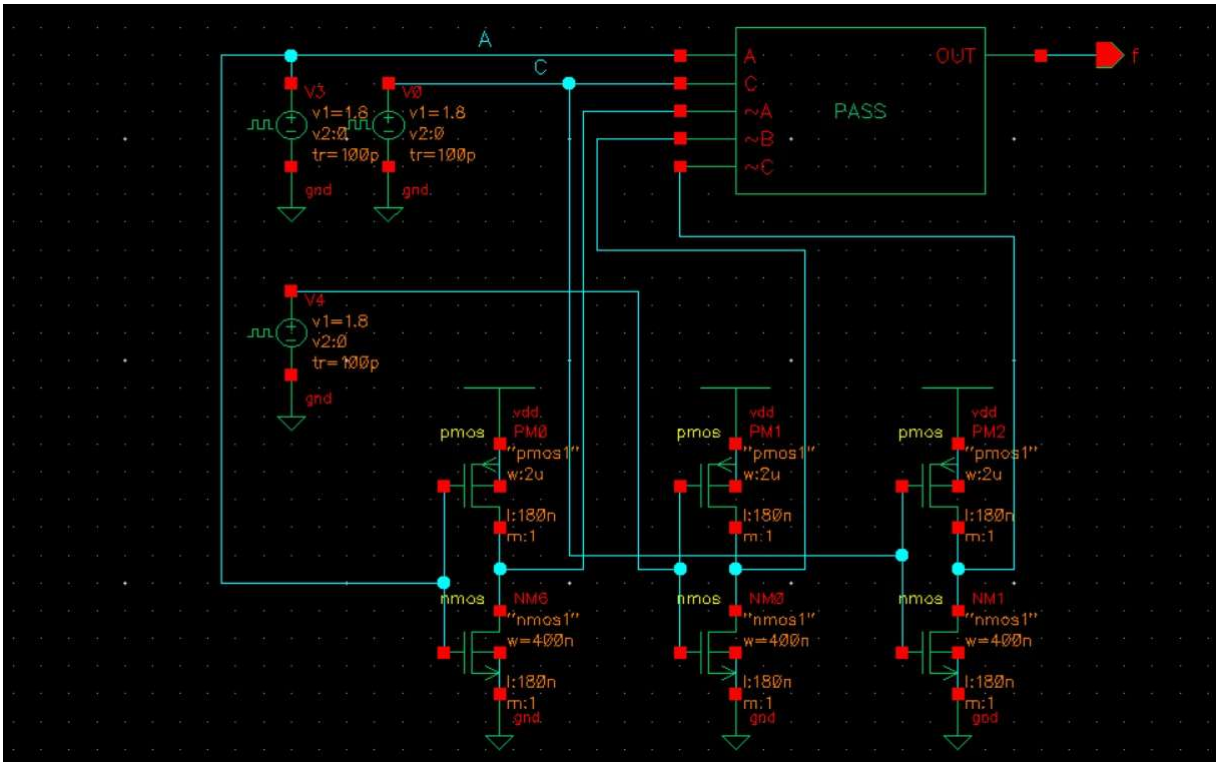

Figure 19 : Symbol of pass transistor schematic

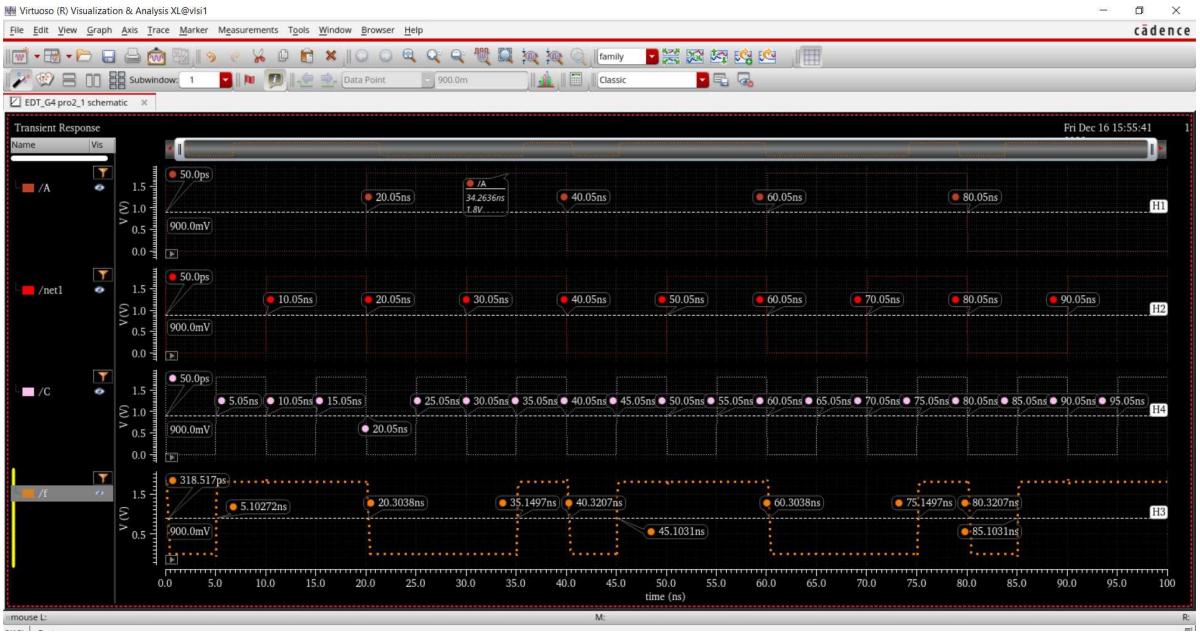

Figure 20 : Obtained outputs with delays of pass transistor logic design

Figure 21: Transition current of pass transistor logic design

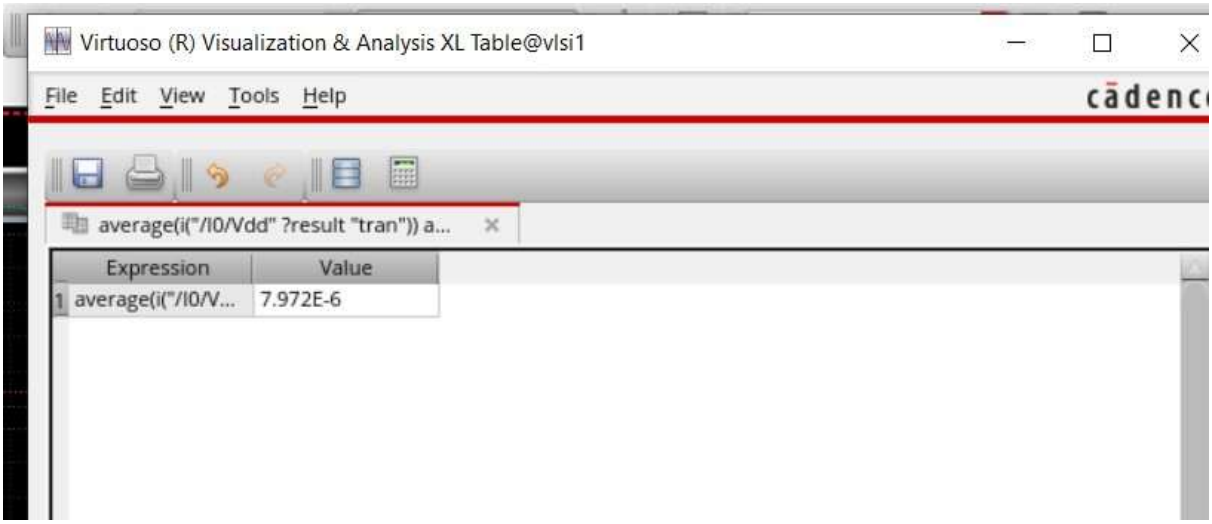

Figure 22 : Pass transistor average power dissipation

TRANSMISSION GATE DESIGN STYLE

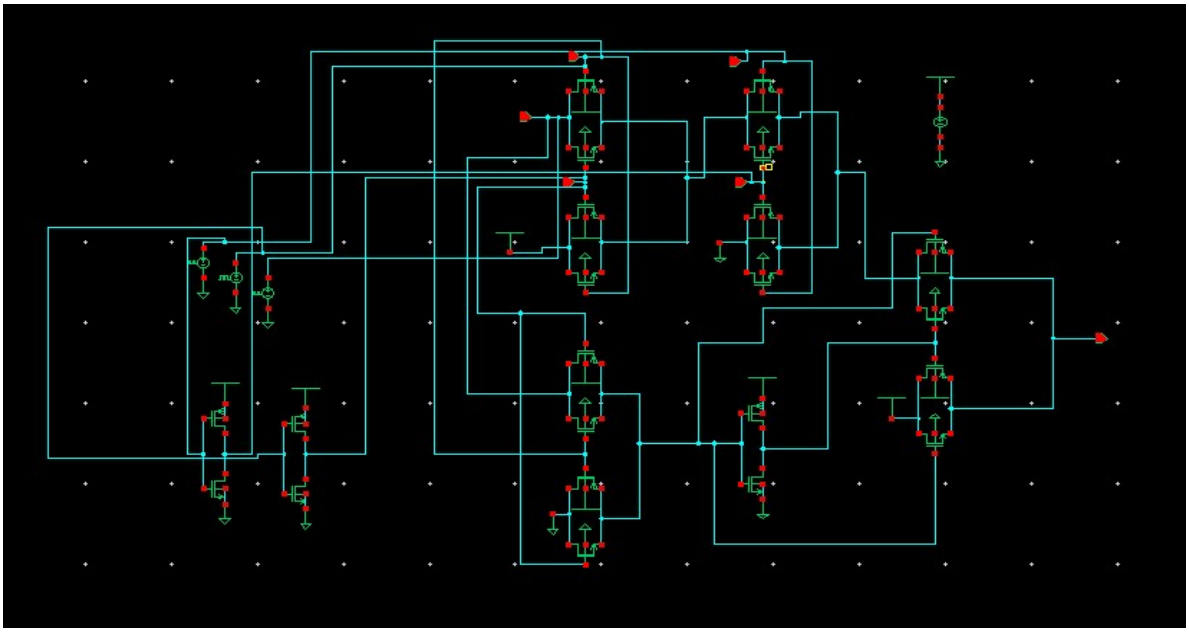

Figure 23 : Transmission gate schematic

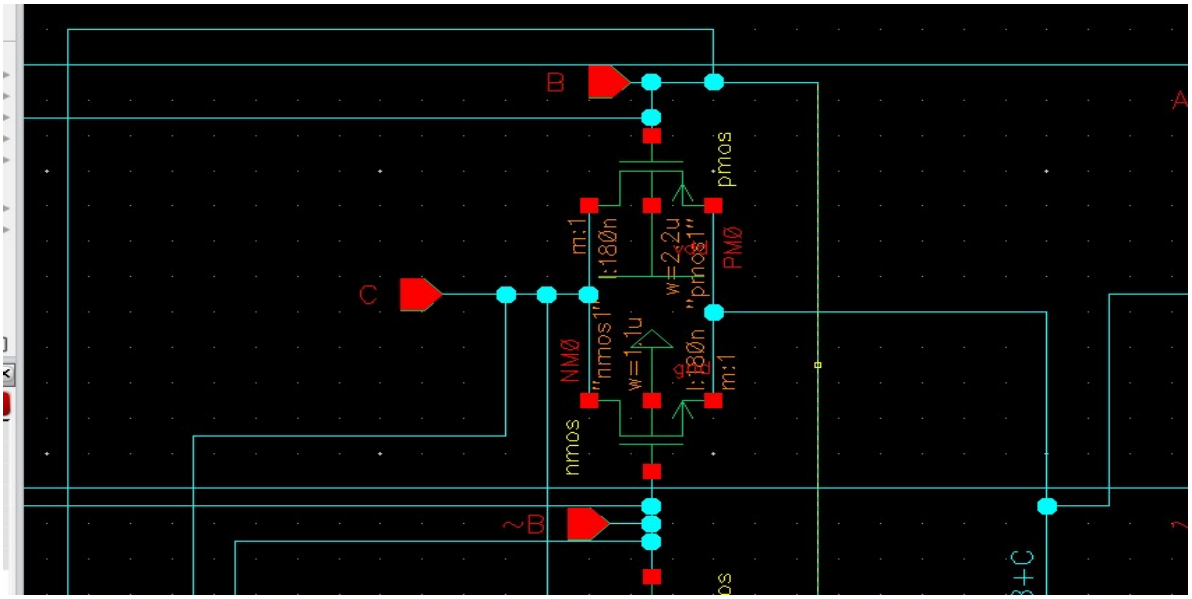

Figure 24 : Transmission gate pmos and nmos sizes

The width of pmos and nmos of the transmission gate logic design are 2.2 µm and 1.1 µm respectively.

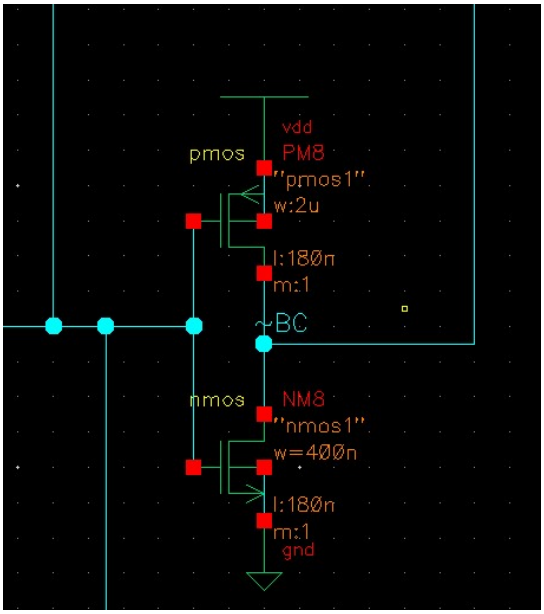

Figure 25 : inverter pmos and nmos sizes

The width of pmos and nmos of the inverter are 2 µm and 400 nm respectively.

Figure 26 : Obtained outputs with delays and transition current of transmission gate logic design

Figure 27 : Transmission gate average power dissipation

OBSERVATION :

	CMOS Logic	Pass Transistor Logic	Transmission Gate Logic
Number of Transistors	16	15	22
Delay (n sec)	0.1731	0.1523	0.1167
Average power dissipation (µ W)	8.688	7.972	8.97

RESULT :

For constant area ,

1. The delay of the transmission gate logic is low because static power dissipation and on resistance are reduced.
2. Power dissipation of pass transistor logic is low due to the use of a level restorer .

CONCLUSION :

In this project , we have designed boolean function $F = A'B + A'C + BC$ using CMOS , pass transistor and transmission gate design styles in cadence virtuoso gpdk 180 nm technology . A comparative analysis is made maintaining a constant area of 6 p sq.meter. This project provides the basis for selecting a design style for a boolean function based on requirement.