Architecture-Level Modeling of Photonic Deep Neural Network Accelerators

Tanner Andrulis

MIT

Cambridge, USA
andrulis@mit.edu

Gohar Irfan Chaudhry *MIT* Cambridge, USA girfan@mit.edu Vinith M. Suriyakumar *MIT*Cambridge, USA vinithms@mit.edu

Joel S. Emer MIT, Nvidia Cambridge, USA jsemer@mit.edu

Vivienne Sze MIT Cambridge, USA sze@mit.edu

Abstract—Photonics is a promising technology to accelerate Deep Neural Networks as it can use optical interconnects to reduce data movement energy and it enables low-energy, high-throughput optical-analog computations.

To realize these benefits in a full system (accelerator + DRAM), designers must ensure that the benefits of using the electrical, optical, analog, and digital domains exceed the costs of converting data between domains. Designers must also consider system-level energy costs such as data fetch from DRAM. Converting data and accessing DRAM can consume significant energy, so to evaluate and explore the photonic system space, there is a need for a tool that can model these full-system considerations.

In this work, we show that similarities between Compute-in-Memory (CiM) and photonics let us use CiM system modeling tools to accurately model photonics systems. Bringing modeling tools to photonics enables evaluation of photonic research in a full-system context, rapid design space exploration, co-design, and comparison between systems.

Using our open-source model, we show that cross-domain conversion and DRAM can consume a significant portion of photonic system energy. We then demonstrate optimizations that reduce conversions and DRAM accesses to improve photonic system energy efficiency by up to $3\times$.

Index Terms—photonics, optical computing, photonic computing, compute-in-memory, modeling, accelerator

I. INTRODUCTION

Deep Neural Networks (DNNs) can be energy-intensive to compute due to the movement of large tensors and the many multiply-accumulate (MAC) operations that they require. To address these challenges, photonic systems (accelerator + DRAM) leverage the digital-electrical (DE), analog-electrical (AE), digital-optical (DO), analog-optical (AO) domains. Specifically, optical $(i.e.,\ DO)$ and $(i.e.,\ AE)$ and $(i.e.,\ A$

Unfortunately, in a full system, the benefits of these domains can be limited by the costs of other components. Specifically, systems may pay significant energy to convert data between domains [5]–[9] and to fetch data from DRAM [5], [6]. To evaluate photonic systems, there is a need for a tool that can model these costs. Furthermore, to optimize full systems, the tool must rapidly explore a large co-design space that includes components (*e.g.*, data converters, SRAM buffers,

The model, tutorials, and examples are available in the CiMLoop [1] repository at https://github.com/mit-emze/cimloop.

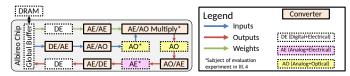


Fig. 1. Albireo architecture. As data traverse the DE, AO, and AE domains, they leverage different movement and reuse opportunities but pay energy for data converters, notated X/Y for conversion from domain X to domain Y.

optical resonators), architecture (*i.e.*, what components are used, how many components, how they connect), workload (*i.e.*, DNN layer types, tensor shapes/values), and mapping (*i.e.*, how the workload is scheduled onto the architecture).

Fortunately, these characteristics are not unique to photonics. Analog Compute-in-Memory (CiM) systems have a large full-system co-design space, leverage the advantages of multiple domains (AE and DE), and face the challenge of high cross-domain conversion energy.

In this work, we show that these similarities let us leverage the open-source CiMLoop [1]–[4] tool to accurately model photonic systems. Bringing this tool to photonics enables researchers to (1) accurately evaluate and compare research contributions in a full-system context (*e.g.*, see how a novel component affects a full system or compare two photonic systems across a range of DNN workloads) (2) perform fast design-space exploration over the large co-design space [1], and (3) share knowledge between the photonics and CiM research communities.

II. PHOTONICS MODELING TOOL

The tool takes as input specifications of a DNN workload, components, and architecture as defined in Section I. The tool maps the given workload on the architecture and outputs full-system area, energy, and throughput estimations.

In this work, we model the Albireo [6] photonic system, which leverages the DE, AE, and AO domains (DO is used in [10]). Fig. 1 shows how Albireo moves data through each domain. DE can reuse data spatially and temporally with multicast/reduction networks, buffer hierarchies, and DRAM. AE can use low-energy analog multiplications, additions, and data movement. AO can further reduce data movement energy with low-energy, high-throughput optical interconnects.

A key design decision in photonic systems is where to cross between domains. This is because (1) energy and area costs of data movement, data reuse, and computations change

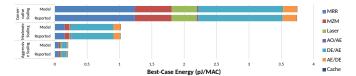


Fig. 2. Energy breakdown validation.

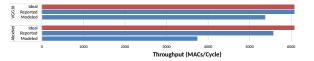


Fig. 3. Throughput for two DNN workloads. CiMLoop captures underutilization, which significantly degraded throughput for Albireo running AlexNet.

significantly between domains [11] and (2) crossing domains requires high-energy data converters, shown in Fig. 1 as X/Y for a domain crossing from X to Y. In particular, AE/DE and DE/AE, commonly known as analog-to-digital and digital-to-analog converters, can consume significant energy [8], [9].

Reducing data converter energy is a key challenge in both CiM and photonic systems [7], [8]. The number of conversions, and thus data conversion energy, can be reduced by leveraging *reuse*: converting a value into a domain and reusing the converted value multiple times in that domain (*e.g.*, convert DE value V_{DE} to AE value V_{AE} with a DE/AE converter, then use the V_{AE} for multiple AE-domain computations) [8].

To model Albireo, we augment CiMLoop's DE and AE component library with AO components such as microring resonators, star couplers, lasers, Mach-Zender modulators, and photodiodes [5], [12]–[20]. We expose each component's data movement and reuse opportunities to CiMLoop's mapper, which finds mappings that leverage available reuse to minimize energy-intensive conversions and DRAM accesses.

III. EVALUATION

We first validate the energy accuracy of the modeling tool. We then evaluate throughput on two DNN workloads, evaluate the full Albireo system with DRAM, and explore architectural approaches to reducing data converter energy.

- 1) Accelerator Energy Breakdown: Fig. 2 shows the modeled versus reported energy breakdown results. We show all components in the Albireo [6] paper, including the accelerator and an off-chip laser. The average overall energy error is 0.4%.
- 2) Throughput: Fig. 3 shows the modeled versus reported throughput for VGG16 [21] and AlexNet [22]. We also include an ideal throughput, which assumes 100% compute unit utilization. While results in [6] are near ideal, we find that modeled throughput is significantly lower when accounting for underutilization due to different DNN weight tensor shapes. In particular, Albireo is designed for unstrided convolutional layers, and fully-connected and strided convolutional severely underutilize Albireo's compute units. These differences illustrate the importance of using a model that can accurately evaluate throughput [1] by capturing many sources of underutilization.
- 3) Full-System (Accelerator+DRAM): Albireo fetches operands from DRAM, but the paper omits DRAM energy. We connect Albireo to DRAM in our model to see how it impacts

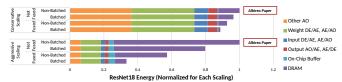


Fig. 4. Memory exploration. Aggressively-scaled Albireo is dominated by DRAM energy. DRAM-energy-reducing operations such as batching and fusion are required to realize the benefits of aggressive scaling,

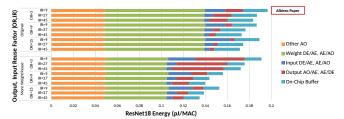


Fig. 5. Increasing the amount of reuse in the analog and photonic domains can reduce data conversion energy, leading to a lower-energy system.

energy. We evaluate two configurations from the Albireo paper based on aggressive (high-energy) and conservative (lowenergy) scaling projections for future optical components.

Fig. 4 shows that for the conservatively-scaled Albireo, DRAM consumes little overall energy, but for the aggressively-scaled Albireo, DRAM consumes 75% of overall system energy. To achieve the potential energy benefits of aggressive scaling, it is critical to reduce DRAM energy. We explore two strategies to do so. First, we batch inputs and outputs to amortize weight movement energy. Next, we keep inputs and outputs on-chip in the global buffer between layers rather than fetching them from DRAM [23]. The former strategy increases latency, while the latter requires a larger global buffer and therefore more global buffer energy. Using both of these strategies together, we can reduce aggressively-scaled system energy by 67% (3× improvement).

4) Architecture Exploration: Albireo pays significant energy for data converters. To decrease data conversion energy, we can reduce the number of conversions by converting a value once and reusing the converted value spatially among multiple components [8]. In Fig. 5, we explore variations of the aggressively-scaled Albireo architecture that modify the amount of data reuse. Note that increasing AO reuse will also decrease DE/AE and AE/DE energy because Albireo uses AE as an intermediate between DE and AO.

We modify the AE/AO $Multiply^*$ block in Fig. 1, connecting more AO components to spatially reuse AE weights (lower weight conversion energy) rather than reusing AO inputs and outputs (higher input and output conversion energy). To reduce input conversion energy, we increase the number of components that spatially reuse AO inputs in the AO^* block. To reduce output conversion energy, we increase the number of output-reusing AE components by modifying the AE^* block. We find that increasing reuse can reduce data converter energy by 42% and can reduce accelerator energy by 31%.

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