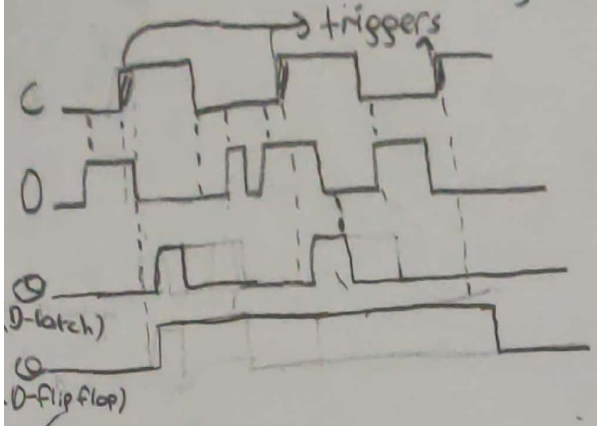
Gökbey Gazi KESKİN
1901042631
CSE232 - Midterm
Group 6 Key

a) compare the behaviour of D-latch and D-flip flop devices by completing the timing diagram given below. Assure each device initially stores 0.



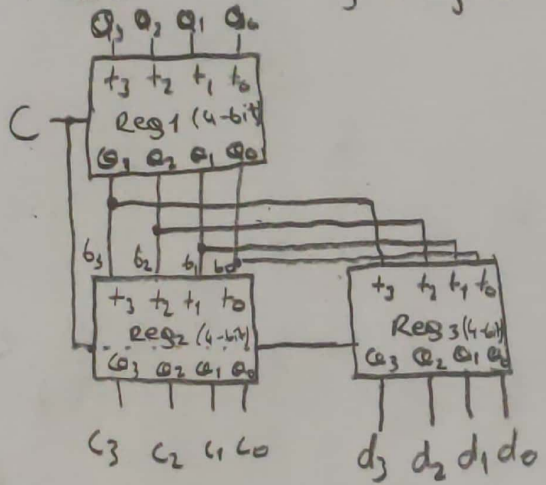
Difference:

D flip-flop is edge-triggered (only effected at triggers.)

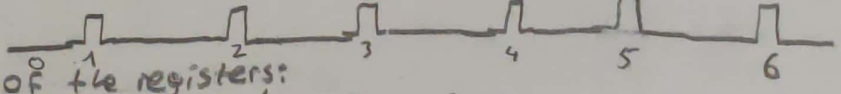
D-latch is affected every time C is 1.

b) Consider 3 four-bit registers connected as shown. Initial values are 9.

Trace the timing diagram by completing it.



$q_3\ q_2\ q_1\ q_0$ 10|15|13|12|6|18|6|5|7|11|8|16|3|13|10|2|4|6|P|2



Stored values of the registers:

Clock:	0	1	2	3	4	5	6
$b_3 b_2 b_1 b_0$	9	15	6	5	8	13	4
$c_3 c_2 c_1 c_0$	9	9	15	6	5	8	13
$d_3 d_2 d_1 d_0$	9	9	15	6	5	8	13