Homework 4

CSE 232

May 2021

Design a 6 bit register for *load*, *swap*, *clear* using the control inputs (ld, sw, cl) to swap the 6 bits data inputs I5 I4 I3 I2 I1 I0 and result the data outputs Q5Q4Q3Q2Q1. The load input will load the data to register, the clear input will load 0 to the register and the swap function *swap* the consecutive bits. For example, after running the swap function, the abcdef will become badefe. The bits at location 5 and 6 are swapped, the bits at 4 and 3 are swapped, the bits at 2 and 1 locations are swapped.

(The priority rank is clear, load, swap)

Make your design following the steps below

1- Define MUX size
2- Create MUX table
3- Connect MUX input
4- Map control lines

States → 2 control input

00 → Maintain the current State

01 → Swap the consecutive bits

10 → Load

11 → Clear

1) Mux Size:

There are four states so I used 4x1 muxes

2) Selection for ld, sw, cl (combinational part) and Mux table (states according to S_1S_0)

S_1S_0 are output of comb. circuit.

cl	ld	sw	S_1	S_0	States
0	0	0	0	0	(maintain)
0	0	1	0	1	(swap)
0	1	0	1	0	(load)
0	1	1	1	0	(load)
0	1	0	1	1	(clear)
1	0	0	1	1	(clear)
1	0	1	1	1	(clear)
1	1	0	1	1	(clear)
1	1	1	1	1	(clear)

k-map for S_1:

cl \ ld-sw	00	01	11	10
0			1	1
1	1	1	1	1

cl

ld

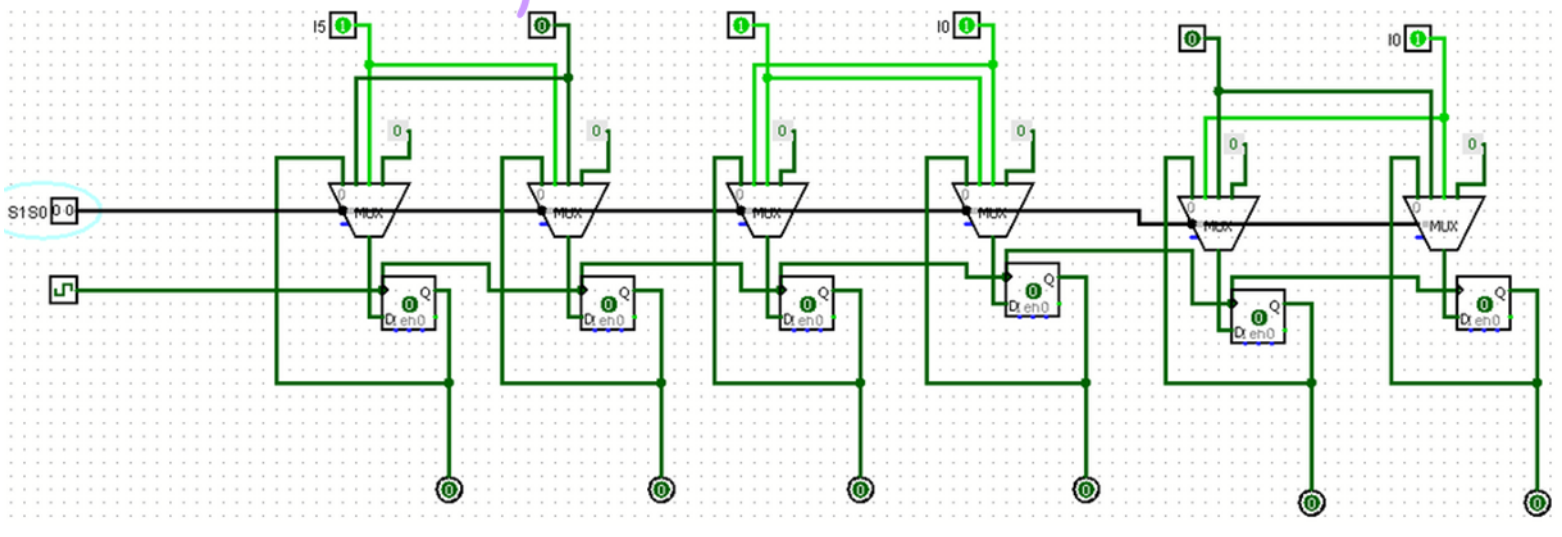
$S_1 = cl + ld$

k-map for S_0:

cl \ ld-sw	00	01	11	10
0		1		
1	1	1	1	1

$S_0 = cl + ld\bar{}sw$

3) Mux Input



4) Map Control Lines (table is on Pg. 2)