Computer Organization Assignment 3

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R-Type Single Cycle MIPS with Structural Verilog

Except the modules below all the other modules are ALU's testbenchs and modules. So they are not included in this report.

PS: The .mem file I included in my project does not include the end result, it includes the register contents before the program simulation/execution.

control_unit.v

Control unit gets the function code of the instruction given by input and uses the combinational circuit given in the schematics to create the ALU Select signal.

mips_registers.v

Inputs: First register to read's address

Second register to read's address

Register to write's address

Data to write to the register to write

RegWrite signal

Clock

This module reads the file at posedge of the clock and gets the values to the read registers values. Then at the negedge of the clock if the RegWrite signal is 1 and the writing register's address is not 0, it writes the given writing data to the register which has the address of the register to write's address.

mips32.v

Inputs: instruction and clock

This module implements the schematic given below for the whole circuit design for R-type single cycle MIPS.

Uses control unit, muxes, register block, concat_shamt, alu block, sltuResult modules.

First it gets the ALU Select from control unit.

Then it chooses if it will get rs address or rt address as the first register to be read.

Once the first register is decided, that register and rt address is entered in to the register block. Their contents are outputted to the ALU but after register block runs depending on if the instruction is a shift or not, second register content and extended shift amount is entered in to a mux to be chosen.

ALU inputs are decided they are entered in to the ALU block. Then the output is entered in to a mux to decide if the output will the sltu result or the alu result. Depending on the value that mux's output is entered into the write data portion of the register block.

concat_shamt.v

This module concatenate 27 0's with the shift amount in the instruction which will be the least significant 5 bits in the newly created extended shift amount.

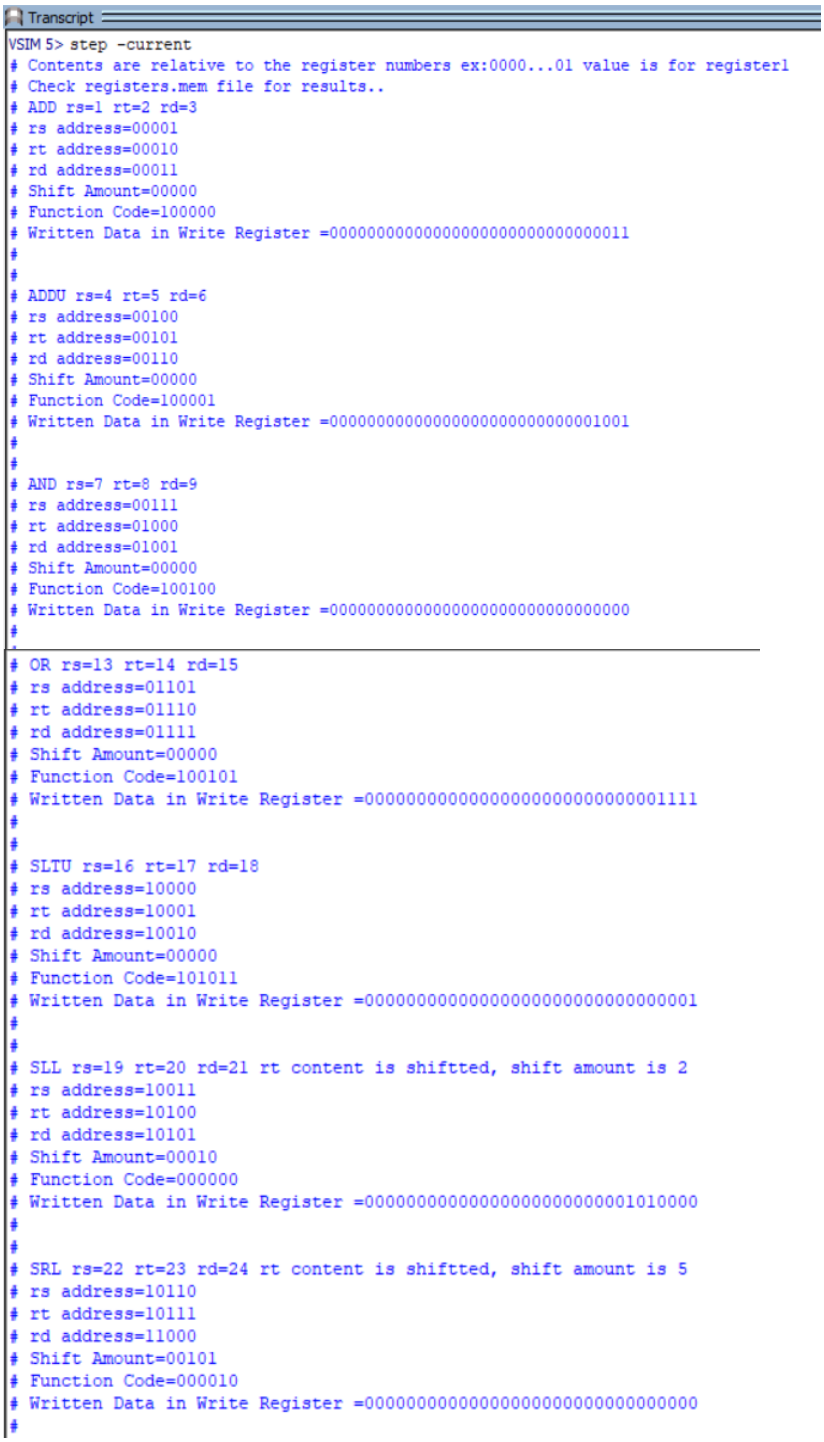
sltuResult.v

This module concatenates the given result's most significant bit with 31 0's which will be the most significant 31 bits in the newly created extended sltu result.

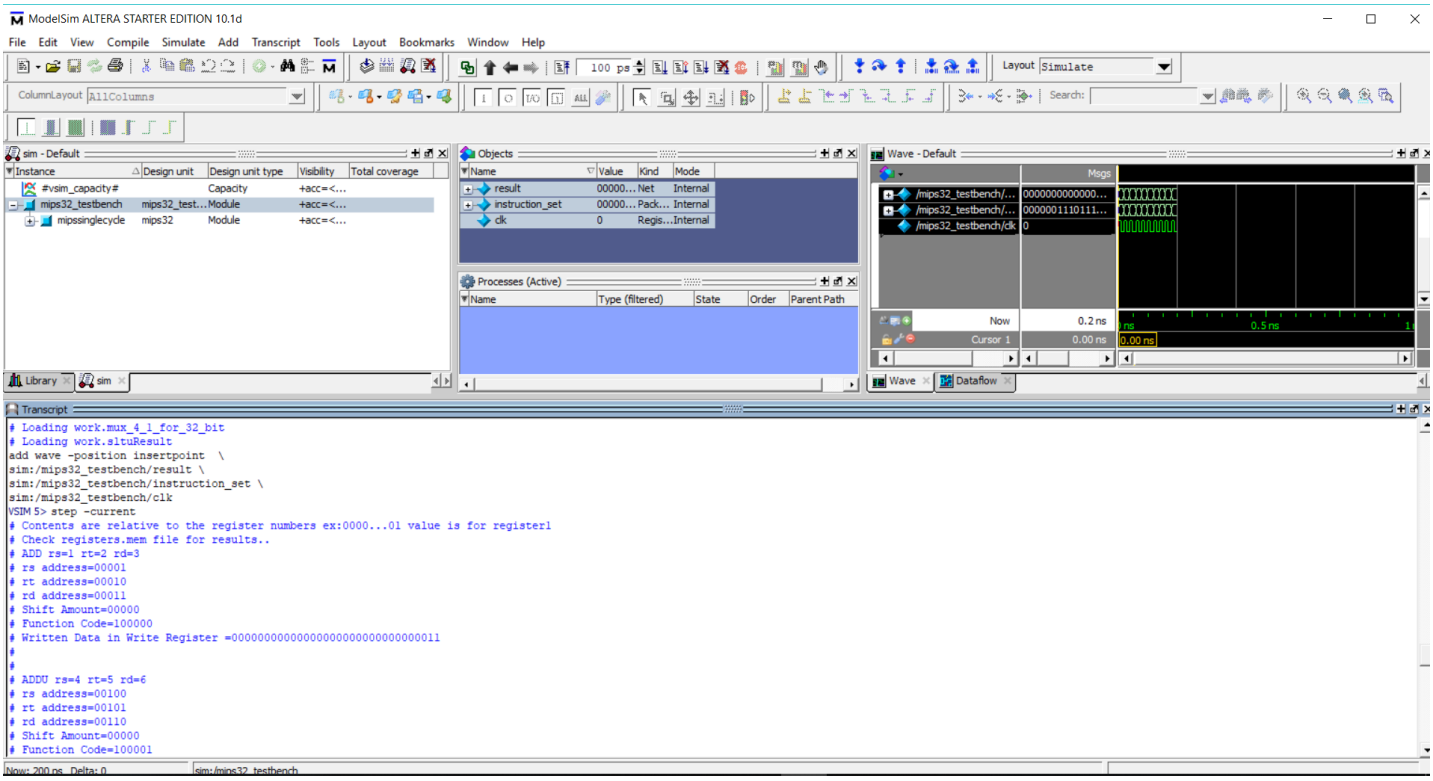
mux_2_1_for_5_bit.v

This module is the representation of a 2:1 mux for 5 bits.

Simulation Results and Output Results



```
# SUB rs=25 rt=26 rd=27
# rs address=11001
# rt address=11010
# rd address=11011
# Shift Amount=00000
# Function Code=100010
# Written Data in Write Register =11111111111111111111111111111111
#
#
# SUBU rs=29 rt=28 rd=30
# rs address=11101
# rt address=11100
# rd address=11110
# Shift Amount=00000
# Function Code=100011
# Written Data in Write Register =00000000000000000000000000000001
#
```



Schematics for the Circuits