CSE 433 EMBEDDED SYSTEMS PROJECT #0

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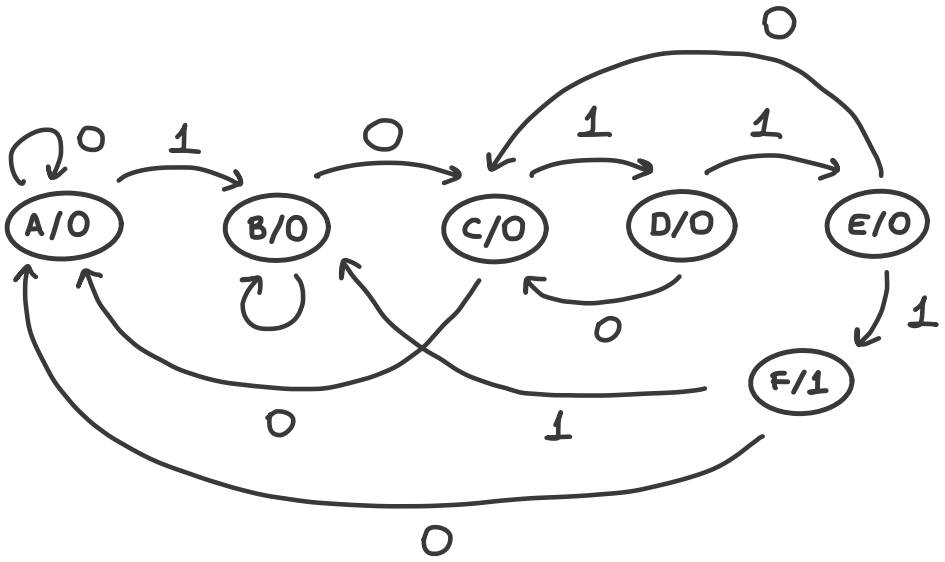
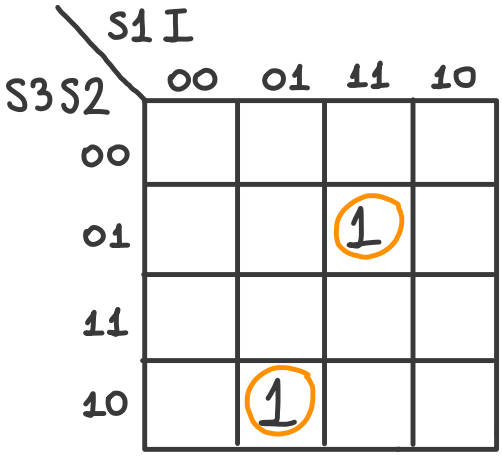
STATE DIAGRAM & STATE TABLES

A → Initial State → out = 0
B → "1" State → out = 0
C → "10" State → out = 0
D → "101" State → out = 0
E → "1011" State → out = 0
F → "10111" State → out = 1

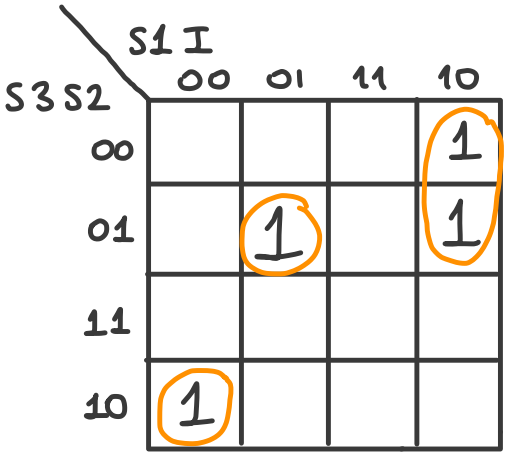


Current State	Input	Next State	Output
A	0 1	A B	0 0
B	0 1	C B	0 0
C	0 1	A D	0 0
D	0 1	C E	0 0
E	0 1	C F	0 0
F	0 1	A B	1 1

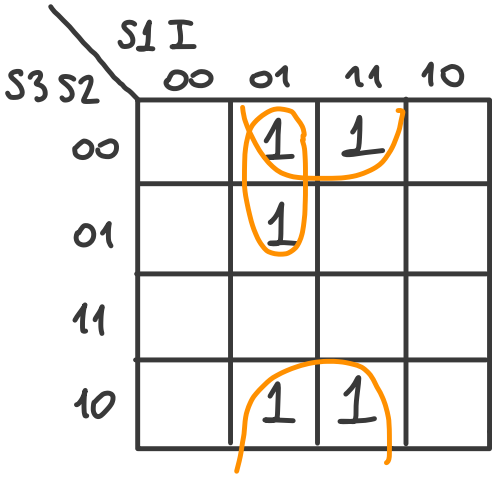
Curr. State S3 S2 S1	Input	Next State D3 D2 D1	Output
000 000	0 1	000 001	0 0
001 001	0 1	010 001	0 0
010 010	0 1	000 011	0 0
011 011	0 1	010 100	0 0
100 100	0 1	010 101	0 0
101 101	0 1	000 001	1 1



$$D3 = \overline{S3}.S2.S1.I + S3.\overline{S2}.\overline{S1}.I$$



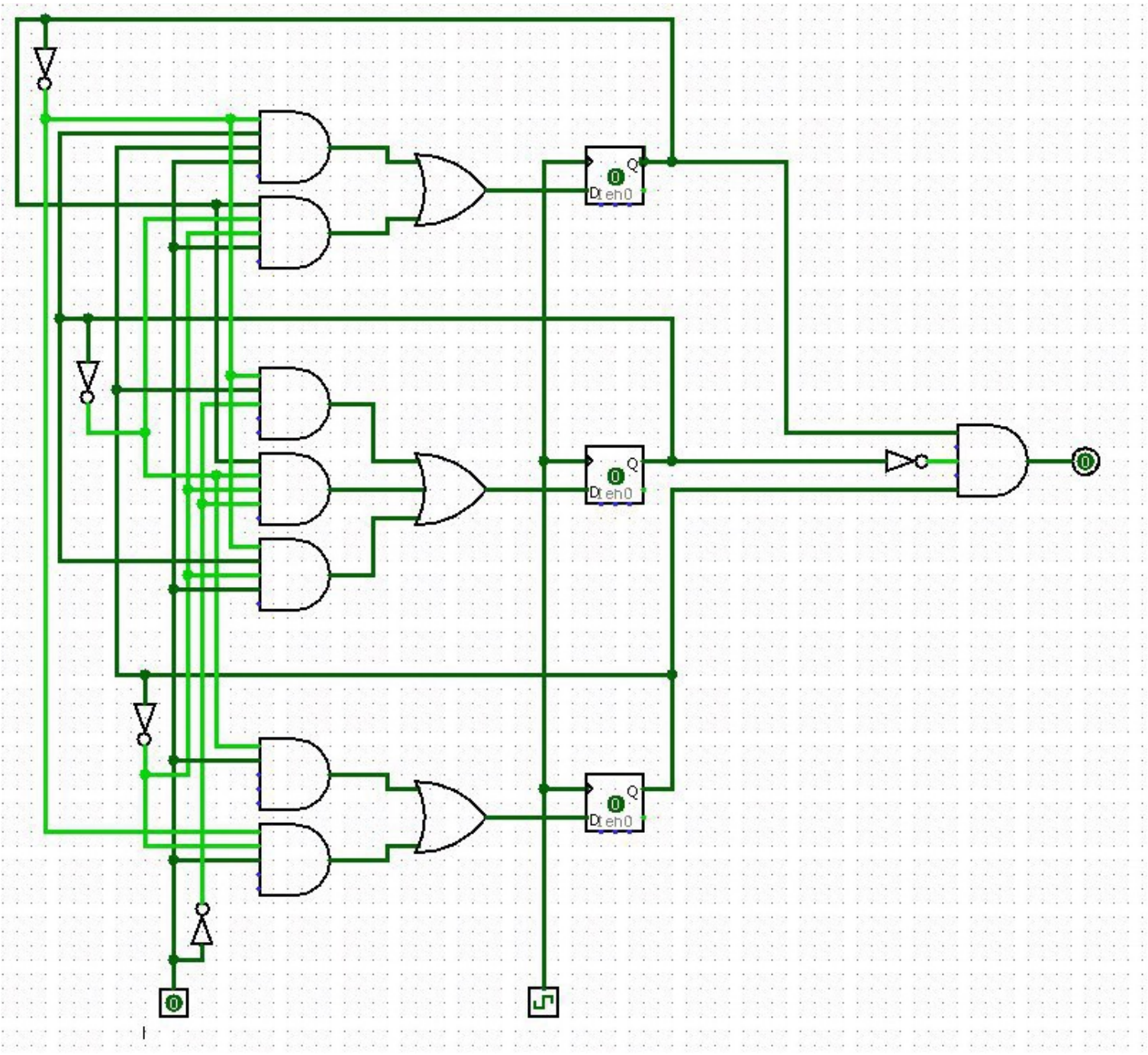
$$D2 = \overline{S3}.S1.\overline{I} + S3.\overline{S2}.\overline{S1}.\overline{I} + \overline{S3}.S2.\overline{S1}.I$$



$$D1 = \overline{S2}.I + \overline{S3}.\overline{S1}.I$$

$$Output = S3.\overline{S2}.S1$$

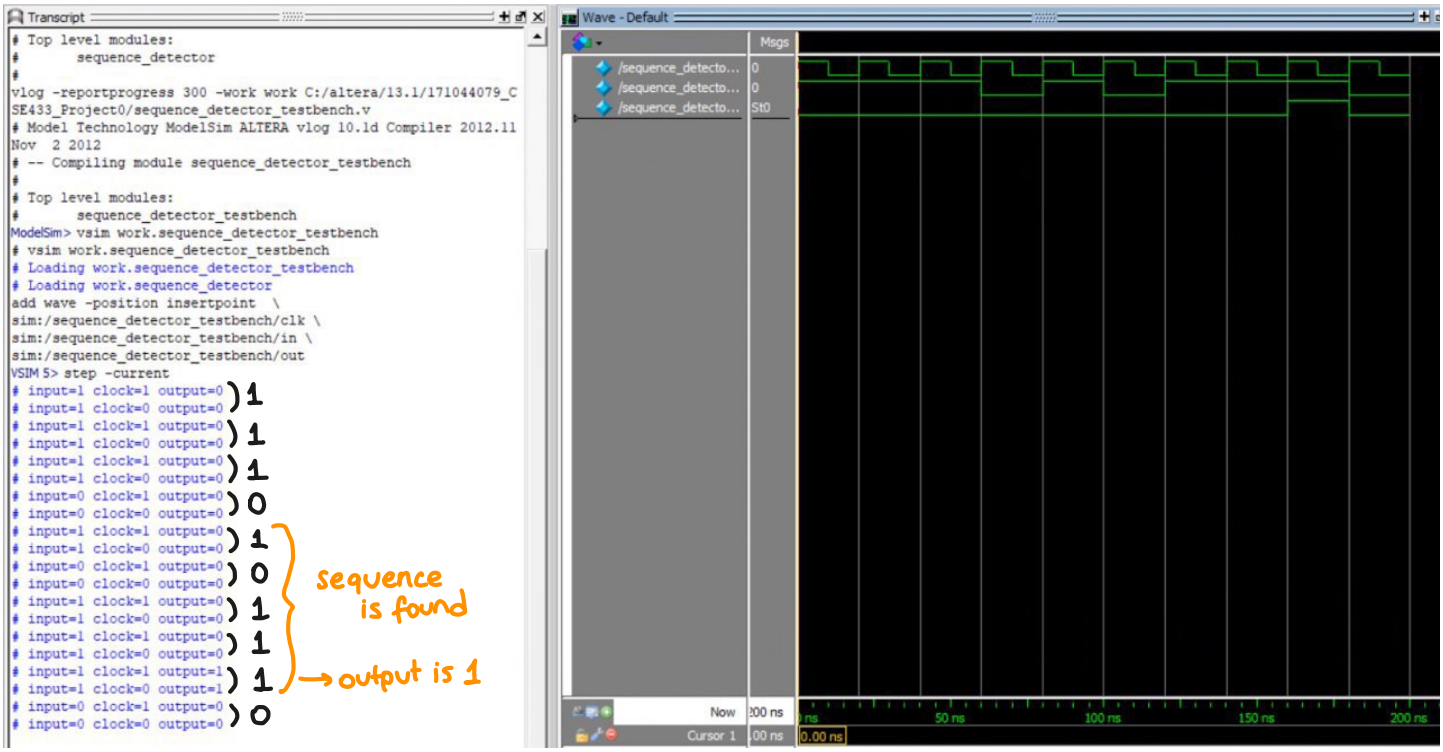
CIRCUIT DESIGN



TEST CASES

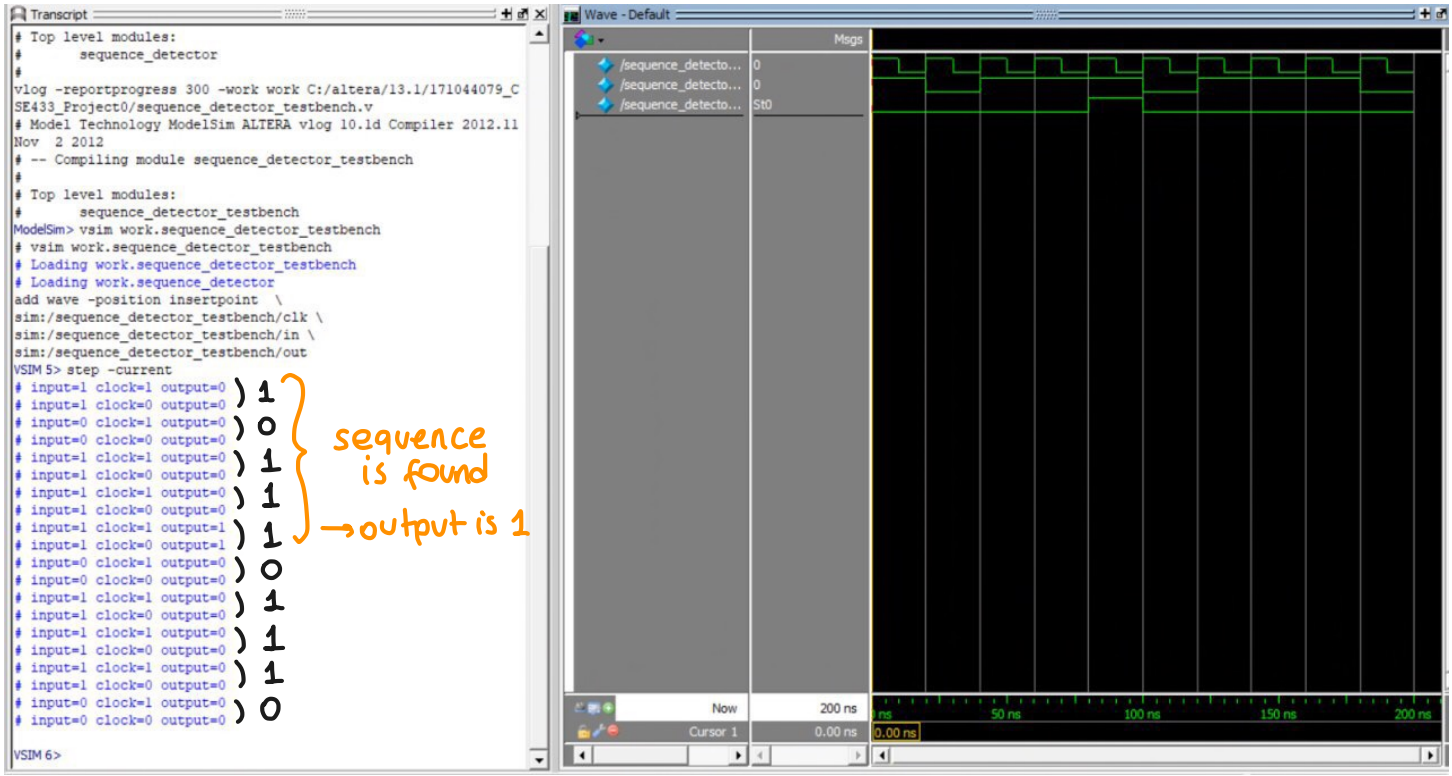
CASE 1: 1110101110

In this case, it is expected to see the output at 1 when 9th digit of this stream is given as the input.



CASE 2: 1011101110

In this case it is expected to see the output as 1 when 5th digit of the bit stream is given as the input.



PS to Case 2 : Project PDF assumed that 101110111 will be detected like there is only one 10111. That is why the simulation doesn't show output as 1 for the second, intermixed 10111. Detector sees it as "0111...."

CASE 3: 00110011110

In this case since the sequence we are looking for is not in the bit stream the output will be observed 0 always.