CSE 331 PROJECT 3 MIPS LOAD – STORE

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NOT : Dosyalardan okuma yapan modüllerde dosya yolu (path) sorun yaratabilmektedir. Eğer hata alınırsa dosya yolunun kontrol edilerek düzeltilmesi gerekmektedir.

NOT : Ana modül (mips_32) hariç, diğer modüllerin testbenchleri düzgün çalışmaktadır. Diğer modüller testbenchlerden ayrı ayrı kontrol edilebilir.

Register Modül :

```
VSIM 4> step -current
# time =  0,
# Read_Reg_1 = 00010,
# Read_Data_1 = 00000000000000000000000000000010
# Read_Reg_2 = 00110,
# Read_data_1 = 00000000000000000000000000000110
# Write_Register = 01010,
# Write_data = 00000000000000000000000000001110
# Signal_RegWrite = 1
#
#
# time = 160,
# Read_Reg_1 = 00011,
# Read_Data_1 = 00000000000000000000000000000011
# Read_Reg_2 = 00111,
# Read_data_1 = 00000000000000000000000000000111
# Write_Register = 01011,
# Write_data = 00000000000000000000000000001110
# Signal_RegWrite = 1
#
#
# time = 320,
# Read_Reg_1 = 00100,
# Read_Data_1 = 00000000000000000000000000000100
# Read_Reg_2 = 01000,
# Read_data_1 = 00000000000000000000000000001111
# Write_Register = 01100,
# Write_data = 00000000000000000000000000001110
# Signal_RegWrite = 1
#
#
# ** Note: $finish    : C:/altera/13.1/project3workspace/register_testbench.v(17)
#    Time: 321 ps  Iteration: 0  Instance: /register_testbench
# 1
# Break in Module register_testbench at C:/altera/13.1/project3workspace/register_testbench.v line 17
```

Control Unit Modül: Sinyaller kodda yorum satırlarında açıklanmıştır.

```
VSIM 4> step -current
# Opcode = 100000, MemRead = 1, LastSignal0 = 1, LastSignal1 = 1, RegWrite = 1, MemWrite = 0, SB = 0, SH = 0, ZeroOrSign =0
# Opcode = 100100, MemRead = 1, LastSignal0 = 1, LastSignal1 = 1, RegWrite = 1, MemWrite = 0, SB = 0, SH = 0, ZeroOrSign =1
# Opcode = 100001, MemRead = 1, LastSignal0 = 1, LastSignal1 = 0, RegWrite = 1, MemWrite = 0, SB = 0, SH = 0, ZeroOrSign =0
# Opcode = 100101, MemRead = 1, LastSignal0 = 0, LastSignal1 = 0, RegWrite = 1, MemWrite = 0, SB = 0, SH = 0, ZeroOrSign =1
# Opcode = 001111, MemRead = 0, LastSignal0 = 0, LastSignal1 = 0, RegWrite = 0, MemWrite = 0, SB = 0, SH = 0, ZeroOrSign =1
# Opcode = 100011, MemRead = 0, LastSignal0 = 0, LastSignal1 = 1, RegWrite = 0, MemWrite = 0, SB = 0, SH = 0, ZeroOrSign =1
# Opcode = 101000, MemRead = 0, LastSignal0 = 0, LastSignal1 = 0, RegWrite = 0, MemWrite = 1, SB = 1, SH = 0, ZeroOrSign =1
# Opcode = 101001, MemRead = 0, LastSignal0 = 0, LastSignal1 = 0, RegWrite = 0, MemWrite = 1, SB = 0, SH = 1, ZeroOrSign =1
# Opcode = 101011, MemRead = 0, LastSignal0 = 0, LastSignal1 = 0, RegWrite = 0, MemWrite = 1, SB = 0, SH = 0, ZeroOrSign =1
```

SignExtender Modül:

```
# time = 0,     Immediate = 1111111111111111,          Result = 11111111111111111111111111111111
# time =20,     Immediate = 1111111100000001,          Result = 11111111111111111111111100000001
# time =40,     Immediate = 0000000000001111,          Result = 00000000000000000000000000001111
# time =60,     Immediate = 0000000000000000,          Result = 00000000000000000000000000000000
```

ZeroExtender Modül:

```
# time = 0,     Immediate = 1111111111111111,          Result = 00000000000000001111111111111111
# time =20,     Immediate = 1111111100000001,          Result = 00000000000000001111111100000001
# time =40,     Immediate = 0000000000001111,          Result = 00000000000000000000000000001111
# time =60,     Immediate = 0000000000000000,          Result = 00000000000000000000000000000000
```

Inst_Modül:

```
#  time =  0, Insruction: 10000000011000100000000000001010
#  time = 20, Insruction: 10000000010000111111010100110000
#  time = 40, Insruction: 10010000101001100011000100110001
#  time = 60, Insruction: 10010000110001011111000110110001
```

Immediate Modül:

```
# time = 0,     Immediate = 1111111111111111,          Result = 11111111111111110000000000000000
# time =20,     Immediate = 1111111100000001,          Result = 11111111000000010000000000000000
# time =40,     Immediate = 0000000000001111,          Result = 00000000000011110000000000000000
# time =60,     Immediate = 0000000000000000,          Result = 00000000000000000000000000000000
```

Mips_32 Modül:

Modülün kendisinde yorum satırlarıyla hangi işlemin ne amaçlar için yapıldığı açıklanmıştır.

Datapath'in temize geçirilmemiş hali zipdeki ssler klasöründe bulunmaktadır.

```
# time:  0 PC: 00000000000000000000000000000000,
# instruction: 10000000011000100000000000001010,
# Opcode= 100000 ,
# rs = 00011 ,
# rt = 00010 ,
# immediate = 0000000000001010
# Mem_read = 1 ,
# Last_signal0 = 1,
# Last_signal1 = 1,
# Reg_Write = 1,
# Mem_Write = 0,
# Store_Byte = 0,
# Store_Halfword = 0,
# ZeroOrSign = 0,
# WriteData = 00000000000000000000000xxxxxxxx,
# Read_Data_1 = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx,
# Read_Data_2 = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
#
#
# time: 50 PC: 00000000000000000000000000000001,
# instruction: 10000000010000111110101000110000,
# Opcode= 100000 ,
# rs = 00010 ,
# rt = 00011 ,
# immediate = 1110101000110000
# Mem_read = 1 ,
# Last_signal0 = 1,
# Last_signal1 = 1,
# Reg_Write = 1,
# Mem_Write = 0,
# Store_Byte = 0,
# Store_Halfword = 0,
# ZeroOrSign = 0,
# WriteData = 00000000000000000000000xxxxxxxx,
# Read_Data_1 = 00000000000000000000000000000011,
# Read_Data_2 = 00000000000000000000000000000010
*

# time: 150 PC: 00000000000000000000000000000010,
# instruction: 10010000101001100011000100110001,
# Opcode= 100100 ,
# rs = 00101 ,
# rt = 00110 ,
# immediate = 0011000100110001
# Mem_read = 1 ,
# Last_signal0 = 1,
# Last_signal1 = 1,
# Reg_Write = 1,
# Mem_Write = 0,
# Store_Byte = 0,
# Store_Halfword = 0,
# ZeroOrSign = 1,
# WriteData = 00000000000000000000000xxxxxxxx,
# Read_Data_1 = 00000000000000000000000xxxxxxxx,
# Read_Data_2 = 00000000000000000000000000000011
#
#
# time: 250 PC: 00000000000000000000000000000011,
# instruction: 10010000110001011111000110110001,
# Opcode= 100100 ,
# rs = 00110 ,
# rt = 00101 ,
# immediate = 1111000110110001
# Mem_read = 1 ,
# Last_signal0 = 1,
# Last_signal1 = 1,
# Reg_Write = 1,
# Mem_Write = 0,
# Store_Byte = 0,
# Store_Halfword = 0,
# ZeroOrSign = 1,
# WriteData = 00000000000000000000000xxxxxxxx,
# Read_Data_1 = 00000000000000000000000000000101,
# Read_Data_2 = 00000000000000000000000000000110
#
```

```
time: 350 PC: 00000000000000000000000000000100,
instruction: 10000110010101000000111000011010,
Opcode= 100001 ,
rs = 10010 ,
rt = 10100 ,
immediate = 0000111000011010
Mem_read = 1 ,
Last_signal0 = 1,
Last_signal1 = 0,
Reg_Write = 1,
Mem_Write = 0,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 0,
WriteData = 00000000000000000000000xxxxxxxx,
Read_Data_1 = 00000000000000000000000xxxxxxxx,
Read_Data_2 = 00000000000000000000000000000101


time: 450 PC: 00000000000000000000000000000101,
instruction: 10000110100100101111000000110101,
Opcode= 100001 ,
rs = 10100 ,
rt = 10010 ,
immediate = 1111000000110101
Mem_read = 1 ,
Last_signal0 = 1,
Last_signal1 = 0,
Reg_Write = 1,
Mem_Write = 0,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 0,
WriteData = 00000000000000000000000xxxxxxxx,
Read_Data_1 = 00000000000000000000000000010010,
Read_Data_2 = 00000000000000000000000000010100
```

```
time: 550 PC: 00000000000000000000000000000110,
instruction: 10010110110010010000101010101000,
Opcode= 100101 ,
rs = 10110 ,
rt = 01001 ,
immediate = 0000101010101000
Mem_read = 1 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 1,
Mem_Write = 0,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 00001010101010000000000000000000,
Read_Data_1 = 00000000000000000000000xxxxxxxx,
Read_Data_2 = 00000000000000000000000000010010


time: 650 PC: 00000000000000000000000000000111,
instruction: 10010101001101101111000001010100,
Opcode= 100101 ,
rs = 01001 ,
rt = 10110 ,
immediate = 1111000001010100
Mem_read = 1 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 1,
Mem_Write = 0,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 11111000001010100000000000000000,
Read_Data_1 = 00000000000000000000000000010110,
Read_Data_2 = 00000000000000000000000011110000


time: 750 PC: 00000000000000000000000000001000,
instruction: 00111100110010000101000010001001,
Opcode= 001111 ,
rs = 00110 ,
rt = 01000 ,
immediate = 0101000010001001
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 0,
Mem_Write = 0,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 01010000100010010000000000000000,
Read_Data_1 = 00001010101010000000000000000000,
Read_Data_2 = 00000000000000000000000000010110
```

```
time: 850 PC: 00000000000000000000000000001001,
instruction: 00111101000001100101010101001000,
Opcode= 001111 ,
rs = 01000 ,
rt = 00110 ,
immediate = 0101010101001000
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 0,
Mem_Write = 0,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 01010101010010000000000000000000,
Read_Data_1 = 00000000000000000000000xxxxxxxx,
Read_Data_2 = 00000000000000000000000000001111


time: 950 PC: 00000000000000000000000000001010,
instruction: 10001110001100110000000010000000,
Opcode= 100011 ,
rs = 10001 ,
rt = 10011 ,
immediate = 0000000010000000
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 1,
Reg_Write = 0,
Mem_Write = 0,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 00000000100000000000000000000000,
Read_Data_1 = 00000000000000000000000000001111,
Read_Data_2 = 00000000000000000000000xxxxxxxx


time: 1050 PC: 00000000000000000000000000001011,
instruction: 10001110011100011110000000000010,
Opcode= 100011 ,
rs = 10011 ,
rt = 10001 ,
immediate = 1110000000000010
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 1,
Reg_Write = 0,
Mem_Write = 0,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 11100000000000100000000000000000,
Read_Data_1 = 00000000000000000000000000010001,
Read_Data_2 = 00000000000000000000000000010011
```

```
time: 1150 PC: 00000000000000000000000000001100,
instruction: 10100000111001100001000010000100,
Opcode= 101000 ,
rs = 00111 ,
rt = 00110 ,
immediate = 0001000010000100
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 0,
Mem_Write = 1,
Store_Byte = 1,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 00010000100001000000000000000000,
Read_Data_1 = 00000000000000000000000000010011,
Read_Data_2 = 00000000000000000000000000010001


time: 1250 PC: 00000000000000000000000000001101,
instruction: 10100000110001111111000000010011,
Opcode= 101000 ,
rs = 00110 ,
rt = 00111 ,
immediate = 1111000000010011
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 0,
Mem_Write = 1,
Store_Byte = 1,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 11110000000100110000000000000000,
Read_Data_1 = 00000000000000000000000000000111,
Read_Data_2 = 00000000000000000000000xxxxxxxx


time: 1350 PC: 00000000000000000000000000001110,
instruction: 10100110001001100000010000001111,
Opcode= 101001 ,
rs = 10001 ,
rt = 00110 ,
immediate = 0000010000001111
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 0,
Mem_Write = 1,
Store_Byte = 0,
Store_Halfword = 1,
ZeroOrSign = 1,
WriteData = 00000100000011110000000000000000,
Read_Data_1 = 00000000000000000000000xxxxxxxx,
Read_Data_2 = 00000000000000000000000000000111
```

```
time: 1450 PC: 00000000000000000000000000001111,
instruction: 10100100110100010001011111000000,
Opcode= 101001 ,
rs = 00110 ,
rt = 10001 ,
immediate = 0001011111000000
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 0,
Mem_Write = 1,
Store_Byte = 0,
Store_Halfword = 1,
ZeroOrSign = 1,
WriteData = 00010111110000000000000000000000,
Read_Data_1 = 00000000000000000000000000010001,
Read_Data_2 = 00000000000000000000000xxxxxxxx


time: 1550 PC: 00000000000000000000000000010000,
instruction: 10101110001001110000011111100011,
Opcode= 101011 ,
rs = 10001 ,
rt = 00111 ,
immediate = 0000011111100011
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 0,
Mem_Write = 1,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 00000111111000110000000000000000,
Read_Data_1 = 00000000000000000000000xxxxxxxx,
Read_Data_2 = 00000000000000000000000000010001


time: 1650 PC: 00000000000000000000000000010001,
instruction: 10101100111100010000101111000001,
Opcode= 101011 ,
rs = 00111 ,
rt = 10001 ,
immediate = 0000101111000001
Mem_read = 0 ,
Last_signal0 = 0,
Last_signal1 = 0,
Reg_Write = 0,
Mem_Write = 1,
Store_Byte = 0,
Store_Halfword = 0,
ZeroOrSign = 1,
WriteData = 00001011110000010000000000000000,
Read_Data_1 = 00000000000000000000000000010001,
Read_Data_2 = 00000000000000000000000000000111
```