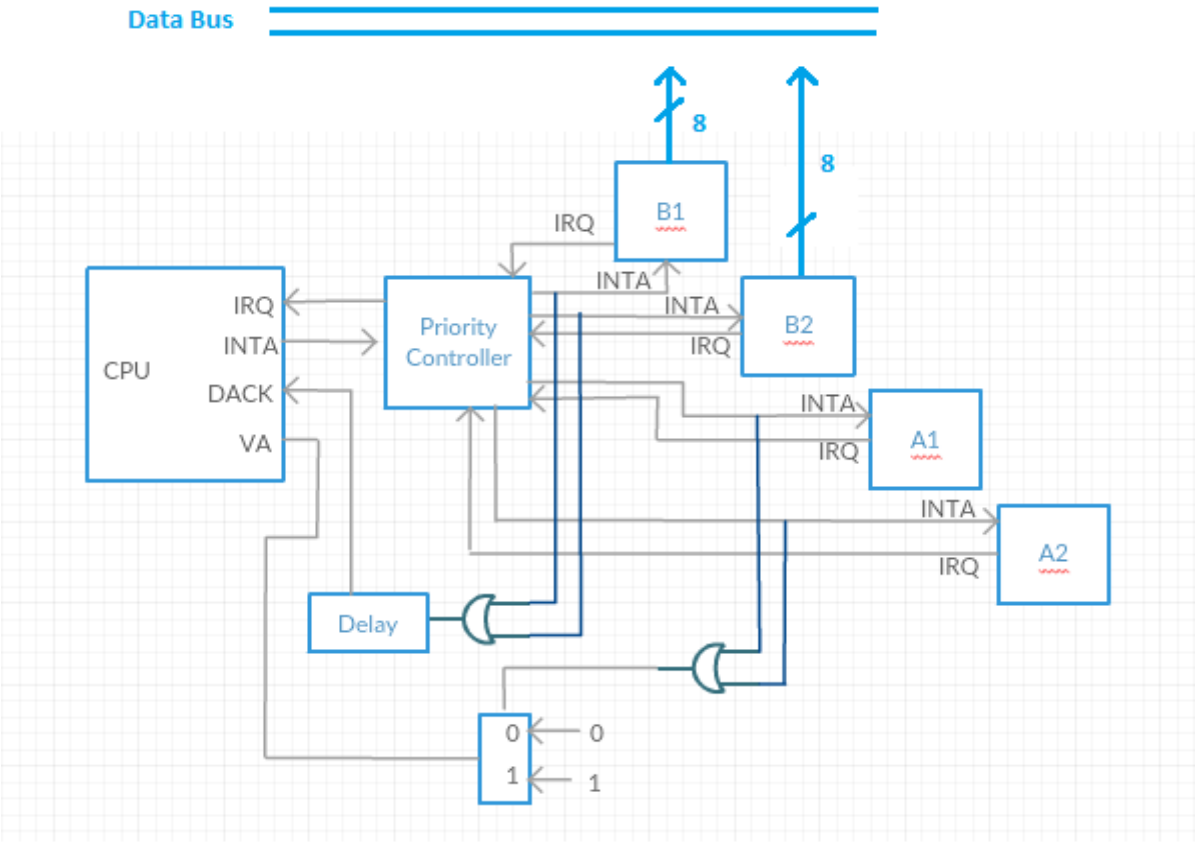
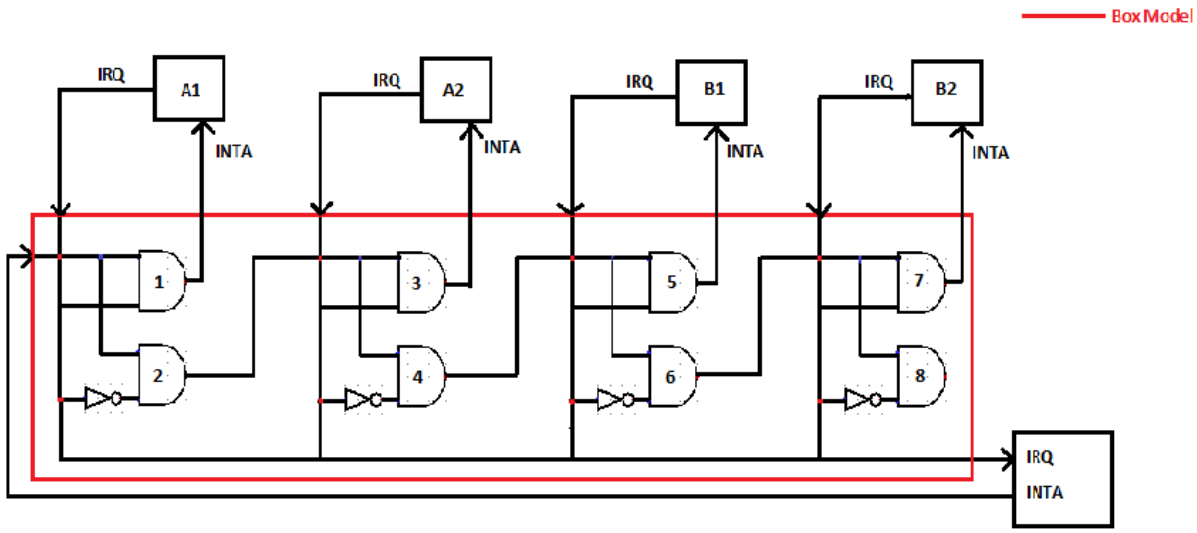
a)



Internal Structure:



b)

IRQ(A1) = 1 , IRQ(B1) = 1; (Request interrupt)

INTA(CPU) = 1; (Request Accepted)

After AND gate (1) INTA(1) = 1 ; (Source of interrupt is A1)

INTA(A1) = 1 (A1 gets acknowledgement)

VA = 0 (CPU accepts autovectored interrupt and determines the starting address of ISR from predetermined and fixed rows of vector table, runs ISR)

IRQ(A1) = 0 (Request of A1 granted, it becomes 0)

CPU returns from ISR of A1

IRQ(A1) = 0, IRQ(B1) = 1;

AND(1) = 0, INTA(1) = 0, AND(2) = 1, AND(3) = 0, INTA(2) = 0, AND(4) = 1,

AND(5) = 1, INTA(3) = 1; (Source of interrupt is B1)

INTA(B1) = 1; (B1 gets acknowledgement), Puts its VN to the data bus;

VA(0), DTACT(1) ; (CPU reads vector number and performs ISR by taking starting address from vector table)

IRQ(B1) = 0; (Request of B1 granted, it becomes 0)

CPU returns from ISR of B1, ISR returns to the main program.

c)

type A: A type devices does not have VN numbers, w when they get acknowledgement CPU accepts autovectored interrupt and determines the starting address of ISR from predetermined and fixed rows of vector table.

type B: B type devices puts its VN on the data bus, when they get acknowledgement. Then, CPU reads VN from data bus and uses it to get starting address of the ISR from vector table.