Middle East Technical University - Department of Computer Engineering

CENG 232

Logic Design

Spring 2020-2021

Lab 2 Quiz Logisim Part

Due date: Sunday, May 23, 2021, 19:00

1 Quiz Rules

Your Logisim part consists of 3 questions. Labelling conventions are provided in each question section.

- Please implement each question in different circ file.
- "Multiplexer" question's circ file should be named as e{Student number}Mux.circ
  Example : e1234567Mux.circ
- "Encoder" question's circ file should be named as e{Student number}Encoder.circ
  Example : e1234567Encoder.circ
- "Demultiplexer" question's circ file should be named as e{Student number}Demux.circ
  Example : e1234567Demux.circ

2 Multiplexer

Create an 11-to-1 multiplexer using only 4-to-1 and 2-to-1 multiplexers. You should use at least one 4-to-1 multiplexer. As you know, Logisim do not have any 2-to-1 multiplexer. However, "4-to-1 MUX (x2) (74153)" can be used as 2-to-1 Multiplexer as shown in Figure 1.

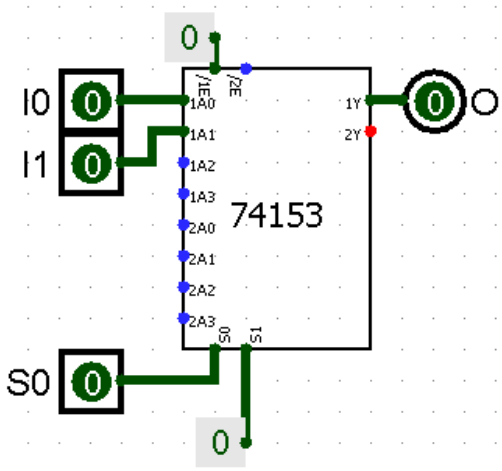

Figure 1: 2-to-1 Multiplexer

2.1 Labelling Specifications

- Your input pins should be labeled as I0, I1, I2, I3, I4, I5, I6, I7, I8, I9, I10, S0, S1, S2, S3.
- Your output pins should be labeled as O.
- Label properties are case-sensitive. **Please be very careful on the correct naming of labels.**
- You will receive grade **penalty** unless labelling is done properly.

3 Encoder

Normally, Encoder circuitry outputs the binary representation of the activated input hence yields reverse function of Decoder circuitry. But for this question, you are expected to implement a different type of 8x3 encoder. This encoder consists of 8 inputs (I7, I6, I5, I4, I3, I2, I1, I0) and 3 outputs (O2, O1, O0). At a given time only one of the inputs will be activated (1).

Input								Output		
I7	I6	I5	I4	I3	I2	I1	I0	O2	O1	O0
0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	1	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0

3.1 Labelling Specifications

- Your input pins should be labeled as I7, I6, I5, I4, I3, I2, I1, I0.
- Your output pins should be labeled as O2, O1, O0.
- Label properties are case-sensitive. **Please be very careful on the correct naming of labels.**
- You will receive grade **penalty** unless labeling is done properly.

4 Demultiplexer

Demultiplexer circuitry takes an input and transfers it to the selected output. It can be likened to a railway controller which connects a specific railway to different directions. You are expected to implement a 2x4 (two inputs, four outputs) demultiplexer consisting of 2 inputs (I1, I0), 2 selector bits (S1, S0), and 4 outputs (O3, O2, O1, O0). (Hint: you can make use of decoder and controlled buffers)

Input		Selector		Output			
I1	I0	S1	S0	O3	O2	O1	O0
B	A	0	0	B	0	0	A
B	A	0	1	0	B	A	0
B	A	1	0	0	A	B	0
B	A	1	1	A	0	0	B

Where A $\in \{0, 1\}$, B $\in \{0, 1\}$.

4.1 Labelling Specifications

- Your input pins should be labelled as I1, I0, S1, S0.
- Your output pins should be labeled as O3, O2, O1, O0
- Label properties are case-sensitive. **Please be very careful on the correct naming of labels.**
- You will receive grade **penalty** unless labeling is done properly.

5 Cheating Policy

All the work should be individual and there is a zero-tolerance policy for cheating. See the course website for further information about the cheating policy.

6 References

CENG Logisim Version.