Gokulan Ravi

ravig@purdue.edu | https://gokulan97.github.io

EDUCATION

Ph.D. in Electrical & Computer Engineering Jan 2021 - Present
Purdue University, West Lafayette, USA GPA: 3.87/4.00

B.Tech + M.Tech (Dual Degree) in Computer Science & Engineering Jul 2015 - May 2020
Indian Institute of Technology Madras, Chennai, India GPA: 8.23/10.00

RESEARCH PROJECTS

Scalable verification of hardware memory consistency, *PhD thesis* May 2021 - present
- Verifying memory consistency for all programs in an out-of-order-issue processor of any scale
- (work-in-progress) Formal verification of RISC-V Weak Memory Ordering in BOOMv3

Hardware accelerator for Graph Neural Networks, *Purdue University* Jan 2021 - May 2021
- Aimed at exploiting ultra sparsity of graphs to accelerate GNNs
- Reported that GPUs SpMM is a good fit and no further opportunity remained to be explored

Systolic-array based co-processor for Deep Neural Network inference Jun 2019 - May 2020
Masters thesis, IIT Madras
- Led the implementation of a parameterized systolic-array based co-processor in Bluespec
- Built an end-to-end working solution with a prototype compiler based on TVM

MOESI Cache Coherence for in-order processor, *IIT Madras* May - Jun 2018, Jan - May 2019
Summer Research Project (Snoop-based protocol), Senior Design project (Directory-based protocol)
- Modified memory subsystem of a 5-stage RISC-V core to enable multicore extensions
- Designed the finite state machine and implemented the entire cache controller in Bluespec
- Implemented and customized Tilelink-Cacheable (TL-C) bus protocol to support P2P transactions

PUBLICATIONS

QED: Scalable Verification of Hardware Memory Consistency, arXiv:2404.03113 Apr 2024
Gokulan Ravi, Xiaokang Qiu, Mithuna Thottethodi, T. N. Vijaykumar

PROFESSIONAL EXPERIENCE

Engineering Intern, *Ventana Microsystems Inc., Remote* Jul 2023 - Jan 2024
- Was involved in the design, verification and performance analysis of the Branch Predictor Unit for Ventana's V2 processor
- Implemented multiple features to optimize for performance and power
- Wrote verification tests that identified bugs of different complexity, contributing to better performance
- Crafted performance tests for stress-testing and reasoning about changes in performance

Graduate Teaching Assistant Aug 2019 - May 2023
- Purdue University - Operating Systems (S21, S22, S23), Object Oriented Prog (F21), Compilers (F22)
- IIT Madras - Computer System Design (F19), Systems for Deep Learning (S20)

SKILLS

Relevant Courses: Computer Architecture, Parallel Computer Architecture, GPU Programming, Concurrent Programming, Operating Systems, Compilers

Misc.: SystemVerilog, Bluespec SystemVerilog, Chisel, Jaspergold

OTHER ACTIVITIES

Member of Artifact Evaluation Committee, MICRO 54 Aug 2021
Reproduced and verified results of one paper in MICRO 54's proceedings

Head, Web Operations, Shaastra 2018, IIT Madras Mar 2017 - Jan 2018
- Led a team of 20 to build the software stack of the technical symposium
- Unified different user-facing applications, streamlined internal operations, increased registrations by 80%

Instructor, Webops Club, Center for Innovation, IIT Madras May 2017 - Dec 2019
Organized various workshops in web, mobile app and Python development for undergraduates