```
entity process_data is
    Port ( clk : in  STD_LOGIC;
           reset : in  STD_LOGIC;
           data_in : in  STD_LOGIC_VECTOR (7 downto 0); -- Data from the UART
           RX_full : in  STD_LOGIC; -- Indicate a is availbe from the UART
           TX_busy_n : in  STD_LOGIC; -- Indicate UART busy transmitting
           RD_n : out  STD_LOGIC; -- Read the byte from the UART
           WR_n : out  STD_LOGIC; -- Write a byte to the UART
           data_out : out  STD_LOGIC_VECTOR (7 downto 0); -- Data for UART to transmit
           soft_reset : out std_logic;
-------------------------------------------------------------------------------
-- User Modified
-------------------------------------------------------------------------------
           Reg0In  : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
           Reg1In  : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
-------------------------------------------------------------------------------
           LD0 : out std_logic;
           LD1 : out std_logic;
           LD2 : out std_logic
           );
end process_data;
```