```
entity MP1_top is
port
(
  sysclk    : in  std_logic;  -- system clock
  RESET_low : in  std_logic;  -- Active low (but polarity is immediate made active high)
  FPGA_SERIAL1_TX  : out std_logic;
  FPGA_SERIAL1_RX  : in  std_logic;
-------------------------------------------------------------------------------
-- User Modified: The input signals to the FPGA are assigned here, i.e., the
--                pins for I/O match to these signals
-------------------------------------------------------------------------------
    Quad0_ChA  : IN STD_LOGIC;
    Quad0_ChB  : IN STD_LOGIC;
    Quad1_ChA  : IN STD_LOGIC;
    Quad1_ChB  : IN STD_LOGIC;
-------------------------------------------------------------------------------
  LD0 : out std_logic;
  LD1 : out std_logic;
  LD2 : out std_logic
);
end MP1_top;
```