```
COMPONENT sensor_log is
    Port (
        clk         : in  STD_LOGIC;
        reset       : in STD_LOGIC;
-----------------------------------------------------------------------------
-- User Modified
-----------------------------------------------------------------------------
        Reg0In   : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
        Reg1In   : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
-----------------------------------------------------------------------------
        log_data : out std_logic_vector(LOG_DATA_WIDTH-1 downto 0)
            );
end COMPONENT;
-----------------------------------------------------------------------------
```