```
-- Port map process_data for processing recived data
process_data_1  : process_data
port map
(
  clk       => sysclk,
  reset     => reset,
  data_in   => D_OUT,  -- Data recived by the FPGA
  RX_full   => RX_full, -- Indicate a byte has been recived by the UART
  TX_busy_n => TX_busy_n, -- Indicate UART is busy transmitting
  RD_n      => RD_n,   -- Request to read a byte from the UART
  WR_n      => WR_n,  -- Write a byte to the UART inteface for transmission
  data_out  => D_IN,  -- Data to be transmitted by the FPGA
  soft_reset => soft_reset,
-----------------------------------------------------------------------------
-- User Modified
-----------------------------------------------------------------------------
  Reg0In  => Reg0In,
  Reg1In  => Reg0In,
-----------------------------------------------------------------------------
  LD0 => LD0,
  LD1 => LD1,
  LD2 => LD2
);
```