```vhdl
entity echo is
    generic(
        rtc_divid : integer range 2 to 200000000 := 25000000
        );
    Port (
        clk      : in  STD_LOGIC;
        reset    : in STD_LOGIC;
        new_data : in  STD_LOGIC; -- Indicate a new byte has been captured from UART
        data_in  : in  STD_LOGIC_VECTOR (7 downto 0);
        TX_busy_n : in  STD_LOGIC;
        send_data : out  STD_LOGIC; -- Request UART to tranmite data_out
        data_out : out  STD_LOGIC_VECTOR (7 downto 0);
        soft_reset : out std_logic;
-------------------------------------------------------------------------------
-- User Modified
-------------------------------------------------------------------------------
        Reg0In : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
        Reg1In : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
-------------------------------------------------------------------------------
        LD0 : out std_logic;
        LD1 : out std_logic;
        LD2 : out std_logic
        );
end echo;
```