```
-- Component that echos data recived from the PC
-- back to the PC.
component echo
generic (
   rtc divid : integer range 1 to 200000000 := 200000000
   );
port
 clk : in STD LOGIC:
 reset : in STD LOGIC;
 new data : in STD LOGIC; -- Indicate UART has recieved a new byte
 data in : in STD LOGIC VECTOR (7 downto 0); -- Data from the UART
 TX busy n : in STD LOGIC; -- Active low, indicates when UART is ready to transmit
 send data : out STD LOGIC; -- Tell UART to transmit a byte
 data out : out STD LOGIC VECTOR (7 downto 0); -- Data to send to the UART
 soft reset : out std logic;
-- User Modified
 RegOIn : IN STD LOGIC VECTOR(31 DOWNTO 0);
 ReglIn : IN STD LOGIC VECTOR (31 DOWNTO 0);
 LD0 : out std logic;
 LD1 : out std logic;
 LD2 : out std logic
end component;
```