```
-- Component that passes data to/from a
-- subcomponent that does the actaully data processing
component process_data
port
(
  clk        : in  STD_LOGIC;
  reset      : in  STD_LOGIC;
  data_in    : in  STD_LOGIC_VECTOR (7 downto 0); -- data recived
  RX_full    : in  STD_LOGIC;  -- Indicate a byte is ready to be read from UART
  TX_busy_n  : in  STD_LOGIC;  -- Active low: indicate UART is busy transmitting
  RD_n       : out  STD_LOGIC; -- Active low: read a byte from the UART
  WR_n       : out  STD_LOGIC; -- Active low: write a byte to UART for transmission
  data_out   : out  STD_LOGIC_VECTOR (7 downto 0); -- data to transmit
  soft_reset : out std_logic;
-----------------------------------------------------------------------------
-- User Modified
-----------------------------------------------------------------------------
  Reg0In   : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
  Reg1In   : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
-----------------------------------------------------------------------------
  LD0 : out std_logic;
  LD1 : out std_logic;
  LD2 : out std_logic
);
end component;
```