UNIVERSITY OF TEXAS AT DALLAS

800 W Campbell Rd, Richardson, TX 75080, USA

VLSI DESIGN (EECT 6325)

PROJECT DONE ON:
D-FLIP FLOP

Team Members:

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	Transition from 0 to 1	Transition from 1 to 0
$T_{clk->Q}$	4.54 ns	3.16 ns
T_{su_dd}	894 ps	865 ps
T_{hold}	894 ps	865 ps
T_{su_opt}	2.86 ns	1.26 ns
t_d	1.68 ns	4.42 ns

- Height of the Flip-Flop – 9.2 um
- Width of the Flip-Flop – 5.516 um
- Area of the Flip-Flip – 50.74 pm^2

ACKNOWLEDGEMENT

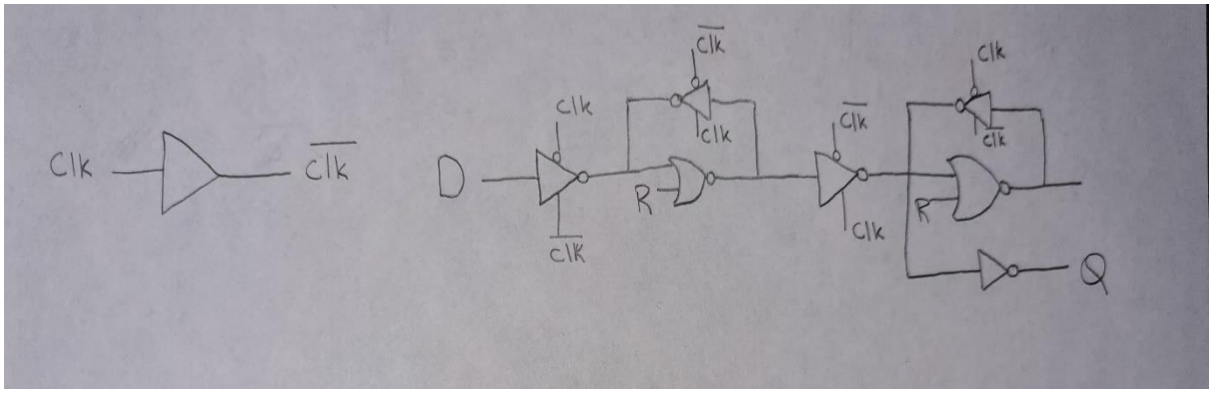
We are grateful to Professor CARL SECHEN for providing us an opportunity to explore and conduct Flip-Flop based projects in VLSI Design.

We also take this opportunity to express our gratitude to MR VAIBHAV KUMARSWAMY SALIMATH for his guidance in conducting the project.

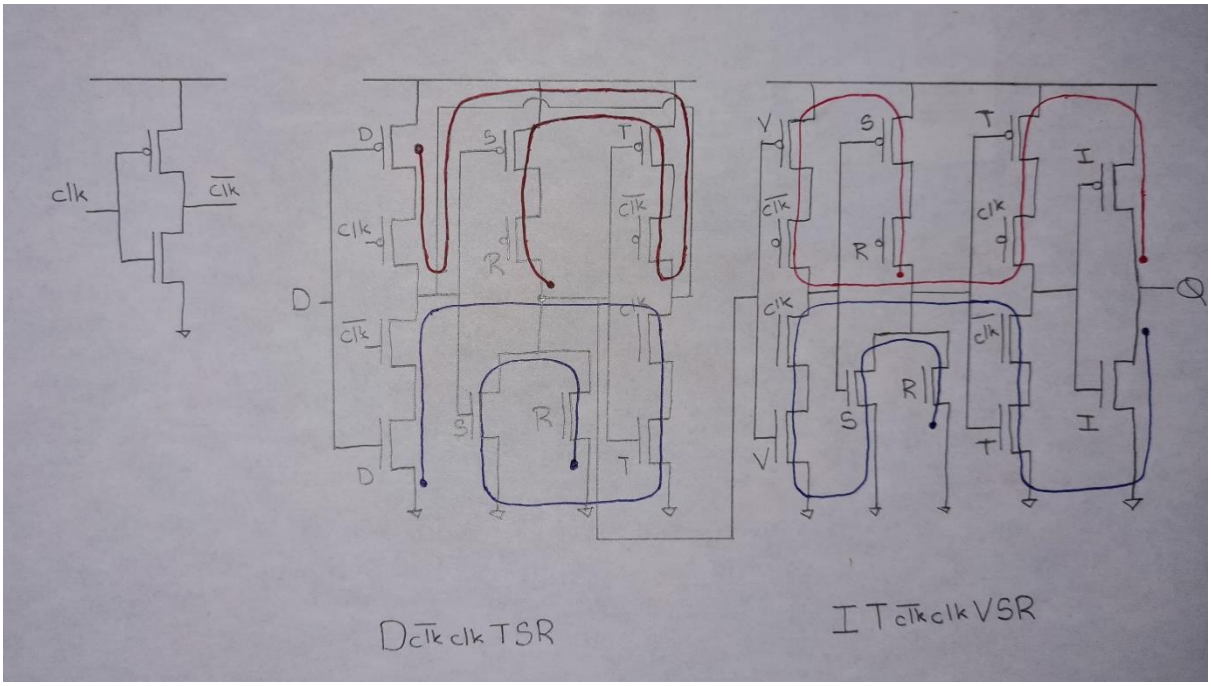
OBJECTIVE

In this project, we have used the Cadence Design tools to design, layout and characterize the D-Flip-Flop by minimizing the diffusion breaks and cell width.

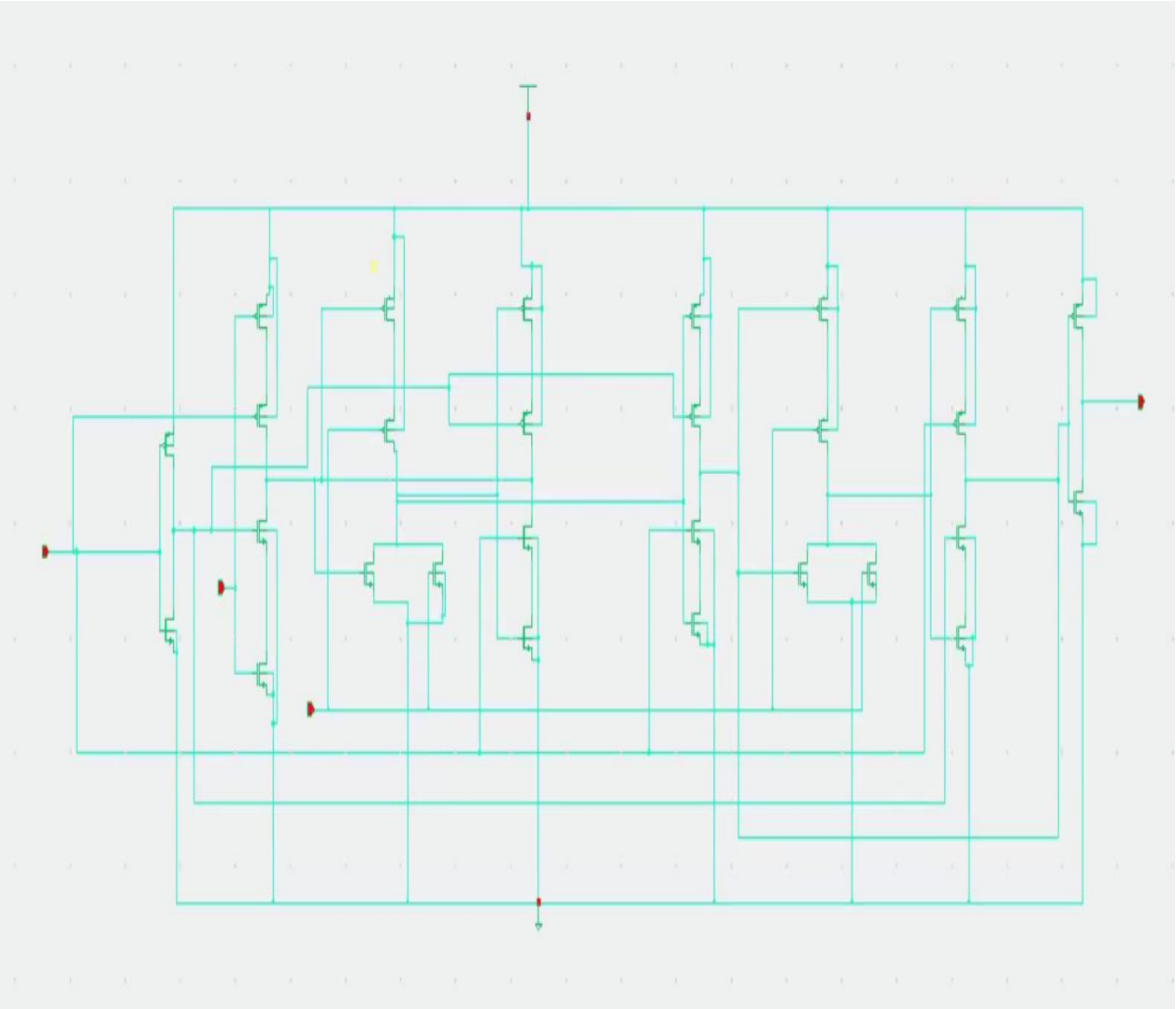
D FLIP-FLOP



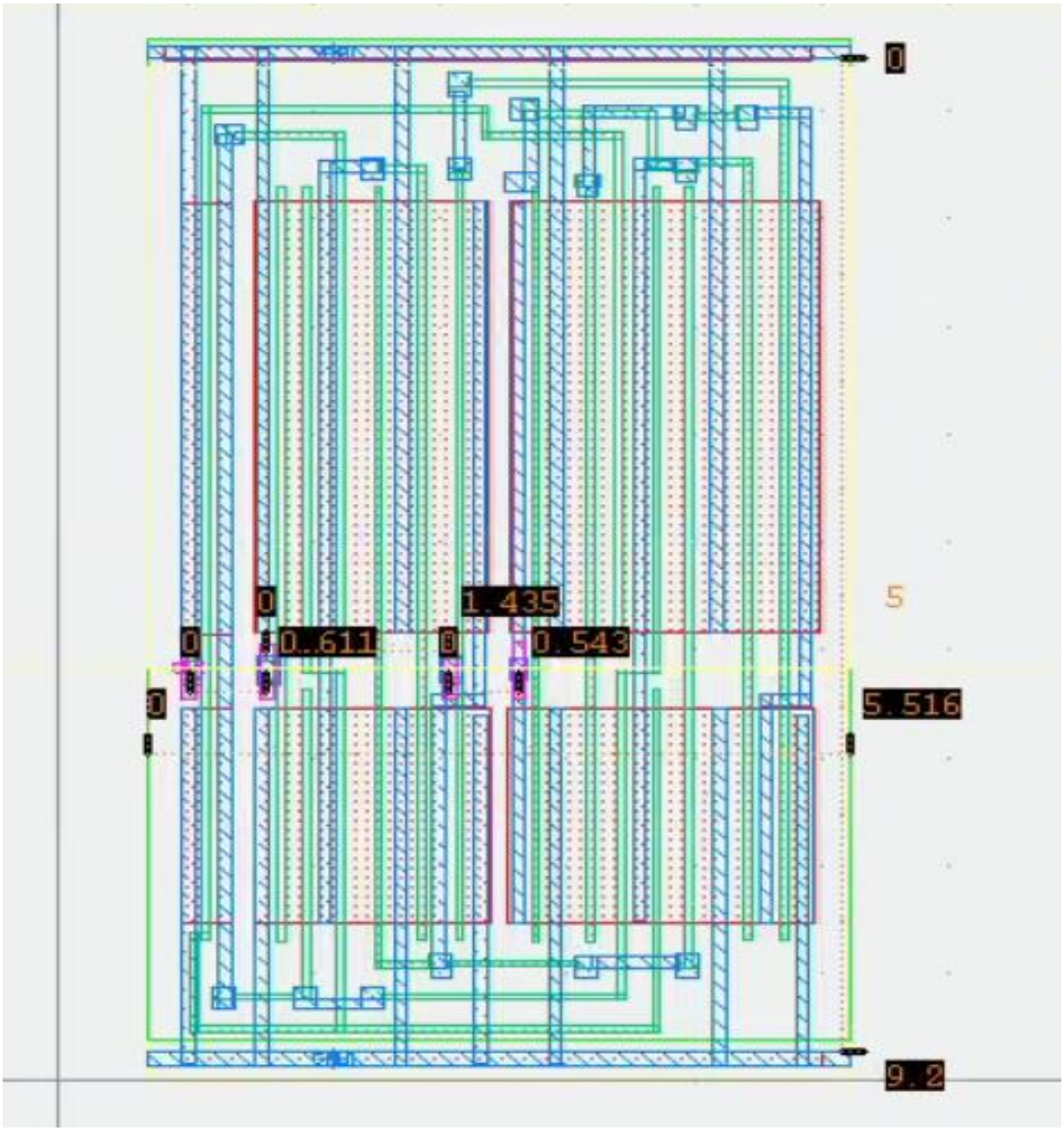
EULER TRAIL



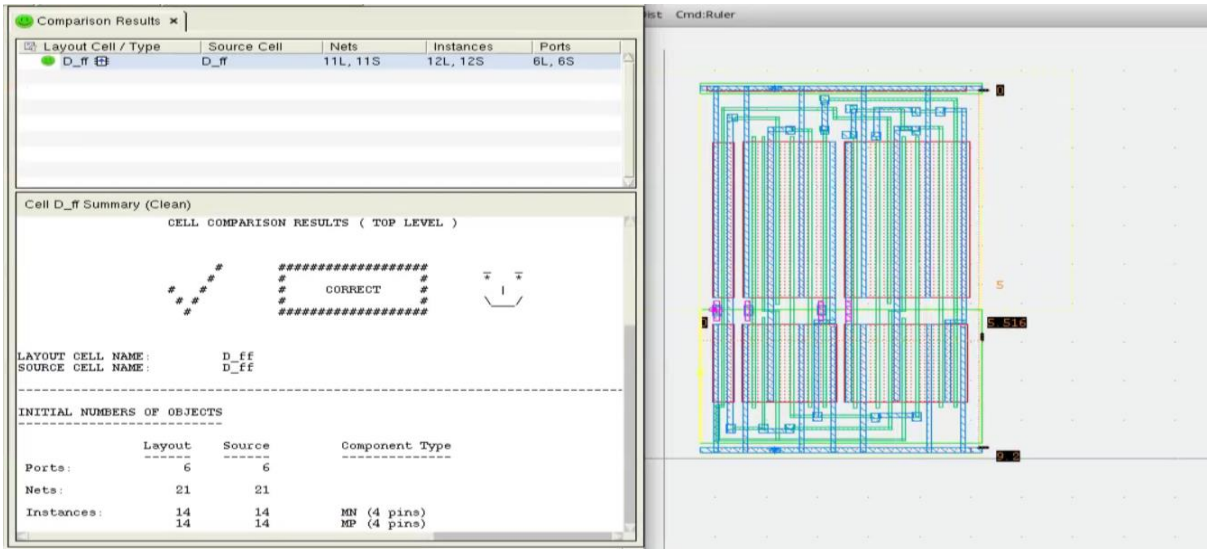
SCHEMATIC



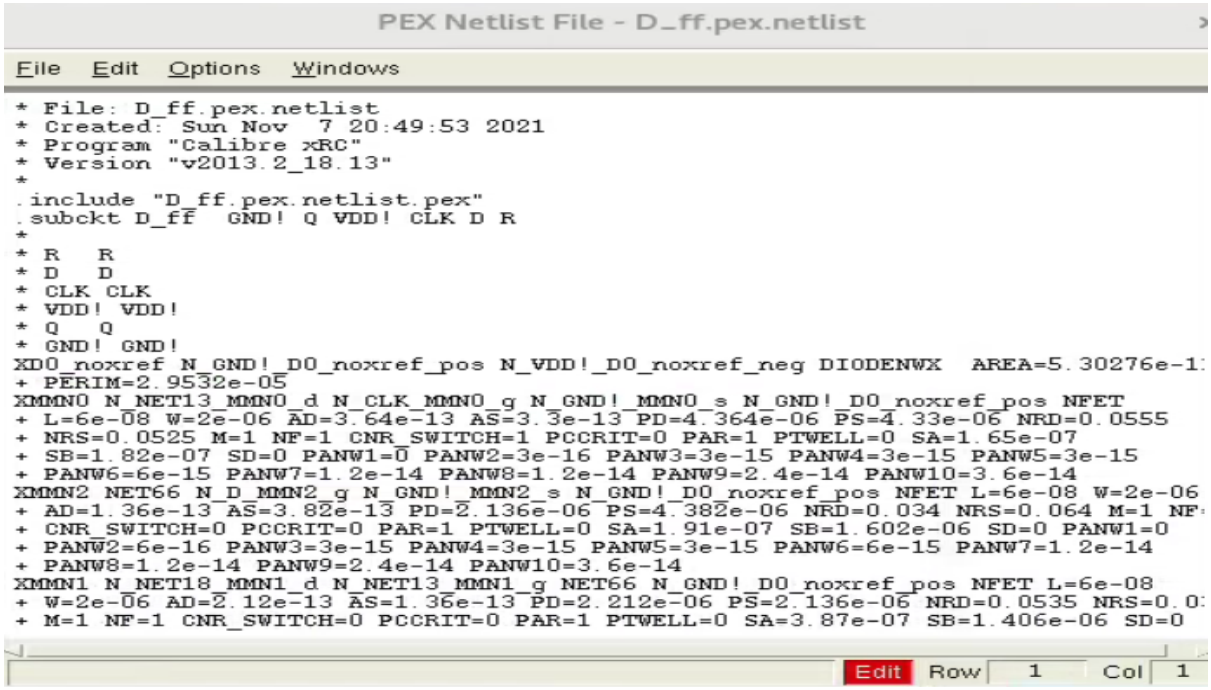
LAYOUT



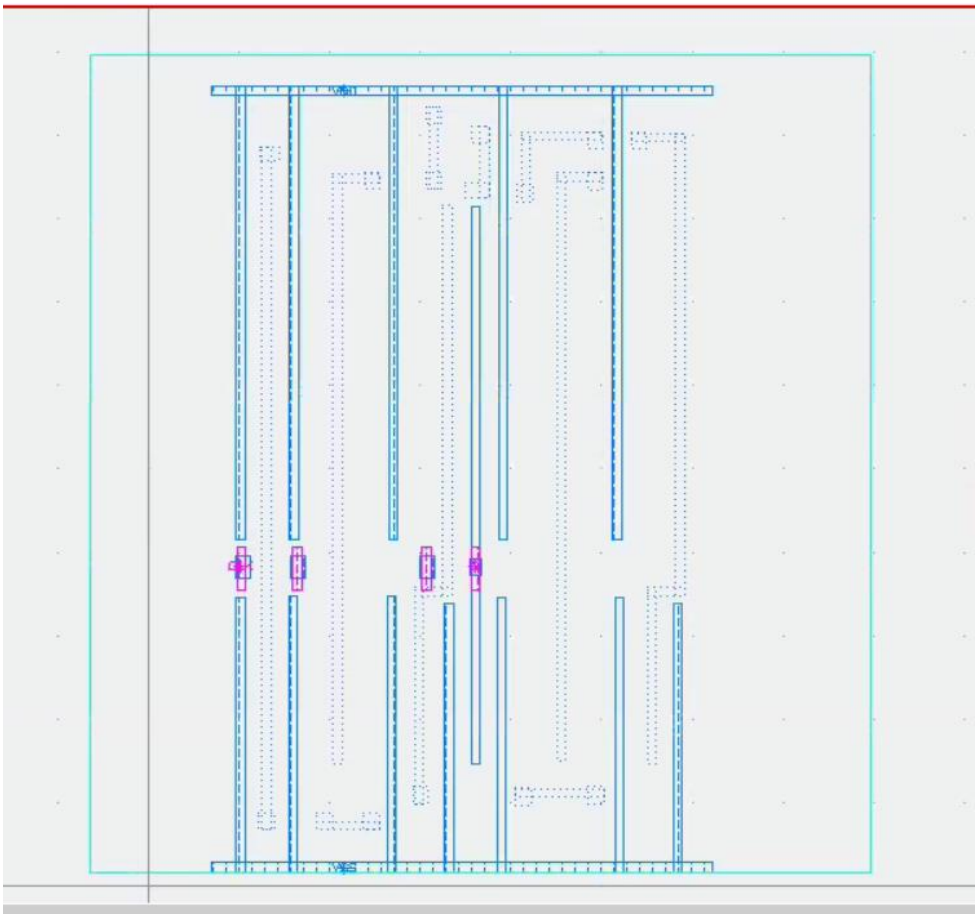
- Layout vs Schematic match



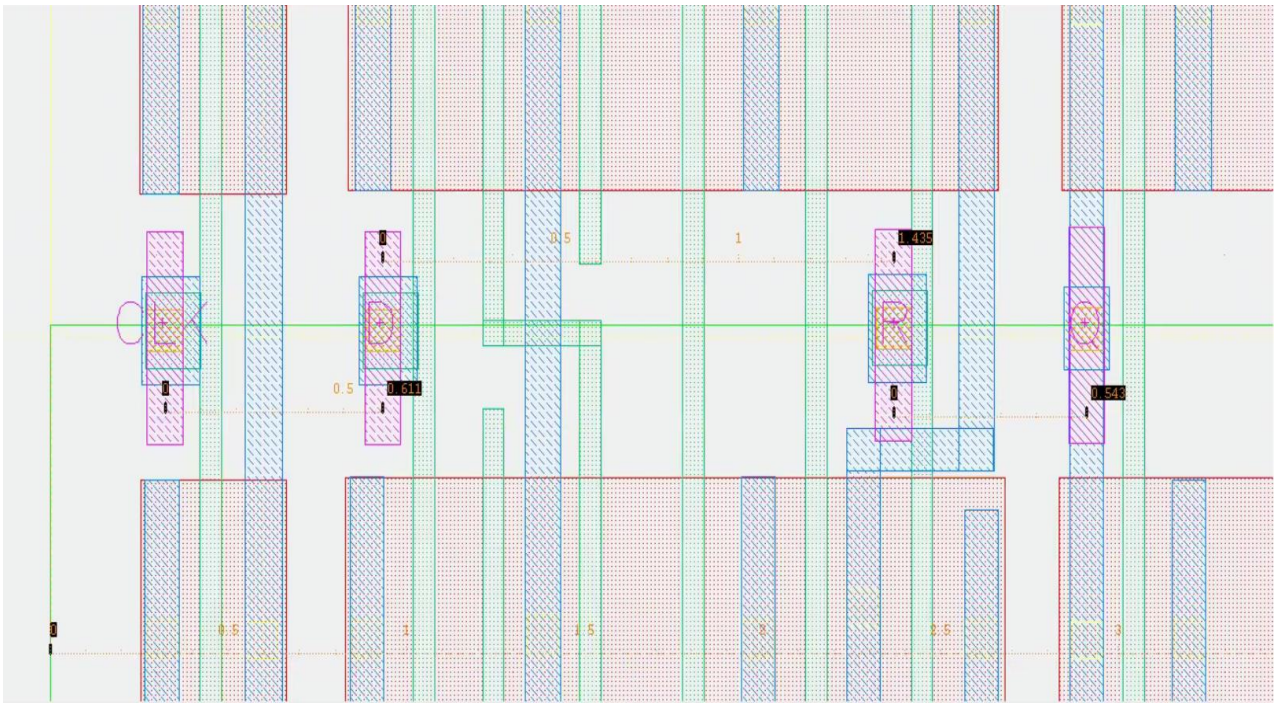
- Generated PEX File:



ABSTRACT



PIN MEASUREMENTS



SIMULATION AND WAVEFORM

D FLIP-FLOP FUNCTIONALITY:

- SPICE FILE:

$example HSPICE setup file

$transistor model
.include"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

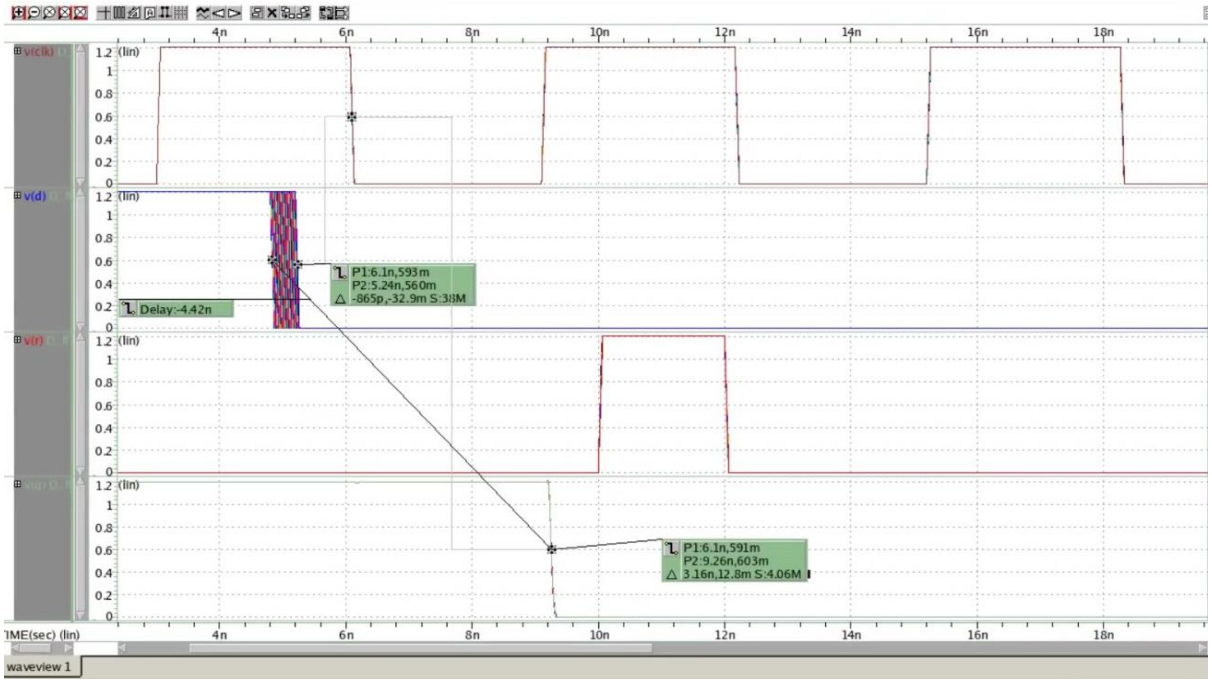
.include D_flip_flop_connection.pex.sp
.option post runlvl=5

xi GND! Q VDD! CLK D R D_flip_flop_connection
vdd vdd! gnd! 1.2v
vb CLK gnd! PULSE (0v 1.2v 0ps 0ps 0ps 1000ps 2000ps)
V_D D gnd! pwl (0ns 1.2v 2.5ns 1.2v 2.55ns 0v 6ns 0v 6.05ns 1.2v 8ns 1.2v 8.06666ns 1.2v 16ns 1.2v 16.06666ns 1.2v 22ns 1.2v 22.06666ns 0v 28ns 0v 28.06666ns 1.2v 32ns 1.2v)
V_R R gnd! pwl (0ns 0v 10ns 0v 10.06666ns 1.2v 11ns 1.2v 12ns 1.2v 12.06666ns 0v)
cout Q GND! 90f

$transient analysis
.tr 100ps 12ns
.end

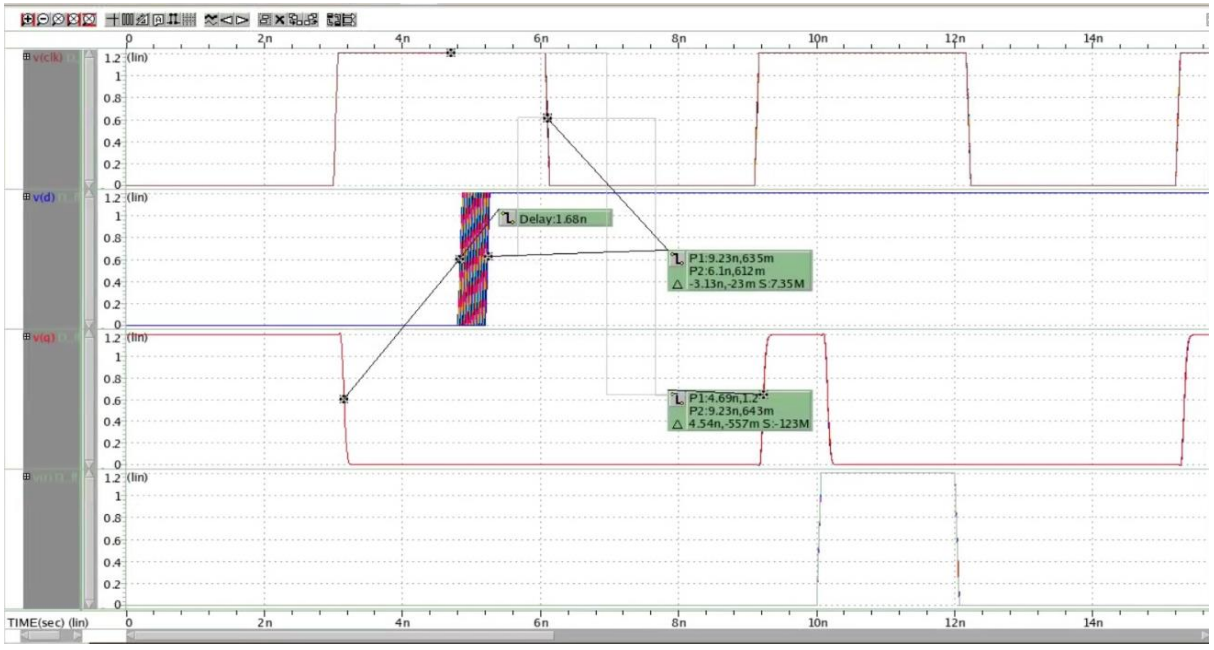
- SPICE FILE FOR PASSING 0:

```
$example HSPICE setup file
$transistor model
.include
"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_2016
0415/models/YI-SM00030/Hspice/models/design.inc"
.include "D_ff.pex.netlist"
.global vdd! gnd!
.option post runlvl=5
xi GND! Q VDD! CLK D R D_ff
VDD VDD! GND! 1.2v
vclk clk gnd! PULSE (0v 1.2v 3ns 66.66ps 66.66ps 3ns 6.1ns)
vd D gnd! pwl (0ns 1.2v 't1'1.2v 't1+0.066ns' 0v)
vr R gnd! pwl (0ns 0v 10ns 0v 10.06666ns 1.2v 11ns 1.2v 12ns 1.2v
12.06666ns 0v)
cout Q gnd! 50f
.MEAS tsetup TRIG v(d) VAL=0.6V FALL=1 TARG v(clk) VAL=0.6v
FALL=3
.MEAS tclktoq TRIG v(clk) VAL=0.6v FALL=3 TARG v(Q) VAL=0.6v
FALL=1
.MEAS tran tdelay param='tsetup+tclktoq'
.trans 10ps 40ns sweep t1 4800ps 5200ps 5ps
.end
```



- SPICE FILE FOR PASSING 1:

```
$example HSPICE setup file
$transistor model
.include
"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_
11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "D_ff.pex.netlist"
.global vdd! gnd!
.option post runlvl=5
xi GND! Q VDD! CLK D R D_ff
VDD VDD! GND! 1.2v
vclk clk gnd! PULSE (0v 1.2v 3ns 66.66ps 66.66ps 3ns 6.1ns)
vd D gnd! pwl (0ns 0v 't1'0v 't1+0.066ns' 1.2v)
vr R gnd! pwl (0ns 0v 10ns 0v 10.06666ns 1.2v 11ns 1.2v 12ns
1.2v 12.06666ns 0v)
cout Q gnd! 50f
.MEAS tsetup TRIG v(d) VAL=0.6V FALL=1 TARG v(clk)
VAL=0.6v FALL=3
.MEAS tclktoq TRIG v(clk) VAL=0.6v FALL=3 TARG v(Q)
VAL=0.6v FALL=1
.MEAS tran tdelay param='tsetup+tclktoq'
.trans 10ps 40ns sweep t1 4800ps 5200ps 5ps
.end
```



- We generated a batch of inputs to find Tsu_dd, Tsu_opt and calculation of Tclk->q,

```
$DATA1 SOURCE='HSPICE' VERSION='L-2016.06-SP1-2 linux64' PARAM_COUNT=1
.TITLE '$example hspice setup file'
 t1              tsetup          tclktoq         temper
                 alter#
  4.800e-09       1.347e-08      -9.044e-09        25.0000
                1
  4.810e-09       1.346e-08      -9.044e-09        25.0000
                1
  4.820e-09       1.345e-08      -9.044e-09        25.0000
                1
  4.830e-09       1.344e-08      -9.044e-09        25.0000
                1
  4.840e-09       1.343e-08      -9.044e-09        25.0000
                1
  4.850e-09       1.342e-08      -9.044e-09        25.0000
                1
  4.860e-09       1.341e-08      -9.044e-09        25.0000
                1
  4.870e-09       1.340e-08      -9.044e-09        25.0000
                1
  4.880e-09       1.339e-08      -9.044e-09        25.0000
                1
  4.890e-09       1.338e-08      -9.044e-09        25.0000
                1
  4.900e-09       1.337e-08      -9.044e-09        25.0000
                1
  4.910e-09       1.336e-08      -9.044e-09        25.0000
                1
  4.920e-09       1.335e-08      -9.044e-09        25.0000
                1
  4.930e-09       1.334e-08      -9.044e-09        25.0000
                1
  4.940e-09       1.333e-08      -9.044e-09        25.0000
                1
  4.950e-09       1.332e-08      -9.044e-09        25.0000
                1
  4.960e-09       1.331e-08      -9.044e-09        25.0000
```

EXPLANATION

- DROP DEAD SETUP TIME (T_{su}_dd): T_{su}_dd is the minimum time that is taken by the input to arrive before the active clock edge so that input signal can be captured at the output. This is usually calculated by plotting a graph of setup time vs gate time delay.

- OPTIMUM SETUP TIME (T_{su}_opt): Optimum Setup time is defined as the setup time for which time delay(t_d) is minimum. T_{su}_opt + $T_{clk>Q}$ = t_d

- HOLD TIME (T_{hold}): The minimum amount of time that the data signal should be held steady after the clock even making sure the data is processed is called hold time.
  T_{su}_dd(1) = Thold(0) and T_{su}_dd(0) = Thold(1).

- T CLK TO Q ($T_{clk->Q}$): The clk to Q time is the time required for the output to have a stable/valid value after the falling edge of the clock. It is the time difference between 50% amplitude of the clock and the output.

- DELAY TIME(t_d): Delay time is defined as t_d = T_{su}_opt + $T_{clk>Q}$

RESULT

The functionality of D-flip flop is verified.