UNIVERSITY OF TEXAS AT DALLAS

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VLSI DESIGN (EECT 6325)

Project Done On:

INVERTER DESIGN, LAYOUT AND SIMULATION

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Obtained Result:

1.	ENERGY (E)	-1.076e - 11
2.	DELAY (D)	1.104e - 10
3.	EDP	1.188e - 23
4.	AREA	W = 0.649 um & H = 5.539 um A = W*H = 3.594 pm^2

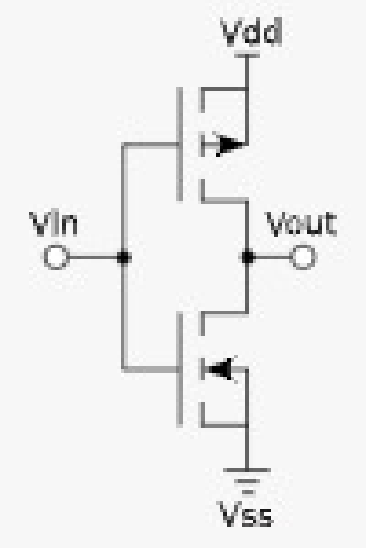
ACKNOWLEDGEMENT

We are grateful to Professor CARL SECHEN for providing us an opportunity to explore and conduct projects based on VLSI Design.

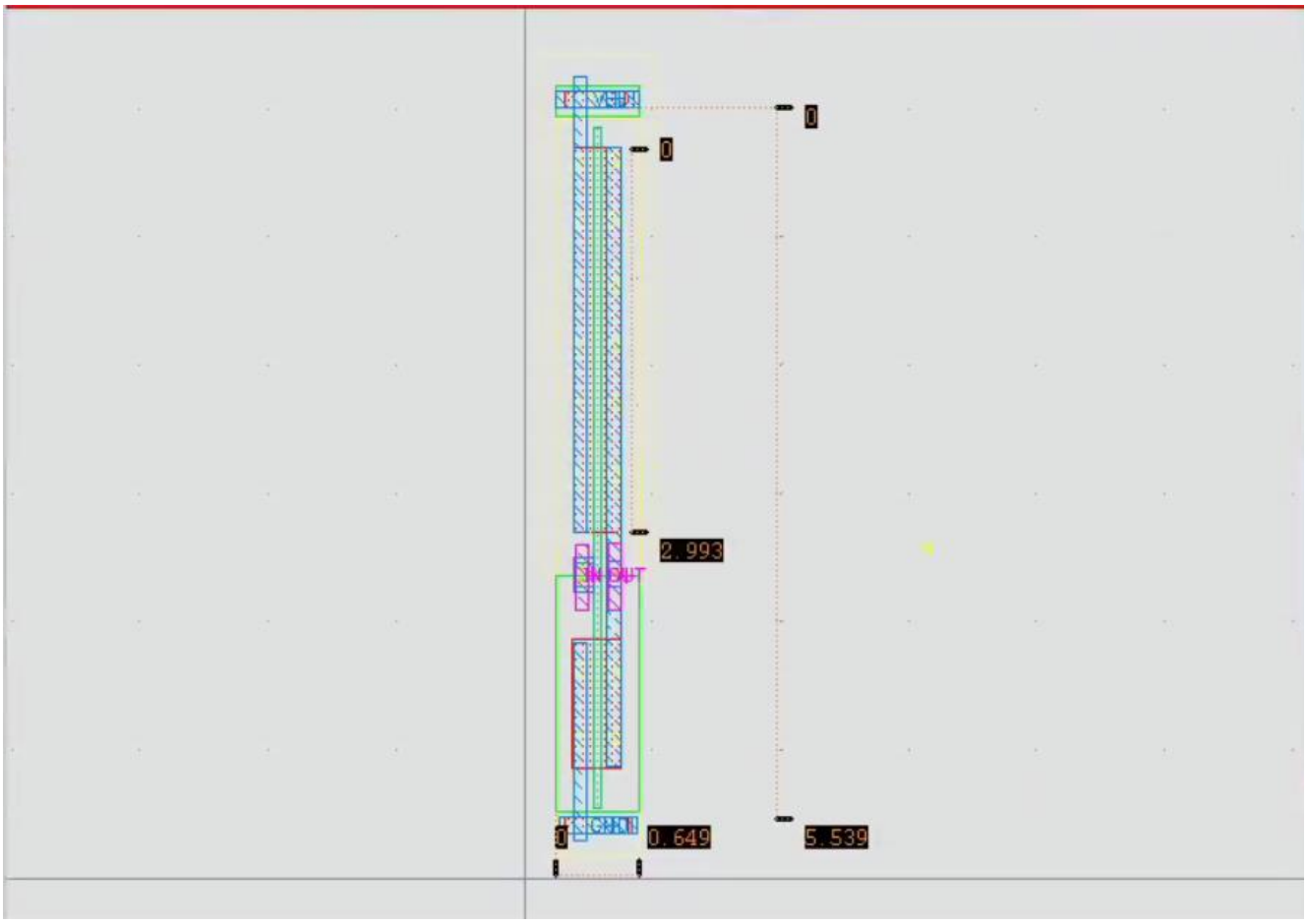
We also take this opportunity to express our gratitude to MR VAIBHAV KUMARSWAMY SALIMATH for his guidance in conducting the project.

INTRODUCTION

An inverter circuit outputs a voltage representing the opposite logic-level to its input. Its main function is to invert the input signal applied. If the applied input is low then the output becomes high and vice versa. Inverters can be constructed using a single NMOS transistor or a single PMOS transistor. It is called as CMOS inverter as it has both NMOS and PMOS

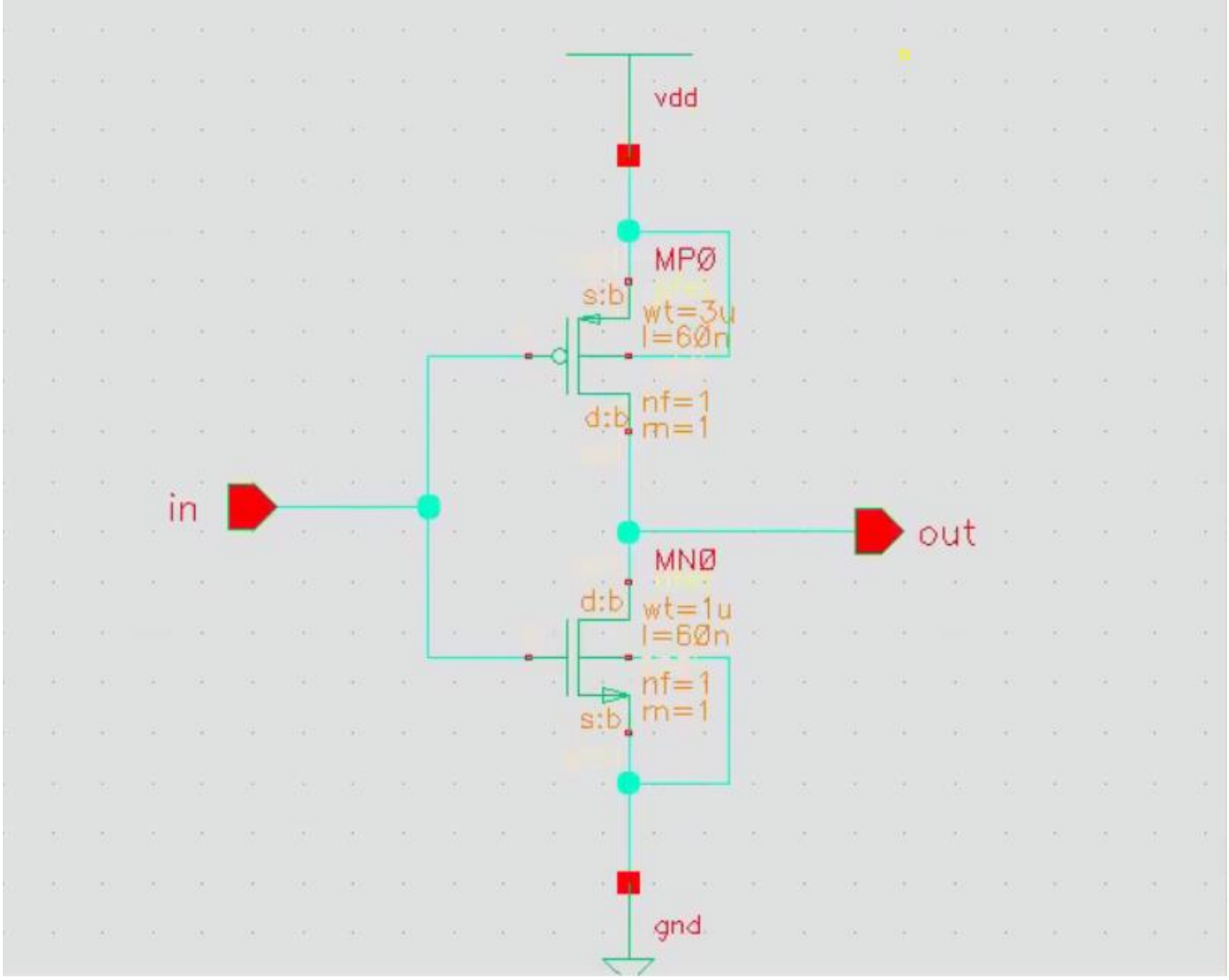


INVERTER LAYOUT



The MOS inverter we designed has a gate width of 0.06 um, the width of pMOS being 3 um and the width being 1 um. Here we have maintained the pMOS to nMOS width ratio as 3:1.
The distance between the top and bottom M1 metal layer is 5.539 um and the width is 0.649 um. The total area is 3.59 pm^2.

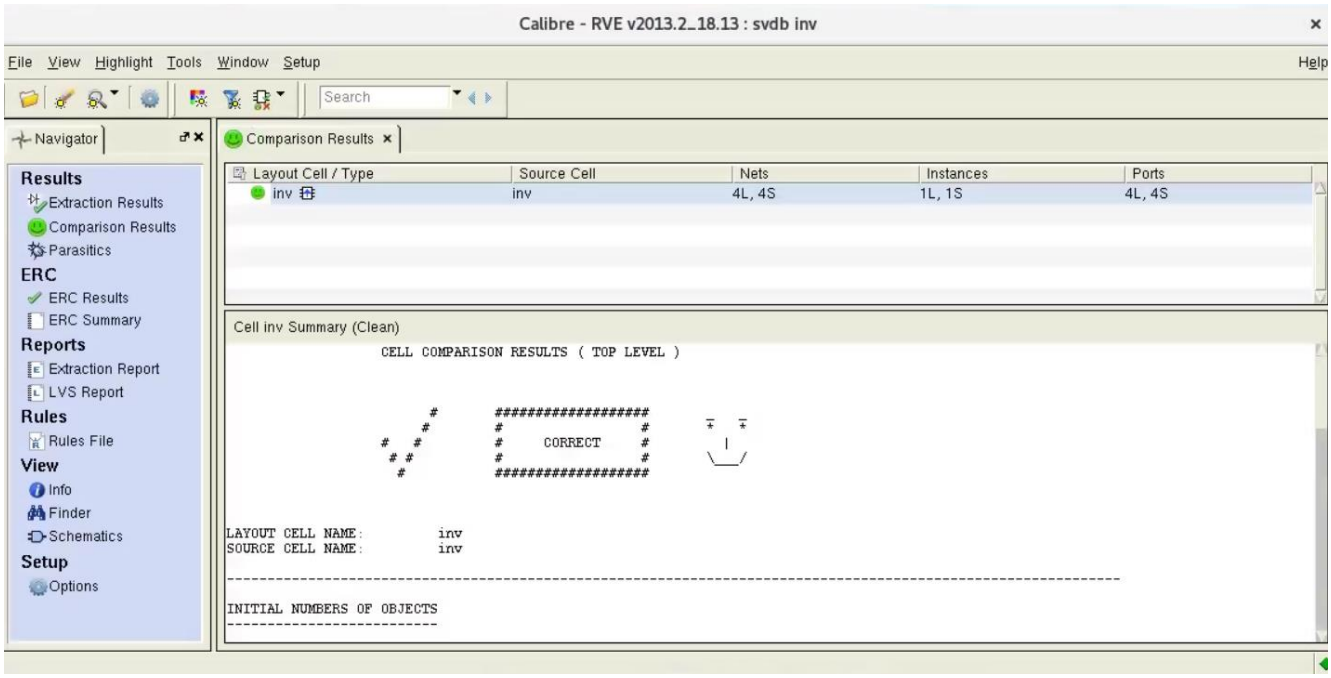
INVERTER SCHEMATIC



DESIGN RULE CHECK OUTPUT

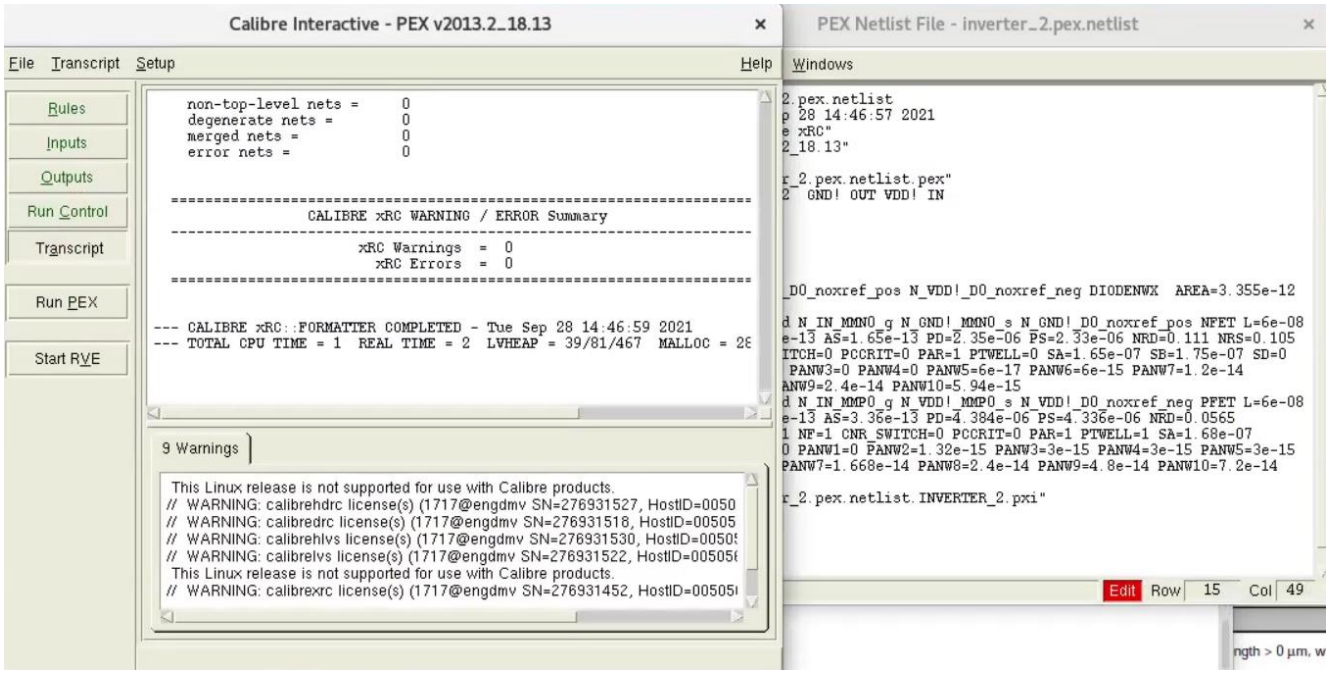
The DESIGN RULE CHECK was successful with zero errors.

LAYOUT VS SCHEMETIC OUTPUT



The LAYOUT VS SCHEMETIC test was also successful with zero warnings.

CREATION OF PEX FILE FOR H-SPICE

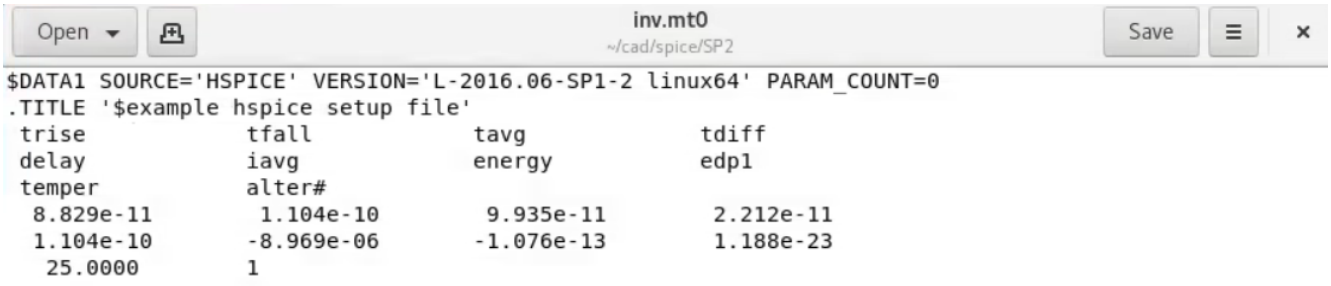


SPICE TEST SETUP FILE

```
$example HSPICE setup file

$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "inv.pex.netlist"


.option post runlvl=5

xi GND! OUT VDD! IN inv

vdd VDD! GND! 1.2v
vin IN GND! pwl(0ns 1.2v 1ns 1.2v 1.0833ns 0v 6ns 0v 6.0833ns 1.2v 12.00ns 1.2v)
cout OUT GND! 70f

$transient analysis
.tr 100ps 12ns
$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp
$.tr 100ps 12ns sweep WP 1u 9u 0.5u

.measure tran trise trig v(IN) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1 $measure tlh at 0.6v
.measure tran tfall trig v(IN) val=0.6v rise=1 targ v(OUT) val=0.6v fall=1 $measure tpl at 0.6v
.measure tavg param = '(trise+tfall)/2' $calculate average delay
.measure tdiff param='abs(trise-tfall)' $calculate delay difference
.measure delay param='max(trise,tfall)' $calculate worst case delay

$ method 1
.measure tran iavg avg i(vdd) from=0 to=10n $average current in one clock cycle
.measure energy param='1.2*iavg*10n' $calculate energy in one clock cycle
.measure edp1 param='abs(delay*energy)'

.end
```

EDP MINIMIZATION

The EDP of the first design was 1.197e – 23 with pMOS to nMOS ratio of 3:1 and the area being 5.9384 pm^2. Our current design was able to achieve EDP of 1.188e – 23 with the same pMOS and nMOS ratio with the area of 3.594 pm^2. This reduction in EDP was achieved by reducing the width by 0.355 um (from 1.04 um to 0.649 um) and also height by 0.171 um (from 5.71 um to 5.539 um). By this reduction in height and width resulted in the reduction in overall area, which further minimized the value of EDP.



HEIGHT AND WIDTH OF nMOS & pMOS

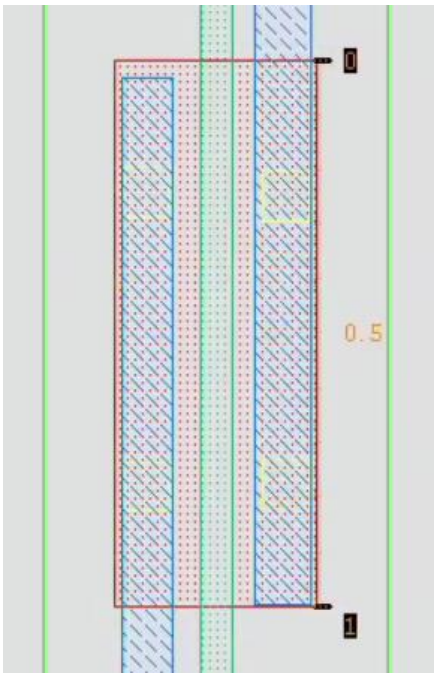


Fig. Height of nMos

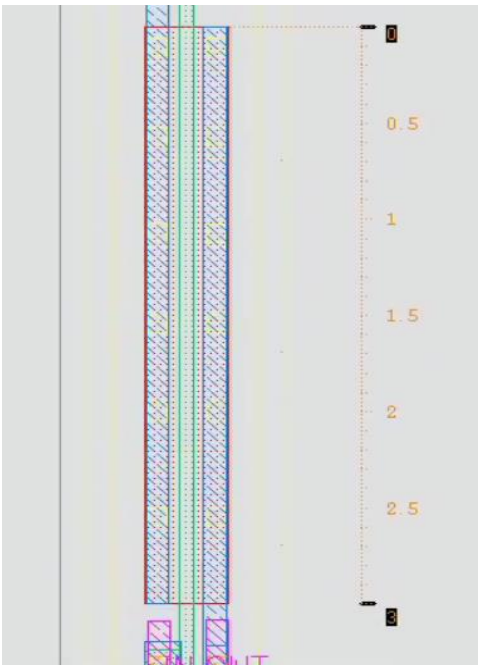


Fig. Height of pMOS

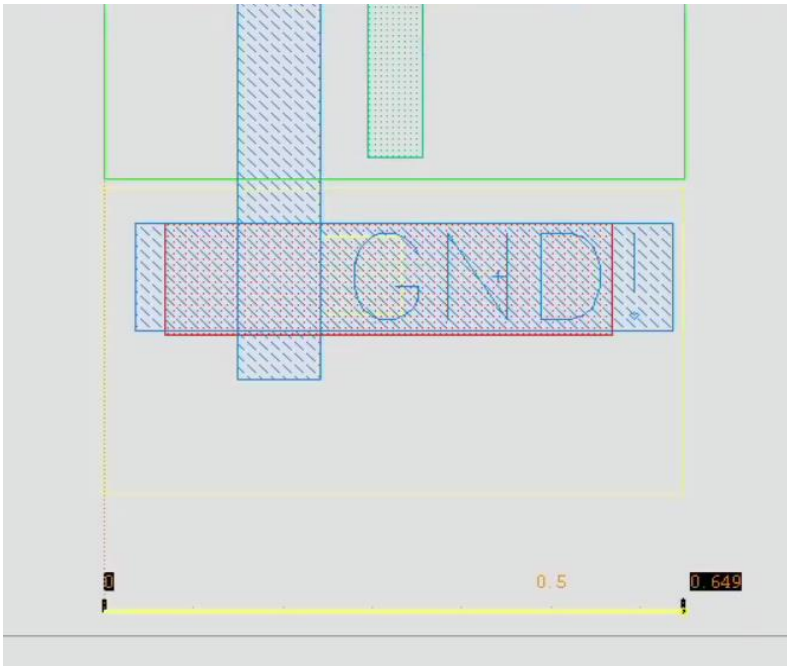
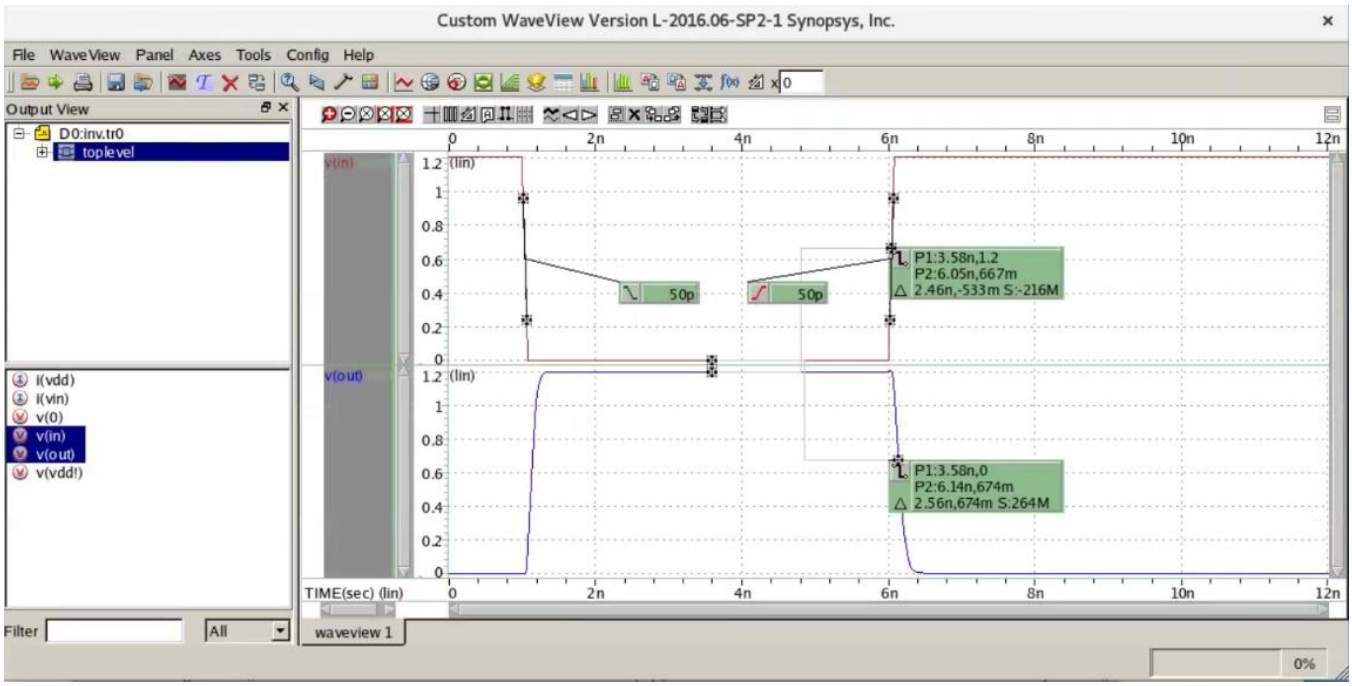


Fig. Width

I/O WAVEFORM


Custom WaveView Version L-2016.06-SP2-1 Synopsys, Inc.
File WaveView Panel Axes Tools Config Help
Output View
D0:inv.tr0
toplevel
i(vdd)
i(vin)
v(0)
v(in)
v(out)
v(vdd!)
Filter
All
v(in)
v(out)
(lin)
50p
50p
P1:3.58n,1.2
P2:6.05n,667m
Δ 2.46n,-533m S:-216M
P1:3.58n,0
P2:6.14n,674m
Δ 2.56n,674m S:264M
TIME(sec) (lin)
0
2n
4n
6n
8n
10n
12n
waveview 1
0%

CONCLUSION

The inverter layout and schematic designed through the cadence tool was successful completed without any errors by passing both DRC and LVS test. Our design has also successfully minimized the value of EDP and the result obtained has been plotted on WaveView.