UNIVERSITY OF TEXAS AT DALLAS

800 W Campbell Rd, Richardson, TX 75080, USA

VLSI DESIGN (EECT 6325)

Project Done On:

CELL LIBRARY DESIGN AND LAYOUT

Team Members:

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ACKNOWLEDGEMENT

We are grateful to Professor CARL SECHEN for providing us an opportunity to explore and conduct projects based on VLSI Design.

We also take this opportunity to express our gratitude to MR VAIBHAV KUMARSWAMY SALIMATH for his guidance in conducting the project.

OBJECTIVE

In this project, the below mentioned cells are designed and laid out to form a cell library,

- INVERTER
- NAND2
- NOR2
- XOR2
- MUX2:1
- AOI22
- AOI211
- OAI21

All the cells mentioned above were placed next to each other with their boundaries touching each other. There were no DRC errors when we checked the cells individually and when they were placed together.

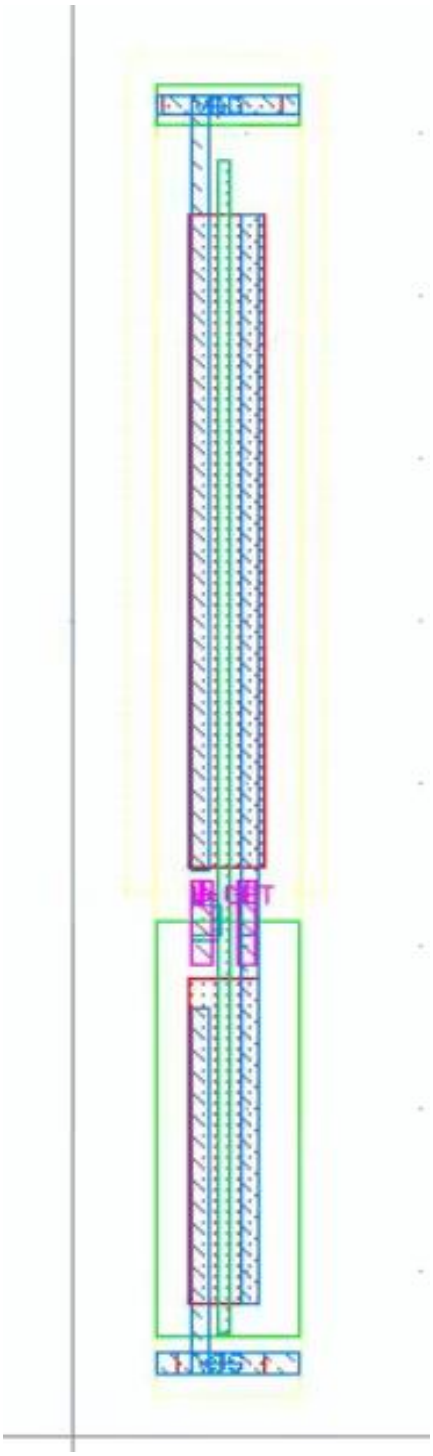
INVERTER

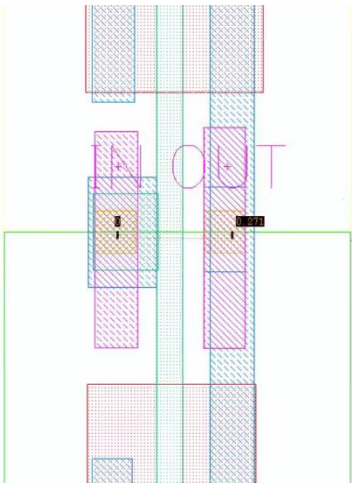
Dimensions of cell:

Height – 7.605 um

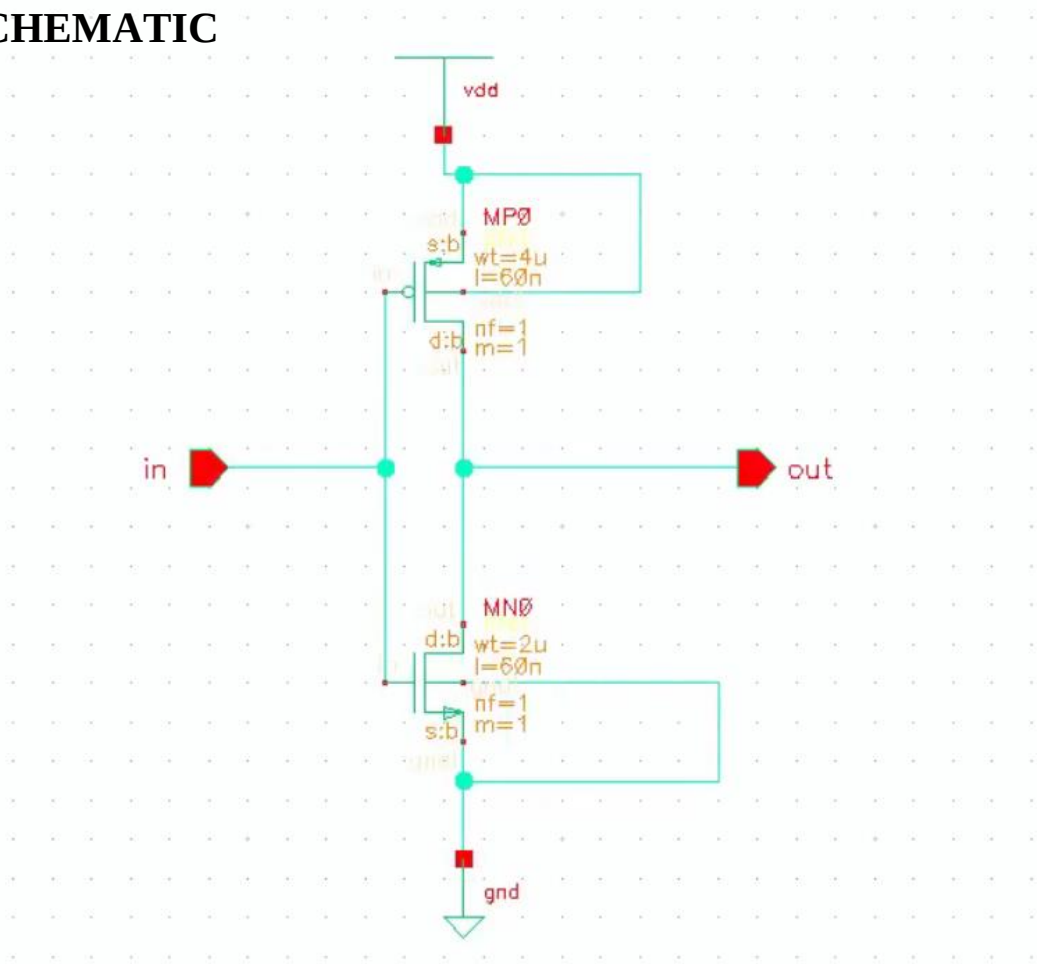
Width – 0.784 um

- **LAYOUT :**





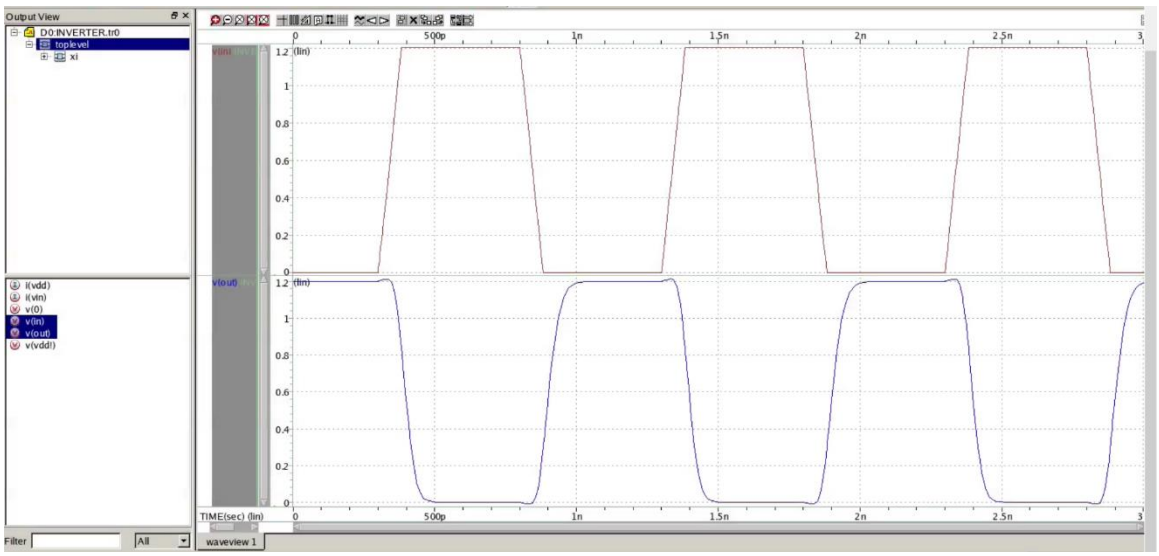
- **SCHEMATIC**



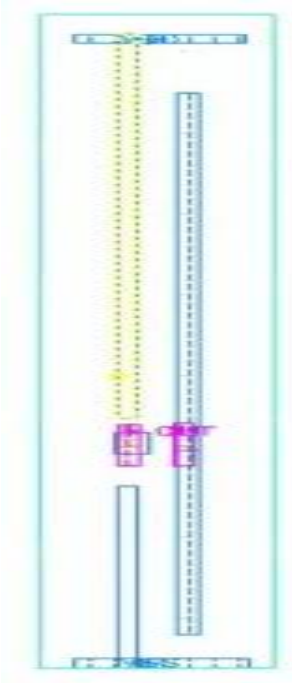
- **TRUTH TABLE**

INPUT	OUTPUT
0	1
1	0

- **WAVEFORM**



- **ABSTRACT**



- **NETLIST**

NoMachine - VLSI_DESIGN

Activities File Viewer -

File Edit Options Windows

```
* File: INVERTER.pex.netlist
* Created: Fri Oct 22 00:32:47 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "INVERTER.pex.netlist.pex"
.subckt INVERTER  GND! OUT VDD! IN
*
* IN  IN
* VDD VDD
* OUT OUT
* VSS VSS
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=5.6694e-12
+ PERIM=1.2508e-05
XMMN0 N_OUT_MMN0_d N_IN_MMN0_g N_GND!_MMN0_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=3.5e-13 AS=3.3e-13 PD=4.35e-06 PS=4.33e-06 NRD=0.0555 NRS=0.0525
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.65e-07 SB=1.75e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=5.16e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP0 N_OUT_MMP0_d N_IN_MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=7.68e-13 AS=6.72e-13 PD=8.384e-06 PS=8.336e-06 NRD=0.02835
+ NRS=0.02625 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.68e-07
+ SB=1.92e-07 SD=0 PANW1=7.56e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15
+ PANW5=3e-15 PANW6=4.86e-13 PANW7=1.2e-14 PANW8=1.32e-14 PANW9=4.8e-14
+ PANW10=7.2e-14
*
.include "INVERTER.pex.netlist.INVERTER.pxi"
*
.ends
*
*
```

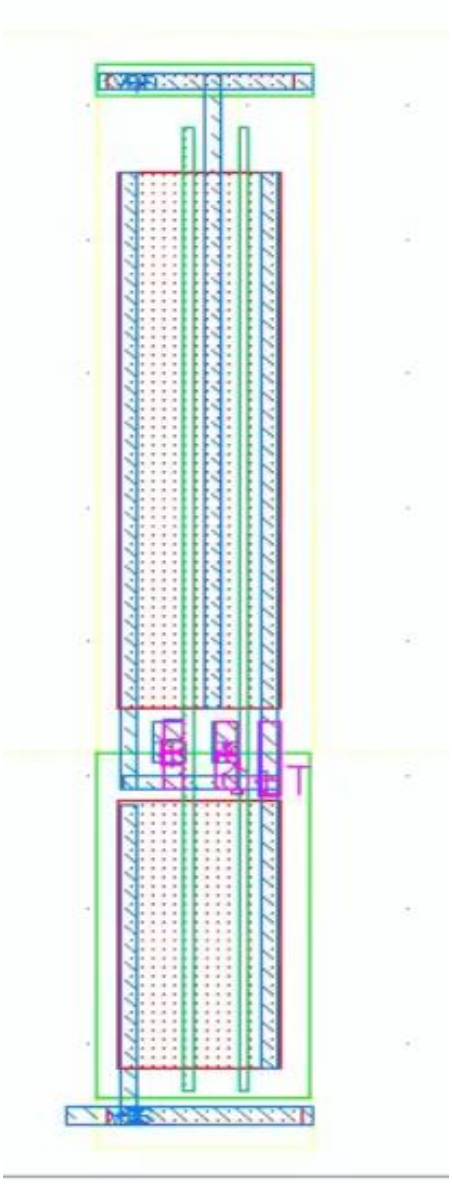
NAND2

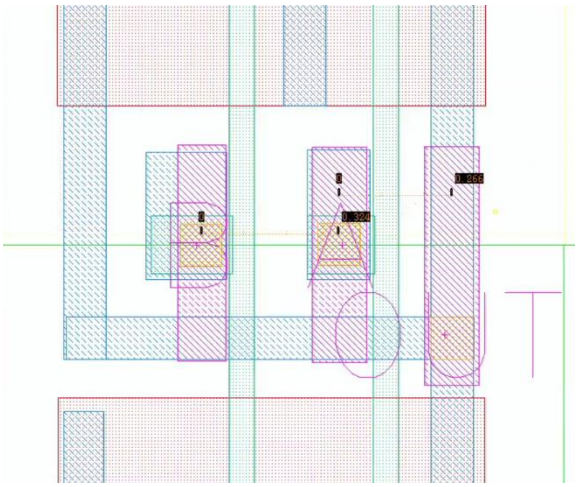
Dimensions of cell:

Height – 7.605 um

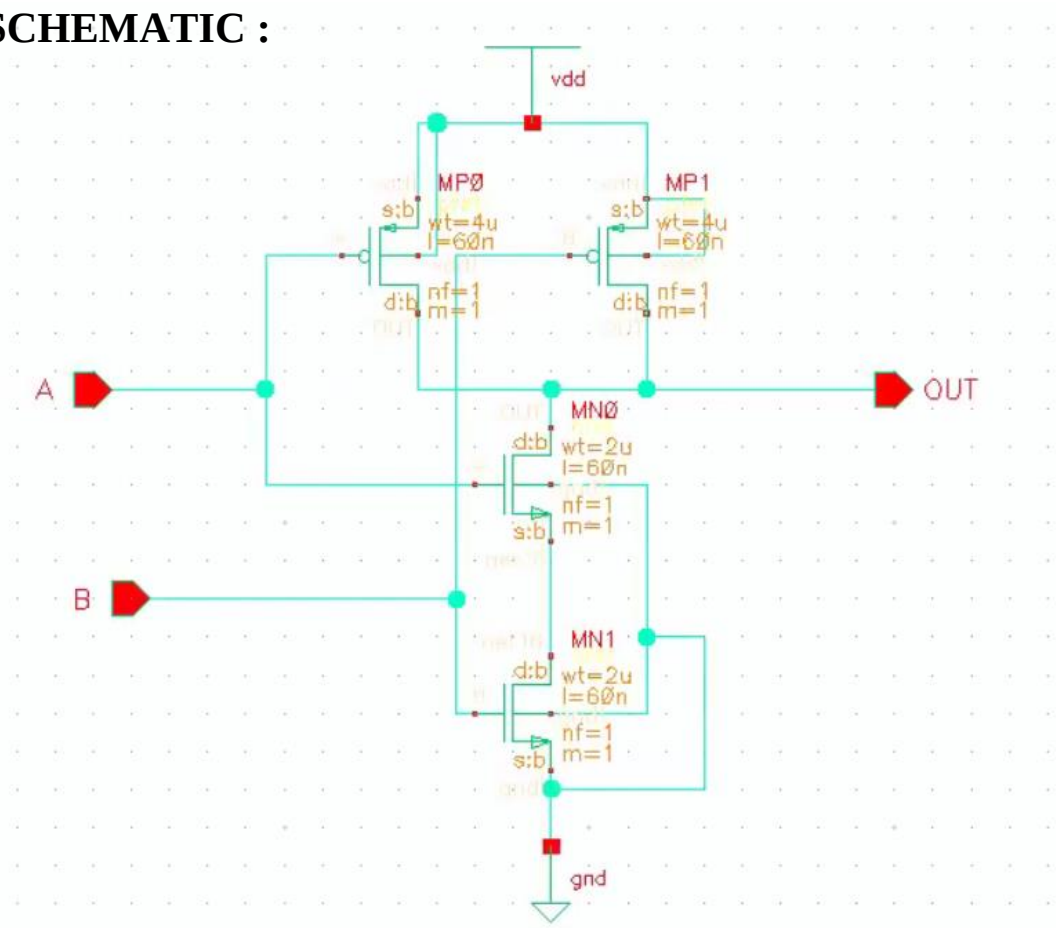
Width – 1.336 um

- **LAYOUT :**





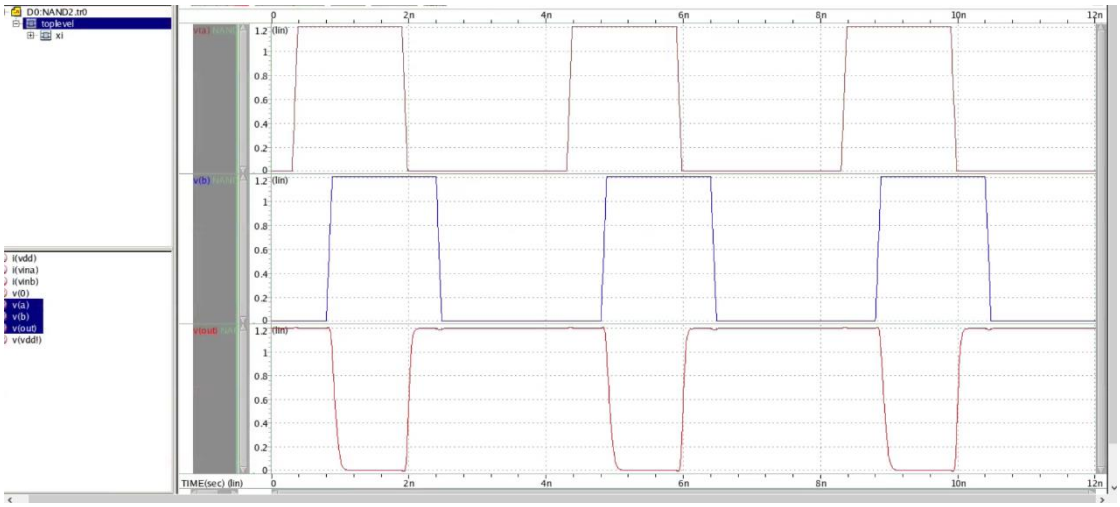
- **SCHEMATIC :**



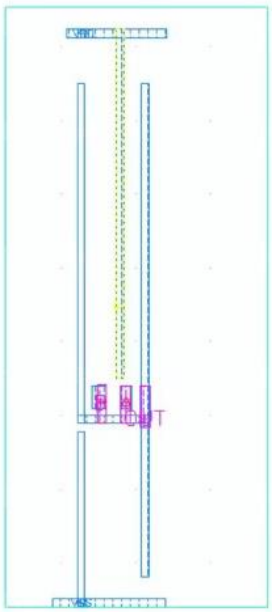
- **TRUTH TABLE**

INPUT A	INPUT B	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

- **WAVEFORM**



- **ABSTRACT**



- **NETLIST :**

NoMachine - VLSI_DESIGN

Activities File Viewer -

File Edit Options Windows

```
* File: NAND2.pex.netlist
* Created: Fri Oct 22 00:39:07 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "NAND2.pex.netlist.pex"
.subckt NAND2  GND! OUT VDD! B A
*
* A   A
* B   B
* VDD VDD
* OUT OUT
* VSS VSS
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=1.90297e-11
+ PERIM=1.7824e-05
XMMN1 NET16 N_B_MMN1_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=2.8e-13 AS=8.08e-13 PD=2.28e-06 PS=4.808e-06 NRD=0.07 NRS=0.172 M=1 NF=1
+ CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=4.04e-07 SB=5.44e-07 SD=0 PANW1=0
+ PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN0 N_OUT_MMN0_d N_A_MMN0_g NET16 N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=4.08e-13 AS=2.8e-13 PD=4.408e-06 PS=2.28e-06 NRD=0.063875 NRS=0.07 M=1 NF=1
+ CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=7.44e-07 SB=2.04e-07 SD=0 PANW1=0
+ PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP1 N_OUT_MMP1_d N_B_MMP1_g N_VDD!_MMP1_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=1.628e-12 AS=5.6e-13 PD=8.814e-06 PS=4.28e-06 NRD=0.086 NRS=0.0295
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=4.07e-07 SB=5.46e-07 SD=0
+ PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=1.7378e-13 PANW10=1.84e-13
XMMP0 N_OUT_MMP0_d N_A_MMP0_g N_VDD!_MMP1_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=8.24e-13 AS=5.6e-13 PD=8.412e-06 PS=4.28e-06 NRD=0.03185 NRS=0.0405
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=7.47e-07 SB=2.06e-07 SD=0
+ PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=4.578e-14 PANW10=5.52e-13
*
.include "NAND2.pex.netlist.NAND2.pxi"
*
.ends
*
```

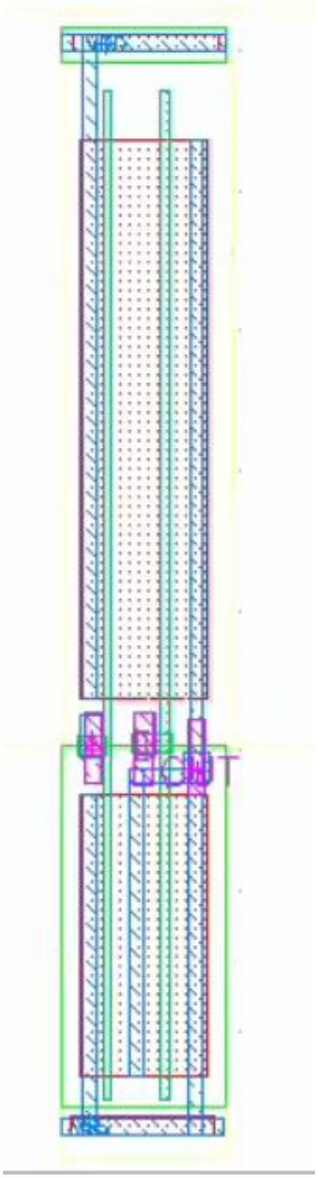
NOR2

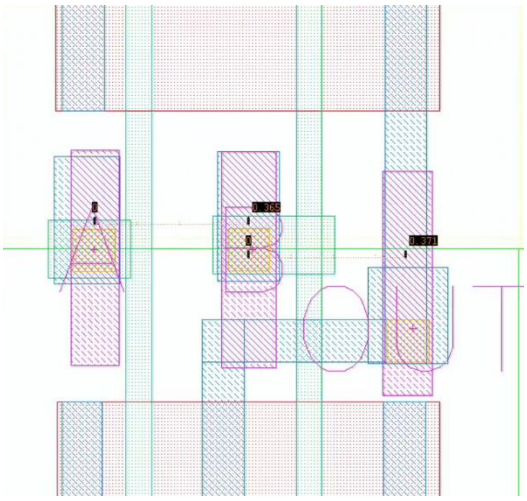
Dimensions of cell:

Height – 7.605 um

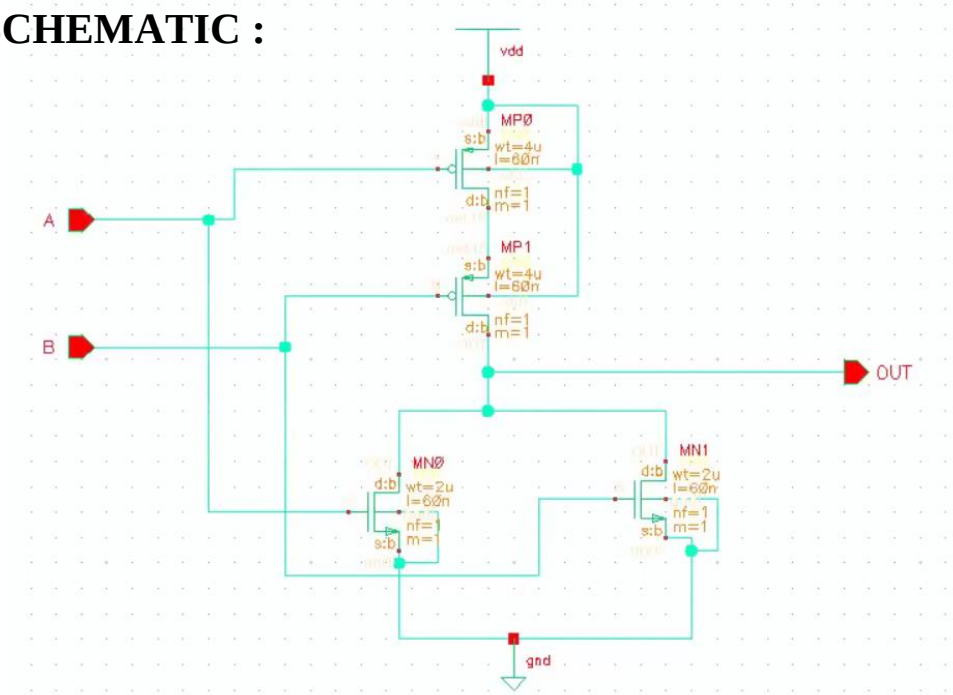
Width – 1.227 um

- **LAYOUT :**





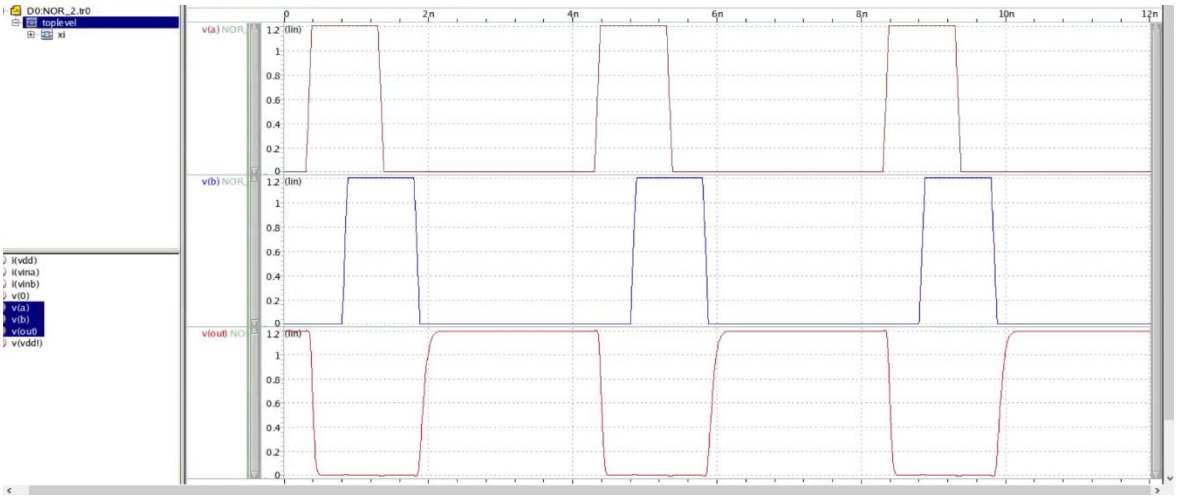
- **SCHEMATIC :**



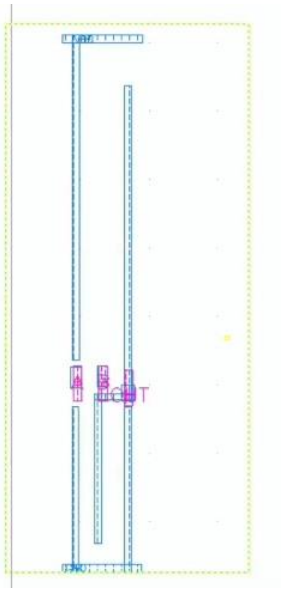
- **TRUTH TABLE**

INPUT A	INPUT B	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

- **WAVEFORM**



- **ABSTRACT**



- **NETLIST :**

NoMachine - VLSI_DESIGN

Activities File Viewer -

File Edit Options Windows

```
* File: NOR_2.pex.netlist
* Created: Fri Oct 22 02:14:48 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "NOR_2.pex.netlist.pex"
.subckt NOR_2  GND! OUT VDD! A B
*
* B   B
* A   A
* VDD VDD
* OUT OUT
* VSS VSS
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=1.85721e-11
+ PERIM=1.7566e-05
XMMN0 N_OUT_MMN0_d N_A_MMN0_g N_GND!_MMN0_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=3.43e-13 AS=3.26e-13 PD=2.343e-06 PS=4.326e-06 NRD=0.08475
+ NRS=0.0515 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.63e-07
+ SB=6.82e-07 SD=0 PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN1 N_OUT_MMN0_d N_B_MMN1_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=3.43e-13 AS=5.58e-13 PD=2.343e-06 PS=4.558e-06 NRD=0.08675
+ NRS=0.098875 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5.66e-07
+ SB=2.79e-07 SD=0 PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP0 NET16 N_A_MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6e-08 W=4e-06
+ AD=6.86e-13 AS=6.64e-13 PD=4.343e-06 PS=8.332e-06 NRD=0.042875 NRS=0.02575 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.66e-07 SB=6.83e-07 SD=0 PANW1=0
+ PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.752e-14 PANW9=2.88e-13 PANW10=7.2e-14
XMMP1 N_OUT_MMP1_d N_B_MMP1_g NET16 N_VDD!_D0_noxref_neg PFET L=6e-08 W=4e-06
+ AD=1.12e-12 AS=6.86e-13 PD=8.56e-06 PS=4.343e-06 NRD=0.04975 NRS=0.042875 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5.69e-07 SB=2.8e-07 SD=0 PANW1=0
+ PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.752e-14 PANW9=4.8e-14 PANW10=4.84e-13
*
.include "NOR_2.pex.netlist.NOR_2.pxi"
*
.ends
*
*
```

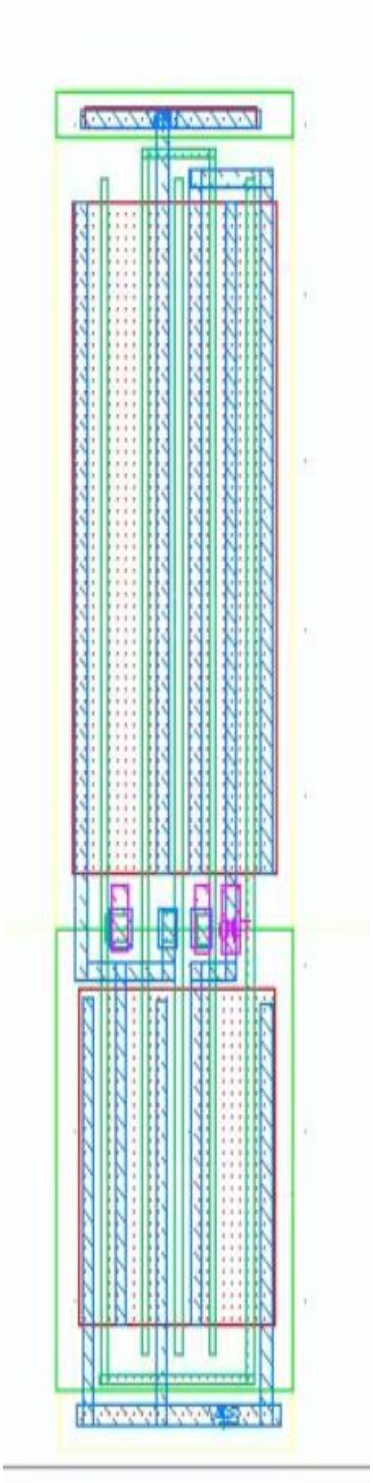
XOR2

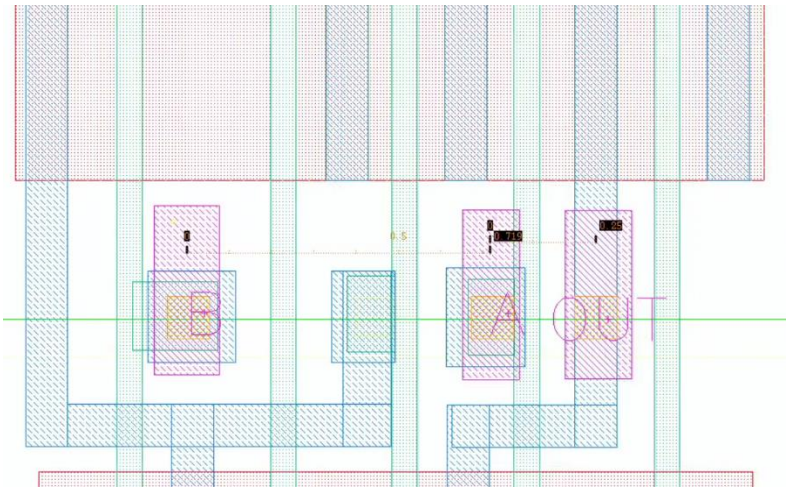
Dimensions of cell:

Height – 7.605 um

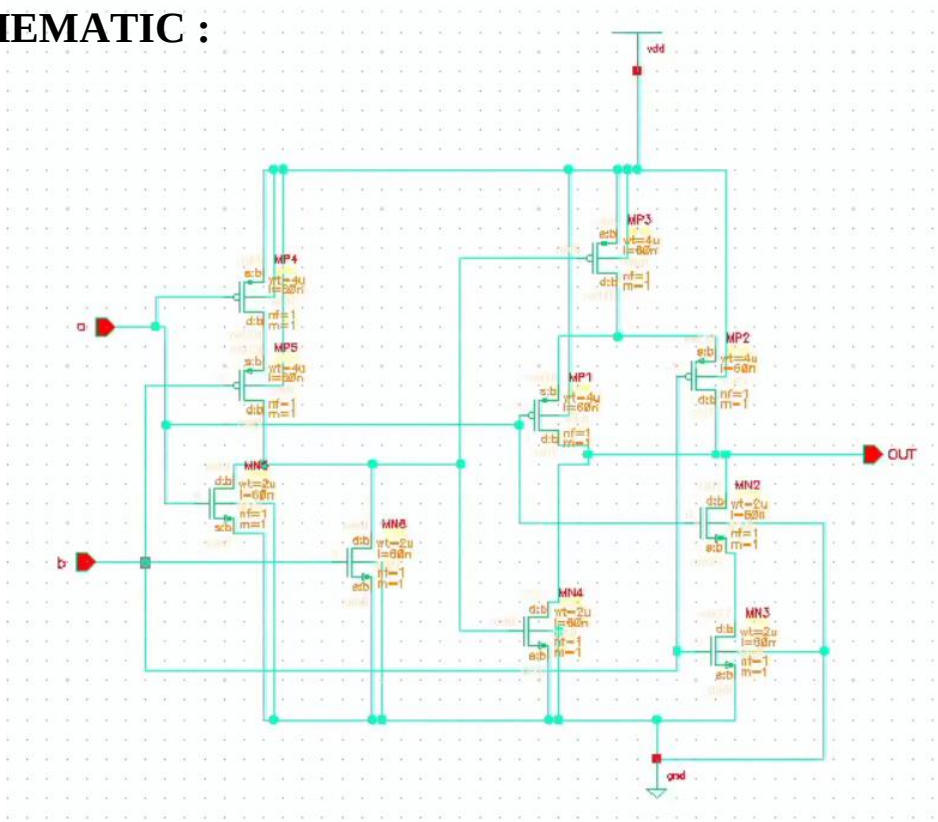
Width – 2.038 um

- **LAYOUT :**





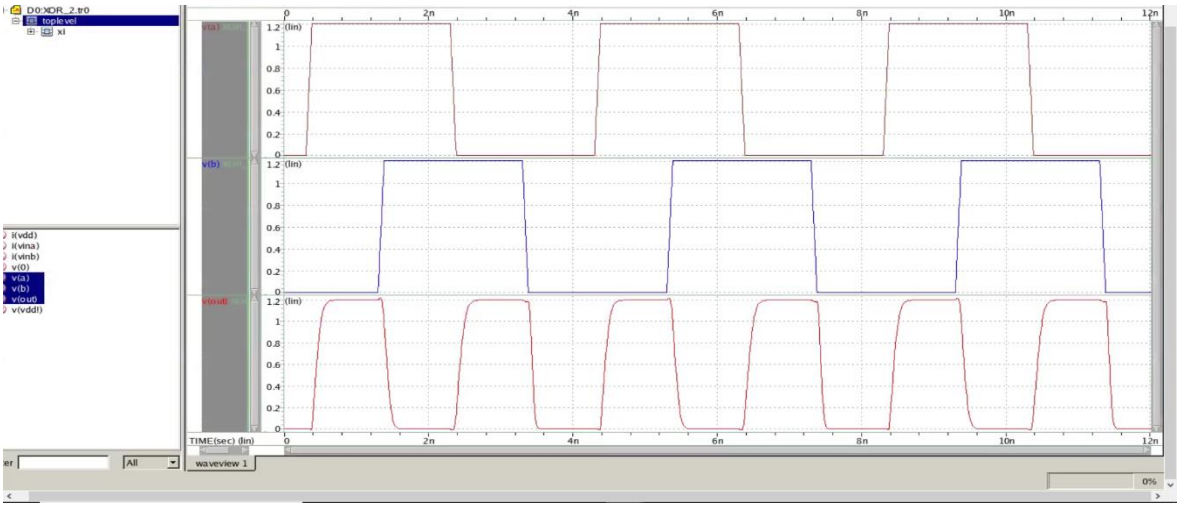
- **SCHEMATIC :**



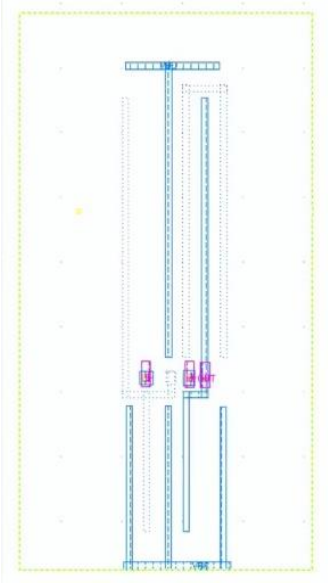
- **TRUTH TABLE**

INPUT A	INPUT B	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

- **WAVEFORM**



- **ABSTRACT :**



- **NETLIST :**

NoMachine - VLSI_DESIGN

Activities File Viewer -

File Edit Options Windows

```
* File: XOR_2.pex.netlist
* Created: Fri Oct 22 01:32:51 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "XOR_2.pex.netlist.pex"
.subckt XOR_2  GND! OUT VDD! B A
*
* A   A
* B   B
* VDD VDD
* OUT OUT
* VSS VSS
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=2.73896e-11
+ PERIM=2.0996e-05
XMMN6 N_NET9_MMN6_d N_B_MMN6_g N_GND!_MMN6_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=3.04e-13 AS=3.72e-13 PD=2.304e-06 PS=4.372e-06 NRD=0.0585
+ NRS=0.0545 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.86e-07
+ SB=1.446e-06 SD=0 PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN5 N_NET9_MMN6_d N_A_MMN5_g N_GND!_MMN5_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=3.04e-13 AS=2.26e-13 PD=2.304e-06 PS=2.226e-06 NRD=0.0935
+ NRS=0.0525 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5.5e-07
+ SB=1.082e-06 SD=0 PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN4 N_OUT_MMN4_d N_NET9_MMN4_g N_GND!_MMN5_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=2.3e-13 AS=2.26e-13 PD=2.23e-06 PS=2.226e-06 NRD=0.0605 NRS=0.0605
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=8.36e-07 SB=7.96e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN2 N_OUT_MMN4_d N_A_MMN2_g NET27 N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=2.3e-13 AS=2.72e-13 PD=2.23e-06 PS=2.272e-06 NRD=0.0545 NRS=0.068 M=1 NF=1
+ CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.126e-06 SB=5.06e-07 SD=0 PANW1=0
+ PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN3 NET27 N_B_MMN3_g N_GND!_MMN3_s N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=2.72e-13 AS=3.48e-13 PD=2.272e-06 PS=4.348e-06 NRD=0.068 NRS=0.0548333 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.458e-06 SB=1.74e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP5 N_NET9_MMP5_d N_B_MMP5_g NET28 N_VDD!_D0_noxref_neg PFET L=6e-08 W=4e-06
+ AD=9.68e-13 AS=6.08e-13 PD=8.484e-06 PS=4.304e-06 NRD=0.04175 NRS=0.038 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=2.42e-07 SB=1.472e-06 SD=0
+ PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.856e-14 PANW10=3.12e-13
XMMP4 NET28 N_A_MMP4_g N_VDD!_MMP4_s N_VDD!_D0_noxref_neg PFET L=6e-08 W=4e-06
+ AD=6.08e-13 AS=4.52e-13 PD=4.304e-06 PS=4.226e-06 NRD=0.038 NRS=0.0295 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=6.06e-07 SB=1.108e-06 SD=0
+ PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.856e-14 PANW10=7.2e-14
XMMP3 N_NET16_MMP3_d N_NET9_MMP3_g N_VDD!_MMP4_s N_VDD!_D0_noxref_neg PFET
```

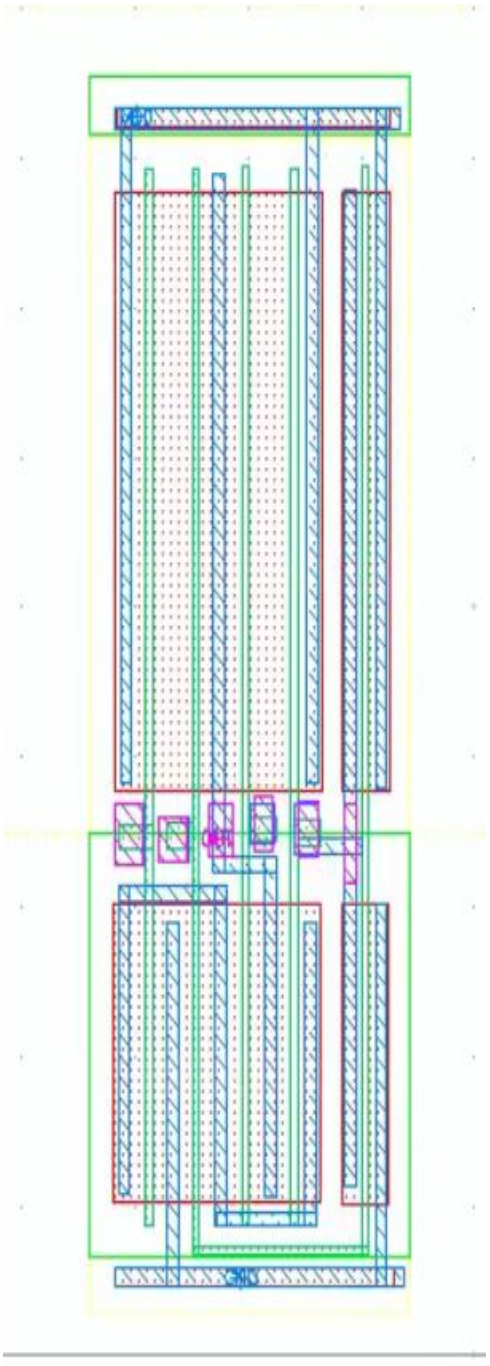
MUX 2:1

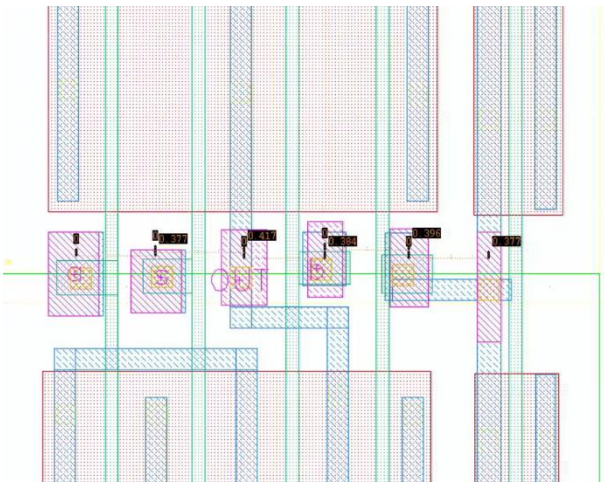
Dimensions of cell:

Height – 7.605 um

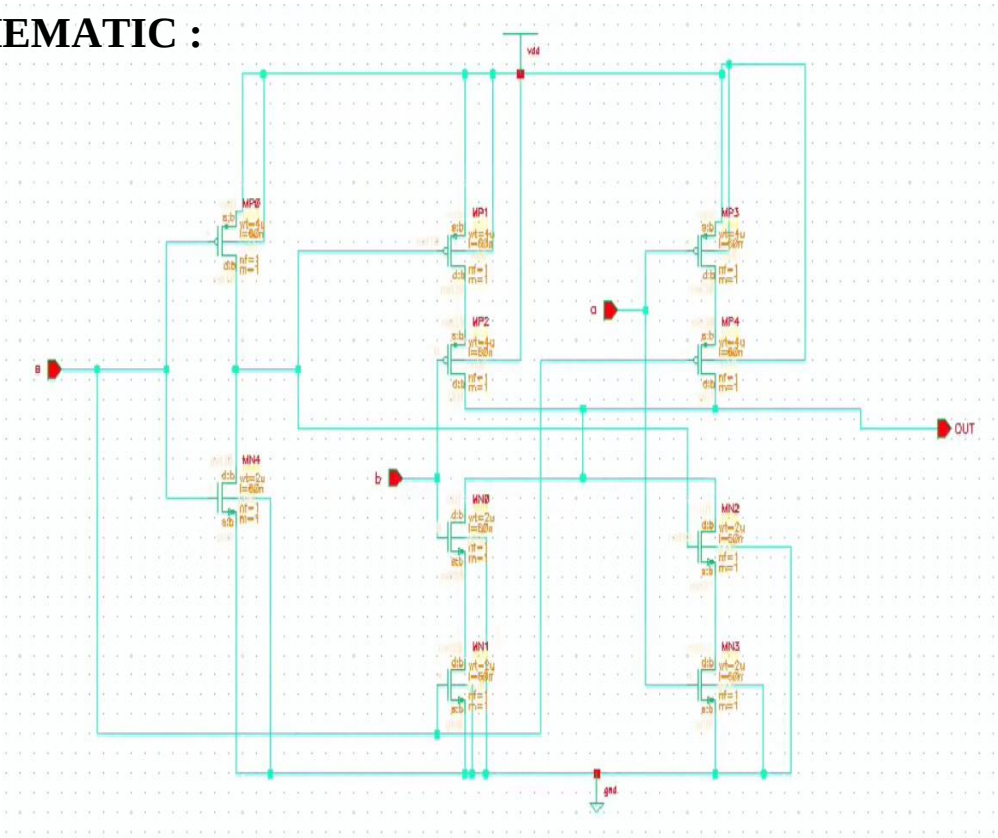
Width – 2.834 um

- **LAYOUT :**





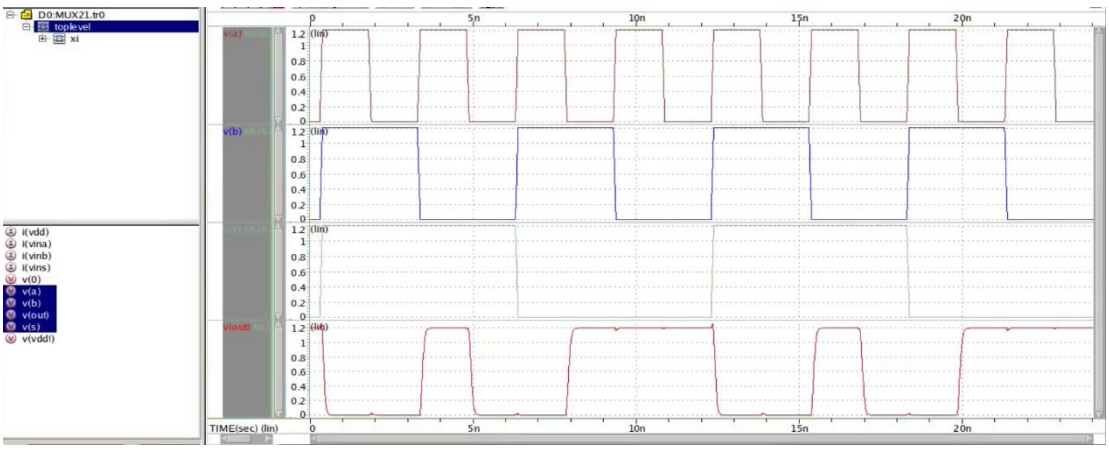
- **SCHEMATIC :**



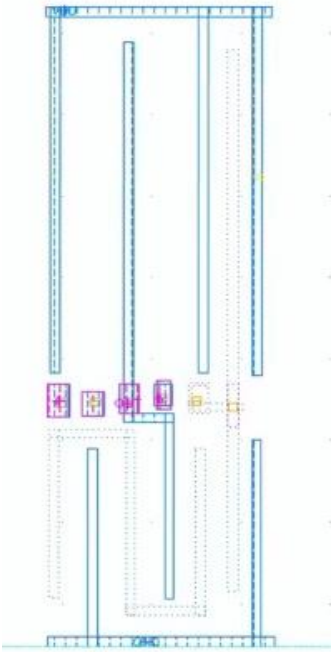
- **TRUTH TABLE**

INPUT A	INPUT B	SELECT	OUTPUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1

- **WAVEFORM**



- **ABSTRACT**



- **NETLIST :**

NoMachine - VLSI_DESIGN

Activities PEX Netlist File - MUX21.pex.netlist

File Edit Options Windows

```
* File: MUX21.pex.netlist
* Created: Fri Oct 22 02:29:18 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "MUX21.pex.netlist.pex"
.subckt MUX21  GND! OUT VDD! A S B
*
* B   B
* S   S
* A   A
* VDD VDD
* OUT OUT
* GND GND
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=4.79118e-11
+ PERIM=2.8412e-05
XMMN3 N_NET27_MMN3_d N_A_MMN3_g N_GND!_MMN3_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=5.88e-13 AS=3.51e-13 PD=4.588e-06 PS=2.351e-06 NRD=0.0953333
+ NRS=0.0906667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=2.94e-07
+ SB=1.477e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=2.28e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN1 NET28 N_S_MMN1_g N_GND!_MMN3_s N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=3.82e-13 AS=3.51e-13 PD=2.382e-06 PS=2.351e-06 NRD=0.0955 NRS=0.0848333 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=7.05e-07 SB=1.066e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=2.28e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN0 N_OUT_MMN0_d N_B_MMN0_g NET28 N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=3.67e-13 AS=3.82e-13 PD=2.367e-06 PS=2.382e-06 NRD=0.0925 NRS=0.0955 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.147e-06 SB=6.24e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=2.28e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN2 N_OUT_MMN0_d N_NET10_MMN2_g N_NET27_MMN2_s N_GND!_D0_noxref_pos NFET
+ L=6e-08 W=2e-06 AD=3.67e-13 AS=3.94e-13 PD=2.367e-06 PS=4.394e-06 NRD=0.091
+ NRS=0.0561667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.574e-06
+ SB=1.97e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=2.28e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN4 N_NET10_MMN4_d N_S_MMN4_g N_GND!_MMN4_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=3.3e-13 AS=3.5e-13 PD=4.33e-06 PS=4.35e-06 NRD=0.0525 NRS=0.0555
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.65e-07 SB=1.75e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=1.62e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP3 NET30 N_A_MMP3_g N_VDD!_MMP3_s N_VDD!_D0_noxref_neg PFET L=6e-08 W=4e-06
+ AD=7.02e-13 AS=1.068e-12 PD=4.351e-06 PS=8.534e-06 NRD=0.043875 NRS=0.04375
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=2.67e-07 SB=1.508e-06 SD=0
+ PANW1=5.4e-16 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=3.492e-14 PANW10=7.2e-14
```

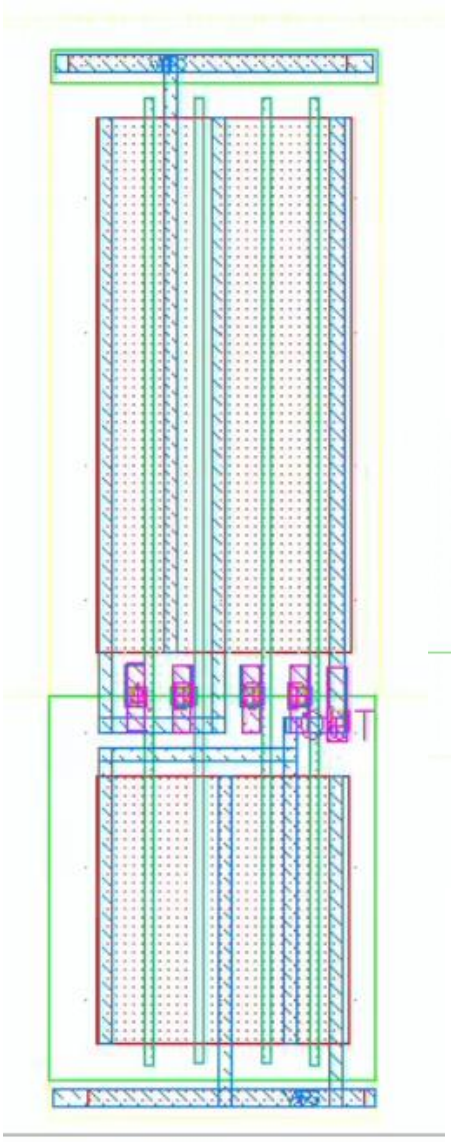
AOI211

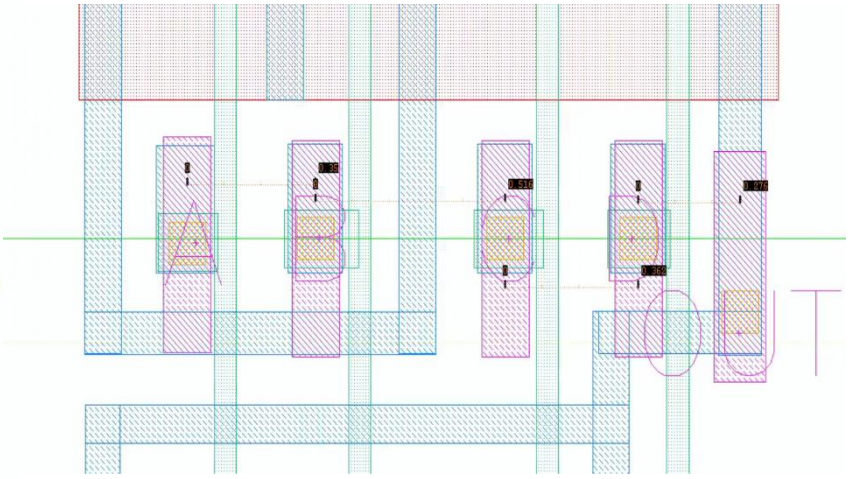
Dimensions of cell:

Height – 7.605 um

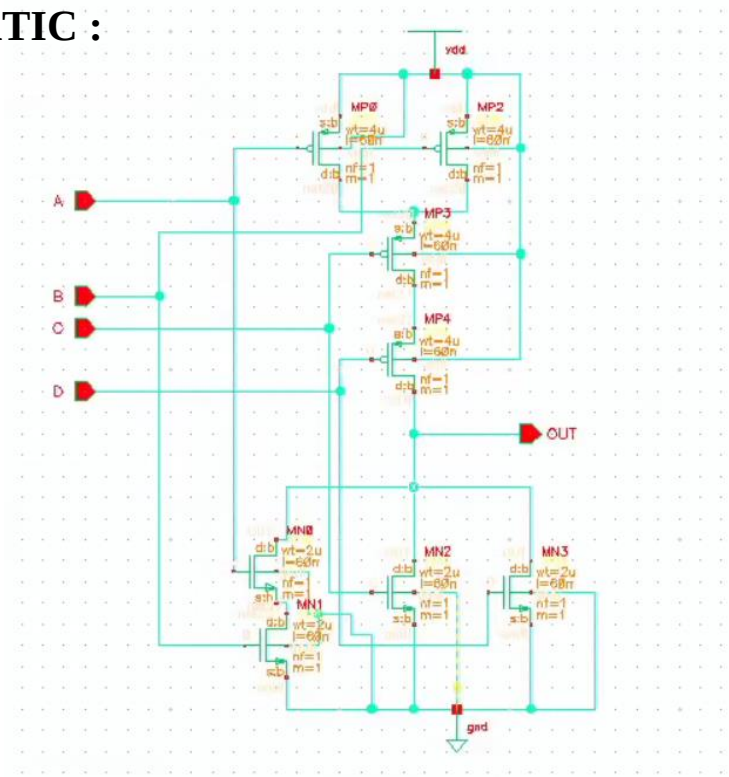
Width – 2.44 um

- **LAYOUT :**





- **SCHEMATIC :**

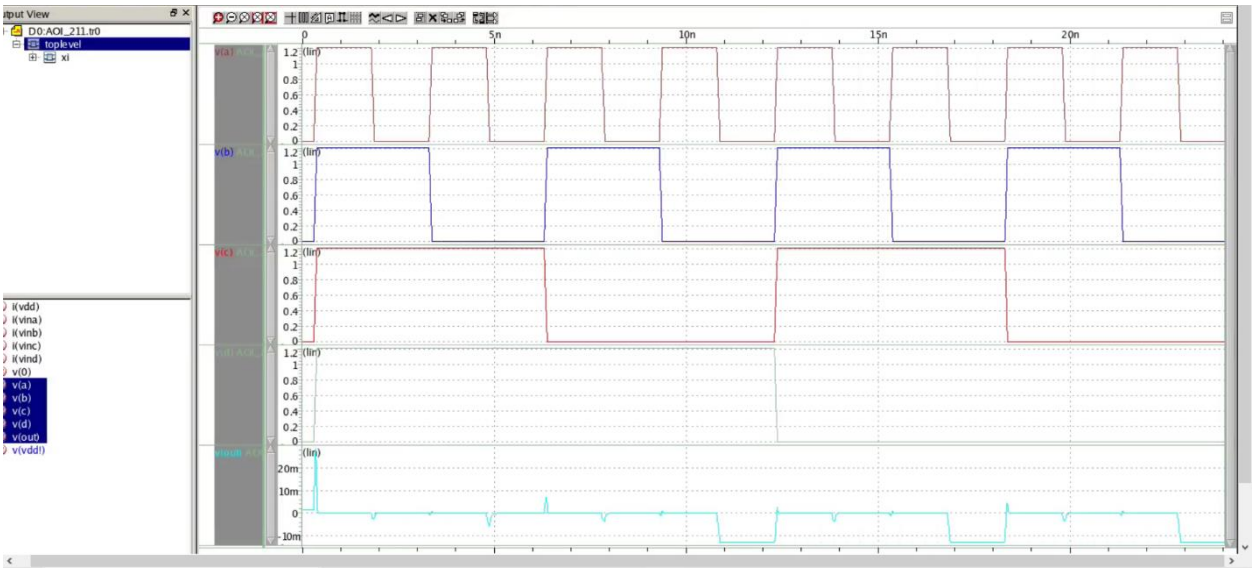


- **TRUTH TABLE**

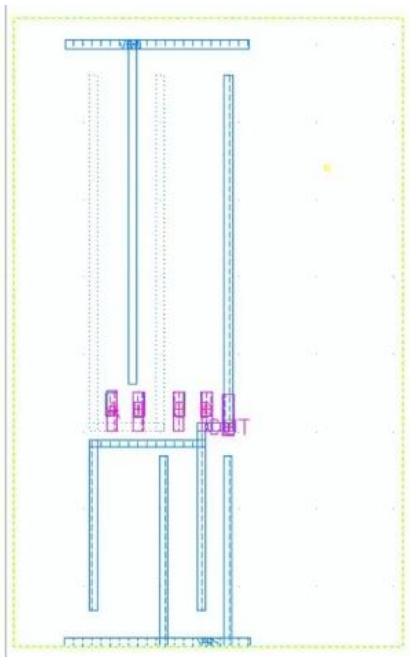
INPUT A	INPUT B	INPUT C	INPUT D	OUTPUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0

1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**0**
1	**1**	**1**	**1**	**0**

- **WAVEFORM**



- **ABSTRACT**



- **NETLIST :**

NoMachine - VLSI_DESIGN

Activities File Viewer -

File Edit Options Windows

```
* File: AOI_211.pex.netlist
* Created: Fri Oct 22 00:00:27 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "AOI_211.pex.netlist.pex"
.subckt AOI_211  OUT GND! VDD! A B C D
*
* D   D
* C   C
* B   B
* A   A
* VDD VDD
* VSS VSS
* OUT OUT
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=2.534e-11
+ PERIM=2.0136e-05
XMMN0 N_OUT_MMN0_d N_A_MMN0_g NET22 N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=7.26e-13 AS=3.07e-13 PD=4.726e-06 PS=2.307e-06 NRD=0.1515 NRS=0.07675 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=3.63e-07 SB=1.46e-06 SD=0 PANW1=0
+ PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=6e-17 PANW7=1.2e-14 PANW8=1.2e-14
+ PANW9=2.4e-14 PANW10=3.6e-14
XMMN1 NET22 N_B_MMN1_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=3.07e-13 AS=4.49e-13 PD=2.307e-06 PS=2.449e-06 NRD=0.07675 NRS=0.0855 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=7.3e-07 SB=1.093e-06 SD=0 PANW1=0
+ PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=6e-17 PANW7=1.2e-14 PANW8=1.2e-14
+ PANW9=2.4e-14 PANW10=3.6e-14
XMMN2 N_OUT_MMN2_d N_C_MMN2_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=2.96e-13 AS=4.49e-13 PD=2.296e-06 PS=2.449e-06 NRD=0.072 NRS=0.139
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.239e-06 SB=5.84e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=6e-17 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN3 N_OUT_MMN2_d N_D_MMN3_g N_GND!_MMN3_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=2.96e-13 AS=4.56e-13 PD=2.296e-06 PS=4.456e-06 NRD=0.076 NRS=0.0685
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.595e-06 SB=2.28e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=6e-17 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP0 N_NET20_MMP0_d N_A_MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=1.464e-12 AS=6.14e-13 PD=8.732e-06 PS=4.307e-06 NRD=0.07575
+ NRS=0.0335 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=3.66e-07
+ SB=1.475e-06 SD=0 PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.56e-14 PANW8=2.4e-14 PANW9=2.88e-13 PANW10=7.2e-14
XMMP2 N_NET20_MMP2_d N_B_MMP2_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=8.98e-13 AS=6.14e-13 PD=4.449e-06 PS=4.307e-06 NRD=0.03205
+ NRS=0.04325 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=7.33e-07
+ SB=1.108e-06 SD=0 PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.56e-14 PANW8=2.4e-14 PANW9=4.8e-14 PANW10=3.12e-13
XMMP3 NET27 N_C_MMP3_g N_NET20_MMP2_d N_VDD!_D0_noxref_neg PFET L=6e-08 W=4e-06
+ AD=5.92e-13 AS=8.98e-13 PD=4.296e-06 PS=4.449e-06 NRD=0.037 NRS=0.0802 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.242e-06 SB=5.99e-07 SD=0
+ PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
```

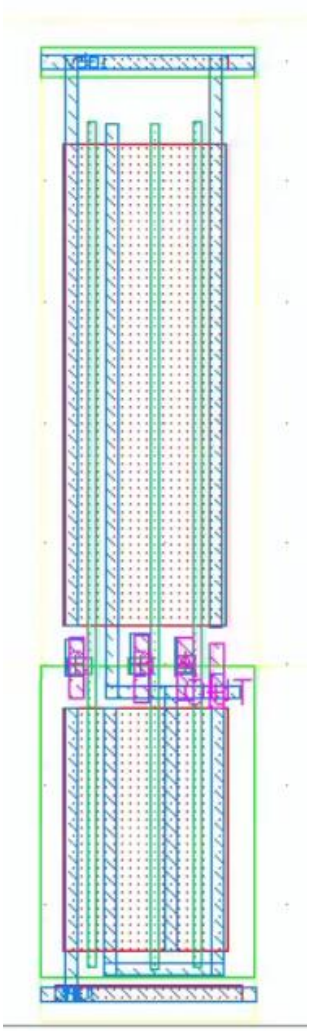
OAI21

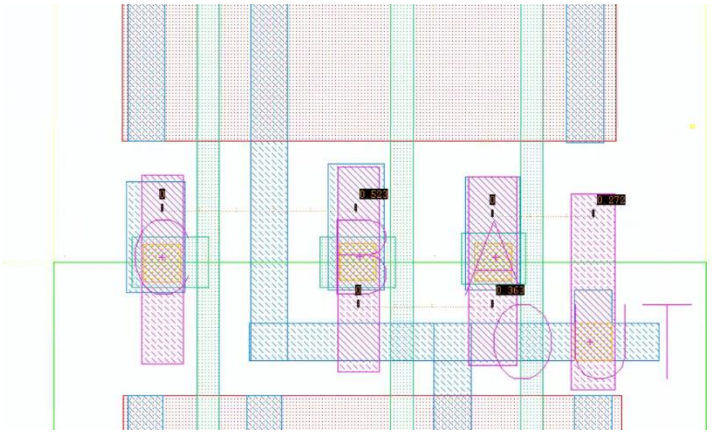
Dimensions of cell:

Height – 7.605 um

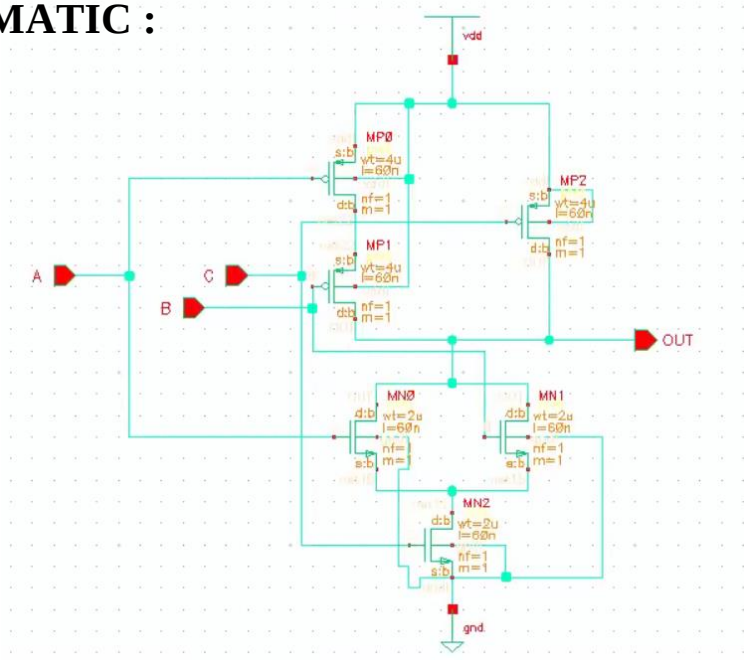
Width – 1.763 um

- **LAYOUT :**





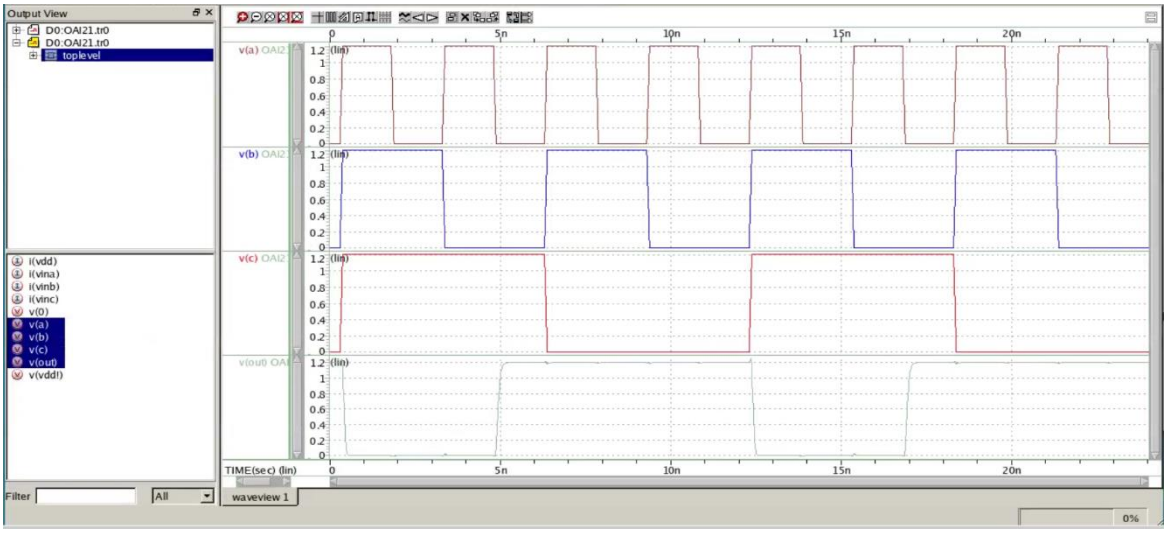
- **SCHEMATIC :**



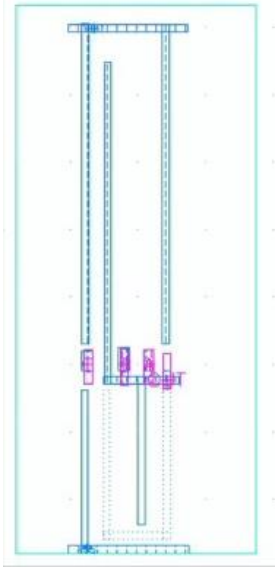
- **TRUTH TABLE :**

Input A	Input B	Input C	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

- **WAVEFORM**



- **ABSTRACT :**



- **NETLIST :**

NoMachine - VLSI_DESIGN

Activities File Viewer -

File Edit Options Windows

```
* File: OAI21.pex.netlist
* Created: Fri Oct 22 01:16:39 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "OAI21.pex.netlist.pex"
.subckt OAI21  GND! OUT VDD! C B A
*
* A   A
* B   B
* C   C
* VDD! VDD!
* OUT OUT
* GND! GND!
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=1.89374e-11
+ PERIM=1.7772e-05
XMMN2 N_NET15_MMN2_d N_C_MMN2_g N_GND!_MMN2_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=4.64e-13 AS=3.98e-13 PD=2.464e-06 PS=4.398e-06 NRD=0.061 NRS=0.0695
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.99e-07 SB=1.088e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN1 N_OUT_MMN1_d N_B_MMN1_g N_NET15_MMN2_d N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=2.9e-13 AS=4.64e-13 PD=2.29e-06 PS=2.464e-06 NRD=0.0545 NRS=0.171
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=7.23e-07 SB=5.64e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN0 N_OUT_MMN1_d N_A_MMN0_g N_NET15_MMN0_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=2.9e-13 AS=4.28e-13 PD=2.29e-06 PS=4.428e-06 NRD=0.0905
+ NRS=0.068375 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.073e-06
+ SB=2.14e-07 SD=0 PANW1=0 PANW2=0 PANW3=2.4e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP2 N_OUT_MMP2_d N_C_MMP2_g N_VDD!_MMP2_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=9.28e-13 AS=8.08e-13 PD=4.464e-06 PS=8.404e-06 NRD=0.0337
+ NRS=0.03475 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=2.02e-07
+ SB=1.072e-06 SD=0 PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.8734e-13 PANW10=7.2e-14
XMMP1 N_OUT_MMP2_d N_B_MMP1_g NET22 N_VDD!_D0_noxref_neg PFET L=6e-08 W=4e-06
+ AD=9.28e-13 AS=5.8e-13 PD=4.464e-06 PS=4.29e-06 NRD=0.0823 NRS=0.03625 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=7.26e-07 SB=5.48e-07 SD=0 PANW1=0
+ PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=4.734e-14 PANW10=5.52e-13
XMMP0 NET22 N_A_MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6e-08 W=4e-06
+ AD=5.8e-13 AS=7.92e-13 PD=4.29e-06 PS=8.396e-06 NRD=0.03625 NRS=0.02885 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.076e-06 SB=1.98e-07 SD=0
+ PANW1=0 PANW2=1.32e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=4.734e-14 PANW10=3.12e-13
*
.include "OAI21.pex.netlist.OAI21.pxi"
*
.ends
*
```

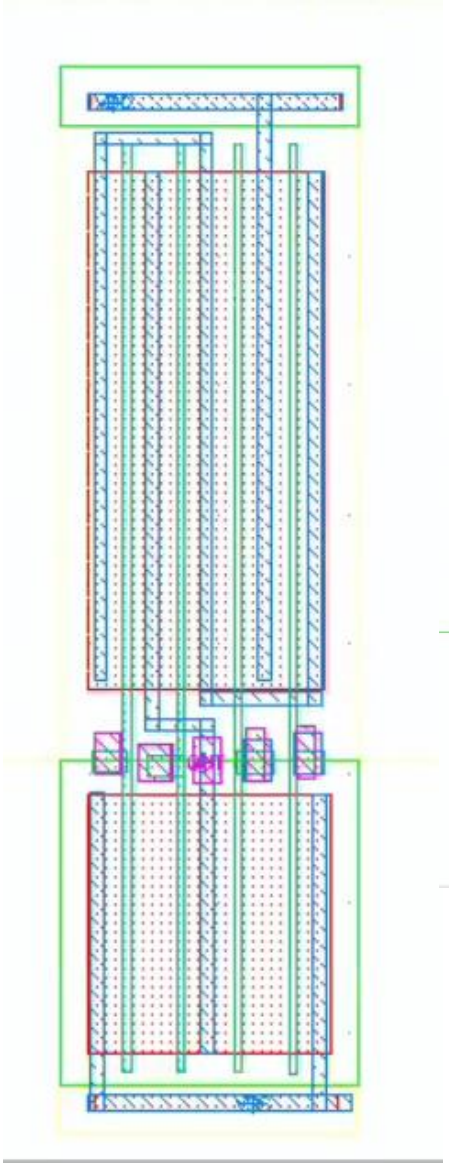
AOI22

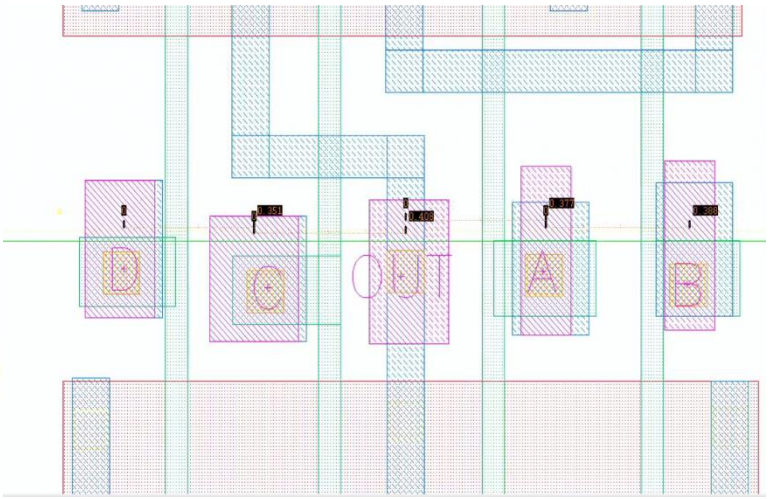
Dimensions of cell:

Height – 7.605 um

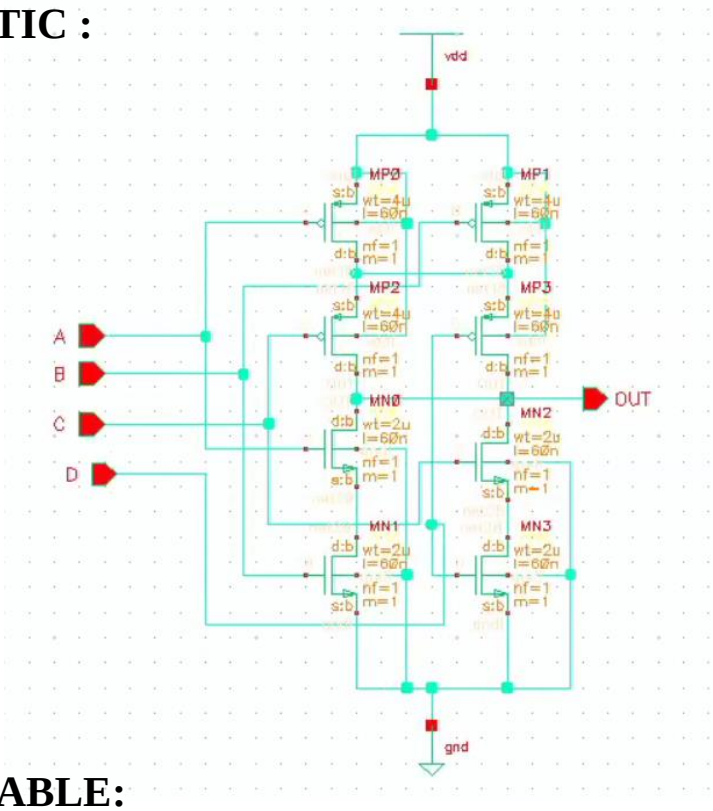
Width – 2.302 um

- **LAYOUT :**





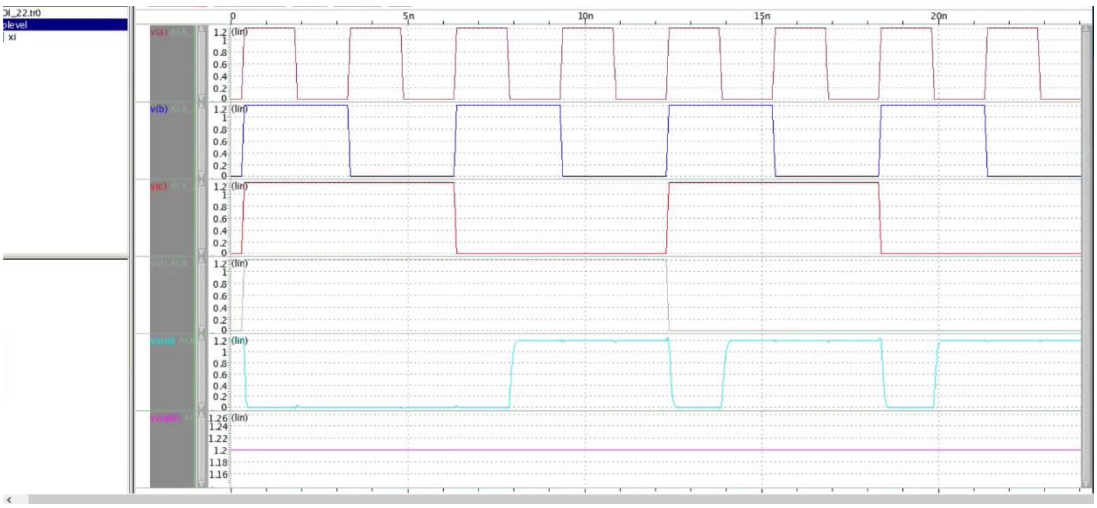
- **SCHEMATIC :**



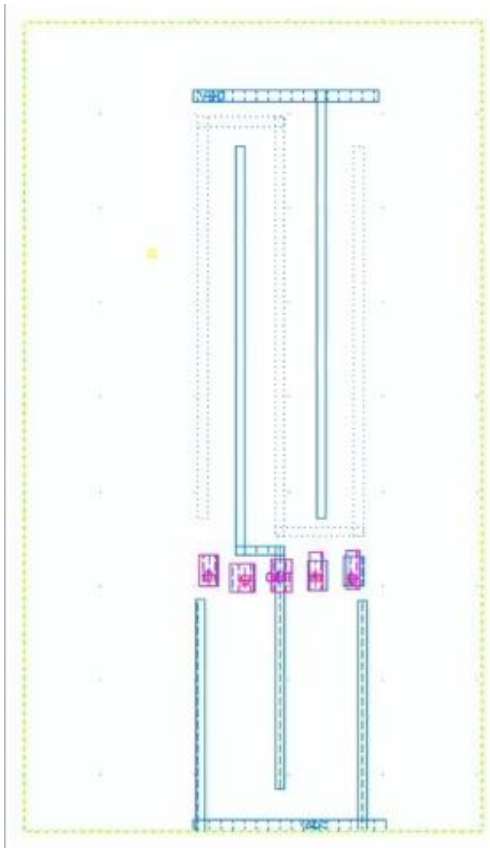
- **TRUTH TABLE:**

Input A	Input B	Input C	Input D	Output
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

- **WAVEFORM**



- **ABSTRACT**



- **NETLIST :**

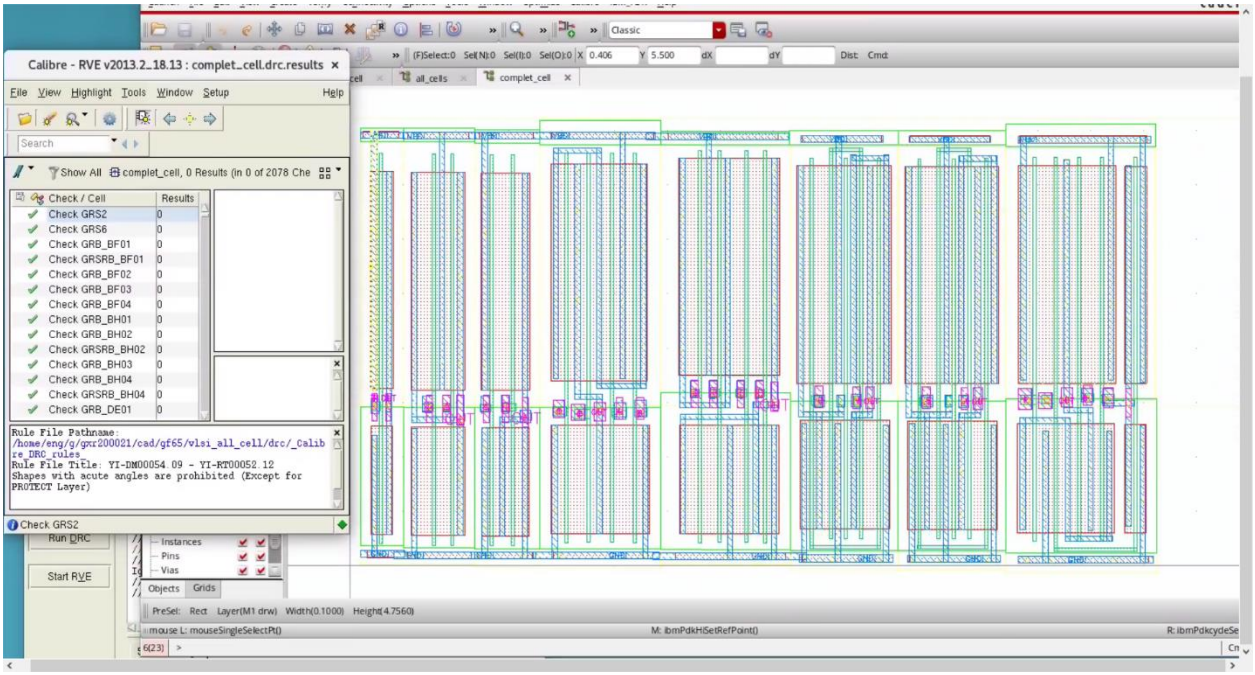
NoMachine - VLSI_DESIGN

Activities File Viewer -

File Edit Options Windows

```
* File: AOI_22.pex.netlist
* Created: Fri Oct 22 00:11:44 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "AOI_22.pex.netlist.pex"
.subckt AOI_22  GND! OUT VDD! D C A B
*
* B   B
* A   A
* C   C
* D   D
* VDD VDD
* OUT OUT
* VSS VSS
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=2.84606e-11
+ PERIM=2.1438e-05
XMMN3 NET28 N_D_MMN3_g N_GND!_MMN3_s N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=3.51e-13 AS=5.5e-13 PD=2.351e-06 PS=4.55e-06 NRD=0.08775 NRS=0.101 M=1 NF=1
+ CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=2.75e-07 SB=1.535e-06 SD=0
+ PANW1=2.76e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN2 N_OUT_MMN2_d N_C_MMN2_g NET28 N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=3.82e-13 AS=3.51e-13 PD=2.382e-06 PS=2.351e-06 NRD=0.0871667 NRS=0.08775
+ M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=0 SA=6.86e-07 SB=1.124e-06 SD=0
+ PANW1=2.76e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN0 N_OUT_MMN2_d N_A_MMN0_g NET29 N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=3.82e-13 AS=3.67e-13 PD=2.382e-06 PS=2.367e-06 NRD=0.103833 NRS=0.09175 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.128e-06 SB=6.82e-07 SD=0
+ PANW1=2.76e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN1 NET29 N_B_MMN1_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=3.67e-13 AS=5.1e-13 PD=2.367e-06 PS=4.51e-06 NRD=0.09175 NRS=0.0893333 M=1
+ NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.555e-06 SB=2.55e-07 SD=0
+ PANW1=2.76e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP3 N_OUT_MMP3_d N_D_MMP3_g N_NET15_MMP3_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=7.02e-13 AS=1.1e-12 PD=4.351e-06 PS=8.55e-06 NRD=0.0423 NRS=0.04375
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=2.75e-07 SB=1.492e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=2.34e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.928e-14 PANW10=7.2e-14
XMMP2 N_OUT_MMP3_d N_C_MMP2_g N_NET15_MMP2_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=7.02e-13 AS=7.64e-13 PD=4.351e-06 PS=4.382e-06 NRD=0.04545
+ NRS=0.0427 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=6.86e-07
+ SB=1.081e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=2.34e-15
+ PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.928e-14 PANW10=7.2e-14
XMMP0 N_NET15_MMP2_s N_A_MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=4e-06 AD=7.64e-13 AS=7.34e-13 PD=4.382e-06 PS=4.367e-06 NRD=0.0528
+ NRS=0.04295 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.128e-06
+ SB=6.39e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=2.34e-15
```

COMBINED LAYOUT



RESULT:

There were no DRC errors in the Combined Layout.