UNIVERSITY OF TEXAS AT DALLAS

800 W Campbell Rd, Richardson, TX 75080, USA

VLSI DESIGN (EECT 6325)

PROJECT DONE ON:

STANDARD CELL LIBRARY

(Final Project: Layout & Verification)

Team Members:

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ACKNOWLEDGEMENT

We are grateful to Professor CARL SECHEN for providing us an opportunity to explore and conduct Flip-Flop based projects in VLSI Design.

We also take this opportunity to express our gratitude to MR VAIBHAV KUMARSWAMY SALIMATH for his guidance in conducting the project.

OBJECTIVE

In this project, we used our Verilog code from project 2 and laid it out using the calls that we generated in our cell library.

Project Goals:

1) Automatic placement and routing of your design using Cadence's Innovus

2) Run DRC (design rule checker) and LVS (layout versus schematic)

3) Run PrimeTime on the final layout using the extracted netlist to ascertain the worst-case delay

DESIGN PROCESS

Project 1:

Coded our Digital Design in Behavioural Verilog. We Created a Test bench for our Design.

Project 2:

Based on the library cells, Synopsys Design Vision was used to produce a Mapped netlist. We gained a deeper understanding of the complexity of our design as well as a precise cell count during this project.

Project 3:

Using the help of Virtuoso Design tools, we designed a layout for an Inverter. We got a better understanding of the tools.

Project 4:

With the Understanding of the Virtuoso tools, we created a standard library of cells which will be used for our final design. The Cells which we laid out are INV, NAND2, NOR2, XOR2, MUX2:1, AOI211, OAI21, AOI22.

- Schematic was created for all the Cells.
- DRC - Design Rule Checking (DRC) is a physical design process to determine if chip layout satisfies a number of rules as defined by the semiconductor manufacturer.
- LVS - The Layout Versus Schematic is the class of electronic design automation verification software that determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design.
- **All the cells passed DRC and LVS** .
- **Height of all cells – 9.62 um**
- Abstract views were generated for all the cells and also obtained the spice files for all the cells.
- Using the extracted netlist, the functionality of each cell is checked by simulating in spice and Waveview.

Project 5:

Using the Cadence Design tools to design, D-Flip-Flop layout was designed.

Project 6:

We used the cells that we developed in our cell library to lay out the Verilog code that we used in project 2 during this Final Design.

We used Cadence Innovus in this Final Project to assist us automatically position cells in the design. Following that, we looked for DRC and LVS. We also used an extracted netlist to run the PrimeTime (a Synopsys Static Timing Analysis(STA) tool) on our final layout to determine the worst-case latency.

NETLIST FILE GENERATED

```
endmodule

module D_ff( D, CLK, R, Q);
input D, CLK, R;
output Q;
reg Q;
//always @(posedge CLK or negedge R)
  //if (R == 1'b0)
    //Q = 1'b0;
  //else
    //Q = D;
endmodule
module FIFO_1 ( clk, rst, re, we, data_in, emp, full, data_out );
  input [31:0] data_in;
  output [31:0] data_out;
  input clk, rst, re, we;
  output emp, full;
  wire   N0, N1, N2, N3, N5, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16,
         N17, N18, N19, N20, N21, N22, N23, N24, N25, N26, N27, N28, N29, N30,
         N31, N32, N33, N34, N35, N36, N37, N38, N39, N40, N41, N42, N43, N44,
         N45, N46, N47, N48, N49, N50, N51, N52, N53, N54, N55, N56, N57, N58,
         N59, N60, N61, N62, N63, N64, N65, N66, N67, N104, N105, N106, N107,
         N712, N713, N714, N715, N716, N717, N718, N719, N720, N721, N722,
         N723, N724, N725, N726, N727, N728, N729, N730, N731, N732, N733,
         N734, N735, N736, N737, N738, N739, N740, N741, N742, N743, N744,
         \mem[15][31] , \mem[15][30] , \mem[15][29] , \mem[15][28] ,
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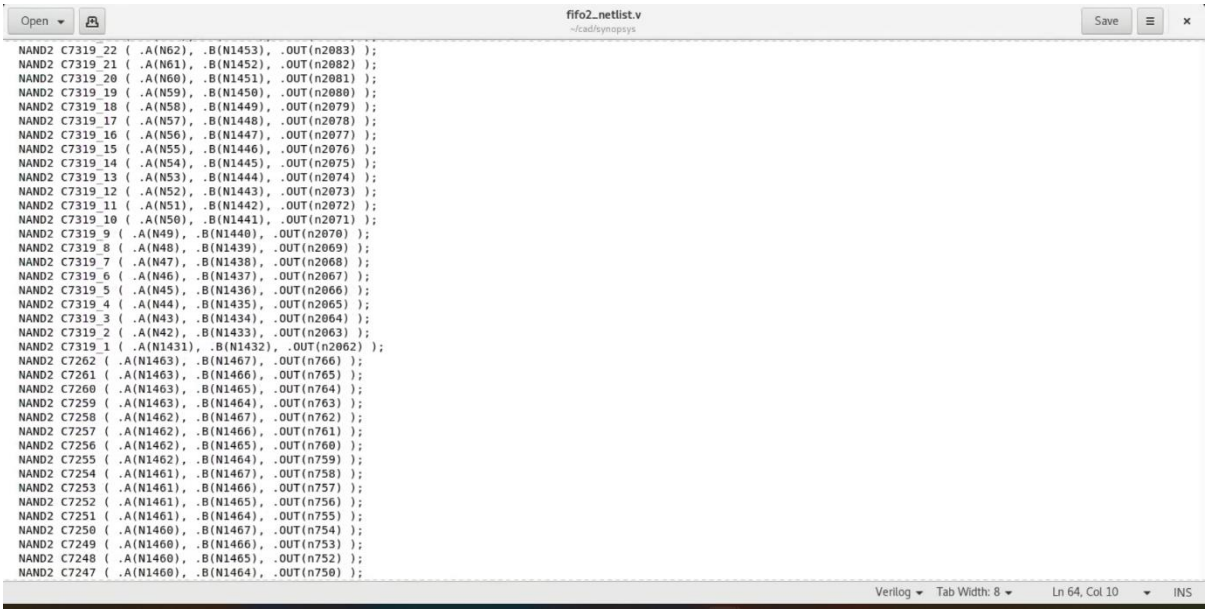
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NAND2 C7319_22 (.A(N62), .B(N1453), .OUT(n2083));
NAND2 C7319_21 (.A(N61), .B(N1452), .OUT(n2082));
NAND2 C7319_20 (.A(N60), .B(N1451), .OUT(n2081));
NAND2 C7319_19 (.A(N59), .B(N1450), .OUT(n2080));
NAND2 C7319_18 (.A(N58), .B(N1449), .OUT(n2079));
NAND2 C7319_17 (.A(N57), .B(N1448), .OUT(n2078));
NAND2 C7319_16 (.A(N56), .B(N1447), .OUT(n2077));
NAND2 C7319_15 (.A(N55), .B(N1446), .OUT(n2076));
NAND2 C7319_14 (.A(N54), .B(N1445), .OUT(n2075));
NAND2 C7319_13 (.A(N53), .B(N1444), .OUT(n2074));
NAND2 C7319_12 (.A(N52), .B(N1443), .OUT(n2073));
NAND2 C7319_11 (.A(N51), .B(N1442), .OUT(n2072));
NAND2 C7319_10 (.A(N50), .B(N1441), .OUT(n2071));
NAND2 C7319_9 (.A(N49), .B(N1440), .OUT(n2070));
NAND2 C7319_8 (.A(N48), .B(N1439), .OUT(n2069));
NAND2 C7319_7 (.A(N47), .B(N1438), .OUT(n2068));
NAND2 C7319_6 (.A(N46), .B(N1437), .OUT(n2067));
NAND2 C7319_5 (.A(N45), .B(N1436), .OUT(n2066));
NAND2 C7319_4 (.A(N44), .B(N1435), .OUT(n2065));
NAND2 C7319_3 (.A(N43), .B(N1434), .OUT(n2064));
NAND2 C7319_2 (.A(N42), .B(N1433), .OUT(n2063));
NAND2 C7319_1 (.A(N1431), .B(N1432), .OUT(n2062));
NAND2 C7262 (.A(N1463), .B(N1467), .OUT(n766));
NAND2 C7261 (.A(N1463), .B(N1466), .OUT(n765));
NAND2 C7260 (.A(N1463), .B(N1465), .OUT(n764));
NAND2 C7259 (.A(N1463), .B(N1464), .OUT(n763));
NAND2 C7258 (.A(N1462), .B(N1467), .OUT(n762));
NAND2 C7257 (.A(N1462), .B(N1466), .OUT(n761));
NAND2 C7256 (.A(N1462), .B(N1465), .OUT(n760));
NAND2 C7255 (.A(N1462), .B(N1464), .OUT(n759));
NAND2 C7254 (.A(N1461), .B(N1467), .OUT(n758));
NAND2 C7253 (.A(N1461), .B(N1466), .OUT(n757));
NAND2 C7252 (.A(N1461), .B(N1465), .OUT(n756));
NAND2 C7251 (.A(N1461), .B(N1464), .OUT(n755));
NAND2 C7250 (.A(N1460), .B(N1467), .OUT(n754));
NAND2 C7249 (.A(N1460), .B(N1466), .OUT(n753));
NAND2 C7248 (.A(N1460), .B(N1465), .OUT(n752));
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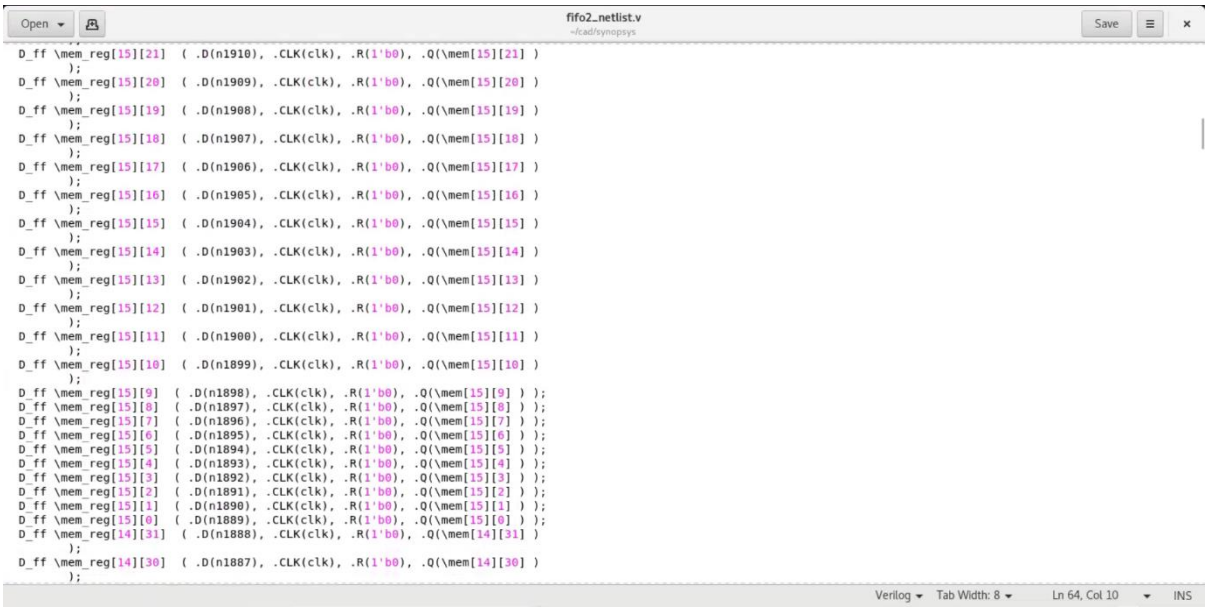
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fifo2_netlist.v
~/cad/synopsys
Save
D_ff \mem_reg[15][21] (.D(n1910), .CLK(clk), .R(1'b0), .Q(\mem[15][21])
);
D_ff \mem_reg[15][20] (.D(n1909), .CLK(clk), .R(1'b0), .Q(\mem[15][20])
);
D_ff \mem_reg[15][19] (.D(n1908), .CLK(clk), .R(1'b0), .Q(\mem[15][19])
);
D_ff \mem_reg[15][18] (.D(n1907), .CLK(clk), .R(1'b0), .Q(\mem[15][18])
);
D_ff \mem_reg[15][17] (.D(n1906), .CLK(clk), .R(1'b0), .Q(\mem[15][17])
);
D_ff \mem_reg[15][16] (.D(n1905), .CLK(clk), .R(1'b0), .Q(\mem[15][16])
);
D_ff \mem_reg[15][15] (.D(n1904), .CLK(clk), .R(1'b0), .Q(\mem[15][15])
);
D_ff \mem_reg[15][14] (.D(n1903), .CLK(clk), .R(1'b0), .Q(\mem[15][14])
);
D_ff \mem_reg[15][13] (.D(n1902), .CLK(clk), .R(1'b0), .Q(\mem[15][13])
);
D_ff \mem_reg[15][12] (.D(n1901), .CLK(clk), .R(1'b0), .Q(\mem[15][12])
);
D_ff \mem_reg[15][11] (.D(n1900), .CLK(clk), .R(1'b0), .Q(\mem[15][11])
);
D_ff \mem_reg[15][10] (.D(n1899), .CLK(clk), .R(1'b0), .Q(\mem[15][10])
);
D_ff \mem_reg[15][9] (.D(n1898), .CLK(clk), .R(1'b0), .Q(\mem[15][9]));
D_ff \mem_reg[15][8] (.D(n1897), .CLK(clk), .R(1'b0), .Q(\mem[15][8]));
D_ff \mem_reg[15][7] (.D(n1896), .CLK(clk), .R(1'b0), .Q(\mem[15][7]));
D_ff \mem_reg[15][6] (.D(n1895), .CLK(clk), .R(1'b0), .Q(\mem[15][6]));
D_ff \mem_reg[15][5] (.D(n1894), .CLK(clk), .R(1'b0), .Q(\mem[15][5]));
D_ff \mem_reg[15][4] (.D(n1893), .CLK(clk), .R(1'b0), .Q(\mem[15][4]));
D_ff \mem_reg[15][3] (.D(n1892), .CLK(clk), .R(1'b0), .Q(\mem[15][3]));
D_ff \mem_reg[15][2] (.D(n1891), .CLK(clk), .R(1'b0), .Q(\mem[15][2]));
D_ff \mem_reg[15][1] (.D(n1890), .CLK(clk), .R(1'b0), .Q(\mem[15][1]));
D_ff \mem_reg[15][0] (.D(n1889), .CLK(clk), .R(1'b0), .Q(\mem[15][0]));
D_ff \mem_reg[14][31] (.D(n1888), .CLK(clk), .R(1'b0), .Q(\mem[14][31])
);
D_ff \mem_reg[14][30] (.D(n1887), .CLK(clk), .R(1'b0), .Q(\mem[14][30])
);
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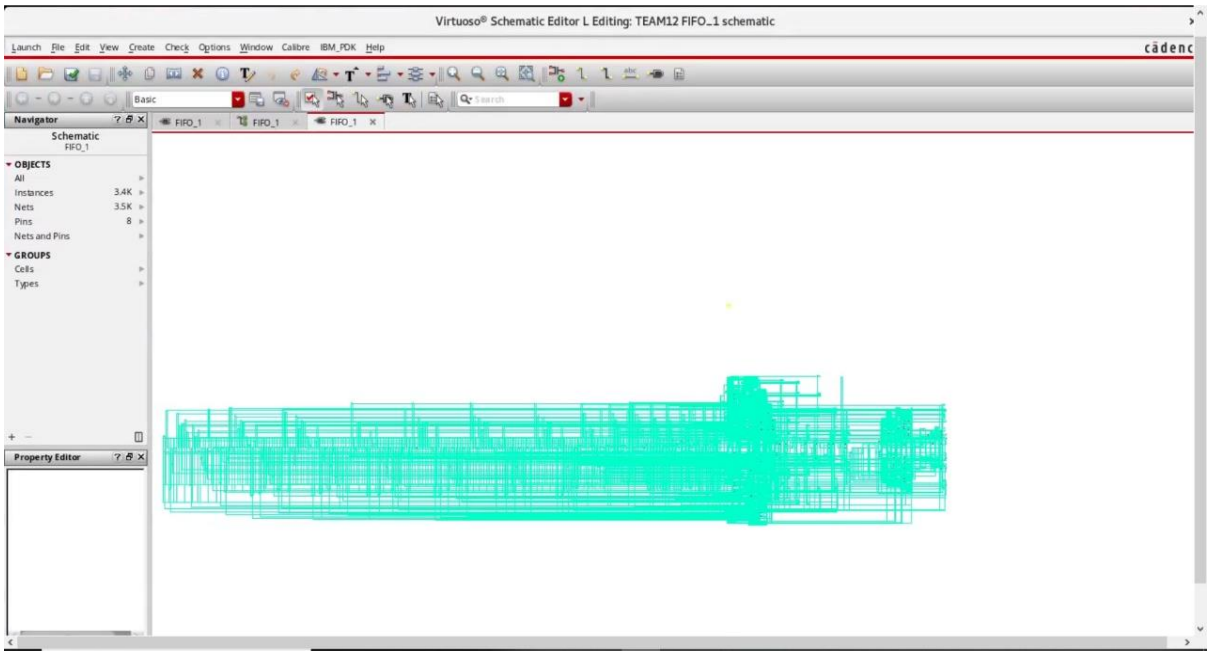
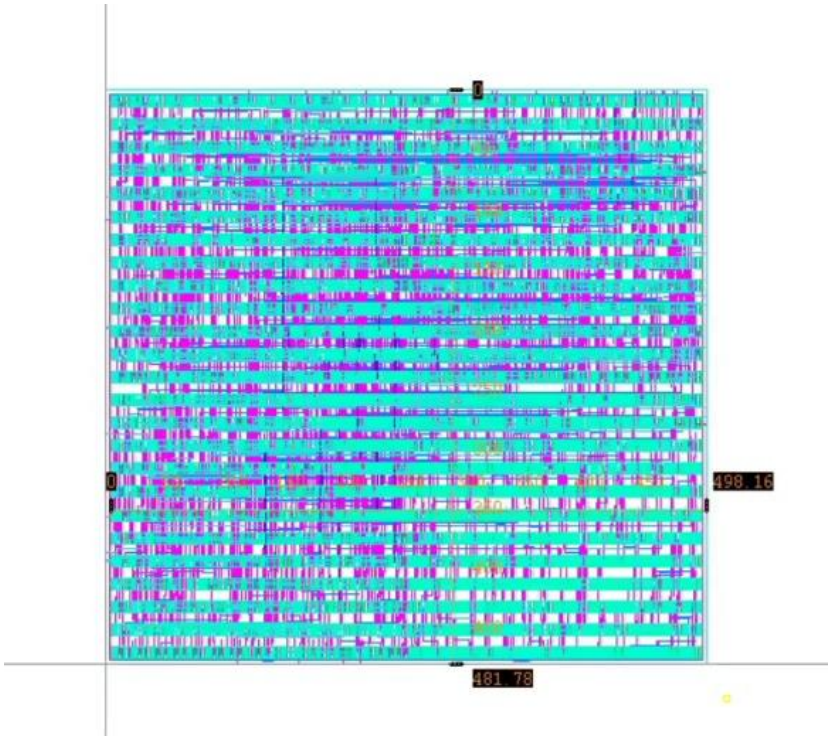
FINAL SCHEMATIC



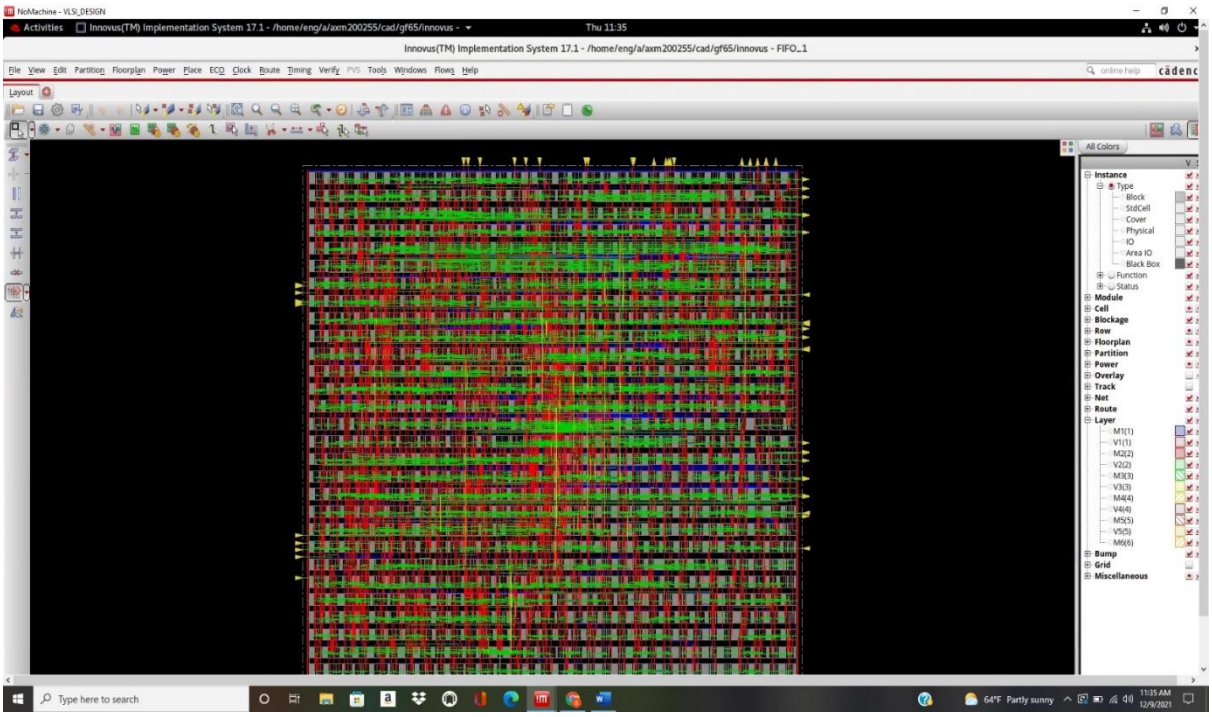
LAYOUT

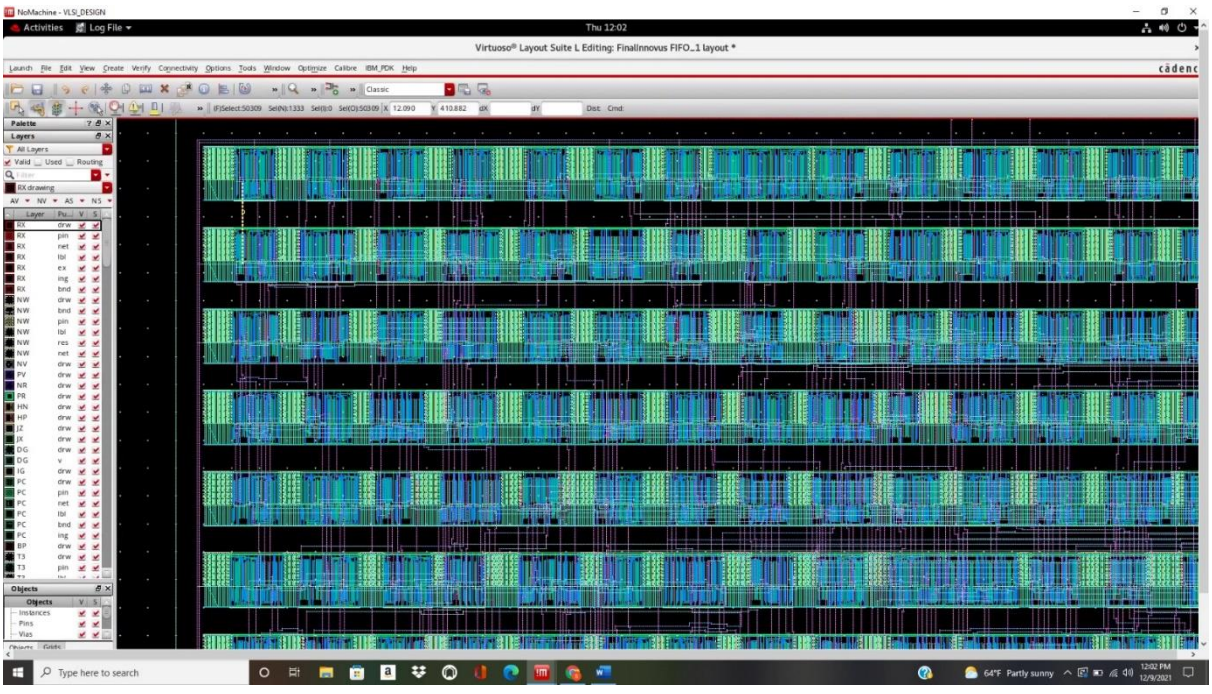
Measurements – Height = 498.16 um & Width = 481.78



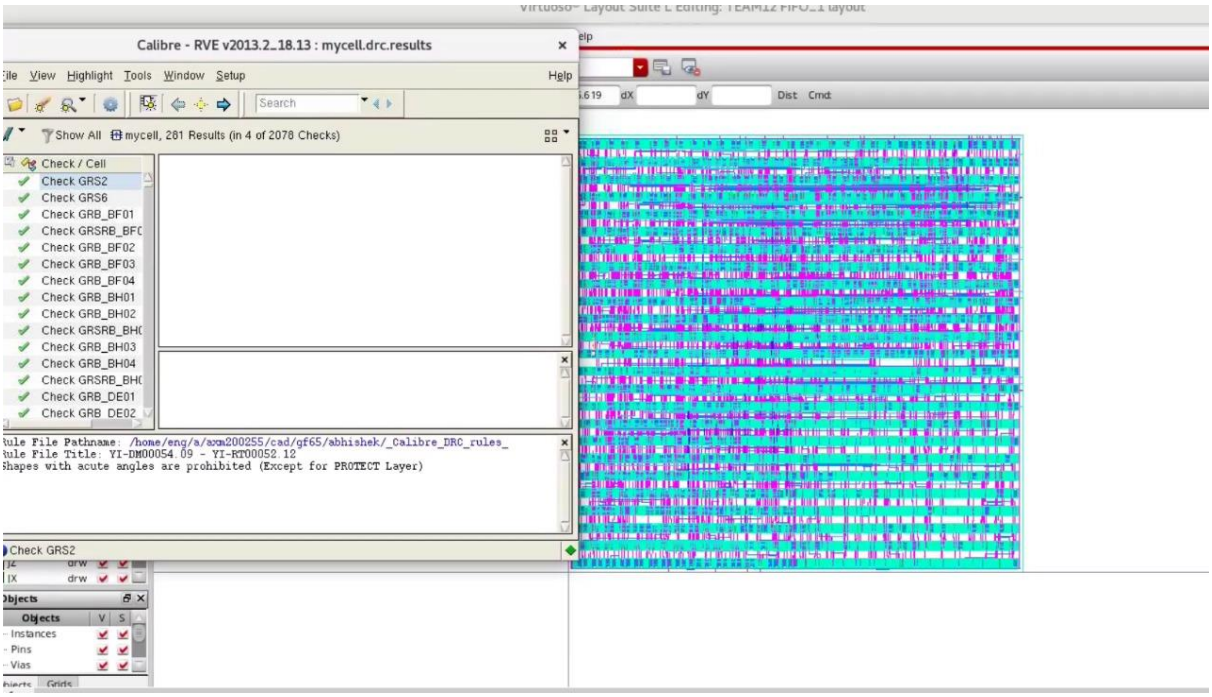
LAYOUT

LAYOUT CREATED IN INNOVUS:

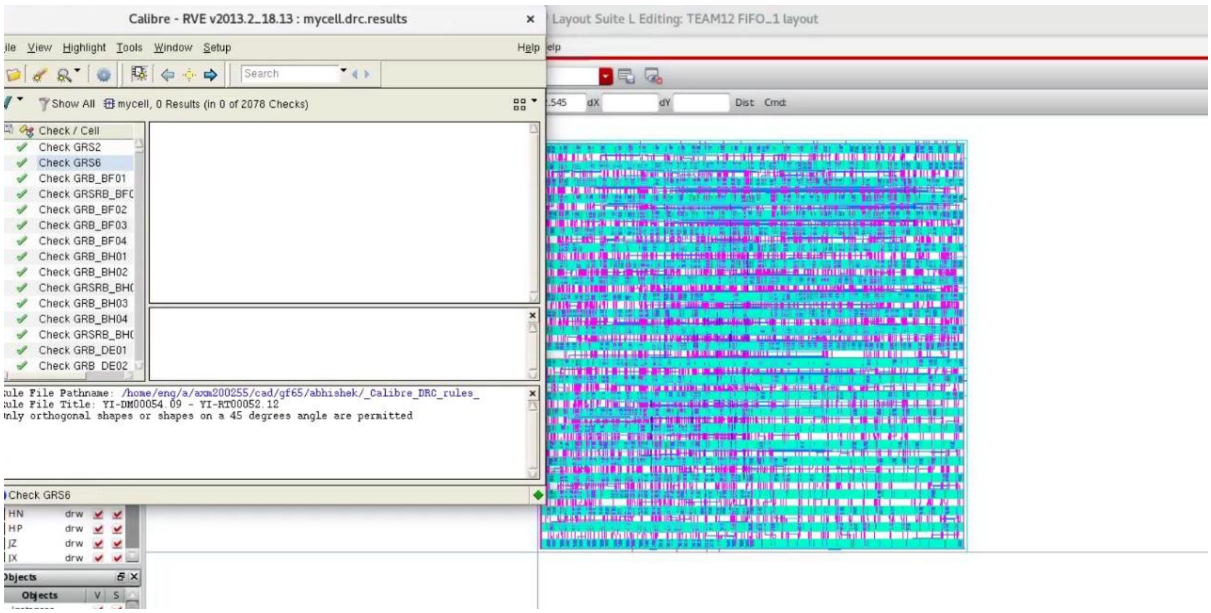




DRC RESULT

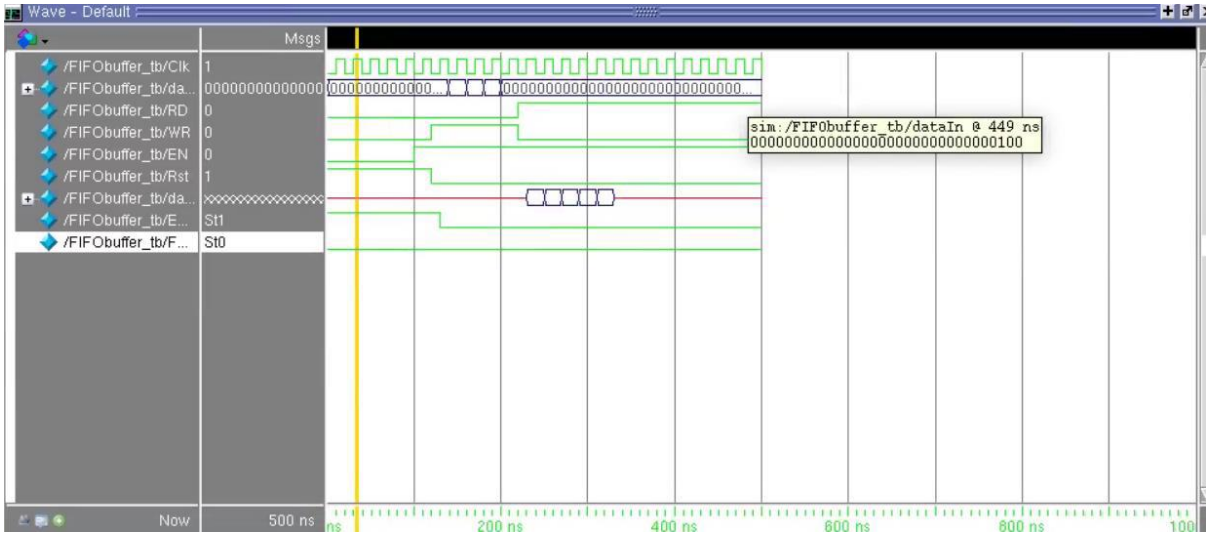


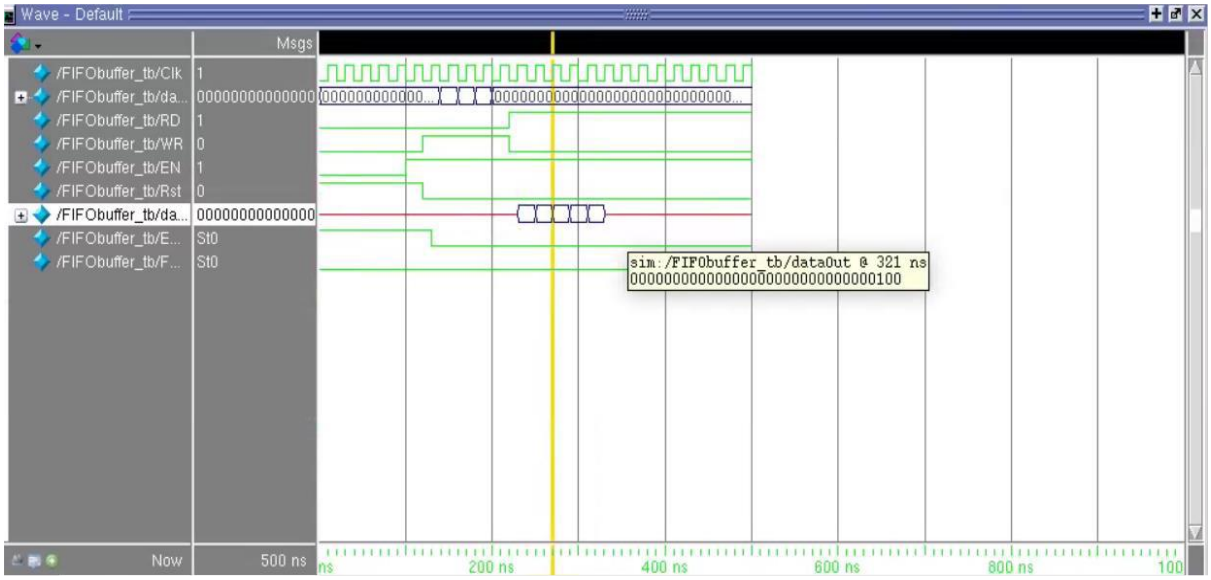
When we first ran the DRC, there were 22986 problems to resolve, but then we were able to get down to roughly 281 errors and then finally made it to 0(zero) errors.



OUTPUT WAVEFORM

Waveforms of our Verilog Code.





CONCLUSION

A 16-bit FIFO was designed to execute a simple first in first out operation. Each location is 16 bits long and has a depth of 16, implying that there are 16 locations. We ultimately put out the FIFO design using technologies like Cadence, Synopsys, and Innovus. The DRC for FIFO was passed, and the simulated waveform revealed the operation of FIFO.