

UNIVERSITY OF TEXAS AT DALLAS

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VLSI DESIGN (EECT 6325)

PROJECT DONE ON: D-FLIP FLOP

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	Transition from 0 to 1	Transition from 1 to 0
$T_{clk \rightarrow Q}$	4.54 ns	3.16 ns
T_{su_dd}	894 ps	865 ps
T_{hold}	894 ps	865 ps
T_{su_opt}	2.86 ns	1.26 ns
t_d	1.68 ns	4.42 ns

- Height of the Flip-Flop – 9.2 μm
- Width of the Flip-Flop – 5.516 μm
- Area of the Flip-Flop – 50.74 μm^2

ACKNOWLEDGEMENT

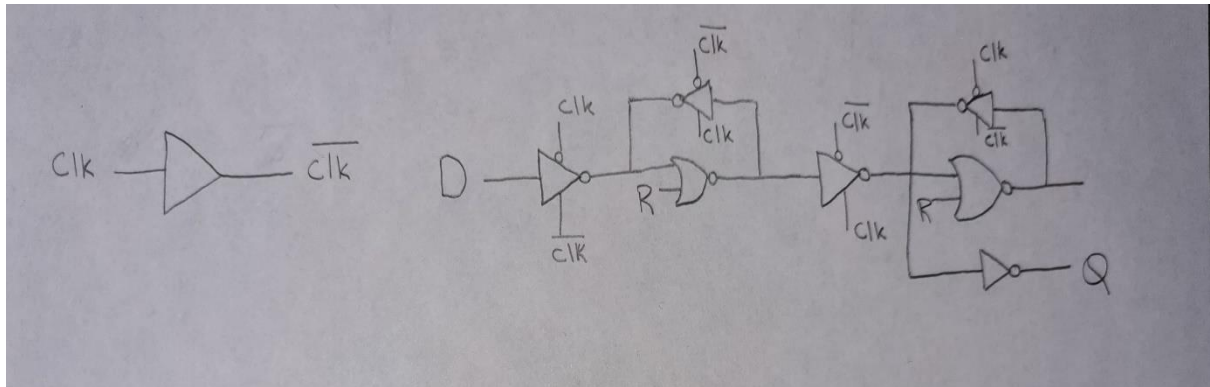
We are grateful to Professor CARL SECHEN for providing us an opportunity to explore and conduct Flip-Flop based projects in VLSI Design.

We also take this opportunity to express our gratitude to MR VAIBHAV KUMARSWAMY SALIMATH for his guidance in conducting the project.

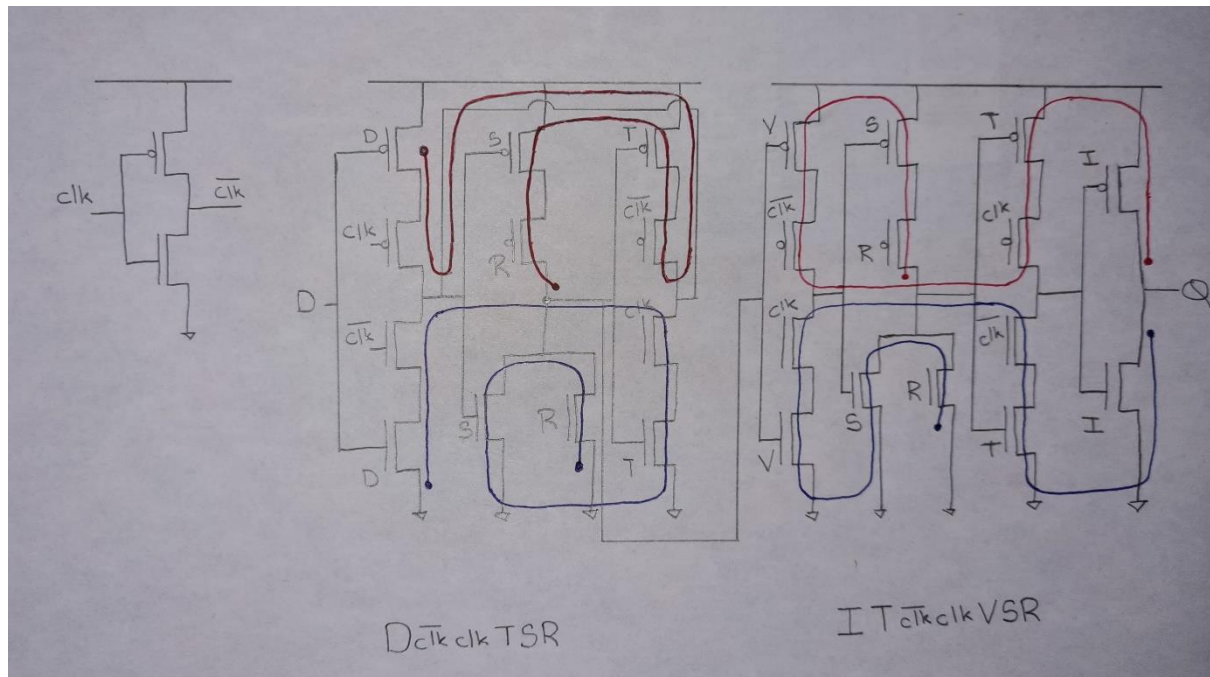
OBJECTIVE

In this project, we have used the Cadence Design tools to design, layout and characterize the D-Flip-Flop by minimizing the diffusion breaks and cell width.

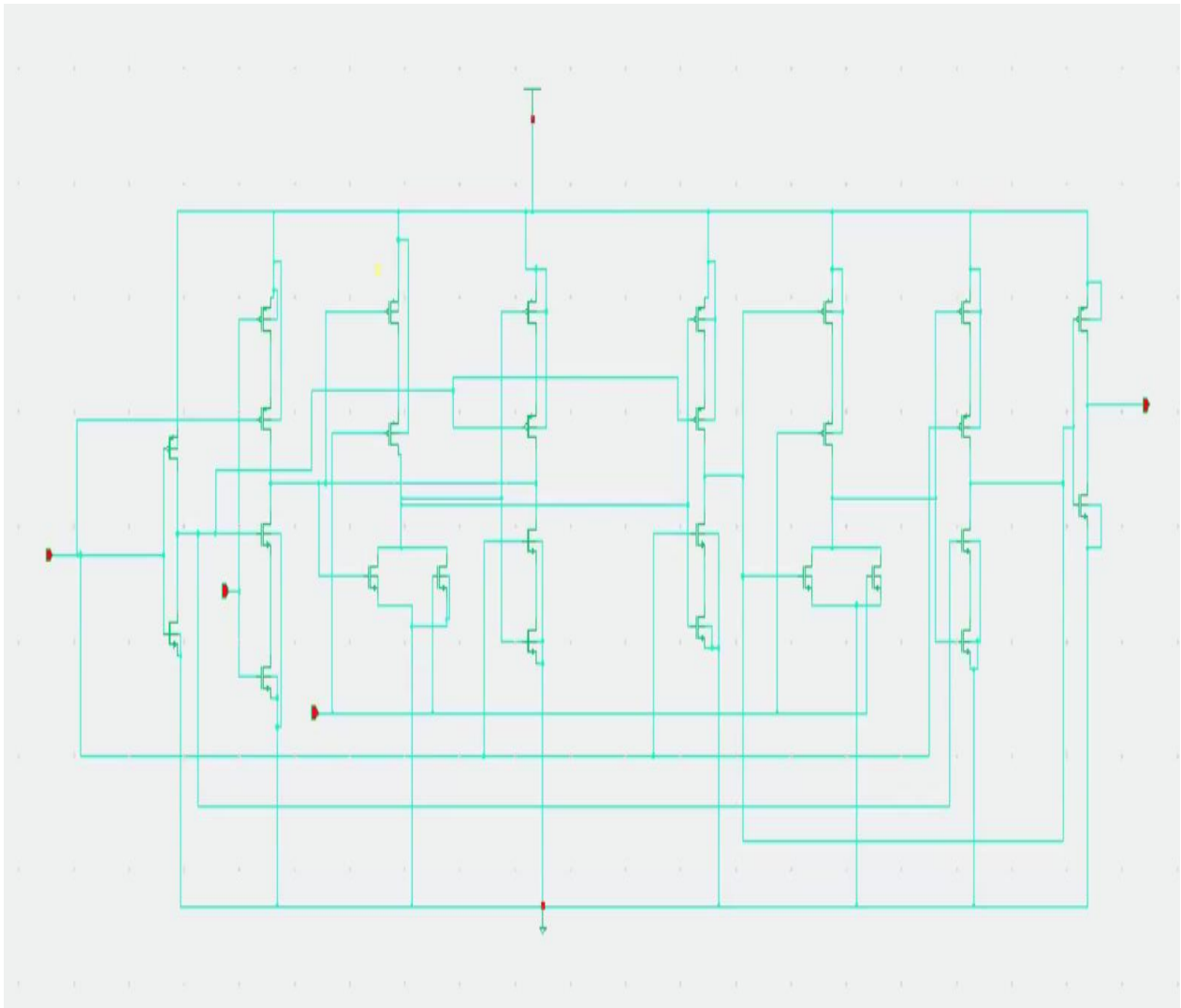
D FLIP-FLOP



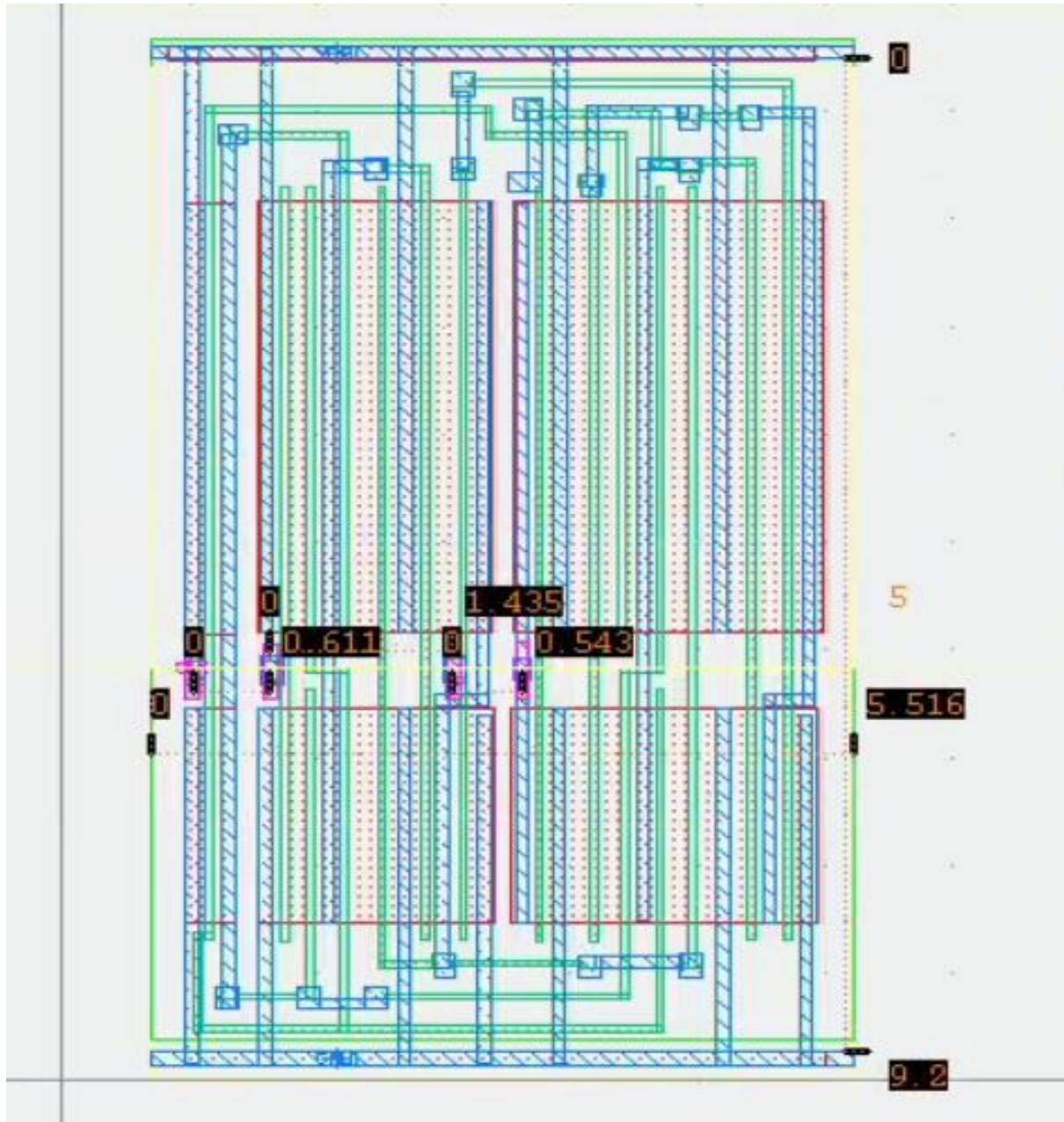
EULER TRAIL



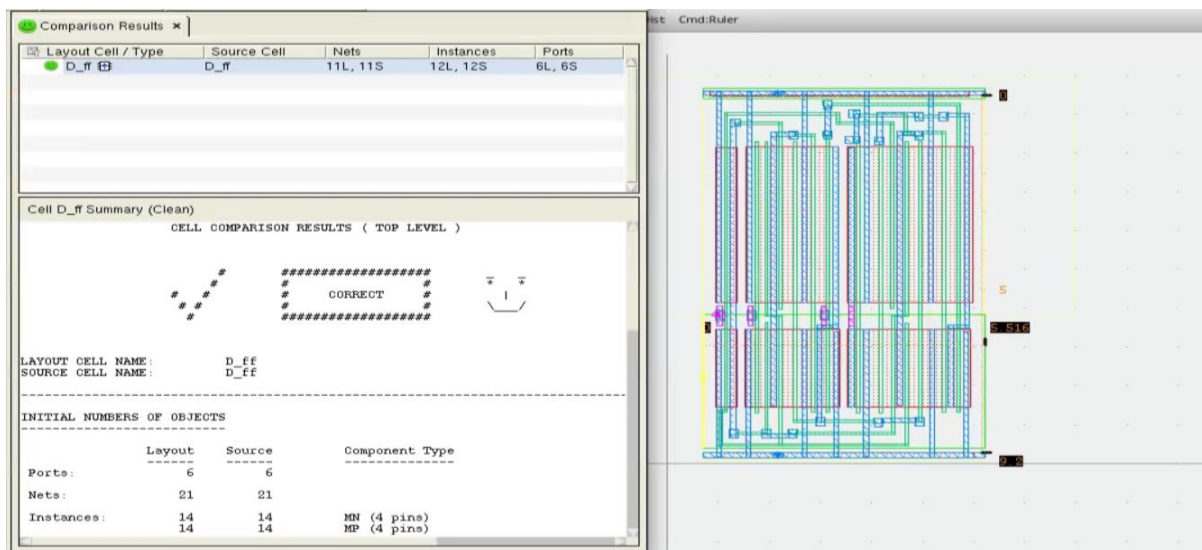
SCHEMATIC



LAYOUT



- Layout vs Schematic match



The screenshot shows a 'Comparison Results' window on the left and a schematic diagram on the right. The window displays a table with columns: Layout Cell / Type, Source Cell, Nets, Instances, and Ports. Below the table is a 'Cell D_ff Summary (Clean)' section showing 'CELL COMPARISON RESULTS (TOP LEVEL)' with a 'CORRECT' status. It also lists 'LAYOUT CELL NAME: D_ff' and 'SOURCE CELL NAME: D_ff'. A table of 'INITIAL NUMBERS OF OBJECTS' compares Layout and Source counts for Ports, Nets, and Instances. The schematic diagram on the right shows a complex circuit with multiple D flip-flops and their interconnections.

Layout Cell / Type	Source Cell	Nets	Instances	Ports
D_ff	D_ff	11L, 11S	12L, 12S	6L, 6S

Cell D_ff Summary (Clean)

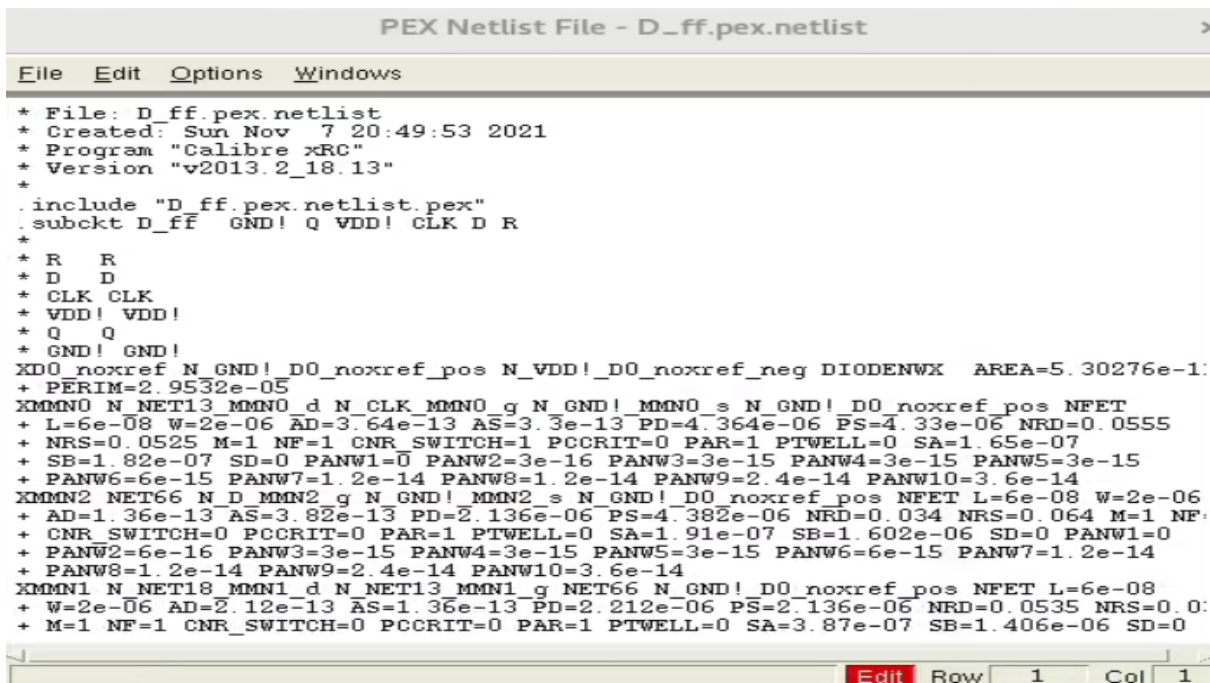
CELL COMPARISON RESULTS (TOP LEVEL)

LAYOUT CELL NAME: D_ff
SOURCE CELL NAME: D_ff

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	6	
Nets:	21	21	
Instances:	14	14	MM (4 pins)
	14	14	MP (4 pins)

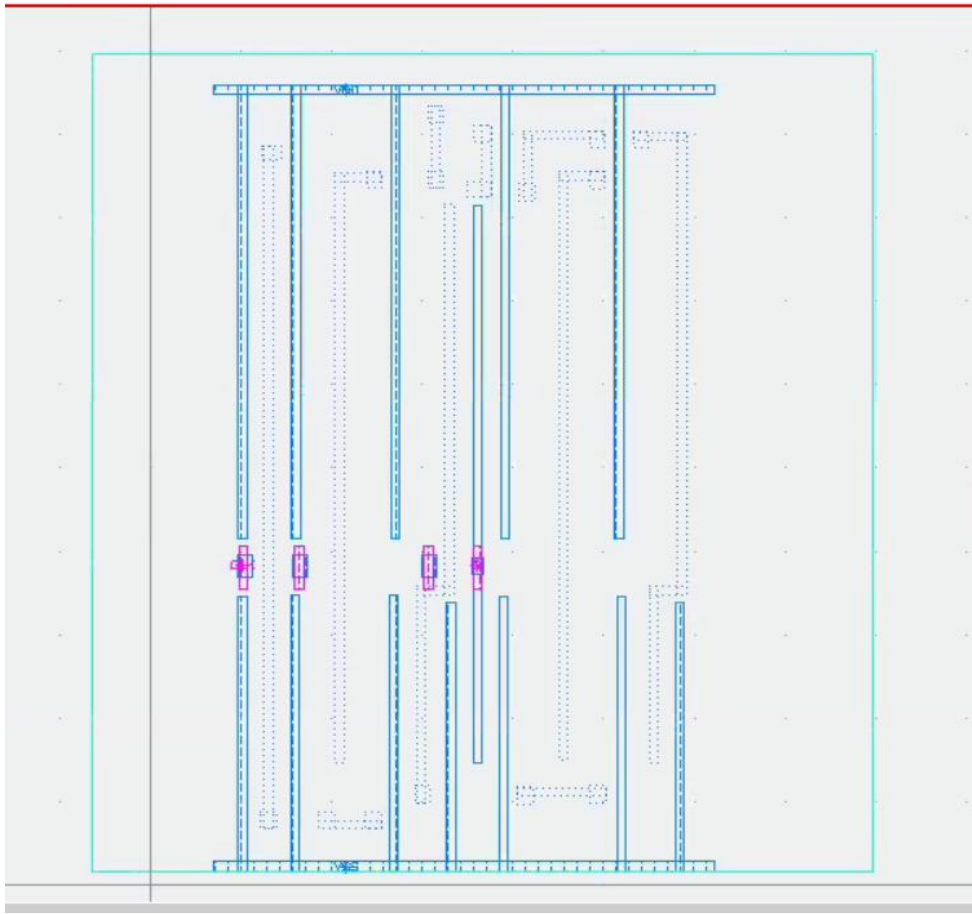
- Generated PEX File:



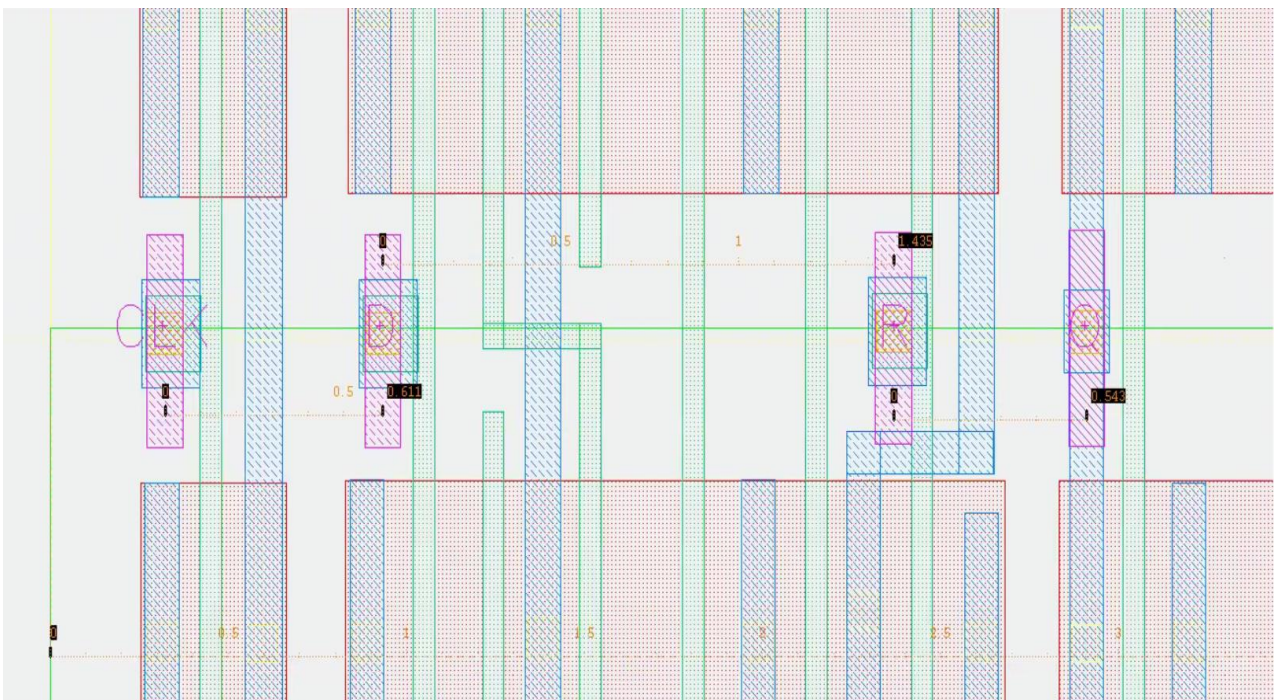
The screenshot shows a 'PEX Netlist File - D_ff.pex.netlist' window. It contains a text editor with the following content:

```
* File: D_ff.pex.netlist
* Created: Sun Nov 7 20:49:53 2021
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "D_ff.pex.netlist.pex"
.subckt D_ff GND! Q VDD! CLK D R
*
* R R
* D D
* CLK CLK
* VDD! VDD!
* Q Q
* GND! GND!
XDD_noxref N_GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=5.30276e-1:
+ PERIM=2.9532e-05
XMMN0 N_NET13 MMN0_d N_CLK MMN0_g N_GND! MMN0_s N_GND! D0_noxref_pos NFET
+ L=6e-08 W=2e-06 AD=3.64e-13 AS=3.3e-13 PD=4.364e-06 PS=4.33e-06 NRD=0.0555
+ NRS=0.0525 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=0 SA=1.65e-07
+ SB=1.82e-07 SD=0 PANW1=0 PANW2=3e-16 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN2 NET66 N_D MMN2_g N_GND! MMN2_s N_GND! D0_noxref_pos NFET L=6e-08 W=2e-06
+ AD=1.36e-13 AS=3.82e-13 PD=2.136e-06 PS=4.382e-06 NRD=0.034 NRS=0.064 M=1 NF=1
+ CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.91e-07 SB=1.602e-06 SD=0 PANW1=0
+ PANW2=6e-16 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14
+ PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN1 N_NET18 MMN1_d N_NET13 MMN1_g NET66 N_GND! D0_noxref_pos NFET L=6e-08
+ W=2e-06 AD=2.12e-13 AS=1.36e-13 PD=2.212e-06 PS=2.136e-06 NRD=0.0535 NRS=0.0:
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=3.87e-07 SB=1.406e-06 SD=0
```


ABSTRACT



PIN MEASUREMENTS



SIMULATION AND WAVEFORM

D FLIP-FLOP FUNCTIONALITY:

- **SPICE FILE:**

\$example HSPICE setup file

\$transistor model

.include"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_d1064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include D_flip_flop_connection.pex.sp

.option post runlvl=5

xi GND! Q VDD! CLK D R D_flip_flop_connection

vdd vdd! gnd! 1.2v

vb CLK gnd! PULSE (0v 1.2v 0ps 0ps 0ps 1000ps 2000ps)

V_D D gnd! pw1 (0ns 1.2v 2.5ns 1.2v 2.55ns 0v 6ns 0v 6.05ns 1.2v 8ns 1.2v 8.06666ns 1.2v 16ns 1.2v 16.06666ns 1.2v 22ns 1.2v 22.06666ns 0v 28ns 0v 28.06666ns 1.2v 32ns 1.2v)

V_R R gnd! pw1 (0ns 0v 10ns 0v 10.06666ns 1.2v 11ns 1.2v 12ns 1.2v 12.06666ns 0v)

cout Q GND! 90f

\$transient analysis

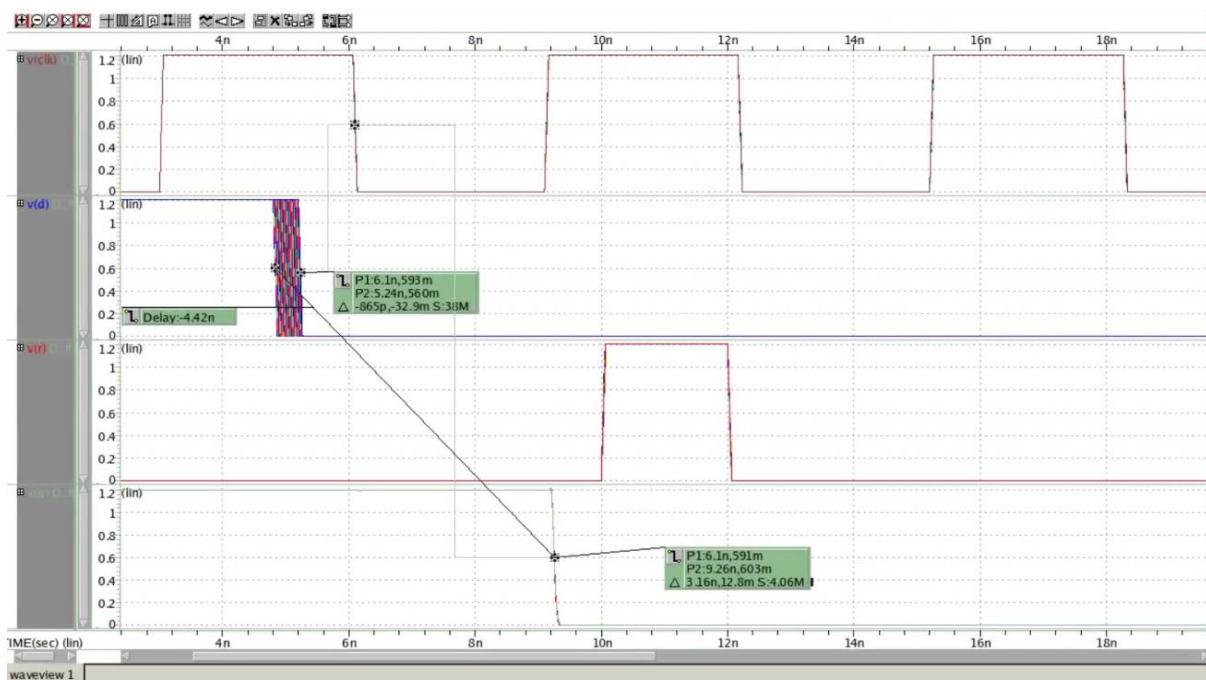
.tr 100ps 12ns

.end



- SPICE FILE FOR PASSING 0:

```
$example HSPICE setup file
$transistor model
.include
"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_2016
0415/models/YI-SM00030/Hspice/models/design.inc"
.include "D_ff.pex.netlist"
.global vdd! gnd!
.option post runlvl=5
xi GND! Q VDD! CLK D R D_ff
VDD VDD! GND! 1.2v
vclk clk gnd! PULSE (0v 1.2v 3ns 66.66ps 66.66ps 3ns 6.1ns)
vd D gnd! pw1 (0ns 1.2v 't1'1.2v 't1+0.066ns' 0v)
vr R gnd! pw1 (0ns 0v 10ns 0v 10.06666ns 1.2v 11ns 1.2v 12ns 1.2v
12.06666ns 0v)
cout Q gnd! 50f
.MEAS tsetup TRIG v(d) VAL=0.6V FALL=1 TARG v(clk) VAL=0.6v
FALL=3
.MEAS tclktoq TRIG v(clk) VAL=0.6v FALL=3 TARG v(Q) VAL=0.6v
FALL=1
.MEAS tran tdelay param='tsetup+tclktoq'
.trans 10ps 40ns sweep t1 4800ps 5200ps 5ps
.end
```



- SPICE FILE FOR PASSING 1:

\$example HSPICE setup file

\$transistor model

.include

"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_d1064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "D_ff.pex.netlist"

.global vdd! gnd!

.option post runlvl=5

xi GND! Q VDD! CLK D R D_ff

VDD VDD! GND! 1.2v

vclk clk gnd! PULSE (0v 1.2v 3ns 66.66ps 66.66ps 3ns 6.1ns)

vd D gnd! pwl (0ns 0v 't1'0v 't1+0.066ns' 1.2v)

vr R gnd! pwl (0ns 0v 10ns 0v 10.06666ns 1.2v 11ns 1.2v 12ns 1.2v 12.06666ns 0v)

cout Q gnd! 50f

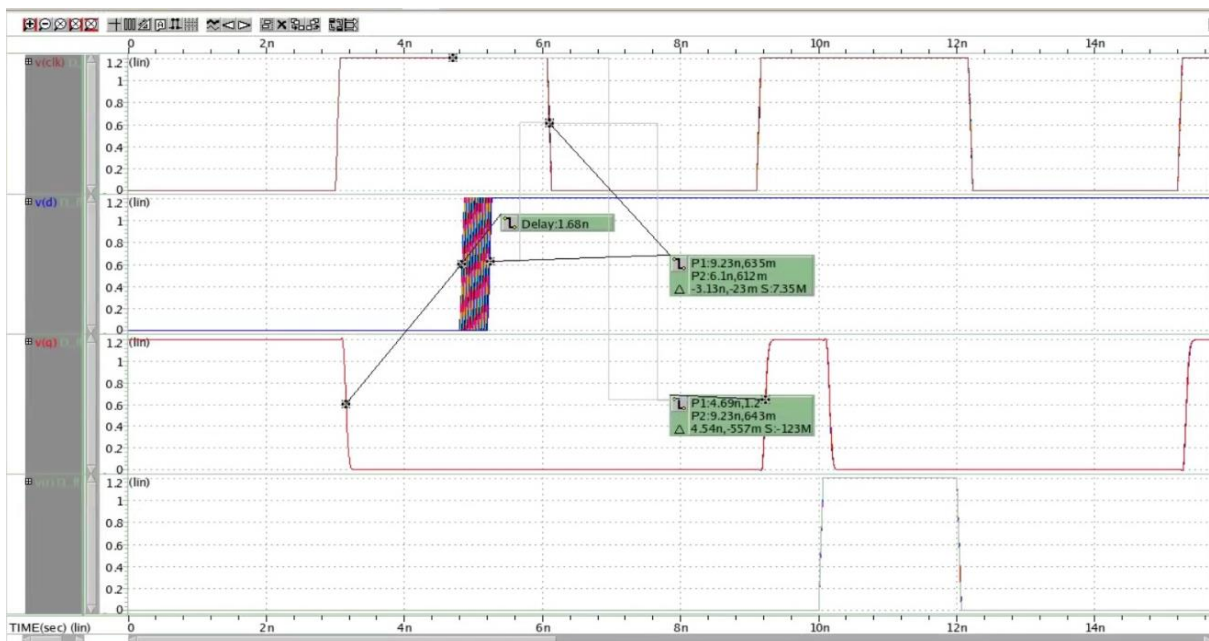
.MEAS tsetup TRIG v(d) VAL=0.6V FALL=1 TARG v(clk) VAL=0.6v FALL=3

.MEAS tclktoq TRIG v(clk) VAL=0.6v FALL=3 TARG v(Q) VAL=0.6v FALL=1

.MEAS tran tdelay param='tsetup+tclktoq'

.trans 10ps 40ns sweep t1 4800ps 5200ps 5ps

.end



- We generated a batch of inputs to find Tsu_dd, Tsu_opt and calculation of Tclk->q,

\$DATA1 SOURCE='HSPICE' VERSION='L-2016.06-SP1-2 linux64' PARAM_COUNT=1 .TITLE '\$example hspice setup file'			
t1	tsetup alter#	tclktoq	temper
4.800e-09	1.347e-08	-9.044e-09	25.0000
4.810e-09	1		
4.810e-09	1.346e-08	-9.044e-09	25.0000
4.820e-09	1		
4.820e-09	1.345e-08	-9.044e-09	25.0000
4.830e-09	1		
4.830e-09	1.344e-08	-9.044e-09	25.0000
4.840e-09	1		
4.840e-09	1.343e-08	-9.044e-09	25.0000
4.850e-09	1		
4.850e-09	1.342e-08	-9.044e-09	25.0000
4.860e-09	1		
4.860e-09	1.341e-08	-9.044e-09	25.0000
4.870e-09	1		
4.870e-09	1.340e-08	-9.044e-09	25.0000
4.880e-09	1		
4.880e-09	1.339e-08	-9.044e-09	25.0000
4.890e-09	1		
4.890e-09	1.338e-08	-9.044e-09	25.0000
4.900e-09	1		
4.900e-09	1.337e-08	-9.044e-09	25.0000
4.910e-09	1		
4.910e-09	1.336e-08	-9.044e-09	25.0000
4.920e-09	1		
4.920e-09	1.335e-08	-9.044e-09	25.0000
4.930e-09	1		
4.930e-09	1.334e-08	-9.044e-09	25.0000
4.940e-09	1		
4.940e-09	1.333e-08	-9.044e-09	25.0000
4.950e-09	1		
4.950e-09	1.332e-08	-9.044e-09	25.0000
4.960e-09	1		
4.960e-09	1.331e-08	-9.044e-09	25.0000

EXPLANATION

- **DROP DEAD SETUP TIME (T_{su_dd}):** T_{su_dd} is the minimum time that is taken by the input to arrive before the active clock edge so that input signal can be captured at the output. This is usually calculated by plotting a graph of setup time vs gate time delay.
- **OPTIMUM SETUP TIME (T_{su_opt}):** Optimum Setup time is defined as the setup time for which time delay(t_d) is minimum.
$$T_{su_opt} + T_{clk \rightarrow Q} = t_d$$
- **HOLD TIME (T_{hold}):** The minimum amount of time that the data signal should be held steady after the clock even making sure the data is processed is called hold time.
$$T_{su_dd}(1) = T_{hold}(0) \text{ and } T_{su_dd}(0) = T_{hold}(1).$$
- **T CLK TO Q ($T_{clk \rightarrow Q}$):** The clk to Q time is the time required for the output to have a stable/valid value after the falling edge of the clock. It is the time difference between 50% amplitude of the clock and the output.
- **DELAY TIME(t_d):** Delay time is defined as $t_d = T_{su_opt} + T_{clk \rightarrow Q}$

RESULT

The functionality of D-flip flop is verified.