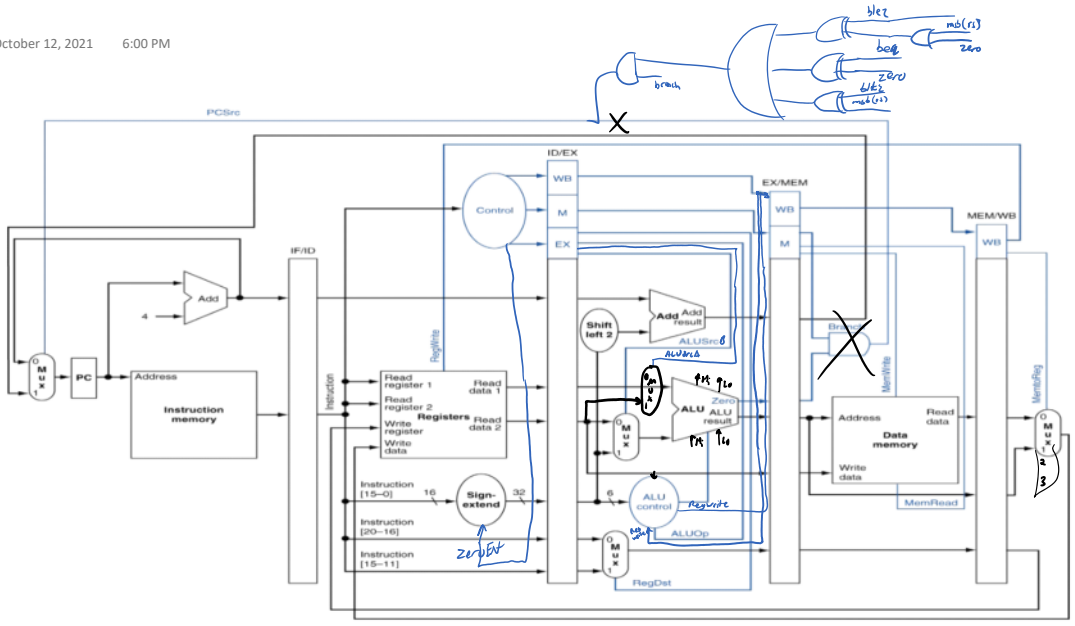
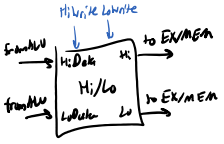
Tuesday, October 12, 2021 6:00 PM



Instruction Type	Instruction	RegWrite	ZeroExt	ALUSrcB	ALUSrcA	ALUOp	RegDst	Branch	MemWrite	MemRead	MemToReg	HiWrite	LoWrite	Beq	Bltz	Blez
Arithmetic, R-type	add rd, rs, rt	1	X	0	0	add	1	0	0	X	1	0	0	X	X	X
	addu rd, rs, rt	1	X	0	0	add	1	0	0	X	1	0	0	X	X	X
	sub rd, rs, rt	1	X	0	0	sub	1	0	0	X	1	0	0	X	X	X
	mul rd, rs, rt	1	X	0	0	mult	1	0	0	X	1	0	0	X	X	X
Arithmetic, I-type	addi rt, rs, imm	1	0	1	0	add	0	0	0	X	1	0	0	X	X	X
	addiu rt, rs, imm	1	1	1	0	add	0	0	0	X	1	0	0	X	X	X
Arithmetic, hi-lo	mult rs, rt	0	X	0	0	mult	X	0	0	X	X	1	1	X	X	X
	multu rs, rt	0	X	0	0	multu	X	0	0	X	X	1	1	X	X	X
	madd rs, rt	0	X	0	0	madd	X	0	0	X	X	1	1	X	X	X
	msub rs, rt	0	X	0	0	msub	X	0	0	X	X	1	1	X	X	X
Data, I-type	lw rt, imm(rs)	1	0	1	0	add	0	0	0	1	0	0	0	X	X	X
	sw rt, imm(rs)	0	0	1	0	add	X	0	1	X	X	0	0	X	X	X
	lh rt, imm(rs)	1	0	1	0	add	0	0	0	1	0	0	0	X	X	X
	sh rt, imm(rs)	0	0	1	0	add	X	0	1	X	X	0	0	X	X	X
	lb rt, imm(rs)	1	0	1	0	add	0	0	0	1	0	0	0	X	X	X
	sb rt, imm(rs)	0	0	1	0	add	X	0	1	X	X	0	0	X	X	X
	lui rt, imm	1	X	1	0	sll16	0	0	0	X	1	0	0	X	X	X
Branch, I-type	beq rs, rt, imm	0	0	0	0	sub	X	1	0	X	X	0	0	1	X	X
	bgez rs, imm	0	0	0	0	X	X	1	0	X	X	0	0	X	0	X
	bne rs, rt, imm	0	0	0	0	sub	X	1	0	X	X	0	0	0	X	X
	bgtz rs, imm	0	0	0	0	add	X	1	0	X	X	0	0	X	X	0
	blez rs, imm	0	0	0	0	add	X	1	0	X	X	0	0	X	X	1
	bltz rs, imm	0	0	0	0	X	X	1	0	X	X	0	0	X	1	X
Jump, J-type	j addr													X	X	X
	jal addr													X	X	X
Jump, R-type	jr rs													X	X	X
Logical, R-type	and rd, rs, rt	1	X	0	0	and	1	0	0	X	1	0	0	X	X	X
	or rd, rs, rt	1	X	0	0	or	1	0	0	X	1	0	0	X	X	X
	nor rd, rs, rt	1	X	0	0	nor	1	0	0	X	1	0	0	X	X	X
	xor rd, rs, rt	1	X	0	0	xor	1	0	0	X	1	0	0	X	X	X
	seh rd, rt	1	X	0	0	seh	1	0	0	X	1	0	0	X	X	X
	seb rd, rt	1	X	0	0	seb	1	0	0	X	1	0	0	X	X	X
	slt, rd, rs, rt	1	X	0	0	slt	1	0	0	X	1	0	0	X	X	X
	sltu rd, rs, rt	1	X	0	0	sltu	1	0	0	X	1	0	0	X	X	X
	movn rd, rs, rt	X	X	X	0	passA	1	0	0	X	1	0	0	X	X	X
	movz rd, rs, rt	X	X	X	0	passA	1	0	0	X	1	0	0	X	X	X
Shifts/Rotates, R-type	sll rd, rt, shamt	1	X	1	1	sll	1	0	0	X	1	0	0	X	X	X
	srl rd, rt, shamt	1	X	1	1	srl	1	0	0	X	1	0	0	X	X	X
	sllv rd, rt, rs	1	X	0	0	sllv	1	0	0	X	1	0	0	X	X	X
	srlv rd, rt, rs	1	X	0	0	srlv	1	0	0	X	1	0	0	X	X	X
	sra rd, rt, shamt	1	X	1	1	sra	1	0	0	X	1	0	0	X	X	X
	srav rd, rt, rs	1	X	0	0	srav	1	0	0	X	1	0	0	X	X	X
	rotr rd, rt, shamt	1	X	1	1	rotr	1	0	0	X	1	0	0	X	X	X



	rotrv rd, rt, rs	1	X	0	0	rotr	1	0	0	X	1	0	0	X	X	X
Logical, I-type	andi rt, rs, imm	1	0	1	0	and	0	0	0	X	1	0	0	X	X	X
	ori rt, rs, imm	1	0	1	0	or	0	0	0	X	1	0	0	X	X	X
	xori rt, rs, imm	1	0	1	0	xor	0	0	0	X	1	0	0	X	X	X
	slti rt, rs, imm	1	0	1	0	slt	0	0	0	X	1	0	0	X	X	X
	sltiu rt, rs, imm	1	0	1	0	sltu	0	0	0	X	1	0	0	X	X	X
Hi/Lo	mthi rs	0	X	X	0	mthi	X	0	0	X	X	1	0	X	X	X
	mtlo rs	0	X	X	0	mtlo	X	0	0	X	X	0	1	X	X	X
	mfhi rd	1	X	X	X	mfhi	1	0	0	X	1	0	0	X	X	X
	mflo rd	1	X	X	X	mflo	1	0	0	X	1	0	0	X	X	X
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