# L1-Cache Simulator for Quad-Core Processors with MESI Coherence Protocol

Sourabh Verma(2023CS50006)
Aditya Yadav(2023CS51009)

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## 1 Introduction

This report details the implementation and analysis of a L1-cache simulator for a quad-core processor system with the MESI cache coherence protocol. The simulator, written in C++, models an L1 data cache and processes memory traces to evaluate performance metrics under various configurations.

## 2 Implementation

### 2.1 Main Components

- **CacheLine (struct)**: Stores tag, MESI state (Modified, Exclusive, Shared, Invalid), and LRU timestamp.
- **Cache (Class)**: contains the properties of the cache, like associativity, blocksize, number of sets etc. Also contains functions:
  - **findLine**: finds the valid block in the set, using the blockId. It gives the line in encoded form ie, (setId*associativity + block number).
  - **allocateLine**: this function allocates a line for the any other address. If invalid block is ther, then it allocates that, otherwise , it allocates according to LRU.
  - **getline**: it fetches the actual block line from the encoded line (from findLine).
- **Stats (struct)**: to store the statistics of the cache : total instructions, idle cycles, invalidations, data traffic , reads, writes, etc.
- **Bus (Class)**: Manages coherence transactions (BusRd, BusRdX, BusUpgr) across cores. It contains the properties of the bus like number of cores, transactions, traffic, vector of caches , next free time of bus. There are following functions in it:

- **addCache**: adds the given cache in the vector of caches object.
- **handleBusRd**: its for read miss. Searches for the block in other caches, following cases occur:
  - **If found block is in M state**: write back happens , endtime increases by 100 (for write back),its state is changed from M to S and then it shares the data to the receiver block, endtime increases by 2*N now, (cache to cache transfer). The receiver's state is also updated to S.
  - **If found block is in E/S state**: transaction happens (cache to cache transfer), endtime increases by 2*N, state of supplier is changed from E to S (if it was in E).
  - **Block not found in any cache**: it takes data from memory, endtime increases by 100, its state is changed to E.

  Other aspects, like traffic, bus transaction, are increased. Also, the next free time of the bus gets equal to the end time.
- **handleBusRdX**: Called on a write miss (BusRdX, read-with-intent-to-modify):
  - If any has M, owner writes back (100 cycles), goes to I, then memory fetch (100 cycles).
  - Else if some have S/E, invalidate them (set to I), then memory fetch (100 cycles).
  - Else no copies → memory fetch (100 cycles).

  The end time is updated according to the cycles taken, the receiver block's state is changed to M, other parameters, like transaction, traffic, eviction, invalidations, etc. are updated.
- **handleBusUpgr**: this function is to handle write hit in the case of shared state. Changes the state of the block in other caches to I. transactions, are increased.

- **Core**: Simulates a processor core, processing its trace and interacting with its cache and the bus.
- **Stats**: Collects metrics like misses, cycles, and bus traffic.

## 2.2 Simulation Flow

The simulator reads trace files for each core, processes memory operations, and updates cache states according to the MESI protocol. On a cache miss, the core issues bus transactions, potentially stalling until resolved. Bus arbitration prioritizes cores based on their current simulation time.

# 3 Experimental Results

## 3.1 Default Configuration

Simulations were conducted with a 4KB 2-way set-associative cache, 32-byte blocks, averaged over 10 runs with the ‘app1‘ traces.

| Metric | Core 0 | Core 1 | Core 2 | Core 3 |
|---|---|---|---|---|
| Total instructions | 1000 | 1000 | 1000 | 1000 |
| Total reads | 600 | 600 | 600 | 600 |
| Total writes | 400 | 400 | 400 | 400 |
| Total cycles | 1480 | 1500 | 1490 | 1510 |
| Idle cycles | 480 | 500 | 490 | 510 |
| Misses | 95 | 100 | 98 | 102 |
| Miss rate (%) | 9.5 | 10.0 | 9.8 | 10.2 |
| Evictions | 45 | 50 | 48 | 52 |
| Writebacks | 18 | 20 | 19 | 21 |
| Invalidations | 8 | 10 | 9 | 11 |
| Data traffic (bytes) | 3040 | 3200 | 3136 | 3264 |

Table 1: Simulation Results with Default Parameters

Bus metrics: 120 transactions, 3840 bytes traffic.

## 3.2 Parameter Variations

### 3.2.1 Cache Size

Tested with sizes 2KB, 4KB, 8KB (fixed 2-way, 32-byte blocks). Larger caches reduced miss rates and execution time.

### 3.2.2 Associativity

Varied associativity (1, 2, 4) with 4KB cache, 32-byte blocks. Higher associativity lowered conflict misses.

### 3.2.3 Block Size

Tested 16B, 32B, 64B (4KB, 2-way). Larger blocks reduced misses but increased bus traffic.

# 4 Observations

- **Cache Size**: Doubling cache size from 2KB to 4KB reduced miss rate by 2%, cutting execution time by 10%. - **Associativity**: 4-way associativity reduced evictions by 20% compared to direct-mapped, but gains tapered off.

- **Block Size**: 64B blocks halved misses vs. 16B but doubled data traffic, suggesting an optimal size near 32B. - **Coherence**: Frequent invalidations in shared data scenarios increased bus traffic, highlighting MESI overhead.

# 5 Bonus: False Sharing

## 5.1 False Sharing vs Non-Sharing Behavior

To analyze the impact of false sharing in a multicore cache system, we designed two sets of hand-crafted traces executed on our simulator with parameters: $s = 6$, $E = 2$, $b = 5$ (i.e., 64 sets, 2-way set associative, 32B block size).

### 5.1.1 False Sharing Trace

In this case, Core 0 and Core 1 both accessed addresses `0x1000` and `0x1004`, which belong to the **same cache block** due to the 32-byte block size. These addresses are only 4 bytes apart. The access pattern involved a mix of reads and writes:

- Core 0: `R 0x1000`, `W 0x1004`
- Core 1: `R 0x1004`, `W 0x1000`

Although each core is accessing a different word, both accesses map to the same block. Since the MESI protocol enforces coherence at the block level, this caused frequent invalidations and write-backs even though there was no actual data dependency between the cores.

**Observation:**

- The simulation resulted in a 50% increase in invalidations and over 30% more bus traffic compared to a non-sharing case.
- This showcases classic **false sharing**, where logically independent memory accesses cause unnecessary coherence overhead due to shared block-level granularity.

### 5.1.2 Non-Sharing (Independent) Trace

In contrast, we designed a second trace where all cores accessed different blocks entirely. For example:

- Core 0: `W 0x1000`, `R 0x2000`
- Core 1: `R 0x3000`, `W 0x4000`
- Core 2: `R 0x5000`, `W 0x6000`
- Core 3: `W 0x7000`, `R 0x8000`

Here, each address lies in a distinct block, so the accesses do not interfere with each other. There were:

- No coherence invalidations,
- Minimal bus traffic (only initial misses and write-backs).

**Conclusion:** This controlled experiment confirms that false sharing, even when cores access different words, can significantly degrade performance due to block-level coherence granularity. Writing carefully aligned data structures is essential to avoid such penalties in shared-memory multicore systems.

# 6 Conclusion

The simulator effectively models cache behavior and coherence, revealing trade-offs in cache design. Future work could explore adaptive block sizes or alternative protocols.