Parrot OS

AMD Ryzen 9 5900x

A: Find out which hardware platform(s) your chosen operating system runs on. In the following research questions, use that platform. If your OS runs on multiple platforms, pick one. If you're working with a historical OS (eg. AmigaOS, Windows 95), then go with a processor of that era (eg. a Motorola 68K CPU for Amiga, an old Pentium for Windows 95).

Parrot OS kører på enten AMD x86-64 eller ARM.
Vi har valgt at gå i dybden med AMD's Ryzen 9 5900x som er en x86-64 processor.
AMD Ryzen 9 5900x er en del af de nyeste generation af AMD cpu'er, og benytter sig at Zen 3 arkitektur

B. Research the basics of your chosen hardware platform. How many registers are there? How big are each? (16-, 32, 64-bit). Are multicore processors available? Give an overview description of the processor.

AMD ryzen 9 5900x har 16 registers af størrelsen 64-bit

- Processor (CPU), 3.7 GHz (4.8 GHz Turbo), Unlocked (kan overclockes), 12 kerner (Dodeca Core), 24 tråde, 70 MB cache, understøtter Dual Channel DDR4-3200 RAM, bedre end intel, 24 PCI Express Gen 4.0 Lanes, AM4 Socket, 105 watt TDP, Box **(dog uden køler)** - Zen 3

AMD ryzen 9 5900x har 12 cores og 24 tråde. CPU'en har en normal clock speed på 3.7 GHz og har en overclock speed på 4.8 GHz

C. Find out what the pipeline architecture of the platform is like. How many stages are there? Can you find out what each stage does? Not all CPU manufacturers publish a full pipeline spec; you can read up on an older pipeline in the same family if you can't find anything on the latest and greatest generation.

19 stages for at execute en given instruction

Type	Superscalar
OoOE	Yes
Speculative	Yes
Reg Renaming	Yes
Stages	19
Decode	4-way

https://www.hardwaresecrets.com/inside-amd64-architecture/

https://en.wikichip.org/wiki/amd/microarchitectures/zen_3

D. Describe the cache architecture (if any) of your chosen hardware platform.

vores valgte processer “AMD Ryzen 9 5900x” har 3 levels af cache L1, L2 og L3.

L1:

Størrelsen på L1 cachen er 64KB per core så 12 x 64KB(768KB) i det her tilfælde men den er delt op i 2 dele af 12 x 32KB(384KB) hvor den ene er “8-way set associative instruction cache” og den anden er “8-way set associative data cache”

L2:

Størrelsen på L2 cachen er 512KB per core så 12 x 512KB(6144KB) af “8-way set associative unified cache”

L3:

Størrelsen på L3 cachen er 64MB som er delt i 2 x 32MB “16-way set associative shared cache”

Cache L1:	64K (per core)

Cache L2:	512K (per core)
Cache L3:	64MB

E. Describe the bus architecture of your chosen platform --- eg. does it use a single bus, a Northbridge/Southbridge split, or something completely different?

Grundet Ryzen 5000 serien bruger vermeer cores, så er både northbridge og southbridge on chip.