General Description

The DS4835 is a low-power, 16-bit microcontroller with a unique peripheral set supporting optical applications that require high-resolution conversion of many analog signals and digital-signal processing (DSP) of those signals, and an external host interface. The device integrates various power management integrated circuits (PMIC) blocks including an inrush control and DC-DC converters that can be used to power various slave components. An integrated TEC controller provides temperature control for DWDM laser applications. A wide variety of optical transceiver controller applications are supported without the need of external circuitry, thereby minimizing cost and PCB area. Power dissipation and throughput are optimized using a programmable round-robin 16-bit analog-to-digital converter (ADC) and 16-bit fast comparator, which operate completely independent of the core and significantly reduce core overhead. A dual multiply/accumulate (MAC) is included to minimize interrupt service timing. 16-bit PWM channels are included to provide an unprecedented level of precision in digital power-control applications.

The DS4835 provides a complete optical control, calibration, and monitor solution compatible with various optical transceiver multisource agreements (MSA). Additional resources include a fast and accurate ADC, fast window comparators, delta-sigma (DS) DAC and current DACs, an accurate internal temperature sensor, two fast sample-holds, and a multi-protocol serial master/slave interface. An independent, 400kHz-compliant, slave I^2C interface with four configurable slave addresses facilitates communication to a host, in addition to password-protected in-system programming of the on-chip flash. Extensive design-in and applications support are available, including comprehensive user's and programmer's guides, complete reference designs with documented code, and in-depth application notes showing numerous code examples in both C and assembly language. Firmware development is supported by third-party vendors.

Applications

- SFP+/SFP28/SF56, Tunable
- OLT: XGSPON, NGPON2
- QSFP28, QSFP56, QSFP-DD, OSFP

Benefits and Features

- Integrated PMIC and Analog Saves Space
  - 4 DC-DC Converters (3 Buck, 1 Buck or Boost)
  - 2 TEC Controllers
  - 4 Current DACs
  - Inrush Current Control
  - Internal 128MHz Oscillator
- Simplifies Complex Optical Module Design
  - 16-Bit 500ksps ADC (with up to 24 External Channels)
  - Internal and External Temperature Sensor, ±3°C
  - 16-Bit Fast Comparator with 8-Input Mux
  - 12 16-Bit Delta-Sigma DAC
  - 4 Programmable Logic Arrays
  - Slave Communication Interface: I^2C Compatible 2-Wire 400kHz without Clock Stretching
  - Master Communication Interface: up to 1MHz I^2C Compatible 2-Wire, SPI or Maxim 3-Wire Laser Driver
  - Two Independent Sample and Holds (300ns Sample Time)
  - 23 GPIO and 4 GPI Pins
  - 8 16-Bit PWM Channels
- Microcontroller Features Enable Flexibility
  - 16-Bit Low-Power Microcontroller
  - 64kB Flash Program Memory
  - 4kB Data RAM
  - 8kB ROM Memory
  - 32-Level Hardware Stack
  - Supply-Voltage Monitor (SVM) and Brownout Monitor
  - I^2C Bootloader
  - 1-Wire® In-System Debug and Programming
  - Dual-Hardware MAC
  - 5mm x 5mm, 40-Pin TQFN Package
  - Three 16-Bit Timers and One Programmable Watchdog Timer

Ordering Information *appears at end of data sheet.*

19-100211; Rev 2; 6/21

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Absolute Maximum Ratings (Note 1)

V_{CCI}, V_{CCO} to GND .....-0.3V to +3.97V
SDA and SCL .....-0.3V to +5.5V
All Other Pins (except BYP18) to EP .....-0.3V to V_{DD} + 0.3V
BYP18 to EP .....-0.3V to +2.0V
Continuous Power Dissipation Multi-Layer Board TQFN
(T_A = +70°C, derate 35.7mW/ºC above +70ºC) ...2857.10mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -40°C to +150°C
DC-DC Boost RMS Current 300mA
DC-DC Buck RMS Current 1.6A
LX3 and PV_{CC3} Voltage.....4.2V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 40 TQFN	
Package Code	T4055+2
Outline Number	**21-0140**
Land Pattern Number	**90-0016**
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	45°C/W
Junction to Case (θ_{JC})	2°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	2°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CCI}, V_{CCO}, PV_{CC1-4} Operating Voltage	V_{DD}		2.85	3.30	3.63	V
Operating Temperature Range			-40		+105	°C

Electrical Characteristics

(V_{DD} = V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = 2.85V to 3.63V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Core Current	I_{CC}	Unprogrammed Device		10		mA
Supply Current (During Flash Write)	I_{CCFW}			15		mA
Brownout Voltage	V_{BO}	Monitors V_{CCO}	1.85	2.0	2.1	V
Brownout Hysteresis	V_{BOH}	Monitors V_{CCO}		50		mV
1.8V Internal Regulator	V_{BYP18}	(Note 2)	1.77	1.85	1.93	V
Core Clock Frequency	f_{MOSC_CORE}	T_A = +25°C		16		MHz
Clock Error	f_{ERR}		-2		+2	%
IDAC						
IDAC Resolution	$IDAC_{RES}$		12			Bits
Full-Scale Range	IFS2			2		mA
	IFS25			25		
	IFS50			50		
	IFS100			100		
	IFS200			200		
Maximum Differential Nonlinearity	$IDAC_{DNL}$	IFS200		±1		LSB
Integral Nonlinearity	$IDAC_{INL}$	IFS200	-10	±4	+17	LSB
Gain Error	G_{ERR}	IFS200, T_A = +25°C			±2	%FS
Gain Error Tempco	G_{ERRTC}	IFS200		200		ppm/°C
Offset Error	$IDAC_{OFF}$	IFS200, T_A = +25°C	-1800	-1000	0	µA
Offset Error Tempco	$IDAC_{OFFTC}$	IFS200		7500		nA/°C
Output-Compliance Range	V_{OCR}	IFS200, $\overline{V}_{CCDAC}$ = V_{DD}			V_{CCDAC} – 0.8	V
Output Resistance	R_{OUT}	IFS200		0.25		MΩ
Slew Rate	SR	IFS200		10		mA/µs
V_{CCDAC} Range	V_{CCDAC_RANGE}		2.1		V_{DD}	V
GPIO						
Output-Logic Low	V_{OL}	I_{OL} = 4mA (Note 2)			0.4	V
Output-Logic High	V_{OH}	I_{OH} = -4mA (Note 2)	V_{DD} - 0.5			V
Pullup Current	I_{PU}	V_{PIN} = 0V		60		µA
Input-Logic Low	V_{IL}	Except SCL and SDA Pins	-0.3		+0.3 x V_{DD}	V
Input-Logic High	V_{IH}	Except SCL and SDA Pins	0.7 x V_{DD}		V_{DD} + 0.3	V
GPIO Drive Strength	R_{HI}	(Note 3)			55	Ω
Pin Leakage	I_{LKG}	For Lx, IDACx pins	-5		+5	µA
		For all other GPIO pins	-1		+1	

Electrical Characteristics (continued)

(V_{DD} = V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = 2.85V to 3.63V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC						
ADC Resolution	ADC_{RES}		16			Bits
ADC Noise	ADC_{NOISE}			16		LSB
ADC Integral Nonlinearity	ADC_{INL}	(Note 3)		±10		LSB
ADC Differential Nonlinearity	ADC_{DNL}	V_{REF} = 2.428V (Note 3)			±1	LSB
ADC Offset Error	V_{OFFSET}	After offset calibration at T_A = +25°C and V_{DD} = 3.3V, V_{REF} = 2.428V (Note 3)		±3	±6	LSB
ADC Gain Error	V_{GE}	After gain calibration at T_A = +25°C and V_{DD} = 3.3V, V_{REF} = 2.428V (Note 3)		±6	±22	LSB
ADC Sample Rate	f_{SAMPLE}	(Note 4)			500	ksps
Acquisition Time	t_{ACQ}	(Note 4)	0.18		2	µs
Input-Voltage Range (Operating Condition)	V_{AIN}	Unipolar	0		V_{REF}	V
		Bipolar, Range = 0	$-V_{REF}/2$		$+V_{REF}/2$	
		Bipolar, Range = 1	$-V_{REF}$		$+V_{REF}$	
ADC Input Capacitance	C_{IN_ADC}			6		pF
ADC Internal-Reference Voltage	ADC_{REFACC}			2.428		V
ADC Reference Startup Time	$ADC_{STARTUP}$	V_{REF} = 2.428V			11	ms
ADC Operating Current	I_{ADC}			10		mA
ADC Reference-Temperature Stability	$ADC_{REF-TEMPSTB}$	V_{DD} = 3.3V, V_{REF} = 2.428V	-0.62		0.62	%
ADC Reference-Voltage Stability	$ADC_{REFVSTB}$	Referenced to 25°C, V_{REF} = 2.428V	-0.12		0.12	%
ADC Reference-Load Current	$ADC_{REFLOAD}$	Reference buffer = 2.428V			0.5	mA
		Reference buffer = 2.0V		2		
SAMPLE AND HOLD						
Input-Voltage Range (Operating Condition)	V_{SHP}		0		1	V
Input Capacitance	C_{IN_SH}			5		pf
Sampling Error	ERRSH	Sample Time = 300ns & Driven with ≥ 10µA current going through 1K		±5		%
Offset	SH_{OFF}			±1		mV

Electrical Characteristics (continued)

(V_{DD} = V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = 2.85V to 3.63V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DELTA-SIGMA DAC						
DAC Resolution	DAC_{RES}		16			Bits
DAC Frequency	f_{DAC}	At 50% duty cycle (Note 3)		8		MHz
PLA						
Input-to-Output Propagation Delay	t_{PD_PLA}	(Note 4)			80	ns
Inrush Control						
On-Resistance Inrush FET	R_{ON_INRUSH}	T_A = +25°C, V_{DD} = 3.3V (Note 3)		0.09	0.11	Ω
Inrush Current Limit	I_{ST}	Startup	75	150	275	mA
Maximum FETOUT Current	$I_{FETOUT-CONT}$				2	A
BUCK DC-DC CONVERTER (Note 5)						
Regulator Output Voltage	V_{OUT}	I_{OUT} = 0mA	1		V_{DD}	V
Startup Current	$I_{STARTUP}$	Discontinuous mode, V_{OUT} = 1.8V,		100		mA
Maximum Load Current	I_{CONT}	Continuous mode, V_{OUT} = 1.8V, I_{LIMIT} is disabled		1500		mA
Short-Circuit Current Limit	I_{LIMIT}	When enabled		1200		mA
LX pFET On-Resistance	R_{ON_PFET}	T_A = +25°C, V_{DD} = 3.3V (Note 3)		100	120	mΩ
LX nFET On-Resistance	R_{ON_NFET}	T_A = +25°C, V_{DD} = 3.3V (Note 3)		75	90	mΩ
Switching Frequency	f_{SW}	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 400mA		3.5		MHz
Output-Voltage Ripple	V_{OUT_RIPPLE}	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 400mA		±15		mV
DC Load Regulation	I_{LDR}	V_{IN} = 3.3V, V_{OUT} = 1.8V, ΔI_{OUT} = 100mA to 600mA		±0.25		%
DC Line Regulation	I_{LNR}	ΔV_{IN} = 2.97V to 3.47V, V_{OUT} = 1.8V, I_{OUT} = 400mA		±0.15		%
Efficiency	η	V_{IN} = 3.3V, V_{OUT} = 1.8V, Low Load, I_{OUT} = 400mA		90		%
		V_{IN} = 3.3V, V_{OUT} = 1.8V, High Load, I_{OUT} = 1000mA		85		

Electrical Characteristics (continued)

(V_{DD} = V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = 2.85V to 3.63V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST DC-DC CONVERTER (Note 6)						
Regulator Output Voltage	V_{OUT}		V_{DD} + 0.1	3.8	4.0	V
Startup Current	$I_{STARTUP}$	Discontinuous mode, V_{OUT} = 3.8V		30		mA
Load Current	I_{LOAD}	Continuous mode, V_{OUT} = 3.8V		200		mA
LX pFET On-Resistance	R_{ON_PFET}	T_A = +25°C, V_{DD} = 3.3V (Note 3)		100	120	mΩ
LX nFET On-Resistance	R_{ON_NFET}	T_A = +25°C, V_{DD} = 3.3V (Note 3)		75	90	mΩ
Switching Frequency	f_{SW}	V_{IN} = 3.3V, V_{OUT} = 3.8V, I_{OUT} = 200mA		1.4		MHz
Output-Voltage Ripple	V_{OUT_RIPPLE}	V_{IN} = 3.3V, V_{OUT} = 3.8V, I_{OUT} = 200mA		30		mV
DC Load Regulation	I_{LDR}	V_{IN} = 3.3V, V_{OUT} = 3.8V, ΔI_{OUT} = 100mA to 200mA, PI Enabled		±0.25		%
DC Line Regulation	I_{LNR}	ΔV_{IN} = 2.97V to 3.47V, V_{OUT} = 3.8V, I_{OUT} = 200mA, PI Enabled		±0.25		%
Efficiency	η	V_{IN} = 3.3V, V_{OUT} = 3.8V, Low Load, I_{OUT} = 100mA		90		%
TEC CONTROLLER						
Control Error	TEC_{ERR}	After 3-point temperature calibration, DS4835ZGTL+, DS4835RGTL+ and DS4835MGTL+ (Refer to the *Ordering Information* table) (Note 7)		±4		LSB
		DS4835JGTL+ (Refer to the *Ordering Information* table) (Note 7)		±25		LSB
		DS4835VGTL+ and DS4835P-GTL+ (Refer to the *Ordering Information* table) (Note 7)		±125		LSB
Maximum Output Voltage	V_{MAX}	(Note 8)		2.5		V
Maximum Current	I_{MAX}			1.5		A
Switching Frequency	f_{SW}	Duty cycle 2% to 98% (Note 4)	1.96	2	2.04	MHz
Current Monitor Accuracy	OCM_{ACC}	I_{TEC} = 0.2A to 1.5A in 3 selectable ranges, after two point calibration		±10		%

Electrical Characteristics (continued)

(V_{DD} = V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = 2.85V to 3.63V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE MEASUREMENT						
Internal Temperature-Measurement Error	INT_TEMPERROR	With 128 samples internal average, V_{DD} = 3.3V (Note 3)	-3		+3	°C
Flash						
Flash Mass-Erase Time	t_{ME}	Mass erase (Notes 4 and 9)			26	ms
Flash Page-Erase Time	t_{PE}	Page erase (Notes 4 and 9)			26	ms
Write Time	t_{WRITE}	Per word time (Notes 4, 9, and 10)			40	µs
Flash Endurance	n_{FLASH}	T_A = +25°C (Note 6)	20,000			Write Cycles
Data Retention	t_{RET}	T_A = +25°C (Note 6)	100			Years
3-WIRE MASTER						
SCL_3W Clock Frequency	f_{SCLOUT}	(Note 4)		1000		kHz
SCL_3W Duty Cycle	t_{3WDC}	(Note 4)		50		%
SDA_3W Setup Time	t_{DS}	(Note 4)	60			ns
SDA_3W Hold Time	t_{DH}	(Note 4)	60			ns
CS_3W Pulse-Width Low	t_{CSW}	(Note 4)	500			ns
CS_3W Leading Time before First SCL_3W Edge	t_L	(Note 4)	500			ns
CS_3W Trailing Time after Last SCL_3W Edge	t_T	(Note 4)	500			ns
SDA_3W, SCL_3W Pin Capacitance	C_{B3W}			10		pF
I²C SLAVE						
SCL Clock Frequency	f_{SCL}		0		400	kHz
Input-Logic High	V_{I2C_IH}		2		5.5	V
Input-Logic Low	V_{I2C_IL}		-0.3		+0.8	V
Output-Logic Low	V_{I2C_OL}	I_{OL} = 4mA (Note 2)			0.4	V
SCL, SDA Leakage	IL_{I2C}				±1	µA
Bus Free-Time between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs

Electrical Characteristics (continued)

(V_{DD} = V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = 2.85V to 3.63V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time (Receive)	t_{HD_DAT}		0			ns
Data Hold Time (Transmit)	t_{HD_DAT}		300			ns
Data Setup Time	t_{SU_DAT}		100			ns
Start Setup Time	t_{SU_STA}		0.6			µs
SDA and SCL Rise Time	t_R	(Note 11)			300	ns
SDA and SCL Fall Time	t_F	(Note 11)			300	ns
Stop Setup Time	t_{SU_STO}		0.6			µs
SCL, SDA Capacitive Loading	C_B	(Note 12)			400	pF
I²C MASTER						
MSCL Clock Frequency	f_{SCL}	(Note 4)			1	MHz
Bus Free-Time Between STOP and START Conditions	t_{BUF}	(Notes 4 and 13)	1.3			µs
Hold Time (Repeated) START Condition	t_{HD_STA}	(Notes 4 and 13)	0.6			µs
Low Period of MSCL	t_{LOW}	(Notes 4 and 13)	1.3			µs
High Period of MSCL	t_{HIGH}	(Notes 4 and 13)	0.6			µs
Data Hold Time (Receive)	t_{HD_DAT}	(Notes 4 and 13)	0			ns
Data Hold Time (Transmit)	t_{HD_DAT}	(Notes 4 and 13)	300			ns
Data Setup Time	t_{SU_DAT}	(Notes 4 and 13)	100			ns
Start Setup Time	t_{SU_STA}	(Notes 4 and 13)	0.6			µs
MSDA and MSCL Rise Time	t_R	(Note 11)			300	ns
MSDA and MSCL Fall Time	t_F	(Note 11)			300	ns
Stop Setup Time	t_{SU_STO}	(Notes 4 and 13)	0.6			µs
MSCL, MSDA Capacitive Loading	C_B	(Note 11)			400	pF
SPI						
Maximum SPI Master Operating Frequency	$1/t_{MSPICK}$	(Note 4)	$f_{MOSC-CORE}/2$			MHz
Maximum SPI Slave Operating Frequency	$1/t_{SSPICK}$	(Note 4)	$f_{MOSC-CORE}/4$			MHz
SPI I/O Rise/Fall Time	t_{SPI_RF}	C_L = 15pF, Pull up = 560Ω		25		ns

Electrical Characteristics (continued)

(V_{DD} = V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = 2.85V to 3.63V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MSPI_CK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	(Note 4)	$t_{MSPICK}/2-t_{SPI\_RF}$			ns
MSPI_MOSI Output Hold After MSPI_CK Sample Edge	t_{MOH}	(Note 4)	$t_{MSPICK}/2-t_{SPI\_RF}$			ns
MSPI_MOSI Output Valid to MSPI_CK Sample Edge (MSPI_MOSI Setup)	t_{MOV}	(Note 4)	$t_{MSPICK}/2-t_{SPI\_RF}$			ns
MSPI_MISO Input Valid to MSPI_CK Sample Edge (MSPI_MISO Setup)	t_{MIS}	(Note 4)	$2t_{SPI\_RF}$			ns
MSPI_MISO Input to MSPI_CK Sample Edge Rise/Fall Hold	t_{MIH}			0		ns
MSPI_CK Inactive to MSPI_MOSI Inactive	t_{MLH}	(Note 4)	$t_{MSPICK}/2-t_{SPI\_RF}$			ns
SSPI_CK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SSPICK}/2$		ns
SSPI_CSEL Active to First Shift Edge	t_{SSE}	(Note 4)	t_{SPI_RF}			ns
SSPI_MOSI Input to SSPI_CK Sample Edge Rise/Fall Setup	t_{SIS}	(Note 4)	t_{SPI_RF}			ns
SSPI_MOSI Input from SSPI_CK Sample Edge Transition Hold	t_{SIH}	(Note 4)	t_{SPI_RF}			ns
SSPI_MISO Output Valid after SSPI_CK Shift Edge Transition	t_{SOV}	(Note 4)			$2t_{SPI\_RF}$	ns
SSPI_CSEL Inactive	t_{SSH}	(Note 4)	$t_{MSPICK} + t_{SPI\_RF}$			ns
SSPI_CK Inactive to SSPI_CSEL Rising	t_{SD}	(Note 4)	t_{SPI_RF}			ns
SSPI_MISO Output Disabled After SSPI_CSEL Edge Rise	t_{SLH}	(Note 4)			$2t_{MSPICK} + 2t_{SPI\_RF}$	ns
Supply Voltage Monitoring (SVM)	V_{SVM}	SVTH = 4 (Note 14) for DS4835ZGTL+, DS4835RGTL+, DS4835PGTL+, and DS4835EGTL+	2.65	2.88	2.99	V

Electrical Characteristics (continued)

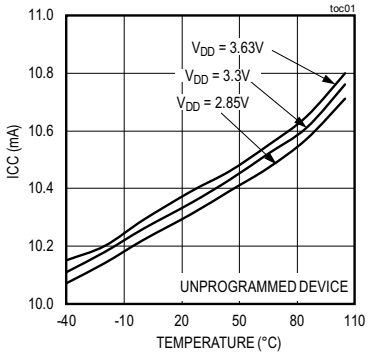
(V_{DD} = V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = 2.85V to 3.63V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C) (Note 1)

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.
Note 2: All voltages are referenced to GND. Currents entering the IC are specified positive and currents exiting the IC are negative.
Note 3: Guaranteed by design.
Note 4: Minimum and maximum timings depend upon $f_{MOSC-CORE}$ error.
Note 5: With input capacitors 0.1µF and 10µF, output capacitors 0.1µF and 10µF, and inductor part no DFE201612P-1ROM. Refer to Table 1 for recommended SFRs settings.
Note 6: With input capacitors 0.1µF and 10µF, output capacitors 0.1µF and 10µF, and inductor part no DFE201612P-1ROM. Refer to Table 2 for recommended SFRs settings.
Note 7: LSBs are based on 16-bit ADC.
Note 8: Voltage = PV_{CC} - I_{TEC} x (R_{ON_PFET} + R_{ON_NFET}).
Note 9: This parameter is set by the internal oscillator and is guaranteed by the oscillator specs.
Note 10: Programming does not include overhead associated with the utility ROM interface.
Note 11: CB—total capacitance of one bus line in pF. Rise time = CB × R_{PU}.
Note 12: The maximum bus capacitance allowable can vary from this value depending on the actual operating voltage and frequency of the application.
Note 13: f_{SCL} must be programmed properly using MTSPECn register for 400kHz.
Note 14: Refer to the *DS4835 User Guide* for a SVTH description.

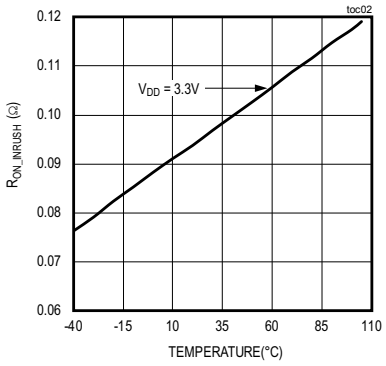
Typical Operating Characteristics

(V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = V_{CCDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

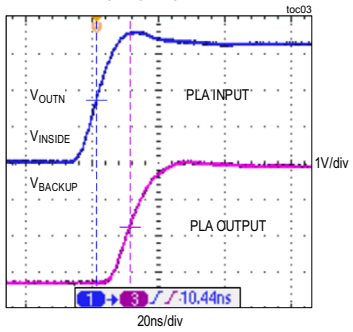
SUPPLY CURRENT vs. TEMPERATURE



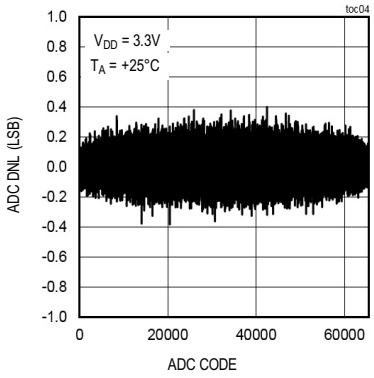
ON-RESISTANCE INRUSH FET vs. TEMPERATURE



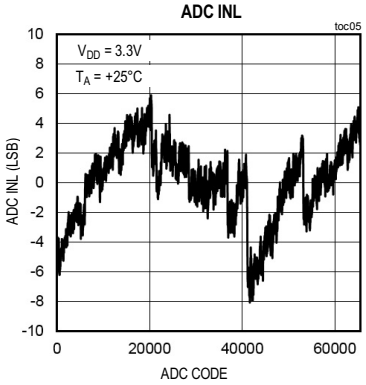
PLA INPUT-TO-OUTPUT PROPAGATION DELAY



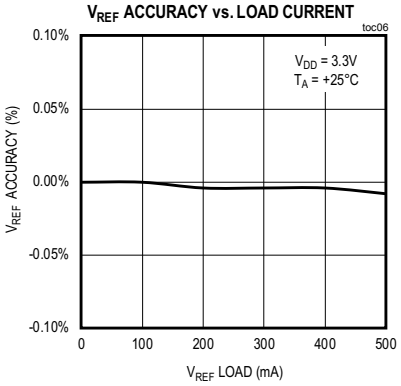
ADC DNL



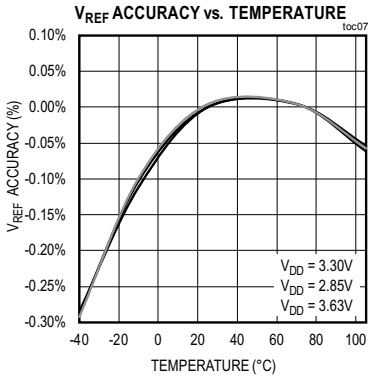
ADC INL



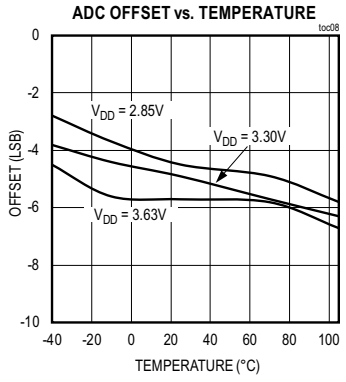
VREF ACCURACY vs. LOAD CURRENT



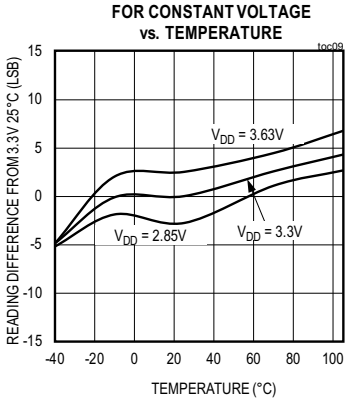
VREF ACCURACY vs. TEMPERATURE



ADC OFFSET vs. TEMPERATURE



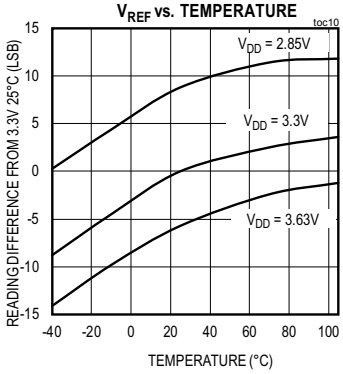
ADC READING DIFFERENCE FOR CONSTANT VOLTAGE vs. TEMPERATURE



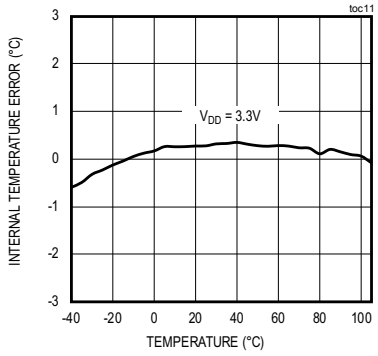
Typical Operating Characteristics (continued)

(V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = V_{CCDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

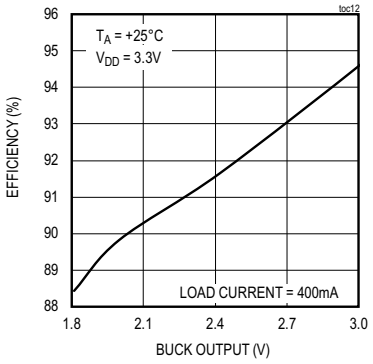
ADC READING DIFFERENCE FOR CONSTANT VOLTAGE V_{REF} vs. TEMPERATURE



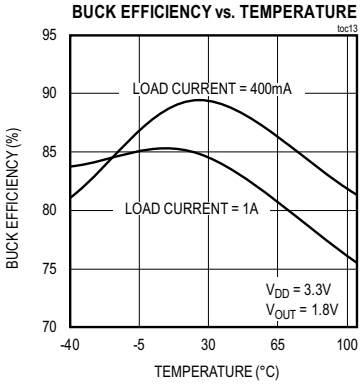
INTERNAL TEMPERATURE ERROR vs. TEMPERATURE



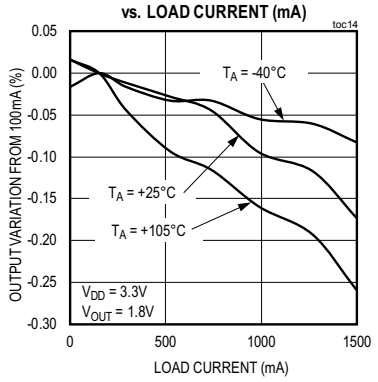
EFFICIENCY vs. BUCK OUTPUT



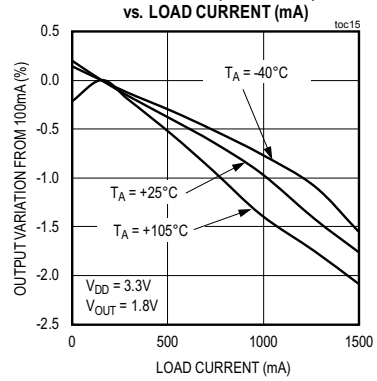
BUCK EFFICIENCY vs. TEMPERATURE



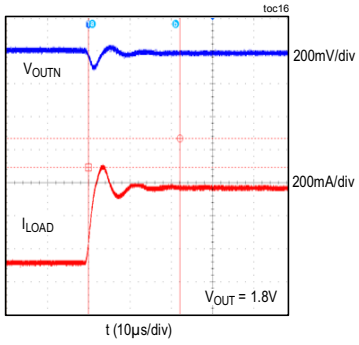
OUTPUT VARIATION 100mA LOAD (WITH PI) vs. LOAD CURRENT (mA)



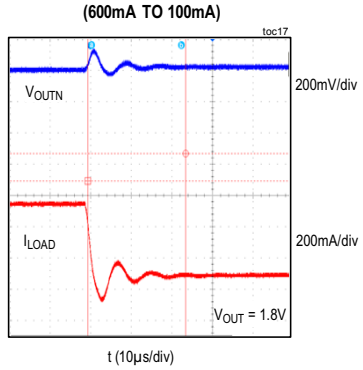
OUTPUT VARIATION 100mA LOAD (WITHOUT PI) vs. LOAD CURRENT (mA)



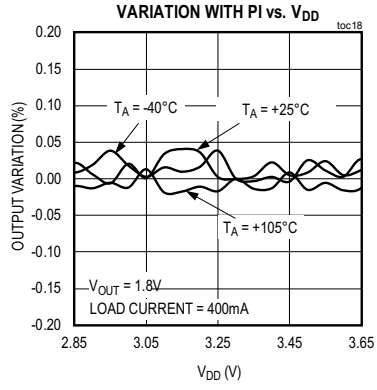
POSTIVE LOAD TRANSIENT 100mA TO 600mA



NEGATIVE LOAD TRANSIENT (600mA TO 100mA)



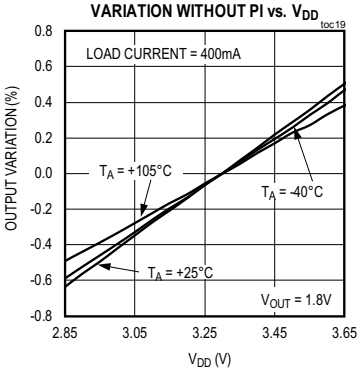
BUCK OUTPUT VARIATION WITH PI vs. V_{DD}



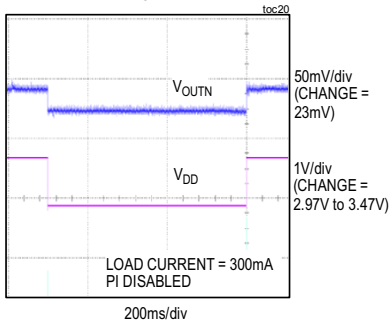
Typical Operating Characteristics (continued)

(V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = V_{CCDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

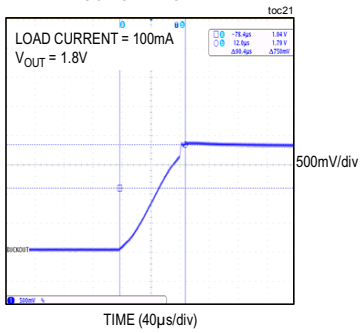
BUCK OUTPUT VARIATION WITHOUT PI vs. V_{DD}



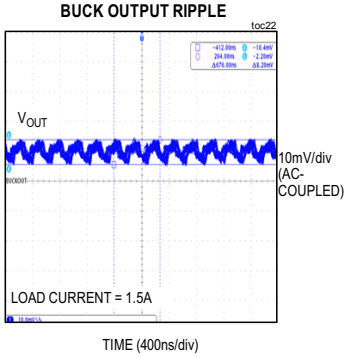
BUCK LINE TRANSIENT vs. TIME



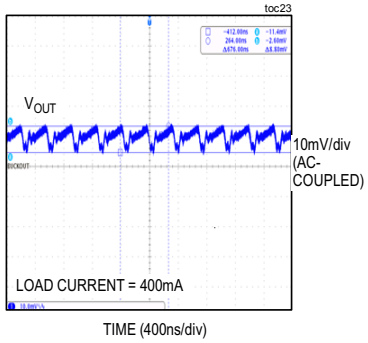
BUCK STARTUP TIME



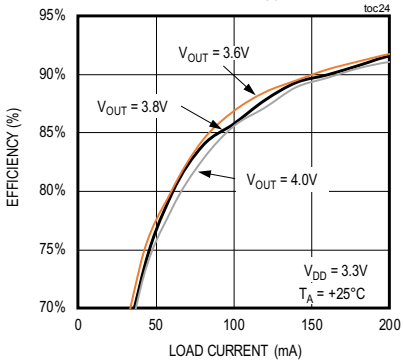
BUCK OUTPUT RIPPLE



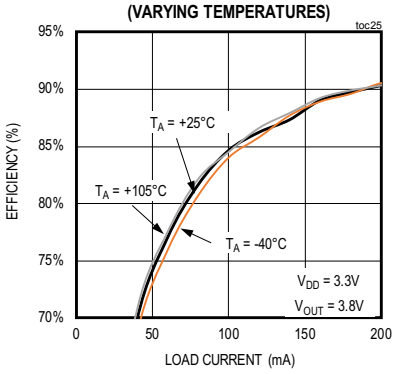
BUCK OUTPUT RIPPLE



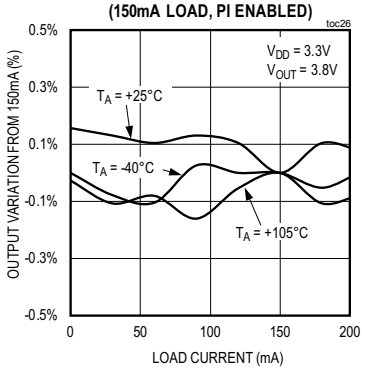
BOOST EFFICIENCY vs. LOAD CURRENT (VARYING V_{OUT})



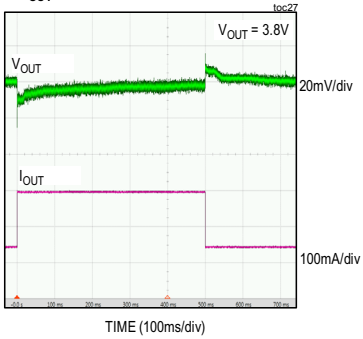
BOOST EFFICIENCY vs. LOAD CURRENT (VARYING TEMPERATURES)



BOOST OUTPUT VARIATION (150mA LOAD, PI ENABLED)



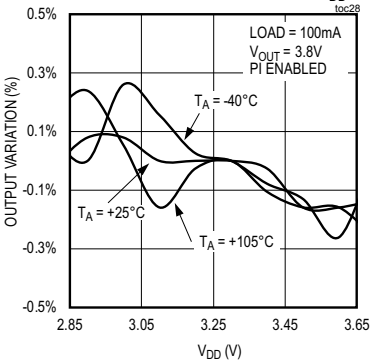
LOAD TRANSIENT RESPONSE (I_{OUT} = 50mA TO 200mA, PI ENABLED)



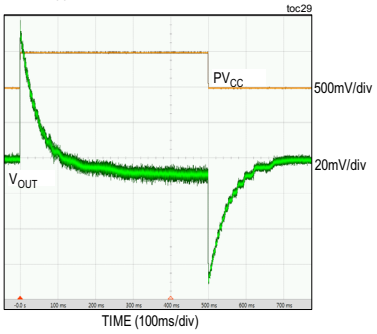
Typical Operating Characteristics (continued)

(V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = V_{CCDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

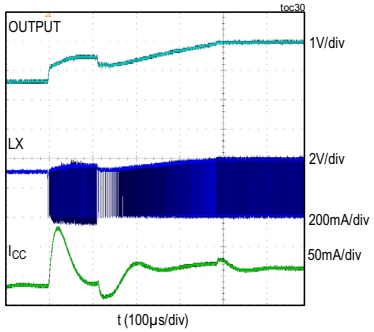
BOOST OUTPUT VARIATION vs. V_{DD}



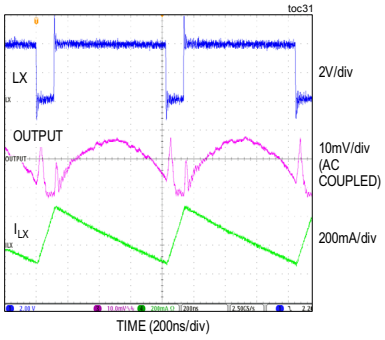
LINE TRANSIENT RESPONSE
(V_{OUT} = 3.8V, I_{OUT} = 50mA, PV_{CC} = 2.97V TO 3.47V, PI ENABLED)



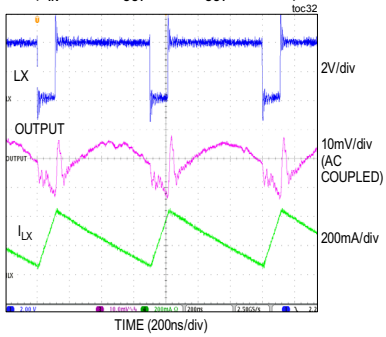
BOOST STARTUP



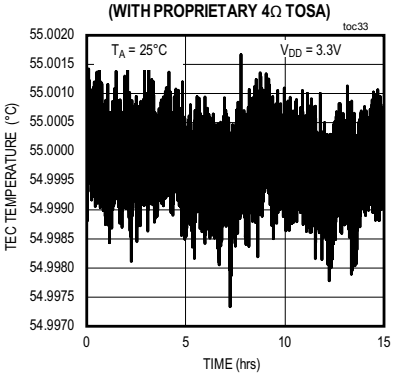
BOOST SWITCHING WAVEFORMS
(V_{IN} = 3.3V, V_{OUT} = 3.8V, I_{OUT} = 50mA)



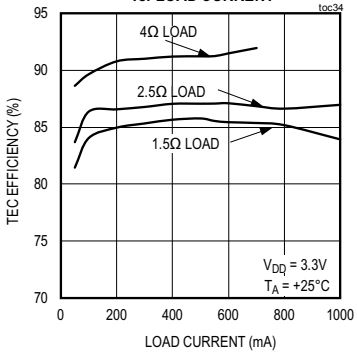
BOOST SWITCHING WAVEFORMS
(V_{IN} = 3.3V, V_{OUT} = 3.8V, I_{OUT} = 200mA)



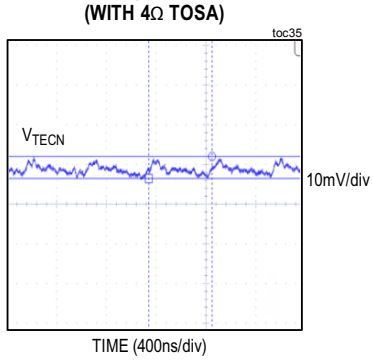
TEC TEMPERATURE STABILITY WITH TIME AT 25°C (WITH PROPRIETARY 4Ω TOSA)



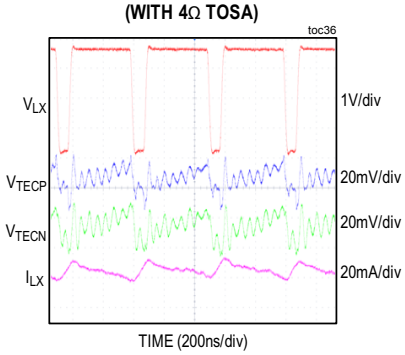
TEC EFFICIENCY vs. LOAD CURRENT



V_{TEC} Ripple (WITH 4Ω TOSA)



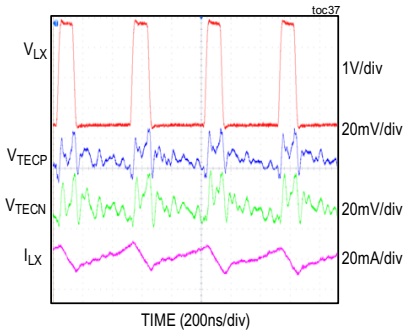
TEC SWITCHING WAVEFORMS-HEATING (WITH 4Ω TOSA)



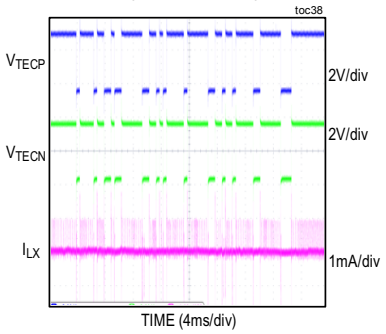
Typical Operating Characteristics (continued)

(V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = V_{CCDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

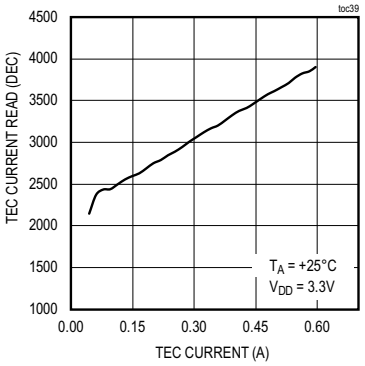
TEC SWITCHING WAVEFORMS-COOLING (WITH 4Ω TOSA)



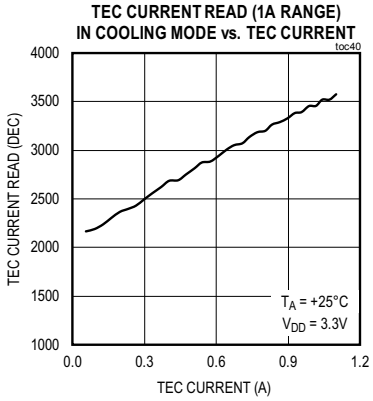
TEC SWITCHING WAVEFORMS GOING BETWEEN COOLING AND HEATING MODE (WITH 4Ω TOSA)



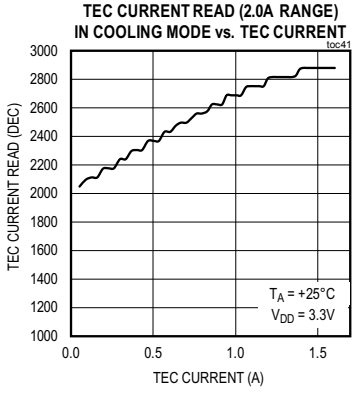
TEC CURRENT READ (500mA RANGE) IN COOLING MODE vs. TEC CURRENT



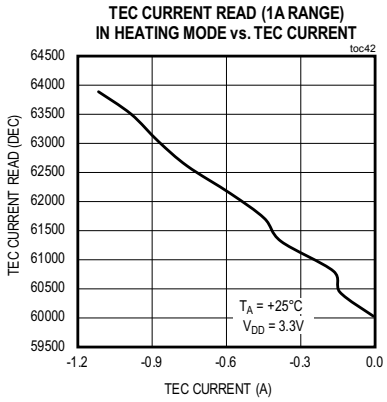
TEC CURRENT READ (1A RANGE) IN COOLING MODE vs. TEC CURRENT



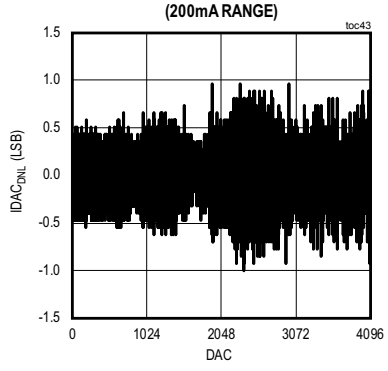
TEC CURRENT READ (2.0A RANGE) IN COOLING MODE vs. TEC CURRENT



TEC CURRENT READ (1A RANGE) IN HEATING MODE vs. TEC CURRENT



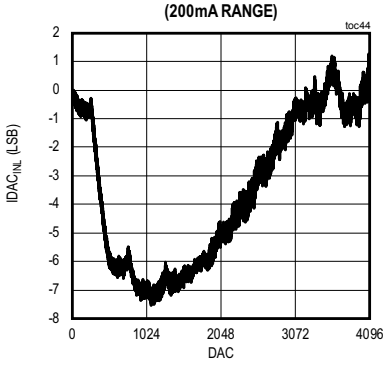
IDAC DNL vs. DAC SETTING (200mA RANGE)



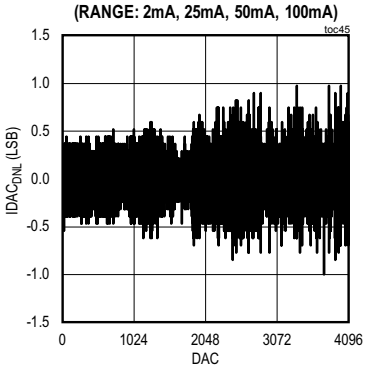
Typical Operating Characteristics (continued)

(V_{CCI} = V_{CCO} = PV_{CC1} = PV_{CC2} = PV_{CC3} = PV_{CC4} = V_{CCDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

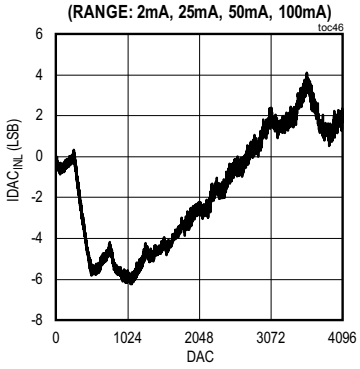
IDAC INL vs. DAC SETTING
(200mA RANGE)



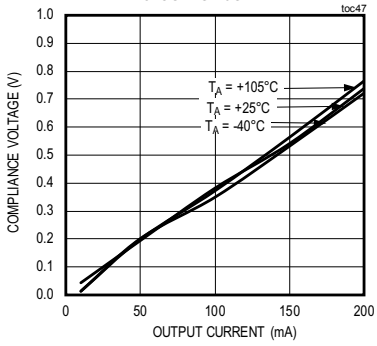
IDAC DNL vs. DAC SETTING
(RANGE: 2mA, 25mA, 50mA, 100mA)



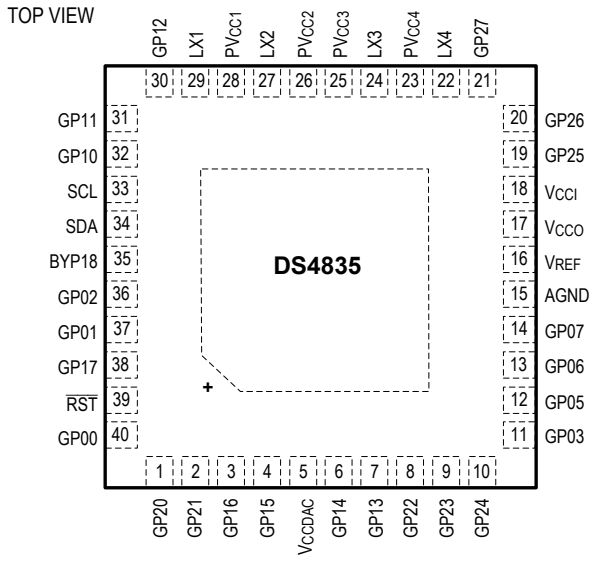
IDAC INL vs. DAC SETTING
(RANGE: 2mA, 25mA, 50mA, 100mA)



IDAC COMPLIANCE VOLTAGE
vs. OUTPUT CURRENT



Pin Configurations



40-PIN TQFN
(5mm x 5mm x 0.8mm)

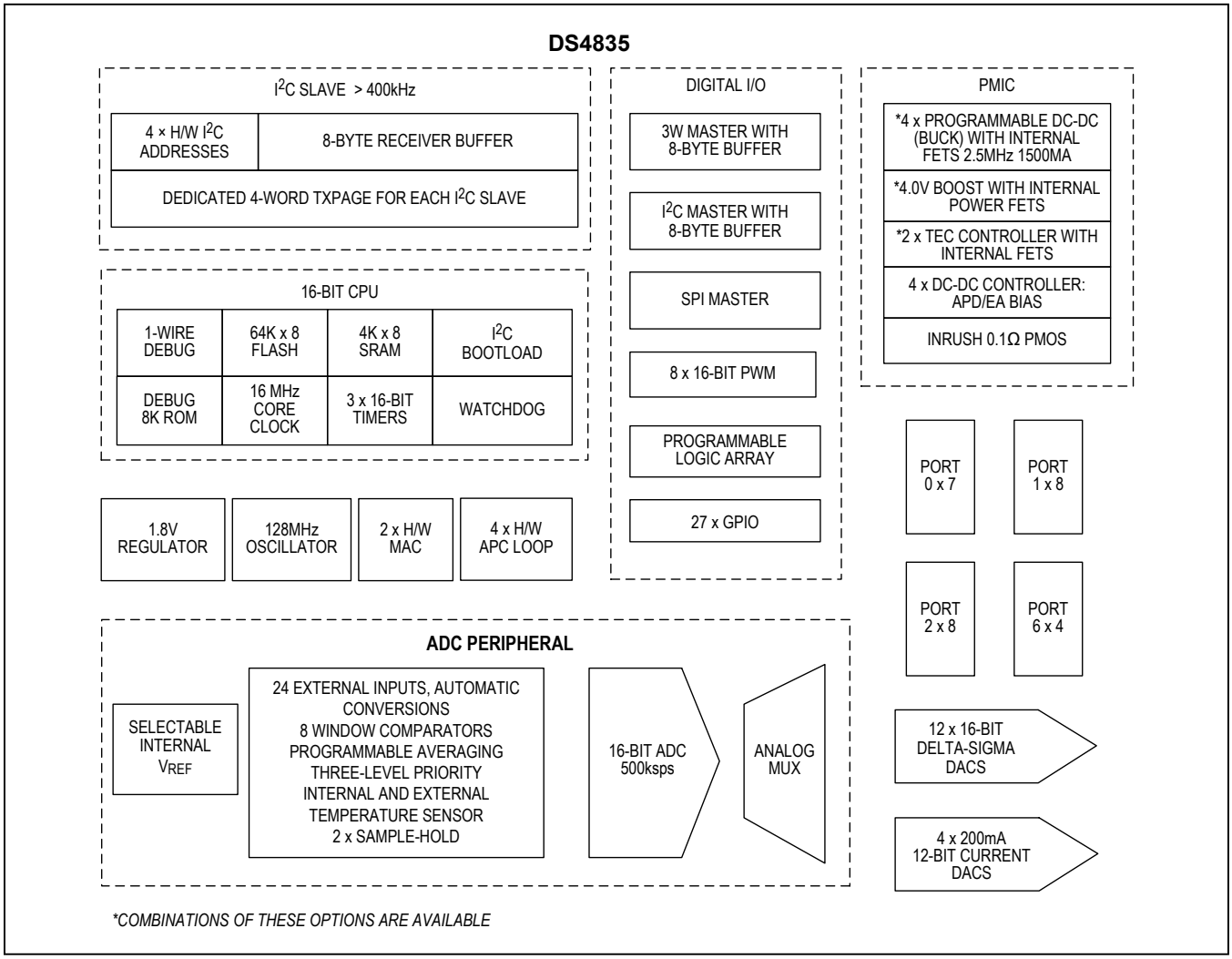
Pin Description

PIN	NAME	FUNCTION
PUSH-PULL IO		
1	GP20	GPIO20, ADC16, PLAOUT[4], DS_DAC0, APD4, PWM0, SHP0
2	GP21	GPIO21, ADC17, PLAOUT[5], DS_DAC1, PWM1, SHN0
3	GP16	GPIO16, ADC14, IDAC4, DS_DAC11, SHEN0
4	GP15	GPIO15, ADC13, IDAC3, DS_DAC10, SHEN0
6	GP14	GPIO14, ADC12, IDAC2, DS_DAC9, MSDA1 ALT
7	GP13	GPIO13, ADC11, IDAC1, DS_DAC8, SSPI_MISO, MSPI_MISO, MSDA1 ALT
8	GP22	GPIO22, ADC18, PLAOUT[6], DS_DAC2, APD1, PWM2
9	GP23	GPIO23, ADC19, PLAOUT[7], DS_DAC3, APD2, PWM3
10	GP24	GPIO24, ADC20, PLAIN[4], DS_DAC4, PWM4
19	GP25	GPIO25, ADC21, PLAIN[5], DS_DAC5, PWM5
20	GP26	GPIO26, ADC22, PLAIN[6], DS_DAC6, PWM6, SHP1
21	GP27	GPIO27, ADC23, PLAIN[7], DS_DAC7, PWM7, SHN1
30	GP12	GPIO12, ADC10, CS_3W, FB2, SSPI_CSEL, MSDA1 ALT
31	GP11	GPIO11, MSCL1, SCL_3W, SSPI_CK, MSPI_CK
32	GP10	GPIO10, MSDA1, SDA_3W, SSPI_MOSI, MSPI_MOSI
38	GP17	GPIO17, ADC15, PLAIN[0], TSENS, APD3, SHEN0

Pin Description (continued)

PIN	NAME	FUNCTION
POWER		
5	V_{CCDAC}	V_{CCDAC}, ADC4, FB1
15	AGND	Analog Ground
16	V_{REF}	Reference Voltage output. Connect 4.7µF capacitor.
17	V_{CCO}	Supply OUT
18	V_{CCI}	Supply IN
23	PV_{CC4}	Power Supply for TEC2-N / Boost 3 / Buck 4
25	PV_{CC3}	Power Supply for DCDC3
26	PV_{CC2}	Power Supply for DCDC2
28	PV_{CC1}	Power Supply for DCDC1
35	BYP18	1.8V Regulator
—	EP	Ground
OPEN DRAIN		
11	GP03	GPIO03, ADC3, PLAOUT[3], SHEN1, MSCL2
12	GP05	GPIO05, ADC5, PLAIN[1], SHEN0
13	GP06	GPIO06, ADC6, PLAIN[2]
14	GP07	GPIO07, ADC7, PLAIN[3], FB3
36	GP02	GPIO02, ADC2, PLAOUT[2], SHEN1, MSDA2
37	GP01	GPIO01, ADC1, PLAOUT[1], SHEN1
40	GP00	GPIO00, ADC0,PLAOUT[0], SHEN1
DC-DC		
22	LX4	Switch Output for DCDC4, GPI63, TECN2, ADC9
24	LX3	Switch Output for DCDC3, GPI62, TECP2
27	LX2	Switch Output for DCDC2, GPI61, TECN1, ADC8
29	LX1	Switch Output for DCDC1, GPI60, TECP1
5.5V TOLERANT I^2C PAD OD		
33	SCL	I^2C Slave Clock
34	SDA	I^2C Slave Data
OPEN DRAIN $\overline{RST}$ PAD		
39	$\overline{RST}$	Reset /1-Wire debug

Functional Diagram



Detailed Description

The following is an introduction to the primary features of the DS4835 Optical Microcontroller. More detailed description of the device features can be found in the *DS4835 User Guide*.

Core Architecture

The device employs a low-power, low-cost, high-performance, 16-bit RISC microcontroller with on-chip flash memory. It is structured on an advanced, 16 accumulator-based, 16-bit RISC architecture. Fetch and execution operations are completed in one cycle without pipelining since the instruction contains both the operation code and data. The highly efficient core is supported by 16 accumulators and a 32-level hardware stack, enabling fast subroutine calling and task switching. Data can be quickly and efficiently manipulated with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers can automatically increment/decrement following an operation, eliminating the need for software intervention.

Instruction Set

The instruction set is composed of fixed-length, 16-bit instructions that operate on registers and memory locations. The instruction set is highly orthogonal, allowing arithmetic and logical operations to use any register along with the accumulator. Special-function registers control the peripherals and are subdivided into register modules.

System Interrupts

Multiple interrupt sources are available to respond to internal and external events. The microcontroller architecture uses a single interrupt vector (IV) and single interrupt-service routine (ISR) design. For maximum flexibility, interrupts can be enabled globally, individually, or by module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the firmware-interrupt routine to avoid repeated interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, execution jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up, so if it is not changed to a different address, application firmware must determine whether a jump to 0000h came from a $\overline{\text{RST}}$ or interrupt source.

Once control has been transferred to the ISR, the interrupt identification register (IIR) can be used to determine which module was the source of the interrupt. The device contains seven peripheral modules, M0 to M6. Once the module that causes the interrupt is singled out, it can then be identified for the specific interrupt source and the software can take appropriate action. Interrupts are evaluated by application code allowing the definition of a unique interrupt priority scheme for each application. Interrupt sources are available from the watchdog timer, the ADC (including sample/holds and temperature sensor), fast comparators, the programmable timers, SVM, the I^2C compatible master and slave interface, 3-wire, master and slave SPI, PLAs, as well as all GPIO pins.

Memory Organization

The device incorporates several memory areas:

- 32K Words of flash memory for application program and constant data storage
- 2K Words of SRAM
- 4K Words of Utility ROM that contain a debugger and program loader
- 32-level stack memory for storage of program return addresses and application use

The memory is implemented with separate address spaces for program memory, data memory, and register space that also allows ROM, application code, and data memory into a single contiguous memory map. The device allows data memory to be mapped into program space, permitting code execution from data memory. In addition, program memory can be mapped into data space, permitting code constants to be accessed as data memory. Figure 1 shows the DS4835's memory map when executing from program memory space. Refer to the *DS4835 User Guide* for memory map information when executing from data or ROM space.

The incorporation of flash memory allows field upgrade of the firmware. Flash memory can be password protected with a 16-word key, denying access to program memory by unauthorized individuals.

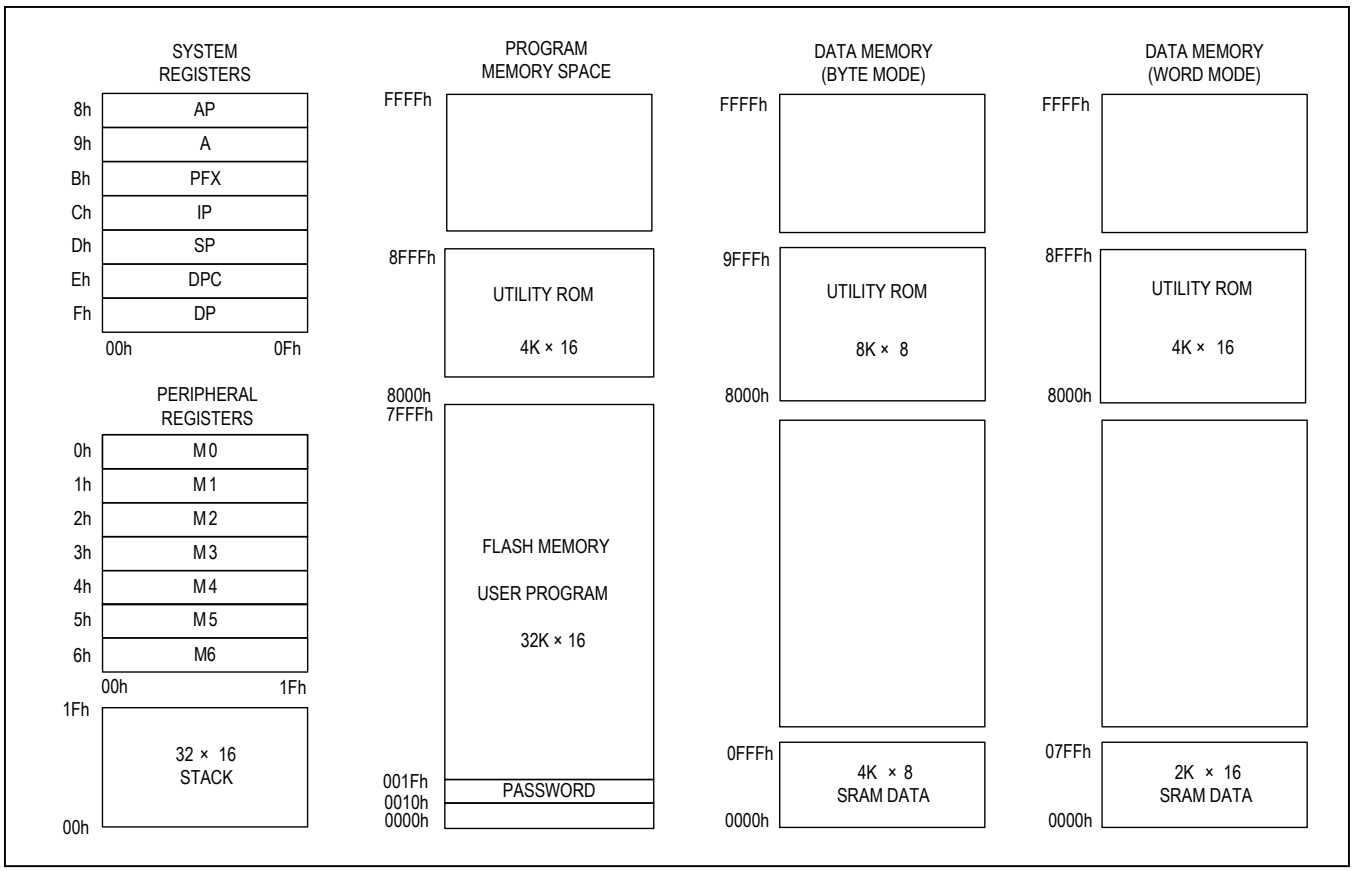


Figure 1. DS4835 Memory Map when Program is Executed from Flash Memory.

Memory

The DS4835 has both flash and SRAM memory.

- 32KW of the flash memory for program and data memory.
- 2KW of the SRAM memory for data memory.

Utility ROM

The utility ROM is a 4K word block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software. These include:

- In-system programming (bootstrap loader) over a 1-Wire loader (OWL) or I^2C compatible interfaces
- Callable routines for in-application flash programming

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of application code, or to one of the special routines mentioned. Routines within the utility ROM are firmware-accessible and can be called as subroutines by the application software.

Stack Memory

A 16-bit, 32-level internal stack provides storage for program return addresses. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The stack can also be used explicitly to store and retrieve data by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (1Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Programming

The microcontroller's flash memory can be programmed by one of two methods: in-system programming and in-application programming. These provide great flexibility in system design as well as reduce the life-cycle cost of the embedded system. Programming can be password protected to prevent unauthorized access to code memory.

In-System Programming

An internal bootstrap loader allows the device to be programmed over the OWL or I2C compatible interfaces. As a result, system software can be upgraded in-system, eliminating the need for a costly hardware retrofit when software updates are required. The programming source select (PSS) bits in the ICDF register determine which interface is used for boot-loading operation. The device supports OWL and I2C as an interface corresponding to bits 00 and 01 of PSS, respectively, as shown in Figure 2.

Password

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh.

A single password lock (PWL) bit is implemented in the device. When the PWL is set to 1 (power-on reset default) and the contents of the memory at addresses 0010h to 001Fh are any value other than all FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to 0, these utilities are fully accessible without the password. The password is automatically set to all 1's following a mass erase. Mass erase can be performed without password match.

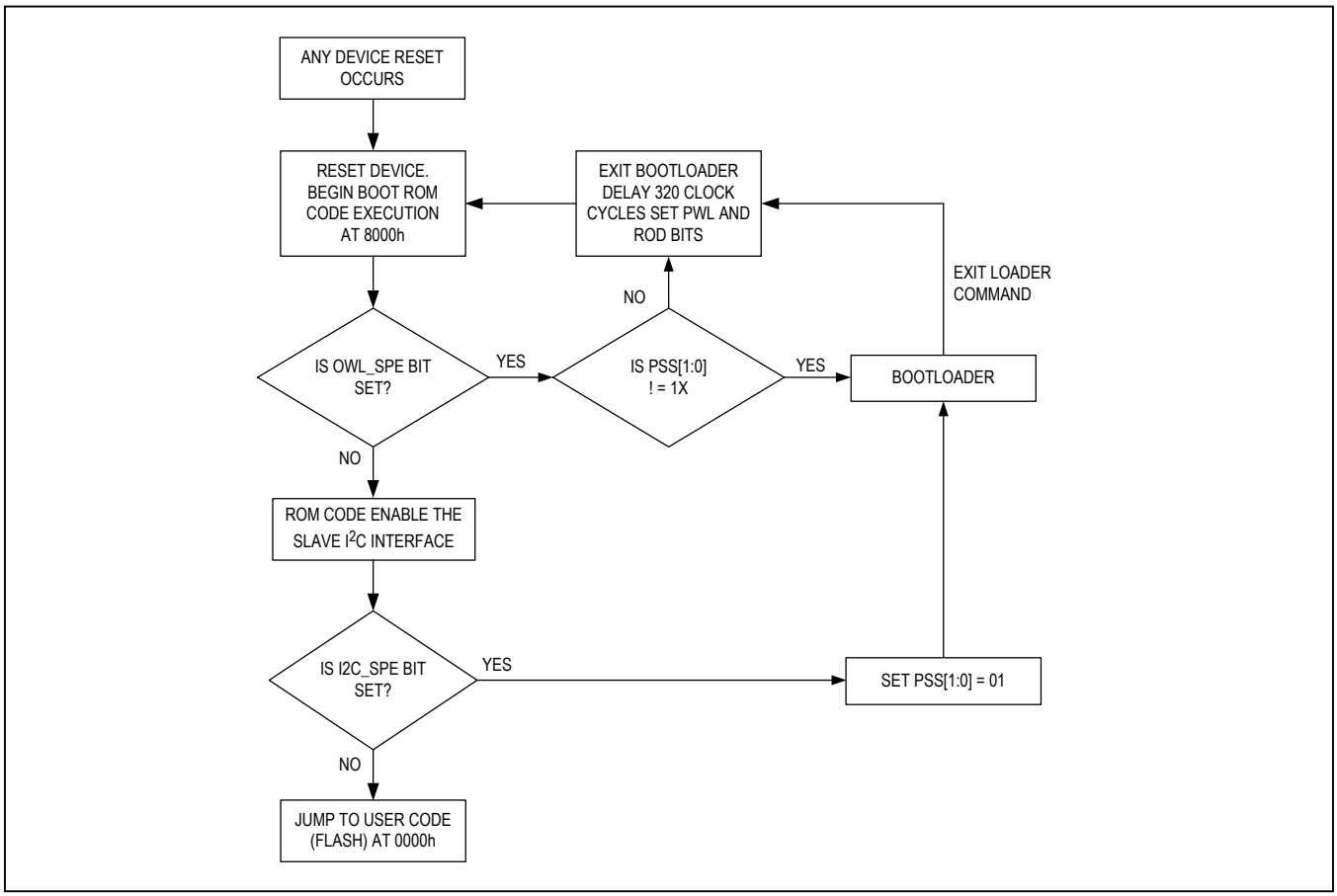


Figure 2. In-System Programming

System Timing

The device generates its 16MHz instruction clock (MOSC) and 128MHz clock for TEC, PWM, and DC-DC converters internally. On power-up, the oscillator's output, which cannot be accessed externally, is disabled until V_{DD} rises above V_{BO}. Once this threshold is reached, the output is enabled after approximately 3ms (t_{SU_MOSC}), clocking the device.

System Reset

The device features several sources that can be used to reset the DS4835.

Power-On Reset

An internal power-on reset (POR) circuit is used to enhance system reliability. This circuit forces the device to perform a POR whenever a rising voltage on V_{DD} climbs above V_{BO}. When this happens, the following events occur:

- All registers and circuits enter their reset state.
- The POR flag (WDCN.7) is set to indicate the source of the reset.
- Code execution begins at location 8000h when the reset condition is released.

Brownout Detect/Reset

The device features a brownout detect/reset function. Whenever the power monitor detects a brown-out condition (when $V_{DD} < V_{BO}$), it immediately issues a reset and stays in that state as long as V_{DD} remains below V_{BO}. Once V_{DD} voltage rises above V_{BO}, the device waits for t_{SU_MOSC} before returning to normal operation, also referred to as CPU state. If a brownout occurs during this t_{SU_MOSC}, the device again goes back to the brownout state. Otherwise, it enters into CPU state. In CPU state, the brownout detector is also enabled. On power-up, the device always enters brownout state first and then follows the above sequence. The reset issued by brownout is same as POR. Any action performed after POR also happens on brownout reset. All the registers cleared on POR are also cleared on brownout reset.

External Reset

Asserting the $\overline{RST}$ pin low causes the device to enter the reset state. Execution resumes at location 8000h after the $\overline{RST}$ pin is released. During normal operation, the DS4835 is placed into external reset when the $\overline{RST}$ pin is held low. The required duration of the logic 0 pulse depends upon whether the 1-Wire test access port (TAP) is enabled. If the TAP is enabled, the $\overline{RST}$ pin must be held low for approximately 150µs to initiate a reset. If the TAP is disabled, the $\overline{RST}$ pin must be held low for 4 system clock cycles to initiate a reset. Once the DS4835 enters reset mode, it remains in reset if the $\overline{RST}$ pin is held at logic 0. After the $\overline{RST}$ pin returns to logic 1, the processor exits reset within 12 clock cycles.

Watchdog Timer Reset

The watchdog timer provides a mechanism to reset the processor in the case of undesirable code execution. The watchdog timer is a hardware timer designed to be periodically reset by the application software. If the software operates correctly, the timer is reset before it reaches its maximum count. However, if undesirable code execution prevents a reset of the watchdog timer, the timer reaches its maximum count and resets the processor.

The watchdog timer is controlled through two bits in the WDCN register (WDCN[5:4] and WD[1:0]). Its timeout period can be set to one of the four programmable intervals ranging from 2^{12} to 2^{21} system clock (MOSC) periods (0.256ms to 0.131s). The watchdog interrupt occurs at the end of this timeout period, which is 512 MOSC clock periods, or approximately 32µs, before the reset. The reset generated by the watchdog timer lasts for 4 system clock cycles, which is 0.25µs. The software can determine if a reset is caused by a watchdog timeout by checking the watchdog timer reset flag (WTRF) in the WDCN register. Execution resumes at location 8000h following a watchdog timer reset. The watchdog reset has the same effect as the external reset as far as the reset values of all registers are concerned.

Internal System Reset

The host can issue an I^2C command (BBh) to slave address 34h to reset the communicating device. This reset has the same effect as the external reset as far as the reset values of all registers are concerned. Also, an internal system reset can occur when the in-system programming is done (ROD = 1). This reset has the same effect as the external reset as far as the reset values of all registers are concerned

Software Reset

The device UROM provides an option to software reset through the application program. The application program jumps to the UROM code, which generates the internal system reset. This reset has the same effect as the internal system reset.

TEC Controller

The DS4835 has two digital proportional (P), integral (I), and differential (D) control-based hardware TEC controllers with internal power FETs. The digital PID control loop has programmable values for the P, I, and D constants. The components of this loop are a 16-bit ADC, programmable digital TEC set-point, PID loop, feedback from thermistor with a low-temperature coefficient resistor connected to the V_{REF} and pulse-width modulation (PWM) that drives the internal FETs. Integration of the power FETs results in the need for only an external inductor and capacitor. On-chip FETs minimize external components and high switching frequency reduces the size of external components in the space constrained optical modules.

The ADC reference voltage available at the V_{REF} pin is used to create a voltage-divider network with the thermistor. For better performance, the AGND pin should have a Kelvin connection between TOSA ground and AGND.

The thermistor voltage is sampled by the ADC and used to adjust the set point for the TEC controller. The 16-bit TEC setpoint is one of the TEC SFRs. The TEC- voltage is internally sampled by the ADC. The TEC+ voltage can be applied to an ADC input to determine the voltage generated across the TEC. One side of the TEC is driven by the digital PWM output from the PID controller while the other side of the TEC is connected to ground or PV_{CC} depending upon heating or cooling mode for the TEC (dynamically switched by the controller). The transition from cooling to heating mode is well-controlled as the digital PID loop has 16-bits of resolution. The device also provides an internal TEC current monitor with 4 configurable ranges.

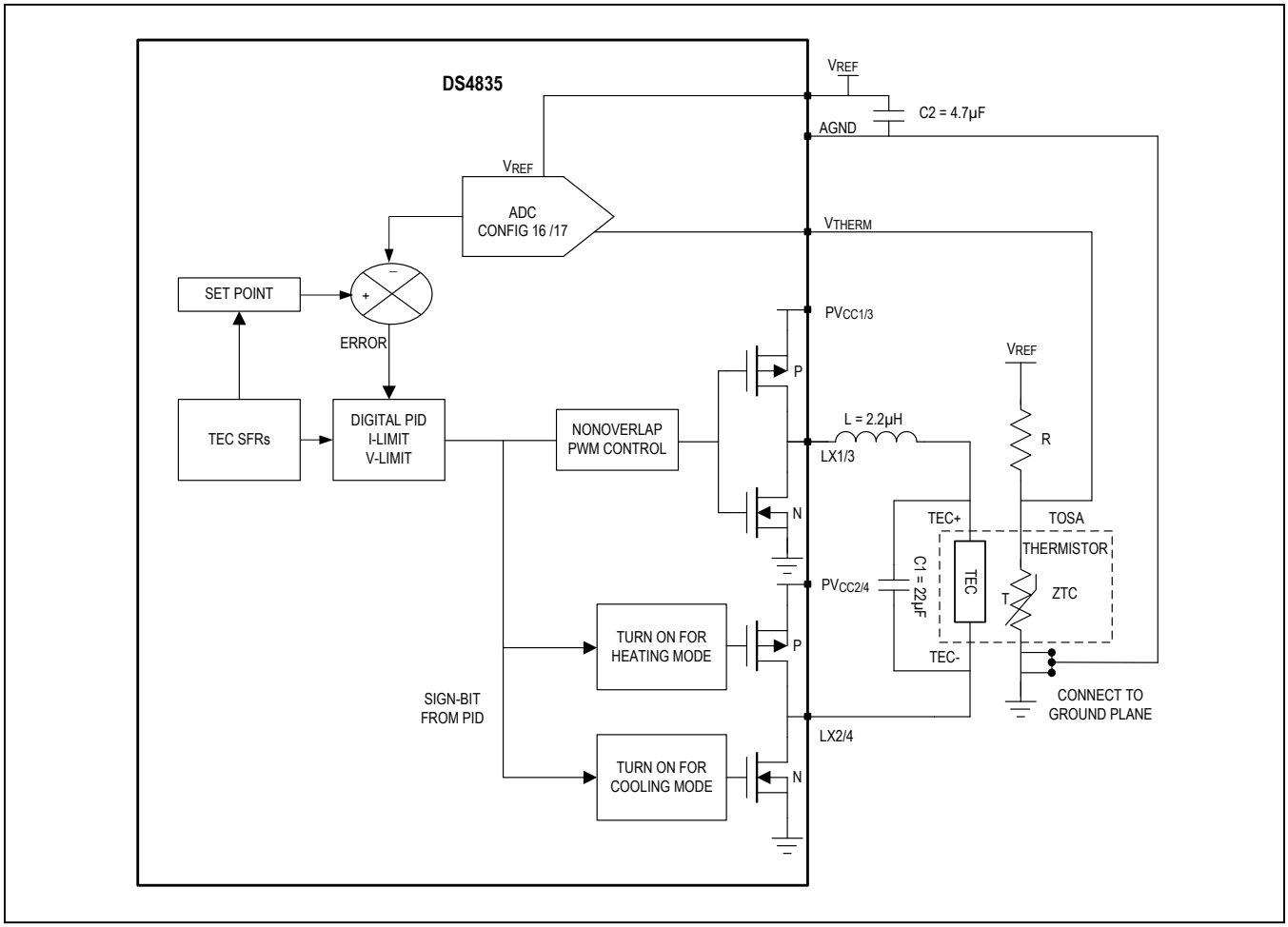


Figure 3. TEC Controller

DC-DC Converters

The device integrates three fully and individually programmable DC-DC buck converters with internal FETs and one of these (DCDC-3) can be configured as a DC-DC boost converter. Four more DC-DC controllers are available using an external FET that can be used to generate high-voltage output for APD bias or inverted output for EA bias.

Buck DC-DC Converters

Each buck DC-DC converter only requires an external inductor and decoupling capacitors to complete the converter circuit. The output voltage (V_{OUT}) should be directly connected to the feedback node (FB) to reduce the component count on the module and V_{OUT} is programmed using an SFR. The switching frequency at LX is up to 3MHz and the internal controller runs at a 128MHz clock rate. Refer to Figure 4.

V_{RDCDC} is the voltage-reference DAC and reference voltage for the DC-DC controller. This is a 10-bit DAC with a full-scale voltage of 1.4V. The V_{RDCDC} register should be adjusted to set the desired output voltage. The voltage comparator compares the output voltage with the V_{RDCDC} DAC reference voltage. The buck converter features an internal resistor divider to reduce the component count on the optical module. Therefore, V_{OUT} can be connected directly to the feedback point (FB) without an external resistor network, which saves board space and cost.

Short Circuit Protection

The DC-DC controller has built-in short-circuit protection, when the output voltage is shorted to GND or when unexpected overcurrents flow due to circuit violations. The protection circuit immediately disables the DC-DC controller and protects the device from getting damaged. Short-circuit protection is implemented into the hardware layer and does not require software programming. Since it is implemented in the hardware layer, the response to a fault condition is fast.

Component Selection

Selection of proper inductor and decoupling capacitors are very important for proper DC-DC functioning. The controller runs at a high frequency of up to 3MHz so inductor size can be as small as possible. The inductor current rating should be double the rated maximum peak current and the DC resistance should be as small as possible. The recommended inductor part number is DFE201612P-1R0M from muRata (1.0µH ±20%, DCR = 54mΩ typical and rated current = 3.3A). Similarly, decoupling capacitors play a vital role in DC-DC converter circuits. Use good X7R capacitors for decoupling. The recommended capacitor voltage rating should be at least double the output voltage. Input capacitor placement and selection is very critical. The input capacitor must be placed so that the current loop at the input switching node is very small. See the *Layout Recommendations* section for more details.

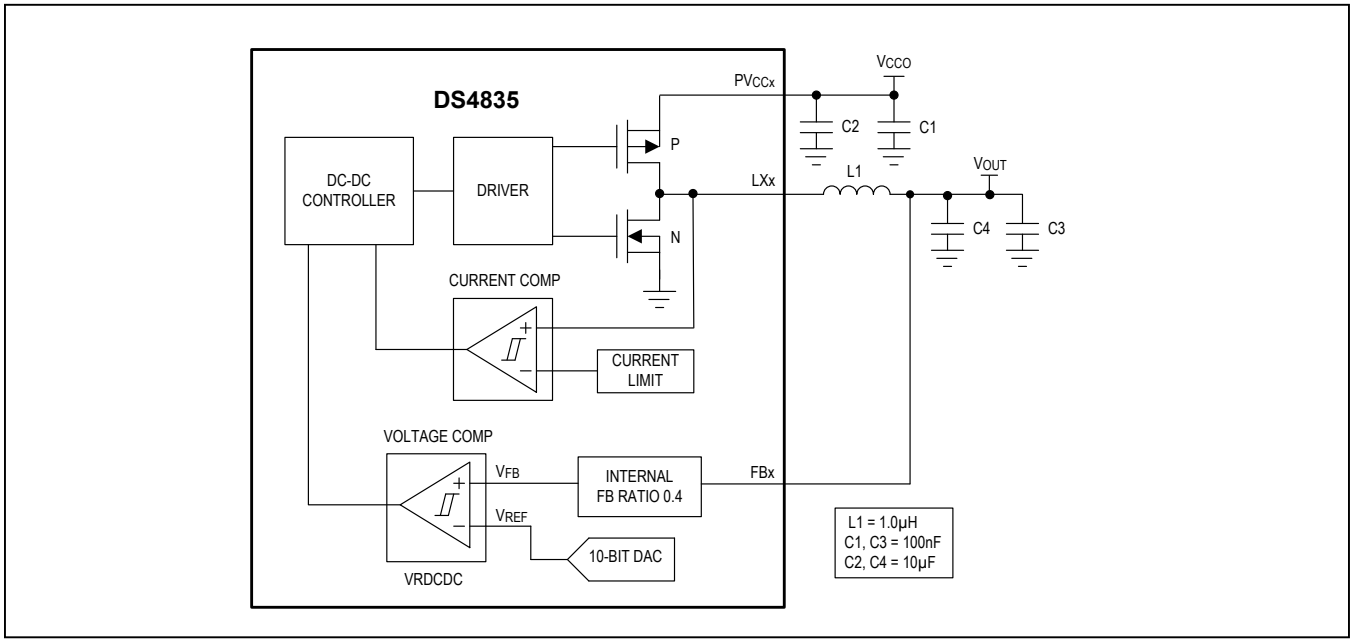


Figure 4. Buck DC-DC Converter Typical Application Circuit

Enabling the DC-DC Converter

The DC-DC converter operates in two states. One is startup and the other is steady-state. In startup state, the DC-DC starts to charge the output capacitors with high peak current from 0V to the configured voltage. Approximately 150µs is the settling time to reach the desired output voltage depending on the load condition and configured voltage level. Once the output voltage is reached, the voltage startup state finishes and the controller enters the steady-state operation. In steady-state, the DC-DC continuously monitors and regulates the output voltage for load-current variation as well as supply voltage fluctuations. The maximum continuous load current is 1500mA.

Table 1. Recommended DC-DC Buck SFR Settings

SFR SETTING VALUE	VALUE
NMOS_ON	0000h
NMOS_ON_ST	0000h
PMOS_ON	0018h
PMOS_ON_ST	0069h

Note: *If there is any load violation in the startup state, the DC-DC might not settle at the configured voltage and the controller will fail to regulate the output. Refer to the DS4835 User Guide for more details.*

Using the Buck Converter to Power the Current DACs

The DC-DC buck converter can be used to lower the supply voltage for the current DACs and reduce the power dissipation. The DCDC1 feedback node is the V_{CCDAC} pin, when Buck1 is used it is the default power supply for IDACs.

4V Boost DC-DC Convertor with an Internal Power FET

The device has an integrated internal power FET and a controller to generate a configurable boost voltage between V_{DD} and 4V. The boost converter can provide up to 200mA load current. As shown in Figure 5 below, the boost DC-DC requires an external inductor, resistors, and decoupling capacitors to complete the converter circuit. The output voltage is monitored at the feedback pin.

Table 2. Recommended DC-DC Boost SFR Settings

SFR SETTING VALUE	VALUE
NMOS_ON	000Eh
NMOS_ON_ST	0006h
PMOS_ON	0010h
PMOS_ON_ST	0100h

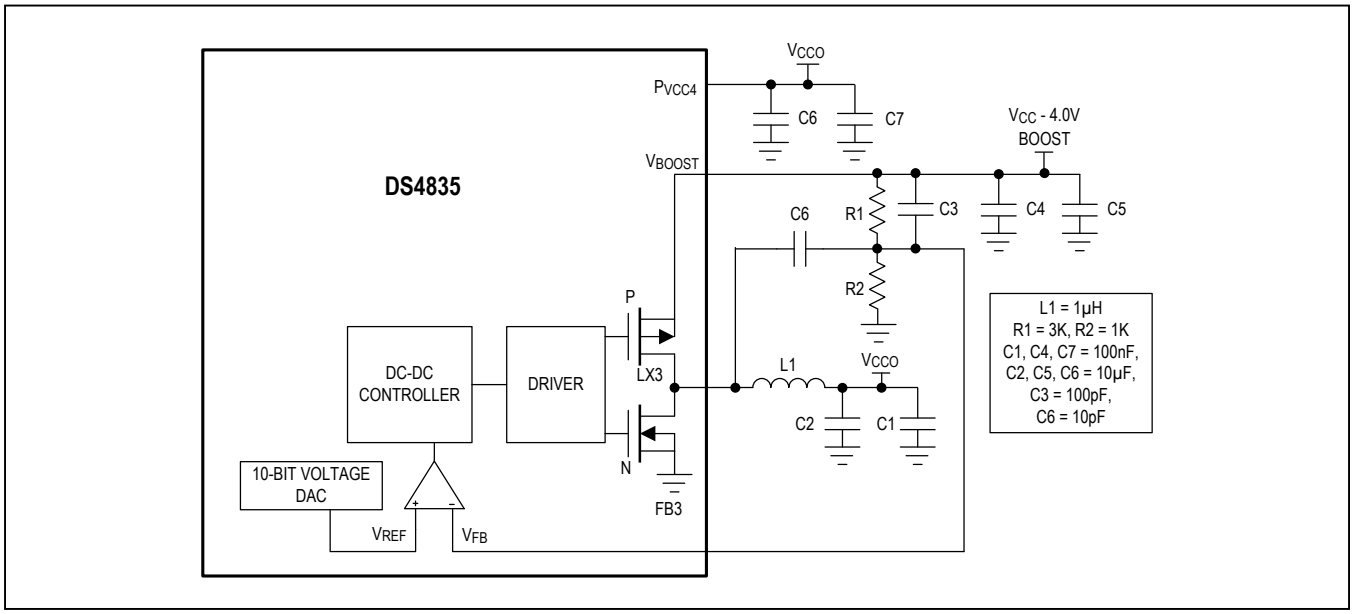


Figure 5. Boost DC-DC Converter Typical Application Circuit

Boost DC-DC Converter with an External FET

A built-in boost controller can be used to generate a high output voltage or inverted output to bias an APD or EA bias, using an external FET, an inductor, a diode, and decoupling capacitors. The controller uses a proportional integral (PI) control algorithm and runs at the 128MHz clock rate. The PWM operating frequency is up to 1MHz. High frequency operation results in small-size inductor and capacitors to save board space and reduces the output-voltage ripple. The boost DC-DC converter typical application circuit is shown below for 40V and 4mA output current. To generate different output voltages and currents, the user should select the appropriate FET, inductor, and diode for better performance. A general-purpose I/O with boost PWM capability is used to drive the FET. The voltage feedback to the ADC can be applied to any GPIO input with an ADC-input function.

Analog-to-Digital Converter

The device contains a 16-bit ADC with a 32-input multiplexer (with up to 24 external channels). The mux selects the ADC input from 24 external channels. Additionally, the channels can be configured to convert internal temperature, Sample and Hold channels and V_{CCO}. The ADC controller is the digital interface block between the CPU and the ADC. It provides all the necessary controls to the ADC and the CPU interface. The ADC uses a set of SFRs for configuring the ADC in the desired mode of operation. Each ADC channel can have its own configuration, such as priority select, conversion-reference select, averaging select, acquisition-time selection, etc. The ADC provides various interrupts for end of external channel sequence, temperature conversion, and SH conversion completion.

Temperature Measurement

The device provides an internal die-temperature-sensor monitor and an external diode-temperature sensor for laser-diode temperature monitoring. These can be enabled independently by setting the appropriate bit locations in the TEMPCN register. Whenever an internal temperature conversion is complete the ITEMPI flag is set. Whenever an external temperature conversion is complete the ETEMPI flag is set. This can be configured to cause an interrupt, and can be cleared by software. The temperature measurement resolution is 0.125°C. The ADC controller provides options to average the internal temperature results. The device provides 2, 4, 8, 16, 32, 64, 128 samples averaging configurations for the internal temperature.

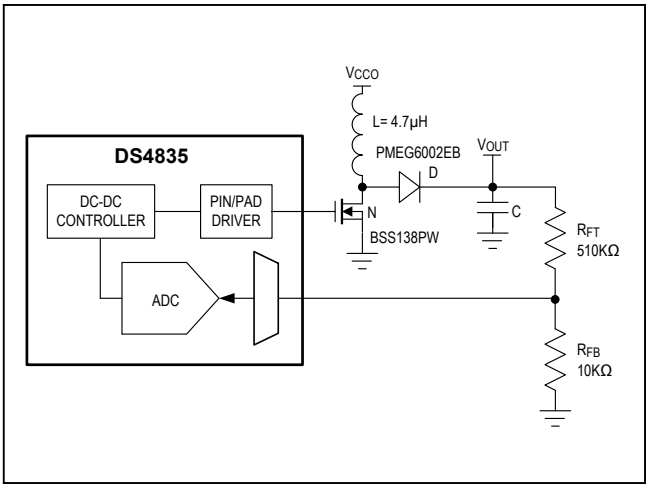


Figure 6. High-Voltage Boost DC-DC Converter Typical Application Circuit

Fast Comparator (Quick Trips)

The device supports 16-bit quick trip comparison functionality for the first eight ADC configurations. The quick trips can be used to continuously monitor user-defined channels in a round-robin priority sequence. The quick trip controller allows the user to control the list of channels to monitor in the round-robin sequence.

The quick trip (digital) performs two comparisons on any selected channel.

1) Comparison with a high-threshold value.
2) Comparison with a low-threshold value.
3) Window Comparator Mode operation.

Any comparison above the high-threshold value or below the low-threshold value causes a bit to set in the corresponding register. This bit can be used to trigger an interrupt. The threshold values are stored in 16 internal registers (8 registers for low-threshold setting and 8 registers for high-threshold setting). The quick-trip controller provides user-defined threshold values for the quick trips.

Inrush Control

The device integrates the inrush control feature to support hot-pluggable functionality of optical modules. This saves optical-module printed-circuit-board space and cost by removing external slow-start circuits. The source terminal of the FET connects to the inrush-supply IN pin (V_{CCI}) of the device and the drain terminal connects to inrush supply OUT pin (V_{CCO}). The inrush controller provides the control for the maximum current on powering up the module. Further detailed information regarding inrush control can be found in the *DS4835 User Guide*.

Current DACs

The device features 4 current DACs with programmable full-scale range. These current DACs can be used to provide laser bias or distributed Bragg reflector (DBR) current. The range selection provides flexibility to choose the range for maximum accuracy at lower currents. The supply voltage for the current DACs can be provided from the DC-DC buck converter 1, or from an external supply. Further detailed information regarding current DAC can be found in the *DS4835 User Guide*.

Delta-Sigma DAC

The device has twelve 16-bit delta-sigma DAC outputs. It has first order delta-sigma modulators. Associated pins can be configured as delta-sigma DACs when enabled. The modulator output translates to a DC voltage when fed to an external passive low-pass filter as shown in Figure 7. The maximum frequency of the delta-sigma modulator output is 8MHz. This frequency output can be observed at half the full-scale value of delta sigma. More detailed information regarding the Delta-Sigma DAC can be found in the *Delta-Sigma DAC* section of the *DS4835 User Guide*.

Pulse-Width Modulation

The DS4835 provides 8 pulse-width modulated (PWM) outputs. These PWMs have 16-bit resolution and can operate at a frequency of 2MHz. This modulator output can be converted to a DC voltage when it's fed to an external passive low-pass filter. More detailed information regarding PWMs can be found in the *DS4835 User Guide*.

Automatic Power Control

The device provides four integrated automatic power controls (APC) that can be used for APC loop, which reduces software overheads. The APC uses the monitor diode feedback at any ADC pin as analog input. The user can set the APC set point to the APC set-point register and based on the monitor diode feedback, the APC loop provides the new bias current value which can be directly written to the laser driver.

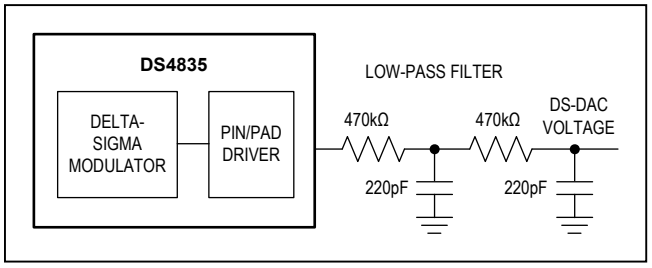


Figure 7. Delta-Sigma DAC

Programmable Logic Array

The device provides four hardware programmable logic arrays (PLA) to meet the time-critical optical-module requirements, e.g., TXD, LOS, TXF, or similar input-to-output operations. This is accomplished in hardware and does not require complex software interrupts and the latency that software would cause. The PLA provides the logic solution for asserting fast output based on different input condition. The connected output pin responds to PLA once PLA is enabled. The PLA output can also be asserted by software control bits. Additionally, PLA output can be controlled enabling quick-trip bits of the logic. More detailed information regarding PLA can be found in the *PLA* section of the *DS4835 User Guide*.

Serial Peripherals

The DS4835 has two I²C master, I²C slave, 3-Wire, SPI master, and SPI slave interfaces.

I²C Compatible Interface Modules

The device provides three independent I²C-compatible interfaces, two I²C masters and one slave. The I²C slave can support up to 4 slave addresses simultaneously.

I²C-Compatible Master Interfaces

The device features two I²C-compatible master interfaces for communication with a wide variety of external I²C devices. The I²C master has an 8-byte buffer that allows for better firmware independent communication. The I²C-compatible master bus is a bidirectional bus using two bus lines, the serial data line (MSDA) and the serial clock line (MSCL). For the I²C-compatible master, the device has ownership of the I²C bus, drives the clock, and generates the START and STOP signals. This allows the device to send data to a slave or receive data from a slave. The I²C-master mode is enabled by setting the master enable bit (TW2WEN). The I²C-master has 8-bytes of buffer to allow multiple byte reads and writes with less firmware control. More detailed information can be found in the *I²C-master* section of the *DS4835 User Guide*.

I²C-Compatible Slave Interface

The device also features an internal I²C-compatible slave interface for communication with a host. Furthermore, the device can be in-system programmed (bootloader) through the I²C-compatible slave interface. The two interface signals used by the I²C slave interface are SCL and SDA. For the I²C-compatible slave interface, the device relies on an externally generated clock to drive SCL and responds to data and commands only when requested by the I²C master device. The I²C-compatible slave inter-

face is open-drain and requires external pullup resistors. The device supports four slave addresses. Each slave address has a dedicated 8-byte transmit page and all slave addresses share a common 8-byte receive FIFO. More detailed information can be found in the *I²C-slave* section of the *DS4835 User Guide*.

SPI Interface (Master and Slave)

The device includes a master and slave SPI interface. The SPI provides an independent serial communication channel to communicate synchronously with peripheral devices in a multiple-master or multiple-slave system. The interface allows access to a four-wire, full-duplex serial bus, and can be operated in the master mode. Collision detection is provided when two or more masters attempt a data transfer at the same time. The maximum data rate of the SPI is 1/2 the system clock frequency for master mode.

SPI-slave mode is used when the SPI is controlled by another peripheral device. The SPI is in slave mode when an internal bit (MSTM) is cleared to logic 0. In slave mode, the SPI is dependent on the SPICK sourced from the master to control the data transfer. The SPICK input frequency should not be greater than the system clock frequency of the slave device divided by 4. Data received from the master replaces data in the slave's shift register at the completion of a transfer. More detailed information can be found in the *SPI* section of the *DS4835 User Guide.*

3-Wire Interface Module

The DS4835 controls devices like the MAX24033/MAX24016/MAX3956/MAX3798/MAX3799 over a proprietary 3-wire interface. The device acts as the 3-wire master, initiating communication with and generating the clock for the 3-wire slave. It is a 3-pin interface consisting of SDA_3W (a bidirectional data line), an SCL_3W clock signal, and a CS_3W chip select output (active high). The 3-wire master has 8-bytes of buffers to support burst mode read and writes with a 3-wire slave device.

I/O Ports

The device allows for most pins to function as general-purpose input and/or output pins. There are four ports: Port0[7:5] and Port0[3:0], Port1[7:0], Port2[7:0], and Port6[3:0]. Port0 is open drain, whereas the other two ports are push-pull IOs. Each port pin is multiplexed with other special function, such as interrupts, ADC, DAC, PWM, etc. Port6[3:0] is an input-only port if any of these pins is not used for the DC-DC operation.

The GPIO pins have Schmitt trigger receivers and full CMOS output drivers, and can support alternate functions. The ports can be accessed through SFRs (PO, PI, PD, IEN, EIE, EIF, and EIES) and each pin can be individually configured. The pin is either high impedance or a weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register. In addition, each pin can function as an external interrupt with individual enable, flag, and active-edge selection when programmed as input. The ADC input channels are by default GPIO pins. The I/O port SFRs are accessed in Module 0 and 1.

Programmable Timers

The device features three general-purpose programmable timers. Various timing loops can be implemented using the timers. The timer can be used in two modes: free-running mode and compare mode. The functionality of the timers can be accessed through three SFRs for each of the general-purpose timers. GTCN is the general control register, GTV is the timer value register, and GTC is the timer-compare register. More detailed information regarding times can be found in the *DS4835 User Guide*.

Hardware Multiplier and Accumulator

The DS4835 has two independent hardware multiplier and accumulators (MAC). The hardware multiplier (a multiply-accumulate, or MAC module) is a very powerful tool, especially for application that requires complex calculations. This multiplier executes the multiply, multiply-negate, multiply-accumulate, multiply-subtract or multiple-shift operation for signed or unsigned operands in a single clock. More detailed information regarding MAC can be found in the *DS4835 User Guide*.

In-Circuit Debug

Embedded debugging capability is available through the 1-Wire interface. Embedded debug hardware and embedded ROM firmware provide in-circuit debugging capability to the user application, eliminating the need for an expensive in-circuit emulator. The in-circuit debug features include:

- Hardware debug engine,
- Set of registers able to set breakpoints on register, code, or data accesses (ICDA, ICDB, ICDC, ICDD, ICDF, ICDT0 and ICDT1),
- Set of debug service routines stored in the utility ROM.

The embedded hardware debug engine is an independent hardware block in the microcontroller. The debug engine can monitor internal activities and interact with selected internal registers while the CPU is executing user code. Collectively, the hardware and software features allow two basic modes of in-circuit debugging:

- Background mode allows the host to configure and set up the in-circuit debugger while the CPU continues to execute the application software at full speed. Debug mode can be invoked from background mode.
- Debug mode allows the debug engine to take control of the CPU, providing read/write access to internal registers and memory, and single-step trace operation.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS4835, decouple the V_{CCO} power supply with a 1µF and 0.01µF X5R capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. Decouple the BYP18 pin using a 1µF and V_{REF} pins using 4.7µF X5R capacitor. The V_{REF} capacitor must be placed close to the device between the V_{REF} and AGND pins.

Note: *do not use the BYP18 pin for external circuitry.*

Thermal Vias

It is recommended to place a thermal landing on the opposite side of the PCB also. This improves the thermal transfer to ambient and increase the thermally conductive area. The thermal landing should be at least as large as the exposed pad and can be made larger depending on the amount of free space from the exposed pad to other pin landings. The thermal landing is connected to the ground plane with thermal vias. The thermal vias direct heat from the thermal landing to the ground plane as well as to ambient through the bottom of the PCB. Multiple vias improve the heat transfer away from the IC and also improve the electrical connection to ground (when applicable). A 1.0 to 1.2mm pitch is the recommended spacing for the vias in most applications. Refer to **application note AN862** for more detailed information.

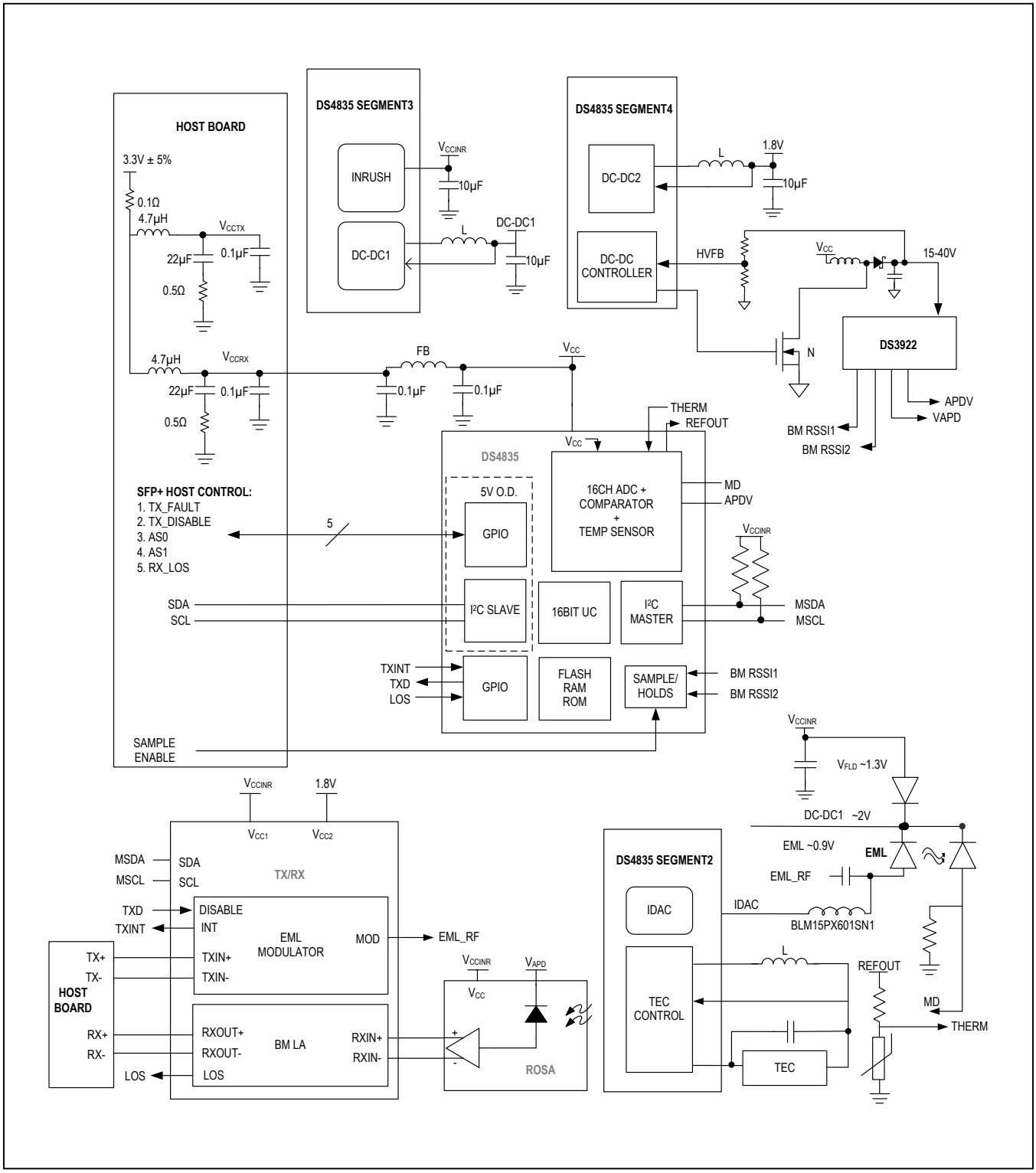
Table 3. GPIO Special Function Cross Reference

PIN #	PIN NAME	ADC	IDAC	DS DAC	PWM	DC-DC	PLA	S/H	I²C	3-WIRE	SPI	PORT
1	GP20	ADC16		DS_DAC0	PWM0	APD4	PLAOUT	SHP0				GPIO20
2	GP21	ADC17		DS_DAC1	PWM1		PLAOUT	SHN0				GPIO21
3	GP16	ADC14	IDAC4	DS_DAC11				SHEN0				GPIO16
4	GP15	ADC13	IDAC3	DS_DAC10				SHEN0				GPIO15
5	V_{CCDAC}	ADC4				FB1						
6	GP14	ADC12	IDAC2	DS_DAC9					MSDA1 ALT			GPIO14
7	GP13	ADC11	IDAC1	DS_DAC8					MSDA1 ALT		MSPI_ MISO/ SSPI_MISO	GPIO13
8	GP22	ADC18		DS_DAC2	PWM2	APD1	PLAOUT					GPIO22
9	GP23	ADC19		DS_DAC3	PWM3	APD2	PLAOUT					GPIO23
10	GP24	ADC20		DS_DAC4	PWM4		PLAIN					GPIO24
11	GP03	ADC3					PLAOUT	SHEN1	MSCL2			GPIO03
12	GP05	ADC5					PLAIN	SHEN0				GPIO05

Table 3. GPIO Special Function Cross Reference (continued)

PIN #	PIN NAME	ADC	IDAC	DS DAC	PWM	DC-DC	PLA	S/H	I²C	3-WIRE	SPI	PORT
13	GP06	ADC6					PLAIN					GPIO06
14	GP07	ADC7				FB3	PLAIN					GPIO07
15	AGND											
16	V_{REF}											
17	V_{CCO}											
18	V_{CCI}											
19	GP25	ADC21		DS_DAC5	PWM5		PLAIN					GPIO25
20	GP26	ADC22		DS_DAC6	PWM6		PLAIN	SHP1				GPIO26
21	GP27	ADC23		DS_DAC7	PWM7		PLAIN	SHN1				GPIO27
22	LX4	ADC9				TECN2						GPI63
23	PV_{CC4}											
24	LX3					TECP2						GPI62
25	PV_{CC3}											
26	PV_{CC2}											
27	LX2	ADC8				TECN1						GPI61
28	PV_{CC1}											
29	LX1					TECP1						GPI60
30	GP12	ADC10				FB2			MSDA1 ALT	CS_3W	SSPI_ CSEL	GPIO12
31	GP11								MSCL1	SCL_3W	MSPI_CK/ SSPI_CK	GPIO11
32	GP10								MSDA1	SDA_3W	MSPI_ MOSI/ SSPI_MOSI	GPIO10
33	SCL											
34	SDA											
35	BYP18											
36	GP02	ADC2					PLAOUT	SHEN1				GPIO02
37	GP01	ADC1					PLAOUT	SHEN1	MSDA2			GPIO01
38	GP17	ADC15 TSENS				APD3	PLAIN	SHEN0				GPIO17
39	$\overline{RST}$											
40	GP00	ADC0					PLAOUT	SHEN1				GPIO00
—	EP (GND)											

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TEC1	TEC2	TEC SET POINT RESOLUTION	DC-DC3 BOOST	IDAC1	IDAC2	IDAC3	IDAC4
DS4835ZGTL+	-40°C to +105°C	40 TQFN	Yes	Yes	16-bit	Yes	Yes	Yes	Yes	Yes
DS4835VGTL+	-40°C to +105°C	40 TQFN	No	Yes	9-bit	No	Yes	Yes	Yes	Yes
DS4835TGTL+	-40°C to +105°C	40 TQFN	No	No	No	No	Yes	Yes	Yes	Yes
DS4835RGTL+	-40°C to +105°C	40 TQFN	Yes	No	16-bit	Yes	No	Yes	No	No
DS4835PGTL+	-40°C to +105°C	40 TQFN	Yes	No	9-bit	Yes	No	Yes	No	No
DS4835MGTL+	-40°C to +105°C	40 TQFN	Yes	Yes	16-bit	No	No	Yes	No	No
DS4835JGTL+	-40°C to +105°C	40 TQFN	No	Yes	12-bit	No	No	Yes	Yes	No
DS4835GGTL+	-40°C to +105°C	40 TQFN	No	No	No	No	No	No	No	No
DS4835EGTL+	-40°C to +105°C	40 TQFN	No	No	No	Yes	No	No	No	No

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—
1	4/18	Updated the *Absolute Maximum Ratings*, *SPI Interface (Master/Slave)*, and *3-Wire Interface Module* sections. Updated the *Electrical Characteristics* and *Pin Description* tables, Table 3, and Figure 7.	2–10, 17, 28–29, 31
1.1		Corrected template format	1
2	6/21	Updated *Electrical Characteristics* table	9, 10

