Chipathon 2025
Prof James Morbius

Project Proposal

Team Introduction

PROF MORBIUS

ONE OF THE CHIPS OF ALL TIME

Team members

- [Leader] James Patrick <@orpheus016:matrix.org>
- [Member] Ibrahim Hanif Mulyana <@ibrhmnhnfm:matrix.org>
- [Member] Goldwin Sonick Wijaya Thaha <@goldwinsonick:matrix.org>

Team background

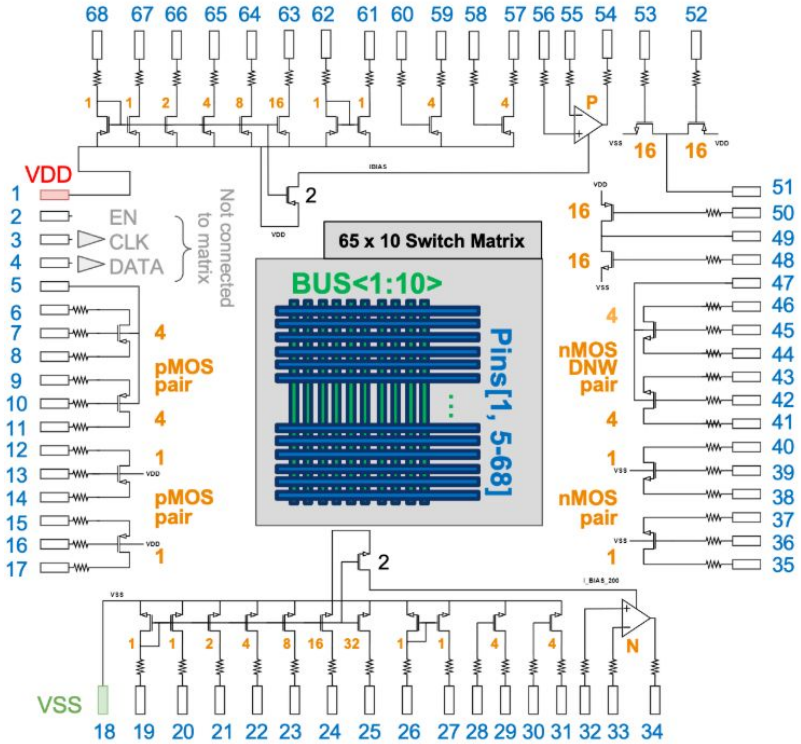
- Experience
  - We are undergraduate student that just finished 3rd year in Electrical Engineering from Institute of Technology Bandung, Indonesia.
  - We have experience designing a chip layout using IIC-OSIC-TOOLS (Xschem, Magic, etc) with SKY130 PDK
  - We have experience designing an RTL using Verilog/VHDL and layout generation using OpenLane2

Project Background and Goals

The MOSbius as a switch matrix can be used to do experiments on analog and RF designs. With wireless communications becomes increasingly used in wider region and scale, we ought to test the reliability of these communication systems, or rather, the reliability of techniques used to ensure our communication to be working. (One of them being spread spectrum techniques, FHSS and DSSS)

By doing this project, our goal is to:

- Design a (Frequency Hopping Spread Spectrum) FHSS Educational Learning Kit with Custom Analog Chip and Comprehensive Learning Guide.
- Design a custom IC with core analog blocks of a frequency synthesizer (VCO, PLL) with system integration to the off-chip components (on MOSbius Board)

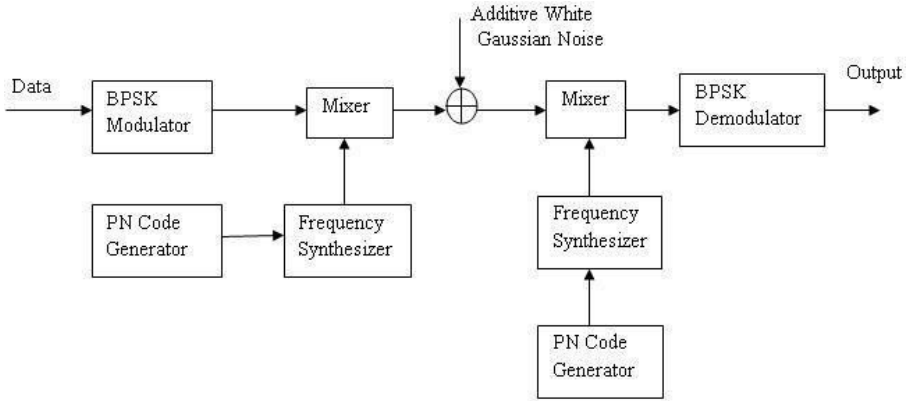


Project Information

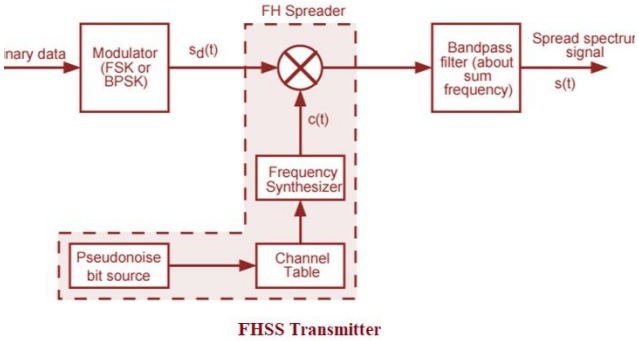
- ***Design***
  - On-Chip (Custom IC), we will design 1) **Voltage-Controlled Oscillator (VCO)** to generate the carrier and 2) **Phase-Locked Loop (PLL)** components: Phase Detector, Charge Pump, and Loop Filter to ensure frequency stability and control.
  - We will use the MOSbius board to make 1) **PN Sequence Generator** to control the frequency hopping pattern, 2) **Mixer** for receiver de-hopping and signal demodulation 3) **Modulator** to impress data onto the hopping carrier 4) **Stable Reference Oscillator** for the PLL.
- ***Application***
  - Education and Experimentation: A hands-on platform for teaching students system-level principles of spread spectrum communication.
- ***Early References***
  - Example of DSSS/FHSS Trainer Kit: https://www.tescaglobal.com/product/cdma-dsss-fhss-trainer
  - https://www.researchgate.net/publication/309521542_A_modified_closed-loop_auto_frequency_calibration_technique_for_a_1571-GHz_integer-N_PLL
  - https://www.researchgate.net/publication/314818626_Design_and_Simulation_of_RADAR_Transmitter_and_Receiver_using_Direct_Sequence_Spread_Spectrum

Block Diagrams

- System Block Diagram

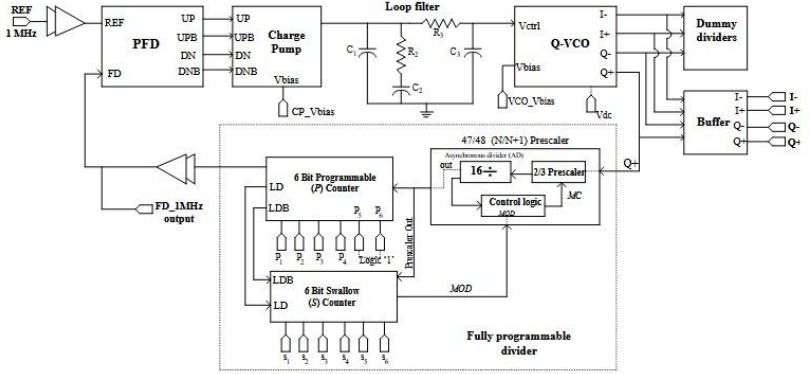


- FHSS Transmitter

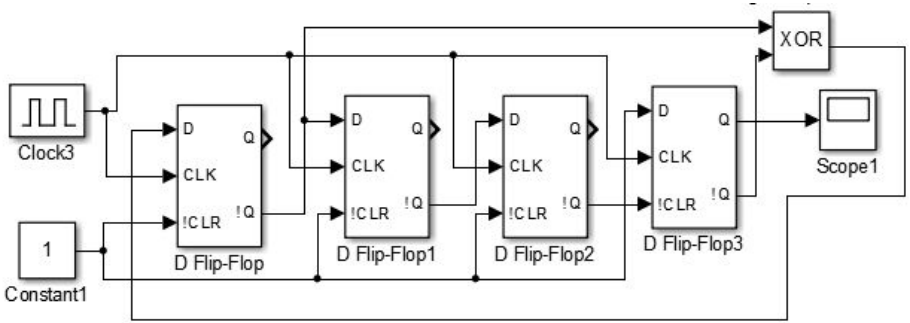


Block Diagrams

- Frequency Synthesizer

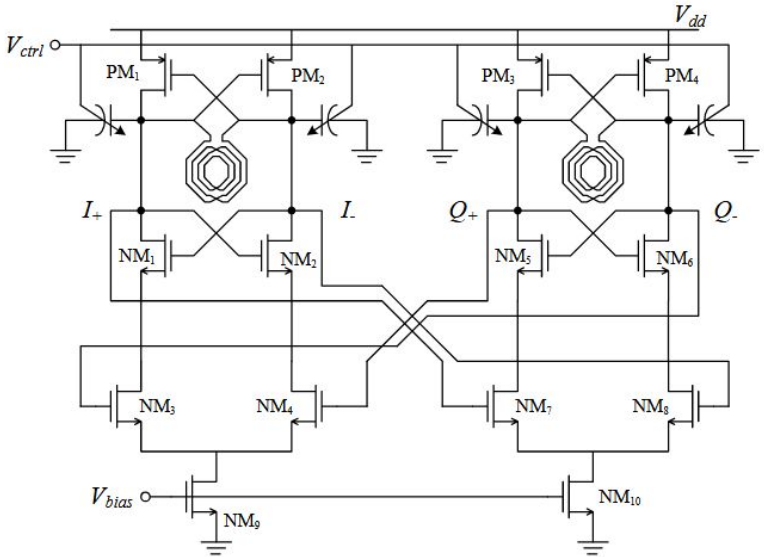


- PN Sequence Generator

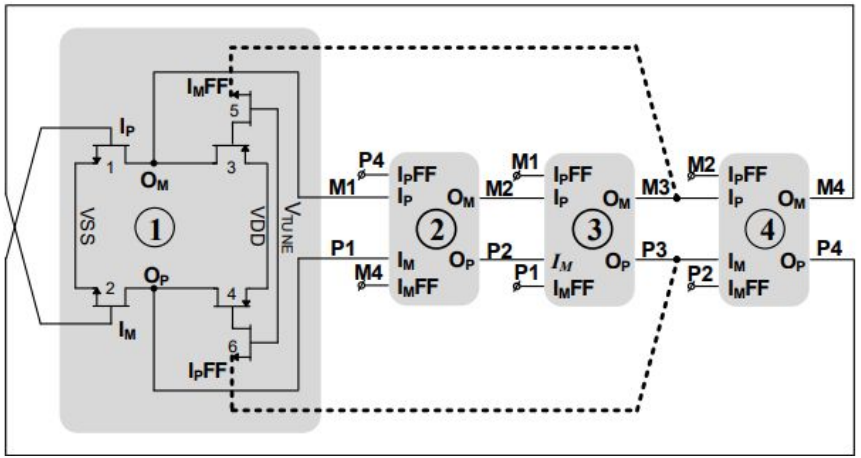


System Block Diagram

- LC VCO

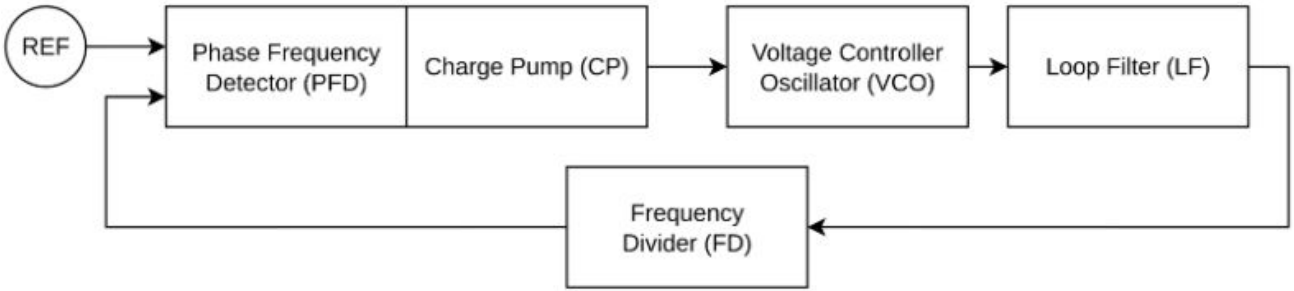


VC Ring Oscillator



Block Diagrams

- PLL



Timeline

Week	Starting Date	Ending Date	Task	PIC	Expected Product	Details
Phase 1 : Setup and Introduction						
Phase 2 : Team Formation and Project Planning						
28	07/07/2025	13/07/2025	Initial proposal and project plans.	All members	-	-
29	14/07/2025	20/07/2025	System parameters and specifications. Standardize the Design Flow.	All members working in parallel	all parameters, architecture, and target specification	Each member is assigned to a block (VCO, PN Generator, and Gilbert Cell Mixer)
30	21/07/2025	27/07/2025	Per Block Schematic Design using Xschem + Testbench	All members working in parallel	sch files, early simulation	Making VCO, PN Sequence Generator and Mixer using Xschem, inc. simulation
Phase 3 : Design and Simulation						
31	28/07/2025	03/08/2025	Per Block Layout Design using Magic + Testbench	All members working in parallel	mag files, parasitic extraction	Manually making each block using magic, extracting necessary files, then simulation using testbench for each block
32	04/08/2025	10/08/2025	Top Level Integration Interface Design	All members working in parallel	top level design, interface	
33	11/08/2025	17/08/2025	Top Level Verification. Design Optimization.	All members working in parallel	optimized design, potential problems identification	

Timeline

Phase 4 : Layout and Verification						
34	18/08/2025	24/08/2025	PCB, MOSbius, Interface Design	All members working in parallel		Integrating our system with MOSbius, designing the final pcb kit, checking interface
35	25/08/2025	31/08/2025	PCB, MOSbius, Interface Design	All members working in parallel	final pcb design and verification	Integrating our system with MOSbius, designing the final pcb kit, checking interface
36	01/09/2025	07/09/2025	Buffer			Tolerance in case deadline is not met, more optimization & verification
37	08/09/2025	14/09/2025	Buffer			Tolerance in case deadline is not met, more optimization & verification
38	15/09/2025	21/09/2025	Testing and Revisions	All members working in parallel		Final revisions
39	22/09/2025	28/09/2025	Testing and Revisions	All members working in parallel		Final Submission Day
40	29/09/2025	05/10/2025	Retrospection			Project Retrospective
Phase 5 : Manufacturing and Testing						
IF TIME ALLOWS	-	-	Designing PLL components	All members working in parallel		Phase Detector, Charge Pump Block Design

Questions?

- What’s the simplest way to do the interfacing between the IC Chip and the MOSbius?
- How can we test the MOSbius design if we doesn't have the chip? Is using the simulation enough to make sure that it is working well?
- We had experience in implementing a MUX and DFF layout using XSchem, Magic in the IIC-OSIC-TOOLS. (Here’s one of the github link for the project https://github.com/goldwinsonick/APIC-2025/tree/main/APIC-UTS) but we aren’t sure about some aspects:
  - What’s the best practice to determine the Power Rail width, placement, etc.
  - Are there any recommended source for learning verification method (UVM, etc.)

Doubts? (Questions asked during the meet + some additional ones)

- We’re new to RF in general, (we only learnt the basics in analog & digital modulation/demodulation) do you think it’s feasible for us to learn and understand this topic and then implement it in this chipathon? If it isn’t should we change tracks or just make a simpler project? Please give us your suggestions.
- This idea stems from our interest on measures to avoid interferences that we can implement on a chip-level. Any recommended references about spread spectrum is helpful.
- Should the mixer be made using the MOSbius chip, or just a COTS one integrated into the PCB testing kit? We haven’t really finalized our system structure.
- Is it better if we include more applications for this chip or focus on spread spectrum communication?
- Should we implement VC Ring Oscillator or LC VCO for 900MHz for LoRa data transmission?