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Assignment 4, Question 2

HyperTransport Overview

The HyperTransport (HT) interconnection standard has gone through a number of versions since its creation in April, 2001. In all of these versions, the HT link can transmit a certain number of bits on the rising and falling edges of its internal clock. Each HT link contains two unidirectional lanes, enabling bidirectional transfers. The lanes can vary in width from 2-bits to 32-bits. Note that the clock speeds and lane widths of receive and transmit links may be different.

The bandwidth of the link is determined by the clock speed and the width of the two lanes. The table below gives the bandwidth of various versions of the HT standard with the maximum 32-bit lane width.

The formula for the bandwidth is: ClockSpeed * 2 (DDR) * 4 (bytes per transfer) * 2 (lanes)

HyperTransport Version	Clock Speed	Bandwidth (aggregate)
HyperTransport 1.0	200Mhz – 800 Mhz	3.2 MB/s – 12.8 MB/s
HyperTransport 2.0	1.0 Ghz – 1.4 Ghz	16.0 MB/s – 22.4 MB/s
HyperTransport 3.0	1.8 Ghz – 2.6 Ghz	28.8 MB/s – 41.6 MB/s

HT is packet-based. All packets are broken up into 32-bit words. The packet-based design and fast clock speed give HT very low latency. One study (Source: http://www.hypertransport.org/docs/wp/Latency_Comparison_HyperTransport_PCIe_in_Communications_Systems.pdf) showed that the latency of a read request over HT was between 144 and 228 ns, depending on the size of the read request and the buffering technique used.

Sources: http://en.wikipedia.org/wiki/HyperTransport ,
http://www.hypertransport.org/tech/tech_faqs.cfm ,
http://www.hypertransport.org/tech/tech_latency.cfm ,

Uses

As a Multiprocessor Interconnect

For multiprocessor systems, HyperTransport interconnects would be an ideal way to communicate between processors. It is extremely low latency, and since high bandwidth is not necessarily required, we can use narrow lanes to make manufacturing easier. Further, since HT interconnects are bidirectional, we only need one connection between two processors.

AMD has already implemented HT interconnects with multiprocessor systems using Opteron processors.

As a Front Side Bus

Making a common interconnect for front side buses is the primary motivation behind HyperTransport. At the moment, different types of machines use different types of buses, which must all interface with other buses, such as AGP and PCI. If all front side buses used HT, then all motherboards could use the same PCI ↔ HyperTransport adaptor chip. In addition, the computer as a whole would theoretically be faster due to increased bandwidth and lower latency.

In Network Switches

Even with low-bandwidth network switches, the internal bandwidth must be much larger to handle data travelling between different ports, and in both directions. HyperTransport, itself packet-based, would be ideal for sending packets between different ports, or on more complicated switches, between routing nodes. It can more than handle the bandwidth, and would transfer the data quickly since it offers low latency.