The Active NPC Converter and Its Loss-Balancing Control

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***Abstract*—The three-level neutral-point-clamped voltage-source converter (NPC VSC) is widely used in high-power medium-voltage applications. The unequal loss distribution among the semiconductors is one major disadvantage of this popular topology. This paper studies the loss distribution problem of the NPC VSC and proposes the active NPC VSC to overcome this drawback. The switch states and commutations of the converter are analyzed. A loss-balancing scheme is introduced, enabling a substantially increased output power and an improved performance at zero speed, compared to the conventional NPC VSC.**

***Index Terms*—Medium voltage, power losses, three-level converter, voltage-source converter (VSC).**

NOMENCLATURE

A_X, B_X, C_X	Loss coefficients.
f_s	Carrier frequency.
f_0	Fundamental frequency.
$i_{\rm ph}$	Instantaneous phase current.
$I_{\rm rms}$	RMS value of the phase current.
M	Modulation depth $(=2\cdot\sqrt{2}/\sqrt{3}\cdot V_{\rm LL}/V_{\rm dc})$.
pf	Power factor.
$P_{\rm on}, P_{\rm off}, P_{\rm rec}$	Turn-on, turn-off, and recovery losses.
$P_{\rm cond}$	Conduction losses.
$V_{\rm dc}$	DC-link voltage.
$V_{\rm LL}$	RMS value of the line-to-line voltage.
$v_{\rm ph}$	Instantaneous phase-to-neutral point (NP) voltage.
$v_{\rm ref}$	Reference voltage for carrier-based modulation.
ϑ_a	Ambient temperature.
ϑ_j	Junction temperature.
$\rm T_{out}, D_{out}$	Outer switches and diodes $\rm T_{x1}, D_{x1}, T_{x4}, D_{x4}$, $\rm x = 1,2,3$.
$\rm T_{in}, D_{in}$	Inner switches and diodes $\rm T_{x2}, D_{x2}, T_{x3}, D_{x3}$, $\rm x = 1,2,3$.
$\rm T_{npc}, D_{npc}$	NPC switches and diodes $\rm T_{x5}, D_{x5}, T_{x6}, D_{x6}$, $\rm x = 1,2,3$.

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I. INTRODUCTION

IN the early 1980s a new, pioneering converter topology was proposed [1], [2]: the three-level neutral-point-clamped voltage-source converter (NPC VSC). The topology offered a simple solution to extend voltage and power ranges of the existing two-level VSC technology, which were severely limited by the blocking voltages of power semiconductors with active turn-on and turn-off capability. Hence, the converter was of particular interest for medium-voltage applications (2.3–7.2 kV). The NPC VSC was soon to be introduced on the market by leading manufacturers, and gained more and more importance [3], [4]. Today, it is widely used in medium-voltage drives (MVDs) for industry (e.g., rolling mills, fans, pumps, and conveyors), marine appliances, mining, and traction. The emerging wind energy market offers new potential applications. Recent investigations have shown that the NPC VSC is also a promising alternative for low-voltage applications, though for different reasons [5].

The topology is shown in Fig. 1. Compared to a two-level converter with a direct series connection of devices the NPC VSC features two additional diodes per phase leg. These diodes link the midpoint of the "indirect series connection" of the main switches to the neutral point of the converter. This allows the connection of the phase output to the converter neutral point and enables the three-level characteristic of the topology. The 27 switch states are depicted in the space-vector diagram in Fig. 1, whereas the two-level converter allows the eight switch states not comprising a "0" only. Hence, the clearly superior output voltage quality is the most distinct advantage over the two-level converter. Furthermore, the topology features a low part count and an increased reliability compared to two-level converters with a complicated series connection of devices (dynamic voltage-balancing networks!). The success on the market shows that the three-level NPC VSC is also an extremely competitive topology compared to the three-level flying-capacitor converter [6]. The expense of NPC diodes versus flying capacitors is one major tradeoff between both topologies. In the range of low and moderate switching frequencies (200 Hz–1 kHz), the NPC VSC is especially advantageous, since the required flying-capacitor size is inversely proportional to the switching frequency.

Aside from these outstanding advantages the NPC VSC has some drawbacks. The neutral-point potential has to be controlled actively. For most modulation schemes and under ideal conditions the dc-link capacitor voltages naturally balance over one fundamental cycle. However, semiconductors with slightly varying characteristics, different gate unit delay times, dynamic

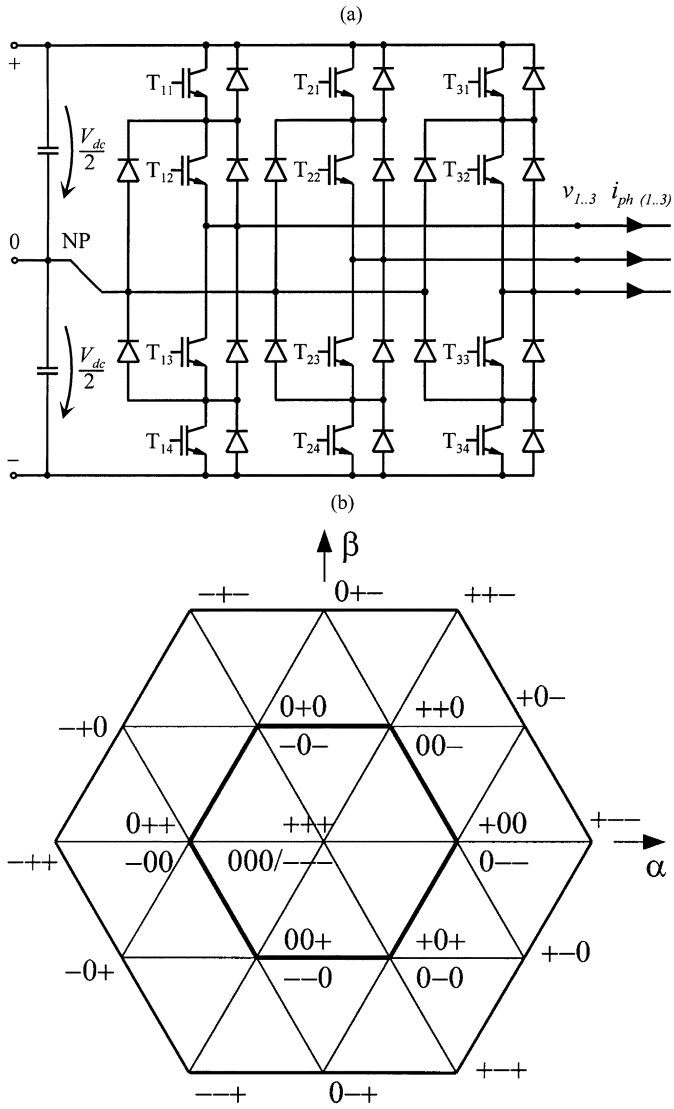

Fig. 1. (a) Three-level NPC VSC topology and (b) space-vector diagram.

load changes, or unbalanced loads can cause a steady drift of the neutral-point potential. However, the problem has been discussed in numerous papers [7]–[10] and solutions have been found. The proper use of redundant switch states of the space vector plot in Fig. 1 allows maintaining long-term stability of the neutral-point potential with no additional circuitry and no additional switching transitions (no additional losses!).

One substantial disadvantage, which has not yet been overcome, is the unequal distribution of semiconductor losses among the devices in the NPC converter. As in every converter the maximum allowable losses limit the switching frequency and the output power. In the special situation of high-power converters, single semiconductor devices [integrated gate bipolar transistors (IGBTs) or integrated gate-commutated thyristors (IGCTs)] are usually installed on separate heat sinks due to insulation requirements and the realization of a modular mechanical and thermal design. Separate heat sinks per device cause a good thermal decoupling of the semiconductors. Hence, an unequal loss distribution—as in the case of the three-level NPC VSC—also yields an unequal junction temperature distribution among the semiconductors. Some devices become hot while others stay much cooler at the same time. The maximum losses of a single device are solely set by its own and its heat sink's thermal characteristics, i.e., maximum operating junction temperature, cooling water temperature, and thermal impedances. Thus, the losses in the most stressed device limit the switching frequency and the maximum phase current of the entire converter. The overall switch utilization is low. The total converter losses (of all semiconductors and passive components such as capacitors, inductors, and resistors) determine the converter efficiency and the size of the back-cooling unit if a water-cooling system is used.

The problem of the unequal loss distribution is analyzed thoroughly in the following section. Subsequently, the authors introduce the three-level VSC with active NPC switches—named active NPC VSC (ANPC VSC)—to overcome the extremely uneven loss distribution and to mitigate the resulting drawbacks. The additional switch states and commutations of the ANPC converter are discussed; their influence on the loss distribution within the converter is explained. Based on this analysis a loss-balancing scheme is proposed, which is capable of increasing the converter output power drastically. This is achieved solely by a better loss distribution within the converter. Simulation results prove the superior performance of the ANPC VSC under loss-balanced operation compared to the conventional NPC VSC. Experimental results of a low-voltage test bench are presented. This paper is meant to extend and refine prior work [11].

II. Analysis of the Loss Distribution Problem

An analysis of the NPC VSC's loss and junction temperature distribution was carried out first in [11], and was extended in [10]. It has been observed that the losses of the respective devices depend on the operating points and the different modulation schemes being applied. The most critical operating points are located at the boundaries of the converter's operating area, namely, being maximum and minimum modulation depth, at power factors of $pf = 1$ and $pf = -1$. Here, the loss distribution is most unbalanced. All operating points in between are less critical.

Figs. 2 and 3 show the loss distribution and the corresponding average junction temperature distribution for a typical commercially available NPC converter, respectively[1]. At the maximum modulation depth of $M = 1.15$ all relevant modulation schemes—e.g., conventional space-vector modulation (SVM) or simple carrier-based sine-triangle modulation[2]—distribute the losses in an equivalent manner. The outer switches T_{out} are the most stressed devices for inverter operation [Fig. 2(a)], its inverse diodes D_{out} for rectifier operation [Fig. 2(b)]. In the latter case, the inner switches T_{in} experience about the

[1]All graphs and waveforms shown in Figs. 2, 3, 5, 11, 12, 13, and 14 are obtained by the means of time-domain MATLAB simulations. The simulation models are discussed in Section V.

[2]SVM using the "three-nearest" space vectors and carrier-based phase-disposition modulation are two equivalent approaches [12]. Throughout the paper reference waveforms for carrier-based modulation are used to illustrate the discussion. SVM is then understood as a modulation having centered middle vectors.

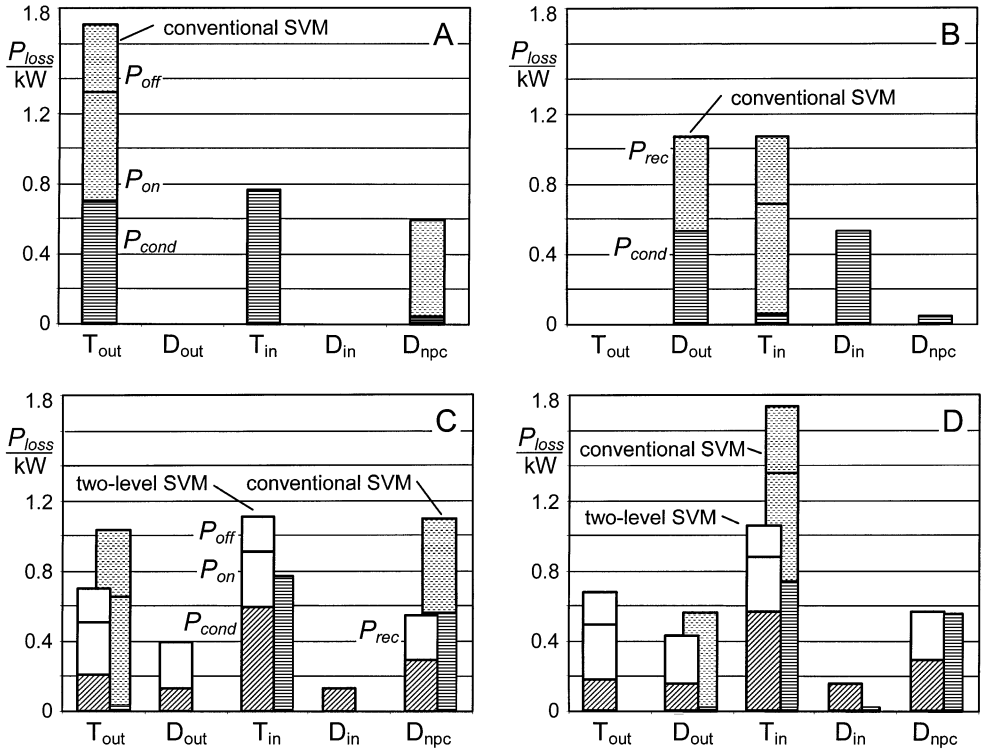

Fig. 2. Simulated loss distribution in a typical three-level NPC VSC featuring Eupec IGBTs ($V_{\rm dc} = 3400$ V, $I_{\rm rms} = 600$ A, $f_s = 1050$ Hz, Eupec FZ 1200 R33 KF2) (a) $pf = 1,\ M = 1.15$. (b) $pf = -1,\ M = 1.15$. (c) $pf = 1,\ M = 0.05$, (d) $pf = -1,\ M = 0.05$.

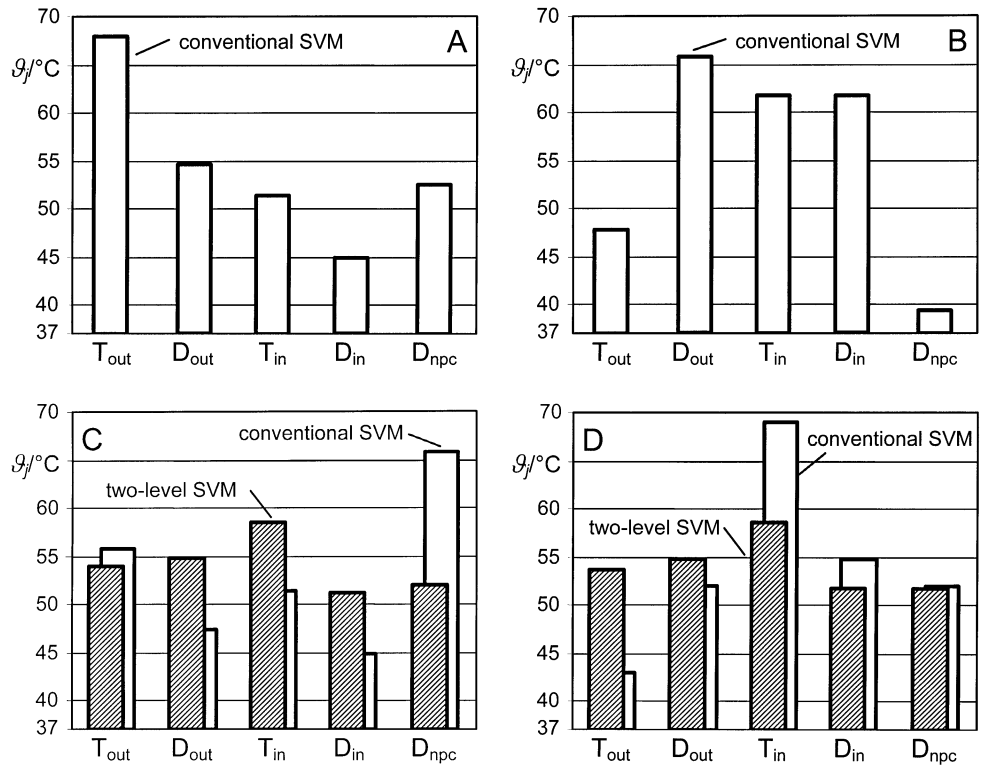

Fig. 3. Simulated average junction temperatures in a typical three-level NPC VSC featuring Eupec IGBTs[3] ($V_{\rm dc} = 3400$ V, $I_{\rm rms} = 600$ A, $f_s = 1050$ Hz, $\vartheta_a = 37$ °C, Eupec FZ 1200 R33 KF2). (a) $pf = 1,\ M = 1.15$. (b) $pf = -1,\ M = 1.15$. (c) $pf = 1,\ M = 0.05$. (d) $pf = -1,\ M = 0.05$.

same amount of losses as $D_{\rm out}$ but reach a lower ϑ_j. A smaller thermal impedance junction-to-case of the IGBT chips compared to the diode chips is the reason therefore. On the other hand, the diodes feature better on-state characteristics and

[3]For applications with repetitive cyclic duty, reliability constraints limit the maximum junction temperature rise of the IGBTs to about $\Delta T_j = 30$ K [13]. Hence, an ambient temperature $\vartheta_a = 37$ °C yields a maximum average junction temperature of roughly $\vartheta_{j-\max} = 67$ °C. This issue is discussed in Section V.

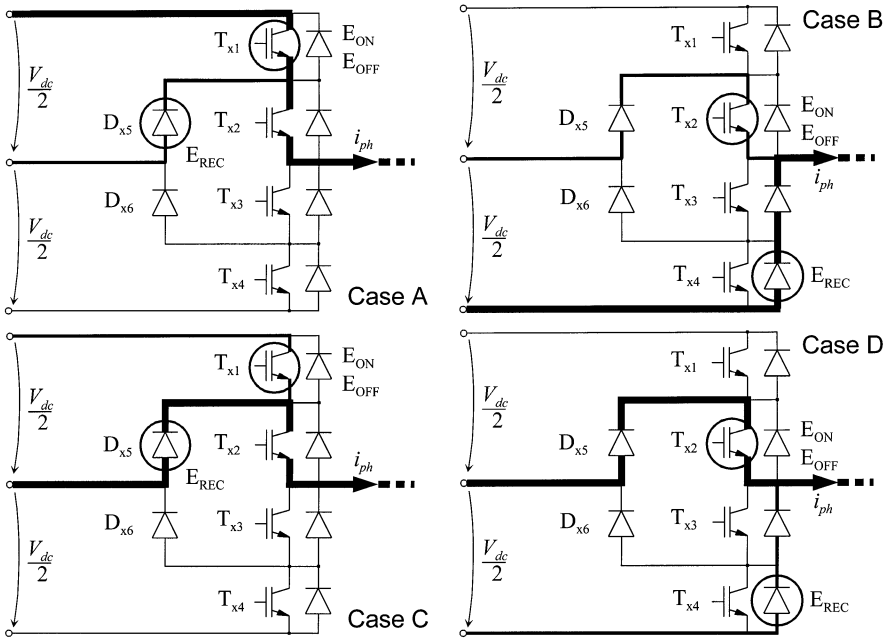

Fig. 4. Conduction and switching stresses in the NPC VSC for positive instantaneous phase current. Case A: $pf = 1,\ M = 1.15$. Case B: $pf = -1,\ M = 1.15$. Case C: $pf = 1,\ M \approx 0$. Case D: $pf = -1,\ M \approx 0$.

lower switching losses in the example being examined. Both these effects compensate each other to a large extend, such that the junction temperatures are a better basis for comparison than the losses. Nevertheless, in Fig. 2(b) the diodes D_{out} are clearly identified as the most stressed devices (regardless of semiconductor characteristics) since they do experience both, significant switching and significant conduction losses exclusively.

For small modulation depths, different modulation schemes distribute the losses differently. Applying conventional, continuous modulation methods for $M \approx 0$ the NPC diodes D_{npc} are most stressed for inverter operation [Fig. 2(c)], while the inner switches T_{in} experience highest losses for rectifier operation [Fig. 2(d)]. The junction temperature imbalance in these cases is immense. However, for a modulation principle called "two-level SVM" the junction temperature distribution is more balanced, as can be observed from Figs. 3(c) and (d). Here, the inner switches experience the highest junction temperature for both, inverter and rectifier operation. The four operating points of Figs. 2 and 3 will be referred to as Cases A–D throughout the paper.

The reasons for the different loss distributions at the different operating points and for the different strategies are explained in the following, firstly for conventional SVM, and secondly for two-level SVM. They can be found in the relation of the equivalent reference waveforms to the phase current. Case A is the simplest case. Consider a single phase leg of the NPC VSC with conventional SVM. For $pf = 1$, phase current and voltage reference are in phase, i.e., for $i_{ph} > 0$ the converter switches between "+" and "0". The outer switch T_{x1} commutates with the NPC diode D_{x5}. The inner switch T_{x2} conducts the phase current for the entire half wave. T_{x1} conducts for nearly the same time (large M!) and additionally experiences switching losses. Thus, T_{x1} is clearly the most stressed device. D_{x5} experiences the corresponding recovery losses and only a small fraction of conduction losses. The situation is visualized in Case A of Fig. 4, where the bold line indicates the current path for long duty cycles and the narrower line for short duty cycles, respectively. The reference and current waveforms are shown in Fig. 5(b).

For Case B ($pf = -1$) the current is 180° phase shifted to the reference function, i.e., for $i_{ph} > 0$ the converter switches between "0" and "−". The outer inverse diode D_{x4} commutates with the inner switch T_{x2} (Case B of Fig. 4). The inverse diodes D_{x3} and D_{x4} both conduct for the predominant part of the time, while D_{x4} also experiences recovery losses. T_{x2} conducts only for small duty cycles but it is stressed with significant turn-on and turn-off losses. Nevertheless, D_{x4} is identified as the most stressed device, as has been discussed before. In Case B, the ϑ_j distribution is somewhat worse compared to Case A, even if the maximum junction temperature is lower in the example being examined. The inner switch and the inner diode are both stressed with considerable losses. Since in the typical case of IGBT modules, IGBT and diode are in the same housing, T_{in} and D_{in} also reach significant junction temperatures. The NPC diodes experience very little conduction losses only, whereas in Case A every group of devices (inner, outer, and NPC) experiences substantial losses.

Cases C and D with conventional SVM shown in Fig. 4 differ only as conduction losses are shifted compared to Cases A and B. For $M \approx 0, pf = 1$, the NPC diode D_{x5} takes over the majority of conduction time from T_{x1}. Since it also experiences recovery losses, it is the most stressed device in Case C. For Case D, D_{x5} and T_{x2} carry the current most of the time, while T_{x2} also experiences turn-on and turn-off losses. Thus, it is the most stressed device.

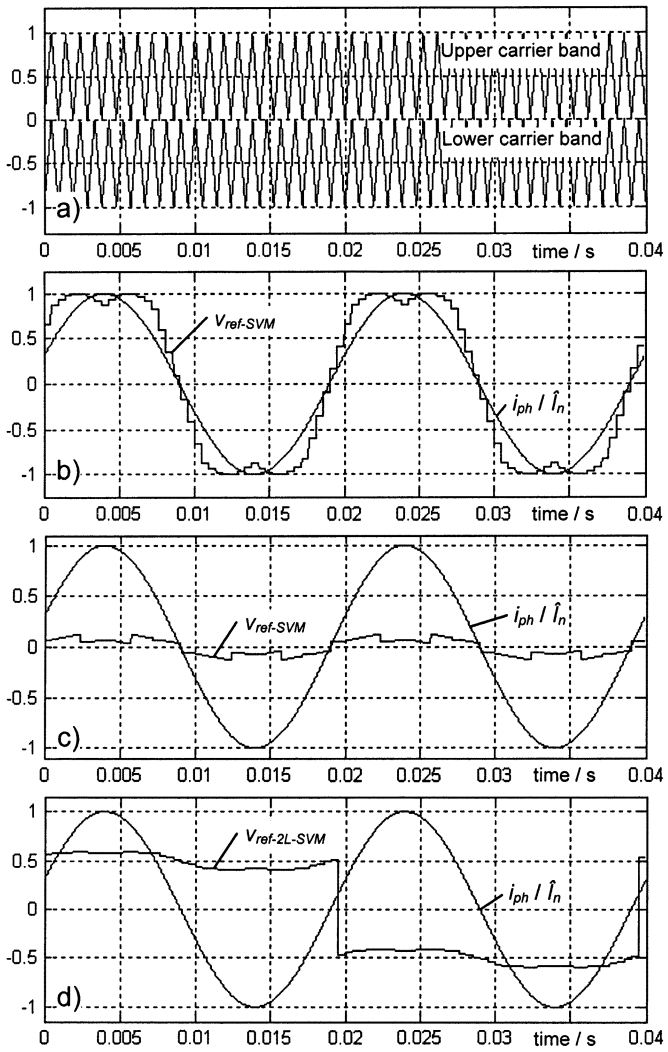

Fig. 5. Carrier-based modulation for the three-level NPC VSC. (a) Carrier signals. (b) Normalized phase current and equivalent reference waveform for conventional SVM with centered middle vectors for $(M = 1.15,\ pf = 1)$. (c) Same for $(M = 0.1,\ pf = 1)$. (d) Waveforms for two-level SVM $(M = 0.1,\ pf = 1)$.

Observation of Fig. 2 reveals that the two-level SVM yields nearly the same good loss distribution for both Cases C and D. Ideas for this kind of modulation date back to the early 1990s [7]. In [10], the two-level SVM was identified to be especially advantageous with respect to the loss and junction temperature distribution, as well as total losses and harmonic distortion. However, the scheme can be used for small modulation depths $(M \leq 0.5775)$ exclusively. Contrary to the conventional SVM for three-level converters, either the upper or the lower part of the converter is utilized for certain intervals only. The inner hexagon of the space-vector plot (see Fig. 1) is treated as a two-level converter utilizing the upper (0 to $+$) or the lower set ($-$ to 0) of redundant switch states. The modulation sequence starts at the origin instead of at the equivalent null vectors located on the inner hexagon. In the sense of carrier-based modulation, this means that the reference functions for all three phases are shifted into the upper or lower carrier band by a common-mode dc offset of ± 0.5, respectively. The common-mode offset can be arbitrarily switched between $+0.5$ and -0.5 without any effect on the output voltage[4]. This characteristic is used to distribute the losses between the converter switches and also to control the neutral-point potential. The sets of redundant switch states are alternated as the reference functions are swapped between the carrier bands. Fig. 5(d) depicts an example where the common-mode dc offset changes at half the fundamental frequency of output voltage and current. The same condition is assumed for the calculation of the loss and junction temperature distributions of Figs. 2(c) and (d) and 3(c) and (d). For comparison, the equivalent reference waveform for conventional three-level SVM is depicted in Fig. 5(c) for a small modulation index [12].

The nearly identical behavior of the two-level SVM for both, Cases C and D, is not a coincidence. For a very small modulation depth the voltage-forming part of the equivalent reference waveform becomes nearly flat, as can be seen in Fig. 5(d). All that remains is the dc offset shifting the reference in the upper or lower carrier band. The reference stays in the upper carrier band spanning [1, 0], realizing positive and negative sinusoidal output voltages for equal amounts of time. Then, it stays in the lower carrier band spanning $[0, -1]$, realizing positive and negative output voltages. When the reference function approaches an ideal square wave for $(M \rightarrow 0)$, the phase shift of the current has no effect on the loss distribution. For the sections with $i_{\rm ph} > 0$ the converter switches between "+" and "0" as well as "0" and "−". Thus, the two-level SVM realizes a mix of the situations described before for conventional SVM. The loss distributions for inverter and rectifier operation are averaged. Graphically, this is visible in Figs. 2 and 3. The loss and also the ϑ_j distribution for two-level SVM are approximately (*not* precisely) made up of the average of the four distributions for conventional SVM in Cases A–D.

Finally, an important operating area in electric drive systems has to be mentioned: zero speed. Depending on the type of machine, it is characterized by a fundamental output frequency being zero or close to zero, and a very low modulation depth. Due to the low output frequency the devices of one phase may be stressed with the peak value of the phase current for a time long enough to reach thermal steady state. The converter design method based on average junction temperatures, which is used for output frequencies of $f_0 > 5$ Hz, is no longer applicable. Two-level SVM is also well suited for this most critical operating point. While the instantaneous values of the target voltage remain nearly unchanged over long periods, the references can alternate between the carrier bands frequently, thus distributing the losses among all converter switches. Nevertheless, the loss distribution is worse and the achievable phase current is cut down compared to rated operation.

The characteristics discussed before stand in contrast to what is desired for high-power converters. Naturally, a high utilization of the installed switch power or installed silicon area is desired to achieve a minimum converter cost per kVA. At zero speed, applications like hot and cold rolling mills typically demand up to 250% of rated torque and hence more than twice the rated phase current. However, the uneven loss distribution

[4]Please note, that a common-mode offset is equally added to all three phase references which are 120° phase shifted. It does not contribute to the output voltage, but is cancelled in the line-to-line voltage.

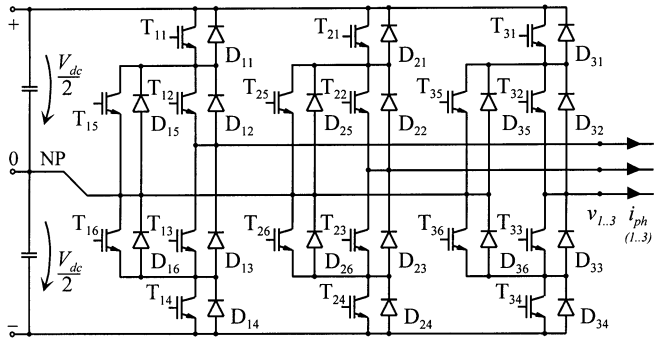

Fig. 6. Three-level NPC VSC with active NPC switches—ANPC VSC.

of the three-level NPC VSC and the resulting unequal junction temperature distribution clearly limit the maximum phase current and the silicon utilization of this topology. While a more equal (but still not ideal) junction temperature distribution at small modulation indexes ($f_0 \gg 0$) can be reached by two-level SVM, the extreme unbalance at large modulation indexes is a substantial, inherent disadvantage of the three-level NPC VSC. In the case of zero speed ($f_0 \approx 0$) the distribution is even worse. The practical consequence is a drastic "current" overrating (e.g., 30%–50%) of the semiconductors of commercially available three-level NPC converters in applications, where full torque at zero speed is requested.

III. Three-Level ANPC VSC

The ANPC VSC is a derivative of the NPC VSC. It features additional active switches in antiparallel to the NPC diodes, as depicted in Fig. 6. Active NPC switches have already appeared in the literature previously. In [14], auxiliary switches are proposed to guarantee an equal voltage sharing between the main devices T_{x1}/T_{x2} and T_{x3}/T_{x4}, respectively. Otherwise, a balancing resistor across the inner switches would be required. This solution is commonly applied in industrial converters today. In the case of a series connection of IGBTs as main switches, active NPC switches can ensure the equal voltage sharing of the series-connected NPC diodes [3]. The antiparallel NPC IGBTs are then operated in the active region (active clamping). However, even for modularity and standardization reasons, IGBT modules are installed instead of single NPC diodes in some commercially available medium-voltage pulsewidth-modulation (PWM) converters. If no active clamping is necessary (no series connection), they are turned off by an external gate-emitter short while the integrated inverse diode acts as NPC diode.

Although the use of active NPC switches is economically advantageous today, its technical capabilities were not exploited by far. The full potential of the ANPC VSC was first discovered and discussed in [11]. The active NPC switches make new switch states and new commutations possible compared to the NPC VSC. They allow a specific utilization of the upper and lower path of the neutral tap and, thus, affect the distribution of conduction and switching losses. Therewith, a mitigation of the loss distribution problem discussed in Section II can be achieved. The detailed effect of the new switch states and commutations on the loss distribution is discussed below.

TABLE I
Switch States of the Diode-Clamped Three-Level NPC VSC

	T_{x1}	T_{x2}	T_{x3}	T_{x4}
State "+"	1	1	0	0
State "0"	0	1	1	0
State "–"	0	0	1	1

TABLE II
Switch States of the Three-Level ANPC VSC.

	T_{x1}	T_{x2}	T_{x3}	T_{x4}	T_{x5}	T_{x6}
State "+"	1	1	0	0	0	1
State "0U2"	0	1	0	0	1	0
State "0U1"	0	1	0	1	1	0
State "0L1"	1	0	1	0	0	1
State "0L2"	0	0	1	0	0	1
State "–"	0	0	1	1	1	0

A. Switch States

Consider a single phase leg of the circuit shown in Fig. 6. In contrast to the conventional diode-clamped NPC VSC, in the phase leg with active NPC switches there is more than one switch state to realize one phase's connection to the neutral point (subsequently called zero state of the phase). The switch states of the diode-clamped NPC VSC and of the ANPC VSC are given in Tables I and II, respectively.

In the NPC VSC the utilization of the upper or lower NPC path is determined by the direction of the phase current. The switches T_{x2} as well as T_{x3} are always turned on in the "0" state. If active NPC switches are applied, by turning on T_{x5} and T_{x2} the phase current can be conducted through the upper path of the neutral tap in both directions. In the same manner, by turning on T_{x6} and T_{x3} the phase current can be conducted through the lower path of the neutral tap in both directions. Of course, all four switches T_{x5}, T_{x2}, T_{x6}, and T_{x3} of the phase considered could be turned on at once. Then, the current distribution between the upper and the lower NPC path is not precisely defined. It would be determined by the on-state characteristics of the devices being used, the prior switch state, and parasitic inductances. Therefore, this state is not investigated further. If the upper NPC path is utilized (T_{x6} and T_{x3} are off) T_{x4} may be in on or off state. This is also true for T_{x1} during the conduction of the lower NPC path (T_{x5} and T_{x2} are off). The resulting four switch states are designated "0L2", "0L1", "0U1", and "0U2", respectively.

During the "+" state T_{x6} should be turned on to guarantee an equal voltage sharing between T_{x3} and T_{x4}. Analogously, T_{x5} should be turned on during the "−" state. Thus, the voltage-balancing resistors across the inner switches can be saved. The distribution of conduction losses during the zero states can be controlled by the selection of the upper or lower NPC path. The conduction losses in the states "+" and "−" cannot be influenced.

B. Commutations

The commutations to or from the new states "0U2", "0U1", "0L1", and "0L2" determine the distribution of the switching losses. All commutations take place between one active switch

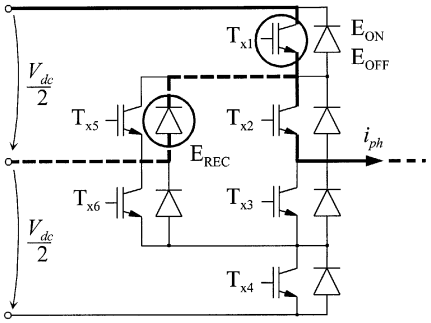

Fig. 7. Commutations in the ANPC VSC: type 1 ($+ \leftrightarrow$ 0U2, $+ \leftrightarrow$ 0U1).

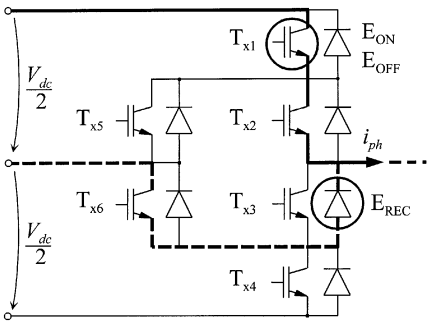

Fig. 8. Commutations in the ANPC VSC: type 2 ($+ \leftrightarrow$ 0L2).

and one diode. Even if more than two devices turn on or off, only one active switch and one diode experience essential switching losses. All remaining devices being involved do not simultaneously take over blocking voltage and carry current during the commutation.

The **conventional commutation $+ \rightarrow 0$** without use of the active NPC switches is recapitulated first. As an example assume an operating condition with a positive phase current and a positive output voltage. The converter phase leg is switched from the positive dc rail (state "+") to the neutral tap (zero state). In the conventional NPC VSC, T_{x1} is turned off and T_{x3} is turned on after a dead time. The current commutates from T_{x1} to D_{x5}. The switches T_{x2} and T_{x4} stay on and off, respectively. Essential switching losses occur in T_{x1}.

The four possible forced commutations[5] from "+" to the zero states in the ANPC VSC are investigated subsequently. During the **commutation $+ \rightarrow$ 0U2** the phase current commutates to the upper path of the neutral tap (Fig. 7). First, T_{x6} has to be turned off, then T_{x1} is turned off and finally (after a dead time) T_{x5} is turned on. As in the conventional commutation T_{x1} experiences switching losses. The **commutation $+ \rightarrow$ 0U1** differs from the commutation $+ \rightarrow$ 0U2 only by the additional lossless turn-on of T_{x4} after the turn-on of T_{x5}. This additional switching transient does not yield a positive effect. Therefore, this commutation is not used.

Through the **commutation $+ \rightarrow$ 0L2** the phase current is commutated to the lower path of the neutral tap (Fig. 8). T_{x1} is turned off and T_{x3} is turned on after a dead time. Since T_{x6} is in the on-state, the current commutates to both, upper and lower path of the neutral tap. T_{x1} experiences notable turn-off losses. By turning off T_{x2} slightly delayed to T_{x1} at zero voltage the entire phase current is forced to the lower path of the neutral tap (which is already conducting) without significant additional losses. During the **commutation $+ \rightarrow$ 0L1** the phase current also commutates to the lower NPC path (Fig. 9). In contrast to the commutation described before T_{x1} remains in the on-state. Only T_{x2} is turned off and T_{x3} is turned on after a dead time. The phase current commutates directly to the lower NPC path. The switch T_{x2} experiences turn-off losses.

[5]Forced or capacitive commutations are characterized by a negative gradient of the converter output power. They are always initiated by an active turn-off transient. The contrary natural or inductive commutations realize a positive gradient of the output power. They are initiated by an active turn-on transient.

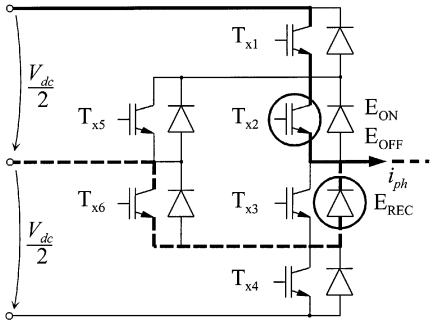

Fig. 9. Commutations in the ANPC VSC: type 3 ($+ \leftrightarrow$ 0L1).

For a better understanding the natural commutations from the zero states back to "+" are also explained briefly. During all forced commutations described above only one actively turned-off switch is subject to essential switching losses. During the natural commutations one active switch and one diode experience essential turn-on and reverse recovery losses, respectively. All switching transitions take place in a reverse order. The conventional commutation in the NPC VSC is started by the turn-off of T_{x3}. After the turn-on of T_{x1} the phase current commutates to the positive dc rail. T_{x1} and D_{x5} experience switching losses. In the ANPC VSC, during the commutation 0U2 $\rightarrow +$ the switch T_{x5} is turned off first (Fig. 7). The phase current commutates to the positive dc rail after the turn-on of T_{x1}. Finally, T_{x6} is turned on. Switching losses also occur in T_{x1} and D_{x5}. The commutation 0U1 $\rightarrow +$ is initiated by the turn-off of T_{x4} and T_{x5}. Following T_{x1} and T_{x6} are turned on after corresponding dead times. This commutation is only used at the transition from the modulation of a negative voltage to the modulation of a positive voltage. Again, switching losses occur in T_{x1} and D_{x5}.

During the commutation 0L2 $\rightarrow +$ the switch T_{x2} is turned on first, followed by the turn-off of T_{x3} (Fig. 8). Not until the final turn-on of T_{x1} does the phase current commutate back to the positive dc rail. Essential switching losses occur in T_{x1} and D_{x3}. The commutation 0L1 $\rightarrow +$ is started by the turn-off of T_{x3} (Fig. 9). The current commutates after T_{x2} is turned on. Switching losses occur in T_{x2} and D_{x3}.

Summarizing the above descriptions, one can distinguish between three different types of commutations with respect to losses. For a positive phase current and a positive output voltage, switching losses occur in T_{x1} and D_{x5} during the commutation $+ \leftrightarrow$ 0U2 (type 1). Utilizing the commutation $+ \leftrightarrow$ 0L2 instead, switching losses are shifted from the NPC diode D_{x5} to the inner inverse diode D_{x3} (type 2).

TABLE III
DEVICE SWITCHING LOSSES IN THE THREE-LEVEL ANPC VSC

Commuta - tion type		T_{x1}	D_{x1}	T_{x2}	D_{x2}	T_{x3}	D_{x3}	T_{x4}	D_{x4}	T_{x5}	D_{x5}	T_{x6}	D_{x6}
	Positive phase current												
1	+ ↔ 0U2	×									×		
1	+ ↔ 0U1	×									×		
3	+ ↔ 0L1			×			×						
2	+ ↔ 0L2	×					×						
2	0U2 ↔ -			×					×				
3	0U1 ↔ -			×			×						
1	0L1 ↔ -								×			×	
1	0L2 ↔ -								×			×	
	Negative phase current												
1	+ ↔ 0U2		×							×			
1	+ ↔ 0U1		×							×			
3	+ ↔ 0L1				×	×							
2	+ ↔ 0L2		×			×							
2	0U2 ↔ -				×			×					
3	0U1 ↔ -				×	×							
1	0L1 ↔ -							×					×
1	0L2 ↔ -							×					×

Furthermore, the switching losses of T_{x1} can be shifted to T_{x2} applying the commutation + ↔ 0L1 (type 3). Analogously the mechanism of these three types of commutations applies to all operating conditions. Table III shows the distribution of the main switching losses for positive and negative currents as well as modulation of positive and negative voltages for all commutations.

IV. ACTIVE LOSS BALANCING

The different commutations and zero states in the ANPC VSC can be used to distribute losses more evenly among the semiconductors. The intention is not to save total converter losses, but to distribute them equally. The total losses remain nearly unchanged. This statement can be concluded from the fact that only one active switch and one diode experience essential switching losses during each commutation. Since the commutation voltage and current are the same, also the switching losses for all three types of commutations are identical under ideal conditions, e.g., negligible stray inductances etc. Differences in the real commutation loop are addressed in Section VI. Secondly, the conduction losses are also identical for all zero states. Then, always one diode and one active switch conduct the phase current. During the active states "+" and "−" two active switches or two diodes are conducting dependent on the direction of the phase current.

Loss balancing can be achieved within the converter phase legs, but not between different phases. Specifically, in cases where the outer devices are most stressed (Cases A and B of Fig. 2), they can be relieved by the appropriate use of type-1 and type-3 commutations. If inner or NPC devices are most stressed (Cases C and D), the alternating use of type-1 and type-2 commutations yields a better loss distribution. The general approach to optimize the ϑ_j distribution is to keep the hottest of all devices always as cool as possible. For that, the junction temperatures of all devices must be estimated. With this knowledge, appropriate commutations and zero states are selected.

A block diagram of a digital control system to fulfill this task is depicted in Fig. 10. This system is inserted after the

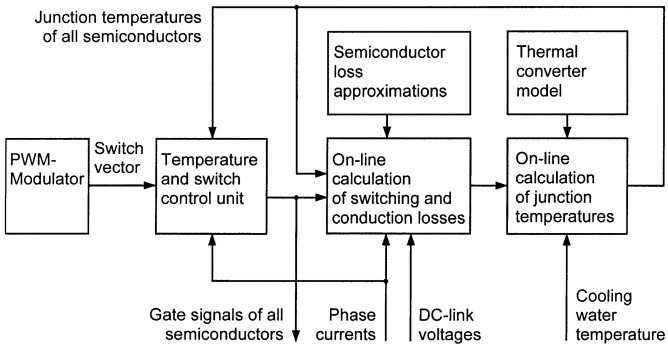

Fig. 10. Block diagram of the loss-balancing system.

conventional PWM modulator for the NPC VSC. It consists of two functional units: the online calculation of losses and junction temperatures, and the generation of gate signals for the 18 switches of the ANPC VSC. Semiconductor losses are calculated from sampled phase currents, half dc-link voltages, and estimated junction temperatures similar to [15], i.e.,

$$P_{\mathrm{cond}X} = v_{0X}(1 + C_{1X}\vartheta_{jX}) \cdot i_{\mathrm{ph}} + r_{FX}(1 + C_{2X}\vartheta_{jX}) \cdot i_{\mathrm{ph}}^2, \quad (1)$$

$$P_{\mathrm{sw}X} = (A_{\mathrm{sw}X} + B_{\mathrm{sw}X} \cdot i_{\mathrm{ph}} + C_{\mathrm{sw}X} \cdot i_{\mathrm{ph}}^2) \cdot \frac{V_{\mathrm{dc}}}{2} \cdot \frac{1}{T_{\mathrm{sample}}} \quad (2)$$

where v_{0X} and r_{FX} are the semiconductor's on-state parameters and A_X, B_X, C_X denote fitting constants. The obtained conduction losses are sampled instantaneous values. The switching loss energies are converted into nearly instantaneous power quantities by averaging them over the sample time T_{sample} of the control system. Conduction losses of IGBTs $P_{\mathrm{cond}T}$ and diodes $P_{\mathrm{cond}D}$, turn-on losses P_{on} and turn-off losses P_{off} of IGBTs, and recovery losses P_{rec} of diodes are taken into account with the aid of the equations given above. The estimated losses are fed into a thermal model of the converter in the form of a Foster equivalent network [16], [17]. Its elements consist of a paralleled thermal resistance R_{th} and capacitance C_{th}. Analysis for the single $R_{\mathrm{th}}C_{\mathrm{th}}$ element yields

$$T(k+1) = \left(1 - \frac{T_{\mathrm{sample}}}{R_{\mathrm{th}}C_{\mathrm{th}}}\right) \cdot T(k) + \left(\frac{T_{\mathrm{sample}}}{C_{\mathrm{th}}}\right) \cdot P_{\mathrm{loss}}(k) \quad (3)$$

where the state variable T is the temperature across C_{th}, and P_{loss} are the losses impressed into the specific $R_{\mathrm{th}}C_{\mathrm{th}}$ element. For the entire system the state-space description can be formulated as

$$\underline{T}(k+1) = \underline{A} \cdot \underline{T}(k) + \underline{B} \cdot \underline{P_{\mathrm{loss}}}(k) \quad (4)$$

$$\underline{\vartheta_j}(k) = \underline{C} \cdot \underline{T}(k) + \underline{D} \cdot \vartheta_a(k). \quad (5)$$

The state variables of the single $R_{\mathrm{th}}C_{\mathrm{th}}$ elements in the system do not influence each other. Thus, the system matrix $\underline{A}$ contains only elements as in (3) on the diagonal and is otherwise empty. The matrix $\underline{B}$ is responsible for allocating losses to the appropriate semiconductors, dependent on the switch states and commutations during the sampling period (e.g., see Table III for switching losses). Thus, $\underline{B}$ is time variant. Beside terms as in (3), it contains functions of the reference v_{ref} to split the

TABLE IV
DECISION CHART FOR COMMUTATIONS TO THE ZERO STATES

Modulation	Phase current	Junction temperatures			Zero state
Positive voltage (+ → 0)	$i_{ph} > 0$	$\vartheta_{jTx1} > \vartheta_{jTx2}$	$\vartheta_{jDx5} > \vartheta_{jDx3}$		0L1
			$\vartheta_{jDx5} < \vartheta_{jDx3}$	$\vartheta_{jTx1} > \vartheta_{jDx3}$	0L1
				$\vartheta_{jTx1} < \vartheta_{jDx3}$	0U2
		$\vartheta_{jTx1} < \vartheta_{jTx2}$	$\vartheta_{jDx5} > \vartheta_{jDx3}$		0L2
			$\vartheta_{jDx5} < \vartheta_{jDx3}$		0U2
	$i_{ph} < 0$	$\vartheta_{jDx1} > \vartheta_{jDx2}$	$\vartheta_{jTx5} > \vartheta_{jTx3}$		0L1
			$\vartheta_{jTx5} < \vartheta_{jTx3}$	$\vartheta_{jDx1} > \vartheta_{jTx3}$	0L1
				$\vartheta_{jDx1} < \vartheta_{jTx3}$	0U2
		$\vartheta_{jDx1} < \vartheta_{jDx2}$	$\vartheta_{jTx5} > \vartheta_{jTx3}$		0L2
			$\vartheta_{jTx5} < \vartheta_{jTx3}$		0U2
Negative voltage (- → 0)	$i_{ph} > 0$	$\vartheta_{jTx2} > \vartheta_{jTx6}$	$\vartheta_{jDx4} > \vartheta_{jDx3}$	$\vartheta_{jTx2} > \vartheta_{jDx4}$	0L2
				$\vartheta_{jTx2} < \vartheta_{jDx4}$	0U1
			$\vartheta_{jDx4} < \vartheta_{jDx3}$		0L2
		$\vartheta_{jTx2} < \vartheta_{jTx6}$	$\vartheta_{jDx4} > \vartheta_{jDx3}$		0U1
			$\vartheta_{jDx4} < \vartheta_{jDx3}$		0U2
	$i_{ph} < 0$	$\vartheta_{jDx2} > \vartheta_{jDx6}$	$\vartheta_{jTx4} > \vartheta_{jTx3}$	$\vartheta_{jDx2} > \vartheta_{jTx4}$	0L2
				$\vartheta_{jDx2} < \vartheta_{jTx4}$	0U1
			$\vartheta_{jTx4} < \vartheta_{jTx3}$		0L2
		$\vartheta_{jDx2} < \vartheta_{jDx6}$	$\vartheta_{jTx4} > \vartheta_{jTx3}$		0U1
			$\vartheta_{jTx4} < \vartheta_{jTx3}$		0U2

sampling period up into the conduction periods of the different devices. The state variables and the ambient temperature are added up to the junction temperatures in (5). $\underline{C}$ and $\underline{D}$ contain only values of one and zero.

Based on the estimated instantaneous junction temperatures and sampled phase currents the "Temperature and switch control unit" selects the most suitable commutations and zero states for the coming sampling period. An algorithm to ensure that the semiconductor with the highest estimated junction temperature is not stressed with significant switching losses is given in Table IV. For example, if a positive instantaneous voltage is modulated ($v_{\mathrm{ref}} > 0$), the phase current is positive, and the instantaneous junction temperatures are $\vartheta_{jTx1} > \vartheta_{jTx2}$, and $\vartheta_{jDx5} > \vartheta_{jDx3}$, "0L1" is selected as the next zero state. Conduction losses are not reflected in this algorithm. However, for a properly designed converter where conduction and switching losses are in the same range, the algorithm yields the most equal distribution of the instantaneous junction temperatures possible. The algorithm requires a fast computation and decision making for every second commutation. This can be accomplished by today's micro controllers, but is not required necessarily. As an alternative, one could define two discrete factors giving the ratio for the use of the three different types of commutations. Slowly computed average junction temperatures can adapt these factors.

As phase currents, dc-link voltages, and cooling water temperature are monitored anyway, no additional sensors are necessary. The entire control system can be implemented using only two additional components. A micro controller is well suited for all online calculations. Time-critical tasks such as the generation of the gate signals can be taken over by an additional programmable logic device.

One example illustrating the operation of the system is explained in the following. Fig. 11(a) shows the estimated instantaneous junction temperature vs. time without loss balancing for Case A ($M = 1.15,\ pf = 1$). As expected, the devices $\mathrm{T_{x1}}, \mathrm{T_{x2}}$, and $\mathrm{D_{x5}}$ experience losses during the positive half wave of the phase current and cool down during the negative half wave. There is a maximum junction temperature ripple of about 6 K with the fundamental frequency f_0. The average values equal that of Fig. 3(a). Small jumps of the junction temperatures of $\mathrm{T_{x1}}$ and $\mathrm{D_{x5}}$ occur during the switching transitions. Fig. 12(a) depicts the waveforms for the same operating point with loss balancing. Now, the junction temperatures of $\mathrm{T_{x1}}$ and $\mathrm{T_{x2}}$ are nearly identical, ϑ_{jTx1} has decreased, and ϑ_{jTx2} has increased. The average junction temperature of $\mathrm{T_{x1}}$, i.e., the highest junc-

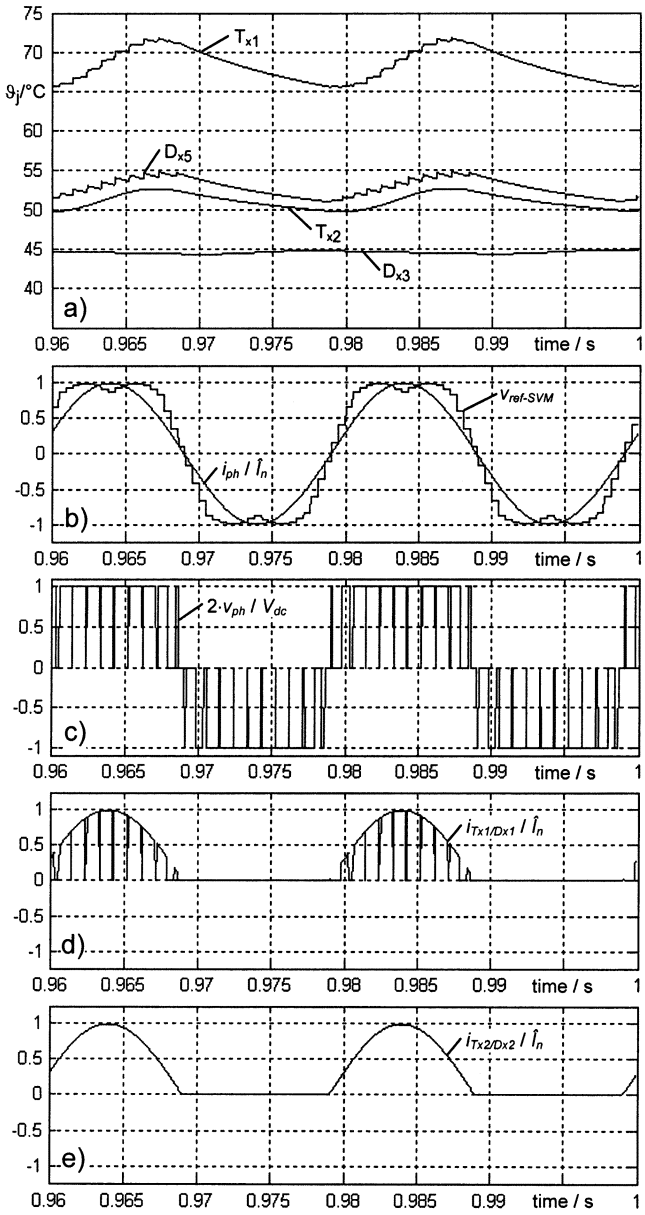

Fig. 11. Simulated junction temperatures and normalized electrical waveforms versus time without loss balancing. (a) Selected junction temperatures. (b) Corresponding reference waveform for SVM and phase current. (c) Phase-to-NP voltage. (d) Current through $\mathrm{T_{x1}}/\mathrm{D_{x1}}$. (e) Current through $\mathrm{T_{x2}}/\mathrm{D_{x2}}$ (Eupec FZ 1200 R33 KF2, $V_{\mathrm{dc}} = 3400$ V, $I_{\mathrm{rms}} = 600$ A, $f_s = 1050$ Hz, $f_s/f_0 = 21,\ M = 1.15, pf = 1, \vartheta_a = 37\ ^{\circ}\mathrm{C}$).

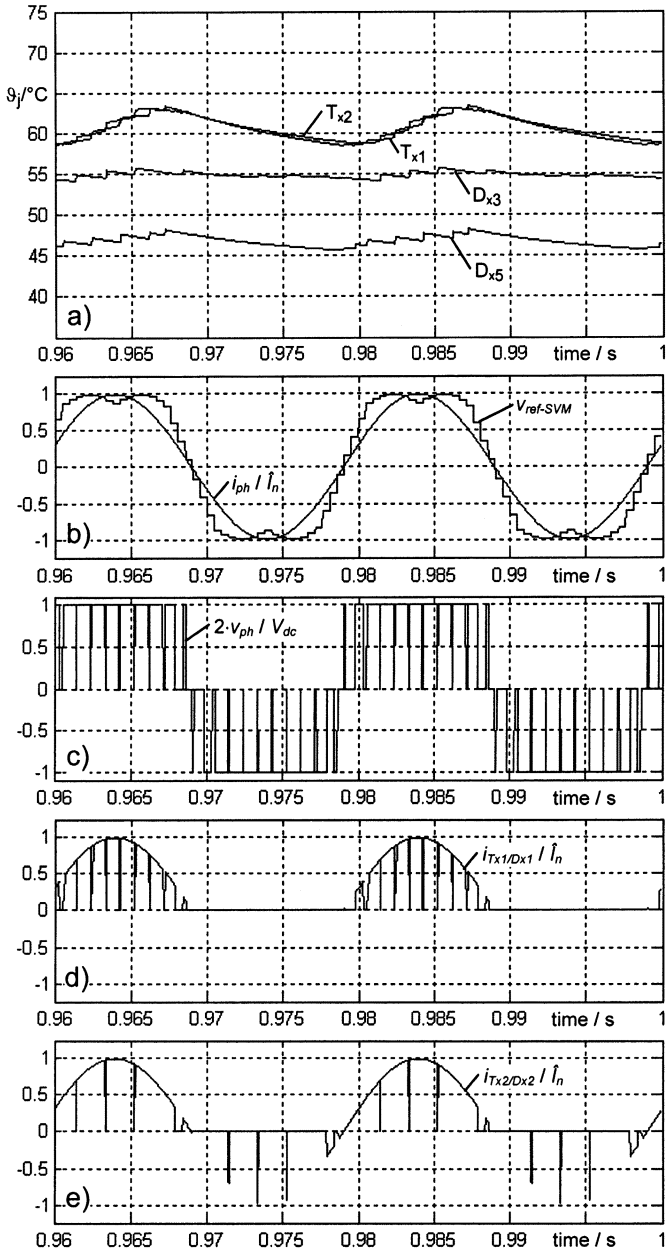

Fig. 12. Simulated junction temperatures and normalized electrical waveforms versus time with loss balancing (subplots and conditions as in Fig. 11).

tion temperature in the phase leg, is cut down from 68 °C to 61 °C. It can be observed that T_{x2} takes over switching losses when $\vartheta_{jTx1} > \vartheta_{jTx2}$. D_{x3} experiences the corresponding recovery losses. The commutations of type 1 $(T_{x1} - D_{x5})$ and type 3 $(T_{x2} - D_{x3})$ occur alternately. During the negative half wave $T_{x4} - D_{x6}$ and $T_{x3} - D_{x2}$ are involved in the type-1 and type-3 commutations, respectively.

The difference between conventional and loss-balanced operation is also visible in the current waveforms shown in Figs. 11(d) and (e) and 12(d) and (e). The current through the outer switch and diode T_{x1}/D_{x1} is identical for operation with and without loss balancing. T_{x1}/D_{x1} conduct only whenever the phase is connected to "+". For normal NPC operation at $pf = 1$, the inner switch T_{x2} conducts for the entire positive half wave without any switching transients. During the negative half wave, the lower NPC path is conducting; D_{x2} is not involved. For loss-balanced operation, T_{x2} is switched off for short pulses during the positive half wave, when the current is commutated to the lower NPC path by the type-3 commutations. Analogously, the diode D_{x2} takes over the current for short pulses during the negative half wave. This happens when the negative phase current is commutated from "−" to the upper NPC path by a turn-off of T_{x3} during the type-3 commutations.

V. Performance Evaluation of the Loss-Balanced ANPC VSC

To verify the analytical considerations and to quantify the benefits of the proposed system, extensive time-domain MATLAB simulations are performed for a typical industrial converter with $V_{\rm dc} = 3.4$ kV, $V_{\rm LL} = 2.3$ kV, and $I_{\rm rms} = 600$ A. The mathematical description of a single phase of the three-level ANPC converter is implemented in an M-file and solved numerically. The model includes the electric circuit, different modulation strategies, as well as semiconductor loss models, thermal models, and the loss-balancing system as described in Section IV. For simplicity, ideal dc voltages and ideally sinusoidal currents are impressed at the converters dc and ac terminals, respectively. The assumed main switches are Eupec 3.3-kV 1200-A single-IGBT modules [18], each installed on a separate water-cooled heat sink of the type Eupec KW51 ($R_{{\rm th}h-a} = 6$ K/kW at a water flow rate of $v_w = 6.2$ L/min). For this specific device, the thermal behavior is modeled by four internal series-connected $R_{\rm th}C_{\rm th}$ elements for junction-to-case (IGBT or diode separately) and two common elements per module for case-to-ambient. The loss coefficients $A_{\rm on}, B_{\rm on}, C_{\rm on}, A_{\rm off}, B_{\rm off}$, etc., as in (1) and (2) and thermal impedances $R_{\rm th}, C_{\rm th}$ as in (3) are extracted from the datasheet. For the modulation the superior principles of asymmetric regular sampling, phase-disposed carrier signals, and centered middle vectors [12] are applied, as shown in Fig. 5.

An important issue for the thermal design of the converter which has to be considered is thermal cycling. To determine the maximum allowable junction temperature one has to take the load cycles of the prospective application into account. Junction temperature cycles cause mechanical stress especially to the die-attach solder joint and the bond connections and, thus, decrease the lifetime of the IGBT modules. Therefore, to limit this thermomechanical stress the converter is designed such that the maximum junction temperature rise does not exceed $\Delta T_j = 30$ K [13]. This design rule applied here is industrial practice for applications with repetitive cyclic duty. Please note that the thermal cycles considered are caused by load cycles in the range of seconds. They are not the fast junction temperature ripple with the fundamental frequency.

Fig. 13 shows the balanced junction temperature distribution in the ANPC VSC at the operating points of Fig. 3. Case A has already been discussed in Section IV. Case B shows a similar behavior. Again, the junction temperature of the hottest device $(D_{\rm out})$ is cut down. However, also, the junction temperature of the alternative switching device $(D_{\rm in})$ is reduced slightly. This is due to the fact that for normal operation without loss balancing

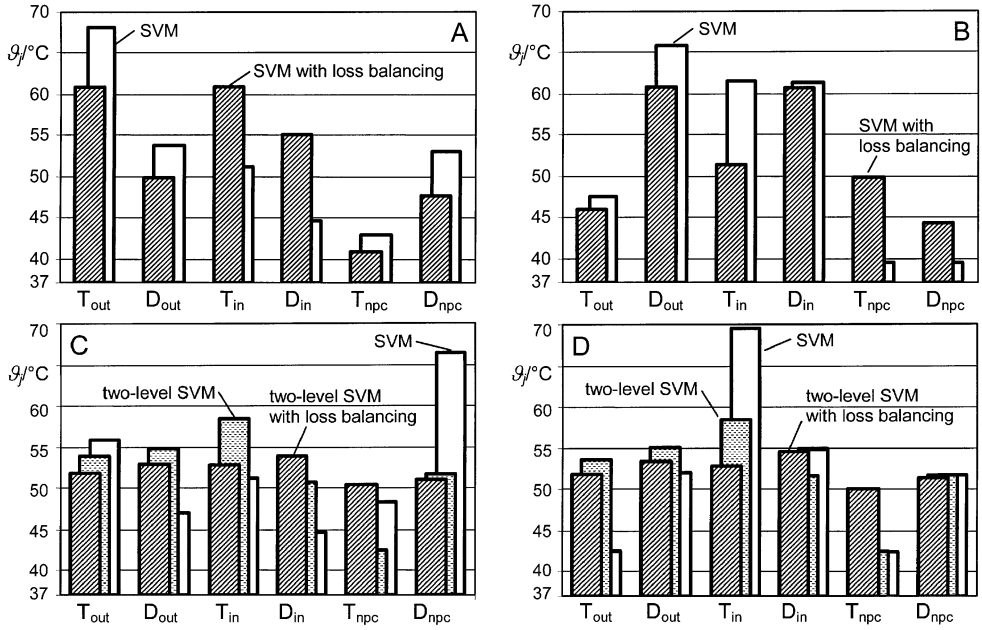

Fig. 13. Simulated average ϑ_j distribution applying loss balancing in a three-level ANPC VSC featuring Eupec IGBTs ($V_{\rm dc} = 3400$ V, $I_{\rm rms} = 600$ A, $f_s = 1050$ Hz, $\vartheta_a = 37$ °C, Eupec FZ 1200 R33 KF2). (a) $pf = 1,\ M = 1.15$. (b): $pf = -1,\ M = 1.15$. (c) $pf = 1,\ M = 0.05$. (d) $pf = -1,\ M = 0.05$.

commutations equivalent to type 2 are utilized (compare with Case B of Fig. 4). Utilizing type-1 and type-3 commutations instead, the inner switch is relieved from part of its switching losses, having an effect on $\vartheta_{jT\rm in}$, too. The ϑ_j distribution for two-level SVM at low modulation depth has also further been improved. Here, the junction temperatures of none devices are absolutely equaled. The reason therefore is the mix of the cases of Fig. 3. Cutting down the highest instantaneous temperature does not necessarily mean to reduce the highest average temperature in this situation.

However, from Fig. 13 it can be found that in all four cases the maximum ϑ_j (in relation to ϑ_a) can be reduced by 16% to 24%. This enables an increase of the rated output power of 20% for the entire range of operation. Alternatively, an increase of the carrier frequency from 1050 Hz (frequency ratio $f_s/f_0 = 21$) to 1950 Hz ($f_s/f_0 = 39$) is possible. For zero speed, the maximum current is enlarged dramatically from 300 to 500 A at $f_s = 1050$ Hz. Applying a reduced carrier frequency of $f_s = 450$ Hz, the rated current of the conventional NPC VSC is reached. Thus, the drastic derating of the converter current is no longer necessary. The effective improvements are summarized in Fig. 14.

The loss-balancing system is especially advantageous for IGBT converters, in which the output power is limited by thermal constraints and not by the current turn-off capability. Where active NPC switches are already built in [3], a substantially increased output power is enabled without any additional semiconductor expense. However, beside the example examined, IGCT converters also are of interest. Here, the phase current is often limited by the semiconductor current turn-off capability. However, simulations showed that the switching frequency of a (3.3 kV, 9 MVA) IGCT converter could be increased from $f_s = 600$ Hz to 1350 Hz. This enables a substantial reduction of the output filter size in retrofit applications. In a filterless design, a substantially smaller current and torque ripple could be achieved.

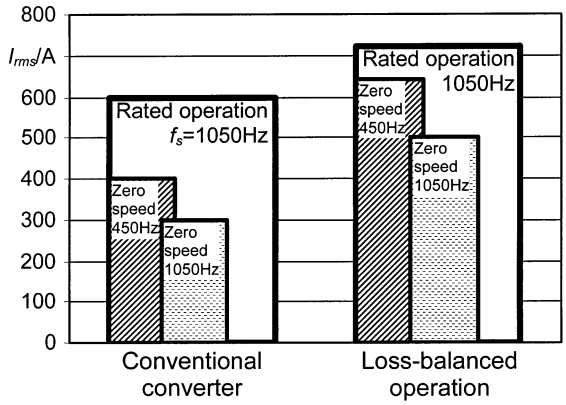

Fig. 14. Gain of achievable rms phase current in a 2.3-kV converter due to active loss balancing (with Eupec FZ 1200 R33 KF2).

The proposed principle can be applied to virtually all modulation schemes. The modulation itself, i.e., output voltage, zero sequence, current ripple, etc., are not affected. Hence, the modulation can be optimized with respect to other important constraints, e.g., torque ripple or neutral-point potential control. An online calculation of semiconductor losses and junction temperatures to improve the switch utilization is also known from [16], [19], and [20]. In [16], a reduction of the switching frequency and/or the phase current is proposed in case the junction temperature of one device exceeds its limit. This concept is extended in [19] to reduce stresses due to thermal cycling. Although this is a tempting idea, it seems rather unrealistic since in many applications the load strictly demands torque and speed. However, limiting the drive's performance in emergency cases ($f_s, I_{\rm rms}$-reduction) is better than a device failure. With the junction temperatures being estimated in the loss-balancing system this add-on feature can be easily implemented. A combination of a proper thermal management strategy with the proposed loss balancing is logical and straightforward.

TABLE V
RATINGS OF THE LABORATORY TEST SETUP

Configuration	three-phase AC/DC/AC converter
- line side	- 12-pulse diode rectifier
- load side	- three-level ANPC VSC
Main switches	SEMIKRON SKM 100 GB 123 D
Rated output power	S = 10kVA
Rated output voltage	V_{LL} = 400V
Nominal dc-link voltage	V_{dc} = 650V
Single-phase RL-Load	L_{LOAD} = 20mH; R_{LOAD} = 10Ω

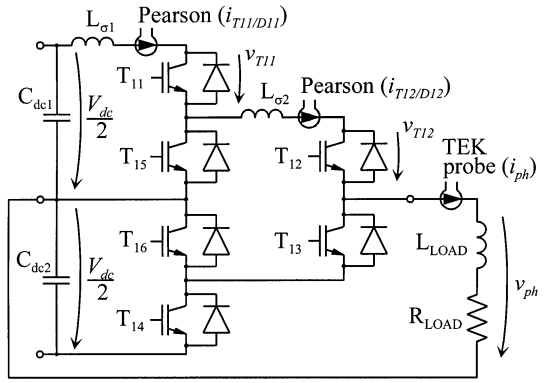

Fig. 15. Phase 1 of the low-voltage ANPC VSC test bench with single-phase *RL* load.

VI. EXPERIMENTAL VERIFICATION

To prove the operating principle of the ANPC VSC and to investigate parasitic effects during the commutations a low-voltage test bench is constructed. Though a low-voltage converter exhibits different thermal characteristics than converters in the megawatt power range, it is well suited to investigate the fundamental behavior of the ANPC VSC. The test bench's main structure and ratings are summarized in Table V. Its main switches are overrated in terms of current- and voltage-carrying capability by a factor of two to prevent destruction in failure cases. Each phase leg is assembled of three half-bridge IGBT modules, viz. T_{x1}/T_{x5}, T_{x2}/T_{x3}, and T_{x6}/T_{x4}. In phase leg 1, Pearson current transducers (type 410) are built in to enable the investigation of the new ANPC commutations. A schematic of phase 1 is depicted in Fig. 15. In a first step, measurements are performed with a single-phase *RL* load. Therefore, a purely sinusoidal modulation with no third harmonic and multiple components is realized.

As an example, a turn-off transient of T_{11} during a type-1 commutation from "+" to the upper path of the neutral tap ("0U2") and a turn-off transient of T_{12} during a type-3 commutation to the lower path of the neutral tap ("0L1") are shown in Figs. 16 and 17, respectively. Both commutations display proper performance. The only distinct difference is the higher peak voltage during the turn-off of T_{12}. This is due to the higher inductance in the commutation loop, which includes C_{dc1}–$L_{\sigma 1}$–T_{11}–$L_{\sigma 2}$–T_{12}–D_{13}–T_{16}. All three IGBT modules are involved. Additional stray inductance is

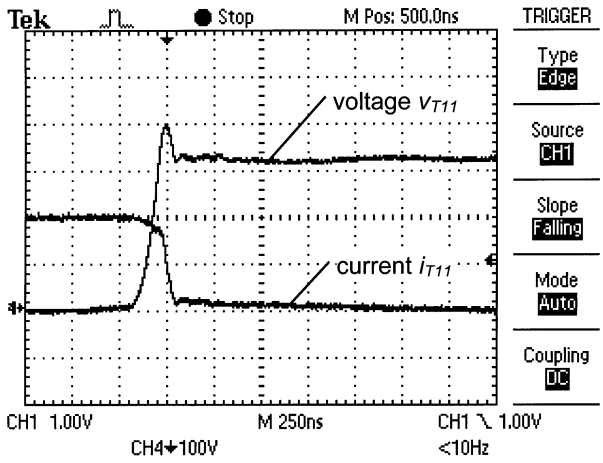

Fig. 16. Measured turn-off transient for T_{11} (type-1 commutation $(+ \rightarrow 0U2), V_{dc}/2 = 325$ V, $i_{ph} = 40$ A, time 250 ns/div, voltage 100 V/div, current 20 A/div).

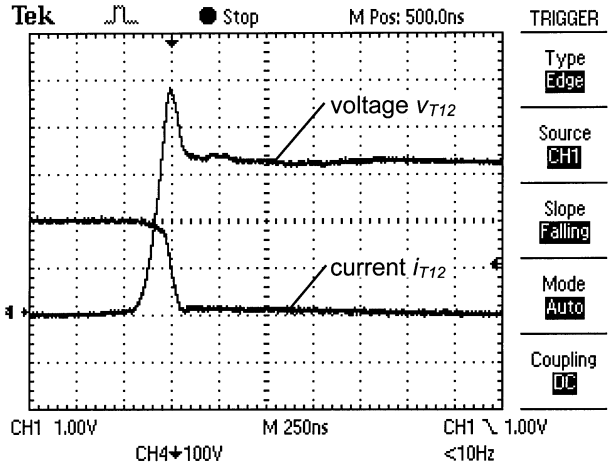

Fig. 17. Measured turn-off transient for T_{12} (type-3 commutation $(+ \rightarrow 0L1)$, conditions as Fig. 16).

introduced by the installation of the Pearson transducers. The commutation loop for the type-1 commutation comprises C_{dc1}–$L_{\sigma 1}$–T_{11}–D_{15} only. From the amplitude of the peak voltages in Figs. 16 and 17, the stray inductances can be estimated to be $L_{\sigma 1} \approx L_{\sigma 2} \approx 180$ nH. The higher peak voltage during the T_{12} turn-off creates slightly higher switching losses compared to the turn-off of T_{11}. On the other hand, the larger commutation inductance slows down the turn-on transient of T_{12} during the reverse commutation, enabling lower turn-on losses for T_{12} compared to T_{11}. The corresponding reverse-recovery losses of the diode again are increased due to the larger inductance. In the examined case, all three effects compensate each other almost completely, such that the total losses remain nearly constant. In a properly designed converter without current sensors, the parasitic inductances and the overvoltages can be kept much smaller for all ANPC commutations and their effect on the total losses is minimized.

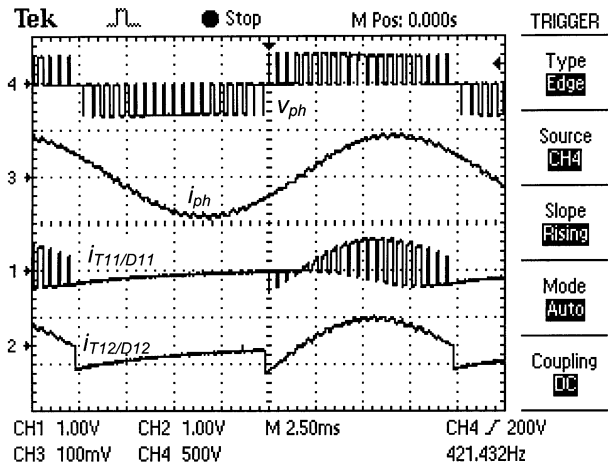

Fig. 18. Measured output voltage and current waveforms for exclusive use of type-1 commutations ($V_{\rm dc}/2 = 325$ V, $I_{\rm rms} = 12$ A, $M = 0.8, pf = 0.85$, $f_s = 2$ kHz, $f_0 = 50$ Hz, time 2.5 ms/div, voltage 500 V/div, currents 20 A/div).

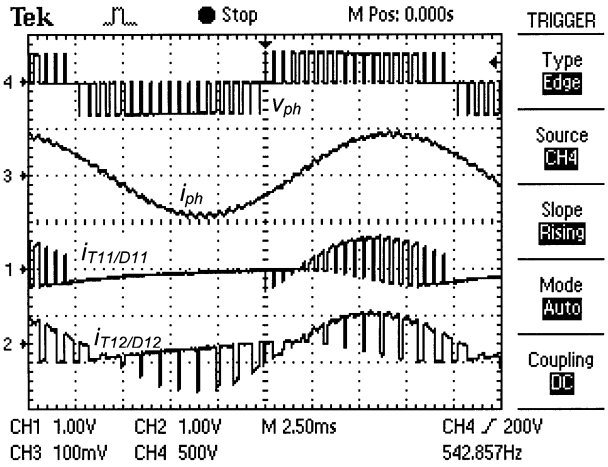

Fig. 19. Measured output voltage and current waveforms for alternating use of type-1 and type-3 commutations (conditions as in Fig. 18).

Experimental results for the output voltage and current waveforms[6] over the fundamental period are depicted in Figs. 18 and 19 for an operating point comparable to the one of Figs. 11 and 12. The modulation index and power factor are somewhat lower ($M = 0.8, pf = 0.85$) than in the simulated most critical case for the high-power converter ($M = 1.15, pf = 1$). For the measurement of Fig. 19 a strict 50% share of type-1 and type-3 commuations was commanded. Compared to Fig. 12(e), the switched pulses of $i_{T12/D12}$ in Fig. 19 are wider due to the lower modulation index and more frequent due to the higher switching frequency. However, the comparison of the experimental results with the simulation discloses a concurrent fundamental behavior and, thus, proves the proper electrical function of the ANPC VSC's commutations and modulation scheme.

[6]The low-frequency distortion of the measured current signals of $i_{T11/D11}$ and $i_{T12/D12}$ is introduced by the transfer function of the high-frequency Pearson current transducers, which do not pass dc components (corner frequency 120 Hz). The phase current $i_{\rm ph}$ is measured with a Tektronix A6303/AM503 current probe.

VII. Summary

This paper has investigated the loss and junction temperature distribution among the semiconductors in the three-level NPC VSC. The analysis shows that the distribution of junction temperatures is unequal, which severely limits the output power of the converter. To overcome this drawback, the NPC VSC is extended to the ANPC VSC. New switch states and commutations are introduced that enable a substantial improvement of the unequal loss distribution and, thus, the mitigation of probably the most severe disadvantage of the three-level NPC topology. A loss-balancing system was proposed, featuring a substantial increase of the converter output power or switching frequency. In the 2.3-kV IGBT converter being examined, a 20% higher output power or 85% higher switching frequency can be achieved compared to a commercially available, state-of-the-art MV converter. Where active NPC switches are already built in (like in many IGBT converters) the proposed control system will notably improve the converter performance at negligible additional cost. Nevertheless, its application is not limited to these cases. In a (3.3 kV, 9 MVA) IGCT converter being investigated, the switching frequency could be increased to 225%. Therefore, the ANPC VSC together with the proposed loss-balancing system is a very attractive solution for both, IGBT and IGCT converters for MVD applications.

References

[1] R. H. Baker, "Bridge converter circuit," U.S. Patent 4 270 163, May 26, 1981.

[2] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518–523, Sept./Oct. 1981.

[3] A. Mertens, M. Bruckmann, and R. Sommer, "Medium voltage inverter using high-voltage IGBTs," in *Proc. EPE'99*, Lausanne, Switzerland, 1999, CD-ROM.

[4] P. K. Steimer, J. K. Steinke, H. E. Grüning, and S. Conner, "A reliable, interface-friendly medium voltage drive based on the robust IGCT and DTC technologies," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Phoenix, AZ, 1999, pp. 1505–1512.

[5] R. Teichmann and S. Bernet, "Three-level topologies for low voltage power converters in drives, traction, and utility applications," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Salt Lake City, UT, 2003, pp. 160–167.

[6] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. IEEE PESC'92*, Toledo, Spain, 1992, pp. 397–403.

[7] J. K. Steinke, "Switching frequency optimal PWM control of a three-level inverter," *IEEE Trans. Power Electron.*, vol. 7, no. 4, pp. 487–496, Jul. 1992.

[8] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[9] L. Helle, S. Munk-Nielsen, and P. Enjeti, "Generalized discontinuous dc-link balancing modulation strategy for three-level inverters," in *Proc. Power Conversion Conf.*, Osaka, Japan, 2002, pp. 359–366.

[10] T. Brückner and D. G. Holmes, "Optimal pulse width modulation for three-level inverters," in *Proc. IEEE PESC'03*, Acapulco, Mexico, 2003, pp. 165–170.

[11] T. Brückner and S. Bernet, "Loss balancing in three-level voltage source inverters applying active NPC switches," in *Proc. IEEE PESC'01*, Vancouver, BC, Canada, 2001, pp. 1135–1140.

[12] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters*. New York: IEEE Press/Wiley-Interscience, 2003.

[13] Y. Shakweh, "Critical assessment of HV power devices for MV PWM VSI converters," in *Proc. EPE'99*, Lausanne, Switzerland, 1999, CD-ROM.

[14] X. Yuan, H. Stemmler, and I. Barbi, "Investigation on the clamping voltage self-balancing of the three-level capacitor clamping inverter," in *Proc. IEEE PESC'99*, Charleston, SC, 1999, pp. 1059–1064.
[15] F. Blaabjerg, J. K. Pedersen, S. Sigurjónsson, and A. Elkjær, "An extended model of power losses in hard-switched IGBT-inverters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, San Diego, CA, 1996, pp. 1454–1463.
[16] V. Blasko, R. Lukaszewski, and R. Sladky, "On line thermal model and thermal management strategy of a three phase voltage source inverter," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Phoenix, AZ, 1999, pp. 1423–1431.
[17] U. Nicolai *et al.*, *Application Manual Power Modules*. Ilmenau, Germany: SEMIKRON, Verlag ISLE, 2000.
[18] "Technical information IGBT-modules, datasheet FZ 1200 R 33 KF2," Eupec GmbH, Warstein, Germany, 1999.
[19] D. A. Murdock, J. E. Ramos, J. J. Connors, and R. D. Lorenz, "Active thermal control of power electronics modules," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Salt Lake City, UT, 2003, pp. 1511–1515.
[20] R. Krümmer, T. Reimann, G. Berger, J. Petzoldt, and L. Lorenz, "On-line calculation of the chip temperature of power modules in voltage source converters using the microcontroller," in *Proc. EPE'99*, Lausanne, Switzerland, 1999, CD-ROM.

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