

NANYANG TECHNOLOGICAL UNIVERSITY**SEMESTER 2 EXAMINATION 2020-2021****EE3019 – INTEGRATED ELECTRONICS**

April / May 2021

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 4 pages.
 2. Answer all 4 questions.
 3. All questions carry equal marks.
 4. This is a closed book examination.
 5. Unless specifically stated, all symbols have their usual meanings.
 6. A List of Formulae is provided in Appendix A on page 4.
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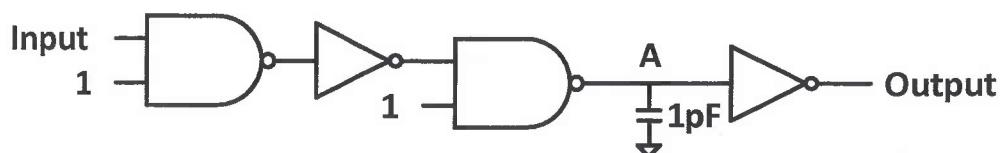
1. The parameters of the pMOS and nMOS transistors are given below:

$$\text{pMOS } V_{tp} = -0.6 \text{ V} \quad \mu_p C_{ox} = 100 \text{ } \mu\text{A/V}^2 \quad (W/L)_p = 5$$

$$\text{nMOS } V_{tn} = 0.6 \text{ V} \quad \mu_n C_{ox} = 250 \text{ } \mu\text{A/V}^2 \quad (W/L)_n = 2$$

$$V_{DD} = 1.8 \text{ V}$$

Figure 1 is designed using the above device parameters.

**Figure 1**

- (a) Determine V_{IH} , V_{IL} , and V_{th} of the 2-input NAND gate and the inverter using the equivalent device sizes of the best case. Assume V_{out} for V_{IL} is 90% of V_{DD} and V_{out} for V_{IH} is 10% of V_{DD} .

(10 Marks)

Note: Question No. 1 continues on page 2.

- (b) Calculate the noise margin of the 2-input NAND gate and the inverter. (5 Marks)
- (c) Determine the propagation delays (τ_{PHL} and τ_{PLH}) of the 2-input NAND gate driving node 'A' using the best case and briefly explain how to make the propagation delays identical. (10 Marks)

2. (a) Figure 2 shows a schematic diagram of the 8-transistor clocked SR latch. The device parameters of the pMOS and nMOS transistors for M₁, M₂, M₃, and M₄ are given below:

$$\text{pMOS } V_{tp} = -0.6 \text{ V } \mu_p C_{ox} = 40 \mu\text{A/V}^2 \quad (W/L)_p = 5$$

$$\text{nMOS } V_{tn} = 0.6 \text{ V } \mu_n C_{ox} = 100 \mu\text{A/V}^2 \quad (W/L)_n = 2$$

$$V_{DD} = 1.8 \text{ V}$$

Determine the minimum size of M₅, M₆, M₇, and M₈ for reliable set and reset operations. Assume that Q and QB need to be pulled down to $\frac{V_{DD}}{3}$.

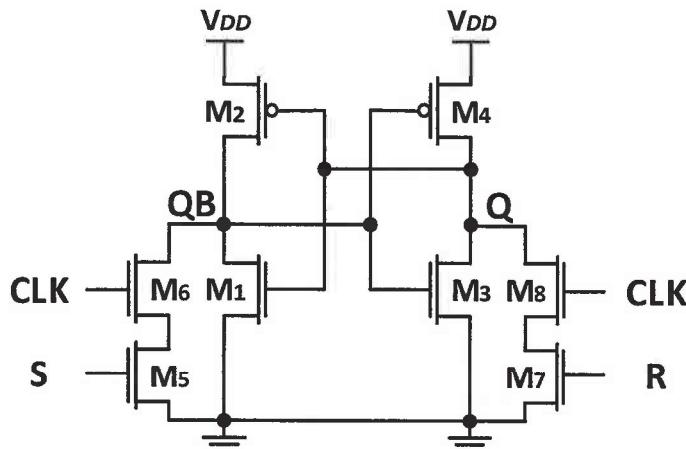


Figure 2

(10 Marks)

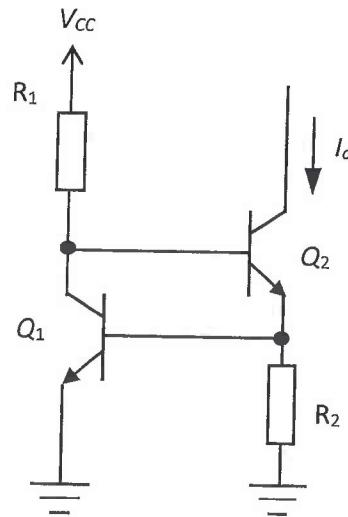
- (b) Draw a schematic diagram of a 6-transistor SRAM cell and explain how to improve the reliability of read and write operations. (10 Marks)
- (c) Explain the characteristics of negative feedback in amplifiers. (5 Marks)

3. (a) Draw schematic diagrams of basic and Wilson current mirrors using bipolar junction transistors and discuss their respective advantages.

(10 Marks)

- (b) Consider the V_{BE} -based bias circuit illustrated in Figure 3 and derive its sensitivity of the output current to the power-supply voltage under the assumption of negligible base currents.

(10 Marks)

**Figure 3**

- (c) Propose an idea to reduce the sensitivity of the output current to the power-supply voltage of the V_{BE} -based bias circuit.

(5 Marks)

4. The DC open loop gain of an op amp is 100 dB, and the dominant pole is 600 kHz. The op amp is used as an inverting amplifier.

- (a) Draw a schematic diagram of the amplifier and find the external resistance values with an input resistance of $10 \text{ k}\Omega$ and gain of -9 .

(10 marks)

- (b) Determine if the amplifier is stable.

(15 marks)

APPENDIX A

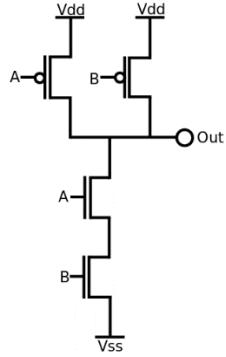
$$V_{IH} = \frac{V_{DD} + V_{tp} + k_R(2V_{out} + V_{tn})}{1 + k_R}$$

$$V_{IL} = \frac{2V_{out} + V_{tp} - V_{DD} + k_R V_{tn}}{1 + k_R}$$

$$V_{th} = \frac{V_{th} + \sqrt{\frac{1}{k_R}(V_{DD} + V_{tp})}}{1 + \sqrt{\frac{1}{k_R}}}$$

$$v_t = V_{to} + \gamma(\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f})$$

END OF PAPER

Question 1(a)**2-input NAND**

For both 2-input NAND gates, one of their inputs are tied to 1 → 1 PMOS is always off, 1 NMOS is always on

$$\text{Equivalent PMOS size (only 1 PMOS is on): } \left(\frac{W}{L}\right)_p$$

$$\text{Equivalent NMOS size: } \frac{1}{2} \left(\frac{W}{L}\right)_n$$

At $V_{in} = V_{IH}$, NMOS is in linear region, PMOS is in saturation region

It is given: $V_{out} = 90\%V_{DD} = 1.62 V$

Equating drain current

$$\mu_n C_{ox} \left[\frac{1}{2} \left(\frac{W}{L} \right)_n \right] \left[(V_{GSn} - V_{tn}) V_{DSn} - \frac{1}{2} V_{DSn}^2 \right] = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_p (V_{SGp} - |V_{tp}|)^2$$

$$250 \left[(V_{IH} - 0.6) 1.62 - \frac{1}{2} 1.62^2 \right] = 250 (1.8 - V_{IH} - 0.6)^2$$

$$V_{IH} = 1.45 V$$

At $V_{in} = V_{IL}$, NMOS is in saturation region, PMOS is in linear region

It is given: $V_{out} = 10\% V_{DD} = 0.18 V$

Equating drain current

$$\frac{1}{2} \mu_n C_{ox} \left[\frac{1}{2} \left(\frac{W}{L} \right)_n \right] (V_{GSn} - V_{tn})^2 = \mu_p C_{ox} \left(\frac{W}{L} \right)_p \left[(V_{SGp} - |V_{tp}|) V_{SDp} - \frac{1}{2} V_{SDp}^2 \right]$$

$$125(V_{IL} - 0.6)^2 = 500 \left[(1.8 - V_{IL} - 0.6) 1.62 - \frac{1}{2} 1.62^2 \right]$$

$$V_{IL} = 0.383 V$$

At $V_{in} = V_{th}$, $V_{out} = V_{in} = V_{th}$, both NMOS and PMOS are in saturation

$$\frac{1}{2}\mu_n C_{ox} \left[\frac{1}{2} \left(\frac{W}{L} \right)_n \right] (V_{GSn} - V_{tn})^2 = \frac{1}{2}\mu_p C_{ox} \left(\frac{W}{L} \right)_p (V_{SGp} - |V_{tp}|)^2$$

$$125(V_{th} - 0.6)^2 = 250(1.8 - V_{th} - 0.6)^2$$

$$V_{th} = 0.951 V$$

Inverter

The calculations are the same as above, except PMOS and NMOS strength

At $V_{in} = V_{IH}$

$$\mu_n C_{ox} \left(\frac{W}{L} \right)_n \left[(V_{GSn} - V_{tn})V_{DSn} - \frac{1}{2}V_{DSn}^2 \right] = \frac{1}{2}\mu_p C_{ox} \left(\frac{W}{L} \right)_p (V_{SGp} - |V_{tp}|)^2$$

$$500 \left[(V_{IH} - 0.6)1.62 - \frac{1}{2}1.62^2 \right] = 250(1.2 - V_{IH})^2$$

$$V_{IH} = 1.43 V$$

At $V_{in} = V_{IL}$

$$\frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L} \right)_n (V_{GSn} - V_{tn})^2 = \mu_p C_{ox} \left(\frac{W}{L} \right)_p \left[(V_{SGp} - |V_{tp}|)V_{SDp} - \frac{1}{2}V_{SDp}^2 \right]$$

$$250(V_{IL} - 0.6)^2 = 500 \left[(1.8 - V_{IL} - 0.6)1.62 - \frac{1}{2}1.62^2 \right]$$

$$V_{IL} = 0.374 V$$

At $V_{in} = V_{th}$

$$\frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L} \right)_n (V_{GSn} - V_{tn})^2 = \frac{1}{2}\mu_p C_{ox} \left(\frac{W}{L} \right)_p (V_{SGp} - |V_{tp}|)^2$$

$$250(V_{th} - 0.6)^2 = 250(1.8 - V_{th} - 0.6)^2$$

$$V_{th} = 0.9 V$$

Question 1(b)

2-input NAND

$$NM_H = V_{OH} - V_{IH} = 1.8 - 1.45 = 0.35 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.383 - 0 = 0.383 \text{ V}$$

$$\Rightarrow NM = 0.383 \text{ V}$$

Inverter

$$NM_H = V_{OH} - V_{IH} = 1.8 - 1.43 = 0.37 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.374 - 0 = 0.374 \text{ V}$$

$$\Rightarrow NM = 0.374 \text{ V}$$

Question 1(c)

Calculate τ_{PHL}

At the start, $V_{out} = V_{DD} = 1.8V$, $V_{in} = V_{DD} = 1.8V$

PMOS is off, NMOS is on.

NMOS is in saturation because $V_{DSn} > V_{GSn} - V_{tn}$

Drain current

$$i_D = \frac{1}{2} \mu_n C_{ox} \left[\frac{1}{2} \left(\frac{W}{L} \right)_n \right] (V_{GSn} - V_{tn})^2 = 125(1.8 - 0.6)^2 = 180 \mu A$$

At the end, $V_{out} = 50\%V_{DD} = 0.9V$, $V_{in} = V_{DD} = 1.8V$

PMOS is off, NMOS is on.

NMOS is in linear region because $V_{DSn} = 0.9 < 1.8 - 0.6 = V_{GSn} - V_{tn}$

Drain current

$$i_D = \mu_n C_{ox} \left[\frac{1}{2} \left(\frac{W}{L} \right)_n \right] \left[(V_{GSn} - V_{tn})V_{DSn} - \frac{1}{2} V_{DSn}^2 \right] = 250 \left[(1.8 - 0.6)0.9 - \frac{1}{2} 0.9^2 \right] = 168.75 \mu A$$

Propagation delay from High to Low

$$\tau_{PHL} = \frac{C \Delta V}{i_{avg}} = \frac{1 \text{ pF} \cdot 0.9 \text{ V}}{(180 + 168.75)/2 \mu A} = 5.16 \text{ ns}$$

Calculate τ_{PLH}

At the start, $V_{out} = 0V, V_{in} = 0V$

PMOS is on, NMOS is off.

PMOS is in saturation because $V_{SDp} > V_{SGp} - |V_{tp}|$

Drain current

$$i_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_p (V_{SGp} - |V_{tp}|)^2 = 250(1.8 - 0 - 0.6)^2 = 360 \mu A$$

At the end, $V_{out} = 50\%V_{DD} = 0.9V, V_{in} = 0V$

PMOS is on, NMOS is off

PMOS is in linear region because $V_{SDp} = 0.9 < (1.8 - 0) - 0.6 = V_{SGp} - |V_{tp}|$

Drain current

$$\begin{aligned} i_D &= \mu_p C_{ox} \left(\frac{W}{L} \right)_p \left[(V_{SGp} - |V_{tp}|) V_{SDp} - \frac{1}{2} V_{SDp}^2 \right] \\ &= 500 \left[(1.8 - 0 - 0.6)(1.8 - 0.9) - \frac{1}{2}(1.8 - 0.9)^2 \right] = 337.5 \mu A \end{aligned}$$

Propagation delay from High to Low

$$\tau_{PHL} = \frac{C \Delta V}{i_{avg}} = \frac{1 pF \cdot 0.9V}{(360 + 337.5)/2 \mu A} = 2.58 ns$$

To make propagation delays identical, we need to match the relative strength between effective PMOS and effective NMOS. In this case, since $V_{tn} = |V_{tp}|$, we can match their strengths by matching $\mu C_{ox} \left(\frac{W}{L} \right)$, thus doubling the width of NMOS.

Question 2(a)

For set operation:

- $Q = 0$, thus M2 is on, M1 is off
- $QB = 1$, thus M3 is on, M4 is off
- $S = 1, R = 0$, thus M5 is on, M7 is off

Assume M5 and M6 have equal sizes $\rightarrow \left(\frac{W}{L}\right)_{M56} = \frac{1}{2} \left(\frac{W}{L}\right)_{M5} = \frac{1}{2} \left(\frac{W}{L}\right)_{M6}$

At $QB = \frac{V_{DD}}{3}$

Look at M56: $V_{DS(56)} = \frac{V_{DD}}{3} = 0.6 < 1.8 - 0.6 = V_{GS(56)} - V_{tn} \rightarrow$ thus M56 is in linear region

Look at M2: $V_{SD(2)} = V_{DD} - \frac{V_{DD}}{3} = 1.2 = (1.8 - 0) - 0.6 = V_{SG(2)} - |V_{tp}|$ (assume Q is still zero) \rightarrow M2 is in saturation

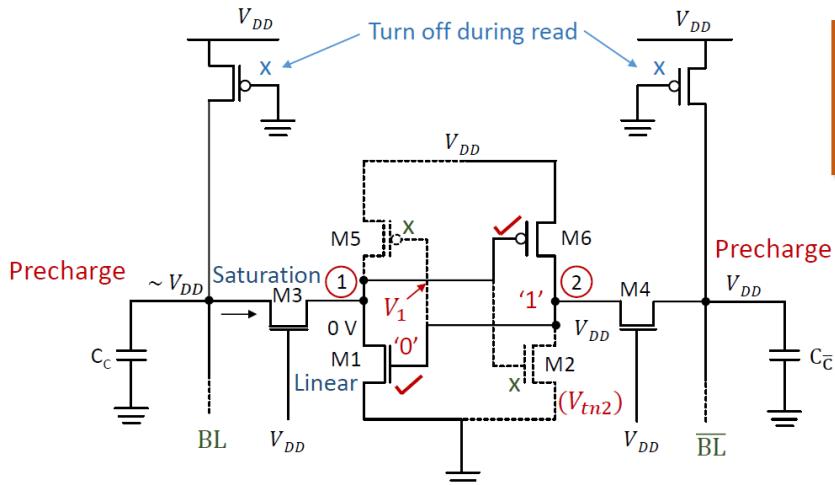
Equating drain current

$$\begin{aligned} \mu_n C_{ox} \left(\frac{W}{L}\right)_{56} \left[(V_{GS(56)} - V_{tn}) V_{DS(56)} - \frac{1}{2} V_{DS(56)}^2 \right] &= \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_{SG(2)} - |V_{tp}|)^2 \\ \left(\frac{W}{L}\right)_{56} &= \frac{\frac{1}{2} \mu_p C_{ox} (V_{SG(2)} - |V_{tp}|)^2}{\mu_n C_{ox} \left[(V_{GS(56)} - V_{tn}) V_{DS(56)} - \frac{1}{2} V_{DS(56)}^2 \right]} \left(\frac{W}{L}\right)_2 \\ \left(\frac{W}{L}\right)_{56} &= \frac{20(1.8 - 0 - 0.6)^2}{100 \left[(1.8 - 0.6)0.6 - \frac{1}{2} 0.6^2 \right]} \cdot 5 = 2.67 \\ \left(\frac{W}{L}\right)_5 &= \left(\frac{W}{L}\right)_6 = 2 \cdot 2.67 = 5.33 \end{aligned}$$

M5 and M6 must be strong enough to pull QB down (competing with M2). Thus the minimum size for M5 and M6 is $\left(\frac{W}{L}\right) = 6$

Since the circuit is symmetric, by solving for reset operation, we will also get minimum size for M7 and M8 to be $\left(\frac{W}{L}\right) = 6$

Question 2(b)



Read operation

Assume the cell is storing "0" \rightarrow node 1 = 0V, node 2 = V_{DD}

M2 is off and M6 is on (due to node 1 = 0V)

M5 is off and M1 is on (due to node 2 = V_{DD})

Bit line BL is pre-charged to V_{DD}

M3 tries to pull up node 1 (because $BL = V_{DD}$) while M1 tries to pull down node 1 to ground. If node 1 voltage is too high, it will turn on M2 and turn off M6 (flip the inverter M2-M6), and change cell state to "1".

Thus to ensure reliable read operation, M1 must be stronger than M3 to keep node 1 low during read operation.

Write operation

Assume the cell is storing "1", and we want to write "0" \rightarrow node 1 = V_{DD} , node 2 = 0V

M2 is on, M6 is off (due to node 1 = V_{DD})

M1 is off, M5 is on (due to node 2 = 0V)

Bit line BL is pre-charged to 0V (since we want to write "0")

M5 tries to pull up node 1 to V_{DD} while M3 tries to pull down node 1 to ground (because $BL = 0V$). To ensure successful write operation, node 1 must be pulled low to flip the inverter M2-M6 (turn off M2, turn on M6). Thus M3 must be stronger than M5.

In summary, $M1 > M3 > M5$. In similar fashion, $M2 > M5 > M6$

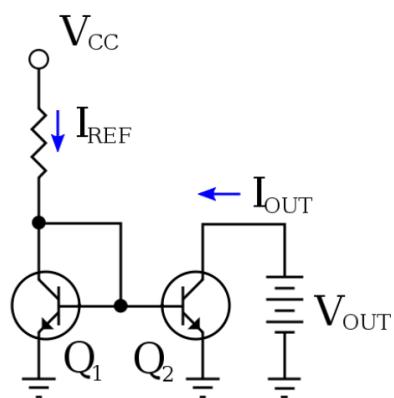
However, it should be noted that to ensure stability of the inverter M1-M5 and M2-M6, strength mismatch between PMOS and NMOS should not be too much.

Question 2(c)

- Gain de-sensitivity
- Bandwidth extension
- Noise reduction
- Reduce non-linear distortion
- Input and output impedance improvement

Question 3(a)

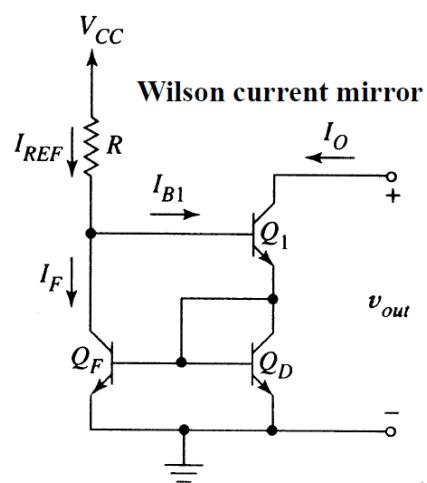
Basic current mirror



Advantages

- Simple, easy to construct

Wilson current mirror



Advantages

- Eliminate base current mismatch by using Q_1 to provide base currents for Q_F and Q_D . Therefore output current follows reference current better

Question 3(b)

Output current depends on R2

$$I_o = I_{R2} = \frac{V_{R2}}{R_2} = \frac{V_{BE1}}{R_2}$$

In active region of BJT

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \Rightarrow V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

Thus

$$I_o = \frac{V_T}{R_2} \ln\left(\frac{I_{C1}}{I_S}\right)$$

I_{C1} is the reference current, set by the input voltage

$$I_{C1} = \frac{V_{CC} - V_{BE2} - V_{BE1}}{R_1}$$

Taking partial derivative of output current wrt input voltage

$$\begin{aligned} \frac{\partial I_o}{\partial V_{CC}} &= \frac{V_T}{R_2} \cdot \frac{I_S}{I_{C1}} \cdot \frac{1}{I_S} \cdot \frac{\partial I_{C1}}{\partial V_{CC}} \\ &= \frac{V_T}{R_2} \cdot \frac{1}{I_{C1} R_1} \left(1 - \frac{\partial V_{BE2}}{\partial V_{CC}} - \frac{\partial V_{BE1}}{\partial V_{CC}} \right) \end{aligned}$$

To ensure probable operation, V_{CC} must be at least larger than 2 times V_{BE} . There will also be voltage drop across R1, thus we can expect V_{CC} is much larger than V_{BE1} and V_{BE2} . Thus we can approximate $\frac{\partial V_{BE2}}{\partial V_{CC}} = 0$, $\frac{\partial V_{BE1}}{\partial V_{CC}} = 0$

Thus

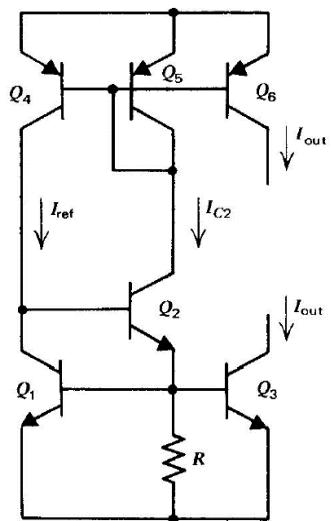
$$\frac{\partial I_o}{\partial V_{CC}} = \frac{V_T}{R_2} \cdot \frac{1}{I_{C1} R_1} = \frac{V_T}{R_2} \cdot \frac{1}{V_{CC} - V_{BE1} - V_{BE2}}$$

Sensitivity

$$\frac{\partial I_o}{\partial V_{CC}} \cdot \frac{V_{CC}}{I_o} = \frac{V_T}{R_2} \cdot \frac{1}{V_{CC} - V_{BE1} - V_{BE2}} \cdot \frac{V_{CC}}{I_o}$$

Question 3(c)

Add a bootstrap circuit



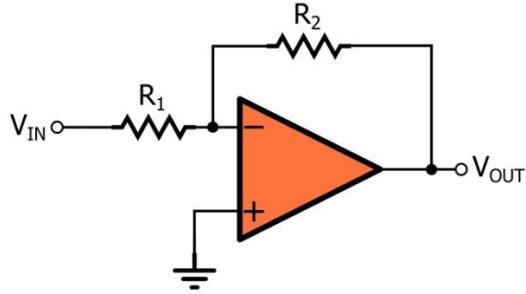
Reference current is mirrored from I_{C2}

$$I_{C2} = \frac{V_T}{R} \ln\left(\frac{I_{C1}}{I_S}\right) = \frac{V_T}{R} \ln\left(\frac{I_{C2}}{I_S}\right)$$

This equation only depends on I_{C2} , thus it does not depend on V_{CC} . Using an external startup circuit, we can ensure that I_{C2} won't be zero (a trivial solution to the above equation).

Question 4(a)

$$A = 100 \text{dB} = 10^5 \text{ V/V}$$



$R_1 = 10 \text{ k}\Omega$ (input resistance)

Inverting gain

$$A_f = -\frac{R_2}{R_1} = -9 \Rightarrow R_2 = 9R_1 = 90 \text{ k}\Omega$$

Question 4(b)

$$\begin{aligned} V_{out} &= -AV_{id} = -A \left[V_{out} - \frac{V_{out} - V_{in}}{R_1 + R_2} R_2 \right] = -A \left[\frac{R_1}{R_1 + R_2} V_{out} + \frac{R_2}{R_1 + R_2} V_{in} \right] \\ &\quad \left(1 + A \frac{R_1}{R_1 + R_2} \right) V_{out} = -A \frac{R_2}{R_1 + R_2} V_{in} \\ A_f &= \frac{V_{out}}{V_{in}} = \frac{-A \frac{R_2}{R_1 + R_2}}{1 + A \frac{R_1}{R_1 + R_2}} = -\frac{0.9A}{1 + 0.1A} \end{aligned}$$

Frequency response of open-loop gain

$$A(jf) = \frac{10^5}{\left(1 + j \frac{f}{600} \right)}$$

We only need to look at loop gain

$$A\beta = 0.1A = \frac{10^4}{1 + j \frac{f}{600}}$$

Finding phase margin by setting $|A\beta| = 1$

$$\begin{aligned} \frac{10^4}{\sqrt{1 + \frac{f^2}{600^2}}} &= 1 \Rightarrow \frac{f^2}{600^2} = 10^8 - 1 \Rightarrow f \approx 600 \cdot 10^4 \text{ kHz} \\ \angle A\beta &= -\tan^{-1} 10^4 = -89.9^\circ \end{aligned}$$

$$\text{Phase margin} = -89.9^\circ + 180^\circ = 90.1^\circ > 0$$

Thus the system is stable