NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE

School of Electrical & Electronic Engineering

E2002 Analog Electronics

Academic Year 2021-2022

L2002A

Operational Amplifier – Parameters and Applications

Project Laboratory (S2-B4a-01/02)

Dress Code in the Laboratory

- **Work shirt that covers the upper torso and arms.**
- **Lower body clothing that covers the entire leg.**
- **Closed-toe shoes that cover the top of the foot.**

Laboratory Manual

OPERATIONAL AMPLIFIER - PARAMETERS AND APPLICATIONS

1. OBJECTIVES

This experiment is divided into two sections. In the first section, we shall examine several basic limitations of an integrated circuit op amp for a linear application. In the latter section, we shall examine the effects of the non-idealities of the op amp for non- linear applications – comparator and square-wave oscillator.

2. EQUIPMENT

a.	Digital Oscilloscope	Tektronix TBS2104
b.	Digital Multimeter	Fluke 45
c.	Function Generator	Tektronix AFG3022C
d.	Power Supply	Siglent SPP-3303C
e.	Breadbox	Global Specialties
f.	Op Amp	1 units: 741
g.	Potentiometers	10 kΩ single-turn
h.	Resistors	2 units: 100 kΩ 1 unit: 10 kΩ, 1 unit: 2 kΩ, 100Ω, 220Ω, 1 kΩ
i.	Capacitors	3 units: 0.1 μF ceramic capacitor 1 unit: 100 pF ceramic capacitor

3. EXPERIMENT

The 741 op amp is a fully bipolar op amp. The power supply connections for this op amp are: +15V at pin 7, and –15V at pin 4. Although these power connections are omitted for clarity in the circuit diagrams, ensure that they are connected before making any measurements.
For each supply, by pass with a 0.1 μF ceramic capacitor.

The input signal source may have DC offset in its outputs and may require adjustment. It is assumed that all signal sources are **offset-free** in the circuit diagrams; if necessary, adjust the input sources. V_{pp} denotes peak-to-peak voltage. Record all measurements and answer all questions in the log sheets.

As this experiment requires extensive use of the digital oscilloscope, students are advised to familiarise themselves with this instrument before embarking on the experiment. In particular, incorrect choice of the AC/DC coupling input would result in erroneous measurements.

The 741 op amp data sheets are attached and where possible, the parameters measured in this experiment should be directly compared to the specifications.

3.1 Basic Op Amp Parameters

3.1.1 DC Offset Measurement

Refer to the **data sheets (Page 10)** for the pin configuration of op amp

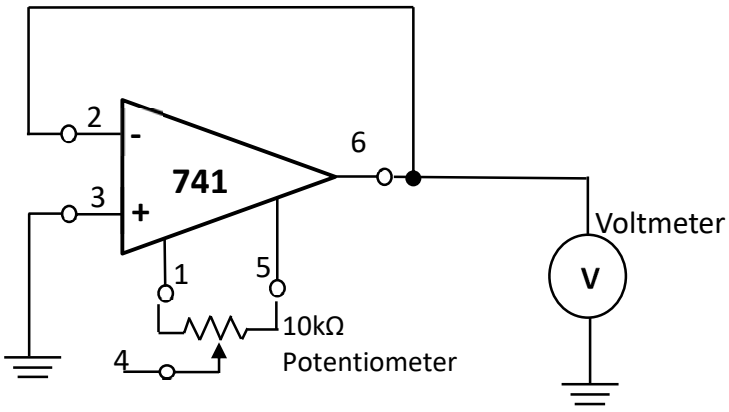


Figure 1: DC Offset Measurement

Note: A potentiometer is a variable tapped resistor that can be used as a variable voltage divider.

With the 10kΩ compensating potentiometer for offset adjustment, record the range of dc offset when the potentiometer is varied from one extreme end to the other. Adjust the potentiometer to obtain zero offset.

	DC offset (+*mV*)	DC offset (-*mV*)
Multi-meter (*mV*)		

3.1.2 Large-Signal Operation

3.1.2.1 Slew Rate Limitation and Saturation

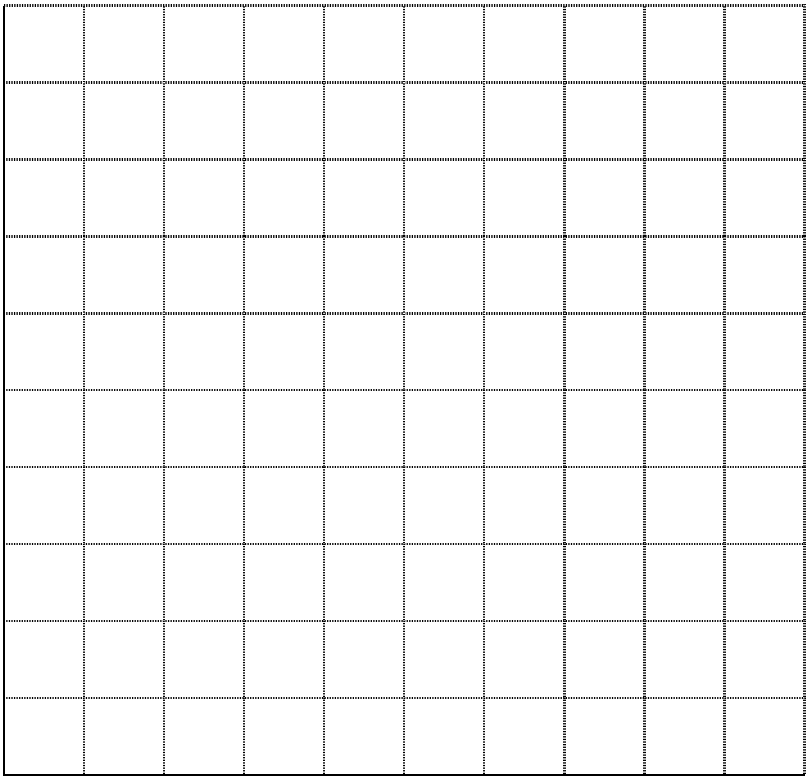
a) Design a unity-gain inverting amplifier with an input impedance of 100kΩ; assume that the op amp has an infinite input impedance. With the DC offset of the op amp adjusted to zero, and also connect a load comprising a 100 pF capacitor in parallel with a 2kΩ resistor to the op- amp output.

b) Connect a $10V_{pp}$, 10kHz square wave signal to the input of the amplifier. **Sketch & determine** the slew-rate of the op amp. Also, comment on the variation, if any, on the output saturation behaviour of the op amp.

Draw your Design Circuit here

Unity-Gain Inverting Amplifier

c) **Measure both positive and negative slew rates.** Explain if the slew rate is affected by the dc offset, and explain the parameters that determine the slew-rate of an op amp.



Slew Rate

Comment: _____

_____

_____

d) Sketch the circuit diagram and show how you could reduce the dc offset in your unity-gain inverting amplifier design (without the offset compensating potentiometer).

Hint: The 741 is a BJT op amp

Draw your Design Circuit here

3.1.2.2 Large-Signal Bandwidth

a) With the offset of the op amp adjusted to zero, connect an input voltage, V_{in}, initially set to **50mV$_{pp}$**, 1 kHz sinewave to the input of the amplifier (the load remains unchanged from the previous section). Determine the input frequency f_C where the output of the op amp becomes –3 dB below the output obtained at 1 kHz.

	Calculate	Measure
V_{in}	Vo at f_C	f_C
50mV$_{pp}$		
3V$_{pp}$		

b) Repeat the above procedure with V_{in} initially set to **3V$_{pp}$**, 1kHz sinewave and **sketch** the input and output waveforms (superimposed) at f_C. **Explain** why the input frequency f_c is different with that of section (a).

V_{in} = 3V$_{pp}$, Input and Output Waveforms (superimposed) at f_C.

Comment:

3.2 Use of the Op Amp as a Comparator

A comparator compares two input voltages and produces a logic output signal whose value (high or low) depends on which of the two inputs is largest. The circuit symbol, shown in Figure 2, is identical to the op amp non-inverting input. If the voltage v_1 applied to the non-inverting input is larger than the voltage v_2 applied to the inverting input, the output v_o goes to its maximum positive level. For opposite state, the output goes to its maximum negative level if v_1 is less than v_2.

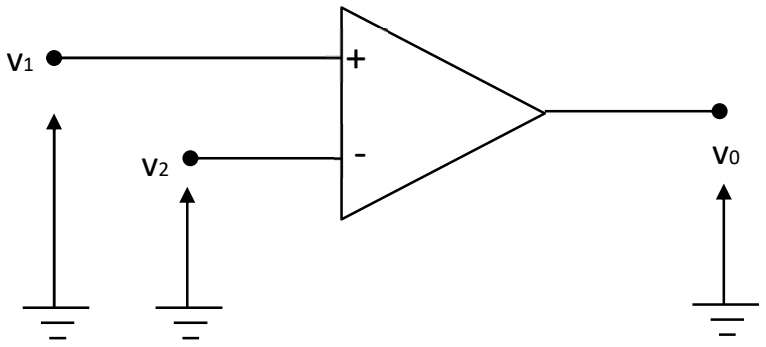


Figure 2: Circuit Symbol for the Comparator

3.2.1 Effect of DC Offset

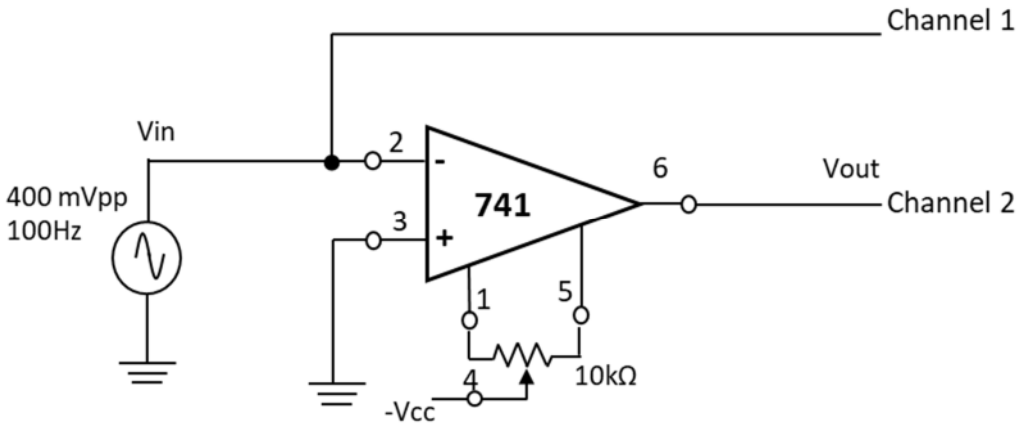
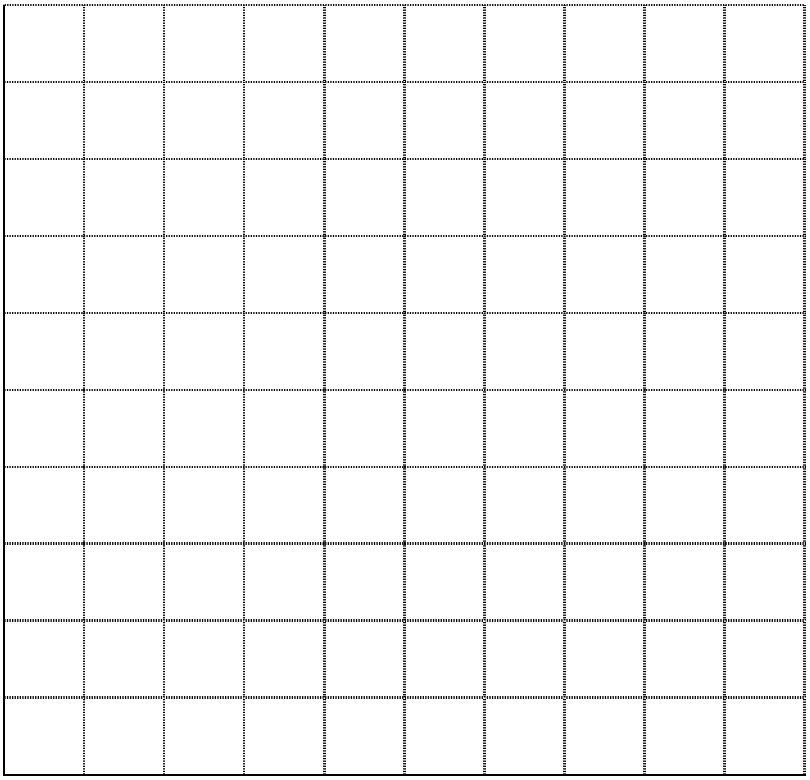


Figure 3: Effect of DC Offset on a Comparator

a) With the DC offset of the op amp set to zero, construct the circuit depicted in Figure 3. With the oscilloscope set to the X-Y mode, sketch the comparator transfer characteristics (V_{out}/V_{in}).
Adjust the DC offset of the op amp to its maximum and minimum value. Sketch and superimpose the transfer function characteristic to the one obtained earlier. Explain how the dc offset changes the transfer characteristics of the comparator.

Comment:

b) Change the input frequency to 10 kHz and comment on the observed waveforms.



X-Y Mode, Comparator Transfer Characteristics (V_{out} / V_{in}).

3.3 Measurement of Open-Loop Gain of Op Amp (Optional)

a) With the offset of the op amp adjusted to zero, apply a 20Hz sinusoidal source voltage V_{in} of $2V_p$ to the input of the amplifier shown in Figure 4. Measure V_O and V*e*.

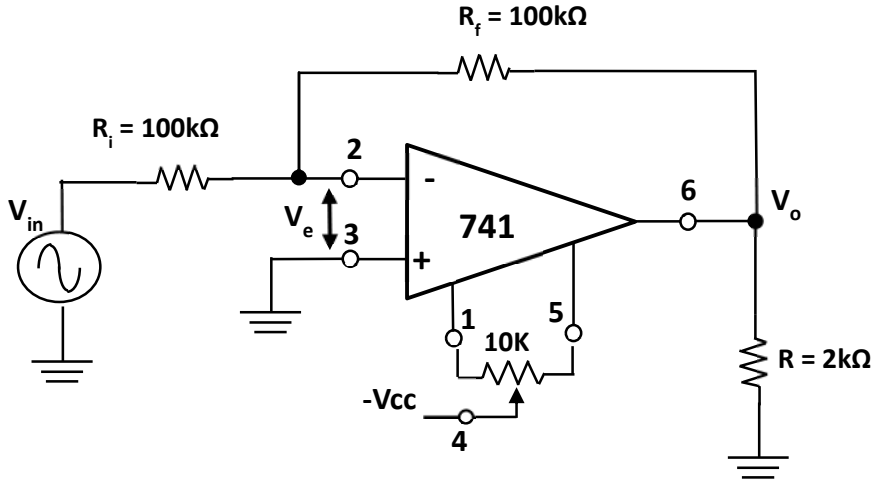


Figure 4: Op Amp Circuit with Feedback

It is given that Closed-Loop Loop Gain $A_{CL} = \frac{Vo}{Vin} = \frac{-R_f}{R_i} = -1$

Measure V_O = _____ and

Ve = _____

b) What are the nature of the signals V_O and Ve? Can you evaluate the Open-Loop Gain A_{OL} = Vo/Ve. Explain your answer.

Comment:

c) What are the nature of the signals V_O and Ve? Can you evaluate the Open-Loop Gain A_{OL} = Vo/Ve? Explain your answer.

d) Construct the circuit depicted in *Figure 5*. Before connecting the function generator to the input, grounded the input Va and conduct zero reference adjustment in oscilloscope. Adjust the offset potentiometer so that the measured dc value @ Ve is zero. To start testing, apply a 20Hz, $2V_p$ sinusoidal source voltage V_{in} to the input Va and measure the **ac** voltage @ V_X and Vo.

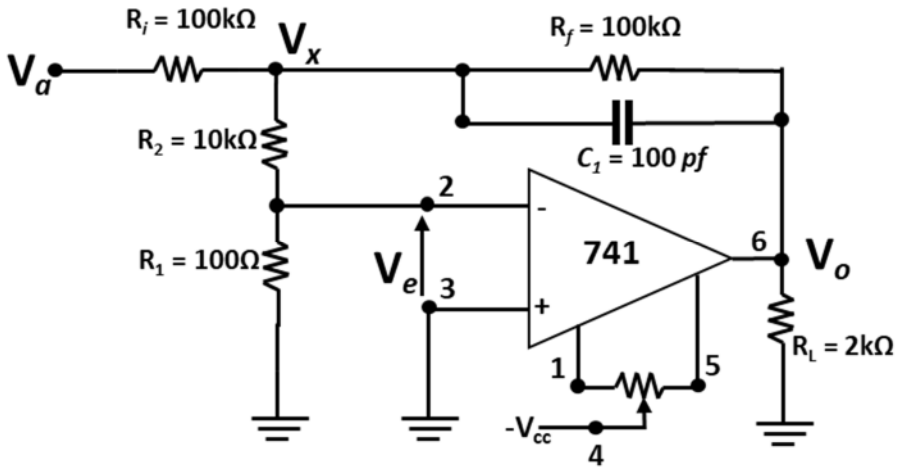


Figure 5: Open-Loop Gain Measurement

From the previously measured slew rate, calculate the maximum test frequency that can be obtained in this measurement setup with Vp =2V. Calculate the open-loop gain using the expression below:

Open-Loop Gain A_{OL} = 101 V*o* / V*x*

Explain how the expression can be derived. What is the unity-gain bandwidth of op amp?

Measure ac voltage @ V*x* = _____ and

V_O = _____

Explain how the expression can be derived. What is the unity-gain bandwidth of op amp?

_____

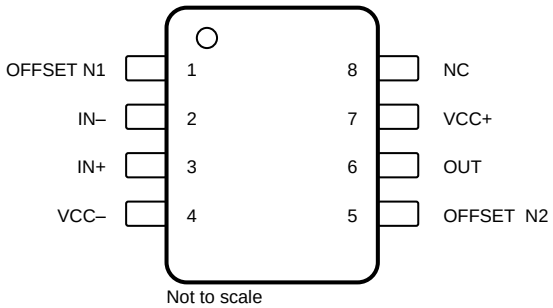
_____

_____

_____

5 Pin Configurations and Functions

uA741C D, P, or PS Package
8-Pin SOIC, PDIP, SO
Top View



Not to scale

NC- no internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN–	2	I	Inverting input
NC	8	—	No internal connection
OFFSET N1	1	I	External input offset voltage adjustment
OFFSET N2	5	I	External input offset voltage adjustment
OUT	6	O	Output
VCC+	7	—	Positive supply
VCC–	4	—	Negative supply

6 Specifications

6.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_{CC}(2)	µA741C		–18	18	V
Differential input voltage, V_{ID}(3)	µA741C		–15	15	V
Input voltage, V_I (any input) (2)(4)	µA741C		–15	15	V
Voltage between offset null (either OFFSET N1 or OFFSET N2) and $V_{CC–}$	µA741C		–15	15	V
Duration of output short circuit(5)			Unlimited		
Continuous total power dissipation			See *Thermal Information*		
Case temperature for 60 seconds		µA741C	N/A	N/A	°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds		µA741C	N/A	N/A	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, P, or PS package	µA741C		260	°C
Operating junction temperature, T_J				150	°C
Storage temperature range, T_{stg}		µA741C	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or either power supply.

6.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$			–5	–15	
T_A	Operating free-air temperature	µA741C	0	70	°C

6.3 Thermal Information

THERMAL METRIC(1)		µA741			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.2	87.4	119.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.6	89.3	66	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	64.4	70	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.9	49.8	27.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.7	64.1	69	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.4 Electrical Characteristics: µA741C

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6	mV
			Full range			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		±15		mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200	nA
			Full range			300	
I_{IB}	Input bias current	V_O = 0	25°C		80	500	nA
			Full range			800	
V_{ICR}	Common-mode input voltage range	25°C		±12	±13		V
		Full range		±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			
		R_L = 2 kΩ	25°C	±10			
		R_L ≥ 2 kΩ	Full range	±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	25°C	20	200		V/mV
		V_O = ±10 V	Full range	15			
r_i	Input resistance	25°C		0.3	2		MΩ
r_o	Output resistance	V_O = 0; see(2)	25°C		75		Ω
C_i	Input capacitance	25°C			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	25°C	70	90		dB
			Full range	70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150	µV/V
			Full range			150	
I_{OS}	Short-circuit output current	25°C			±25	±40	mA
I_{CC}	Supply current	V_O = 0; no load	25°C		1.7	2.8	mA
			Full range			3.3	
P_D	Total power dissipation	V_O = 0; no load	25°C		50	85	mW
			Full range			100	

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C.
(2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

6.5 Electrical Characteristics: µA741Y

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0		1	5	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0		±15		mV
I_{IO}	Input offset current	V_O = 0		20	200	nA
I_{IB}	Input bias current	V_O = 0		80	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	±12	±14		V
		R_L = 2 kΩ	±10	±13		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	20	200		V/mV
r_i	Input resistance		0.3	2		MΩ
r_o	Output resistance	V_O = 0; see(1)		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V		30	150	µV/V
I_{OS}	Short-circuit output current			±25	±40	mA
I_{CC}	Supply current	V_O = 0; no load		1.7	2.8	mA
P_D	Total power dissipation	V_O = 0; no load		50	85	mW

(1) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.
(2) All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

6.6 Switching Characteristics: µA741C

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ C_L = 100 pF; see Figure 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ C_L = 100 pF; see Figure 1		0.5		V/µs

6.7 Switching Characteristics: µA741Y

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ C_L = 100 pF; see Figure 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ C_L = 100 pF; see Figure 1		0.5		V/µs

6.8 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

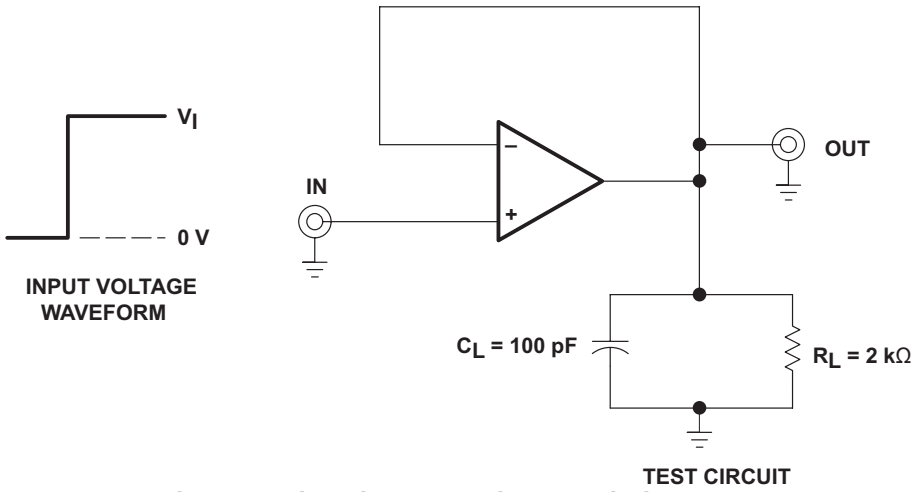


Figure 1. Rise Time, Overshoot, and Slew Rate

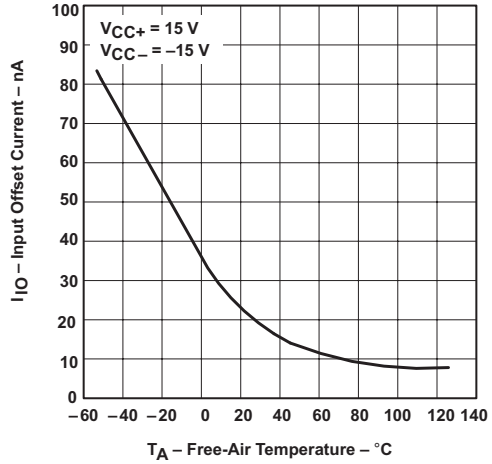


Figure 2. Input Offset Current vs Free-Air Temperature

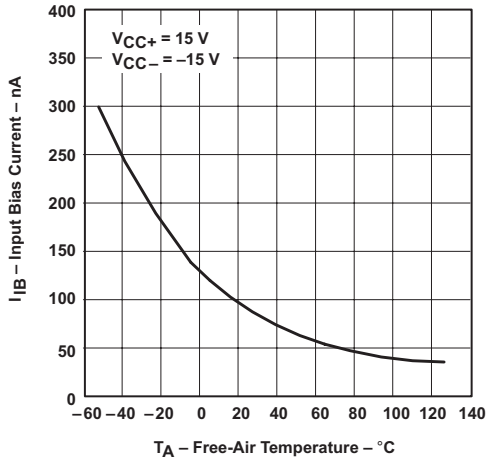


Figure 3. Input Bias Current vs Free-Air Temperature

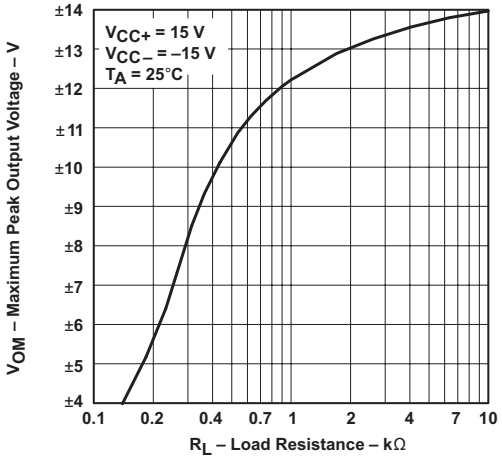


Figure 4. Maximum Output Voltage vs Load Resistance

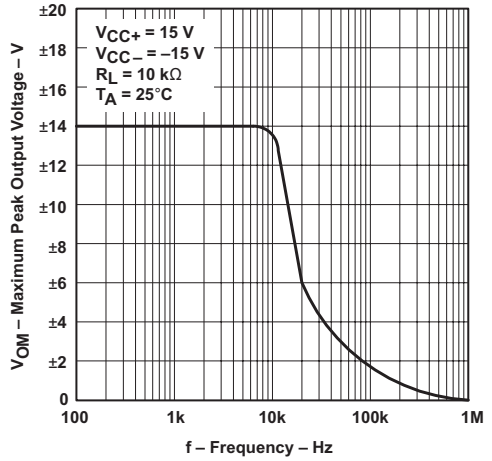


Figure 5. Maximum Peak Output Voltage vs Frequency

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

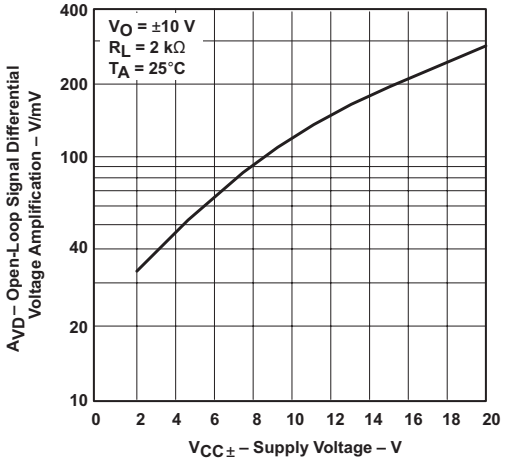


Figure 6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage

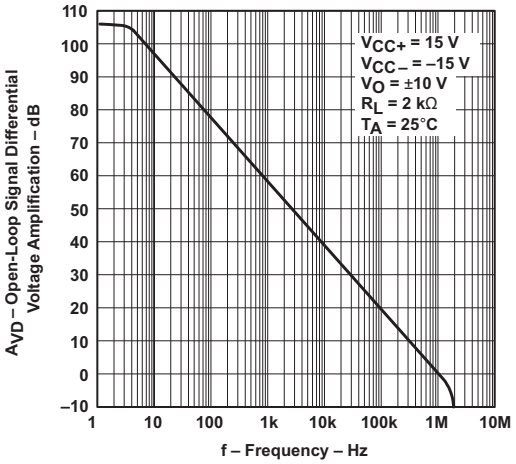


Figure 7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency

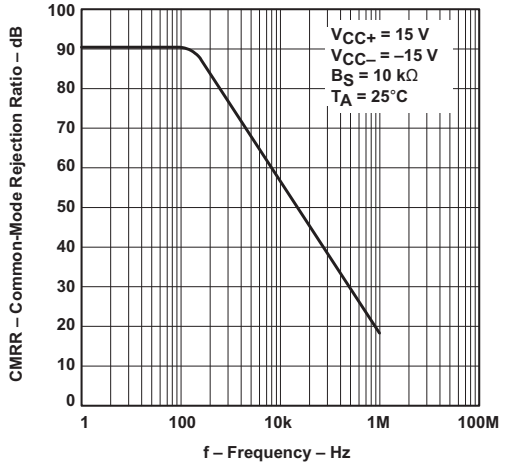


Figure 8. Common-Mode Rejection Ratio vs Frequency

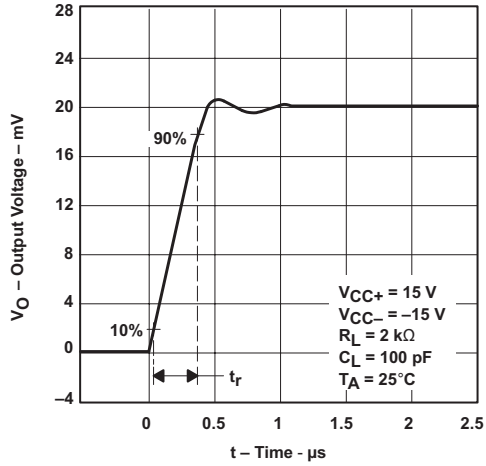


Figure 9. Output Voltage vs Elapsed Time

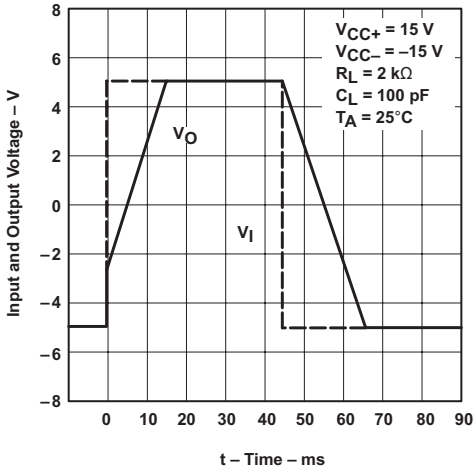


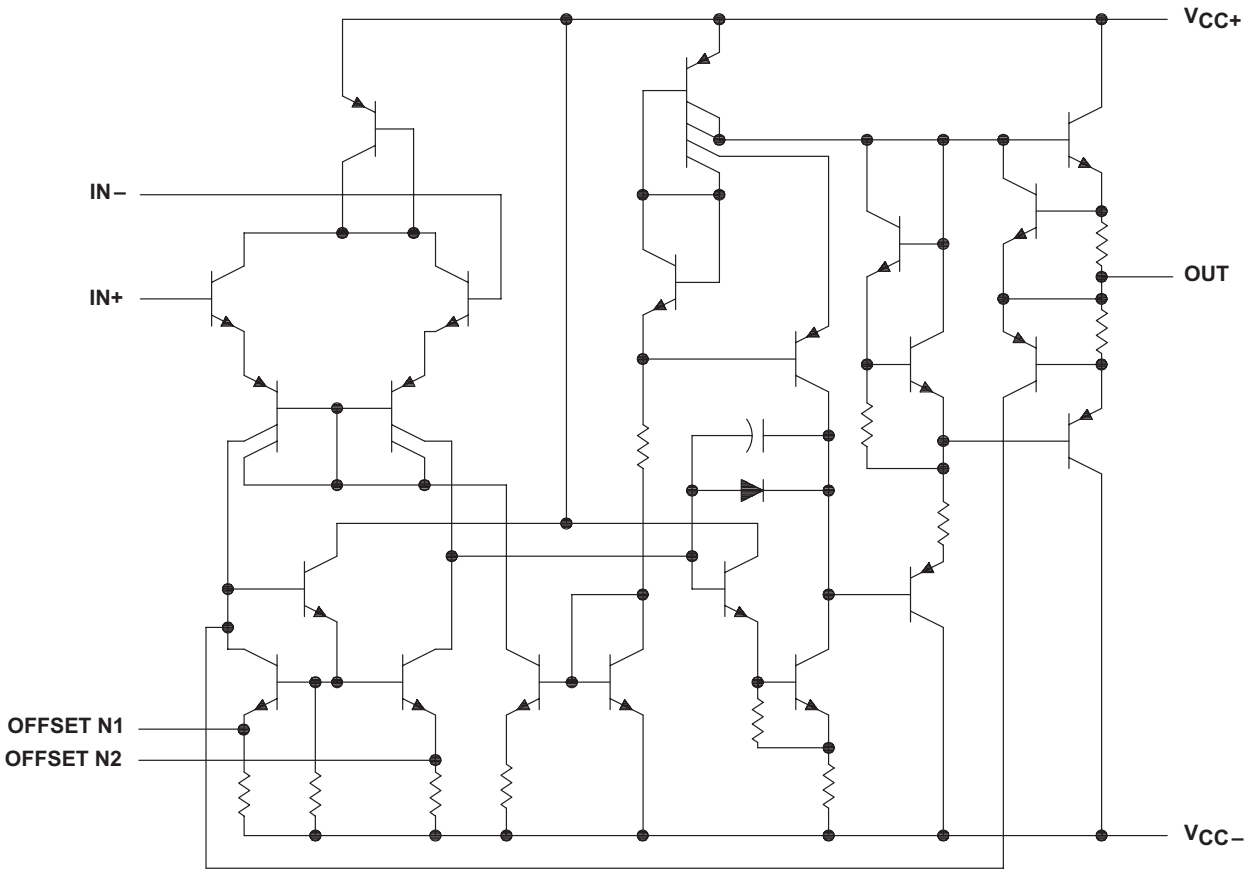
Figure 10. Voltage-Follower Large-Signal Pulse Response

7 Detailed Description

7.1 Overview

The μA741 has been a popular operational amplifier for over four decades. Typical open loop gain is 106 dB while driving a 2000-Ω load. Short circuit tolerance, offset voltage trimming, and unity-gain stability makes the μA741 useful for many applications.

7.2 Functional Block Diagram



Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

7.3 Feature Description

7.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches caused by external circuitry. See *Application and Implementation* for more details on design techniques.