

EE3019

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2019-2020

EE3019 – INTEGRATED ELECTRONICS

November / December 2019

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 4 pages.
2. Answer all 4 questions.
3. All questions carry equal Marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.

1. The parameters of the pMOS and nMOS transistors are given below:

$$\text{pMOS} \quad V_{tp} = -0.6 \text{ V} \quad \mu_p C_{ox} = 100 \text{ } \mu\text{A/V}^2 \quad (W/L)_p = 5$$

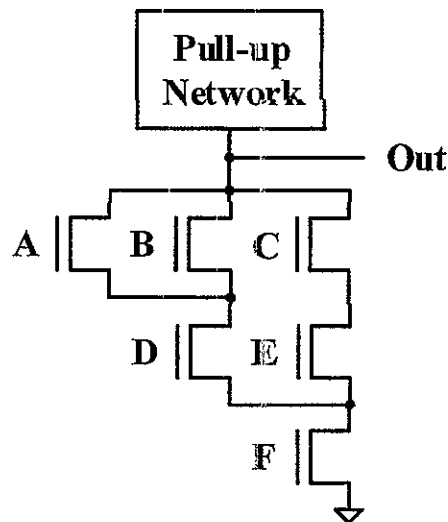
$$\text{nMOS} \quad V_{tn} = 0.6 \text{ V} \quad \mu_n C_{ox} = 250 \text{ } \mu\text{A/V}^2 \quad (W/L)_n = 2$$

- (a) When a 2-input NAND (NAND2) is designed using the given device parameters, determine the switching threshold of the 2-input NAND gate. Use equivalent device sizes when calculating. Assume that the supply voltage is 1.5 V.
(5 Marks)
- (b) Determine the propagation delays (τ_{PHL} and τ_{PLH}) when the 2-input NAND gate designed in part(a) drives 1pF. Assume that all the input signals switch at the same time with zero rise and fall times.
(10 Marks)
- (c) Explain how to make τ_{PHL} and τ_{PLH} of the above 2-input NAND gate in part(b) identical.
(5 Marks)

Note: Question No. 1 continues on page 2.

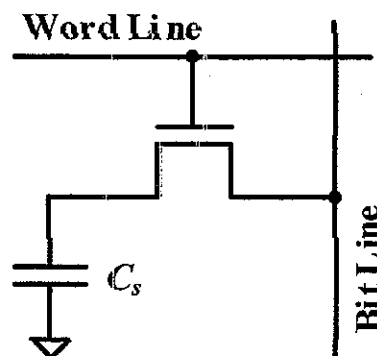
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- (d) When a transmission gate is designed using the given device parameters, calculate the on-resistance of the transmission gate when the output is at 0 V and 1.5 V. Assume that the input signal is 1.5 V and the supply voltage is 1.5 V. (5 Marks)
2. (a) A CMOS logic circuit is shown in Figure 1. Determine the equivalent width of the pull-down network using both best and worst case scenarios. Assume that the width of the nMOS transistors is W . Explain how to increase the switching threshold of the logic circuit.

**Figure 1**

(5 Marks)

- (b) A DRAM cell is shown in Figure 2. Calculate the voltage swing at the bit line when the voltage stored in the cell capacitor (30 fF) is 0 V and 5 V. Each DRAM cell has the parasitic capacitance of 10 fF on the bit line, and the number of DRAM cells on the bit line is 512. Assume that the bit line is pre-charged to 2.5 V.

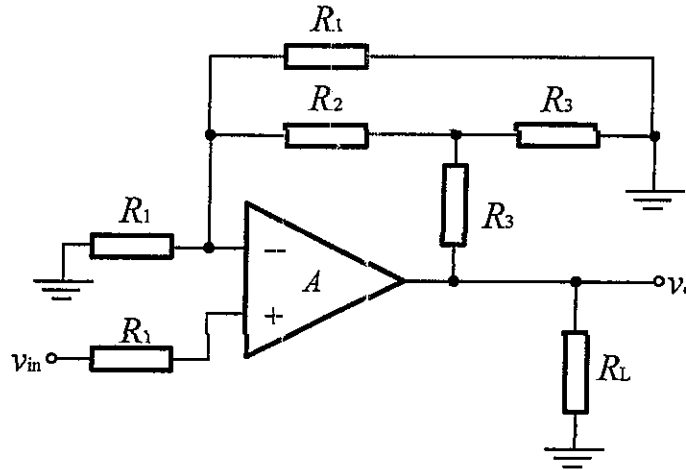
**Figure 2**

(5 Marks)

Note: Question No. 2 continues on page 3.

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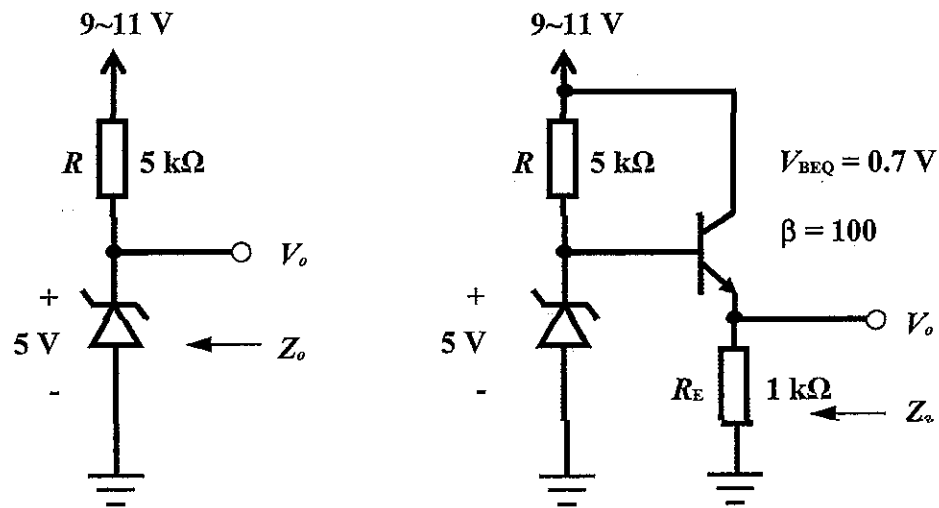
- (c) A negative-feedback amplifier is shown in Figure 3. Assume that $A = 1000$, $R_1 = 1 \text{ k}\Omega$, $R_2 = 2 \text{ k}\Omega$, $R_3 = 3 \text{ k}\Omega$, and $R_L = 4 \text{ k}\Omega$.

**Figure 3**

- (i) Calculate the feedback factor β . (5 Marks)
 - (ii) Derive the closed-loop gain (A_f) equation. (5 Marks)
 - (iii) When A decreases by 30%, determine the corresponding decrease in A_f in percentage (%). (5 Marks)
3. Figure 4 on page 4 shows the voltage-reference circuits. The dynamic small-signal resistance of each Zener diode $r_z = 100 \Omega$.
- (a) Find the DC output voltage of each circuit. (8 Marks)
 - (b) Draw the small-signal equivalent circuit and derive an expression for the output impedance Z_o of each circuit. (10 Marks)
 - (c) Comment on the advantages and disadvantages of the voltage-reference circuits. (7 Marks)

Note: Question No. 3 continues on page 4.

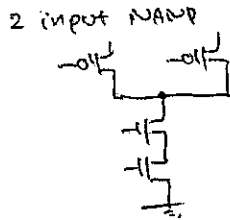
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**Figure 4**

4. Given three MOSFETs with channel lengths of $10\ \mu\text{m}$, channel widths of $100\ \mu\text{m}$, threshold voltage of $1\ \text{V}$, early voltage of $100\ \text{V}$ and $\mu_n C_{ox} = 20\ \mu\text{A}/\text{V}^2$, it is required to design the circuit for a Wilson MOSFET constant current source to obtain an output of $100\ \mu\text{A}$ with a power supply $V_{DD} = 10\ \text{V}$.
- Draw the schematic of the Wilson MOSFET constant current source. (5 Marks)
 - What is the lowest possible value of the output voltage? (10 Marks)
 - Find the change in output current resulting from a 3-V change in the output voltage. (10 Marks)

END OF PAPER

(1) (a)



$$(W/L)_{PMOS} = 5+5=10$$

$$(W/L)_{NMOS} = \frac{1}{\frac{1}{2} + \frac{1}{2}} = 1$$

$$I_{ON} = I_{OP}$$

$$\frac{250}{2} (V_{TH} - 0.6)^2 = \frac{100}{2} 10 (V_{TH} - 1.5 + 0.6)^2$$

$$\frac{V_{TH} - 0.6}{V_{TH} - 0.9} = \sqrt{\frac{1000}{250}} = 2$$

$$V_{TH} = 1.2 \text{ V}$$

(b)

$$\tau_{PHL} = \frac{C \Delta V_{HL}}{I_{AVG}}$$

↳ NMOS

$$V_{IN} = V_G = 1.5 \text{ V}$$

Define τ_{PHL} as t from V_{OH} to $V_{50\%}$

$$\Delta V_{HL} = 1.5 - 0.75 = 0.75 \text{ V}$$

$$I_{AVG} = \frac{1}{2} (I_{V_{OH}} + I_{V_{50\%}})$$

$$\text{at } V_{OH} \rightarrow V_{GS} = 1.5 \text{ V} \quad V_{DS} = V_{OH} = 1.5 \text{ V} \rightarrow V_{DS} > V_{GS} - V_{TH} \rightarrow \text{saturation}$$

$$\text{at } V_{50\%} \rightarrow V_{GS} = 1.5 \text{ V} \quad V_{DS} = \frac{1}{2} V_{OH} = 0.75 \text{ V} \rightarrow V_{DS} < V_{GS} - V_{TH} \rightarrow \text{linear}$$

$$I_{V_{OH}} = \frac{\mu_n C_{ox}}{2} (W/L)_{NMOS} (V_{GS} - V_{TH})^2 = \frac{250 \cdot 10^{-6}}{2} (1) (1.5 - 0.6)^2 = 1.0125 \cdot 10^{-4} \text{ A}$$

$$I_{V_{50\%}} = \mu_n C_{ox} (W/L)_{NMOS} \left((V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$= 250 \cdot 10^{-6} (1) \left((1.5 - 0.6) (0.75) - \frac{0.75^2}{2} \right) = 9.84375 \cdot 10^{-5} \text{ A}$$

$$I_{AVG} = 9.984 \cdot 10^{-5} \text{ A}$$

$$\tau_{PHL} = \frac{10^{-15} \cdot 0.75}{9.984 \cdot 10^{-5}} = 7.511 \cdot 10^{-12} \text{ s}$$

τ_{PLH} → PMOS

$$V_{IN} = V_G = 0 \text{ V}$$

Define τ_{PLH} as t from V_{OL} to $V_{50\%}$

$$\Delta V_{LH} = 0.75 \text{ V}$$

$$\text{at } V_{OL} \rightarrow V_{SG} = 1.5 \text{ V} \quad V_{SD} = 1.5 \text{ V} \rightarrow V_{SD} > V_{SG} - |V_{TP}| \rightarrow \text{saturation}$$

$$\text{at } V_{50\%} \rightarrow V_{SG} = 1.5 \text{ V} \quad V_{SD} = 1.5 - 0.75 = 0.75 \text{ V} \rightarrow V_{SD} < V_{SG} - |V_{TP}| \rightarrow \text{linear}$$

$$I_{V_{OL}} = \frac{\mu_p C_{ox}}{2} (W/L)_{PMOS} (V_{GS} - V_{TP})^2 = \frac{100 \cdot 10^{-6}}{2} (10) (-1.5 + 0.6)^2 = 4.05 \cdot 10^{-4} \text{ A}$$

$$I_{V_{50\%}} = \mu_p C_{ox} (W/L)_{PMOS} \left((V_{GS} - V_{TP}) V_{SD} - \frac{V_{SD}^2}{2} \right)$$

$$= 100 \cdot 10^{-6} (10) \left((-1.5 + 0.6) (-0.75) - \frac{(-0.75)^2}{2} \right) = 3.9375 \cdot 10^{-4} \text{ A}$$

$$I_{AVG} = 3.99375 \cdot 10^{-4} \text{ A}$$

$$\tau_{PLH} = \frac{10^{-15} \cdot 0.75}{3.99375 \cdot 10^{-4}} = 1.8779 \cdot 10^{-12} \text{ s}$$

③ $C_{out} = C_{in} \rightarrow I_{avg, out} = I_{avg, in} \rightarrow \frac{1}{2}(I_{out} + I_{V_{DD}}) = \frac{1}{2}(I_{out} + I_{V_{DD}})$

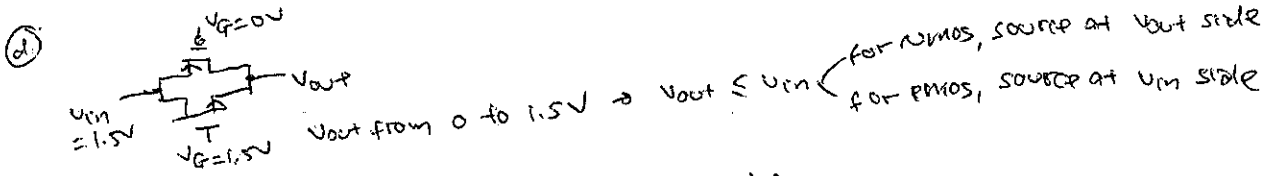
$$\mu_{pCox} \left(\frac{W}{L}\right)_{pMOS} \left(\frac{1}{2}(-1.5 + 0.6)^2 + ((-1.5 + 0.6)(-0.75) - \frac{(-0.75)^2}{2}) \right)$$

$$= \mu_{nCox} \left(\frac{W}{L}\right)_{nMOS} \left(\frac{1}{2}(1.5 - 0.6)^2 + ((1.5 - 0.6)(0.75) - \frac{0.75^2}{2}) \right)$$

$$\mu_{pCox} \left(\frac{W}{L}\right)_{pMOS} = \mu_{nCox} \left(\frac{W}{L}\right)_{nMOS}$$

for $C_{out} = C_{in} \rightarrow \frac{\left(\frac{W}{L}\right)_{pMOS}}{\left(\frac{W}{L}\right)_{nMOS}} = \frac{\mu_{nCox}}{\mu_{pCox}} = \frac{250}{100} = 2.5$

now $\rightarrow \left(\frac{W}{L}\right)_{pMOS} = 10$, so need to decrease W_p or increase W_n .



$V_{out} = 0V$
 NMOS $V_{GS} = 1.5V$ $V_{DS} = 1.5V \rightarrow$ saturation
 $I_{Dn} = \frac{250 \cdot 10^{-6}}{2} (2)(1.5 - 0.6)^2 = 2.025 \cdot 10^{-4} A$

PMOS $V_{GS} = 1.5V$ $V_{SD} = 1.5V \rightarrow$ saturation
 $I_{Dp} = \frac{100 \cdot 10^{-6}}{2} (5)(1.5 - 0.6)^2 = 2.025 \cdot 10^{-4} A$

$$R = \frac{V_{in} - V_{out}}{I_{Dn} + I_{Dp}} = 3703.7 \Omega //$$

$V_{out} = 1.5V$

NMOS $V_{GS} = 0V \rightarrow$ cutoff $\rightarrow I_{Dn} = 0$

PMOS $V_{GS} = 1.5V$ $V_{SD} = 0V \rightarrow I_{Dp} = 0$

$$R = \infty //$$

2. (a) Best case \rightarrow All on.

$$W_{A,B} = 2W$$

$$W_{CE} = \frac{1}{1+1} W = \frac{1}{2} W.$$

$$W_{ABD} = \frac{1}{\frac{1}{2}+1} W = \frac{2}{3} W$$

$$W_{ABDCE} = \frac{2}{3} W + \frac{1}{2} W = \frac{7}{6} W$$

$$W_{ABDCEF} = W_{eq} = \frac{1}{\frac{6}{7}+1} W = \frac{7}{13} W //$$

Worst case \rightarrow C, E, F on or A, D, F on or B, D, F on.

$$W_{CE} = W_{AD} = W_{BD} = \frac{1}{2} W.$$

$$W_{eq} = \frac{1}{2+1} W = \frac{1}{3} W //$$

increase switching threshold \rightarrow by decreasing nmos width.
or increase pmos width.

(b) Store 0V

$$Q_{initial} = Q_{final}$$

$$2.5 \times (512 \times 10^{-15}) = (30 \times 10^{-15} + 512 \times 10^{-15}) V_{final}$$

$$V_{final} = 2.4854 V \rightarrow \Delta V = -0.014563 V //$$

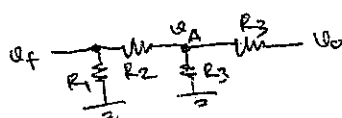
Store 5V

$$Q_{initial} = Q_{final}$$

$$2.5 \times (512 \times 10^{-15}) + 5 \times 30 \times 10^{-15} = (30 \times 10^{-15} + 512 \times 10^{-15}) V_{final}$$

$$V_{final} = 2.5145 V \rightarrow \Delta V = 0.014563 V //$$

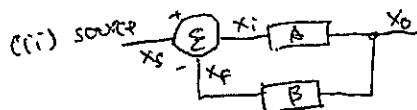
(c) (i).



$$\Rightarrow V_A = \frac{R_3 || (R_2 + R_1)}{R_3 + R_3 || (R_2 + R_1)} V_O = \frac{1}{3} V_O$$

$$V_F = \frac{R_1}{R_1 + R_2} V_A = \frac{1}{3} \cdot \frac{1}{3} V_O = \frac{1}{9} V_O.$$

$$\beta = \frac{V_F}{V_O} = \frac{1}{9} //$$



$$\left. \begin{aligned} x_I &= x_S - x_F \\ x_O &= A x_I \\ x_F &= \beta x_O \end{aligned} \right\}$$

$$x_O = A(x_S - \beta x_O)$$

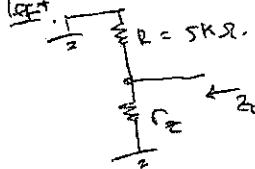
$$\frac{x_O}{x_S} = \frac{1}{1 + \beta A} \rightarrow \frac{x_O}{x_S} = \frac{A}{1 + \beta A} = A_F //$$

$$(iii) \frac{dA_F}{A_F} = \frac{1}{1 + \beta A} \frac{dA}{A}$$

$$\frac{dA_F}{A_F} = \frac{1}{1 + \frac{1000}{9}} (-30\%) = -0.267\% //$$

② a) left $\Rightarrow V_b = 5V$ right $\Rightarrow V_b = 5 - 0.7 = 4.3V_{bc}$

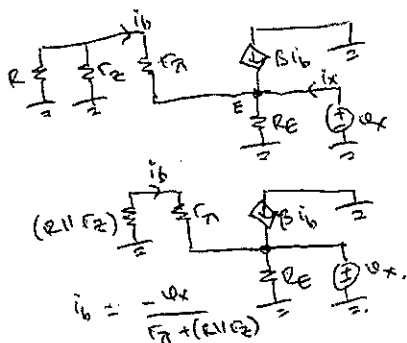
⑥ left $R = 5k\Omega$



$$Z_o = \frac{1}{\frac{1}{R} + \frac{1}{\beta R_L}} = 98.04\Omega$$

right $I_E = \frac{5 - 0.7}{1k} = 4.3 \times 10^{-3} A$ $I_C = \frac{100}{101} I_E = 4.257 \times 10^{-3} A$

$g_m = \frac{I_C}{V_T} = 0.1637 S$ $r_{\pi} = \frac{\beta}{g_m} = 610.7\Omega$



KCL at node E.

$$i_x - \frac{V_x}{R_E} + \beta i_b + i_b = 0$$

$$i_x - \frac{V_x}{R_E} + (\beta + 1) \left(\frac{-V_x}{r_{\pi} + (R_L || R_2)} \right) = 0$$

$$i_x = V_x (0.1435)$$

$$Z_o = \frac{V_x}{i_x} = 6.9683\Omega_{||}$$

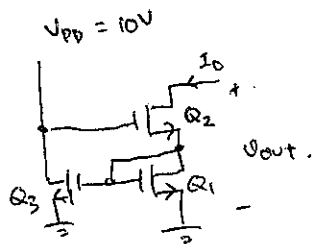
③ - Not sure -

Advantage = giving stable voltage even when supply voltage is unstable

Disadvantage \Rightarrow output voltage slightly changes due to R_2

\rightarrow low efficiency for heavy load currents, because if load current is large, there will be considerable power loss in the series-limiting resistance.

4. a



- 6) V_{out} so transistors in saturation.
- $\frac{W}{L} = 10$ $V_{th} = 1V$ $V_A = 100V$ $\mu_n C_{ox} = 20 \cdot 10^{-6}$
- $I_D \approx 100 \cdot 10^{-6} A = I_{D1} = I_{D2}$
- $I_{D1} = 100 \cdot 10^{-6} = \frac{20 \cdot 10^{-6}}{2} \cdot 10 (V_{GS1} - 1)^2 \rightarrow V_{GS1} = 2V$
- $I_{D2} = 100 \cdot 10^{-6} = \frac{20 \cdot 10^{-6}}{2} \cdot 10 (V_{GS2} - 1)^2 \rightarrow V_{GS2} = 2V$
- $V_{G1} = V_{D1} = V_{S2} = 2V \rightarrow V_{G2} = 2 + 2 = 4V$
- for saturation $\rightarrow V_{DS2} > V_{GS2} - 1$
- $V_{out} - V_{S2} > V_{G2} - V_{S2} - 1$
- $V_{out} > 4 - 1 = 3V //$

c)

$$R_{out} \approx (g_{m2} r_{o2}) r_{o3}$$

$$g_{m2} = 2 \cdot 10^{-4} \text{ A/V} \quad r_{o2} = 1 \text{ M}\Omega \quad r_{o3} = 1 \text{ M}\Omega$$

$$R_{out} \approx 2 \cdot 10^8 \Omega //$$

$$\Delta I = \frac{3}{R_o} = 1.5 \cdot 10^{-8} \text{ A} //$$

TIPS

- All questions have similar difficulty level
 - digital part is "easier" but very tedious
 - analog part is "harder" but can be solved quickly once you get it.
- Analog questions pattern change almost every EYP. It depends on your prof's arrangement (ex- which part has been in quiz, etc.).
- For digital, you ~~can~~ ^{may} expect the questions to be similar to EYP (CPL, CPLT, V_{th} , $(W/L)_{eq}$, transmission gate, feedback)
- Reverse your tutorial / very useful, especially for digital part, since I think there is not much variations for digital questions.

