

**NANYANG
TECHNOLOGICAL
UNIVERSITY**

EE2073 Project Report

Automatic Volume Control for Audio Amplifier System

School of Electrical and Electronic Engineering

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Semester 1

Content:

Chapter 1: Introduction -----	3
Chapter 2: VCA subsystem -----	4
Chapter 3: Power Amplifier (PA) -----	8
Chapter 4: Volume Unit Meter -----	14
Chapter 5: Integration of VCA, PA and VU -----	18
Chapter 6: Manual Volume Control -----	21
Chapter 7: Automatic Volume Control (Complete system) -----	24
Conclusion -----	29
Recommendations for next batches -----	29
References -----	30
Appendix -----	31

Chapter 1: Introduction

The purpose of the project is to design an automated controller system to keep the volume out of an audio system remain at an adjustable value set by the user. To achieve this purpose, a digital system was designed and implemented as shown in Figure 1.1.

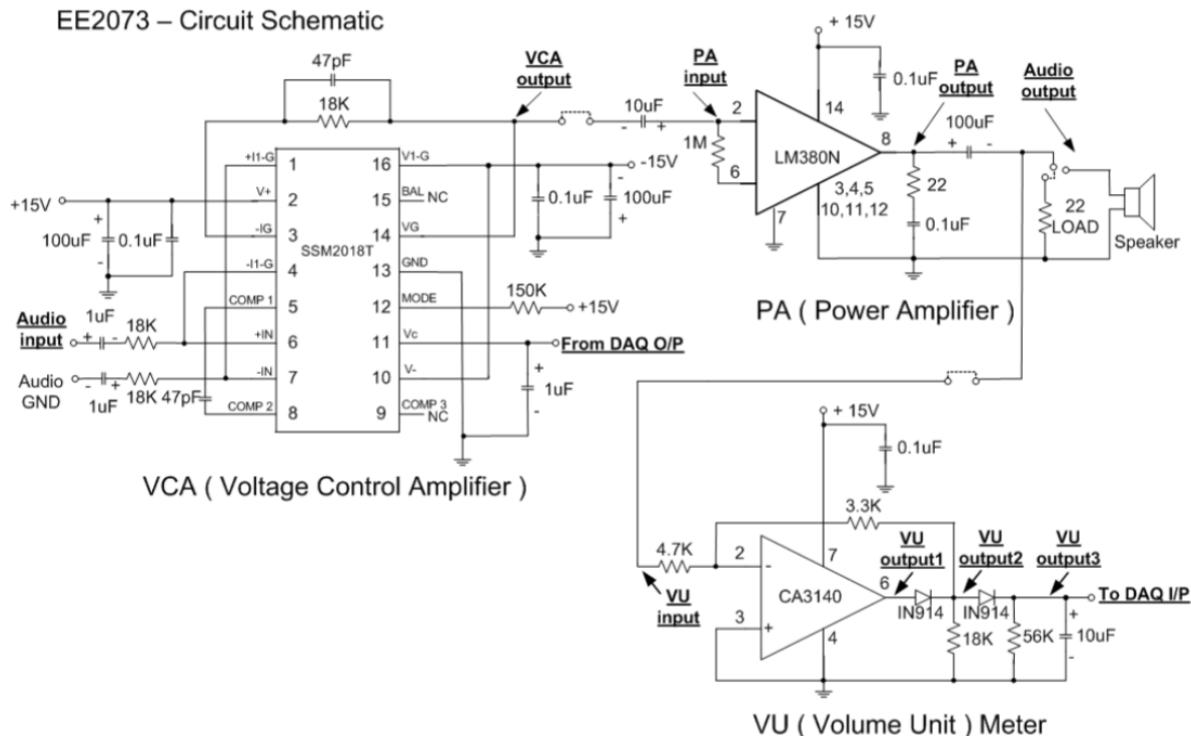


Figure 1.1 The circuit schematic for the entire system

The system contains three major part in the order of:

- Volume Unit Meter** playing the role of **output level sensor**
- Voltage Controlled Amplifier(VCA)** playing the role of **gain control block or actuator**
- Power Amplifier** playing the role of amplifying the signal

In practical implementation of such a digital system, Data Acquisition Block and LabVIEW was used to act as the perfect and integrated platform in the **discrete-time, sampled-data dimension**. The design starts from individual design and testing of VCA, PA and VU sub-circuits and integration of the three. Then an adding of a “forced” or “manual” feedback signal to test the open-loop circuit function. At last, adding of a closed loop feedback system.

Chapter 2: VCA subsystem

The Voltage Controlled Amplifier is an signal subsystem, which could be used to control the gain by applying the control voltage (V_c)

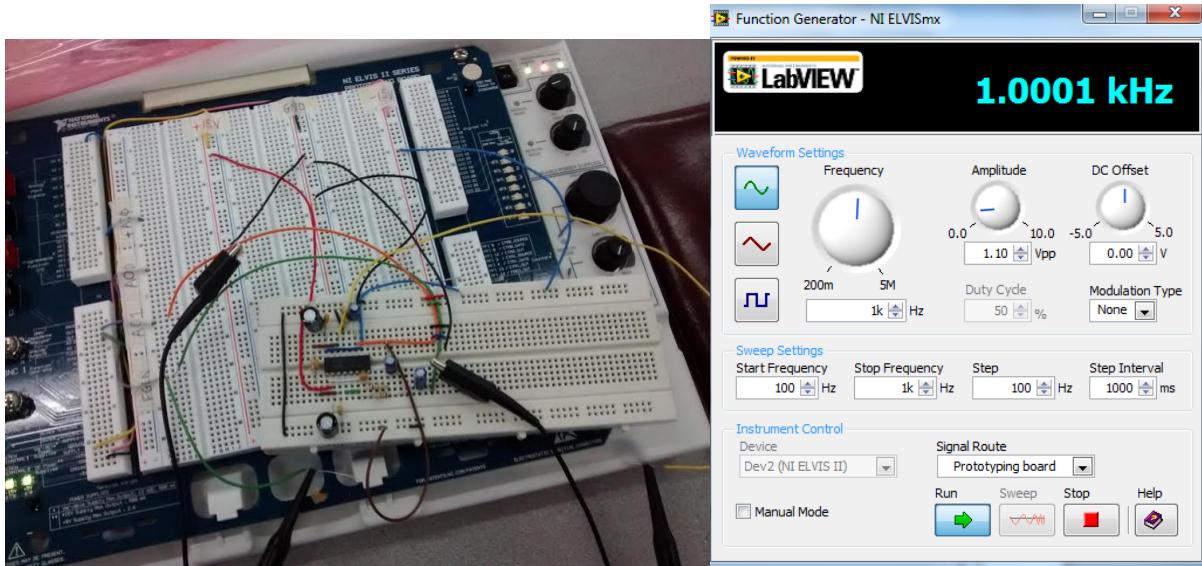


Figure 2.1 Breadboard connection and function generator setting

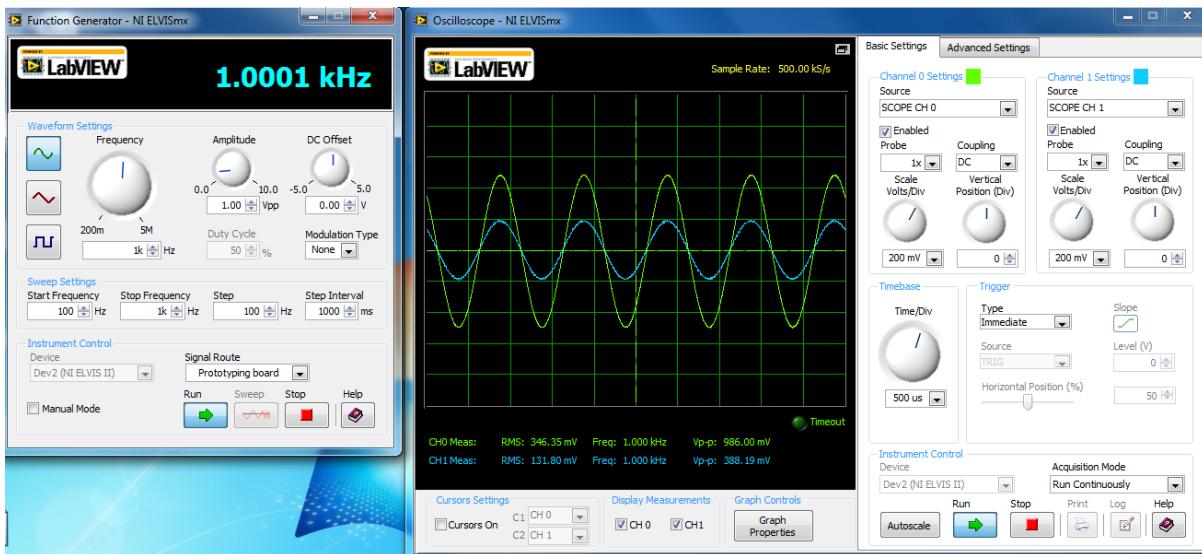


Figure 2.2 Output result sample for the VCA

EE2073 – Circuit Schematic

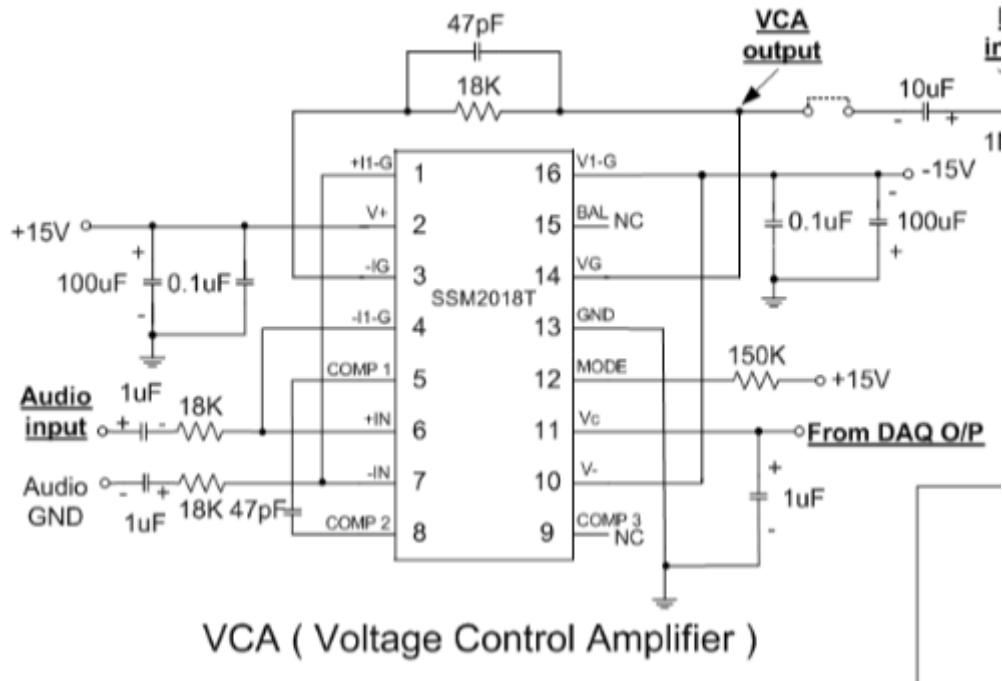


Figure 2.3 Circuit Schematic of VCA

After the assemble of the subsystem, practical experiments have been done on it using a set of values as shown in Table 2.1. Based on the experiment results, Measured Gains were calculated and used to compare with Theoretical Gain. The theoretical gain is computed using the following formula and used as a benchmark:

$$\text{Gain} = e^{-aV_c},$$

where $a=3.623$ when the chipsets are working normally under room temperature. If converted into dB, the following formulas was used instead:

$$\text{Gain (dB)} = 20 \log(e^{-aV_c})$$

Liu Song:	VIN (Vpp)	VC (V)	VOUT (Vpp)	Measured Gain = VOUT/VIN	Measured Gain (dB)	Theoretical Gain	Theoretical Gain (dB)
1.1	1.5	0.02		0.018181818	-34.80725379	0.004363416	-47.20346724
1.1	1	0.04		0.036363636	-28.78665388	0.026702449	-31.46897816
1.2	0.5	0.2		0.166666667	-15.56302501	0.16340884	-15.73448908
1.2	0.25	0.48		0.4	-7.958800173	0.404238592	-7.86724454
1.7	0	1.65		0.970588235	-0.259299543	1	0
0.4	-0.25	0.97		2.425	7.694234859	2.473786567	7.86724454
0.7	-0.5	4.23		6.042857143	15.62484655	6.119619981	15.73448908
0.7	-1	N/A				37.44974871	31.46897816

Table 2.1 Record of the test and calculation results of VCA subsystem

To interpret the measured results intuitively, we have drawn the measured gain against V_c in figure 2.4. The graph of the theoretical gain against V_c is also drawn in figure 2.5 as a comparison.

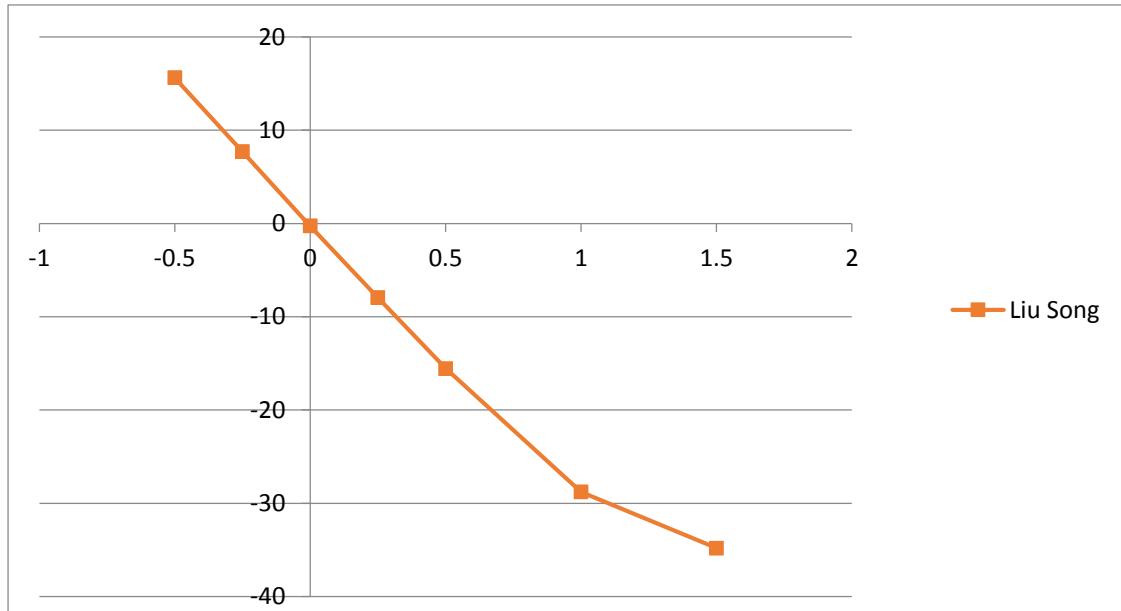


Figure 2.4 Measured Gain against V_c

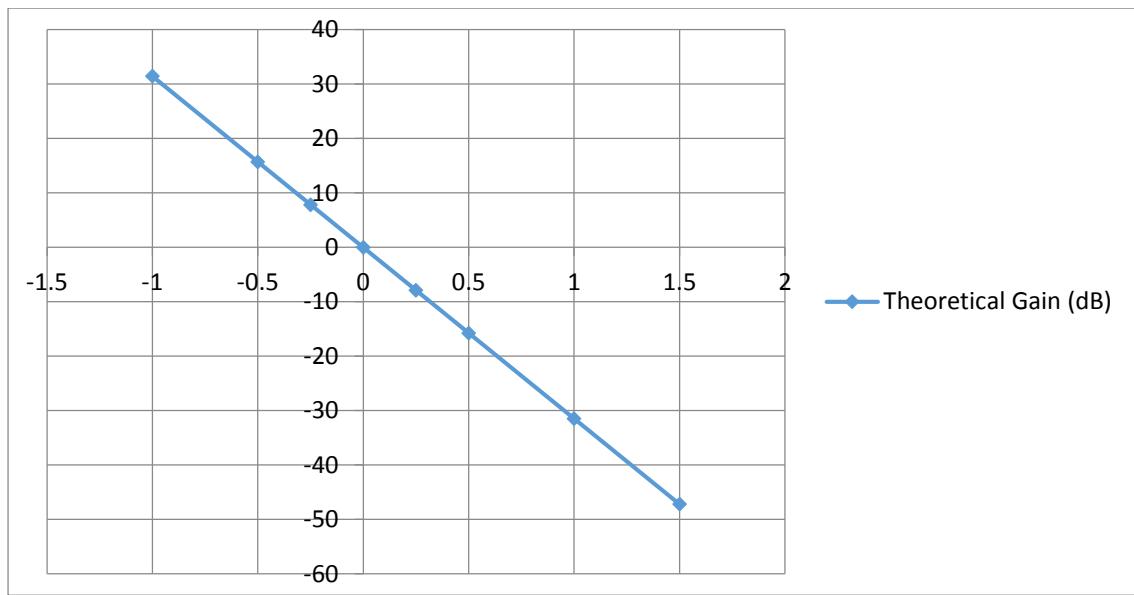


Table 2.5 Theoretical Gain against V_c

The V_c sensitivity is computed as the inverse of the slope of the graph:

$$\text{Sensitivity on } V_c = \frac{1}{(15.269 - (-15.4))/(-0.5 - 0.5)} \approx -0.0326 \text{ } V/\text{dB}$$

This measured and computed value of sensitivity of 32.5 mV/dB is very close the theoretical value of 31.78 mV/dB under the room temperature. The errors were trial and could be ignored. Hence the VCA subsystem is generally satisfactory at this stage.

Chapter 3 Power Amplifier (PA)

Power amplifier is the central component in the entire system that enlarge the signal level to a certain level enough to drive an audio speaker. The breadboard of this subsystem is connected according to the circuit schematic as shown in Figure 3.1

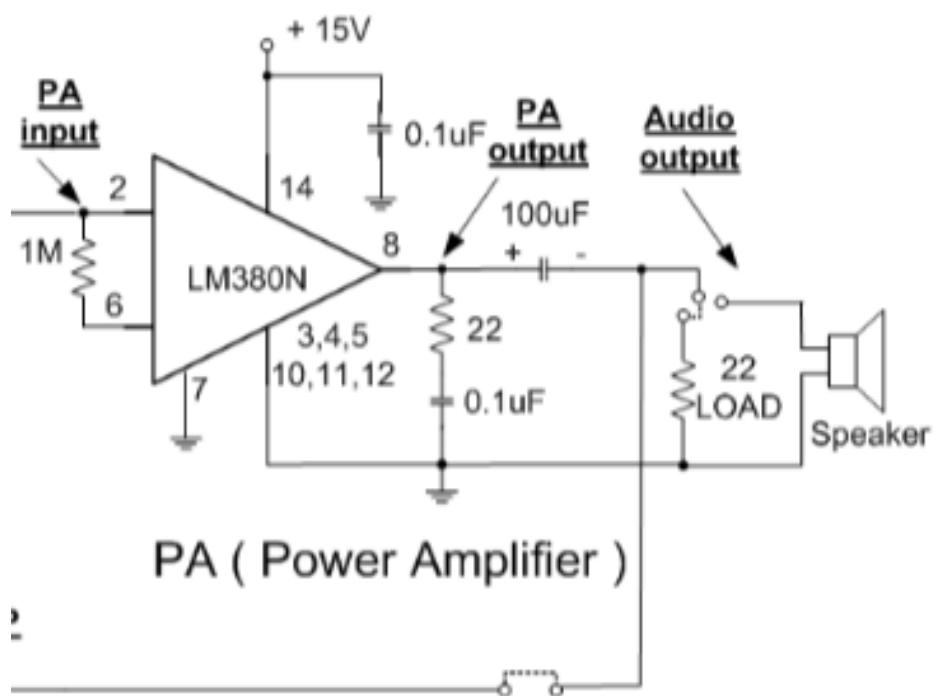
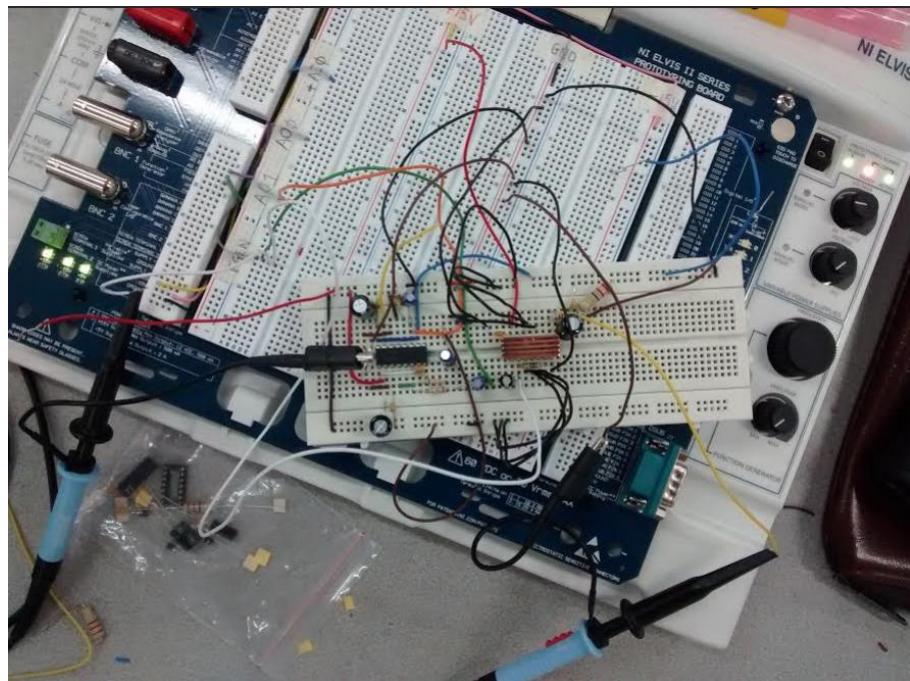


Figure 3.1 Breadboard connection and circuit schematic of PA

3.1 First set of result with a 1kHz sinusoidal input

Connecting Channel 0 to PA input and CH1 to the PA output, setting and use the function generator setting of:

- Sinusoidal wave
- 1k Hz
- 0.002 Vpp
- DC offset: 0v
- Step frequency: 1k Hz
- Step interval: 1000 ms

and we could get a clear graph of the signals at the two nodes as shown in figure 3.2.

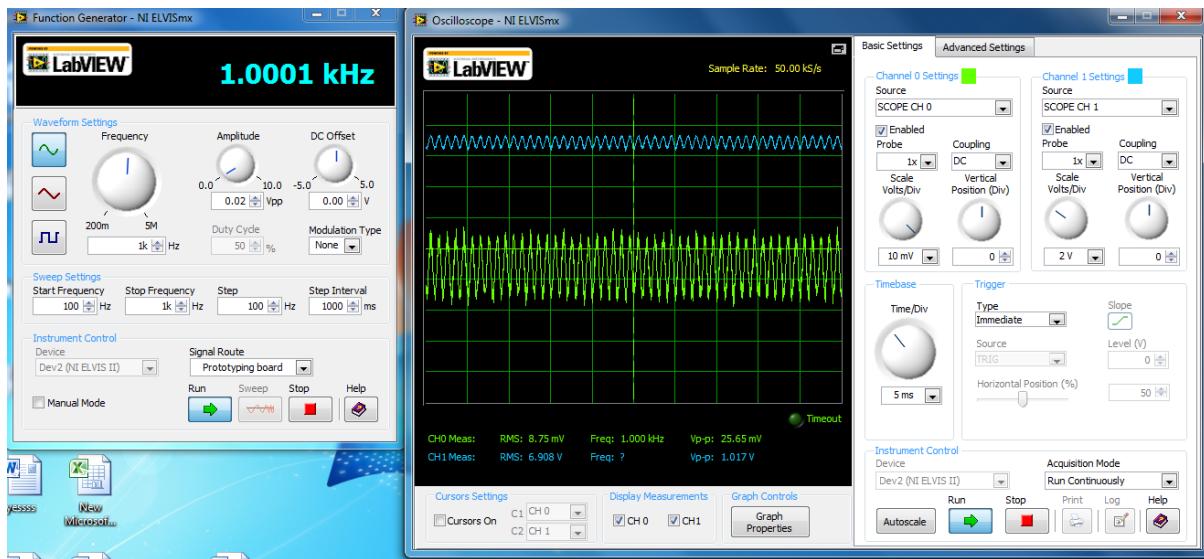


Figure3.2 Graph of PA input and output using a set of input

From the graph above:

$$\text{calculated gain} = 20 \log_{10} \left(\frac{V_{out}}{V_{in}} \right) = 20 \log_{10} \left(\frac{1.017v}{25.65mv} \right) = 32 \text{dB},$$

Which is close to the expected value of 34dB within a reasonable range of error, which may be due to environmental factors such as temperature heat up of chipsets.

3.2 Testing and capture the bode Plot with a Start frequency of 100Hz, stop frequency of 200KHz, Steps as 20 per decade and Vpp=0.01V.

We have captured the bode graph as shown in figure 3.3.



Figure 3.3 Another set of Bode plots for PA

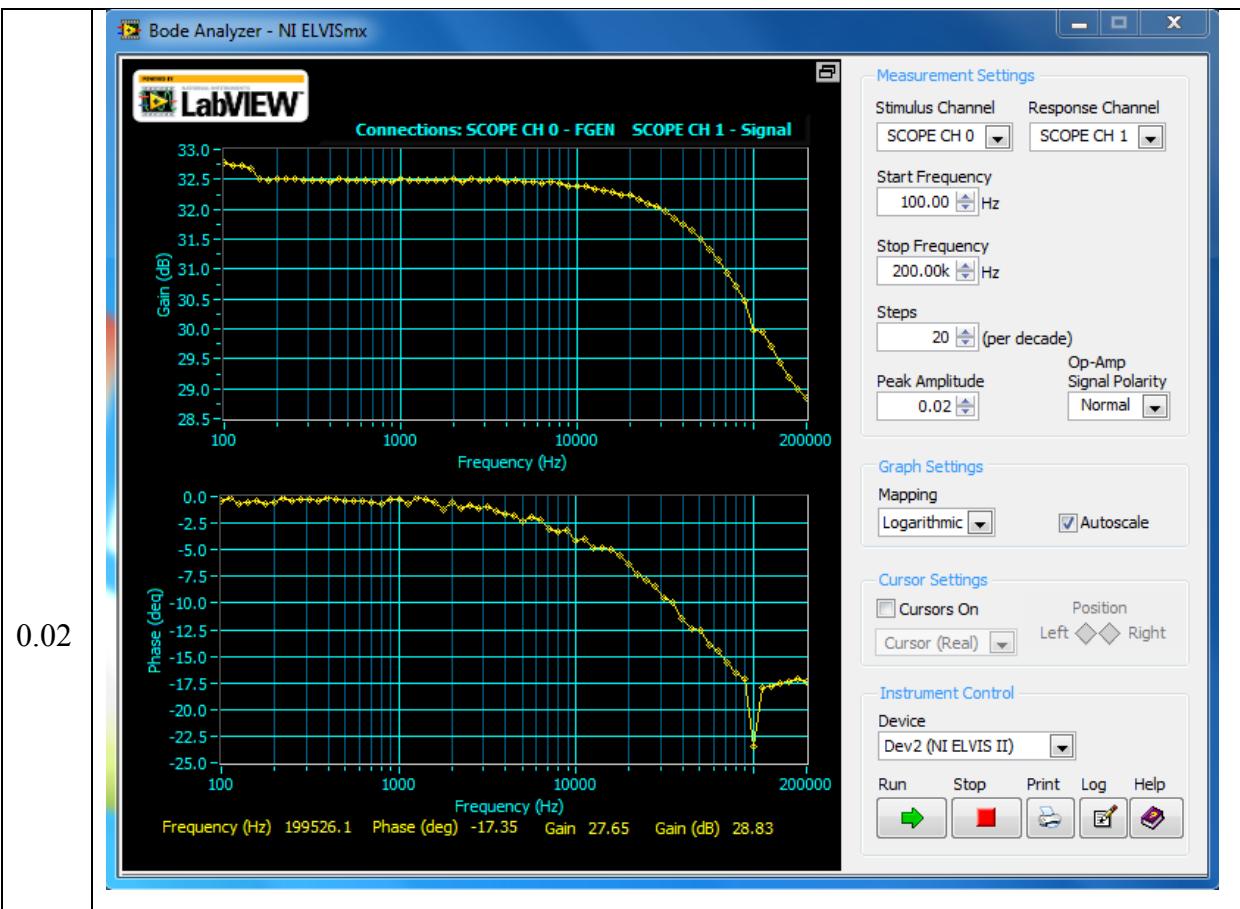
Discussion: is this the frequency response what we expect?

The Gain at low frequency = 32.5dB, cutoff frequency = $32.5 - 3 = 29.5$ dB

The value is very close to what we expected within a reasonable range of experimental error.

3.3 Capture Bode Analyzer Windows with matriculation card numbers(U1122747F):

Vp(Bode analyser window capture of the PA gain and phase response
V)	



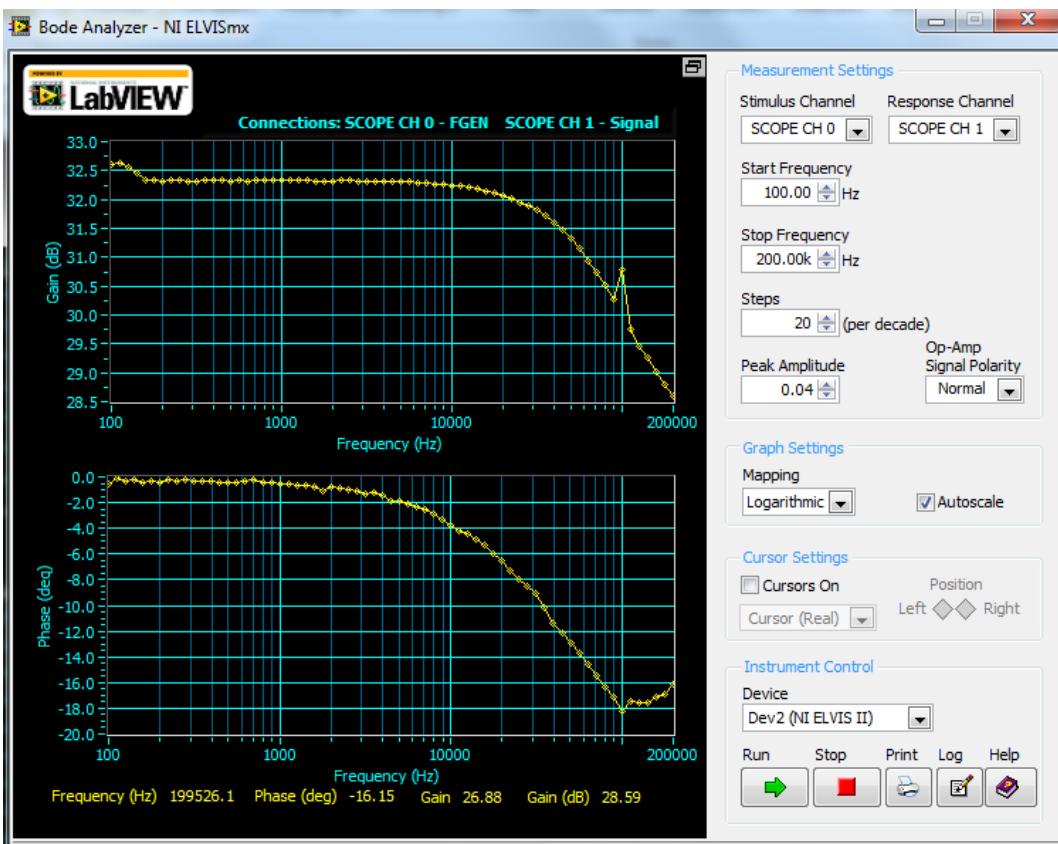


Table 3.1 Bode plots of gain and phase response graph

3.4 Additional observations and discussions

- a) If $V_{pp} = 0.01V, 0.02V, 0.04V, 0.07V$, the measured gain approximate to 32.4dB at frequency range of 100Hz to 10000Hz. This is extremely close to the expected gain of 34dB.
- b) We have observed a different level of distortion for all the above graph. There is no significant distortion for the values we used during the experiments. However, we expect the see very large distortion when V_{pp} exceeds 0.6V. This is because the gain of the PA is approximately 34dB or 50V/V, and when V_{pp} exceeds 0.6V, the range for the output will exceed 30V. Since the output will always be bounded by the power supply (-15, +15), any value beyond the range will not attainable.

Chapter 4 Volume Unit Meter

VU Meter acts as a sensor or output level detector for the PA output signal. Its output could then again used as a feedback node back to the VCA through node Vc. The breadboard is connected according to its circuit schematic as shown in figure 4.1.

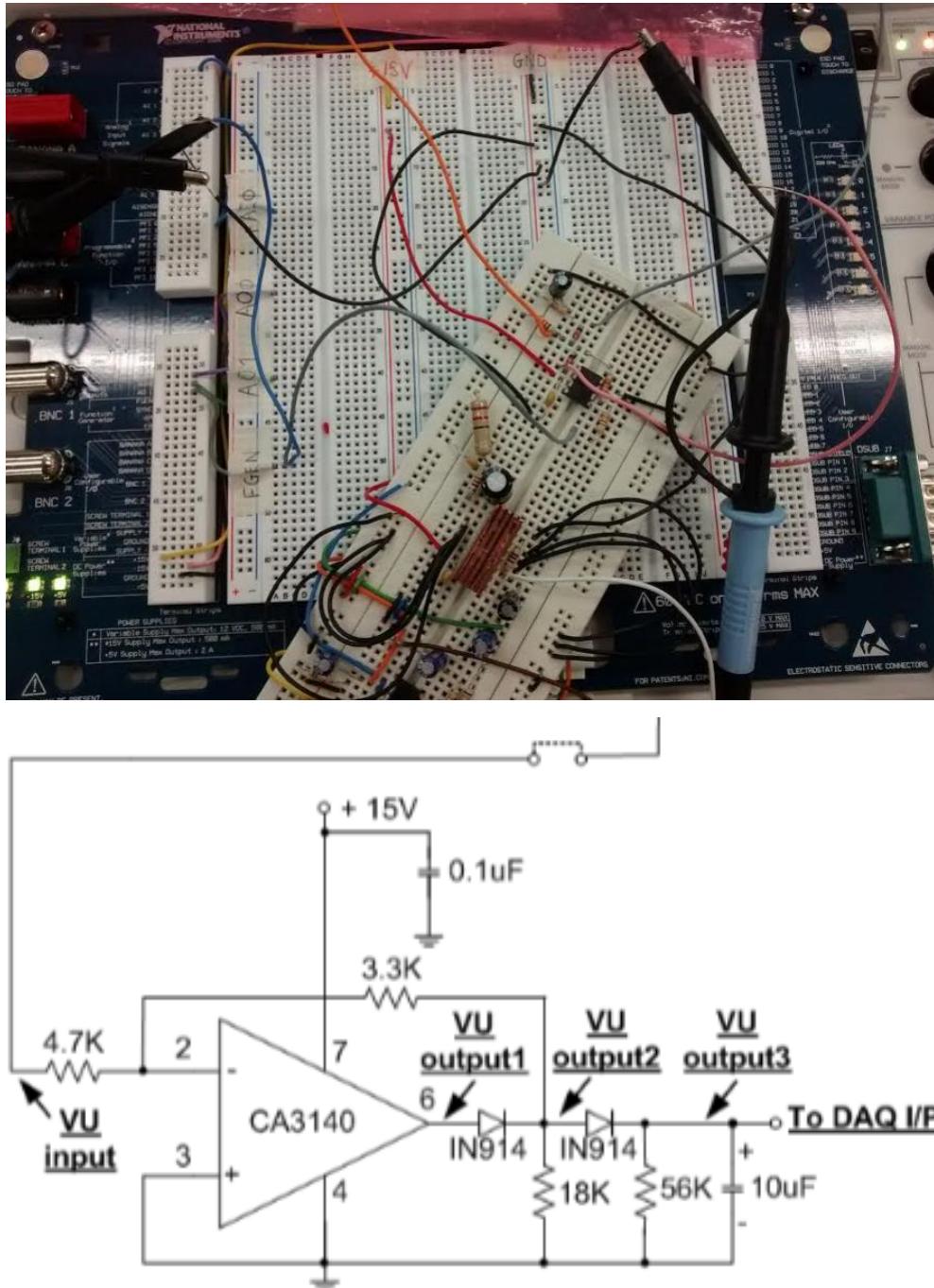


Figure 4.1 Breadboard connection and Circuit schematic for VU

4.1 Testing of the first set of value

This section is simply to show an example of configuring the function generator and oscilloscope. Initial configurations for the testing:

- 1kHz input signal frequency, Vpp=5v, in the function generator
- CH0 connected to VUinput, CH1 to VUoutput1,2,3 respectively.

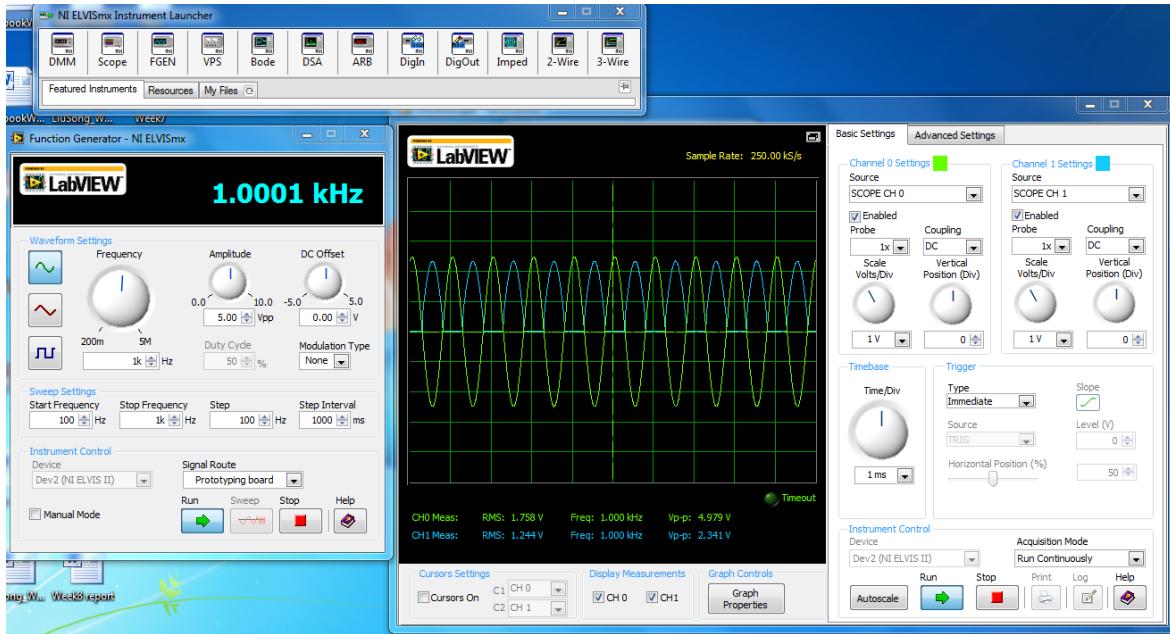


Figure 4.2 Function generator setting and oscilloscope output sample

4.2 Testing and calculate the measured gain based on my matric card number (U1122747F)

Many more tests have been carried out using the general settings in section 4.1. The VUinput used was according to my matric card number. The values used and measured gains are shown in Table 4.1:

VUinput (Vpp)	VUoutput1 (Vpk)	VUoutput2 (Vpk)	VUoutput3 (Vpk)	Measured Gain = 2 VUoutput2 / VUinput
5	2.34	1.716	0.00322	0.6864000
9.1	3.812	3.095	0.00596	0.6802198
4.51	2.162	1.543	0.0029	0.6842572

3.52	1.801	1.228	0.00226	0.6977273
2.52	1.430	0.880	0.00193	0.6984127
1.57	1.068	0.540	0.00161	0.6878981
0.54	0.66	0.196	0.00145	0.7259259
0.27	0.532	0.100	0.00129	0.7407407

Table 4.1 VU testing values and results

1.3 Plot of the measured gain VS VUinput

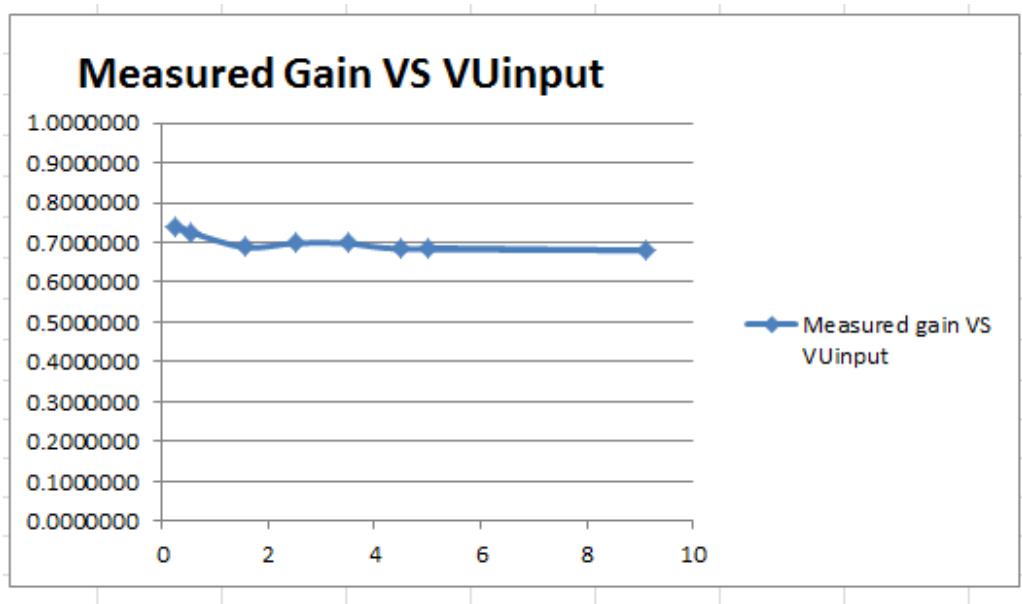


Figure 4.4 Measured Gain VS VUinput for VU meter

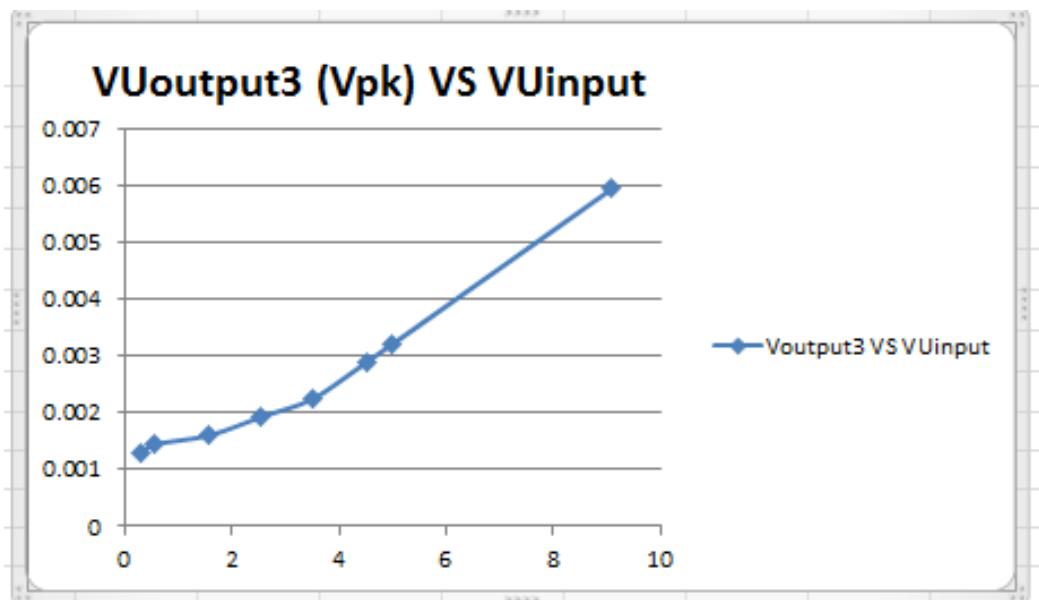


Figure 4.5 Voutput3 VS VUinput for VU meter

Additional Discussion:

Theoretical Gain = $-\frac{R_2}{R_1} = -0.7021$. From figure 4.4, it could be seen that our measured gain ranges from 0.6802198 to 0.7407407, which is very close to our theoretical value given by: $-R_2/R_1=-3.3K/4.7K=-0.702$.

Since the functionality of VU meter is the measure the output signal amplitude form the PA subsystem. From the above graph, we could conclude that the functionality of it is met and we could further see that the VUoutput 3 changes almost linearly with VUinput.

Chapter 5 Integration of VCA, PA and VU

After successfully building and testing three individual circuit blocks, namely VCA, PA and VU, it is time to integrate them into one. Before a real closed feedback path is connected, we used a manually set V_c (from DAQ O/P) for the testing of the audio output level. Both a PCB and a breadboard had been built for this week as shown in Figure 5.1:

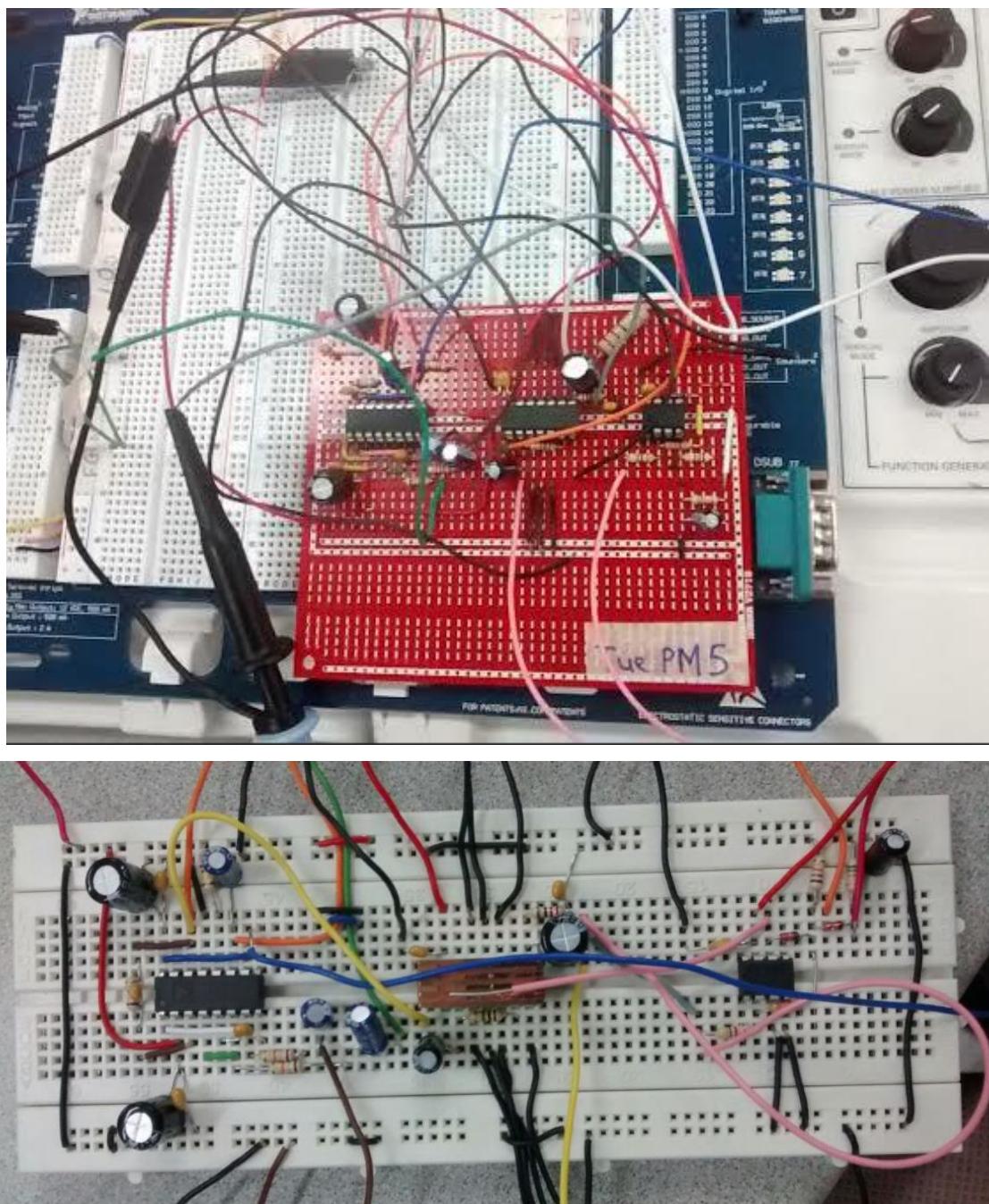


Figure 5.1 PCB and breadboard of the initially integrated system

5.1 Testing the system using values from my matric card number (U1122747F)

Sinusoidal waveform with frequency of 300Hz in FGEN was configured for a thorough testing of the system. The testing values and results are shown in table 5.1.

Audio input	Vc	Audio output	Gain (dB)
1.1	1.5	0.17	-16.2189
1.2	1	1.124	-0.5683
1.2	0.5	7.5	15.9176
1.0	0.25	13	22.27887
0.08	0	4.1	34.19388
0.14	-0.25	9.1	36.25827
0.15	-0.5	9.0	35.56303

Table 5.1 Testing values and audio outputs to test the initial integrated system

5.2 Plot Gain(dB) VS Vc

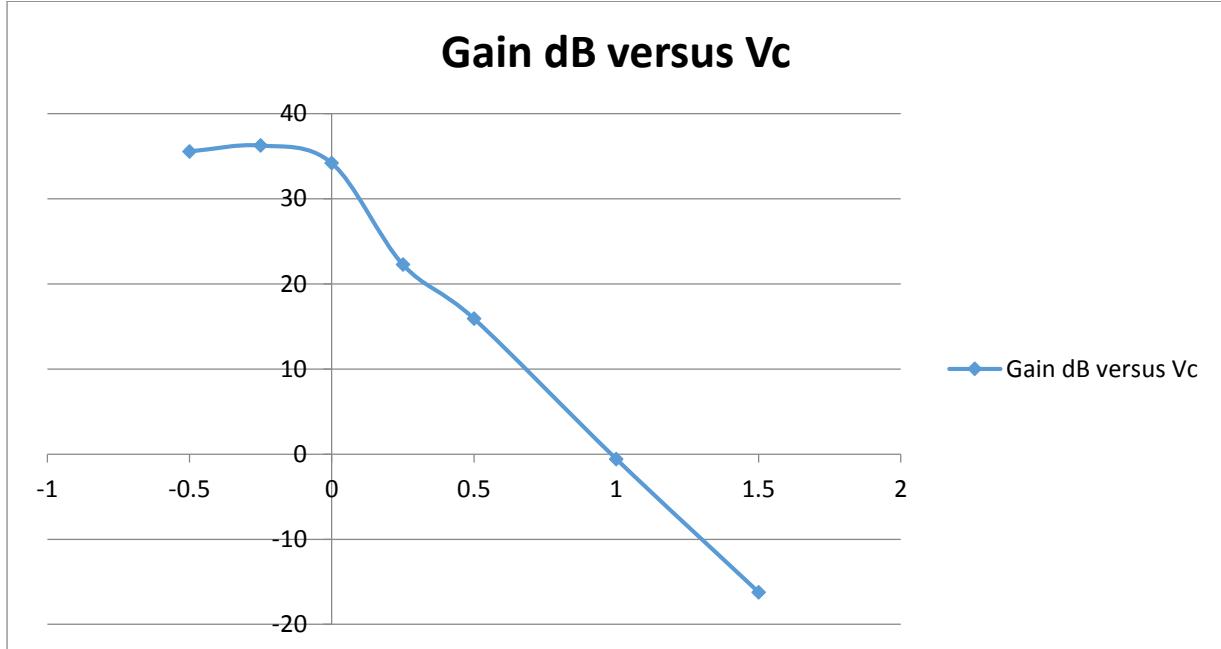


Figure 5.2 Gain VS Vc

Additional discussion:

- 1) The desired design is reasonably met. When V_c is negative, gain maintains very high at a value around 35dB. When V_c is in the positive domain, gain becomes smaller and decreases almost linearly. When V_c reduces to around 1V, gain turns negative and volume also reduce.
- 2) When frequency increases above 100kHz, the output is distorted a lot even though it can still be distinguished as a periodic function.

Chapter 6: Manual Volume Control

Before adding an automatic feedback control circuit, it is necessary to test the data acquisition circuit setup. Hence a manual value control signal V_c is applied to VCA by the operator manually to observe the output of the system. Notice that the manual control should work in accordance with the VCA(actuator) and VU(sensor). At this stage, the entire system is still an open loop circuit. According to the block diagram of the open loop system as shown in Figure 6.1, the breadboard is connected as shown in figure 6.2. Notice that the resistor was replaced by a speaker.

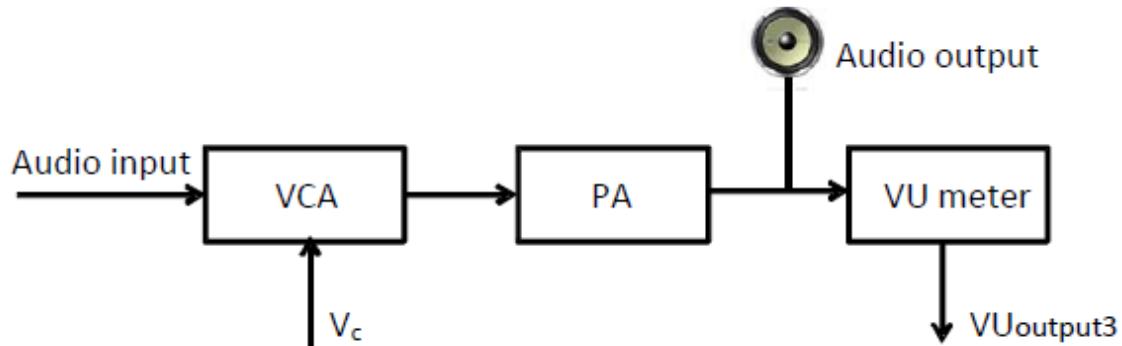


Figure 6.1 Block diagram of the open loop system

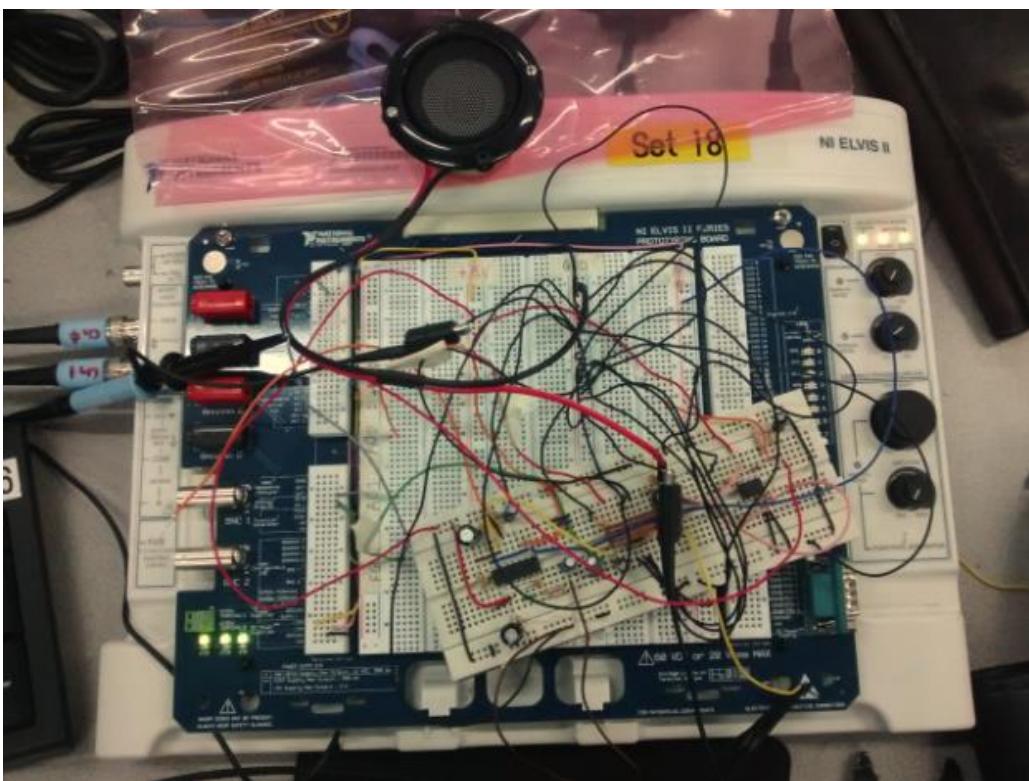


Figure 6.2 Bread connection of the open loop circuit

The manual control circuitry is drawn in LabView and its block diagram is shown in Figure 6.3.

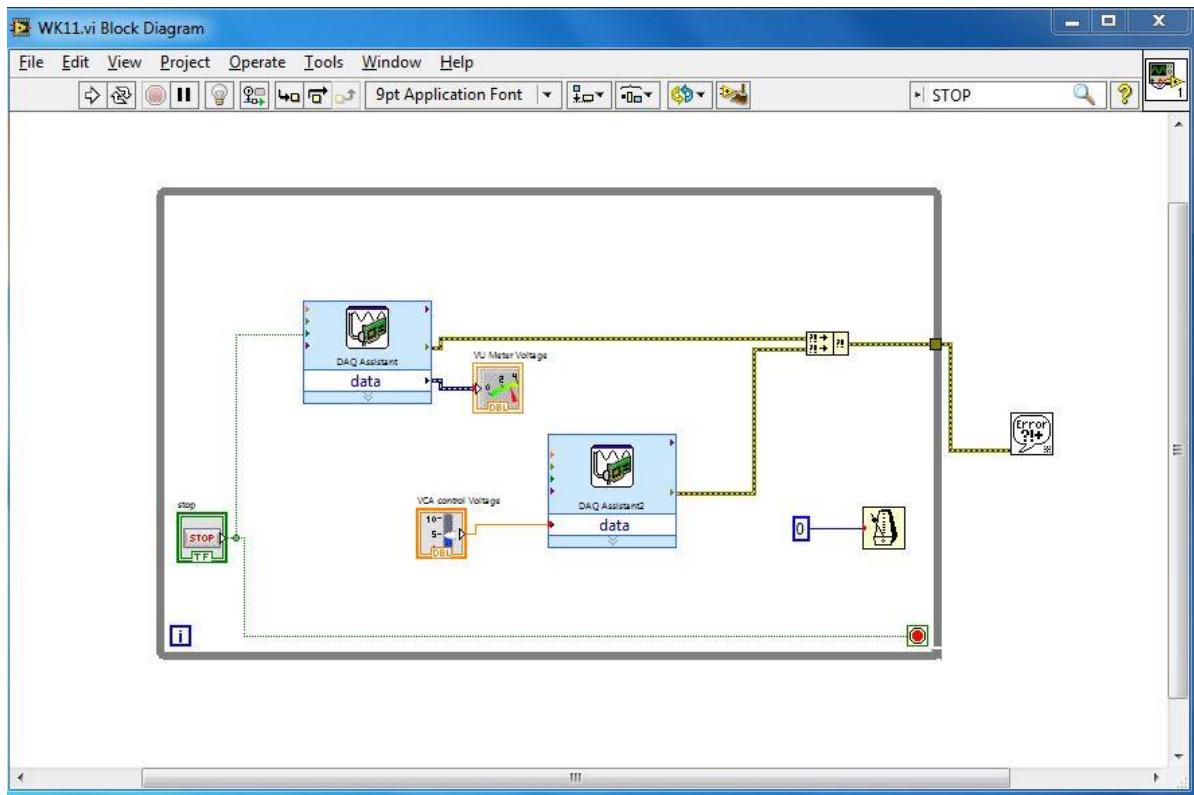
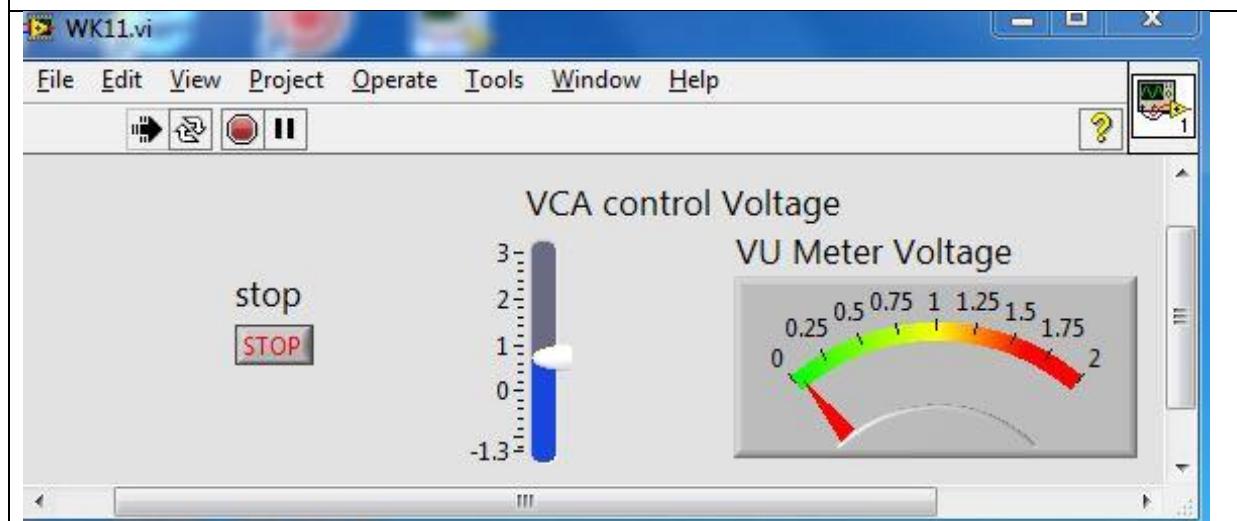
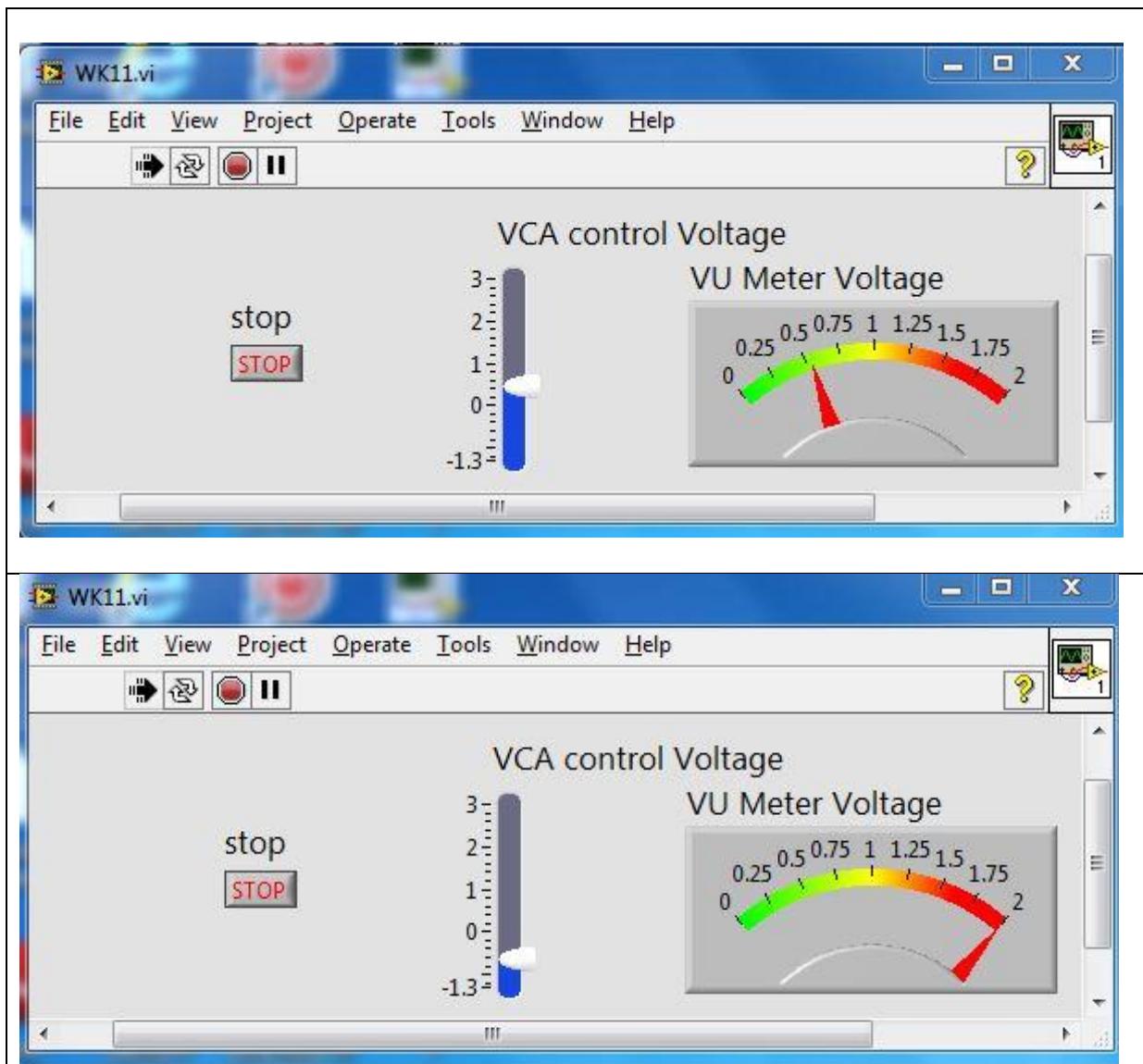


Figure 6.3 LabView block diagram for the open loop system

Different values of VCA control voltages have been tested for the circuits and the front panel displays are shown in table 6.1:

Table 6.1 Front panel displays with different VCA control voltage





Additional discussion:

We observed that when the VU meter display changes with VCA control voltage. In addition, as the control voltage V_c goes up, the VU display goes down. This observation is expected because V_c is a negative feedback signal.

Also as we changed the input signal frequency, we could hear the speaker generating higher tones with higher frequencies.

Chapter 7 Automatic Volume Control (complete system)

At the final stage, we implemented a close loop circuitry to automate the process of volume control. The block diagram of the entire system is shown in figure 7.1. The VU acts like a sensor for the audio output level, the VCA acts as the actuator for the audio input amplification. The close loop circuit feedback the signal from the VU meter to the VCA, and it is developed in LabVIEW/ELVIS.

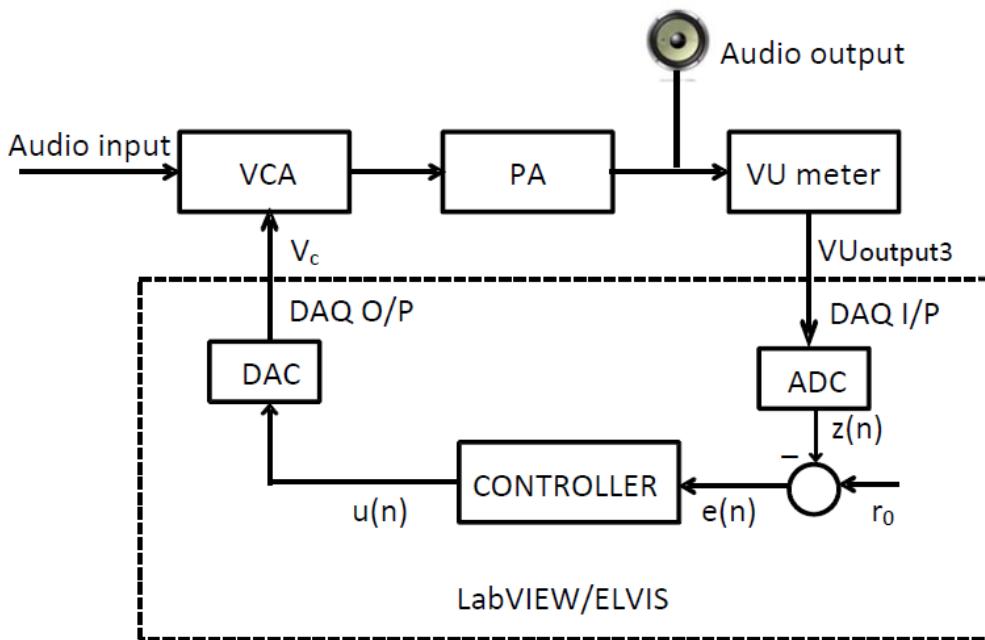


Figure 7.1 Block diagram for the closed loop system

The feedback circuit's working mechanism is shown below. When the VU meter output is bigger than the setpoint value, it will be reduced by a step size until it equals to the setpoint. When the VU meter output is smaller than the setpoint value, it will be enlarged by a step size until it equals to the setpoint.

Step-Up-Down Controller:

$$u(n) = \begin{cases} u(n-1) + \Delta, & e(n) > 0 \\ u(n-1) - \Delta, & e(n) < 0 \end{cases}$$

$$e(n) = r_0 - z(n)$$

where

Δ is the controller parameter variable (step size),

$u(n)$ is the actuator control voltage for VCA,

$z(n)$ is the VU meter envelope detector output sensor value

r_0 is the setpoint value.

The bread is connected to the NI ELVIS II as in figure 7.2, and the LabView block diagram is drawn as in figure 7.3.

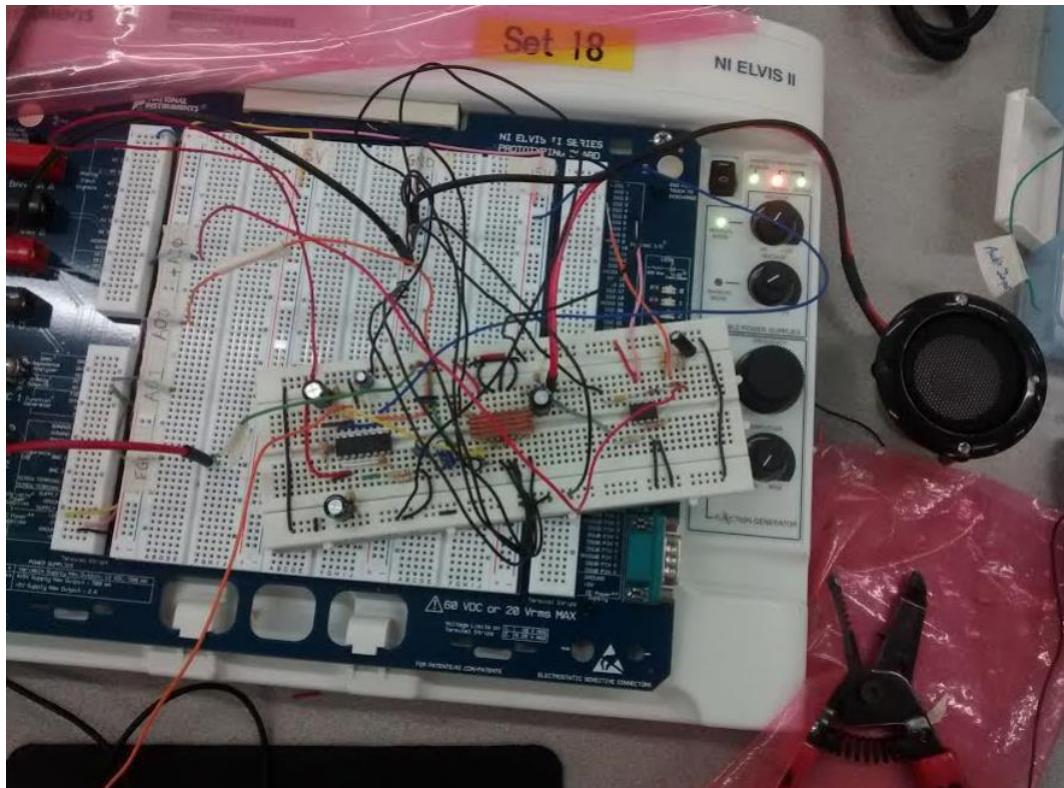


Figure 7.2 Breadboard connection for the closed loop system

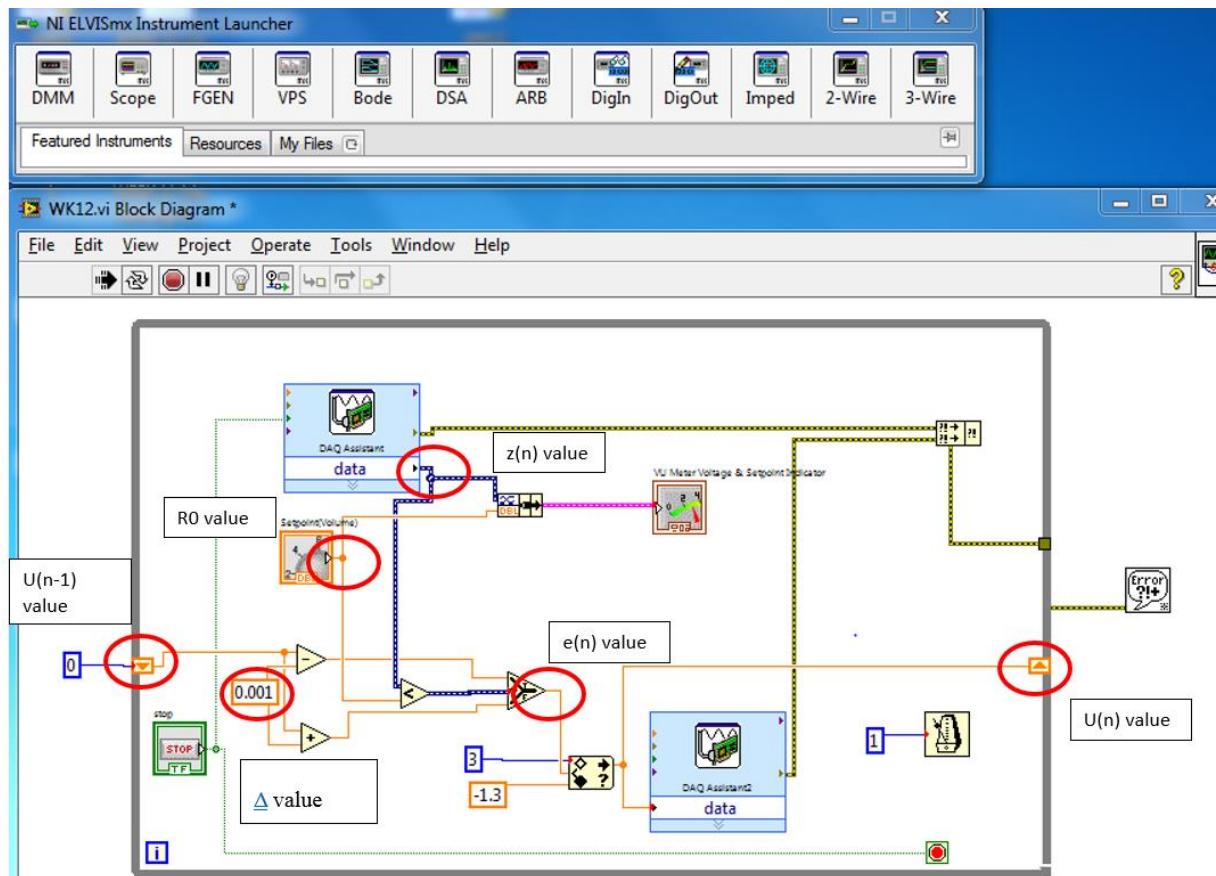


Figure 7.3 LabView block diagram for the closed loop system

The front panel is shown in figure 7.4. The RED needle indicates the actual or real-time output value from the VU meter. The black needle points to the value set by the setpoint knob.

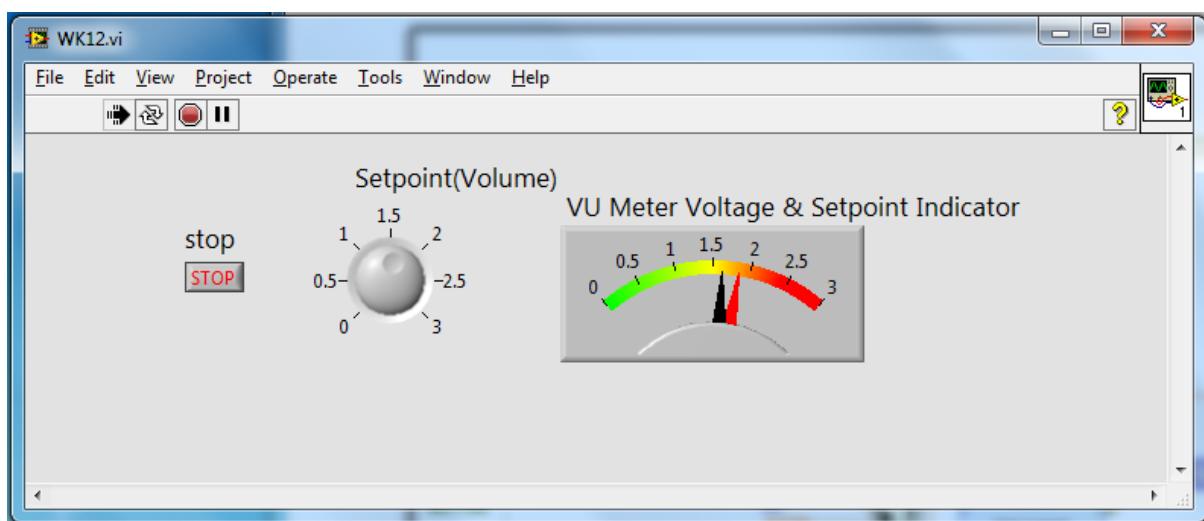
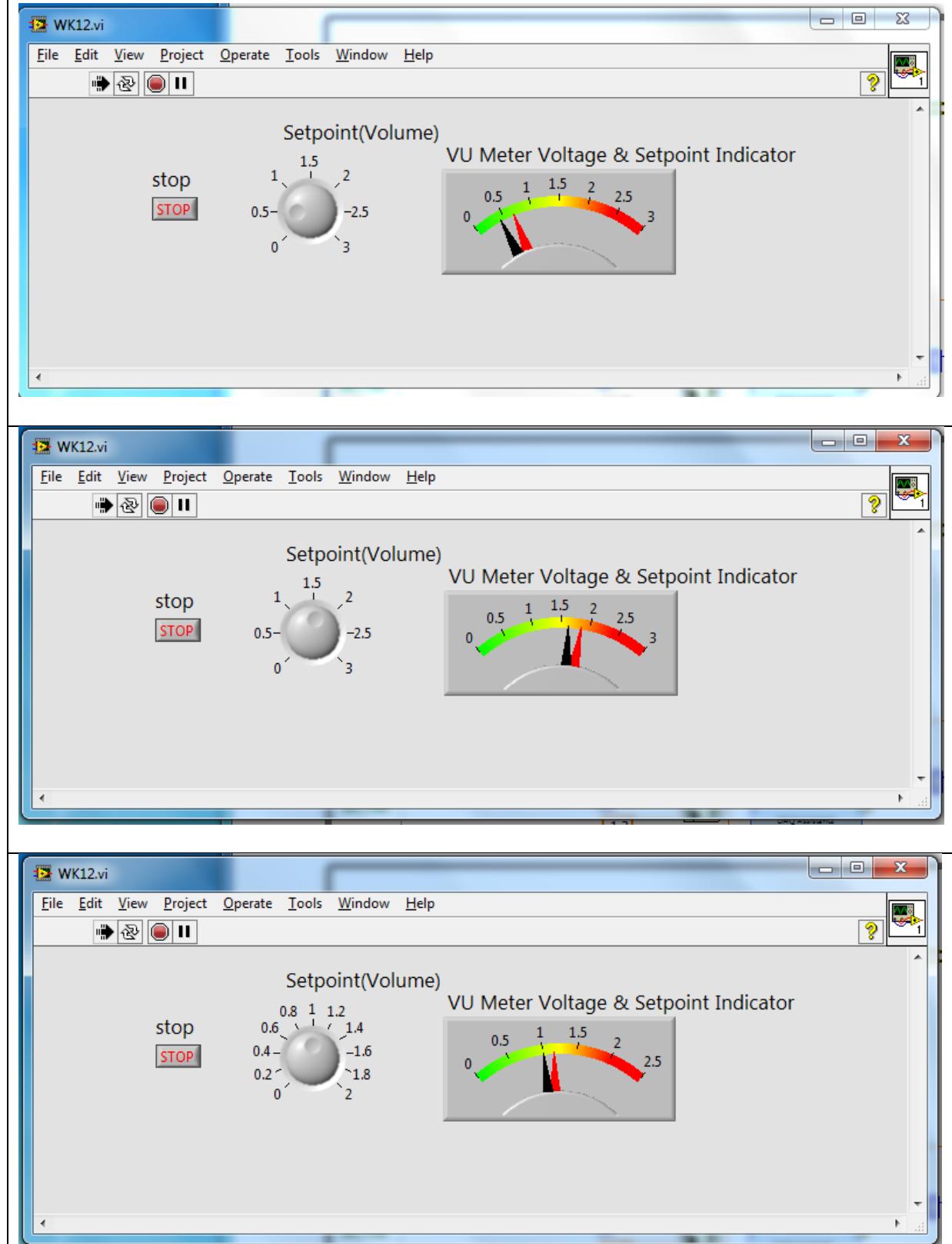


Figure 7.4 front panel of the closed loop system

Next, the system are tested while changing the setpoint value, the results are shown in table 7.1 below.

Table 7.1 The front panel display while changing the setpoint value



Additional discussion:

1. In the idea case, the black needle should overlap with the red needle, meaning that the volume controller should output a constant output audio level. However, there is a certain “response time” of the system. Hence we observed that the red needle oscillate around the black needle within a small range when the audio input changes abruptly, but will get close to the black needle swiftly. The “response time” could be further improved by increasing the step size delta (controller parameter variable). However increasing the delta would decrease the system performance because the step size is not small enough for a precise fine tune of the audio signal.
2. When testing using a speaker and computer audio output, we observed that our system was generally successfully realised the function of controlling the final speaker volume to a fixed value set by the “setpoint”. Further testing is done by inputting a music signal from a PC, it was also observed that the red indicator oscillates around the black within a reasonable range.

Conclusion

This project aims to develop an automatic volume control system as a way to prepare students for the EEE design and innovation projects. The first part of the system is a voltage controlled amplifier circuit, which receives audio input signal and plays the role of an actuator, whose gain are set by a feedback signal V_c . The second part is an power amplifier which is the central item that provides most of the gain and power for the audio output through a speaker. The final part is a volume unit meter used to sense the output signal level and feedback to the control circuit.

In developing the entire system, we have adopted a divide-and-conquer approach. The entire system is divided into three subsystems, namely the voltage controlled amplifier, the power amplifier and the volume unit meter. Each subsystem was implemented and tested individually before integrated together. After the initial integration was done and before adding a closed loop circuit as a final step, we tested the system using a manual feedback signal V_c . Hence we avoided a lot practical problems and the need to debug the entire system from head to toe.

The overall the performance of our system is satisfactory from a customer's point of view. Audio music input from a PC was used to replace to function generator signal, and the sound quality and volume control function was quite impressive. Hence we conclude that we have successfully finished the project.

Recommendations for next batches

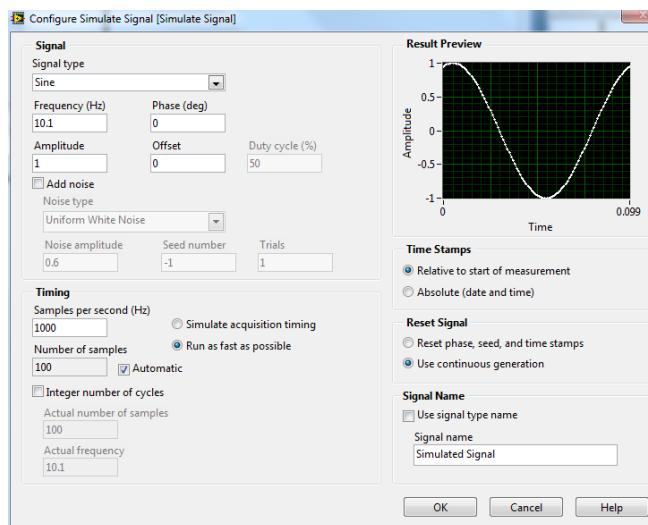
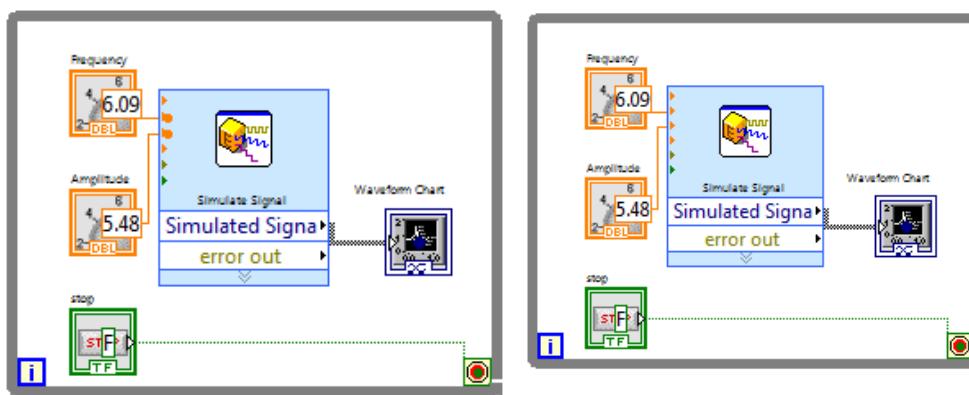
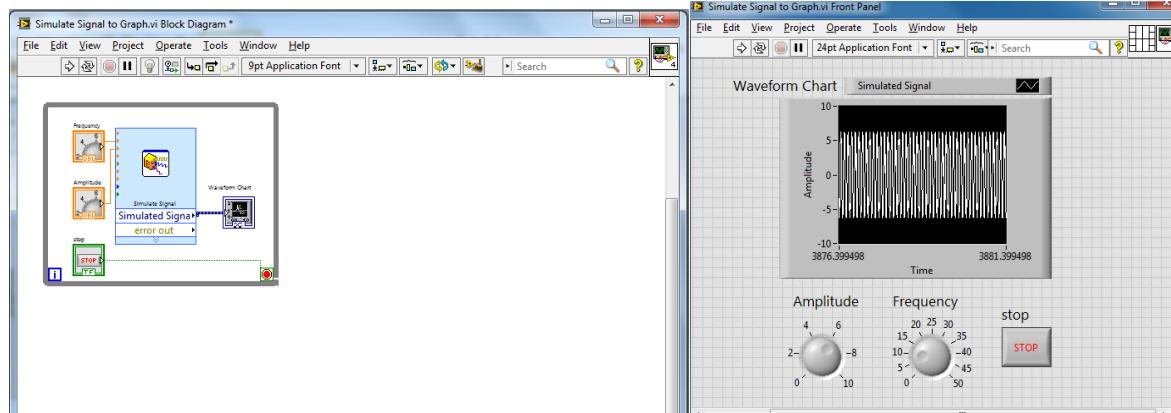
1. Future batches of students are advised to have an overall picture of the entire system before rushing to complete each subsystem. Having a clear understanding of the underlying mechanism would be very helpful in preparing the weekly log and debugging.
2. Many noises when using the breadboard comes from loose connections of wires. Extra attention should be paid into managing the wires in a tidy manner.
3. Double check your PCB connections before rushing to solder them. Debugging a PCB could be very troublesome and time consuming.

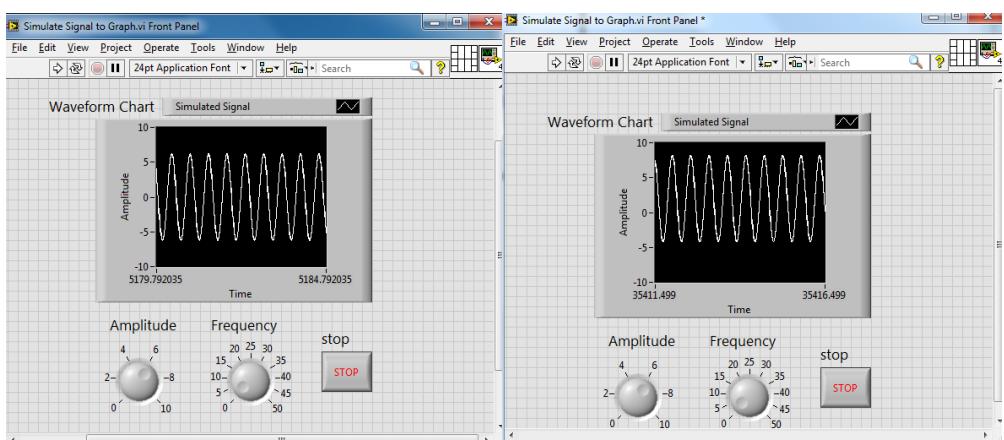
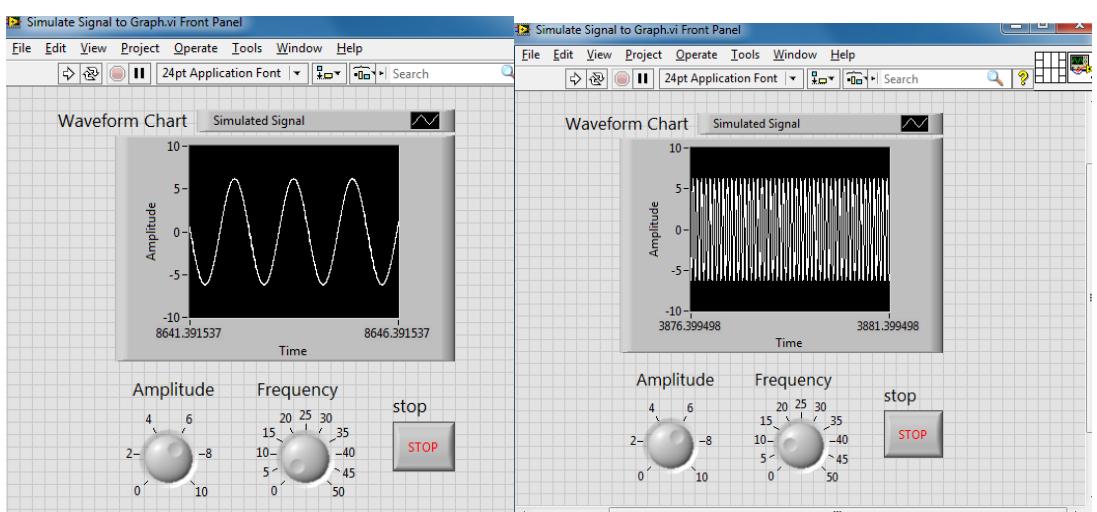
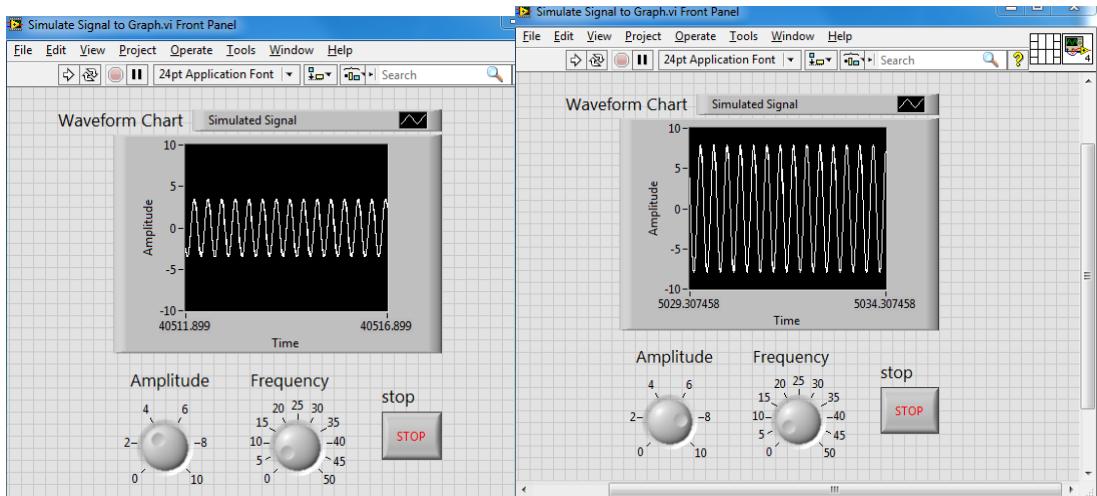
References

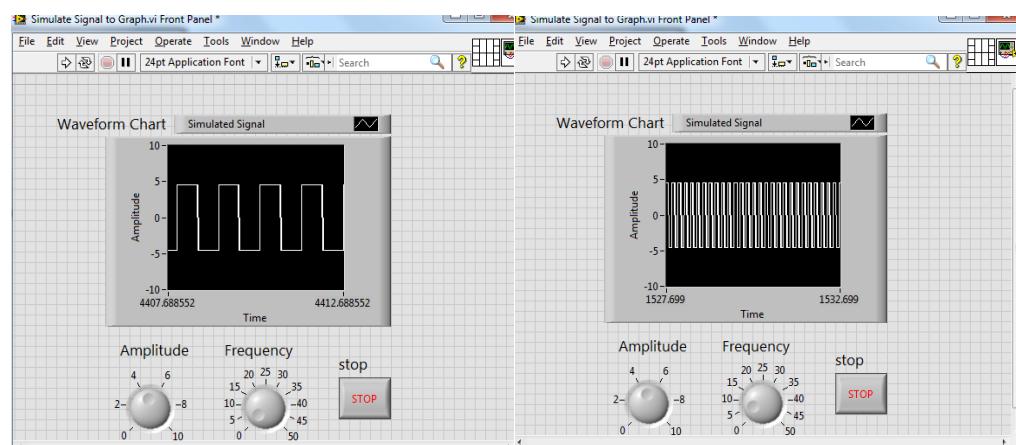
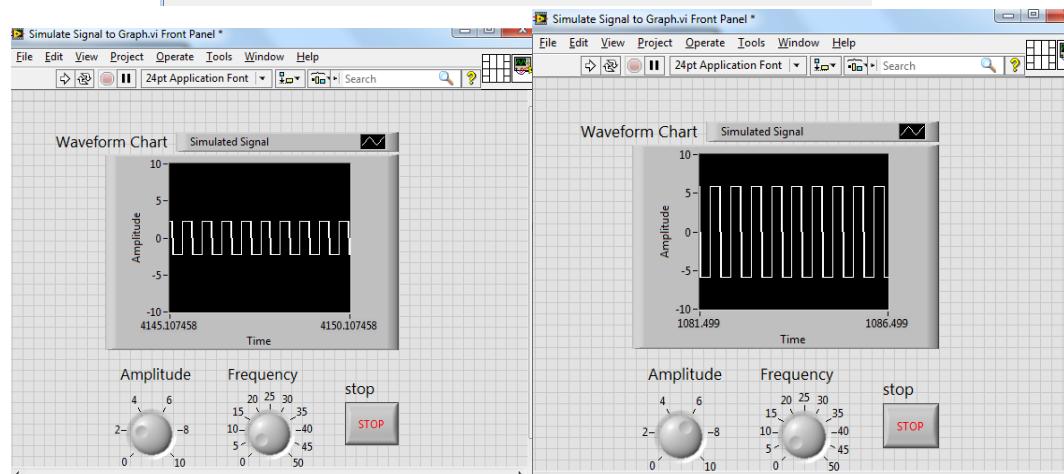
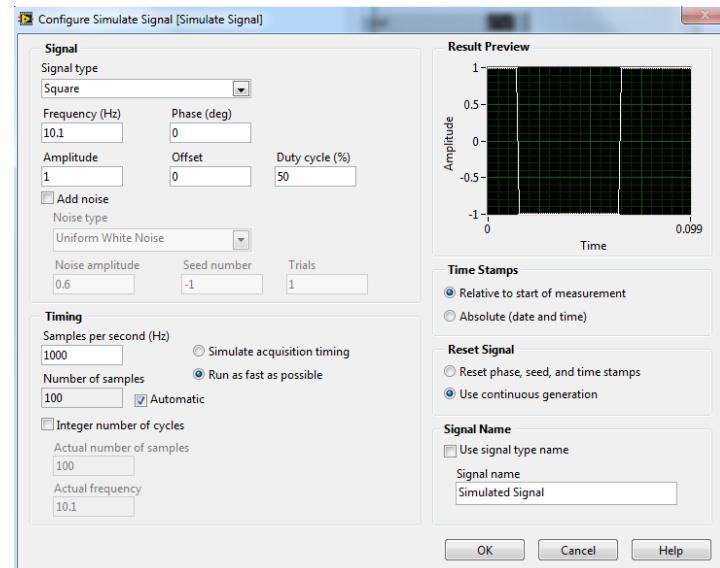
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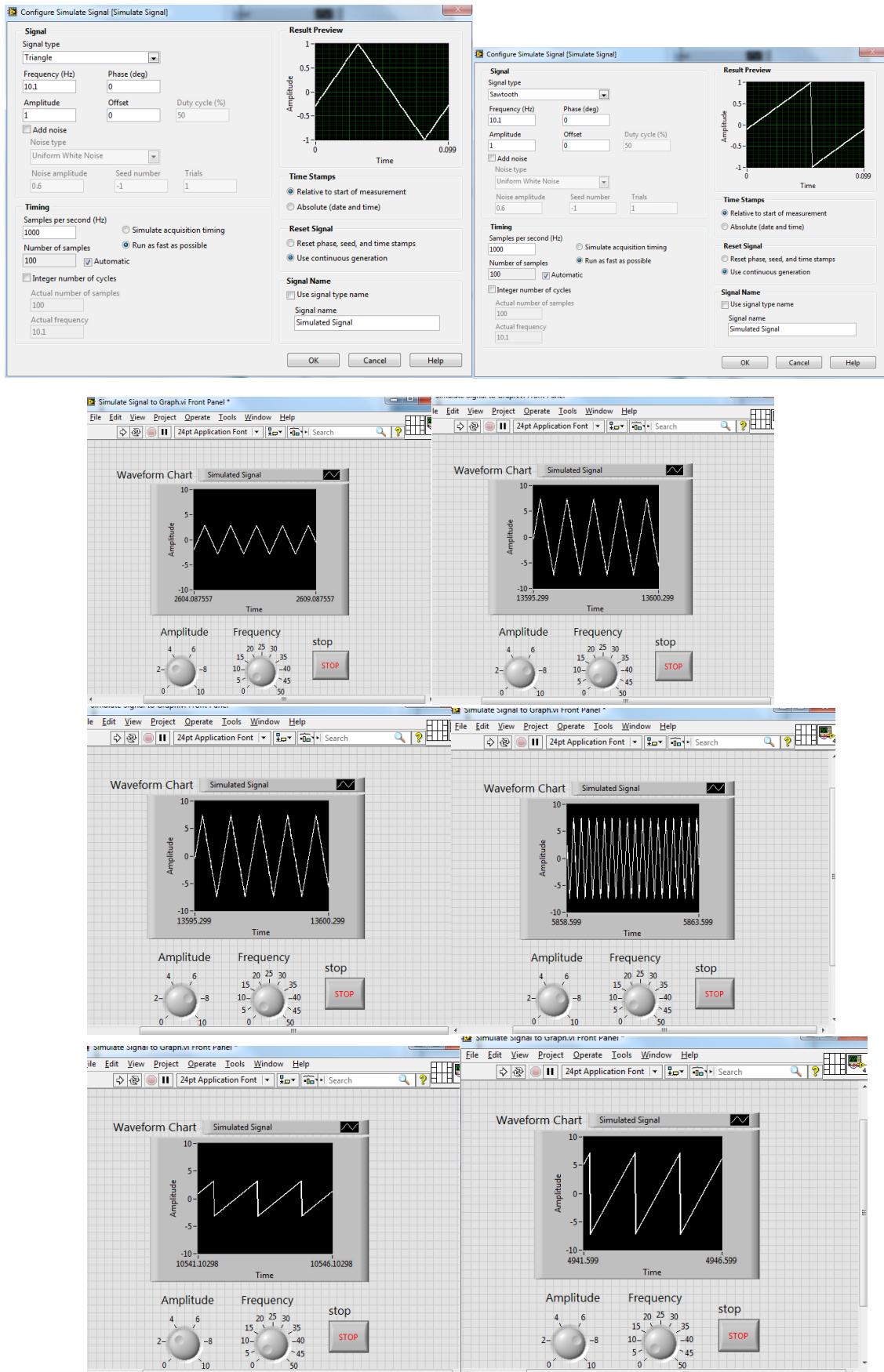
Appendix

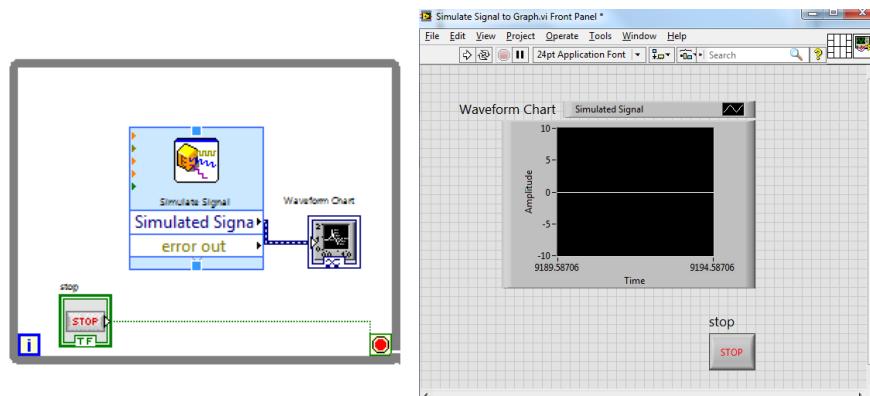
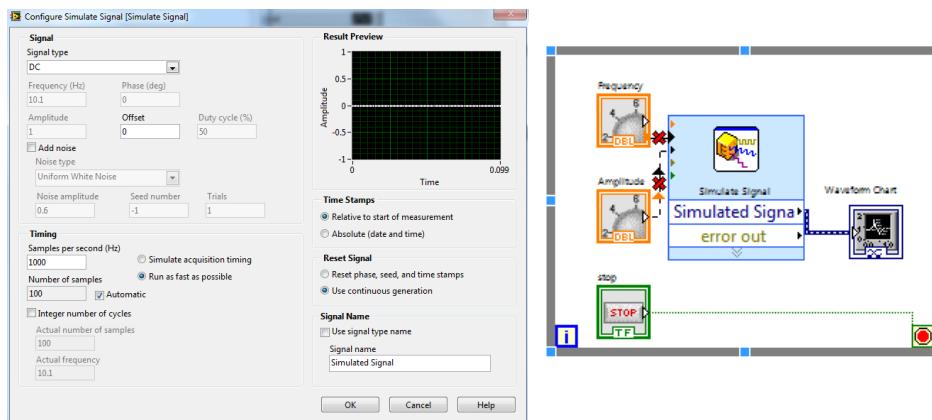
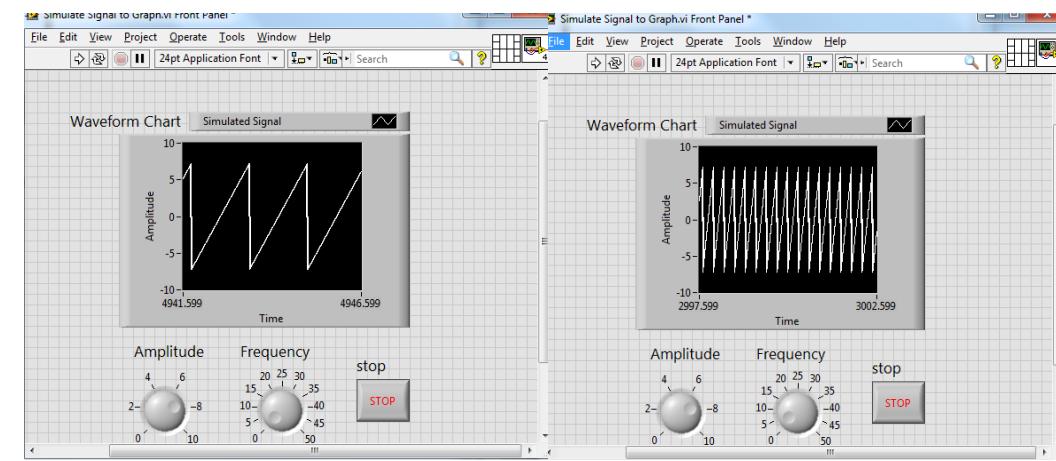
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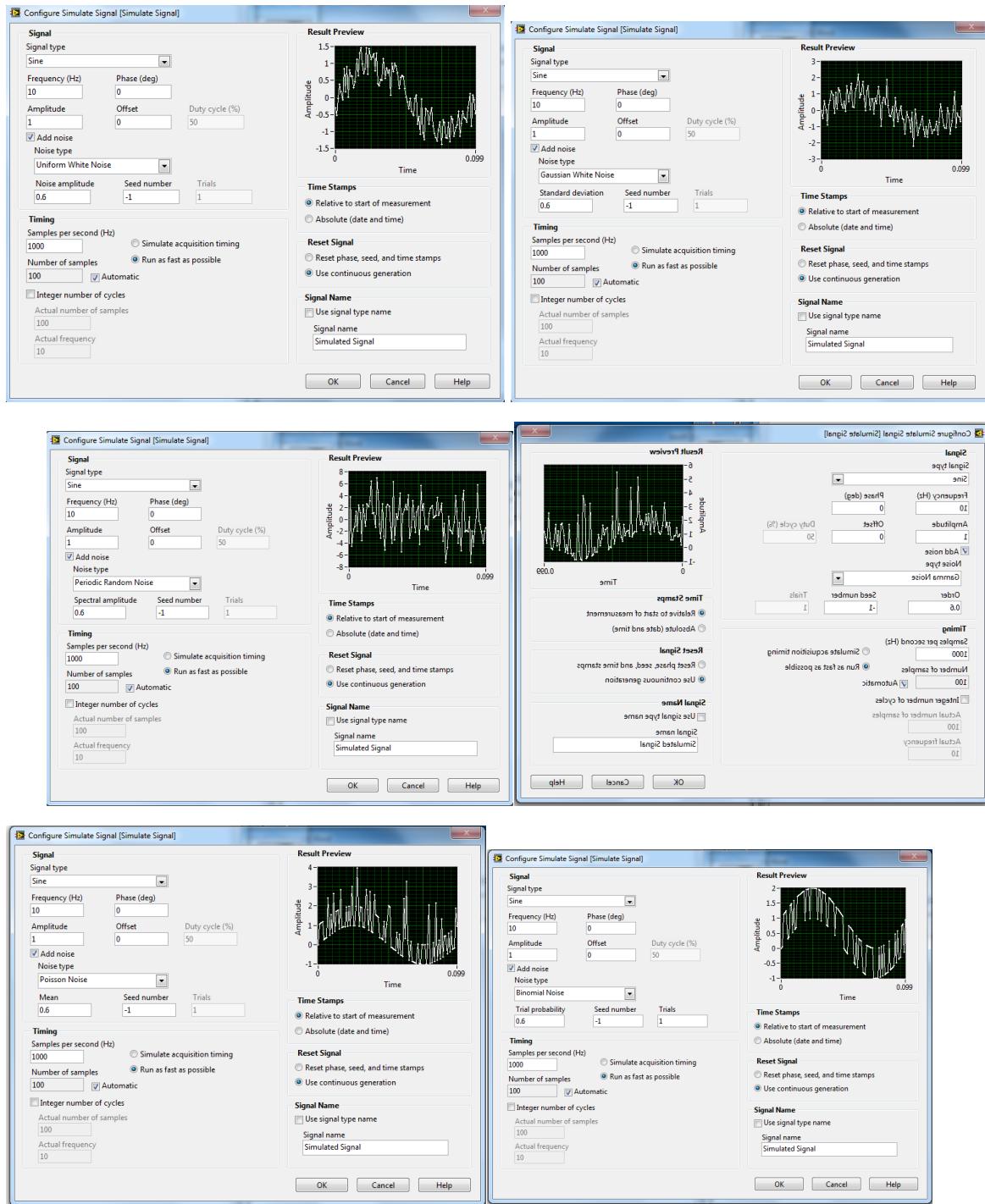


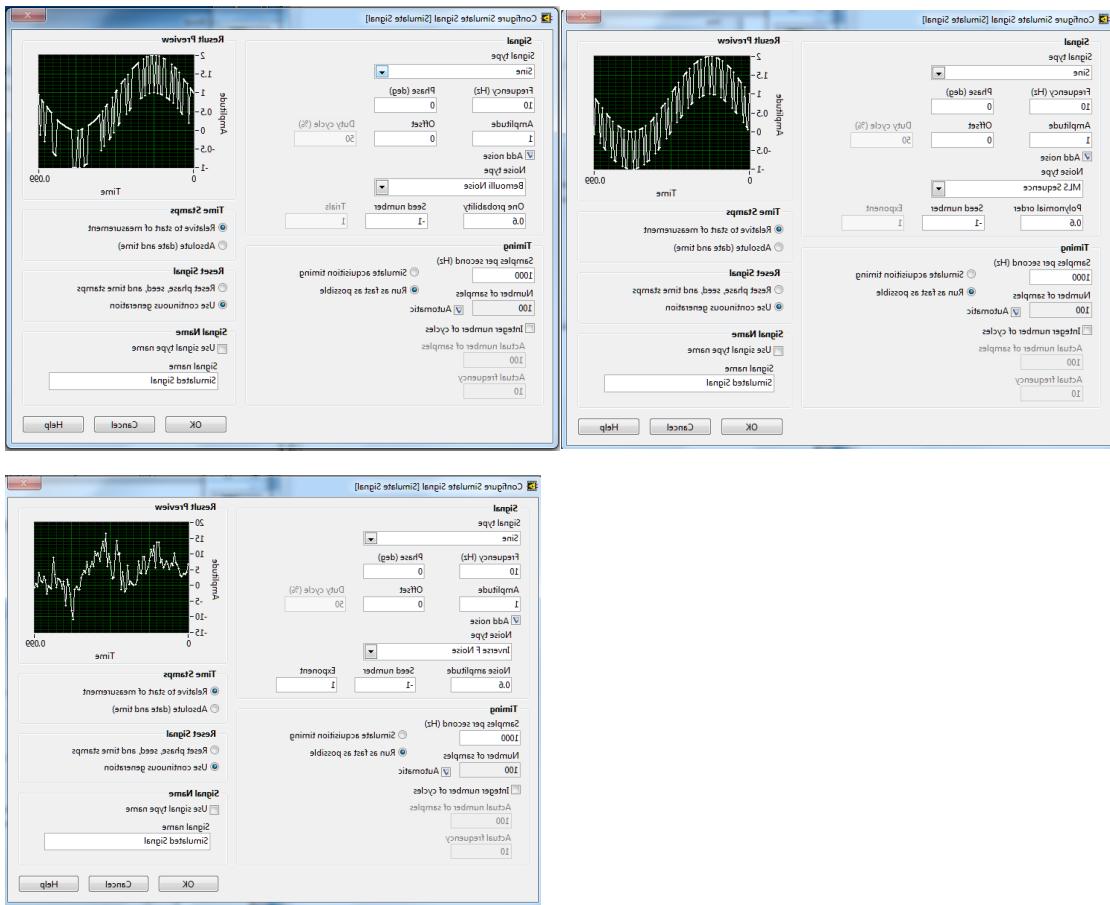




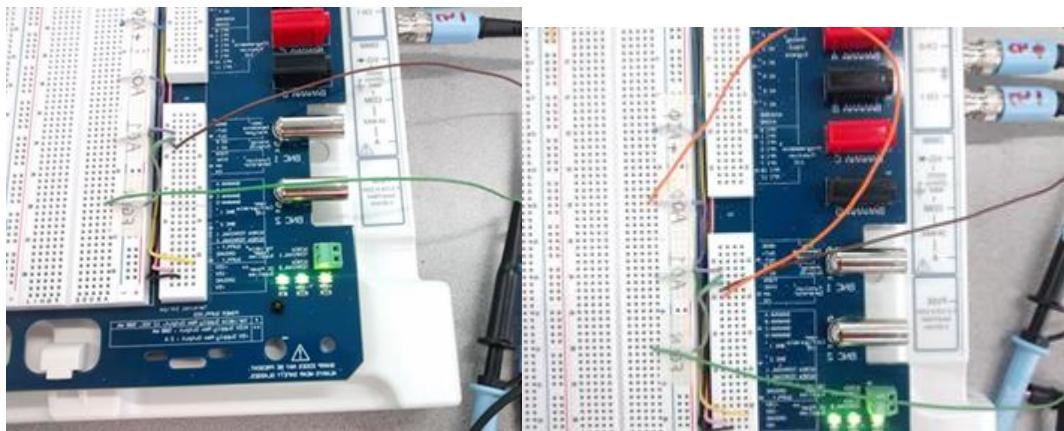


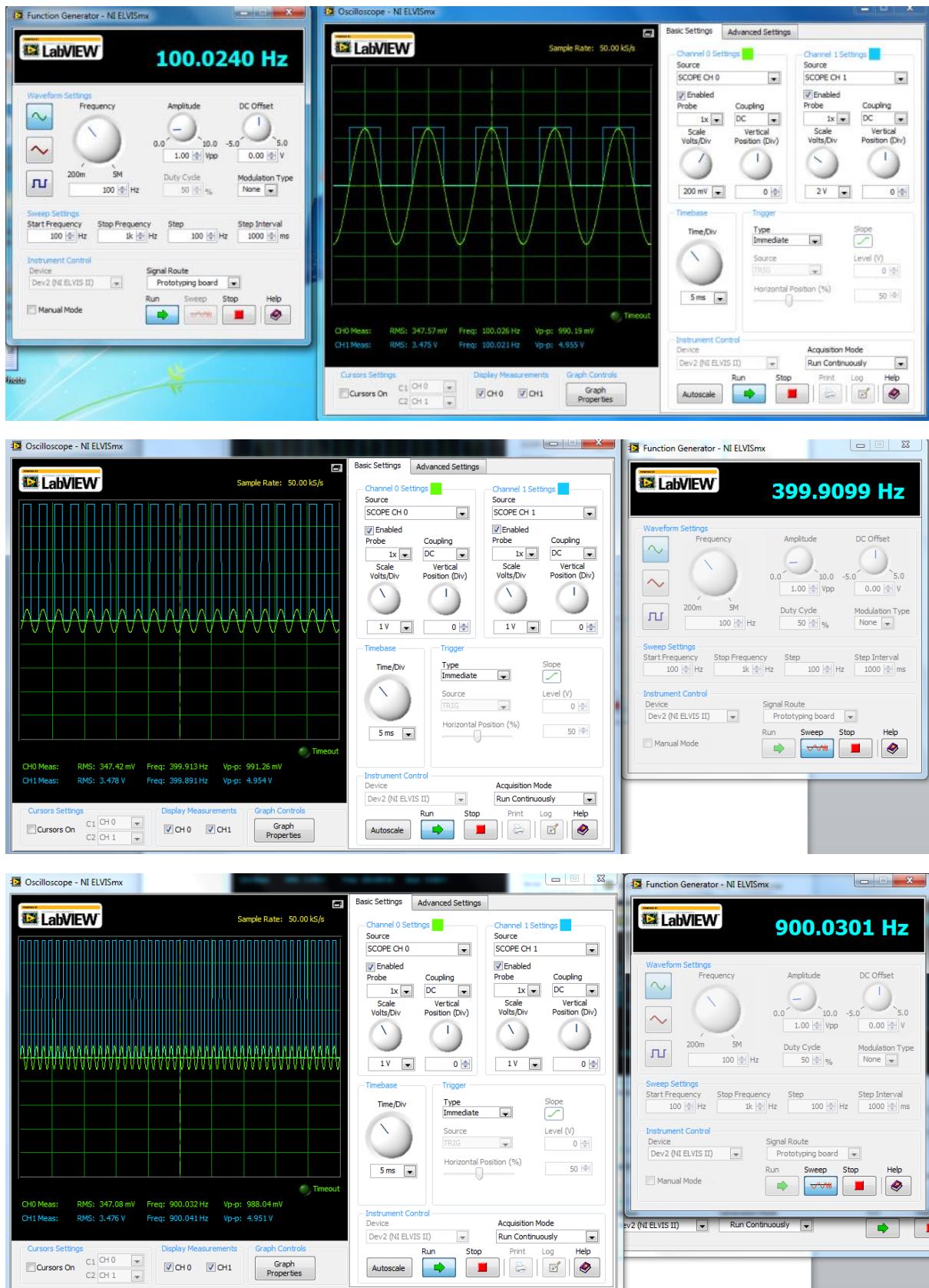


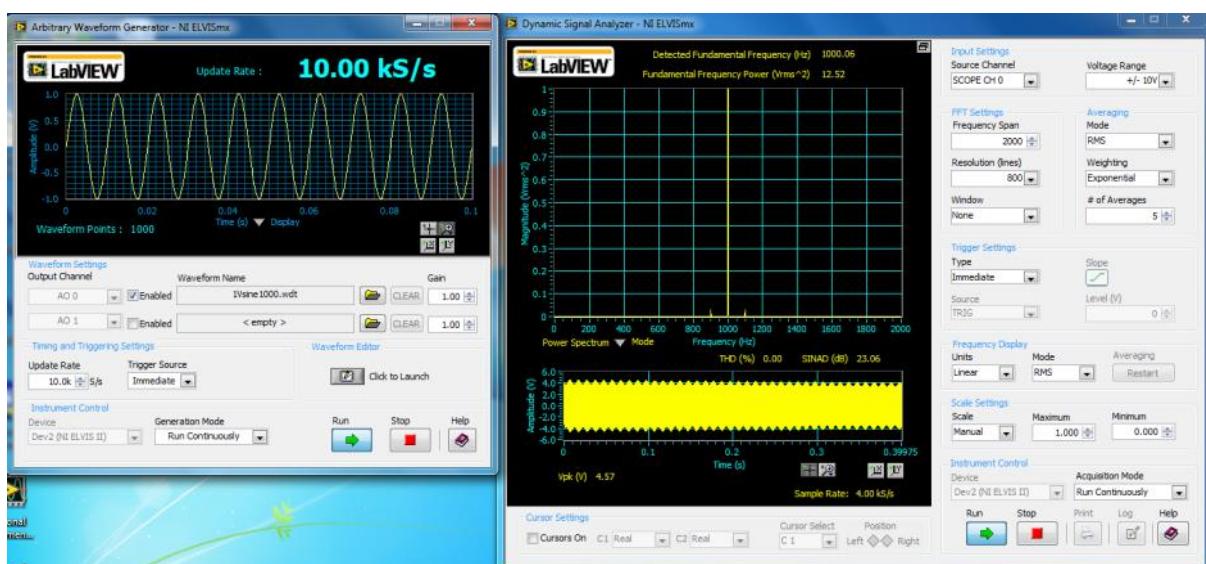
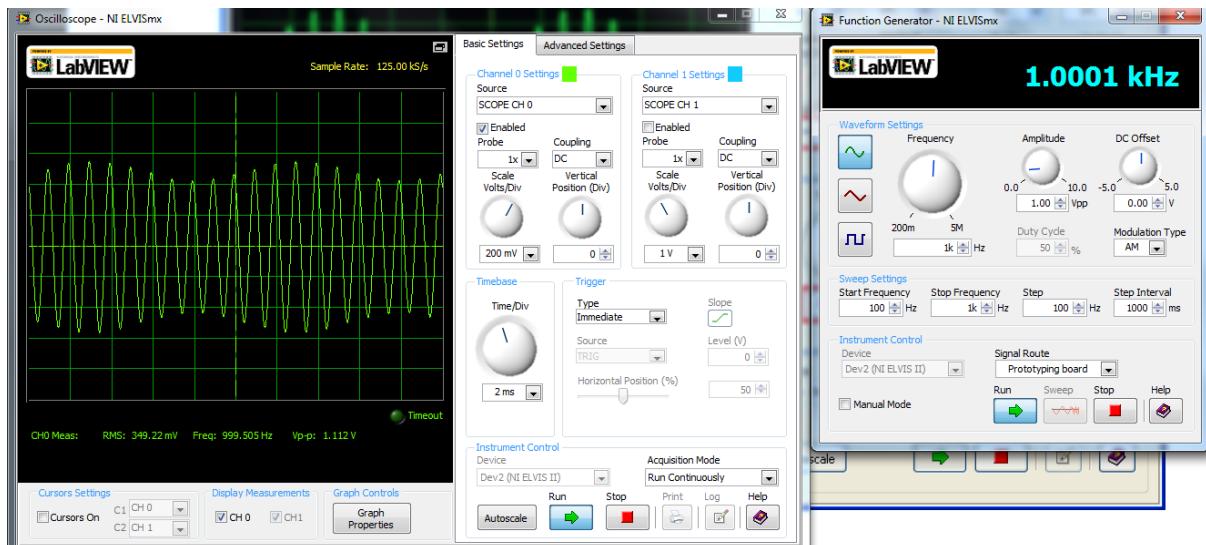


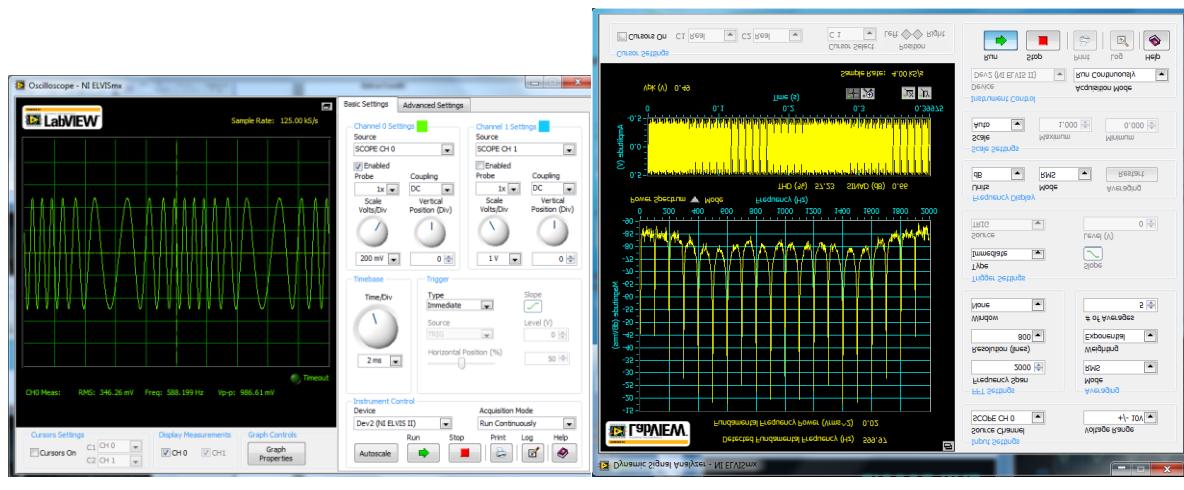
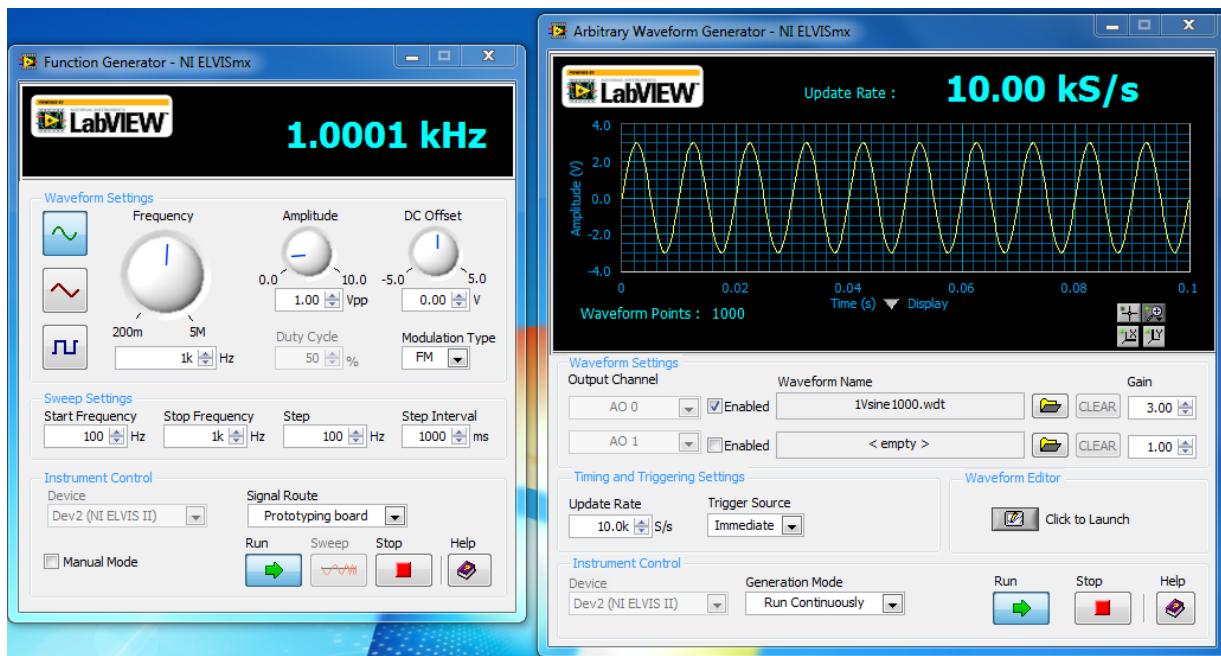


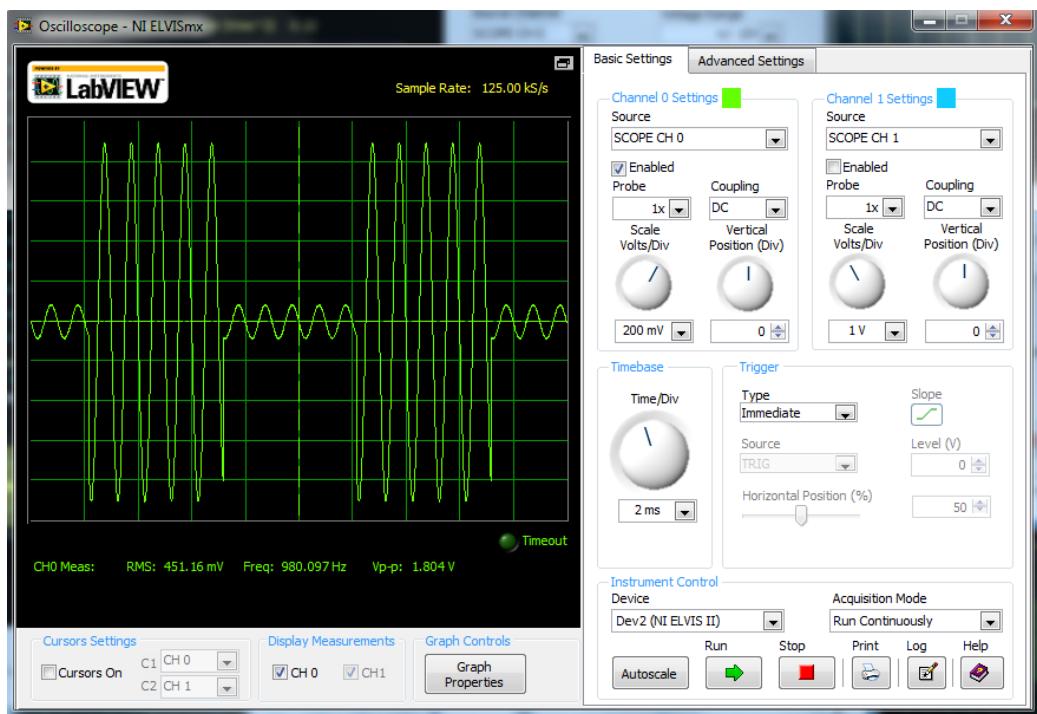
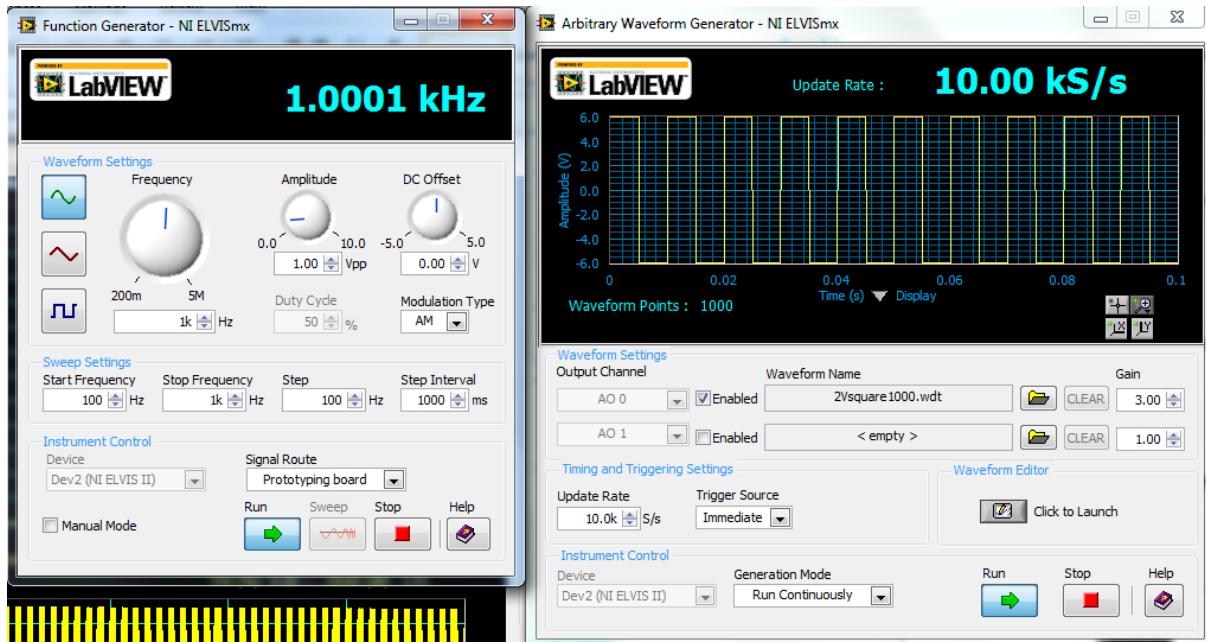
Week 4

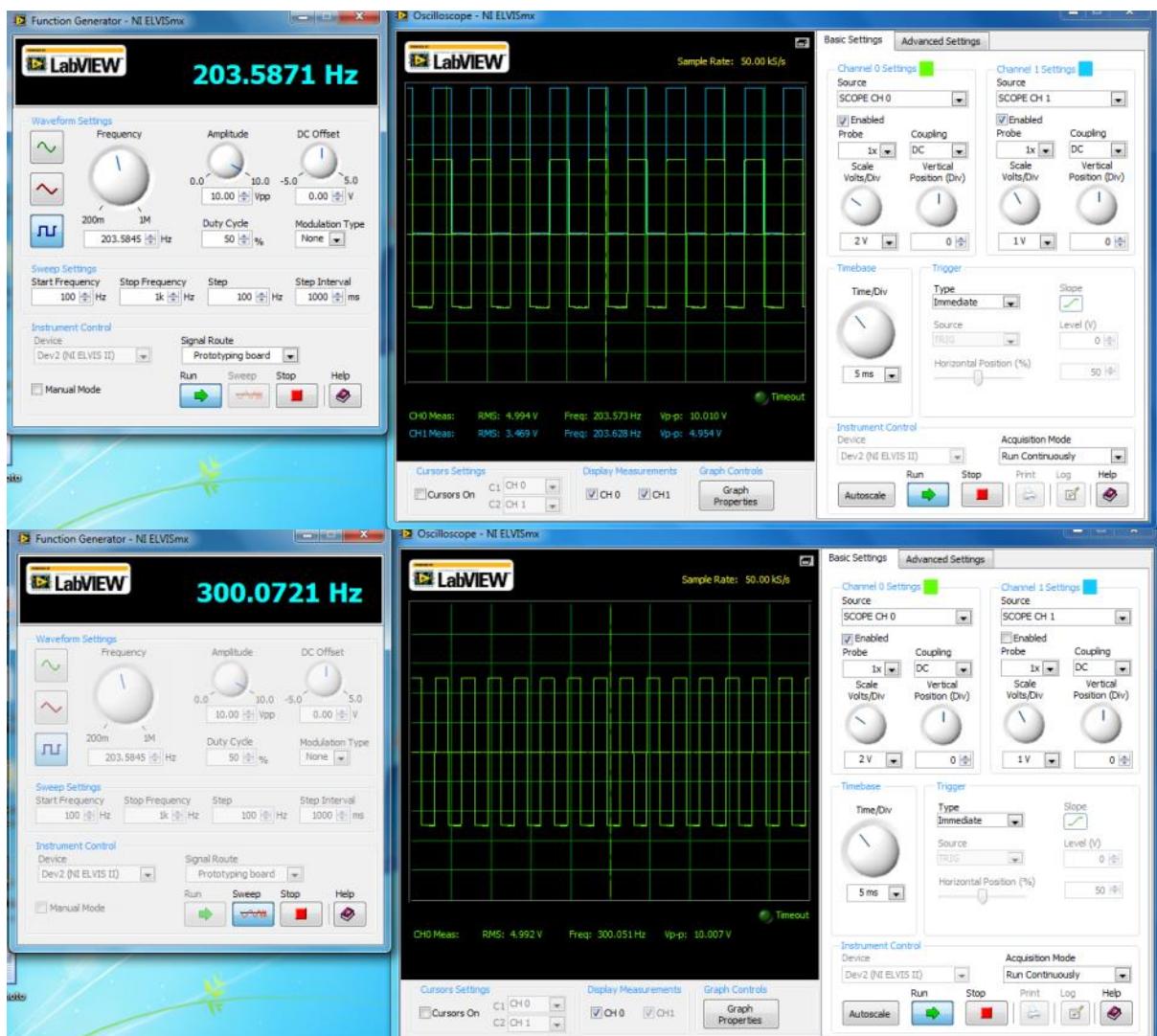


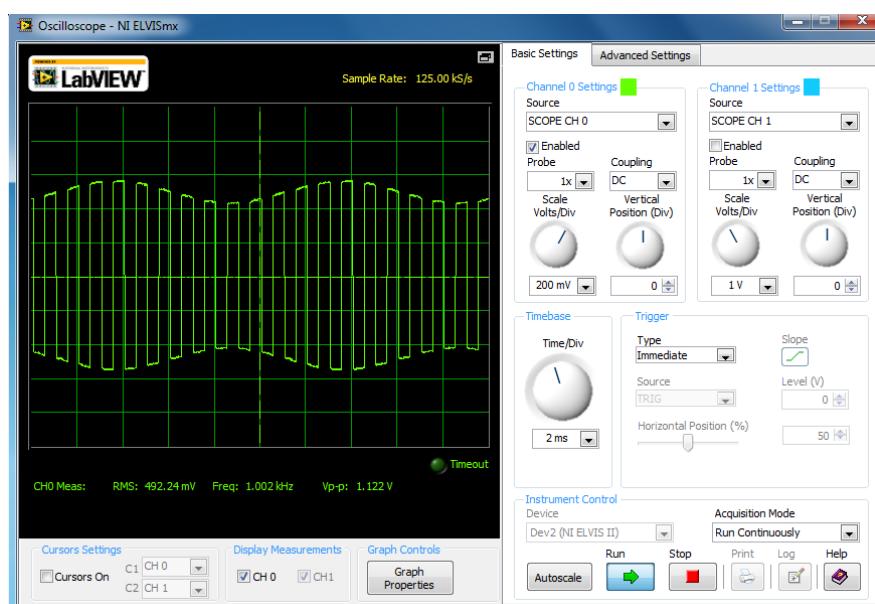
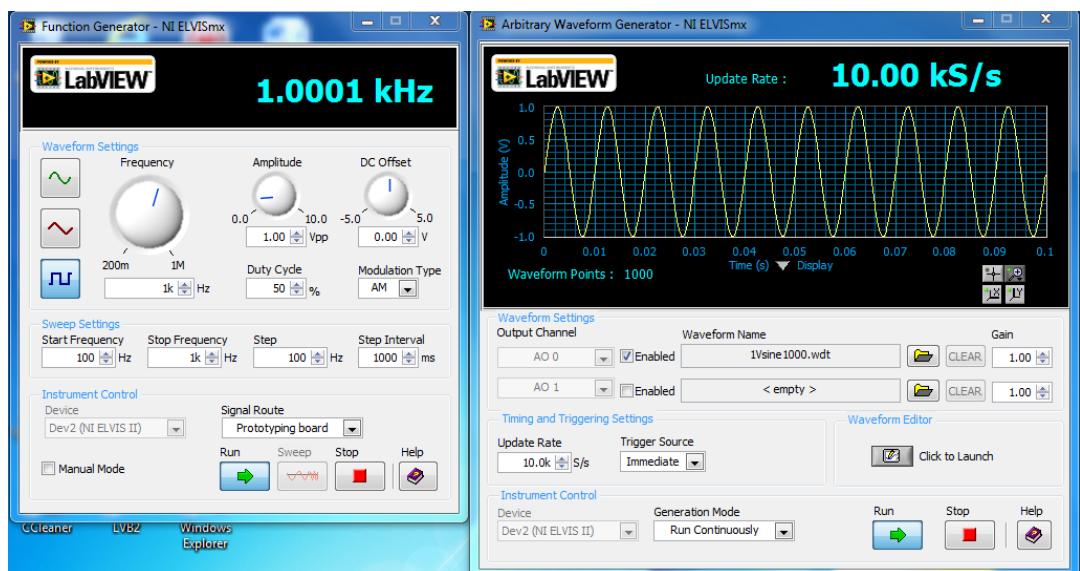
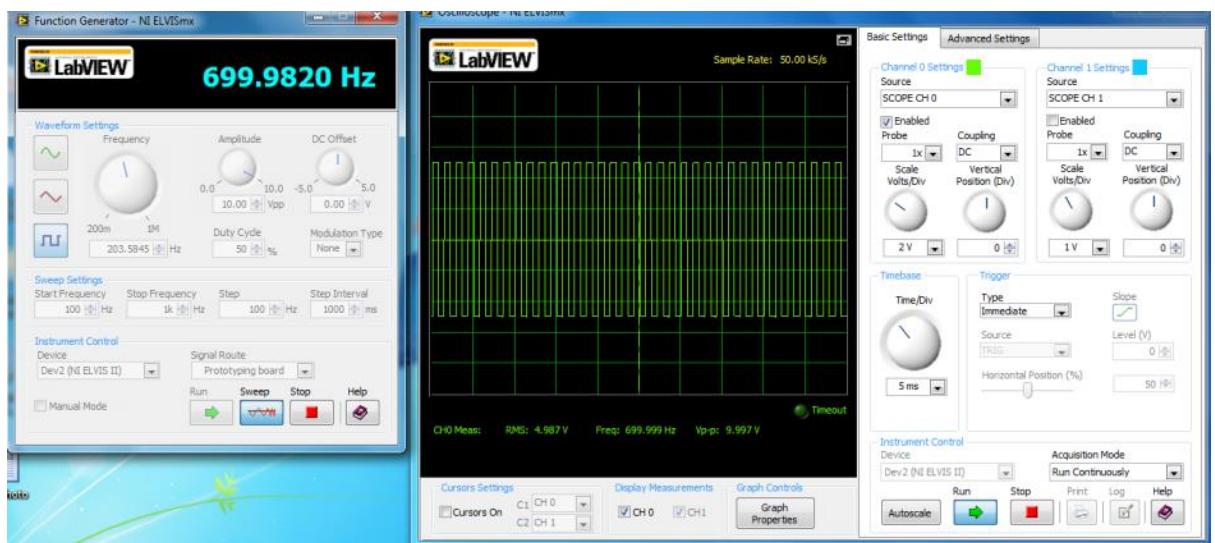


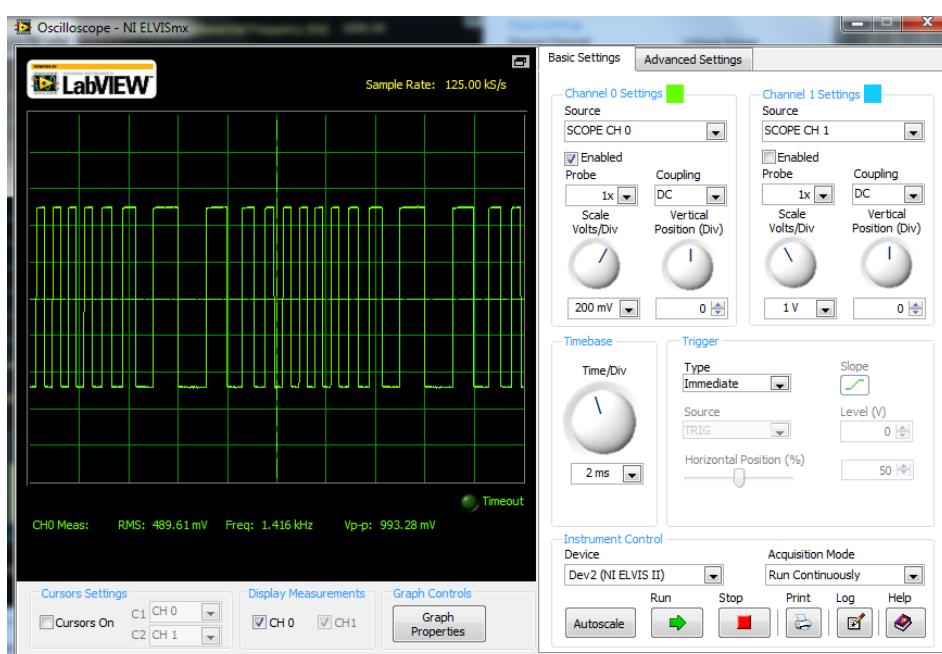
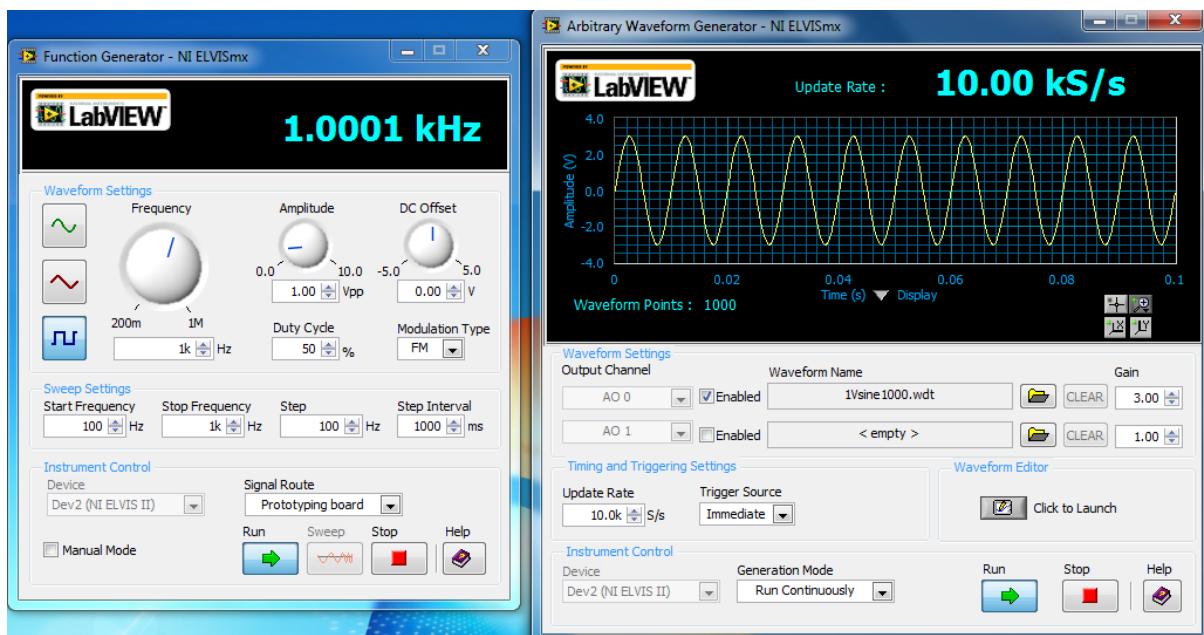


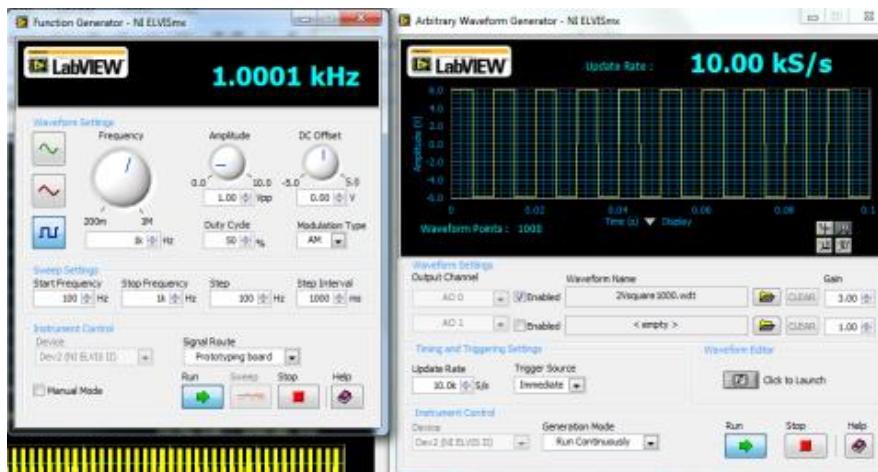
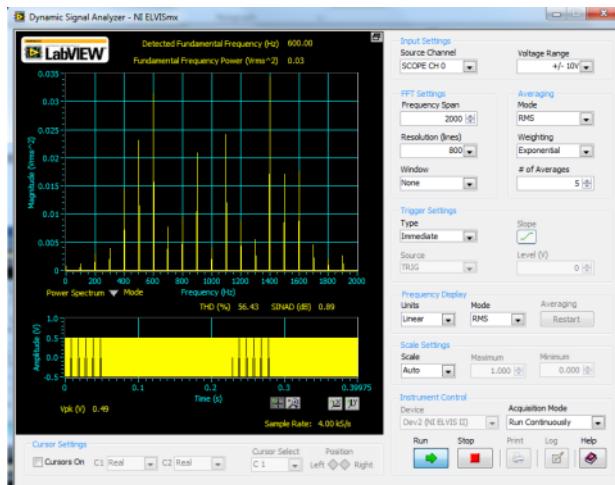


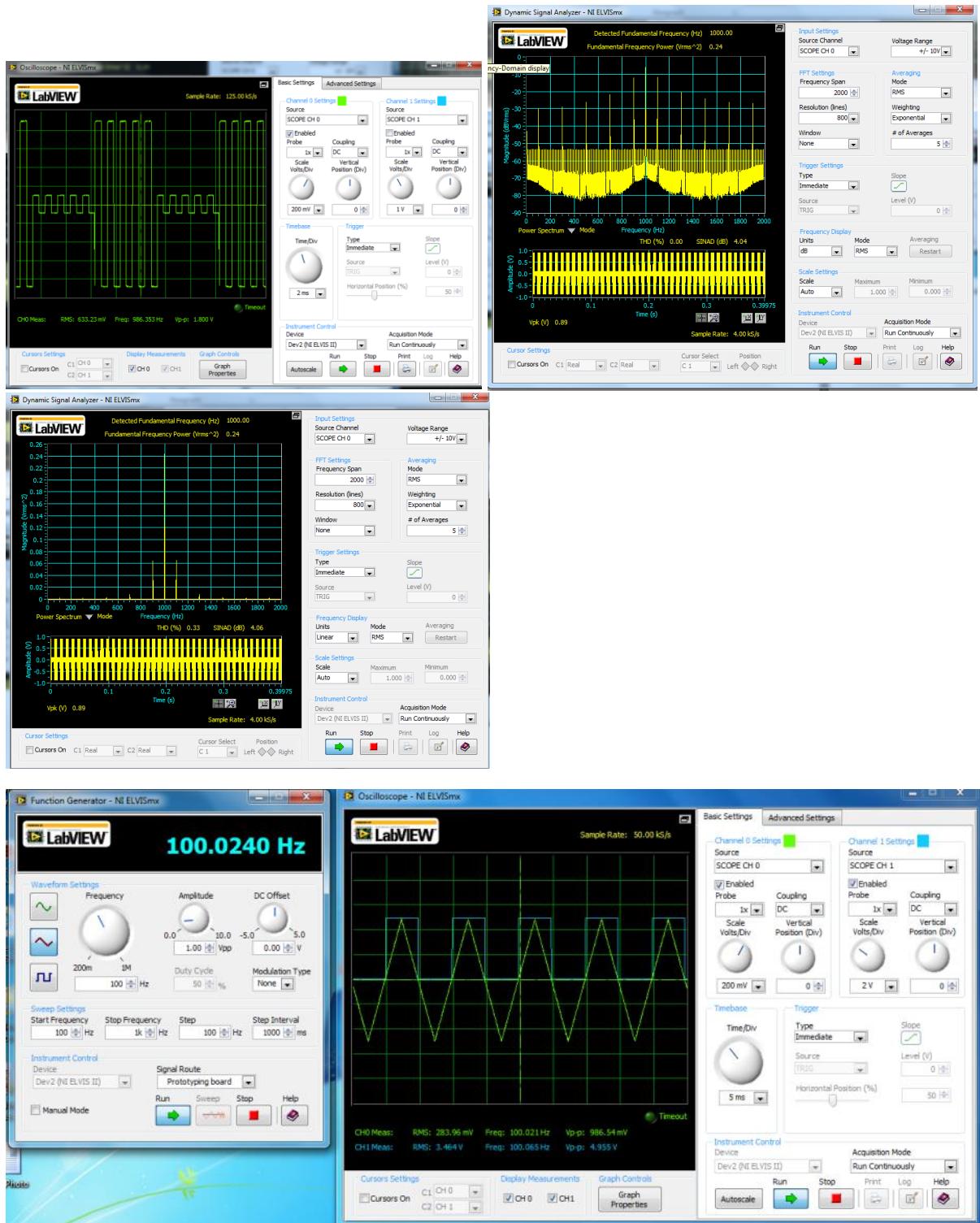


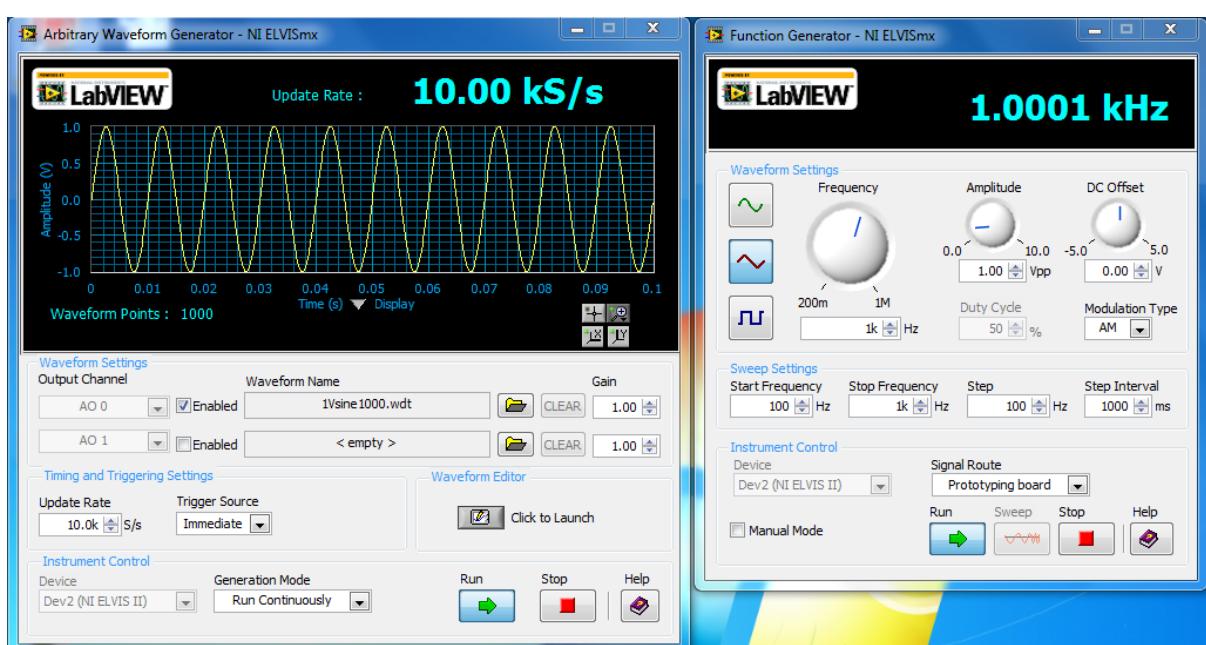
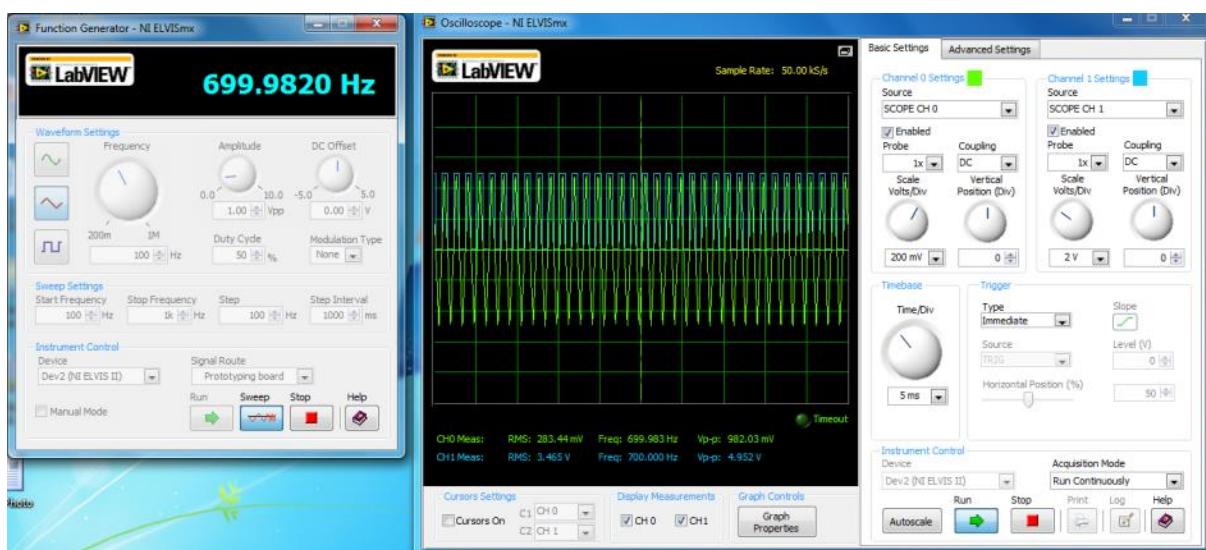
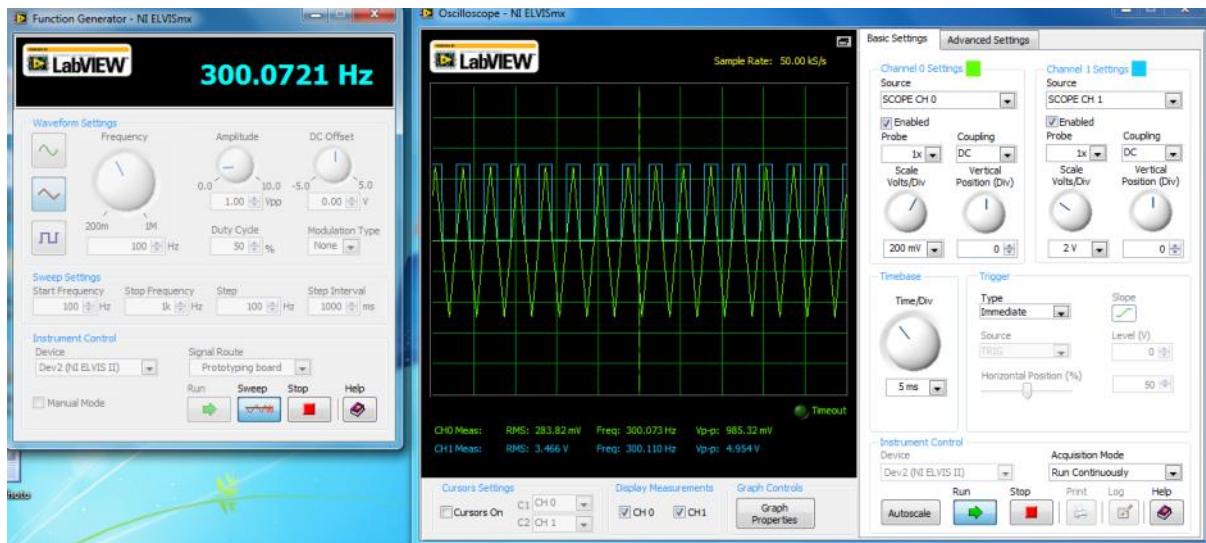


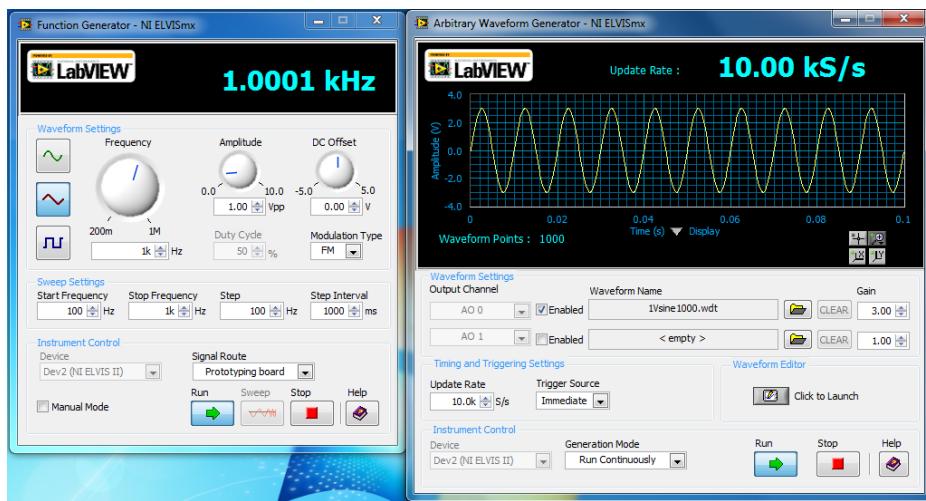
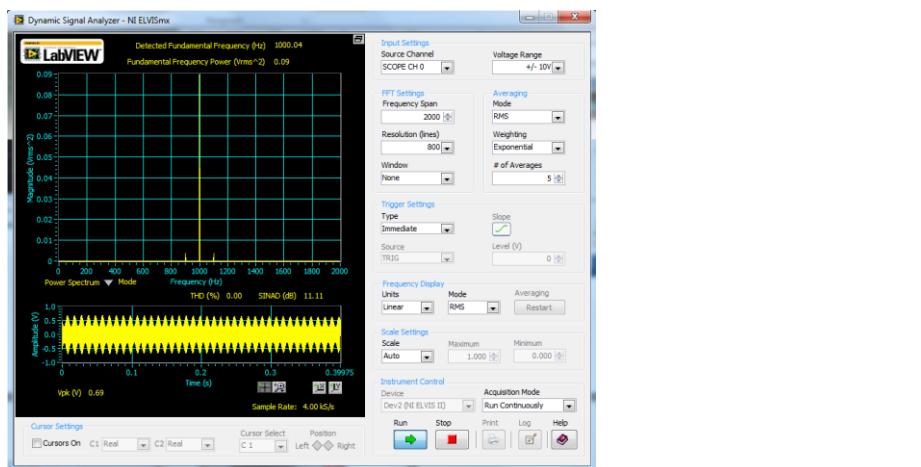
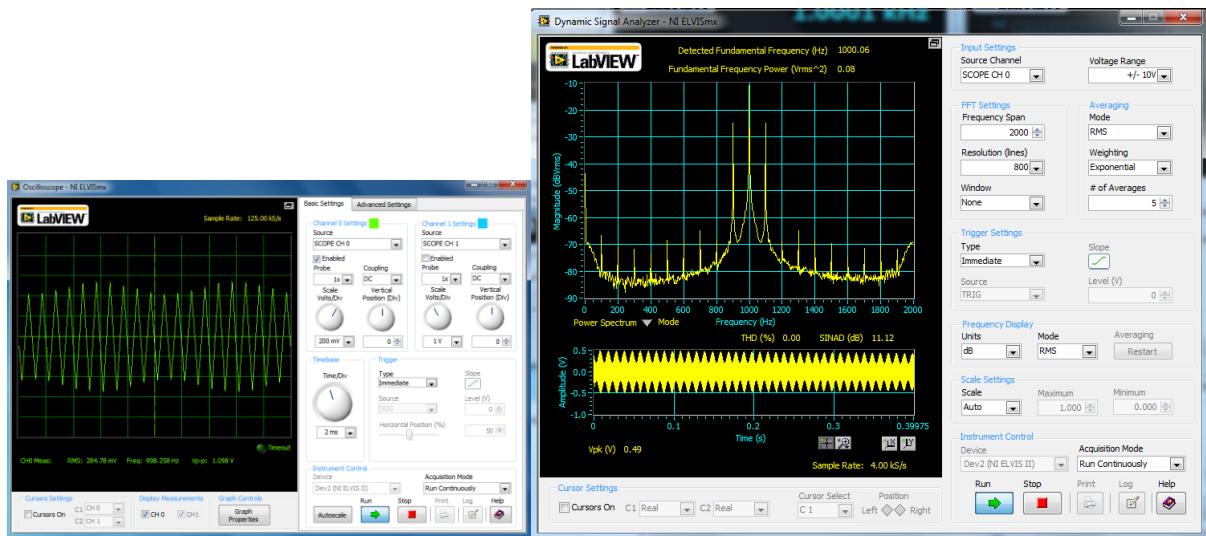


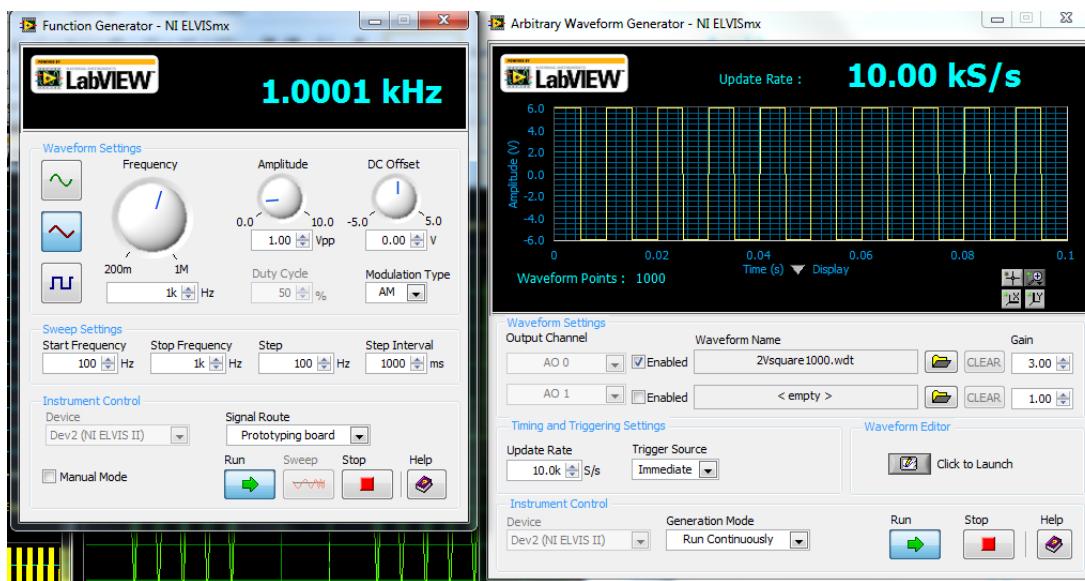
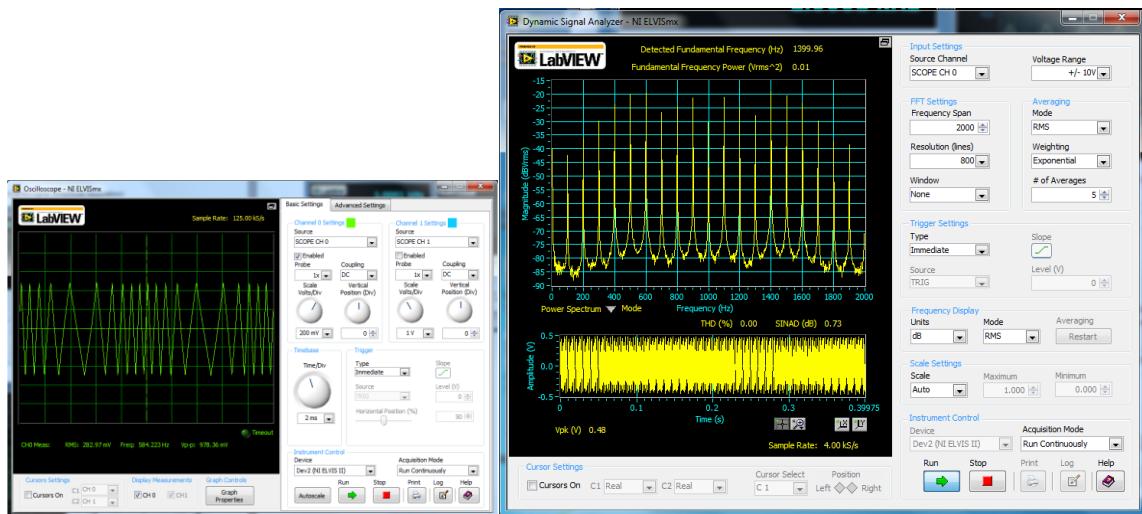


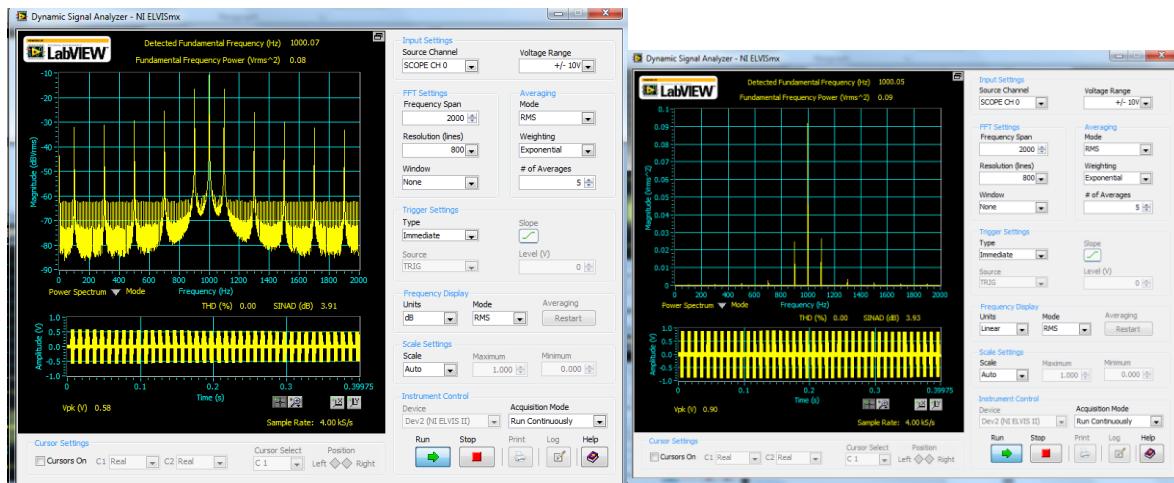




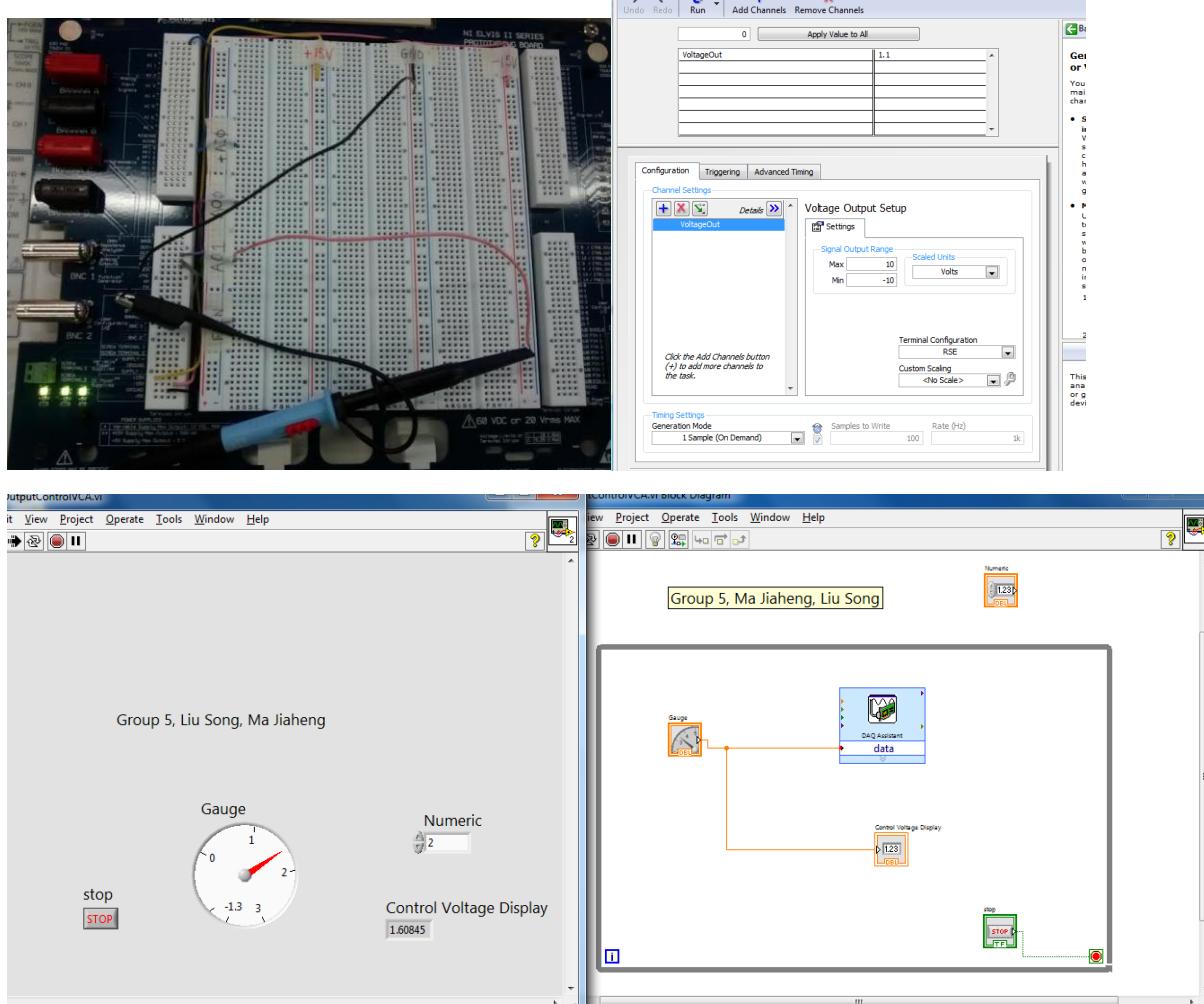


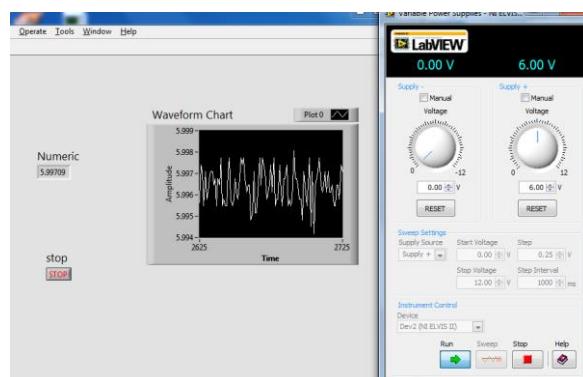
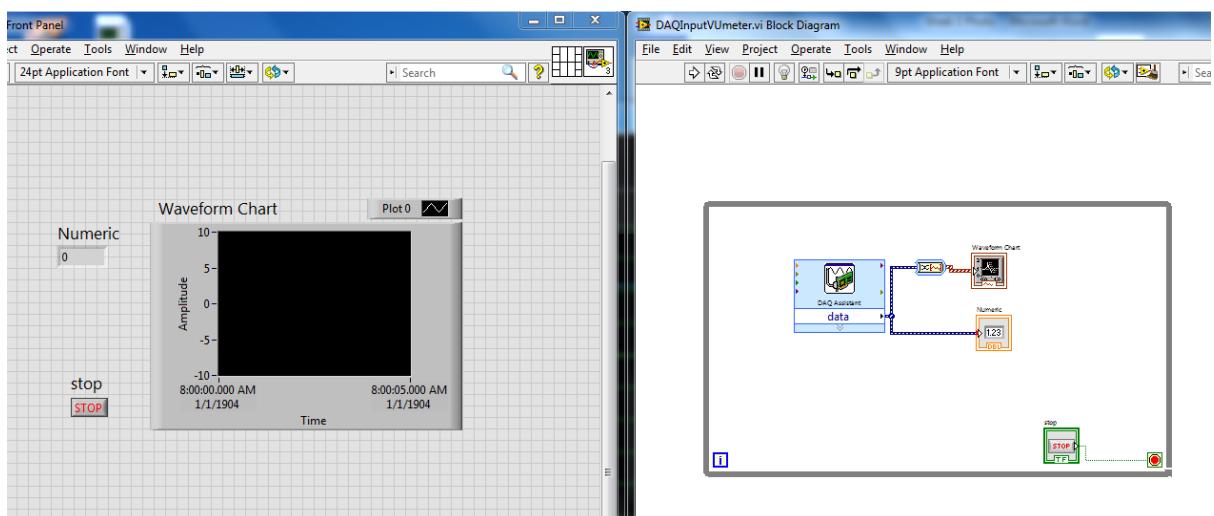
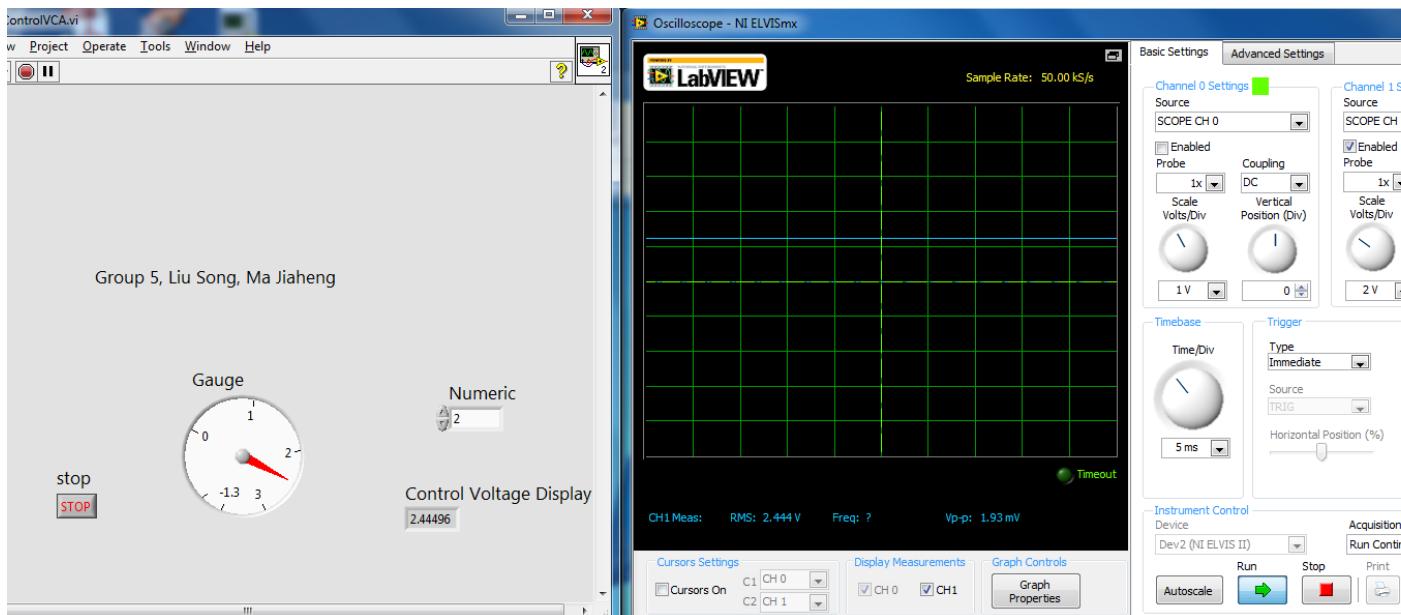




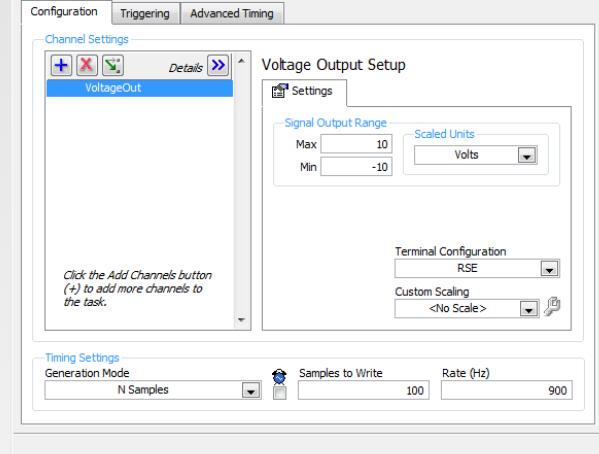
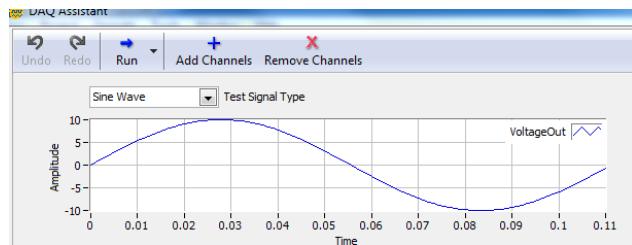
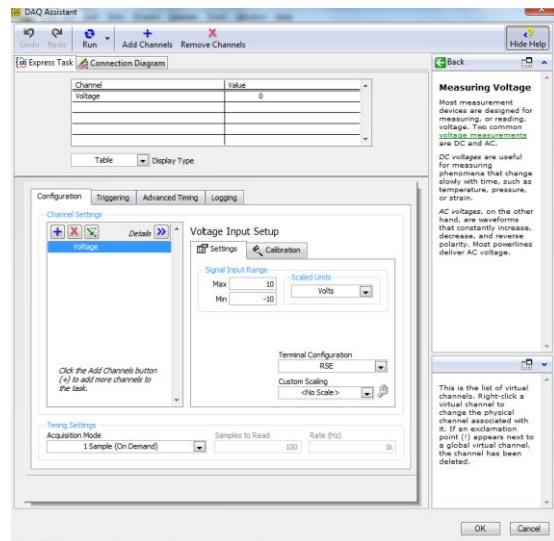
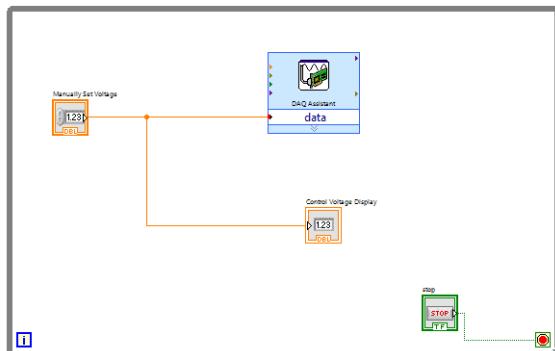


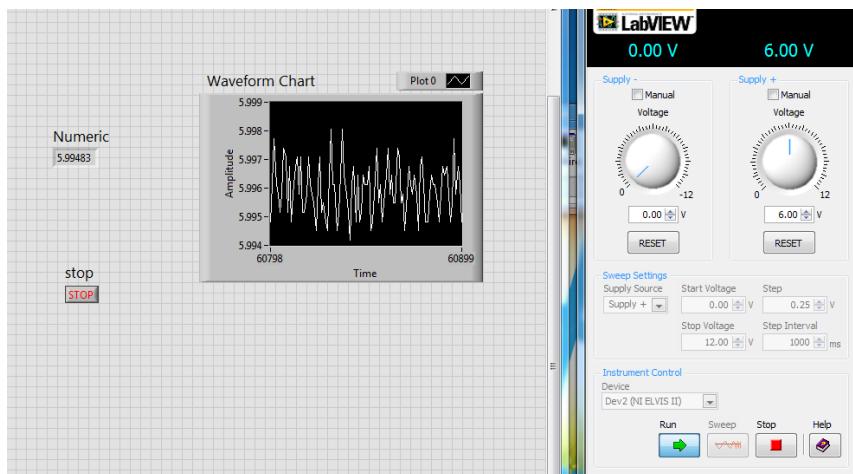
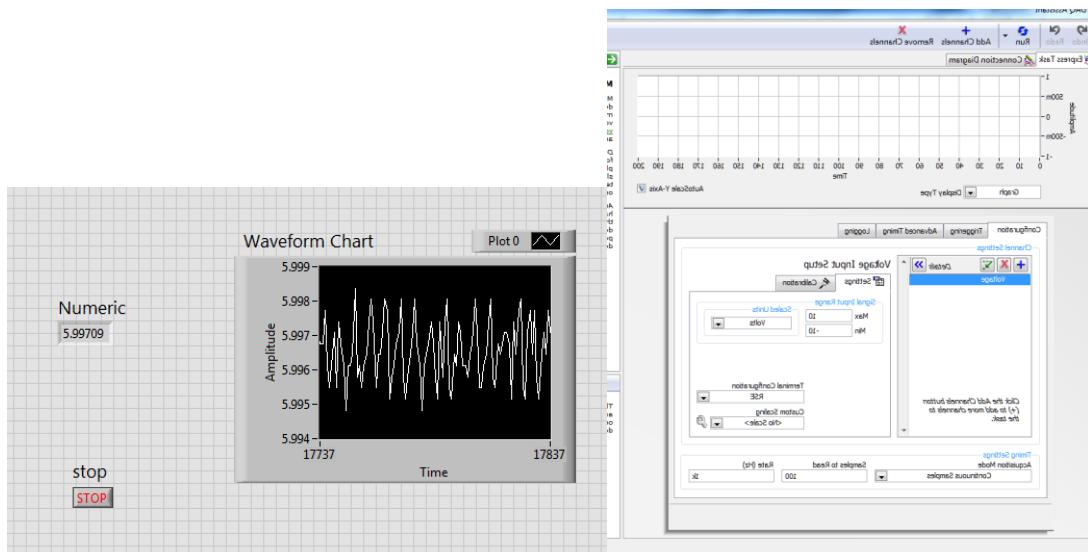
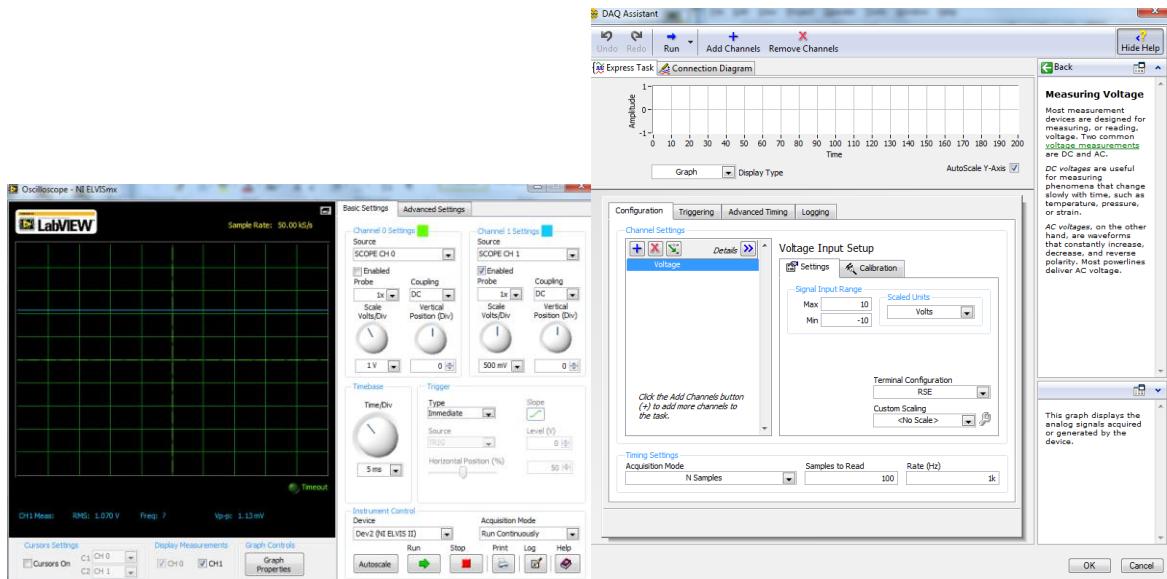
Week 5



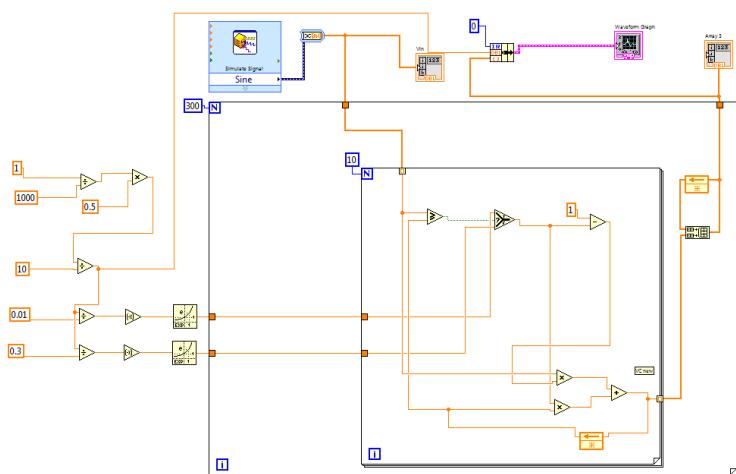
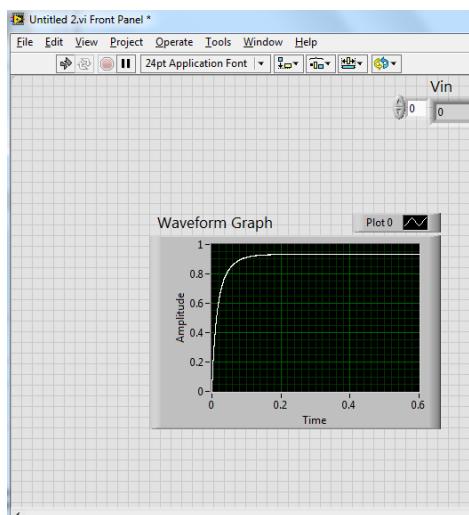
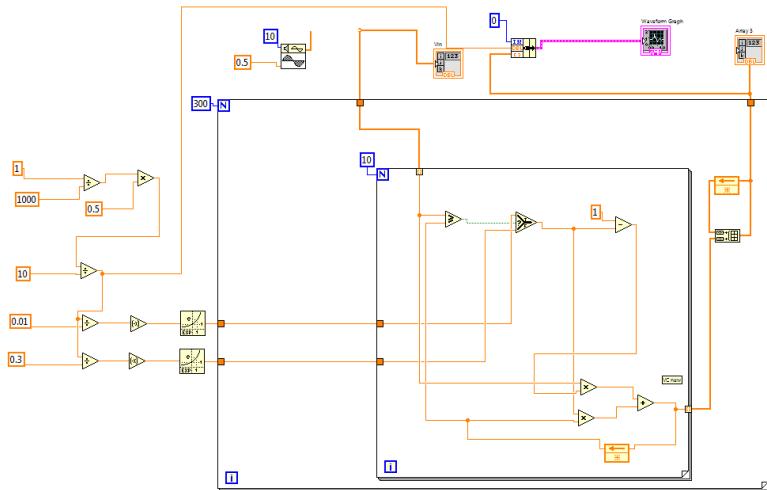


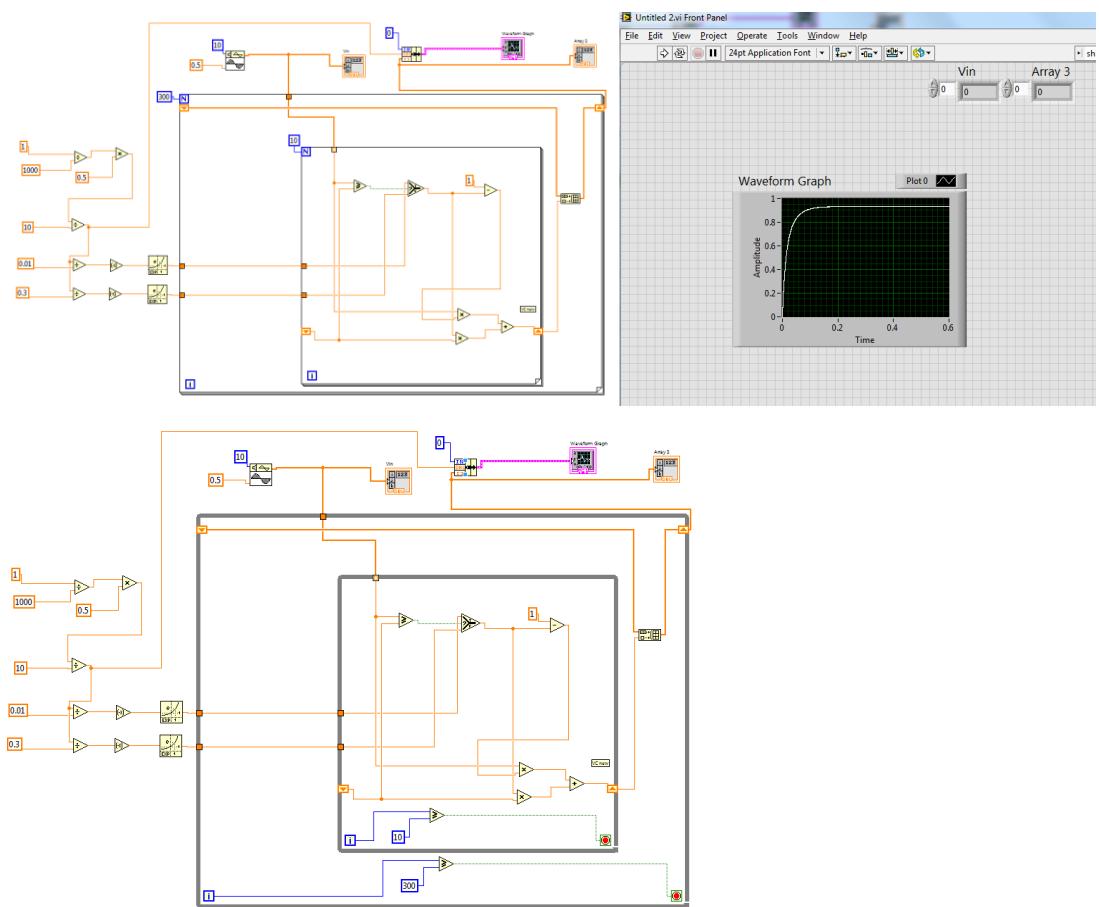
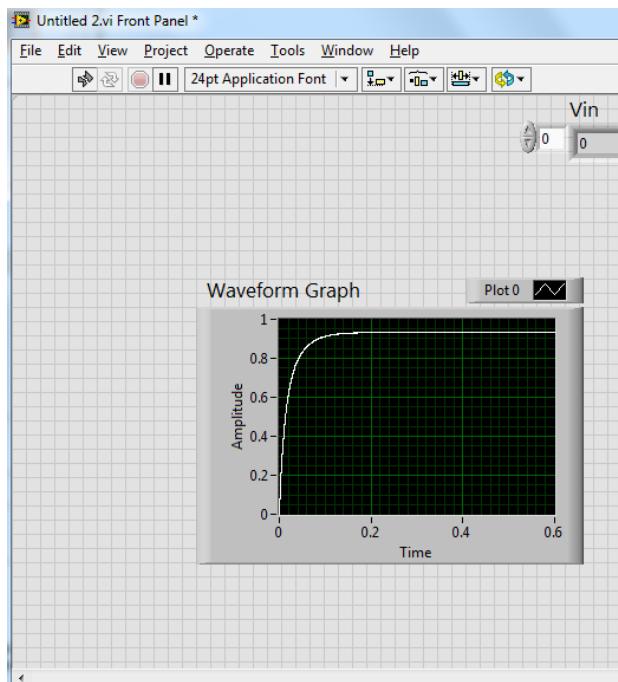
Group 5, Ma Jiaheng, Liu Song

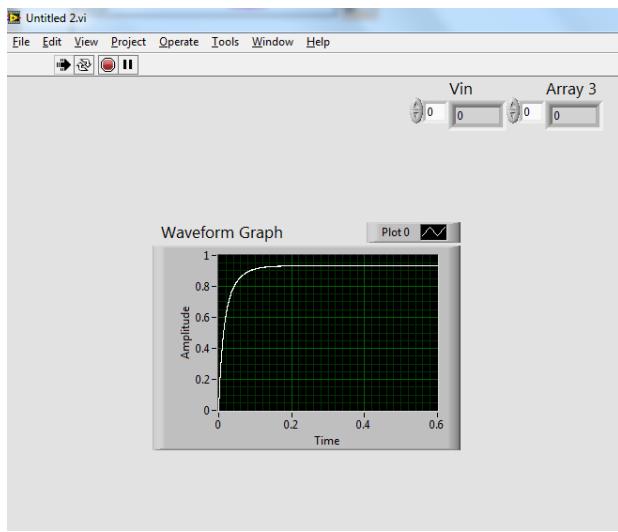




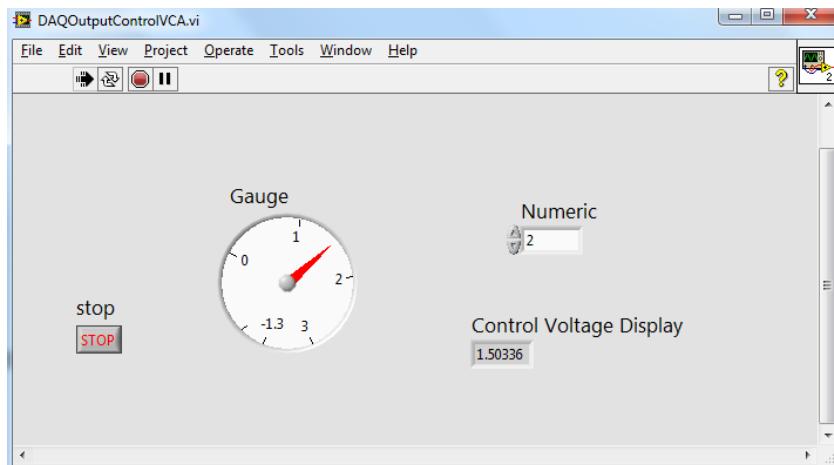
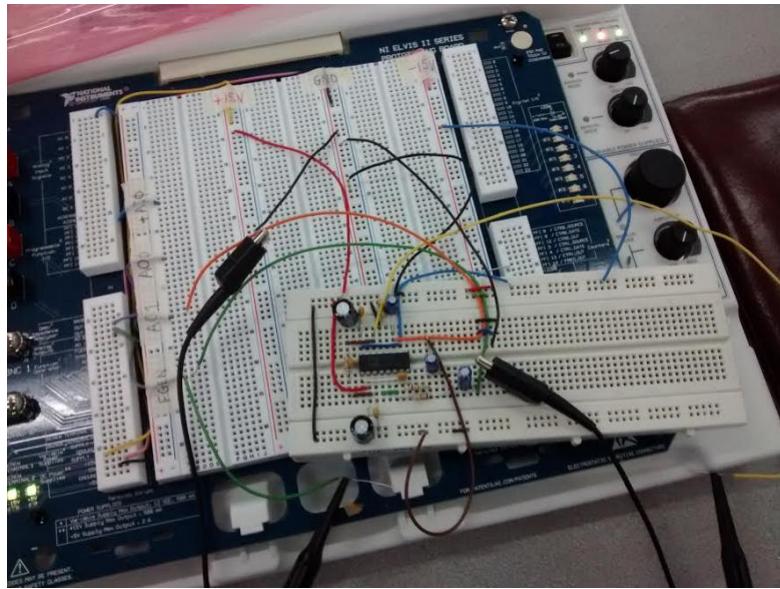
Week6

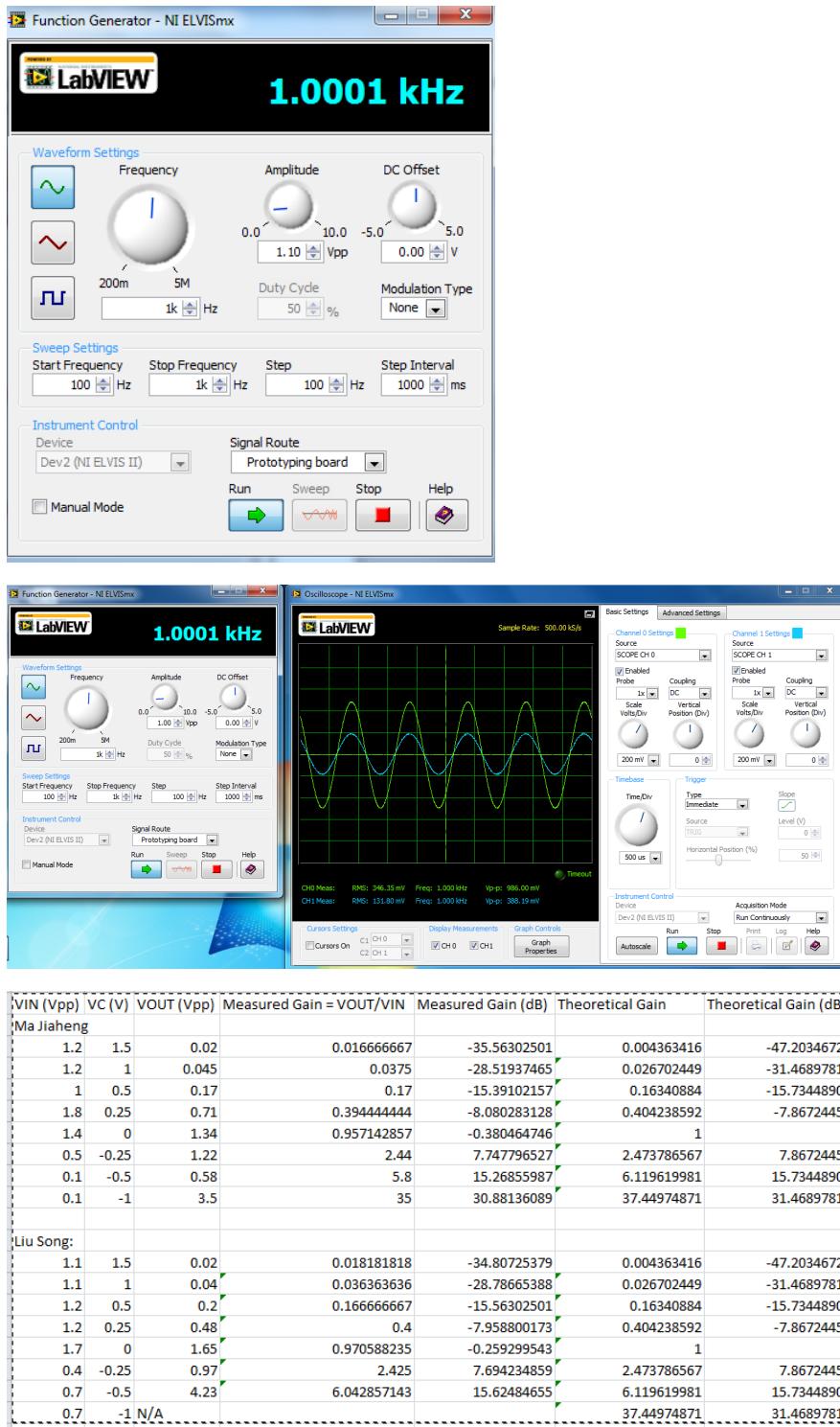


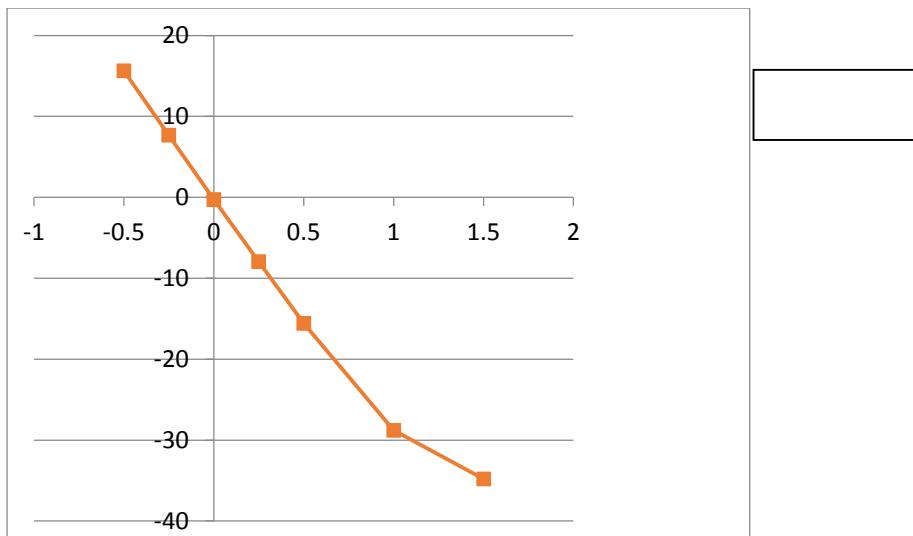




Week 7:







Vp(V)

Bode analyser window capture

0.02



0.01

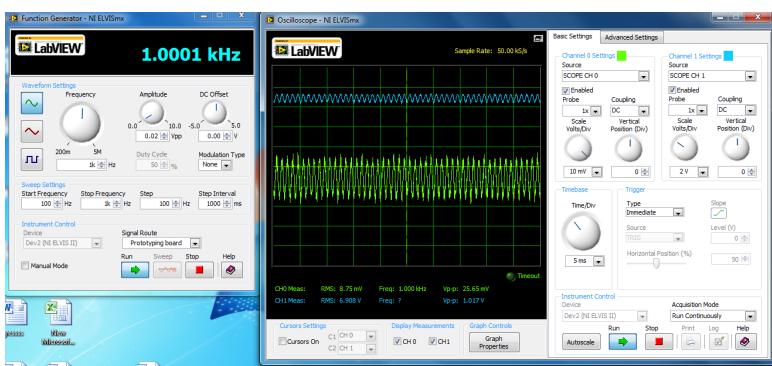
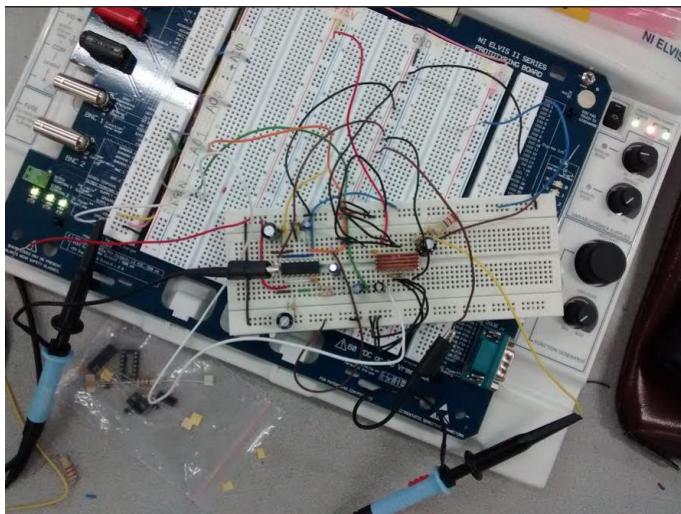


0.07

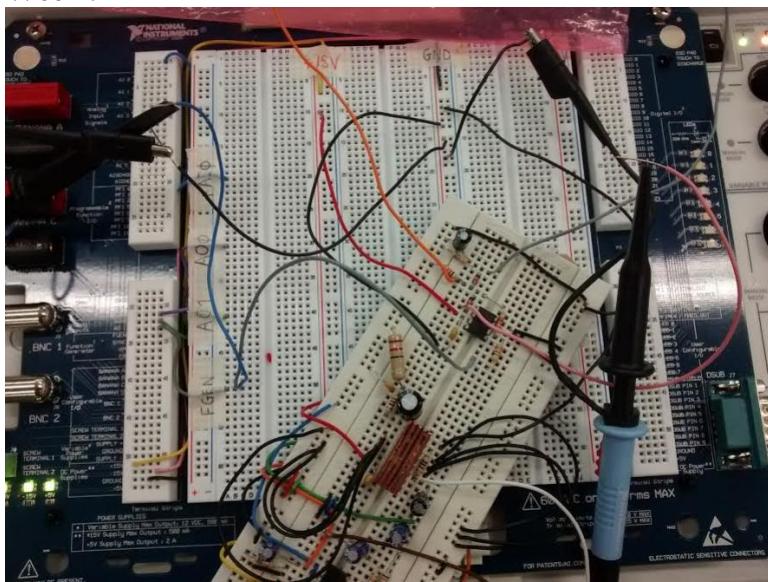


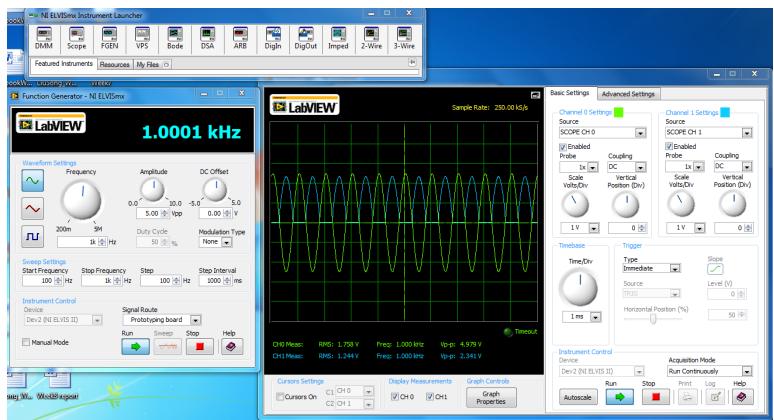
0.04

**Week 8:**

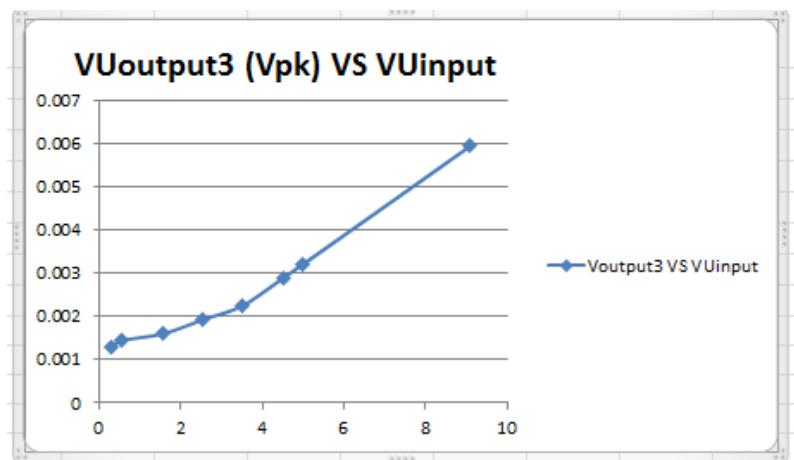
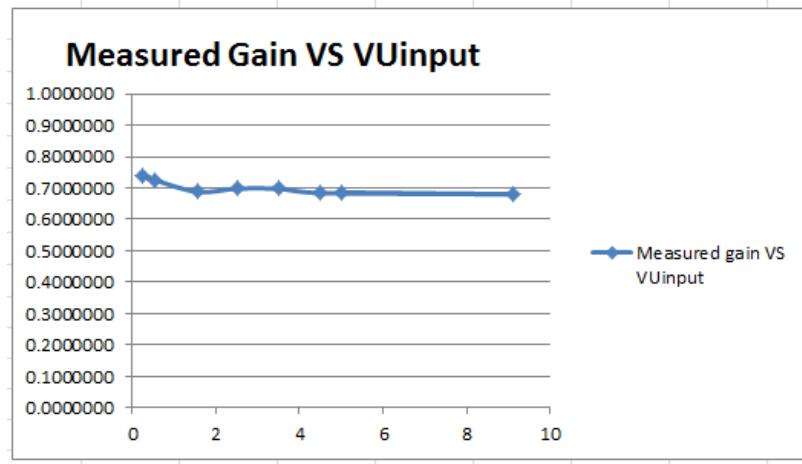


Week 9

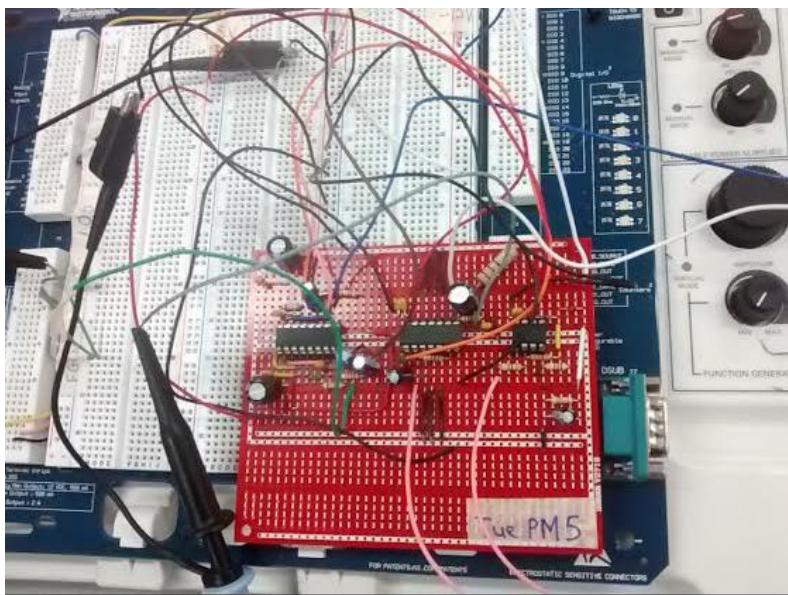




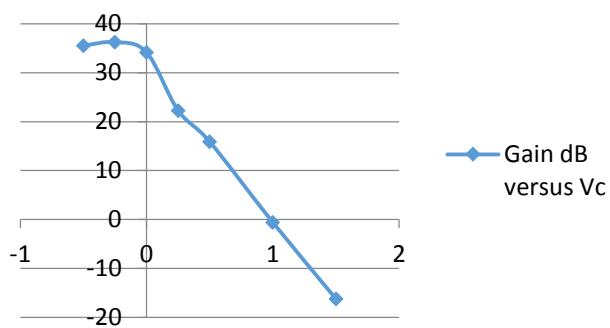
VUinput (Vpp)	VUoutput1 (Vpk)	VUoutput2 (Vpk)	VUoutput3 (Vpk)	Measured Gain
5	2.34	1.716	0.00322	0.6864000
9.1	3.812	3.095	0.00596	0.6802198
4.51	2.162	1.543	0.0029	0.6842572
3.52	1.801	1.228	0.00226	0.6977273
2.52	1.43	0.88	0.00193	0.6984127
1.57	1.068	0.54	0.00161	0.6878981
0.54	0.66	0.196	0.00145	0.7259259
0.27	0.532	0.1	0.00129	0.7407407



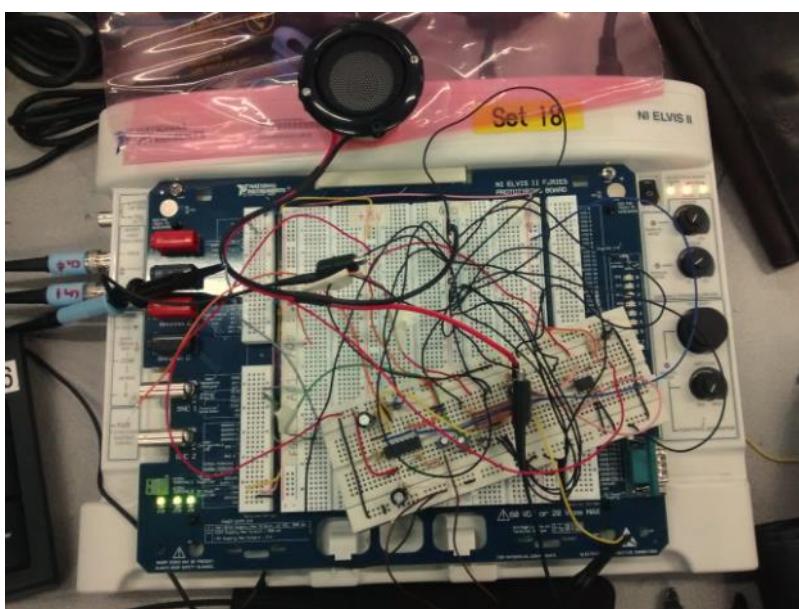
Week 10

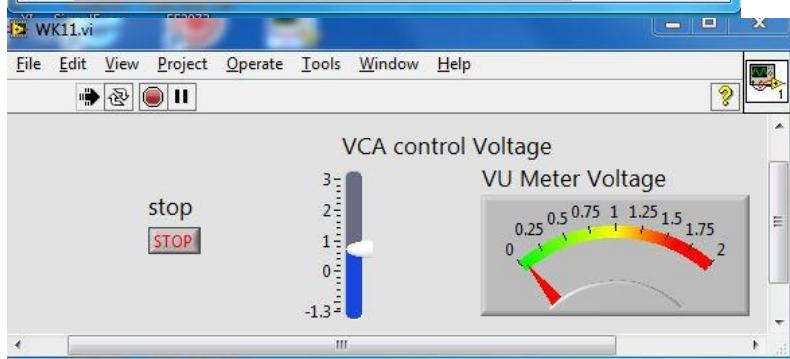
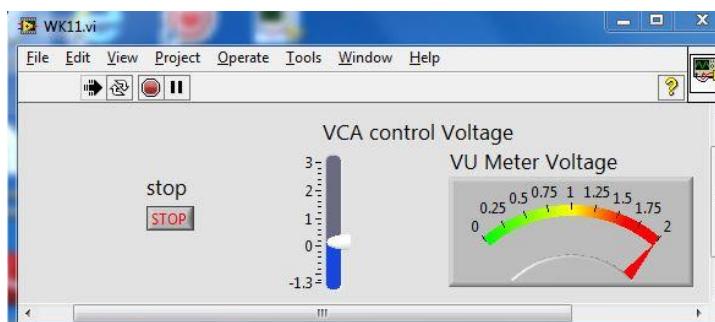
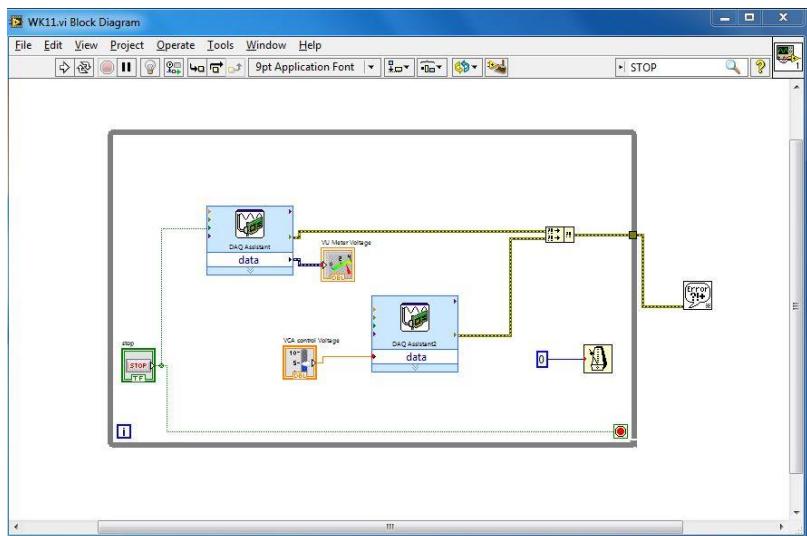


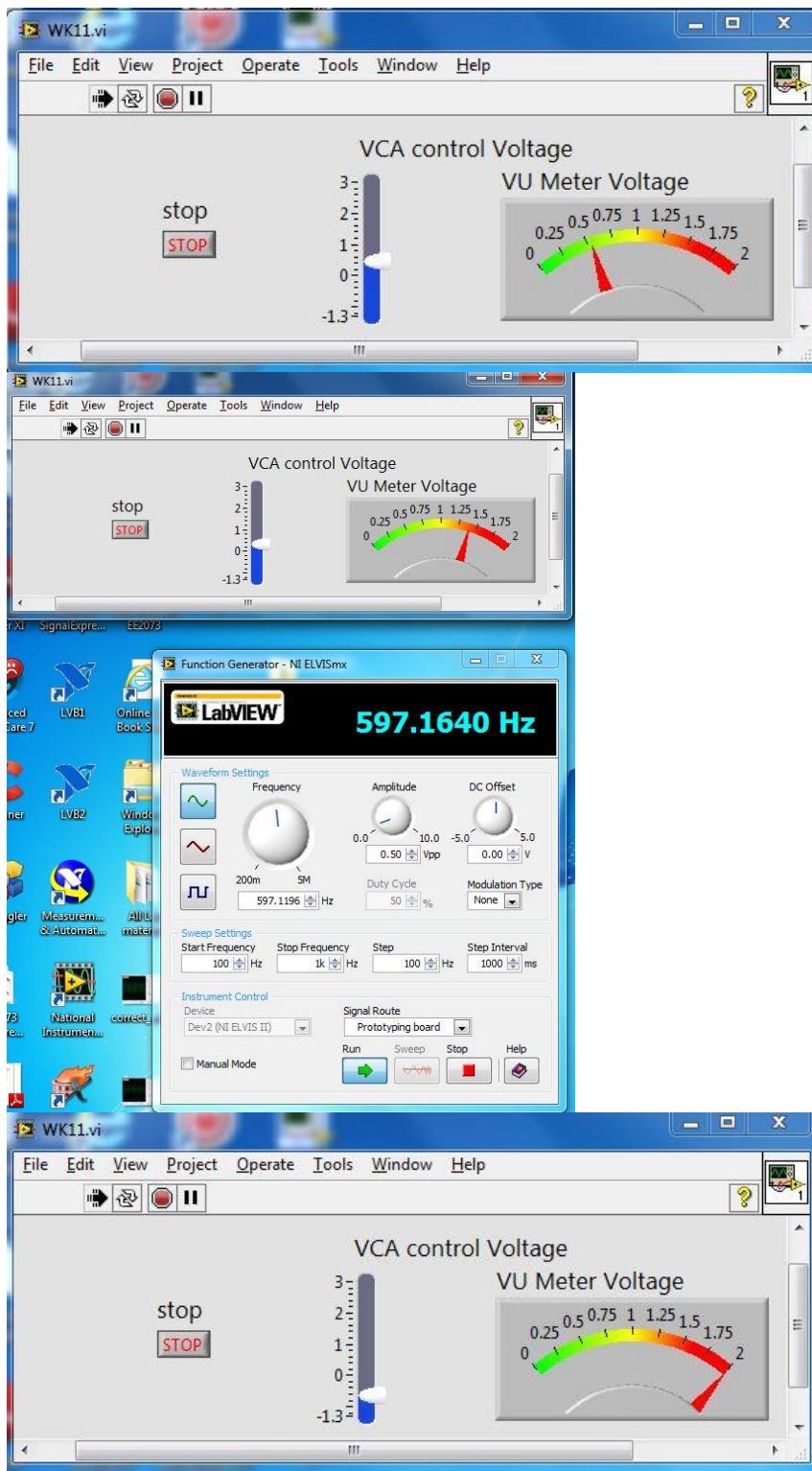
Gain dB versus Vc

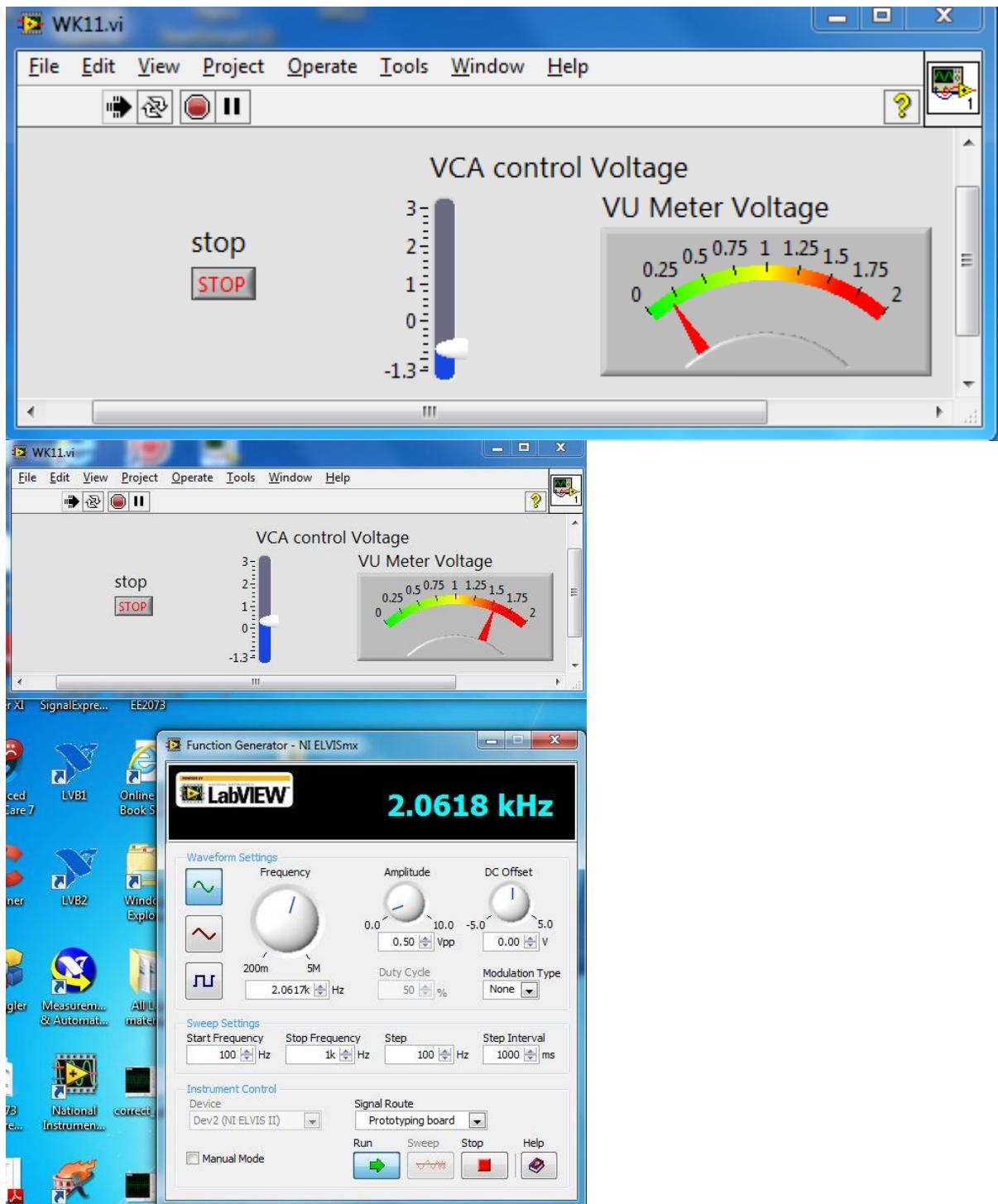


Week 11









Week 12

