



Course: EE3013/ Semiconductor Devices and Processing
School: School of Electrical and Electronic Engineering
Week 12 – MOS Devices

Learning Objectives

At the end of this lesson, you will be able to:

(A) MOS Diode

- Explain the physical structures of an ideal MOS diode and its corresponding energy band diagrams under thermal equilibrium.
- Explain the basic principle of operation and the corresponding energy band diagrams of a MOS diode under depletion, accumulation, inversion and strong inversion.
- Explain the definitions of key parameters such as surface potential, depletion width and threshold voltage.
- Explain the MOS capacitances and the C-V curves for ideal and non-ideal MOS diodes.
- Explain the effects such as work function difference and oxide traps and charges in non-ideal MOS diode and how they affect the energy band diagrams and the threshold voltage.

(B) MOSFET

- Explain the MOSFET physical structure and their principles of operation under cut-off, linear and saturation regions.
- Explain the difference between NMOSFET versus PMOSFET, and depletion- mode versus enhancement mode MOSFET.
- Explain the definition of the cutoff frequency of a MOSFET and how a MOSFET can perform as an amplifying device.

MOS Devices

MOS diode and MOSFET:

- **MOS** diode is expanded as **Metal Oxide Semiconductor** diode.
- **MOSFET** is expanded as **Metal Oxide Semiconductor Field Effect Transistor**.
 - It can be considered as an MOS diode with two p-n junctions formed at two sides of it.

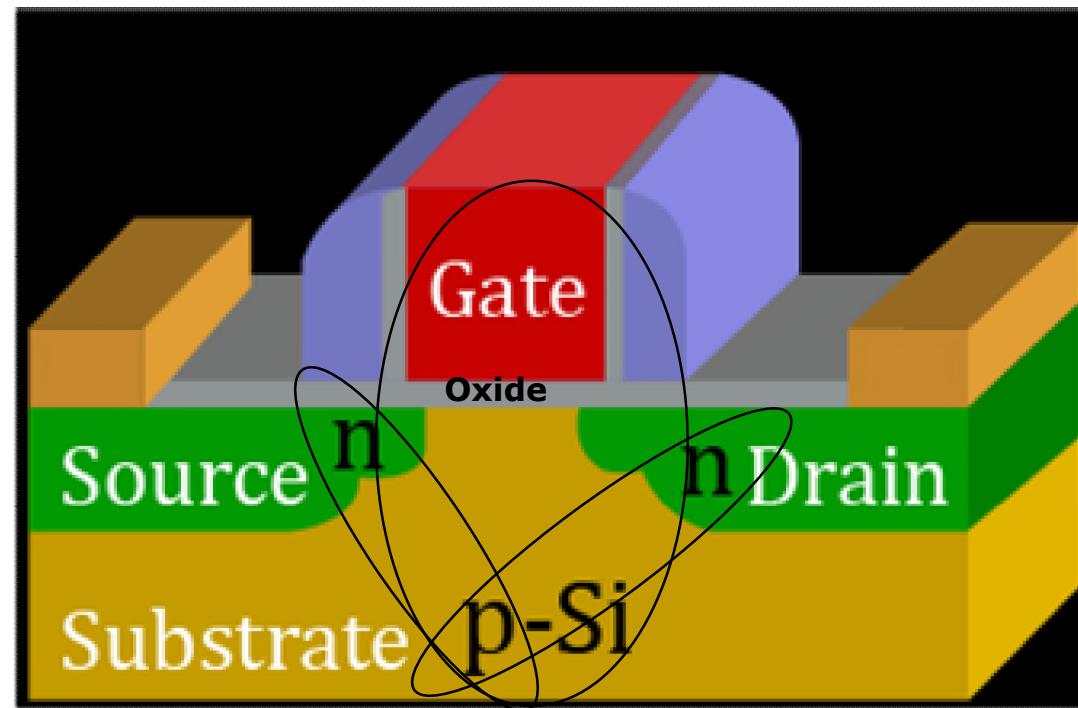


Figure 3.1

MOS Devices

- The first MOSFET made in 1960 was $20\ \mu m$ long channel & $100\ nm$ thick oxide.
- The current technology MOSFET is $14 - 18nm$ channel and $< 1nm$ high-K dielectric.

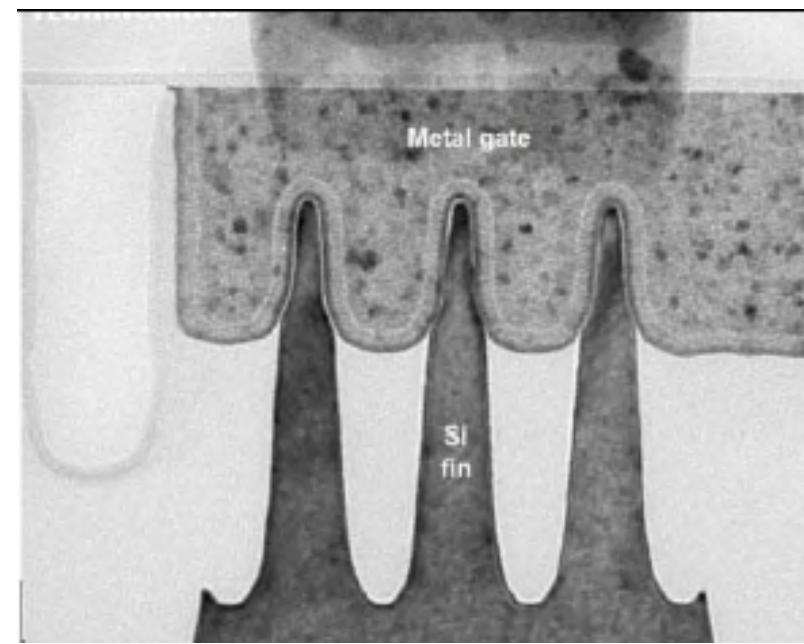
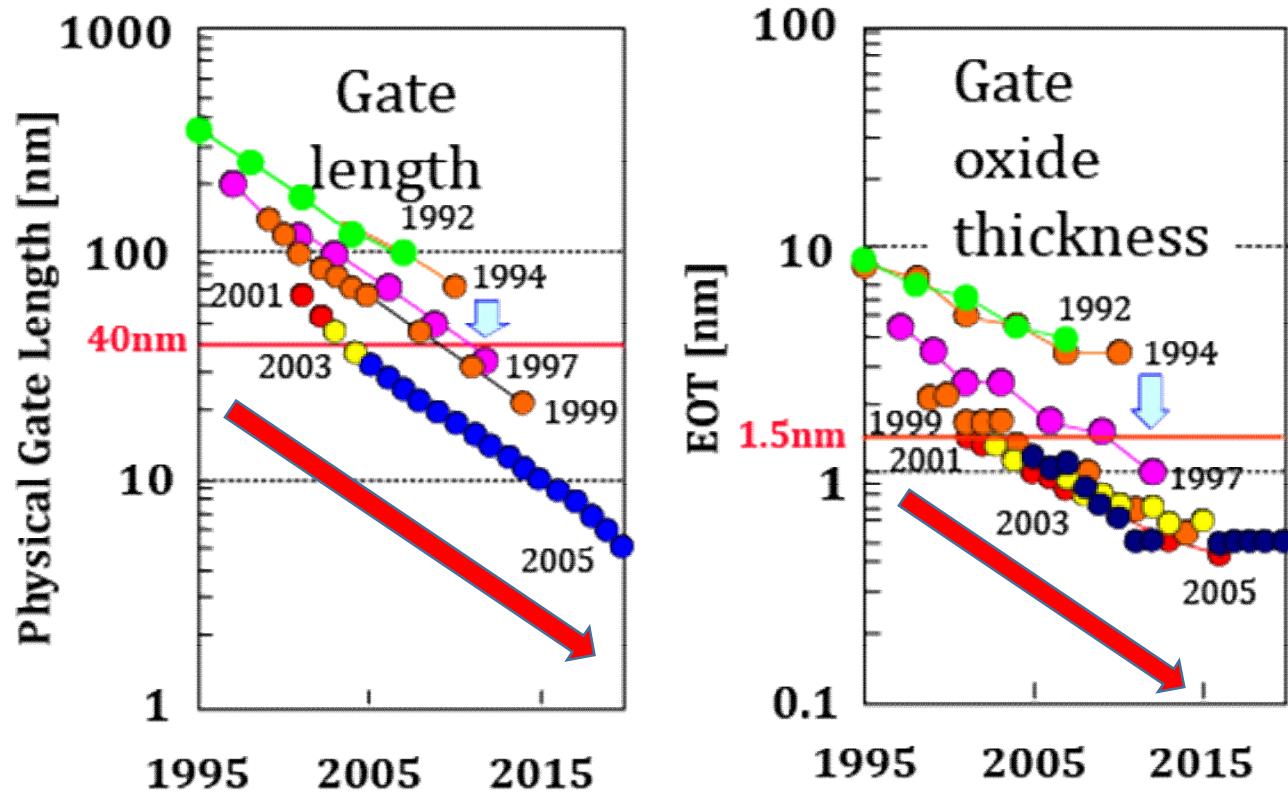


Figure 3.3. Samsung's 14nm gate transistor

Importance of MOS Diodes

1

It is the heart of a MOSFET.

2

It is extremely useful in the study of semiconductor surface.

3

It can be used as a stand-alone storage capacitor and building block for charge-coupled devices (CCD).

Structure of MOS Diodes

MOS diodes consists of:

- p- or n- type Si substrate, usually grounded,
- A thin layer of silicon oxide (as an insulation layer), and
- A layer of metal, as a gate in which a voltage is applied.

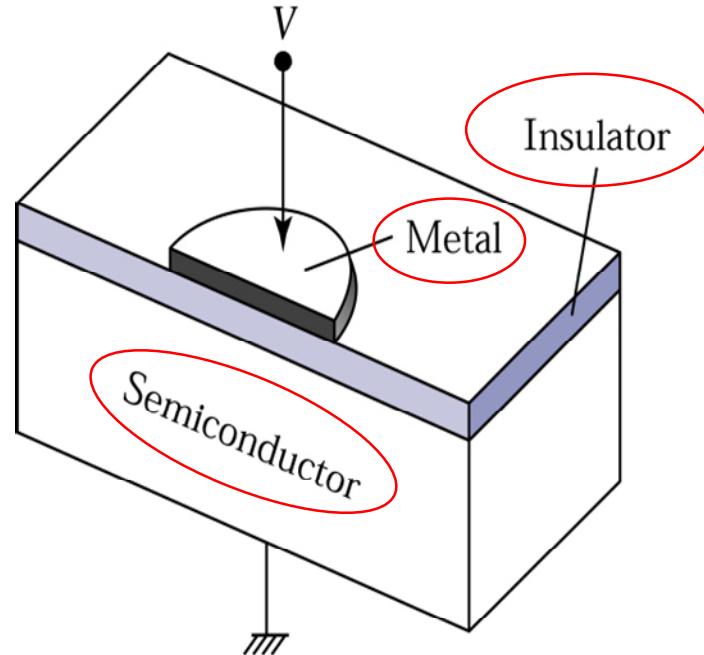


Figure 3.4a

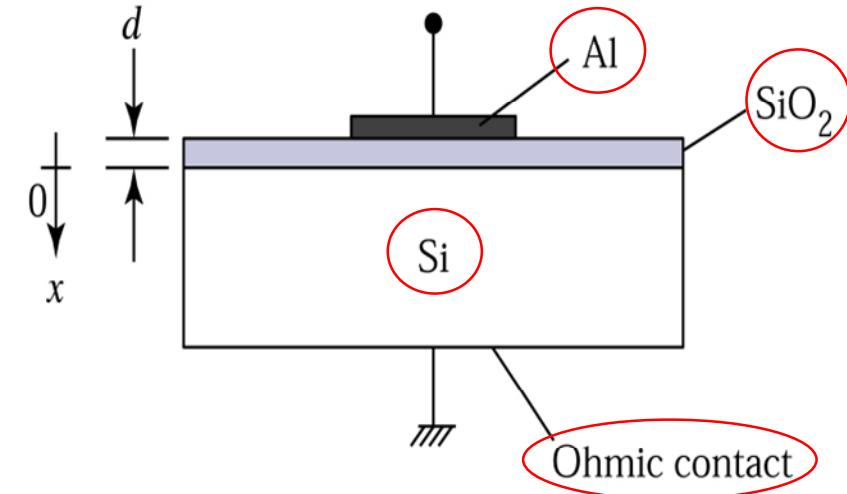


Figure 3.4b

Energy Band Diagram of an Ideal MOS Diode

The band diagram with p-type Si at $V = 0$ is shown below.

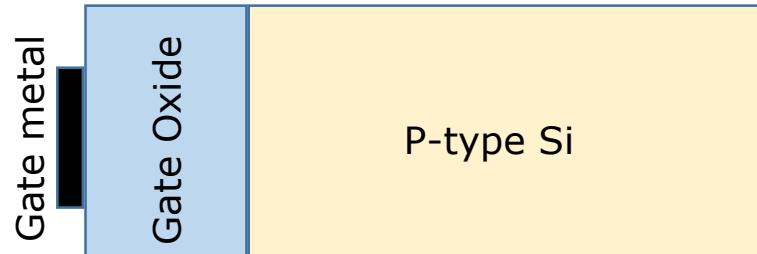


Figure 3.5

$$q\phi_m = q\phi_s$$

$$q\phi_s = qx + \frac{E_g}{2} + q\psi_B \quad (\text{Equation 3.1})$$

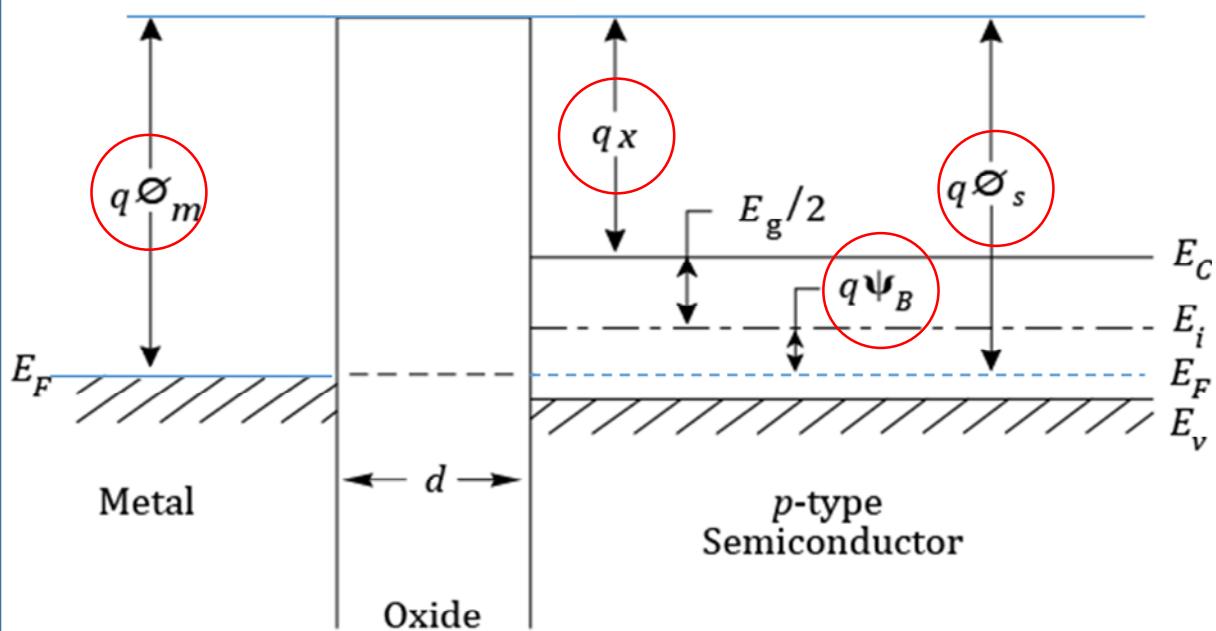


Figure 3.6

Where,

$q\phi_m$: Metal work function (energy difference between Fermi level and vacuum level)

$q\phi_s$: Semiconductor work function

$q\chi$: Electron affinity (energy difference between E_C and vacuum level)

$q\psi_B$: Energy difference between Fermi level E_F and E_i

Definition of Ideal MOS Diodes

An ideal MOS diode is defined as follows:

- **At Zero applied bias**, the energy difference between the metal work function $q\phi_m$ and the semiconductor work function $q\phi_s$ is zero.

$$q\phi_{ms} = q\phi_m - q\phi_s = \boxed{q\phi_m - \left(qx + \frac{E_g}{2} + q\psi_B \right) = 0} \quad (\text{Equation 3.2})$$

Where $q\phi_s = qx + \frac{E_g}{2} + q\psi_B$

- The energy band is flat, also called the **flat band condition**.
- Under any biasing condition, the charges existing in the diode are those in semiconductor and those with equal but opposite sign on metal surface near oxide, There is **no charge in SiO₂**.
- There is no carrier transport through the oxide under DC bias, implying that the **resistivity of the oxide is infinite**.

An Ideal MOS Diode Under Bias

When an ideal MOS diode is biased, then **three cases** exist at the semiconductor surface, as shown below for **p-Si**.

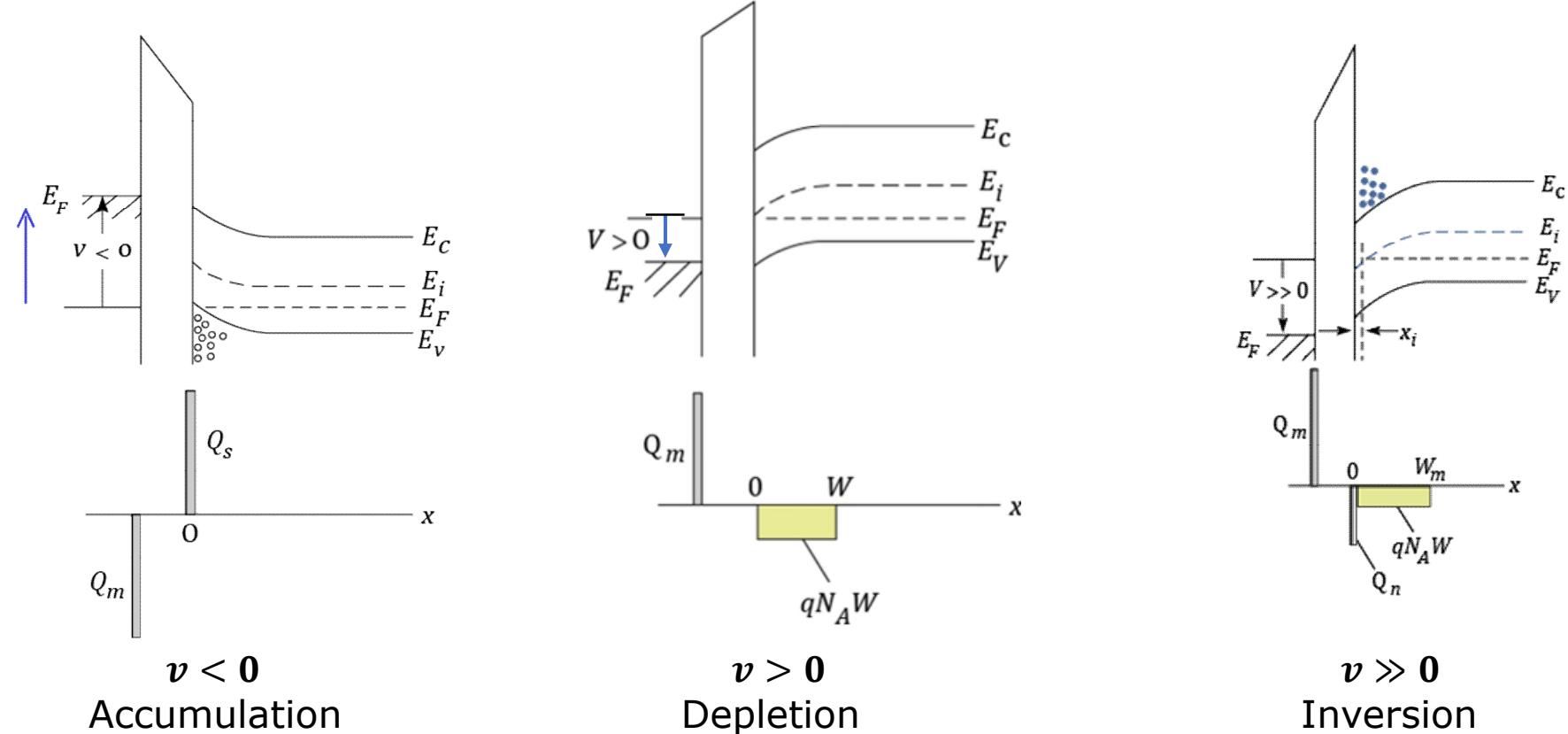


Figure 3.7

Accumulation

A negative voltage ($V < 0$) is applied:

- The E_F in metal **moves up** w.r.t. the E_F of semiconductor.
- Excess **majority carriers** (holes) are induced/**accumulated** at the oxide-semiconductor interface.
- Energy bands (E_i , E_v & E_c) at semiconductor near interface are **bent upward**.
- Ideally **no current flows** through the structure. The E_F in semiconductor remains **constant**.
- The upward bending causes **increase** of $E_i - E_F$ and then the **hole concentration p_p** at the interface.

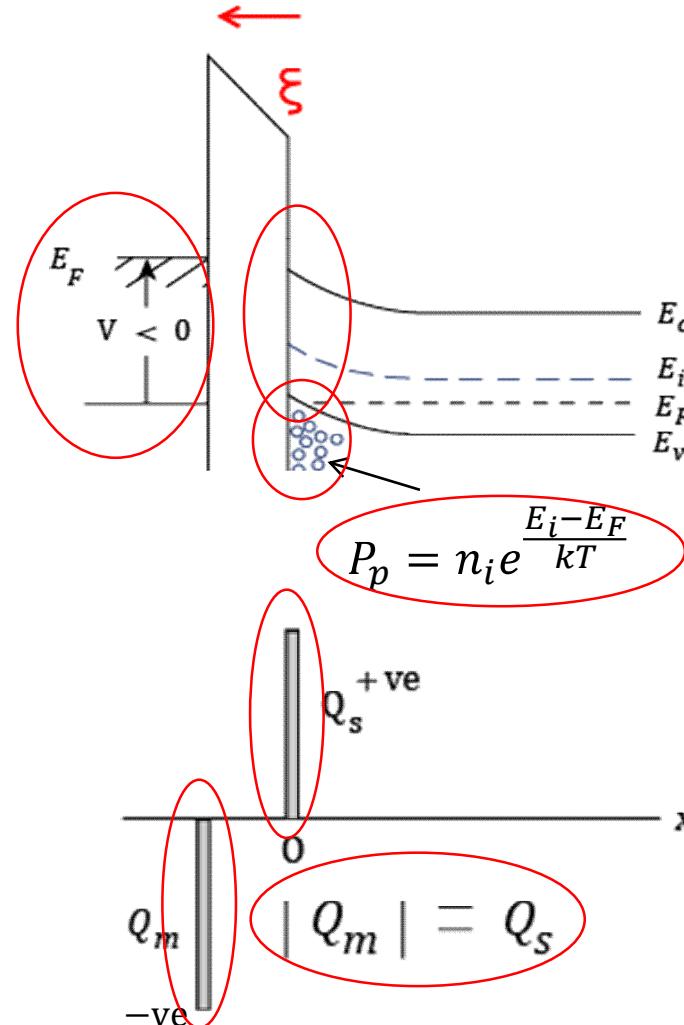


Figure 3.8

Figure 3.9

Depletion

A small positive voltage is applied ($V > 0$):

- The E_F in metal **moves down** w.r.t. the E_F of semiconductor.
- Energy bands (E_i, E_v & E_C) at semiconductor are **bent downward**.
- The **majority carriers** (holes) in the semiconductor near interface become **depleted**. A depletion region with a width W appears.

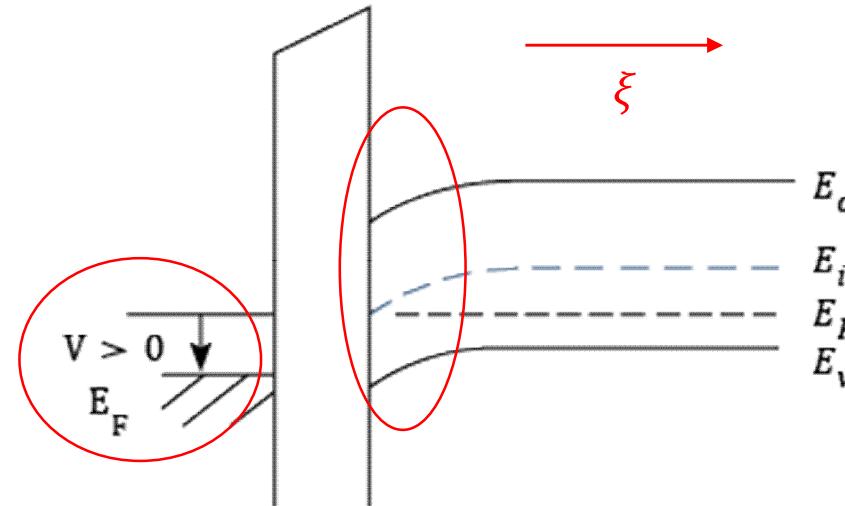


Figure 3.10

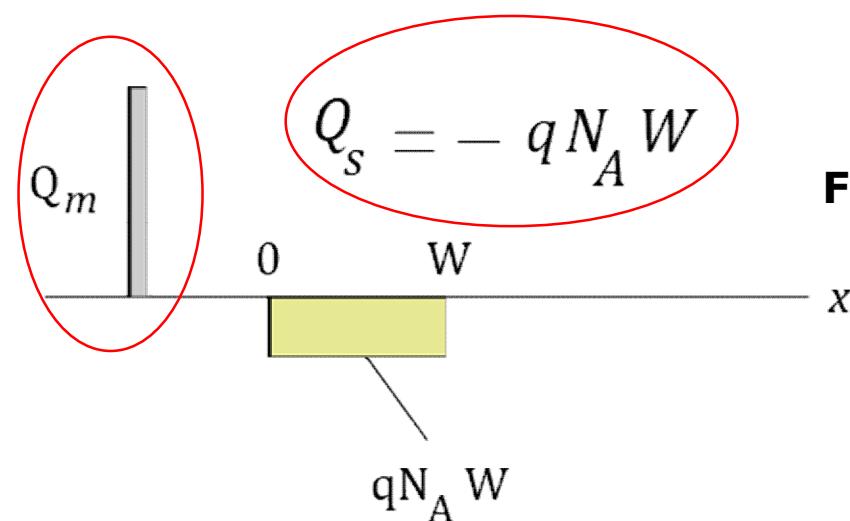


Figure 3.11

Inversion

A large positive voltage ($V \gg 0$) is applied:

- The E_F in metal moves down **further**.
- Energy bands (E_i, E_v & E_c) at semiconductor are bent **downward more**. So, the intrinsic level E_i at surface goes below E_F .
- It means that the semiconductor at surface is **inverted into n-type** with an electron concentration n_p in a thin inversion layer x_j .
- **Q_n is the negative charges due to electrons.**

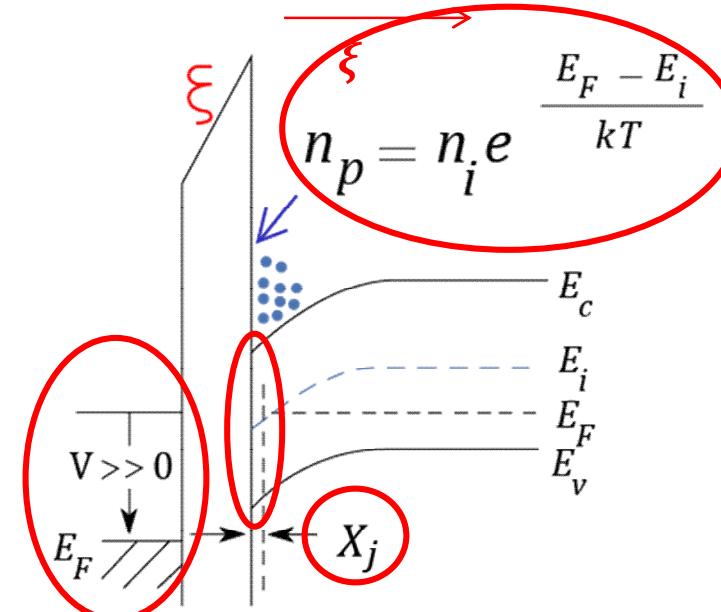


Figure 3.12

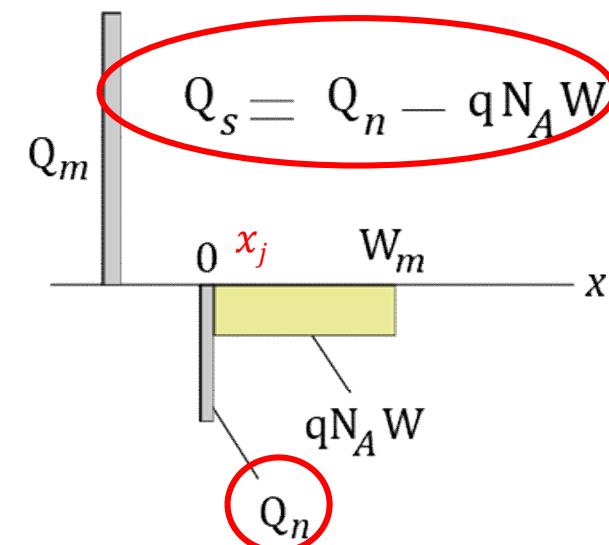


Figure 3.13

Strong Inversion

- Once inversion occurs, further increase in V will increase n_p in a thin inversion layer and the bands are further bent downwards.
- The onset of strong inversion occurs when the electron concentration at the semiconductor surface n_p is equal to the substrate doping level N_A , i.e. ($n_p = N_A$).
- The depletion width will reach a maximum W_m ,** and total charges become:

$$Q_s = Q_n - qN_A W_m \quad (\text{Equation 3.3})$$

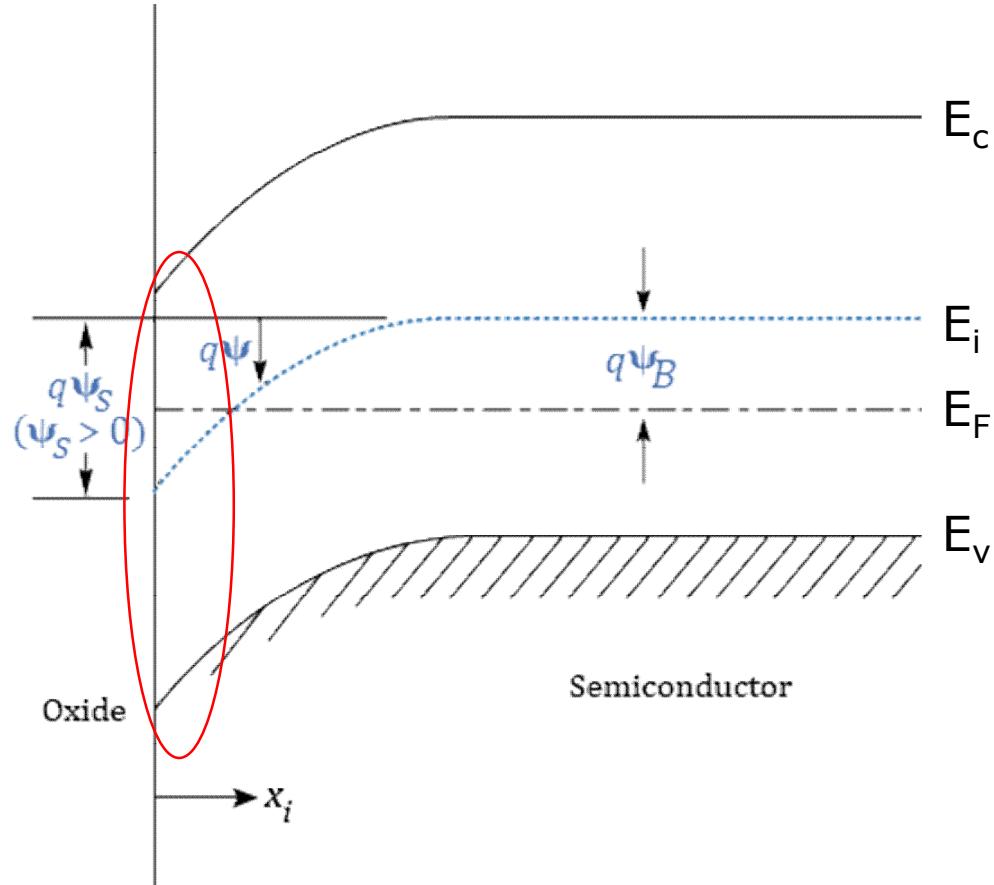


Figure 3.14

Surface Potential (ψ)

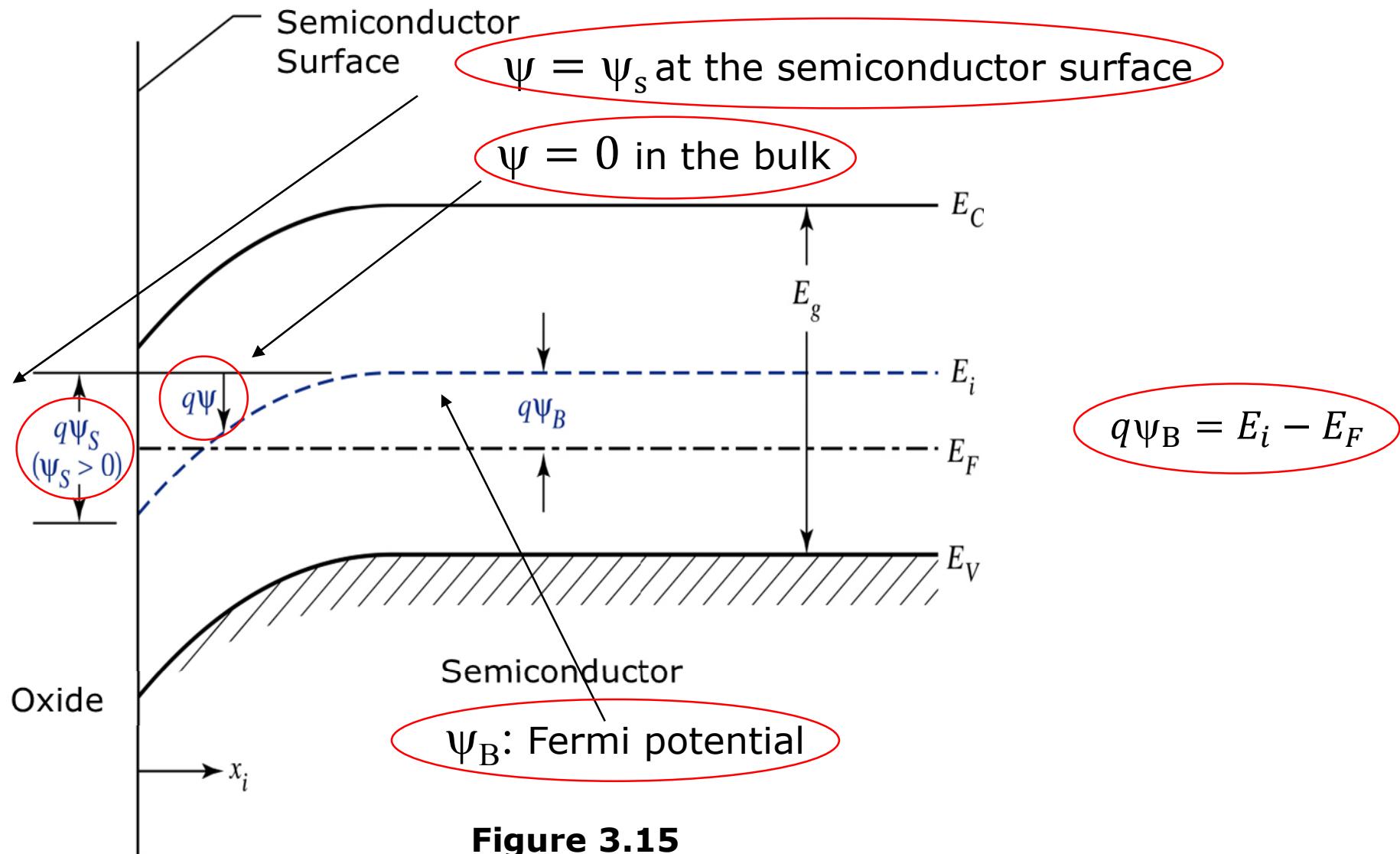


Figure 3.15

Summary

- (a) $\psi_s < 0$ **Accumulation** of holes (bands bend **upward**)
- (b) $\psi_s = 0$ **Flat-band** condition
- (c) $\psi_B > \psi_s > 0$ **Depletion** of holes (bands bend **downward**)
- (d) $\psi_s = \psi_B$ **Midgap** with $n_s = n_i$ (intrinsic concentration)

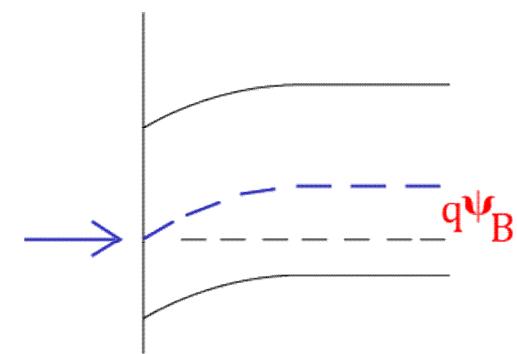
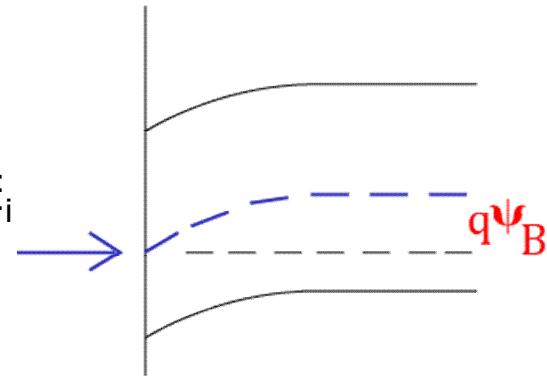
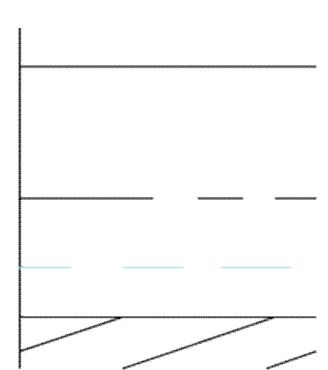
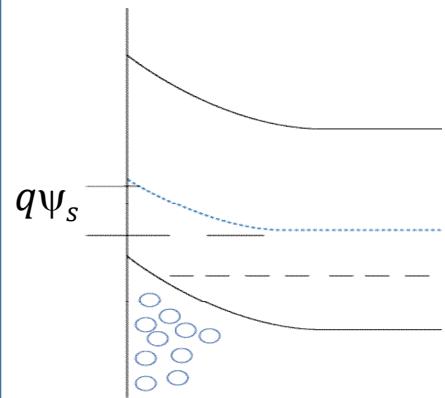
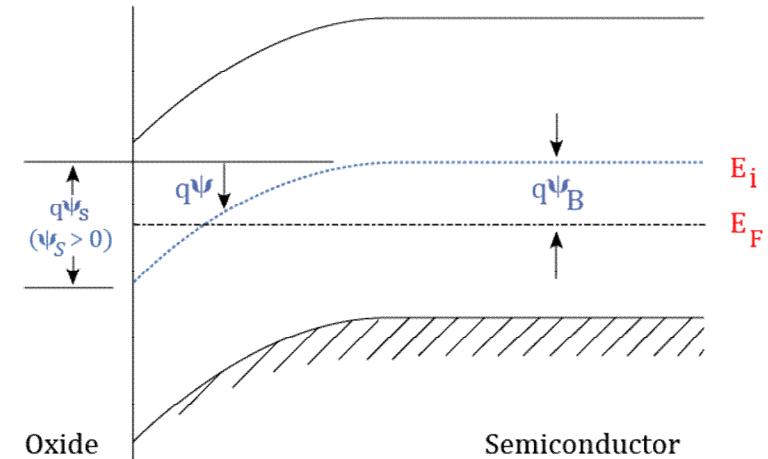


Fig 3.16a

Fig 3.16b

Fig 3.16c

Fig 3.16d

Summary

(e) $\psi_s > \psi_B$ **Inversion** (bands bend **downward**).

(f) $\psi_s = 2\psi_B$ (onset of **Strong inversion**)

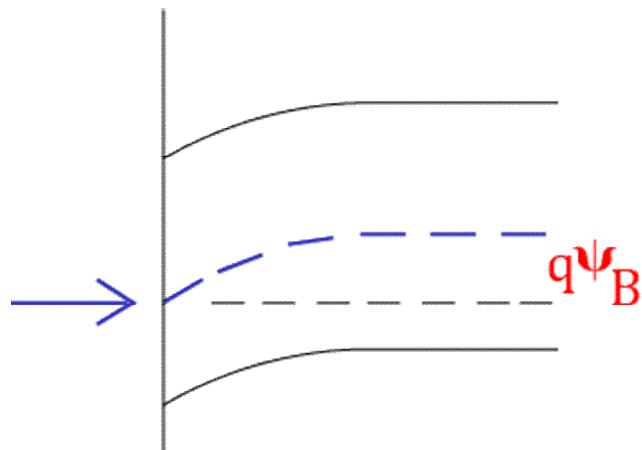


Fig 3.16e

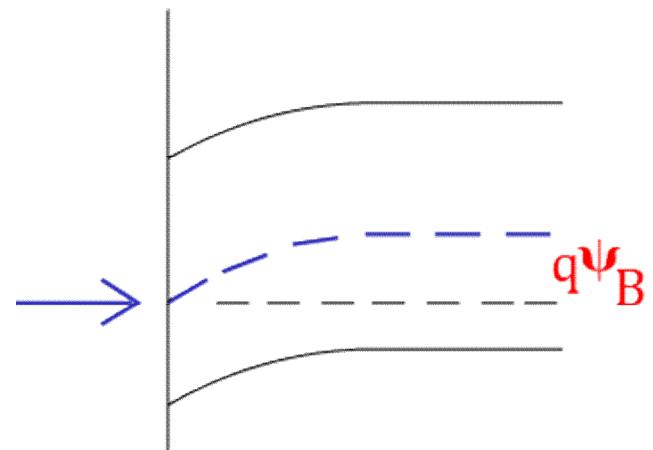


Fig 3.16f

Surface Depletion Region

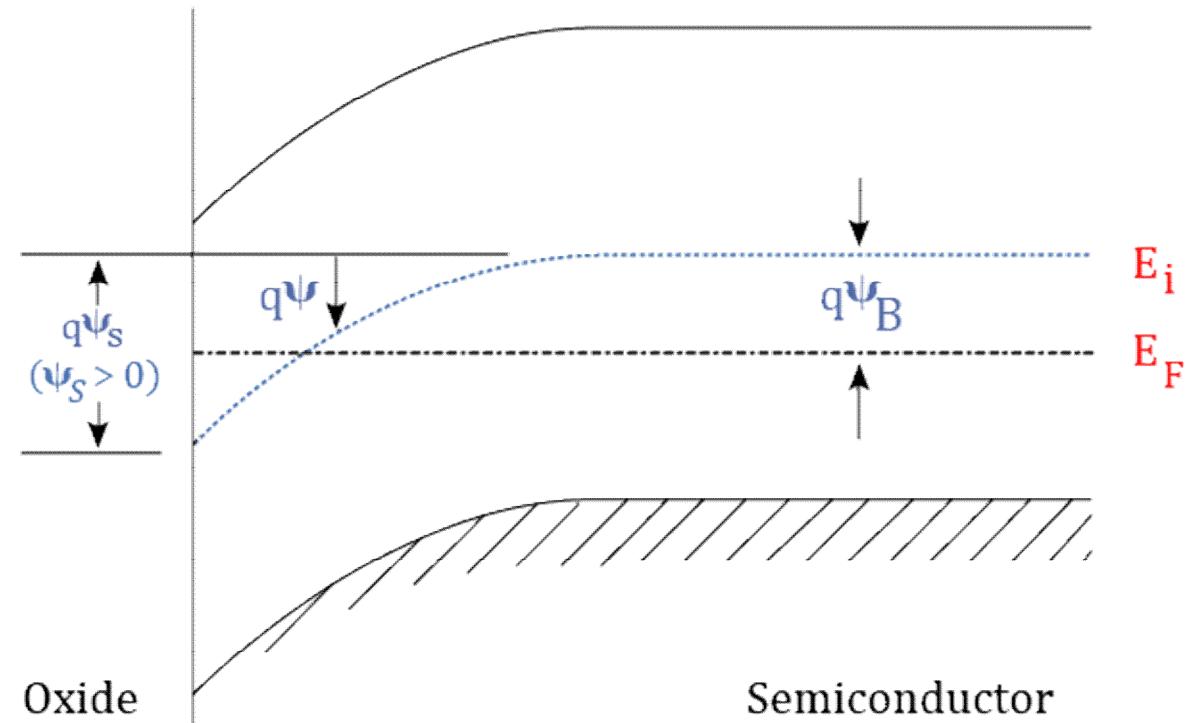
- ψ as a function of x can be obtained by solving one-dimensional **Poisson's** equation:

$$\frac{d^2\psi}{dx^2} = \frac{-\rho(x)}{\epsilon_s} \text{ where } \rho = -qN_A$$

- By integrating two times with boundary conditions, we have:

$$\psi = \psi_s(1 - \frac{x}{W})^2 \quad (\text{Equation 3.1})$$

$$\psi_s = \frac{qN_A W^2}{2\epsilon_s} \quad (\text{Equation 3.2})$$



Surface Depletion Region (Cont'd.)

- At onset of strong inversion, $\psi_s = 2\psi_B$ and the surface electron concentration:

$$n_p = n_i \exp\left(\frac{E_F - E_i}{kT}\right) = n_i \exp\left(\frac{q\psi_B}{kT}\right) = N_A \quad (\text{Equation 3.3})$$

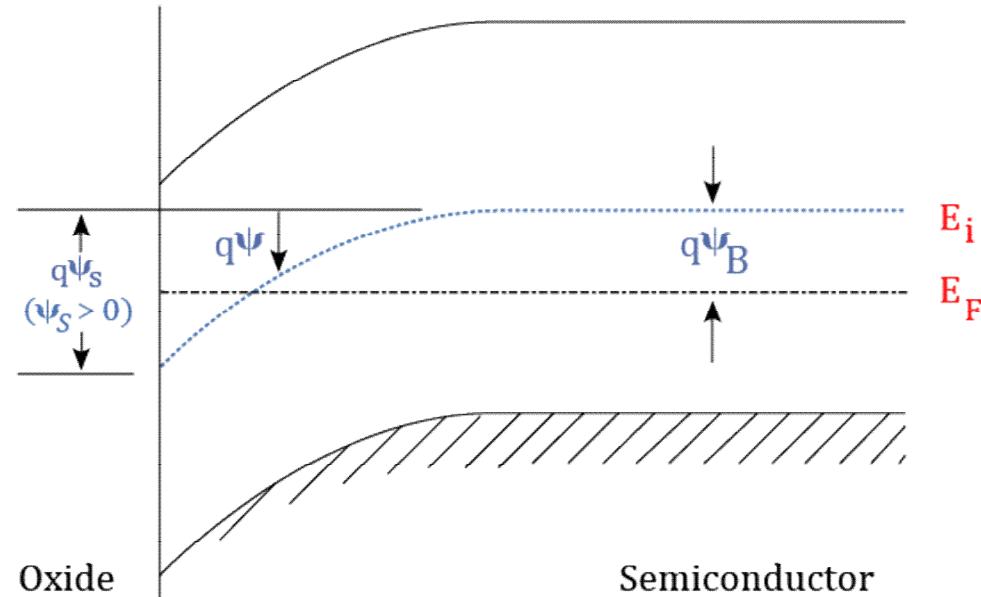
$$\psi_{s(\text{inv})} = 2\psi_B = \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right) \quad (\text{Equation 3.4})$$

- Maximum width of surface depletion layer, W_m :

$$W_m^2 = \frac{2\epsilon_s(2\psi_B)}{qN_A} = \frac{4\epsilon_s(kT)}{q^2N_A} \ln\left(\frac{N_A}{n_i}\right) \quad (\text{Equation 3.5})$$

$$W_m = \sqrt{\frac{2\epsilon_s(2\psi_B)}{qN_A}} = \sqrt{\frac{4\epsilon_s k T \ln\left(\frac{N_A}{n_i}\right)}{q^2 N_A}} \quad (\text{Equation 3.6})$$

and $Q_s = -qN_A W_m \approx -\sqrt{2q\epsilon_s N_A (2\psi_B)}$ *(Equation 3.7)*



Ideal MOS Capacitance

- The applied voltage V will drop across the oxide (V_o) and semiconductor (ψ_s):

$$V = V_o + \psi_s \quad (\text{Equation 3.8})$$

- Total capacitance C is a series combination of oxide capacitance C_o and depletion layer capacitance C_j , thus:

$$C = \frac{C_o C_j}{(C_o + C_j)} \text{ F.cm}^{-2} \quad (\text{Equation 3.9})$$

where $C_j = \epsilon_s / W$ (Equation 3.10)

and $C_o = \epsilon_{ox} / d$ (Equation 3.11)

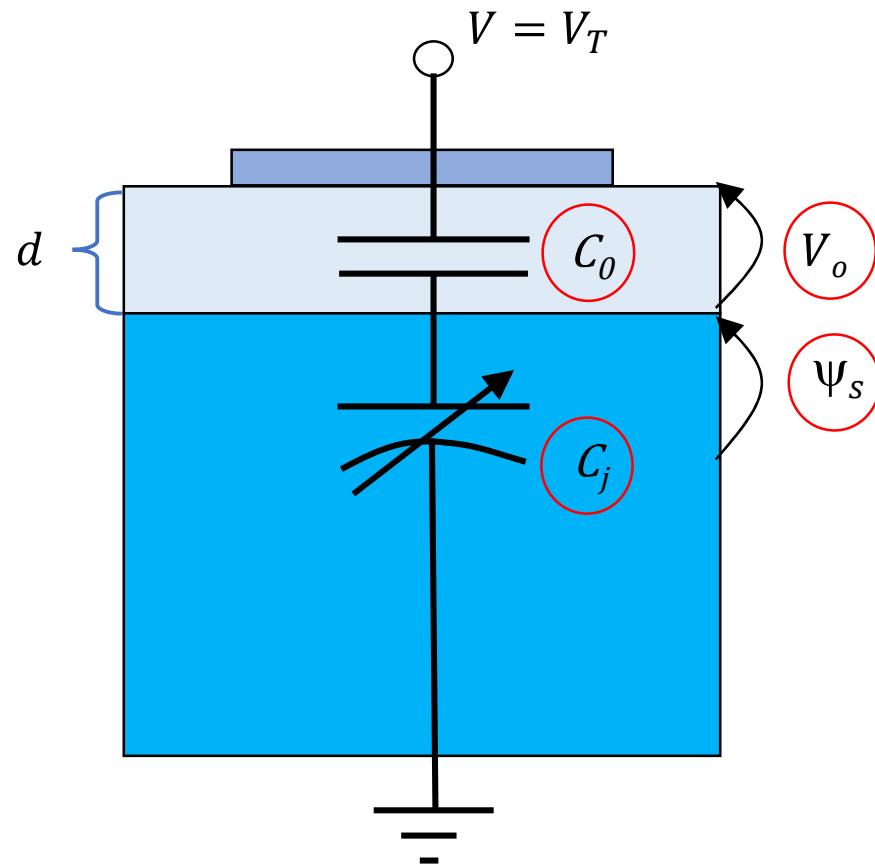


Figure 3.17

1. $V < 0$, Accumulation

Holes accumulate at semiconductor surface → no depletion in semiconductor ($C_j = \varepsilon_s/0 = \infty$).

$$C(\max) \approx C_0 = \frac{\varepsilon_{ox}}{d} = \text{constant} \quad [\text{line (1)}]$$

Derivation: $C = (C_0\infty)/(C_0 + \infty) = C_0\infty/\infty = C_0$

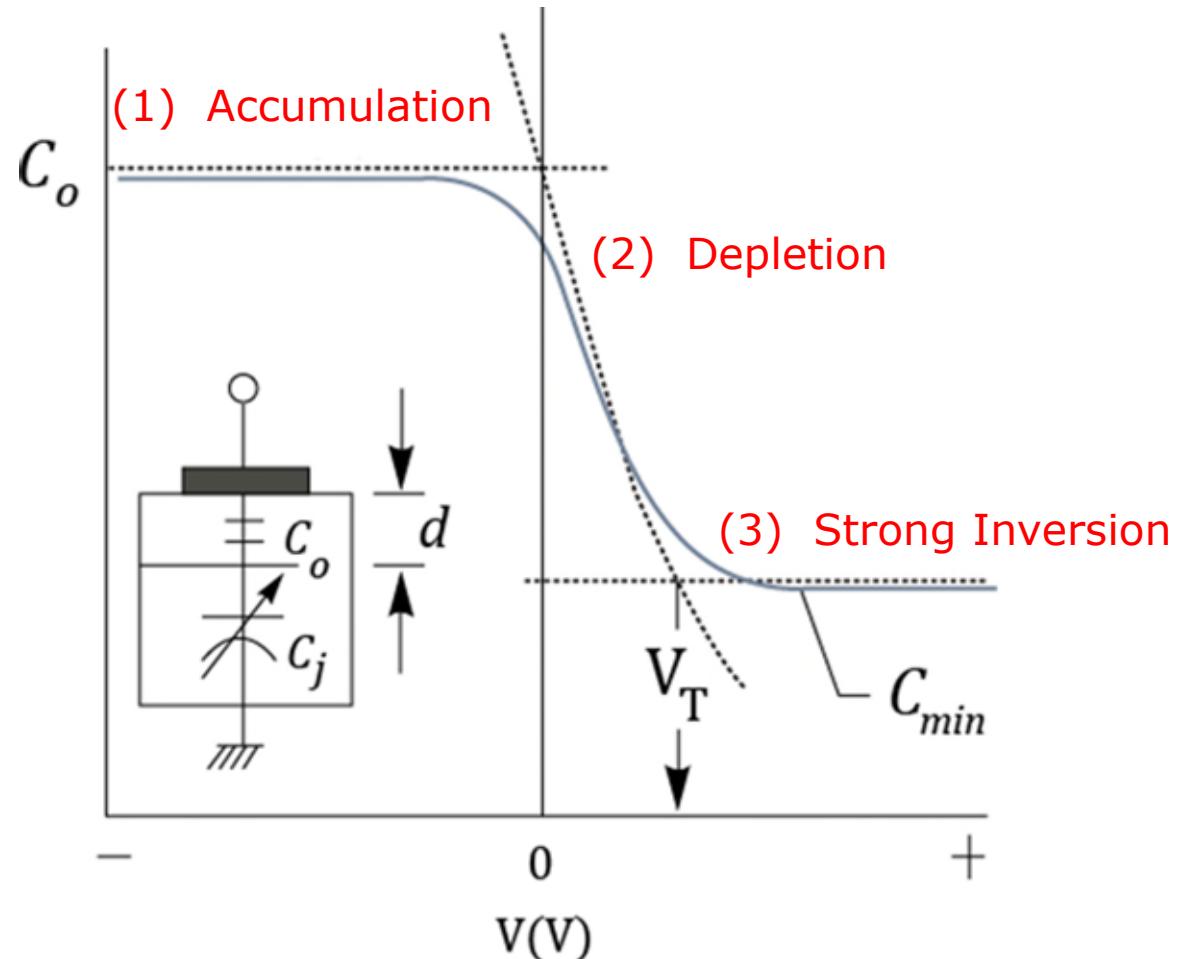


Figure 3.18

C-V Relation of Ideal MOS Capacitance (Cont'd.)

2. $V > 0$ (from $V=0$ to $V=V_T$), Depletion

- C drops with increase of voltage [line (2)].
- Using equations for ψ_s and W , we have:

$$\frac{C}{C_0} = \frac{1}{\sqrt{1 + \frac{2\varepsilon_{ox}^2 V}{qN_A \varepsilon_S d^2}}} \quad (\text{Equation 3.12})$$

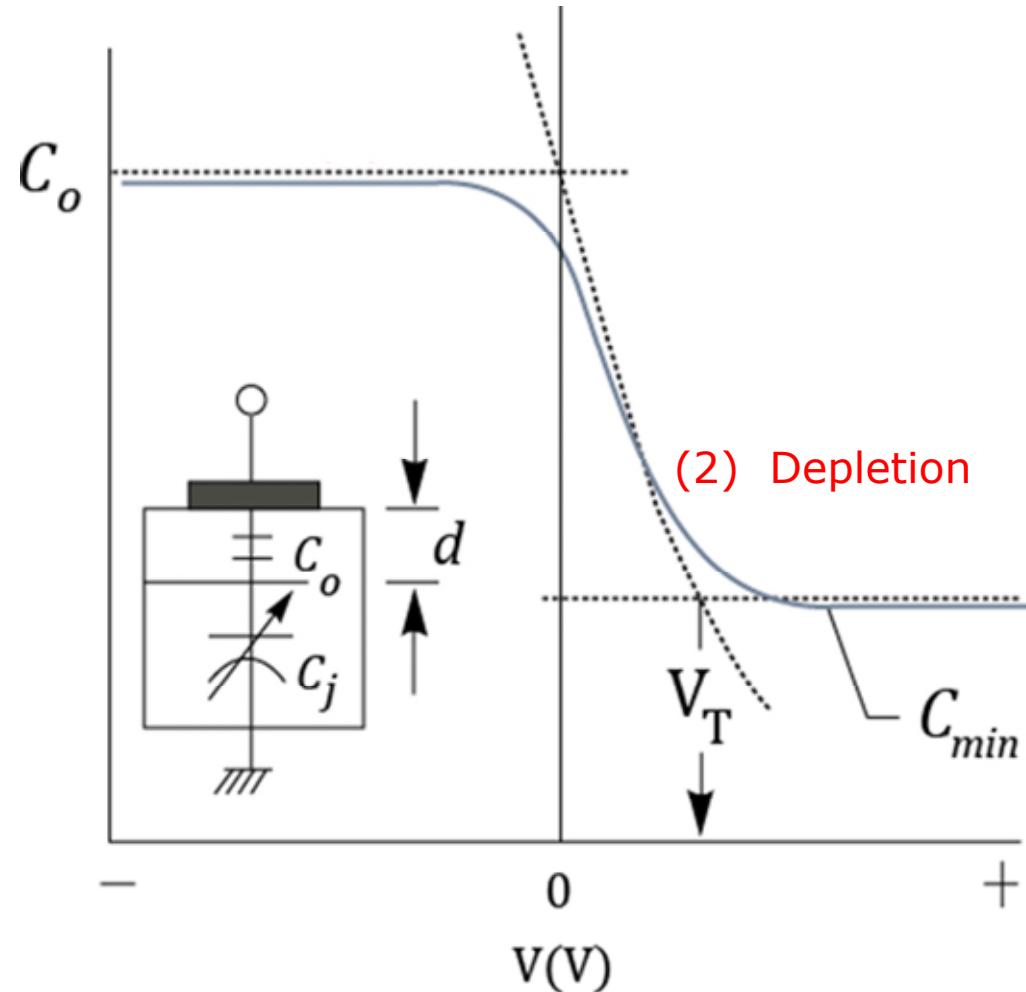


Figure 3.19

C-V Relation of Ideal MOS Capacitance (Cont'd.)

3. $V >> 0$ ($V > V_T$), Strong Inversion

- Depletion width will not increase once reaching a maximum.
- Thus,

$$C_0 = \epsilon_{ox}/d \text{ and}$$

$$C_j = \epsilon_s/W_m$$

- The total C will then remain at minimum [line (3)]:

$$C(\min) = \frac{C_0 C_j}{C_0 + C_j} = \frac{\epsilon_{ox}}{d + (\epsilon_{ox}/\epsilon_s)W_m} \quad (\text{Equation 3.13})$$

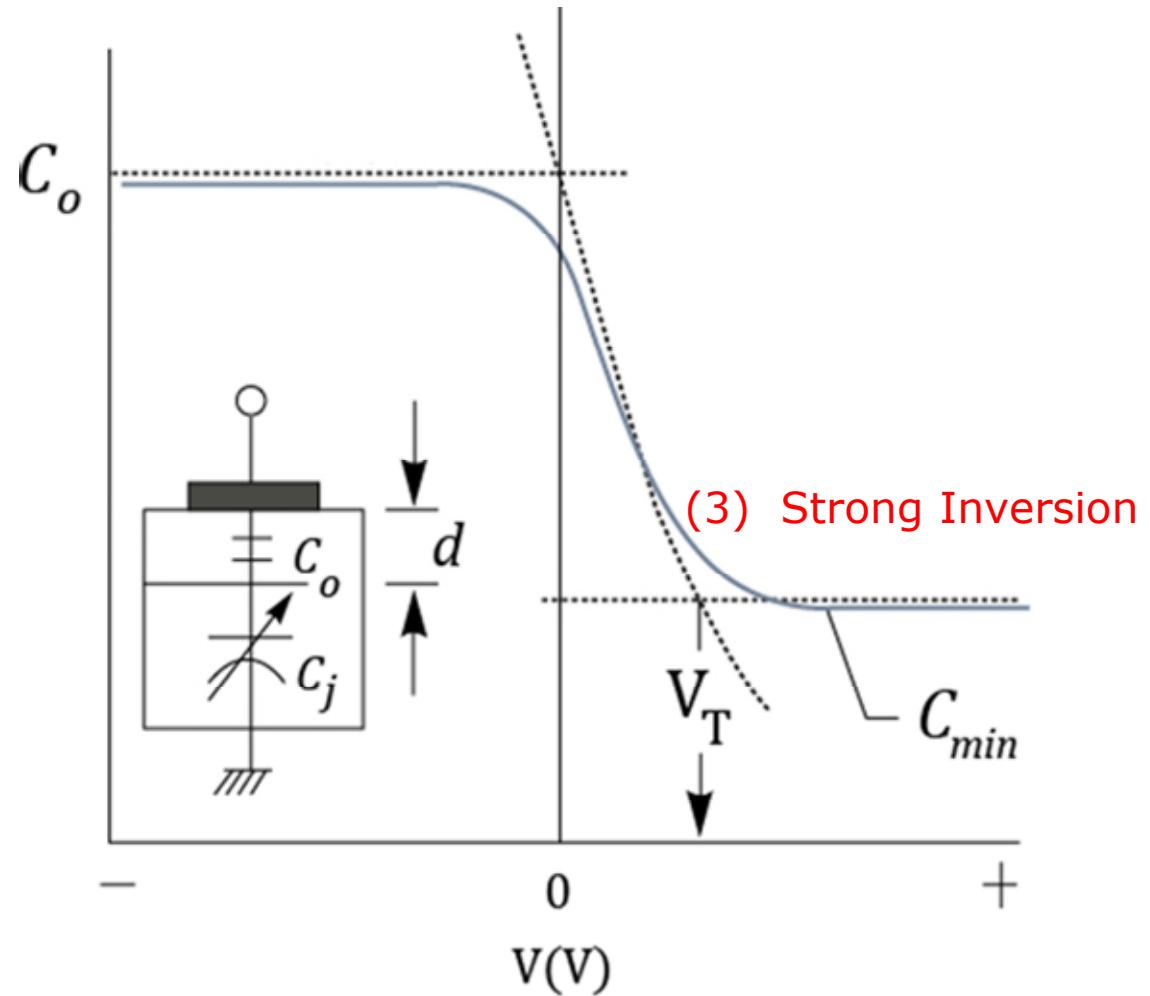


Figure 3.20

Threshold Voltage V_T

- The threshold voltage V_T at the onset of **strong inversion** is given by:

$$V_T = V_o + 2\Psi_B \quad (\text{Equation 3.14})$$

where $V_o = Q_s/C_o$ and $C_o = \epsilon_{ox}/d$

Neglect the inversion layer charge (Q_n)

- $Q_s = -qN_A W_m \cong -\sqrt{2q\epsilon_s N_A (2\Psi_B)} \quad (\text{Equation 3.15})$

- Therefore $V_T = \frac{qN_A W_m}{C_o} + 2\Psi_B = \frac{\sqrt{2\epsilon_s q N_A (2\Psi_B)}}{C_o} + 2\Psi_B \quad (\text{Equation 3.16})$

- Recall that at strong inversion: $\psi_{s(inv)} = 2\Psi_B = \frac{2kT}{q} \ln \left(\frac{N_A}{n_i} \right)$

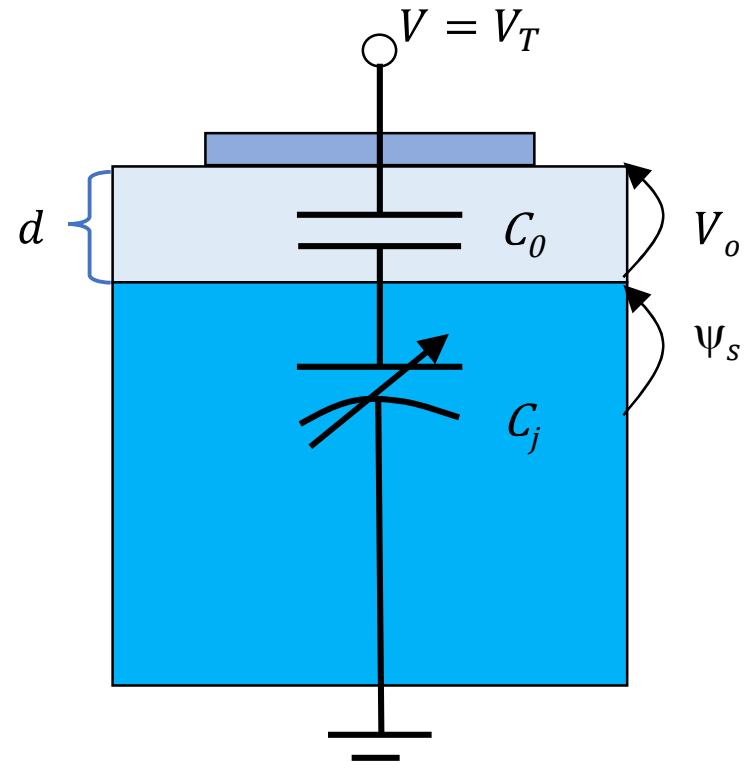


Figure 3.21

Metal – SiO₂ – Si MOS Diode

- Of all MOS diodes, the metal – SiO₂ – Si diode is the most extensively studied one.
- However, for commonly used metal electrodes, the work function difference $q\phi_{ms}$ is generally not zero (**therefore not ideal**).
- There are also various charges **inside** the oxide or at the SiO₂-Si **interface** that make the diode deviate from ideal behavior.

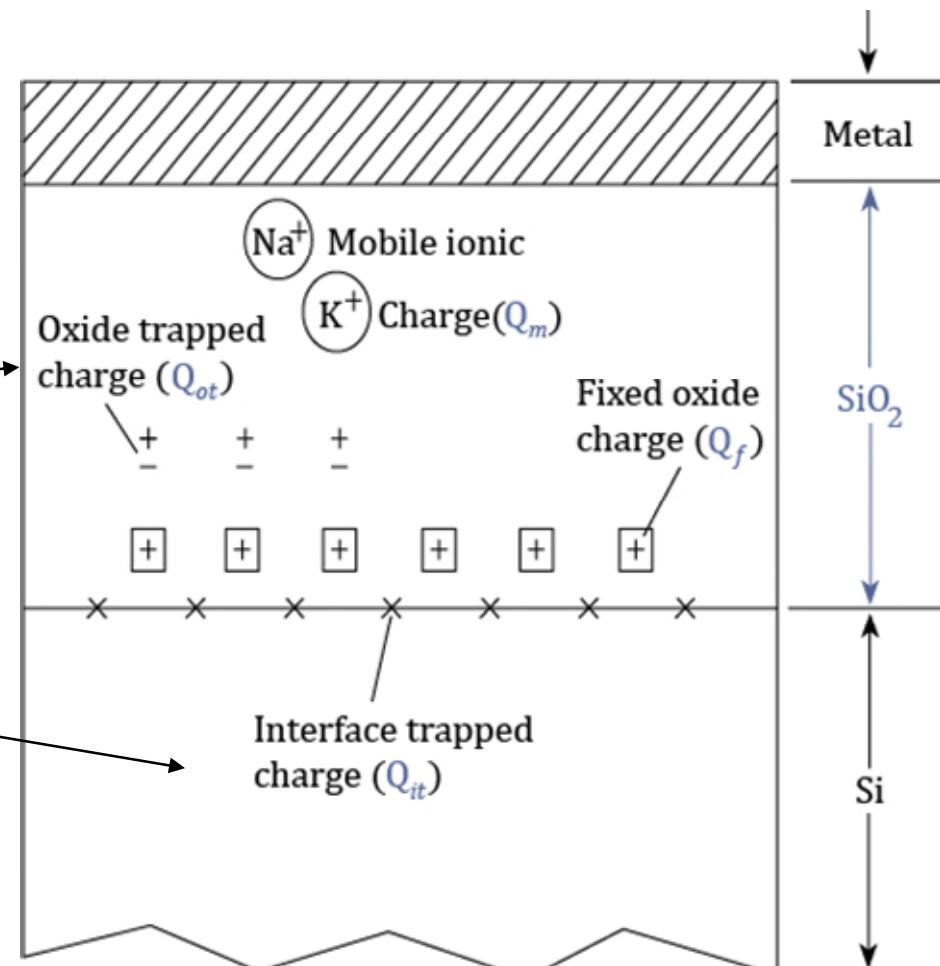
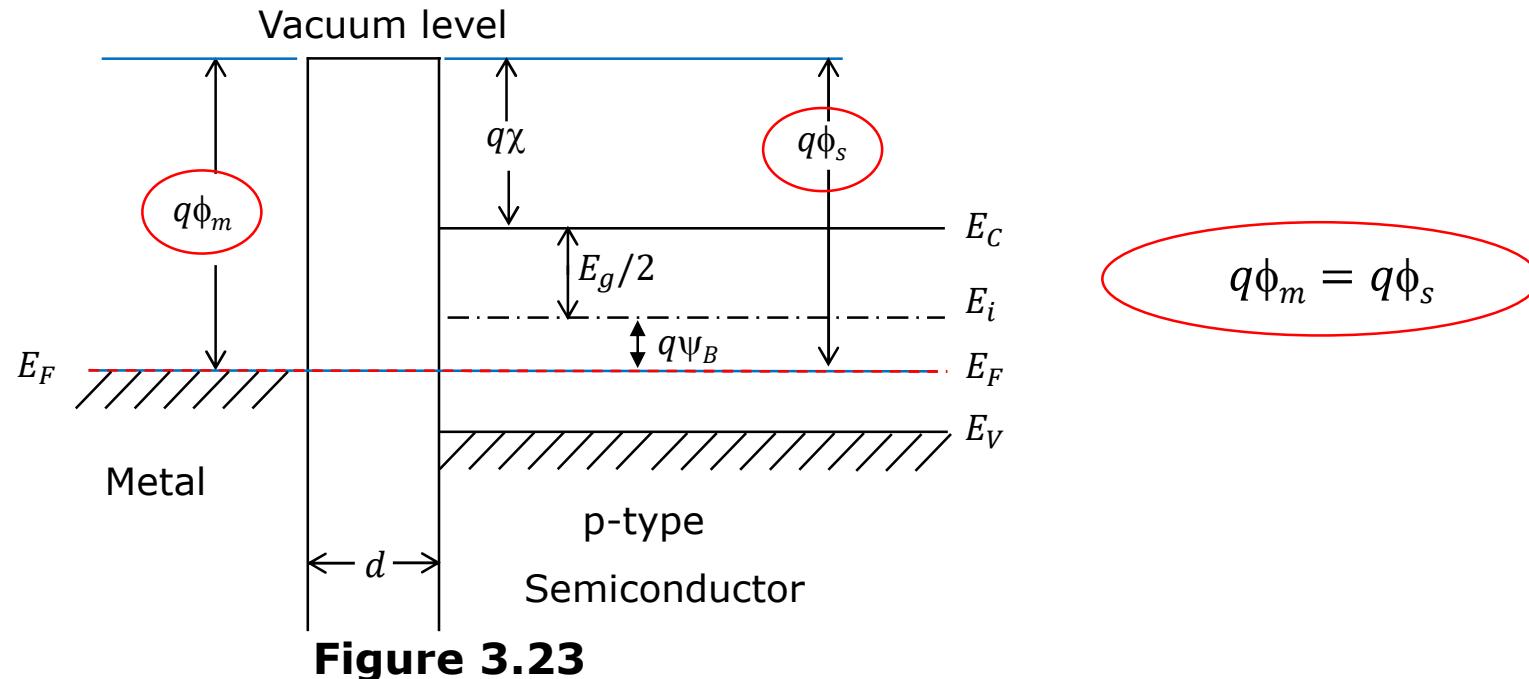


Figure 3.22

Recall for an Ideal MOS Diode

- The band diagram with p-type Si at V=0



where, $q\phi_m$: Metal work function (energy difference between Fermi level and vacuum level)

$q\phi_s$: Semiconductor work function

$q\chi$: Electron affinity (energy difference between E_C and vacuum level)

$q\psi_B$: Energy difference between Fermi level E_F and E_i

Non-ideal MOS Diode - Work Function Difference

The work function difference $q\phi_{ms}$ can vary over a 2 eV range depending on the electrode material and Si doping concentration.

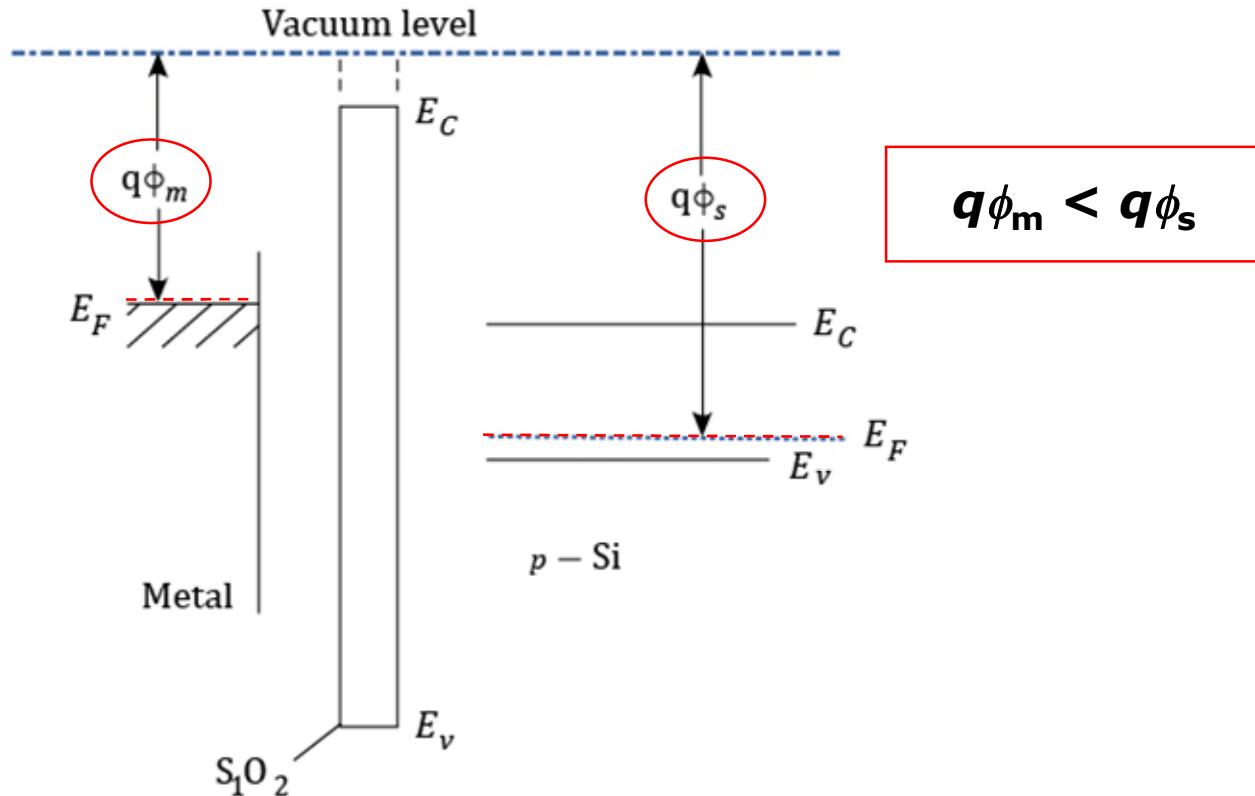


Figure 3.24a Before contract

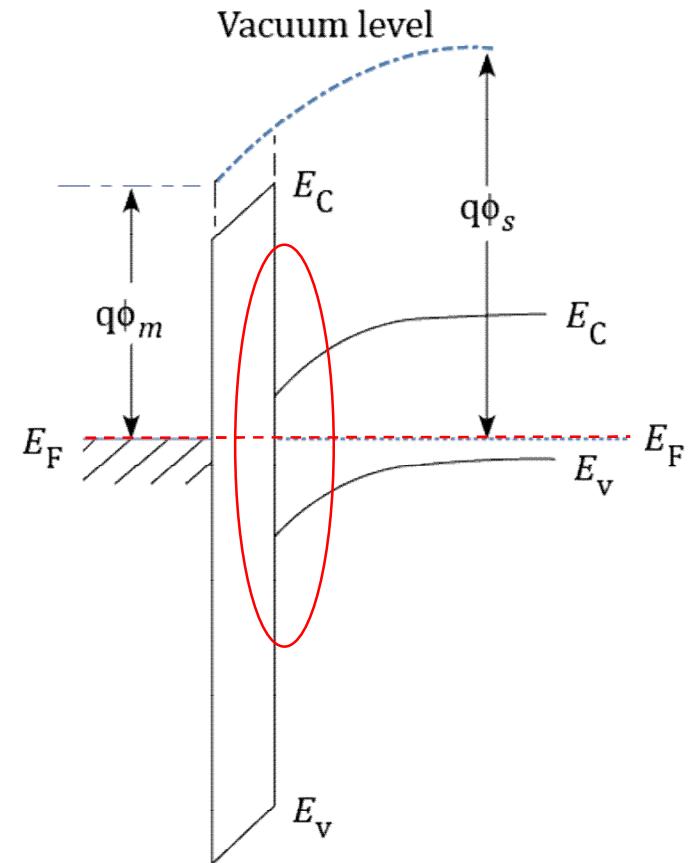


Figure 3.24b After contract

Flat Band Voltage for Work Function Difference

- To achieve ideal flat band condition, we must apply a **negative voltage**, called the **flat band voltage**:

$$V_{FB} = \phi_{ms} = \phi_m - \phi_s \quad (\text{Equation 3.17})$$

- V_T , the threshold voltage for the onset of strong inversion, for SiO_2 – Si MOS needs to add V_{FB} .

$$V_T = \frac{qN_A W_m}{C_o} + 2\psi_B + \phi_{ms} \quad (\text{Equation 3.18})$$

Interface Traps and Oxide Charges

The practical MOS diode is affected by charges in the oxide and traps at the interface (four kinds of charges).

1. Interface trapped charges Q_{it}

- Charges located at the Si-SiO₂ interface
- Due to the chemical composition at interface (**dangling bonds**)

2. Fixed oxide charges Q_f

- Due to unused silicones in oxidation located at or near the interface as a sheet charge
- Usually carry positive charge

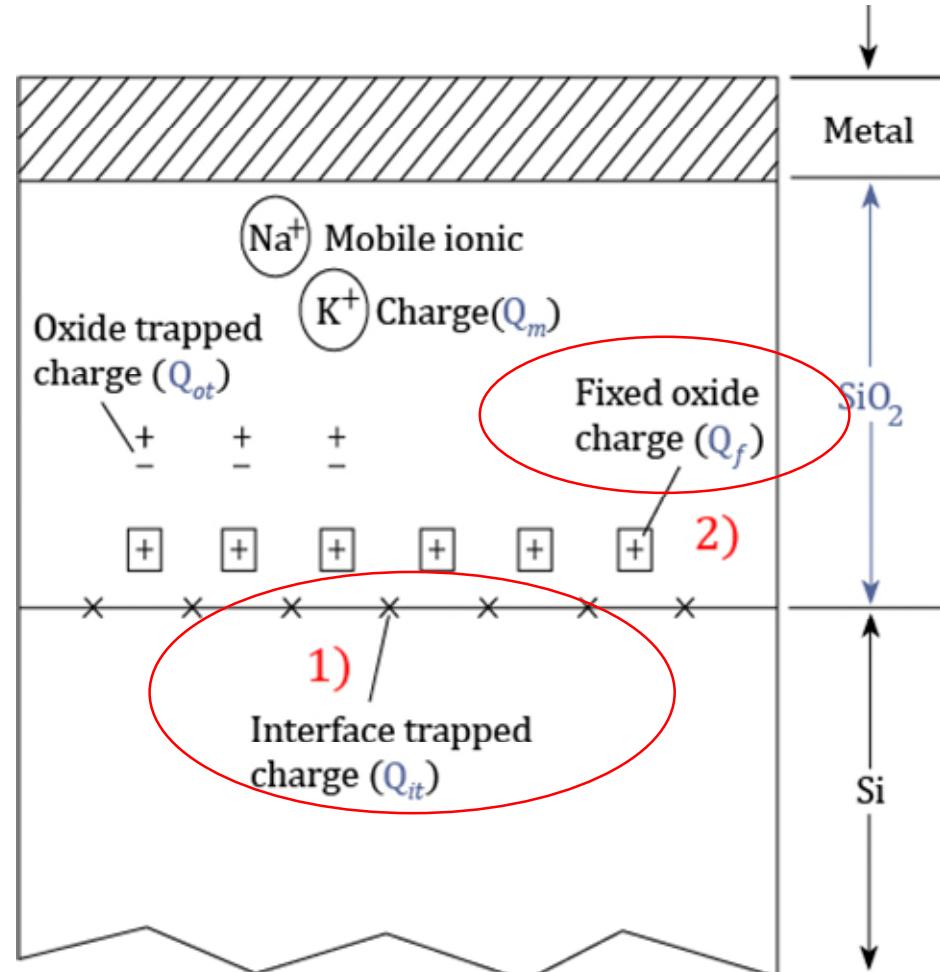


Figure 3.25

Interface Traps and Oxide Charges (Cont'd.)

3. Oxide trapped charges Q_{ot}

- Defects
- Can be created by x-ray or high energy electron bombardment
- Distributed inside oxide
- Most of it can be removed by annealing

4. Mobile ionic charges Q_m

- Alkali ions like sodium
- Mobile at $T > 100^\circ C$ and high electric field
- Can cause shift of C-V curve along V axis

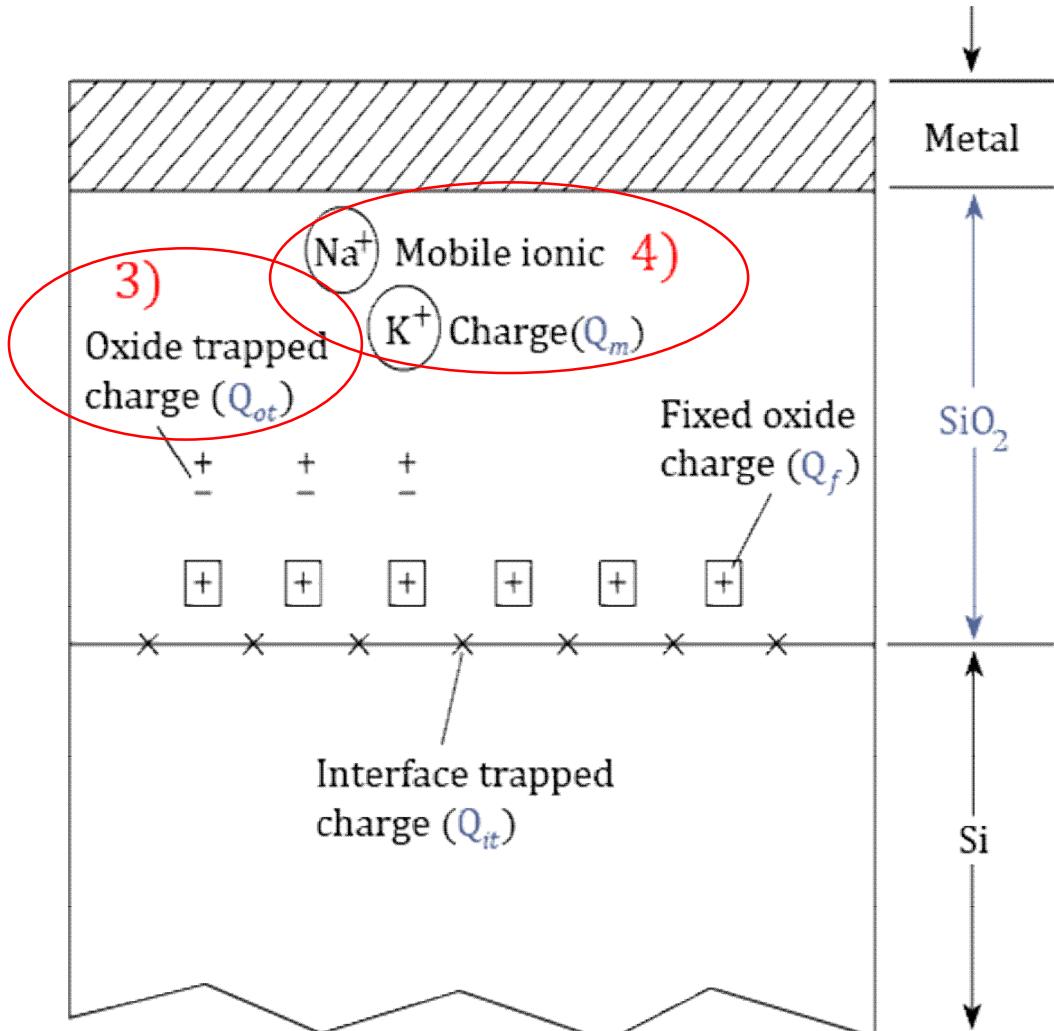


Figure 3.26

Effects of Traps and Charges

- Assume the oxide charges Q_o (namely Q_f , Q_m , Q_{ot}) carry positive charges. They will induce negative charges in both metal and Si.

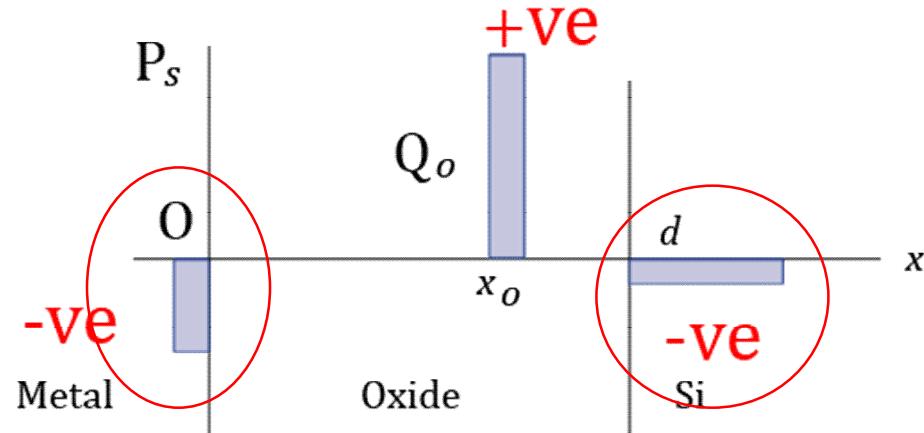


Figure 3.27

- The negative charges in Si will cause an electrical field in Si (as well as energy band bending).

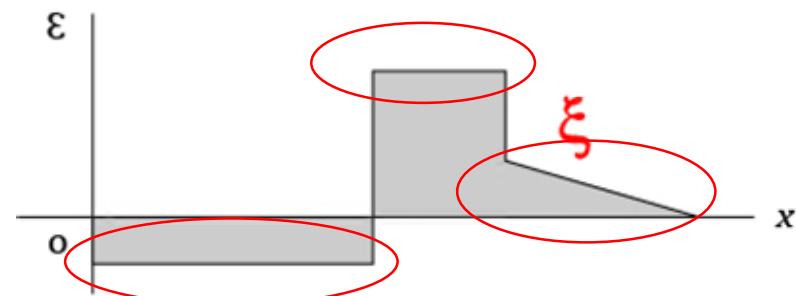


Figure 3.28

Effects of Traps and Charges (Cont'd.)

- To remove the negative charges in Si and realise the flat band, one needs to increase the overall negative value of V_{FB} .

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_o} \quad (\text{Equation 3.19})$$

- In this case, all the negative charges corresponding to Q_o will be in metal surface.

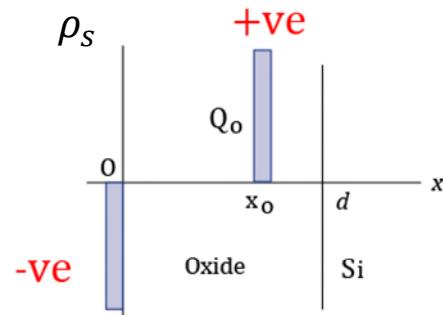


Figure 3.29

- All the electrical field will be in the oxide between metal and x_o (nothing in Si).

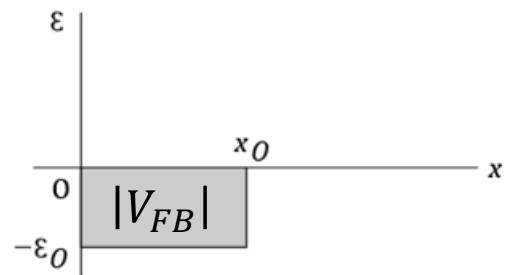


Figure 3.30

Effects on C-V Curve

- By adding the effect of the charges and traps in V_{FB} , the V_T for the $\text{SiO}_2\text{-Si}$ MOS diode becomes

$$V_T = \frac{N_A W_m}{C_o} + 2\psi_B + \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_o} \quad (\text{Equation 3.20})$$

- The effect is to shift the C-V curve **to the left** by an amount equal to the magnitude of V_{FB} .

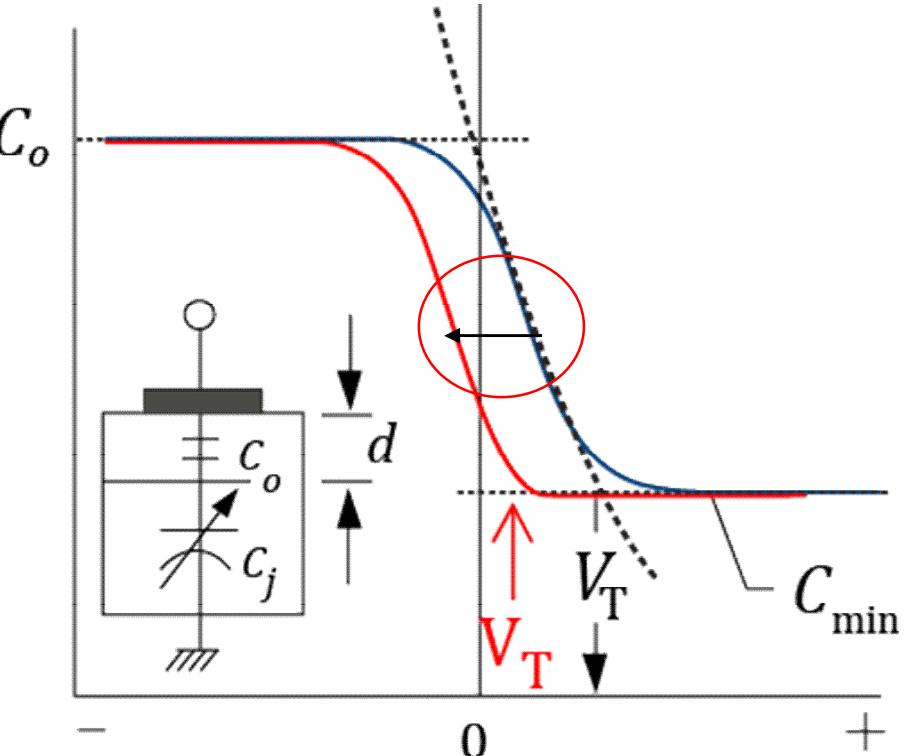
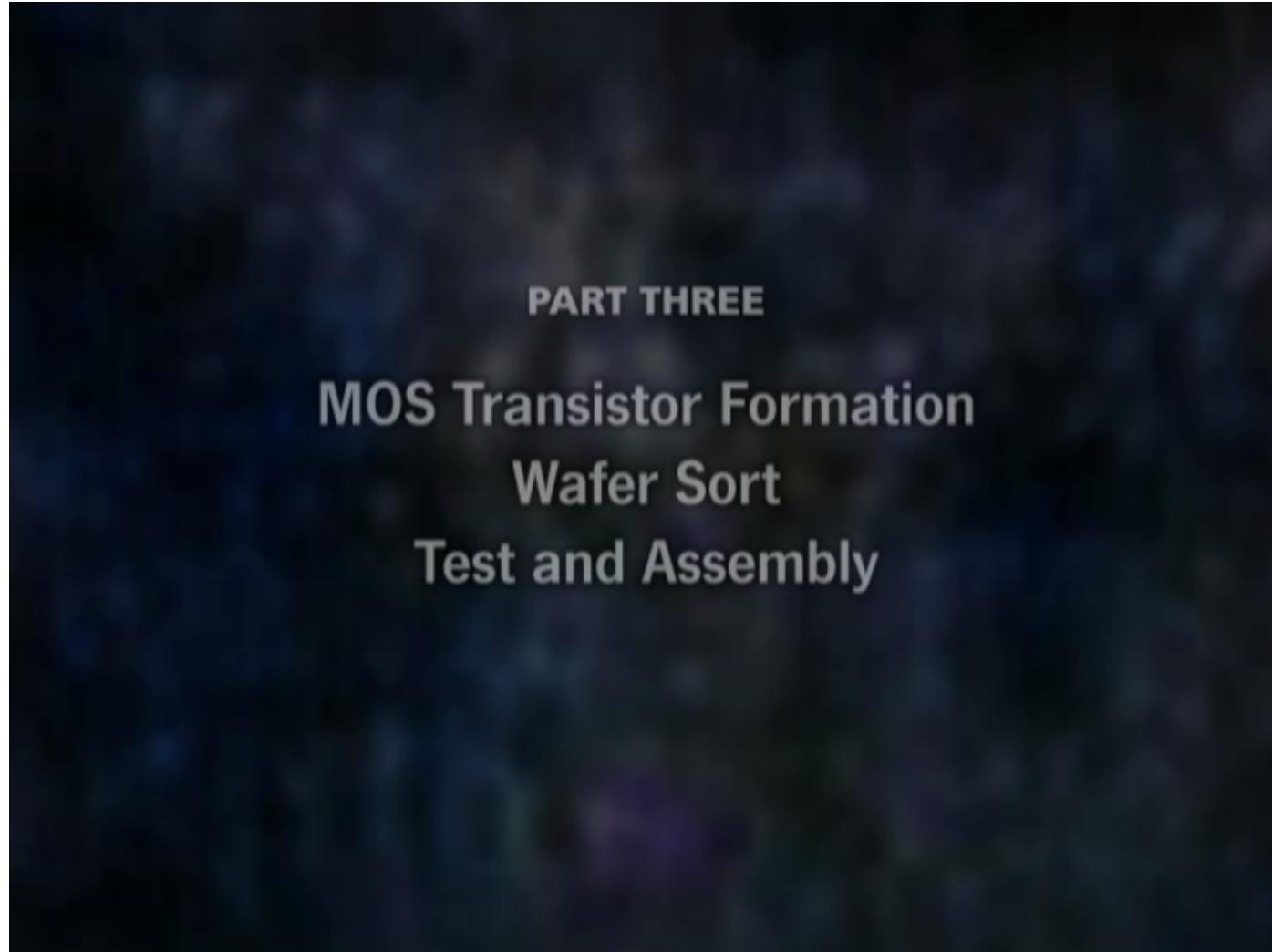


Figure 3.31

- Blue curve: For ideal MOS diode
- Red curve: With work function difference and charges



Structure of an n-channel MOSFET (NMOSFET)

- Gate length: L
- Gate width: Z
- Gate oxide thickness: d

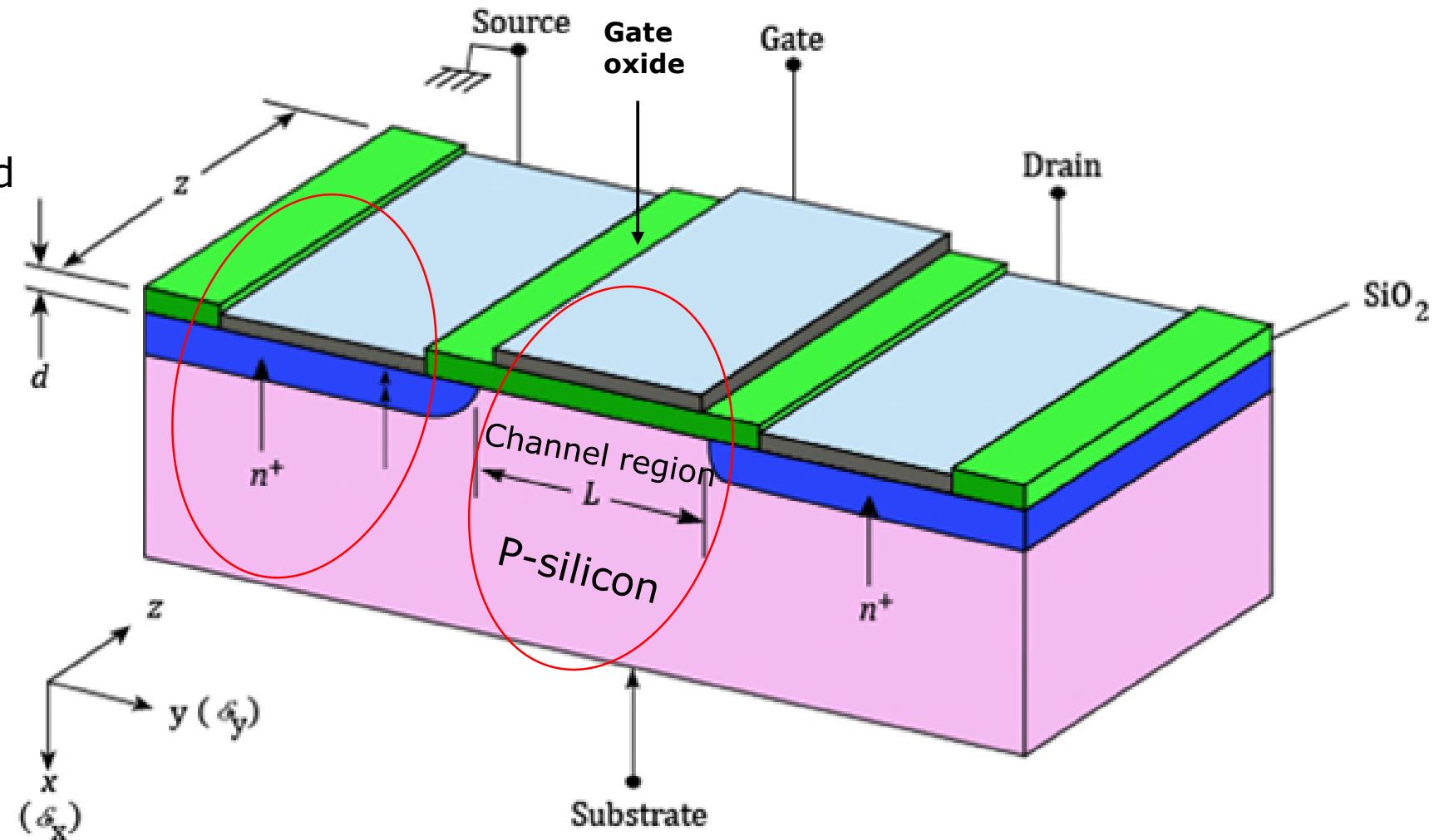


Figure 3.32

Energy Band Diagrams of an NMOSFET

Energy band diagram at z and y directions at thermal equilibrium.

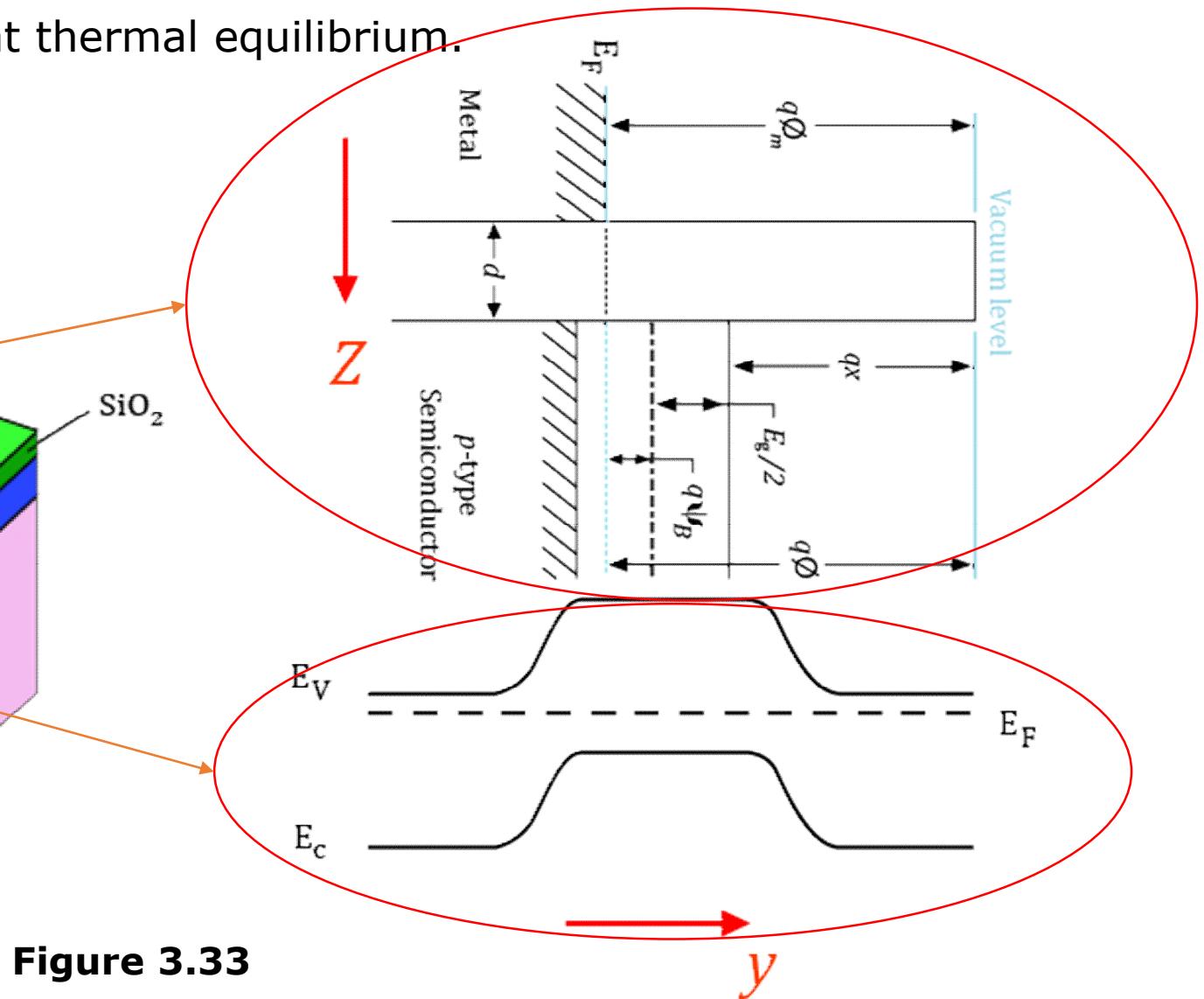
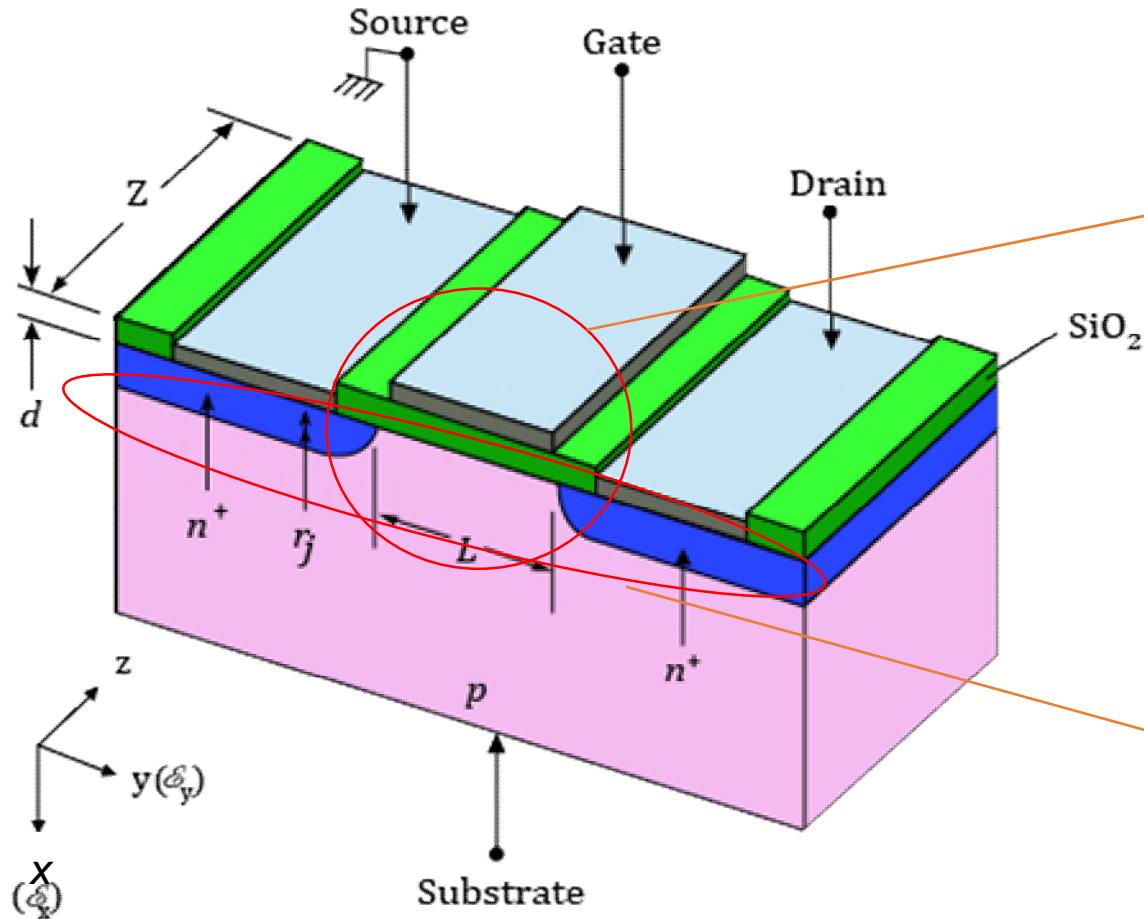


Figure 3.33

MOSFET Operation (Cut-off region)

- Source is grounded. V_G and V_D can be applied.
- When $V_G > 0$ but $< V_T$, (V_T is the threshold voltage to cause inversion):
 - No channel is formed (**cut-off**).
 - The maximum drain current is the reverse leakage current of a p-n junction.

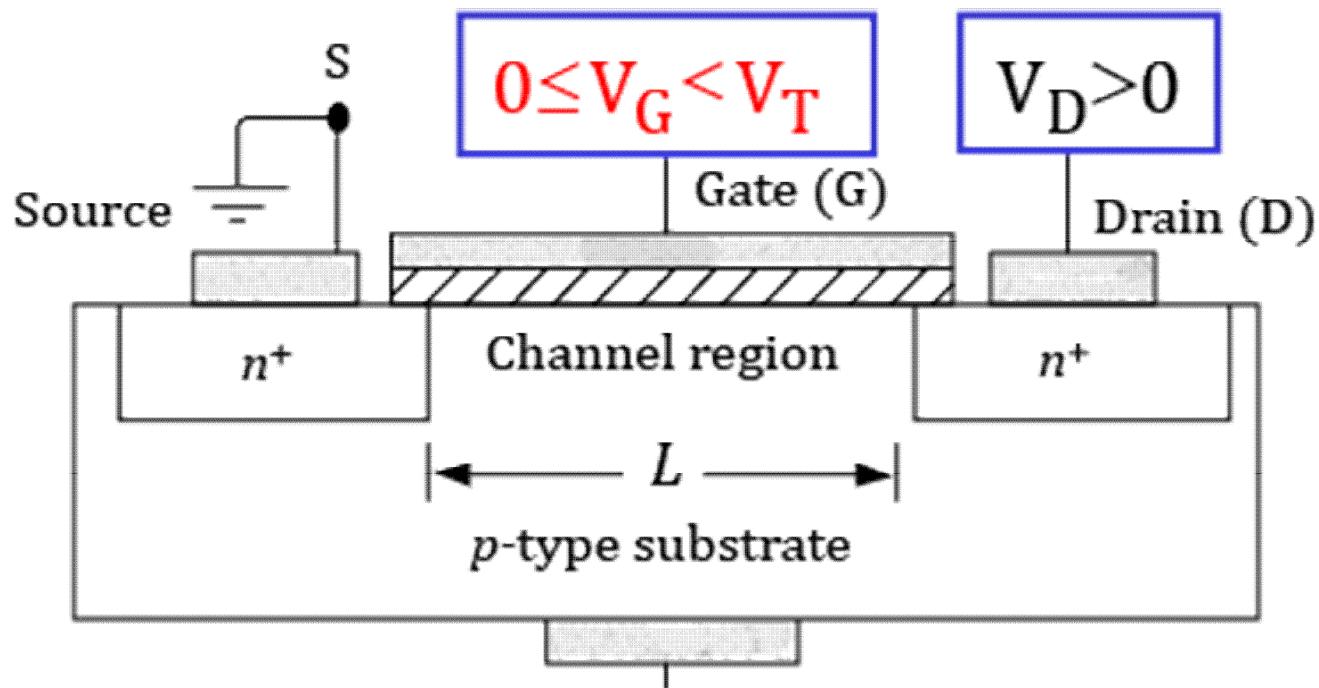


Figure 3.34

MOSFET Operation (cont'd)

- When $V_G \geq V_T$,
 - A channel (inversion) is formed by electrons.
 - There will be a drain current with the magnitude related to V_D .

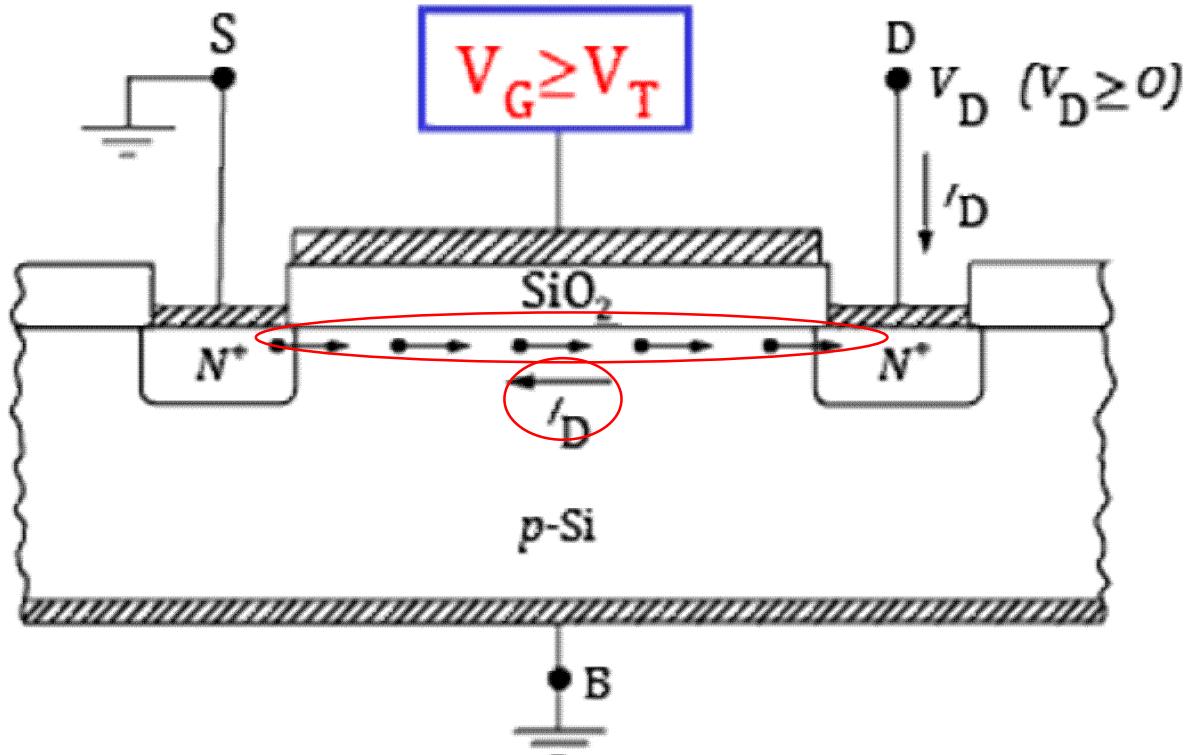


Figure 3.35

MOSFET Operation (Linear Region)

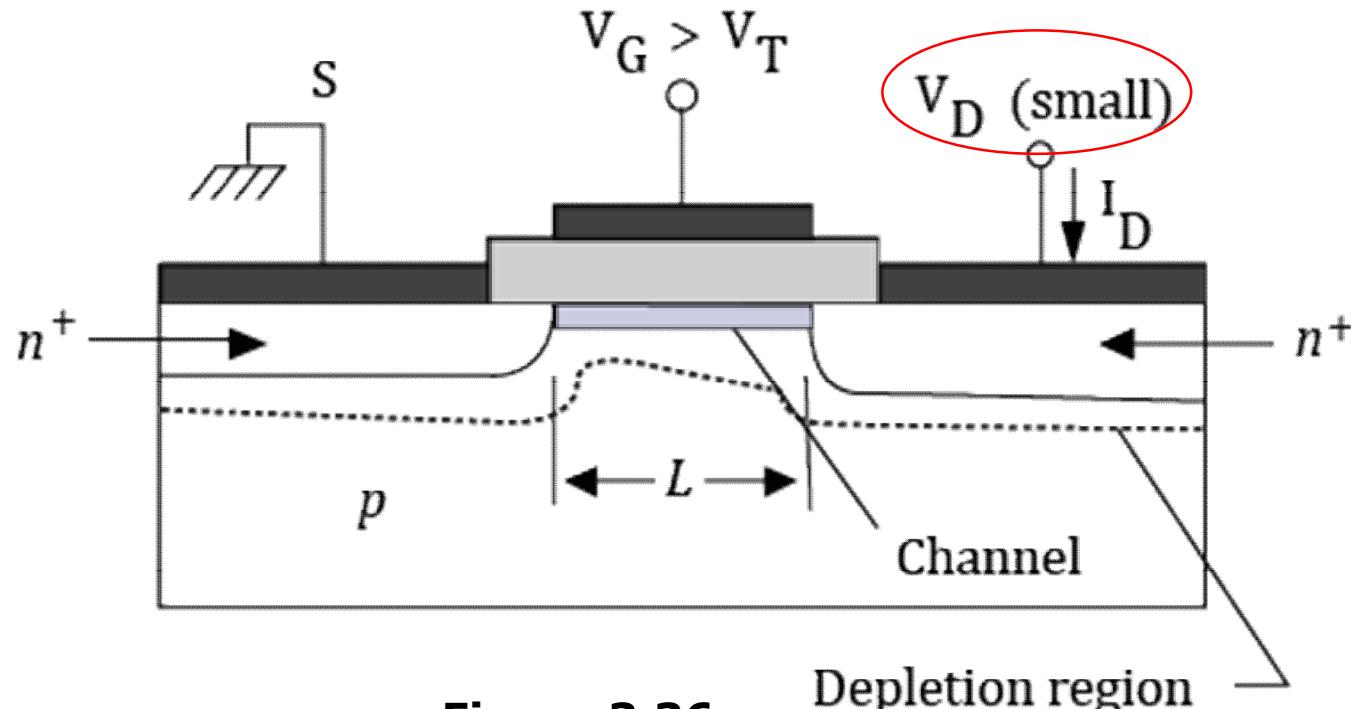


Figure 3.36

Depletion region

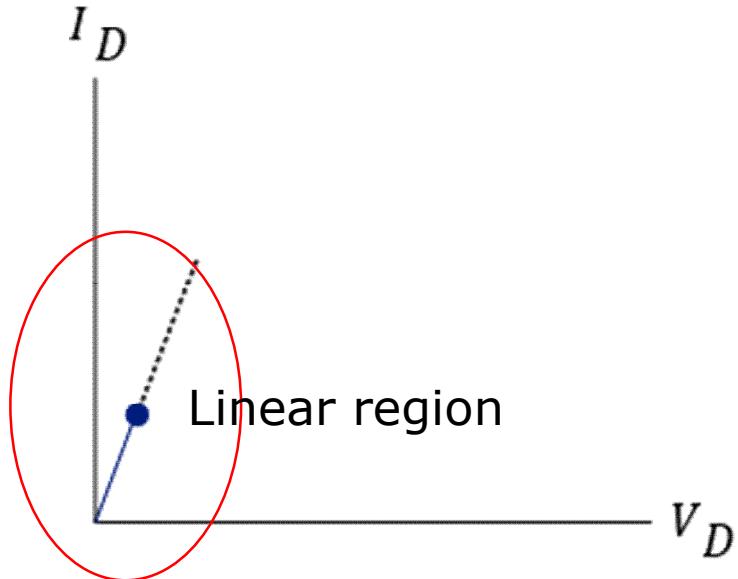


Figure 3.37

- When a small drain voltage ($V_D < V_{GS} - V_T$) is applied, the electrons in the channel will flow from source to drain. So the drain current I_D is from drain to source.
- The drain current is proportional to V_D . That is, $I_D = \frac{V_D}{R}$ (*Ohm's Law*)
- The channel can be treated as a resistor R with a length L .

MOSFET Operation (Pinch-off Point)

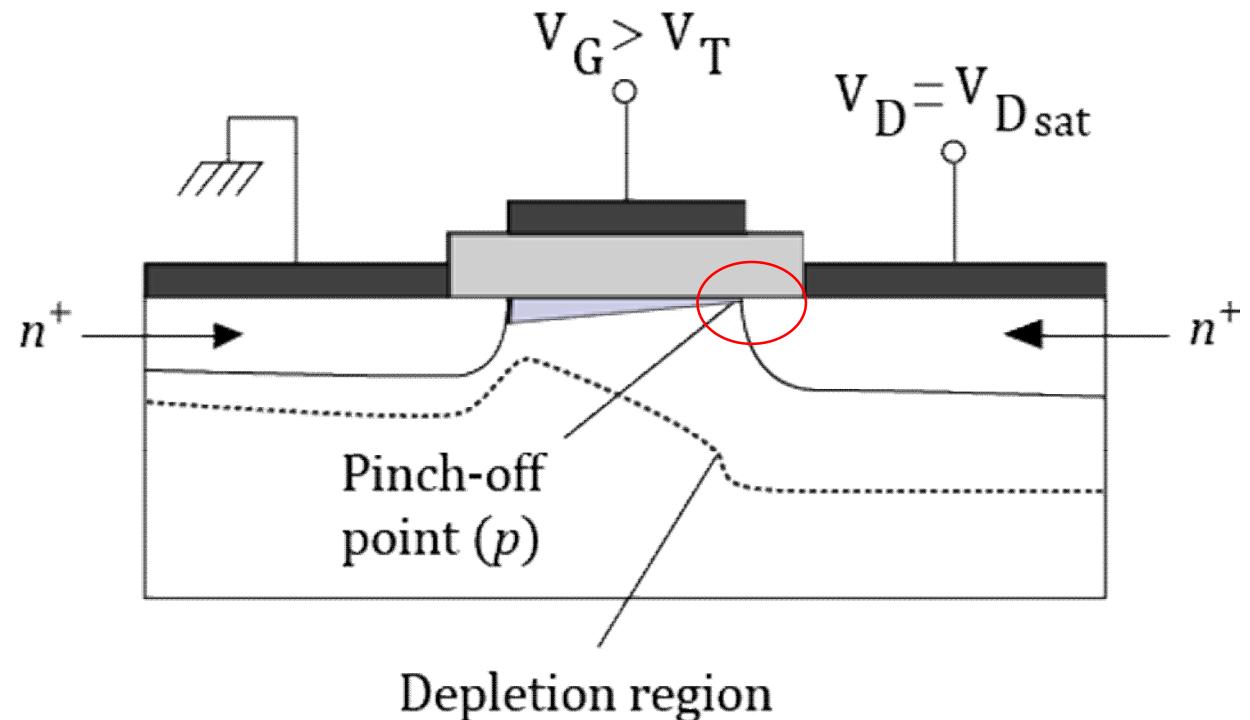


Figure 3.38

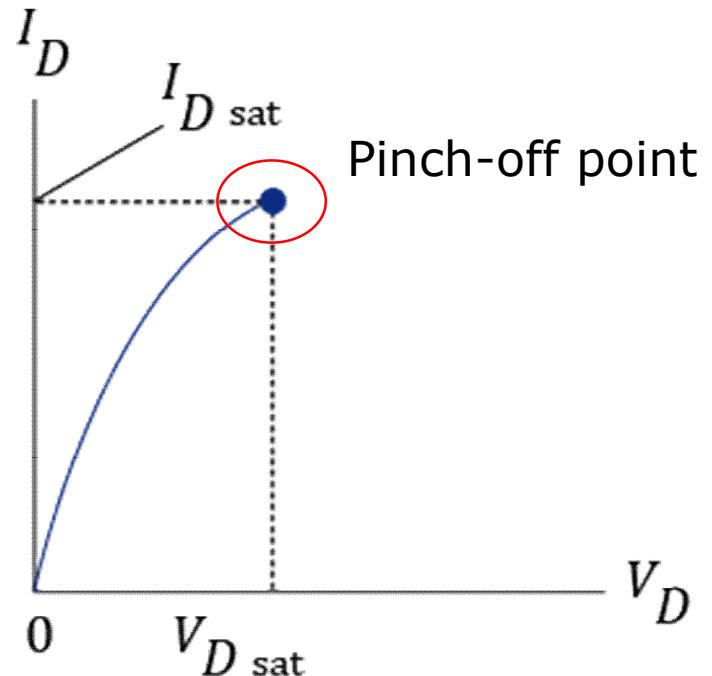


Figure 3.39

- When the drain voltage reaches a value $V_{D\text{sat}}$ or ($V_D = V_{GS} - V_T$), the thickness of the inversion layer at the end of channel L becomes **ZERO**; this is called the **pinch-off point** which is the **onset of saturation region**.
- The drain current reaches a saturation value $I_{D\text{sat}}$ at $V_{D\text{sat}}$.

MOSFET Operation (Saturation Region)

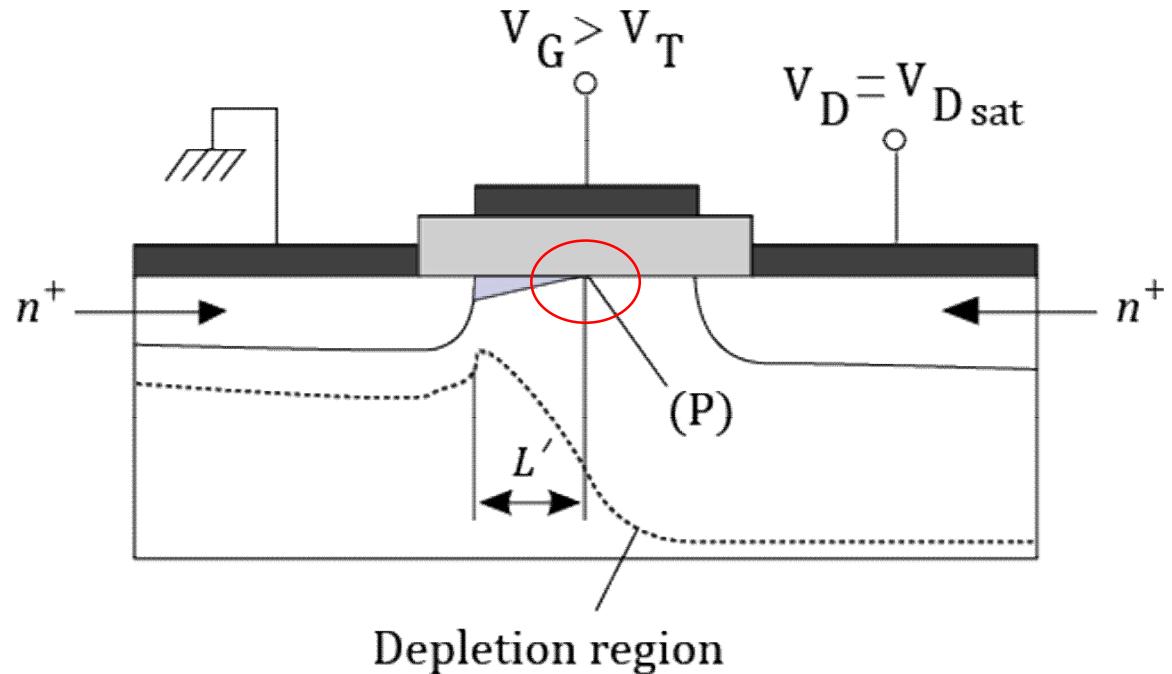


Figure 3.40

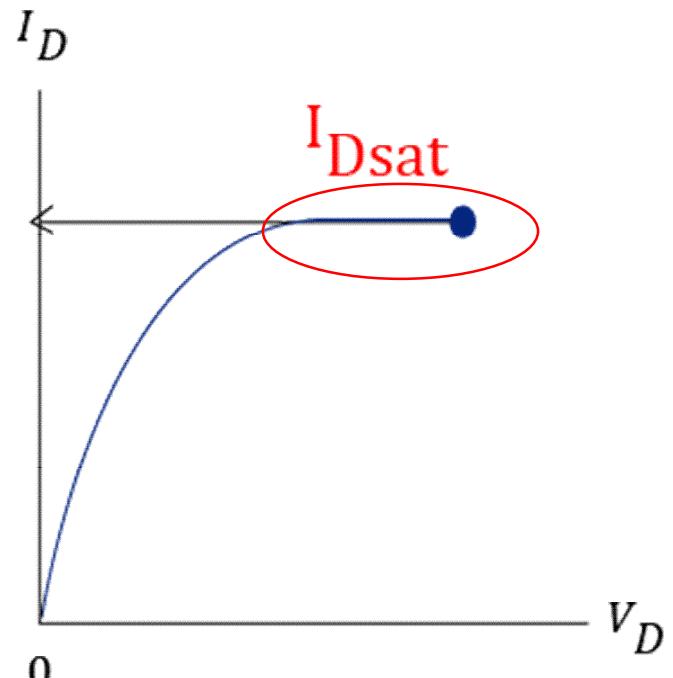


Figure 3.41

- When the drain voltage increases further ($V_D > V_{D_{sat}}$), the pinch-off point moves towards the source (wider depletion).
- Channel becomes shorter (L becomes L').
- The drain current remains the same as $I_{D_{sat}}$ (**Why?** Think about the emitted carriers in base to across b-c junction).

I-V Behavior of an NMOSFET

1. Cut-off region:

$$I_D = 0 \text{ for } V_{GS} \leq V_T$$

2. Linear (Triode) region:

$$I_D = K_n [(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \quad (\text{Equation 3.21})$$

$$\text{for } V_{DS} \leq V_{GS} - V_T$$

3. Saturation region:

$$I_D = \frac{K_n}{2} (V_{GS} - V_T)^2 \quad (\text{Equation 3.22})$$

$$\text{for } V_{DS} \geq V_{GS} - V_T$$

$$K_n = \mu_n C_{ox} (Z/L)$$

and

$$V_T = \frac{qN_A W_m}{C_o} + 2\psi_B = \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_o} + 2\psi_B$$

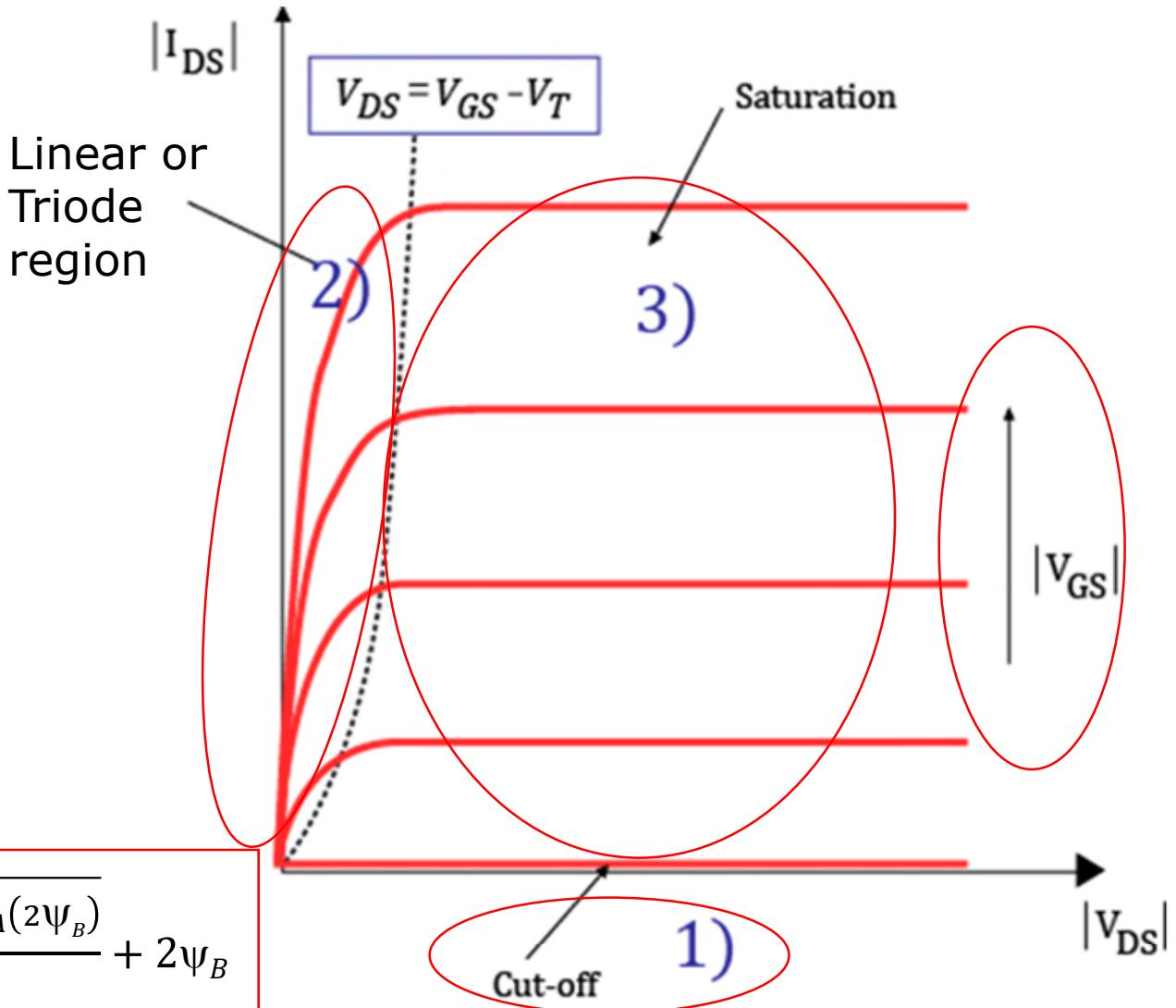
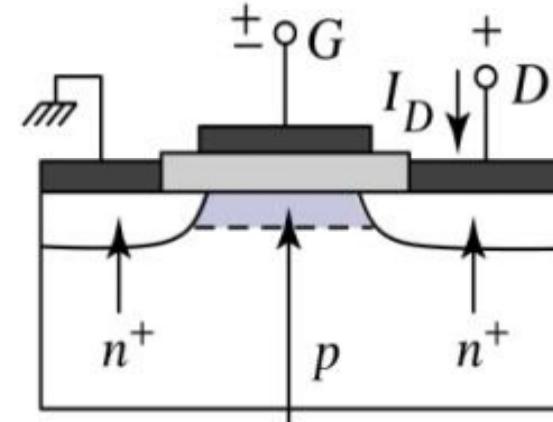


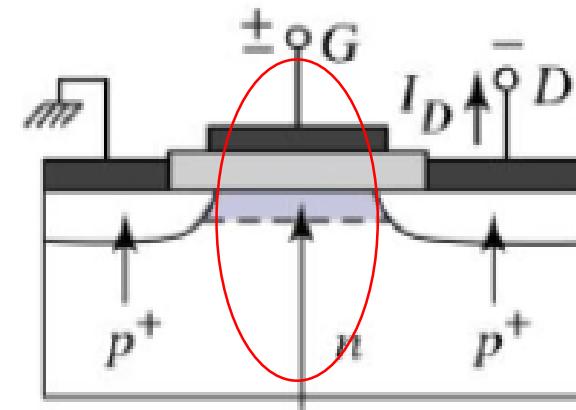
Figure 3.42

p-channel MOSFET (PMOSFET)

- In PMOSFET, the operation is similar to NMOSFET. When we apply a negative gate voltage greater than the threshold voltage V_T , the MOS diode will be in strong inversion and there will be holes accumulated in a thin inversion layer close to the oxide semiconductor interface. If there is no horizontal electric field applied to these electrons, they will not flow.
- When a negative voltage is applied to the drain terminal, the holes in the inversion layer will flow from the source to the drain giving rise to the drain current. The p+ source region is also the source to supply the holes in the channel.



n-Channel
Figure 3.43



p-Channel
Figure 3.44

Depletion and Enhancement mode MOSFETs

- In both NMOSFET and PMOSFET, we can further classify them into two categories namely depletion and enhancement.
- **Depletion mode MOSFET:** in **ON** state when $V_{gs}=0V$ (Figure 3.45). Hence, it is also called **Normally On** MOSFET.

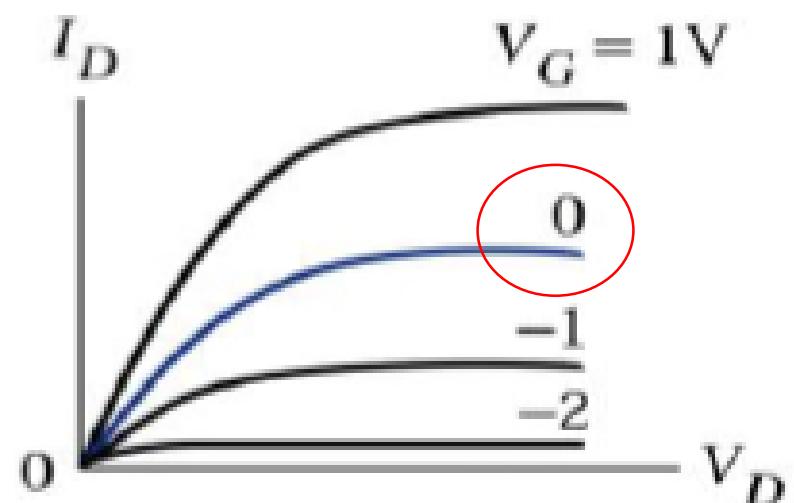


Figure 3.45 Depletion or Normally ON NMOSFET

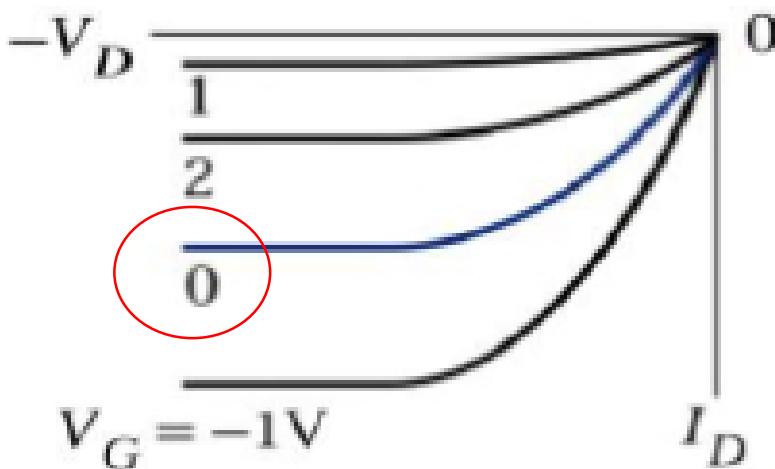


Figure 3.46 Depletion or Normally ON NMOSFET

Depletion and Enhancement mode MOSFETs (cont'd)

- **Enhancement mode MOSFET:** in *OFF* state when $V_{gs}=0V$ (Figure 3.38a). Hence, it is also called ***Normally OFF*** MOSFET.

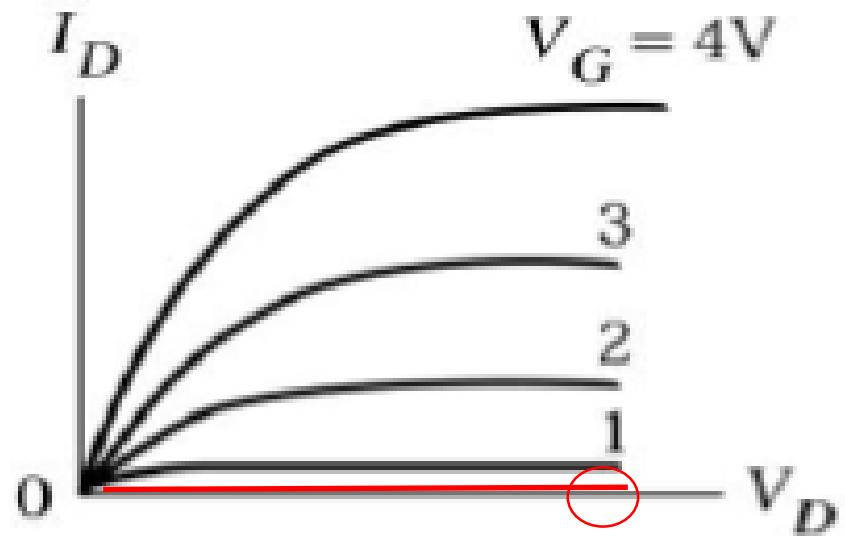


Figure 3.46 Enhancement or Normally OFF NMOSFET

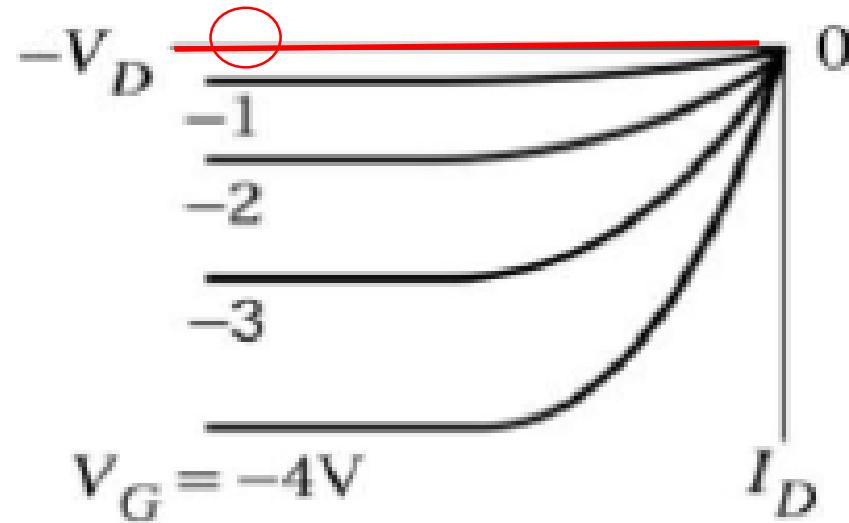


Figure 3.47 Enhancement or Normally OFF NMOSFET

Cut-off Frequency of MOSFETs

- Similar to BJT, the cutoff frequency of a MOSFET may also be expressed as:

$$f_T = \frac{1}{2\pi\tau_T} \quad (\text{Equation 3.23})$$

- Transit time can be obtained by:

$$\tau_T = \frac{L}{V_s} \quad (\text{Equation 3.24})$$

where V_s is the carrier velocity in the channel. For NMOSFET, it is the electron velocity and for PMOSFET, it is the hole velocity.

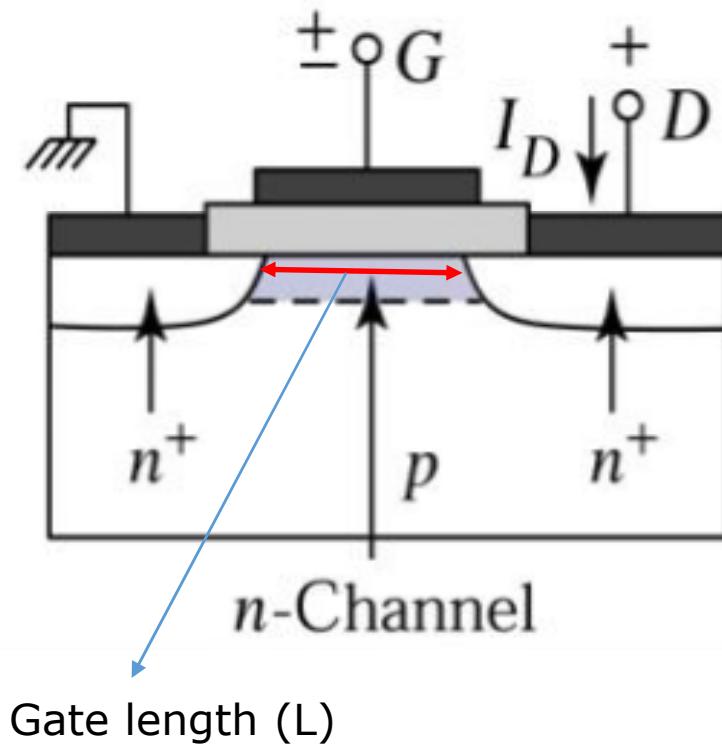
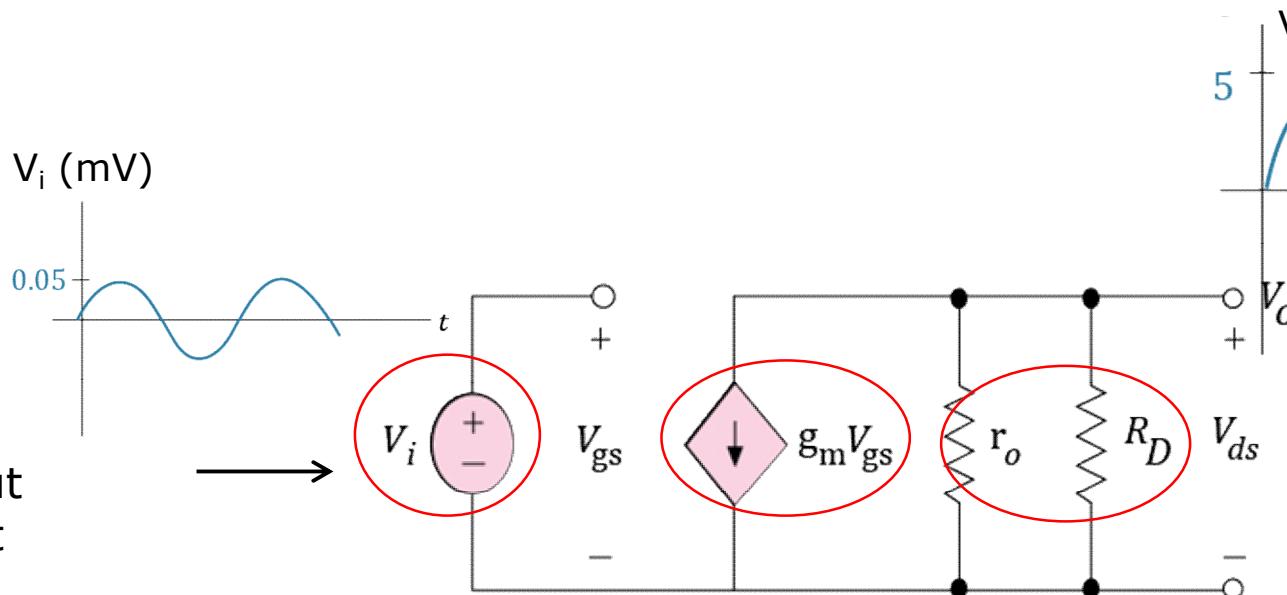
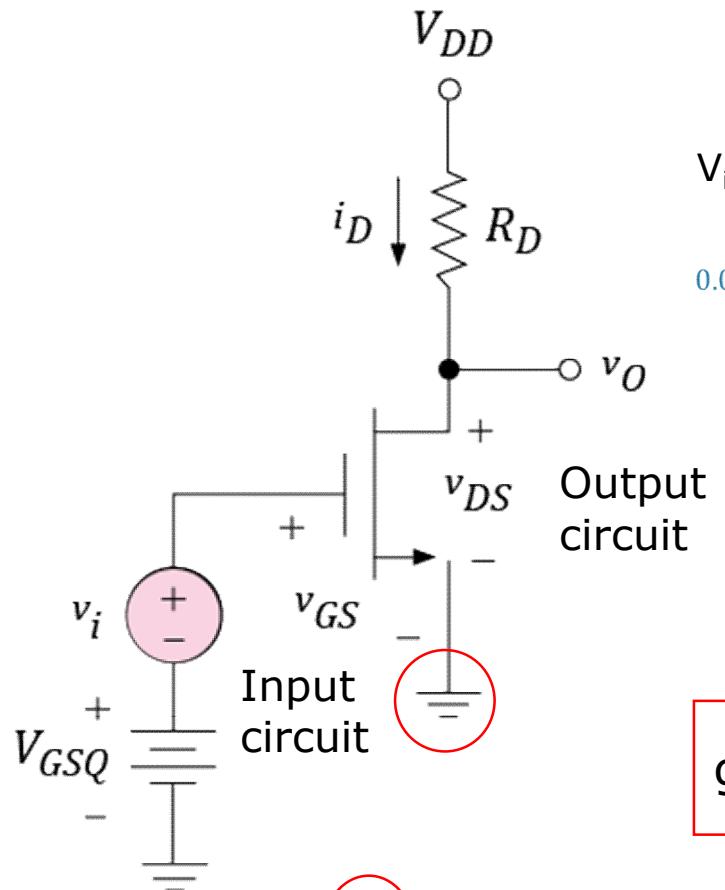


Figure 3.48

How Does a NMOSFET Amplify?



$$g_m = \Delta I_{ds} / \Delta V_{gs} \quad (\text{Equation 3.25})$$

Figure 3.49 v_i (input voltage) \rightarrow $g_m V_{gs}$ (amplified current) \rightarrow V_o (output voltage)

$$A_v = \frac{V_o}{V_i} = -g_m (r_o || R_d) \quad (\text{Equation 3.26})$$

Lesson Summary

(A) MOS Diode with p-Si

1. For ideal MOS diode with p-Si at thermal equilibrium: $q\phi_m = q\phi_s$ and $\phi_s = qx + \frac{E_g}{2} + q\psi_B$
2. For MOS diode with p-Si: when $V < 0 \rightarrow$ Accumulation; $V > 0 \rightarrow$ Depletion; $V \gg 0 \rightarrow$ Inversion
3. At the onset of strong inversion: $\psi_s = 2\psi_B$, $n_p = N_A$ and depletion width is maximum W_m , and

total charges become $Q_s = Q_n - qN_A W_m$. W_m is given by $W_m = \sqrt{\frac{2\epsilon_s(2\psi_B)}{qN_A}} = \sqrt{\frac{4\epsilon_s k T \ln(\frac{N_A}{n_i})}{q^2 N_A}}$, the

Surface potential $\psi_s(inv) = 2\psi_B = \frac{2kT}{q} \ln(\frac{N_A}{n_i})$ and the charges in the depletion region $Q_s = -qN_A W_m \cong -\sqrt{2q\epsilon_s N_A(2\psi_B)}$

- Total MOS capacitance $C = \frac{C_0 C_j}{(C_0 + C_j)} F.cm^{-2}$ where $C_j = \epsilon_s/W$ and $C_0 = \epsilon_{ox}/d$
- CV plot is divided into three distinct regions: Accumulation, Depletion and Strong inversion.

Lesson Summary (cont'd)

6. Threshold voltage V_T at the onset of **strong inversion** is given by:

$$V_T = \frac{qN_A W_m}{C_o} + 2\psi_B = \frac{\sqrt{2\epsilon_s q N_A (2\psi_B)}}{C_o} + 2\psi_B$$

7. For non-ideal MOS diode with p-Si, due to the work function difference and the oxide traps/charges in the oxide, we need to apply a voltage $V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_o}$ to return to the flat-band condition as in the ideal case. Thus V_T is given by:

$$V_T = \frac{N_A W_m}{C_o} + 2\psi_B + \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_o}$$

8. The CV curve will shift horizontally to the negative voltage due to the change in V_T .

Lesson Summary (cont'd)

(B) MOSFET

9. For NMOSFET, it can be divided into three operating modes:

i. **Cut-off region:** $I_D = 0$ for $V_{GS} \leq V_T$

ii. **Linear (Triode) region:** $I_D = K_n[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$ for $V_{DS} \leq V_{GS} - V_T$

iii. **Saturation region:** $I_D = \frac{K_n}{2}(V_{GS} - V_T)^2$ for $V_{DS} \geq V_{GS} - V_T$

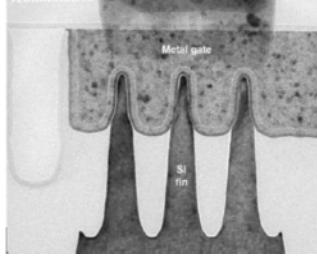
10. MOSFETs can also be divided into:

i. Depletion mode (or Normally ON) MOSFET: in ON state when $V_{gs}=0V$

ii. Enhancement mode (or Normally OFF) MOSFET: in OFF state when $V_{gs}=0V$

11. Cutoff frequency of a MOSFET $f_T = \frac{1}{2\pi\tau_T}$ where $\tau_T = \frac{L}{V_s}$

Reference

No.	Slide No.	Image	Reference
1.	4		By Smith, R. (2014, August 11). Intel's 14nm Technology in Detail. Retrieved April 07, 2017, from http://www.anandtech.com/show/8367/intels-14nm-technology-in-detail