Appendix A
List of Formulae (with the usual notations)

Op-Amps:

Closed-Loop Negative Feedback Inverting Gain, $A_{VCL} = \frac{v_o}{v_i} = -\frac{R_f}{R_i}$ Figure (a)

Closed-Loop Negative Feedback Non-Inverting Gain, $A_{VCL} = \frac{v_o}{v_i} = \left(1 + \frac{R_f}{R_i}\right)$ Figure (b)

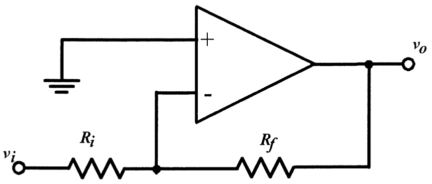


Figure (a)

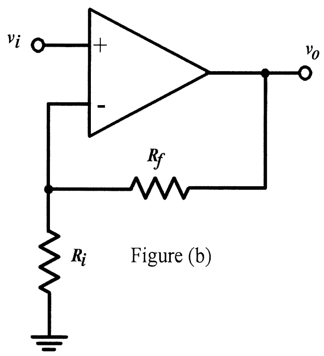
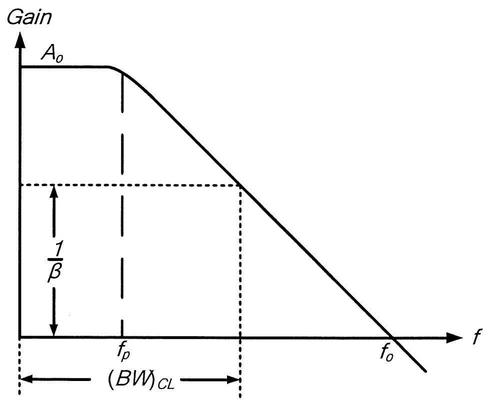


Figure (b)

Op-Amp's Slew Rate, $SR \geq \left|\frac{dv_o}{dt}\right|_{\max} = A_{VCL}\omega a_m = A_{VCL} a_m 2\pi f$,

where $v_i = a_m \sin(\omega\, t)$, $v_o = A_{VCL} v_i$, $v_o = A_{VCL} a_m \sin(\omega t)$ and $\left|\frac{dv_o}{dt}\right| = A_{VCL}\omega\, a_m \cos(\omega t)$

Op-Amp's frequency response: $A_{VOL}(jf) = \frac{A_o}{\left(1 + \frac{jf}{f_p}\right)}$



Gain-Bandwidth Product: $A_o f_p = f_o = \frac{1}{\beta}(BW)_{CL}$

where $\frac{1}{\beta} = \frac{R_f + R_i}{R_i}$

$t_r = \frac{0.35}{(BW)_{CL}}$

Diodes:

$v_D \approx nV_T \ln\left(\frac{i_D}{I_S}\right)$ or $i_D \approx I_S e^{\left(\frac{v_D}{nV_T}\right)}$

where $e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + ...$

Diode conductance: $g_D = \frac{1}{r_D} = \frac{I_D}{nV_T}$

BJT in Forward Active Region:

Ignore early effect: $i_C = I_S \exp\left(\frac{|v_{BE}|}{V_T}\right)$

With early effect: $i_C = I_S \exp\left(\frac{|v_{BE}|}{V_T}\right)\left(1+\frac{|v_{CE}|}{V_A}\right)$

where I_s: Saturation current,
V_T: Thermal voltage, assume 25 mV at room temperature,
V_A: Early voltage.
For npn transistor, $|v_{BE}| = v_{BE}$ and $|v_{CE}| = v_{CE}$;
For pnp transistor, $|v_{BE}| = v_{EB}$ and $|v_{CE}| = v_{EC}$.

Small-signal model parameters of BJT:

$g_m = \frac{I_C}{V_T}$, $r_\pi = \frac{\beta}{g_m}$ and $r_o = \frac{V_A + |V_{CE}|}{I_C} \approx \frac{V_A}{I_C}$

where I_C : DC collector current at Q-point
V_{CE}: DC collector-emitter voltage at Q-point

Criterion for small-signal operation of BJT: $|v_{be}| \leq 0.2V_T$

MOSFET in Saturation Region:

Criterion: $V_{DS} \geq V_{GS} - V_{TN}$ for NMOS;
$|V_{DS}| \geq |V_{GS}| - |V_{TP}|$ for PMOS

where V_{TN}, V_{TP}: Threshold voltage,
V_{DS}: DC drain-source voltage,
V_{GS}: DC gate-source voltage.

Ignore channel-length modulation effect: $i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2$ for NMOS,

$i_D = \frac{K_p}{2}(|v_{GS}| - |V_{TP}|)^2$ for PMOS.

With channel-length modulation effect: $i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2 (1 + \lambda v_{DS})$ for NMOS,

$i_D = \frac{K_p}{2}(|v_{GS}| - |V_{TP}|)^2 (1 + \lambda |v_{DS}|)$ for PMOS.

where λ: channel length modulation parameter,

For NMOS $K_n = K_n'\left(\frac{W}{L}\right)$ and $K_n' = \mu_n C_{ox}$; For PMOS $K_p = K_p'\left(\frac{W}{L}\right)$ and $K_p' = \mu_p C_{ox}$.

MOSFET in Triode Region:

Criterion: $V_{DS} < V_{GS} - V_{TN}$ for NMOS;
$|V_{DS}| < |V_{GS}| - |V_{TP}|$ for PMOS

Ignore channel-length modulation effect: $i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}$ for NMOS,

$i_D = K_p\left(|v_{GS}| - |V_{TP}| - \frac{|v_{DS}|}{2}\right)|v_{DS}|$ for PMOS.

With channel-length modulation effect: $i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}(1+\lambda v_{DS})$ for NMOS,

$i_D = K_p\left(|v_{GS}| - |V_{TP}| - \frac{|v_{DS}|}{2}\right)|v_{DS}|(1+\lambda|v_{DS}|)$ for PMOS.

Small-signal model parameters of MOSFET

For NMOS: $g_m = \sqrt{2K_nI_D(1+\lambda V_{DS})} \approx \sqrt{2K_nI_D}$ and $r_o = \frac{\frac{1}{\lambda} + V_{DS}}{I_D} \approx \frac{1}{\lambda I_D}$

For PMOS: $g_m = \sqrt{2K_pI_D(1+\lambda|V_{DS}|)} \approx \sqrt{2K_pI_D}$ and $r_o = \frac{\frac{1}{\lambda} + |V_{DS}|}{I_D} \approx \frac{1}{\lambda I_D}$

where I_D : DC drain current at Q-point
V_{DS}: DC drain-source voltage at Q-point

Criterion for small-signal operation:
For NMOS: $|v_{gs}| \le 0.2(V_{GS} - V_{TN})$
For PMOS: $|v_{gs}| \le 0.2(|V_{GS}| - |V_{TP}|)$
where V_{GS} : DC gate-source voltage at Q-point.

Frequency Response: OCTC and SCTC

0) DISABLE DC sources…
voltage sources -> SHORT CIRCUIT, current sources -> OPEN CIRCUIT

1) Identify capacitors contributing (reducing V_o or causing trouble) to the frequency of interest (i.e. lower or higher cut-off).

2) DISABLE all independent AC sources...
voltage sources -> SHORT CIRCUIT, current sources -> OPEN CIRCUIT
DO NOT remove or "disable" dependent sources!

higher cut-off (OCTC)

3) Idealize irrelevant capacitors by SHORT CIRCUIT (because at high f, cap → short)

Next step to find time constant

4) For each contributing capacitor C_i, set all other capacitors (other than the one you are looking at) removed (i.e. OPEN CIRCUITS) and determine the resistance, R_i seen by C_i

5) Higher cut-off frequency is estimated as:

$$\omega_{H-3dB} \approx \frac{1}{\sum_i C_i R_i} = \frac{1}{C_1 R_1 + C_2 R_2 + \ldots}$$

lower cut-off (SCTC)

3) Idealize irrelevant capacitors by OPEN CIRCUIT (because at low f, cap → open)

Next step to find time constant

4) For each contributing capacitor C_i, set all other capacitors (other than the one you are looking at) removed (i.e. SHORT CIRCUITS) and determine the resistance, R_i seen by C_i

5) Lower cut-off frequency is estimated as:

$$\omega_{L-3dB} \approx \sum_i \frac{1}{C_i R_i} = \frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} + \ldots$$

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