EE2002

TUTORIAL 2 (with answers at the back)

1. An op-amp is connected in the noninverting amplifier configuration. A voltage source of value v_S is connected via a series resistance R_S to the v_+ terminal.

   a) Find an expression for v_{OUT} as a function of v_s if the op-amp is ideal.

   b) If the op-amp is nonideal and has input bias currents I_+ and I_- and input offset voltage V_{IO}, find an expression for v_{OUT} when v_S=0.

   c) Combine the answers to parts (a) and (b) to find the total output when v_S is nonzero.

   d) The feedback resistors in the amplifier are set to 25kΩ and 100 kΩ, so that the amplifier has a gain of 5. If $I_{BIAS}=(I_+ + I_-)/2$=100 nA, I_{IO}=-40nA, and V_{IO}=2mV, what value of R_S will minimize the total dc offset component to v_{OUT}?

2. A high-gain op-amp circuit is formed by cascading two inverting amplifiers in series. Both op-amps are connected to ±15V power supplies. The first stage has a gain of -20. The cascade is to be designed so that the peak output voltage of the second stage comes no closer than 1V to either power supply voltage. The cascade is built from nonideal op-amps with V_{IO}=2mVand $I_{BIAS}\approx 0$, I_{IO}=0.

   a) If both stages remain in the linear region, find an expression for the output voltage that includes the effect of V_{IO}. Express the gain of each stage in terms of the ratio of its resistor values. (Stage 1 gain = $-R_2/R_1$; stage 2 gain = $-R_4/R_3$.)

   b) If v_{IN} is a sinusoid of 25mV peak magnitude, what is the maximum gain of the second stage if v_{OUT} is to remain within the specified swing limits?

3. An op-amp is connected in the inverting amplifier configuration. The gain of the amplifier is set to –50 by using 100kΩ and 2 kΩ resistors in the feedback circuit. The v+ terminal is connected to ground. The op-amp is non-ideal and has parameters I_{BIAS}=0; I_{IO}=0, V_{IO}=0, and slew rate=1V/us.

   a) If the input voltage is a 10-mV peak sinusoid, what is the maximum frequency that can be applied before the slew rate limitation is reached?

   b) Repeat part((a))for an input voltage that consists of a 10 mV peak triangular waveform.

   c) Sketch the output voltage versus time if the input is a 10 mV peak square wave.

4. An op-amp is connected in the non-inverting amplifier configuration. A gain of 11 is achieved by using 500 kΩ and 50 kΩ resistors in the feedback circuit. The signal source connected to the v_+ input terminal has a 50 Ωseries Thevenin resistance.

   a) If the op-amp has an input bias current of luA, calculate the dc value of v_{OUT} when v_{IN}=0. Assume I_{IO}=0.

   b) Choose an additional resistor to be put in series with the input source so that dc offset found in part (a) is forced to zero.

5. An op-amp circuit with a dc gain of 400 is formed by cascading in series two inverting amplifiers with gains of -20. Both op-amps are connected to ±l5V power supplies and have slew rates of 1V/us.

   a) If the input is a sinusoidal voltage, what peak magnitude drives the output to its full swing range if $V_{sat\text{-}pos}$=14.3 $V_{sat\text{-}neg}$=-14V?

   b) For the input voltage found in part (a), what is the maximum frequency in hertz that the input voltage can have before slew rate limitation becomes important ?

6 .a) The op-amp in Fig. 1 has a unity-gain frequency of l.2MHz.
   i) What is the closed loop BW?
   ii) What is the closed-loop gain at 600kHz ?

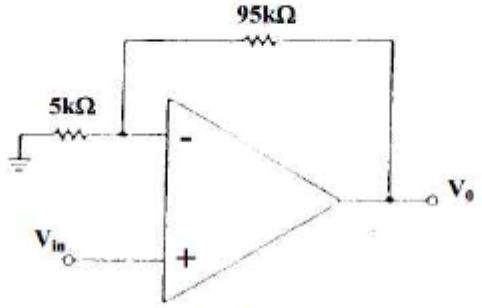

Fig. 1

6 .b)The op-amp shown in Fig. 2 has a SR of 4 V/μS and a unity-gain frequency of 2MHz. Determine whether the amplifier will distort the input signal shown.

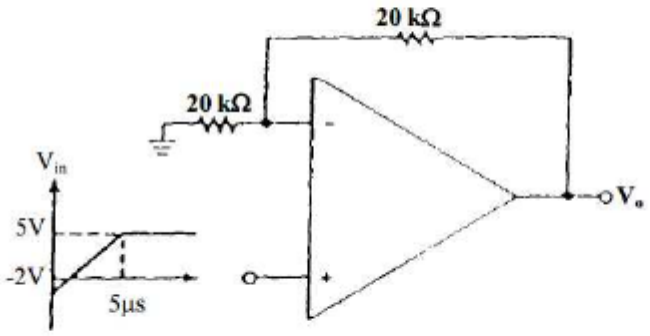

Fig. 2

Answers to Tutorial 2

1. (a) $\mathbf{v_{OUT}} = \left(\frac{\mathbf{R_2 + R_1}}{\mathbf{R_1}}\right)\mathbf{v_s}$

   (b) $\mathbf{v_{OUT}} = \mathbf{V_{IO}}\left(\mathbf{1} + \frac{\mathbf{R_2}}{\mathbf{R_1}}\right) + \mathbf{I_{-}R_2} - \mathbf{I_{+}R_S}\left(\mathbf{1} + \frac{\mathbf{R_2}}{\mathbf{R_1}}\right)$

   (c) $\mathbf{v_{OUT}} = \left(\mathbf{1} + \frac{\mathbf{R_2}}{\mathbf{R_1}}\right)\left(\mathbf{v_s} + \mathbf{V_{IO}} - \mathbf{I_{+}R_S}\right) + \mathbf{I_{-}R_2}$

   (d) R_s = 55 kohm

2. (a)

$$\mathbf{v_{OUT1}} = -\frac{\mathbf{R_2}}{\mathbf{R_1}}\mathbf{v_s} + \mathbf{V_{IO}}\left(\mathbf{1} + \frac{\mathbf{R_2}}{\mathbf{R_1}}\right)\#$$

$$\mathbf{v_{OUT2}} = \frac{\mathbf{R_4}}{\mathbf{R_3}}\left[\frac{\mathbf{R_2}}{\mathbf{R_1}}\mathbf{v_s} - \frac{\mathbf{R_2}}{\mathbf{R_1}}\mathbf{V_{IO}}\right] + \mathbf{V_{IO}}$$

   (b)The maximum permissible gain of the second stage is 26.

3. (a) f_{max} = 318 kHz
   (b) f ≤ 500 kHz

4. (a) V_{OUT} = 499.45 mV
   (b) R_s = 45.4 kohm

5. (a) v_{IN} = ±35 mV_p
   (b) f_{max} = 11.4 kHz

6. (a)
   (i) BWCL = 60 kHz
   (ii) Closed Loop Gain (600kHz) = 2.0 V/V

   (b) No distortion will occur