NANYANG TECHNOLOGICAL UNIVERSITY SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

ACADEMIC YEAR 2020-2021
SEMESTER 2

EE3019 INTEGRATED ELECTRONICS

TUTORIAL 2

---

1. Consider a CMOS inverter working on $V_{DD} = 3.3$ V and with the following device parameters:

   nMOS $V_{t0n} = 0.6$ V $\mu_n C_{ox} = 60\ \mu A/V^2$ $(W/L)_n = 8$
   pMOS $V_{t0p} = -0.7$ V $\mu_p C_{ox} = 25\ \mu A/V^2$ $(W/L)_p = 12$

   (a) Calculate the noise margins and the switching threshold, V_{th}, of this circuit.
   (b) If the channel length of both transistors is $L_n = L_p = 0.8\ \mu m$, determine the (W_n/W_p) ratio so that the switching threshold is changed to 1.4V.

   [Answer: $NM_L = 1.1985$ V, $NM_H = 1.6042$ V, $V_{th} = 1.483$ V, $W_n/W_p = 0.94$]

2. Find the propagation delay for a minimum-size CMOS inverter using the average current method. Given that $\mu_n C_{ox} = 3\ \mu_p C_{ox} = 75\ \mu A/V^2$ and $(W/L)_n = (W/L)_p = 1.2\mu m/0.8\mu m$.

   $V_{DD} = 3.3$V, $|V_t| = 0.2V_{DD}$, and the unit capacitance is roughly 2 fF/μm of device width plus 1 fF/device.

   [Answer: $t_p = 62.3$ *psec*]

3. A CMOS microprocessor chip containing the equivalent of 1 million gates operates from a 5V supply. The power dissipation is found to be 9W when the chip is operating at 120MHz and 4.7W when operating at 50MHz. What is the power lost in the chip due to clock-independent role? If 70% of the gates are assumed to be active at any time, what is the average gate capacitance in such a design?

   [Answer: $P_S = 1.629$W, $C_{gate} = 3.51\ f$F]