

**NANYANG TECHNOLOGICAL UNIVERSITY****SEMESTER 1 EXAMINATION 2021-2022****EE3013 – SEMICONDUCTOR DEVICES AND PROCESSING**

November / December 2021

Time Allowed: 2 hours

**INSTRUCTIONS**

1. This paper contains 4 questions and comprises 8 pages.
  2. Answer all 4 questions.
  3. All questions carry equal marks.
  4. This is a closed book examination.
  5. A **List of Selected Formulae** and a **Table of Physical Constants** are provided in **Appendices A and B** on pages 6 - 8.
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1. (a) The Rayleigh criterion is used to derive the minimum feature size in projection lithography. In each of the following parameters affecting the Rayleigh equation, describe how one will implement the physical change on the lithography system to improve its resolution.
  - (i) Change of wavelength,  $\lambda$
  - (ii) Change of resist constant,  $k$
  - (iii) Change of numerical aperture,  $NA$(4 Marks)
- (b) A photoresist is a light-sensitive material used in several processes in the electronic industry.
  - (i) List some functions of a photoresist.
  - (ii) Name the various process steps before the Soft Bake process.
  - (iii) How does a resist adhesion promotor work?(8 Marks)

Note: Question No. 1 continues on page 2.

- (c) Briefly describe two approaches to mask engineering that can be utilized to improve resolution in optical lithography. (6 Marks)
- (d) An exposure is performed using a step-and-repeat aligner printing system. The light source has a wavelength of 365 nm. If its depth of focus of the image is 1  $\mu\text{m}$ , determine the resolution of the system. Assume  $k_1 = 1$  and  $k_2 = 0.8$ . (7 Marks)
2. (a) In a parallel plate plasma etching system, two electrodes **E1** (powered) and **E2** (grounded) are used.
- Schematically sketch the voltage distribution in the plasma between the two non-symmetrical electrodes in which area size of **E1** < **E2**.
  - If the size area of **E2** is 8 times larger than **E1**, determine the cathode potential if the anode potential with respect to the plasma potential is – 50mV.
  - The etched surface becomes relatively rough when the stainless-steel cathode is replaced by an aluminum one. Comment on this observation.
  - What changes in the etch rate would one expect to observe and why, if
    - the radio frequency (rf) power is decreased?
    - the process temperature is increased?

(12 Marks)

- (b) Figure 1 shows the transport of film particles to a substrate in a Physical Vapour Deposition (PVD) System.

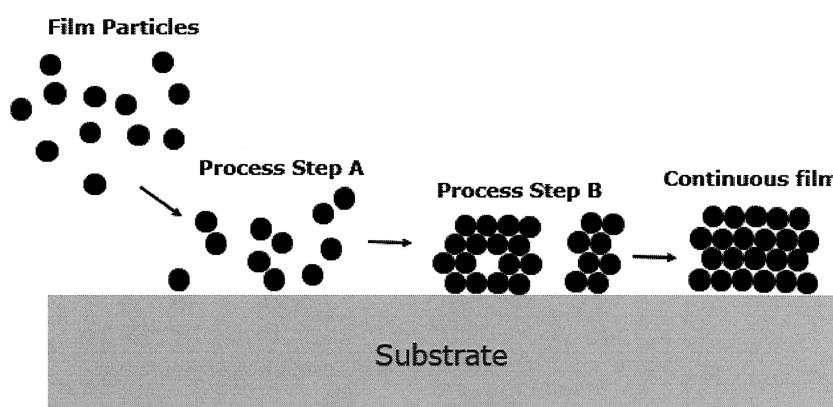


Figure 1: Typical PVD Deposition Mechanism

Note: Question No. 2 continues on page 3.

- (i) Name the process steps Step A and B shown in Figure 1.  
(ii) List some differences between the thermal and electron beam evaporation.
- (7 Marks)
- (c) Figure 2 shows a schematic diagram of a magnetron sputtering system.

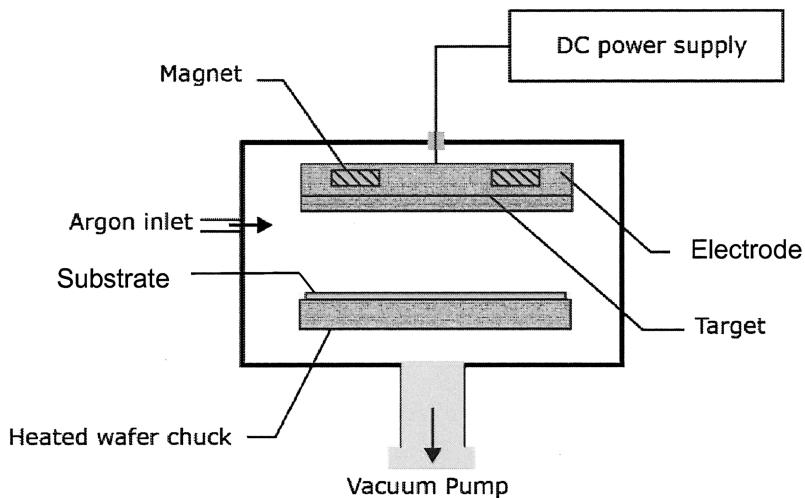


Figure 2: A Magnetron Sputtering System

- (i) Name the electrode on which the target is mounted.  
(ii) Explain why magnets are deployed in the electrode.  
(iii) What is/are the advantage(s) of replacing the DC power supply with a radio frequency (rf) power supply?

(6 Marks)

3. (a) A  $<100>$  silicon wafer with an initial oxide thickness of  $0.025 \mu\text{m}$  has gone through a 30 min of dry oxidation followed by a 120 min wet oxidation cycle at  $1100^\circ\text{C}$ . Assume the following parameters:

For Dry oxidation:  $A = 0.140 \mu\text{m}$  and  $B = 0.024 \mu\text{m}^2/\text{hr}$

For Wet oxidation:  $A = 0.183 \mu\text{m}$  and  $B = 0.529 \mu\text{m}^2/\text{hr}$

- (i) Determine the final total oxide thickness.  
(ii) What are the advantages of dry oxidation versus wet oxidation?
- (6 Marks)
- (3 Marks)

Note: Question No. 3 continues on page 4.

- (b) (i) When a diffusion process should be used in semiconductor wafer fabrication?  
(3 Marks)
- (ii) A p-n junction is formed by diffusing pre-deposited boron atoms into the n-type silicon substrate at  $1150^{\circ}\text{C}$ . Assuming that the diffusion is Gaussian and the doping concentration of the silicon substrate is  $2 \times 10^{16}\text{cm}^{-3}$ , what is the diffusion time required to form a junction depth at  $2\mu\text{m}$ ? Given the surface concentration  $N_s = 2 \times 10^{17}\text{cm}^{-3}$  and  $D = 1 \times 10^{-12}\text{cm}^2/\text{s}$  at  $1150^{\circ}\text{C}$ .  
(6 Marks)
- (c) (i) What is ion channeling in an ion-implantation process? How to avoid it?  
(4 Marks)
- (ii) When is ion-implantation process preferred over thermal diffusion in the doping of semiconductor devices?  
(3 Marks)
- 4 (a) Calculate the applied reverse-biased voltage at which the ideal reverse current in a p-n junction diode at  $T = 300\text{K}$  reaches 90 percent of its reverse-saturation current value.  
(5 Marks)
- (b) For a p-n-p bipolar junction transistor (BJT),
- (i) Explain why the base width ( $W_B$ ) needs to be smaller than the hole diffusion length ( $L_p$ ).  
(6 Marks)
  - (ii) Give one advantage and one disadvantage for a narrow base width BJT.
- (c) An ideal MOS capacitor with an  $\text{n}^+$  polysilicon gate has a silicon dioxide thickness of  $t_{ox} = 12\text{ nm}$  on a p-type silicon substrate doped at  $N_d = 10^{16}\text{cm}^{-3}$ . At a frequency of 1 MHz, determine:
- (i) The maximum capacitance per unit area.
  - (ii) The minimum capacitance per unit area under strong inversion if the depletion width is  $1.182 \times 10^{-4}\text{cm}$ .  
(8 Marks)

Note: Question No. 4 continues on page 5.

- (d) An n-channel MOSFET has a threshold voltage  $V_T = 4.5V$ . The gate terminal is connected to the drain terminal.
- (i) Is the MOSFET in linear or saturation mode? Explain your answer.
  - (ii) If  $K_n = 1.111 \text{ mA/V}^2$ , what is the drain current at  $V_{DS} = 3V$ ?

(6 Marks)

## List of Selected Formulae

### **(1) P-N junction**

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}; \quad N_A x_p = N_D x_n; \quad W = x_p + x_n; \quad C_j = \frac{\epsilon_s}{W}; \quad L_p = \sqrt{D_p \tau_p}$$

$$W = \sqrt{\frac{2\epsilon_s}{q} \left[ \frac{1}{N_A} + \frac{1}{N_D} \right] (V_{bi} - V)}; \quad J = J_n(-x_p) + J_p(x_n) = \left( \frac{qD_p p_{no}}{L_p} + \frac{qD_p n_{po}}{L_n} \right) \left[ e^{qV/kT} - 1 \right]$$

### **(2) Bipolar junction transistors**

$$\gamma \equiv \frac{I_{Ep}}{I_E} = \frac{I_{Ep}}{I_{Ep} + I_{En}}; \quad \alpha_T \equiv \frac{I_{Cp}}{I_{Ep}}; \quad \alpha_0 = \gamma \alpha_T; \quad \beta_0 = \frac{\alpha_0}{1 - \alpha_0}; \quad I_C = \alpha_0 I_E + I_{CBO};$$

$$I_{CEO} = (1 + \beta_0) I_{CBO}; \quad p_n(x) = p_{no} e^{qV_{EB}/kT} \left( 1 - \frac{x}{W} \right); \quad \gamma = \frac{1}{1 + \frac{D_E}{D_p} \cdot \frac{N_B}{N_E} \cdot \frac{W}{L_E}};$$

$$I_{Ep} = qA \frac{D_p p_{no}}{W} e^{(qV_{EB}/kT)}; \quad I_{En} = qA \frac{D_E n_{E0}}{L_E} (e^{qV_{EB}/kT} - 1); \quad I_{Cn} = qA \frac{D_C n_{C0}}{L_C};$$

$$p_{no} \cdot N_B = n_{E0} \cdot N_E = n_{C0} \cdot N_C = n_i^2; \quad \tau_B = \frac{W^2}{2D_p}; \quad f_T = \frac{1}{2\pi\tau_B}.$$

### **(3) MOS devices**

$$\psi_s = 2\psi_B = \frac{2kT}{q} \ln \left( \frac{N_A}{n_i} \right); \quad W_m^2 = \frac{2\epsilon_s (2\psi_B)}{qN_A} = \frac{4\epsilon_s kT}{q^2 N_A} \ln \left( \frac{N_A}{n_i} \right); \quad V_T = \frac{qN_A W_m}{C_o} + 2\psi_B;$$

$$\frac{C}{C_0} = \frac{1}{\sqrt{1 + \frac{2\epsilon_{ox}^2 V}{qN_A \epsilon_s d^2}}}; \quad \frac{1}{C_{min}} = \frac{d}{\epsilon_{ox}} + \frac{W_m}{\epsilon_s}; \quad V_{FB} = \phi_{ms} - \frac{(Q_f + Q_m + Q_{ot})}{C_0}.$$

$$I_D = K_n [(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}] \text{ for } V_{DS} < V_{GS} - V_T; \quad V_T = \frac{qN_A W_m}{C_0} + 2\psi_B \text{ when } V_{FB} = 0;$$

$$I_D = \frac{K_n}{2} (V_{GS} - V_T)^2 \text{ for } V_{DS} \geq V_{GS} - V_T; \quad K_n = \mu_n C_{ox} \frac{W}{L}.$$

**(4) Thermal oxidation**

$$t_{ox}^2 + At_{ox} = B(t + \tau) \quad \tau = \frac{t_{ox}^2}{B} + \frac{t_{ox}}{B/A} \quad t_{ox} = \frac{-A + \sqrt{A^2 + 4B(t + \tau)}}{2}$$

**(5) Thermal diffusion**

$$D = D_o \exp\left(-\frac{E_a}{kT}\right)$$

Constant source diffusion:

$$N(z, t) = N_s \operatorname{erfc}\left(\frac{z}{2\sqrt{Dt}}\right)$$

Limited source diffusion:

$$N(z, t) = \frac{Q}{\sqrt{\pi Dt}} \exp\left[-\frac{z^2}{4Dt}\right], \quad Q = \frac{2}{\sqrt{\pi}} N_s \sqrt{Dt}.$$

**(6) Ion implantation**Before Annealing

$$N(x) = \frac{Q}{\sqrt{2\pi \Delta R_p}} \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right]$$

$$Q = \int_0^\infty N(x) dx = \sqrt{2\pi} N_p \Delta R_p$$

After annealing

$$N(x) = \frac{Q}{\sqrt{2\pi (\Delta R_p^2 + 2Dt)^{1/2}}} \exp\left[-\frac{(x - R_p)^2}{2(\Delta R_p^2 + 2Dt)}\right]$$

Silicon oxide for masking

$$N(t_{ox}) = N_p \exp\left[-\frac{(t_{ox} - R_p)^2}{2\Delta R_p^2}\right] < \frac{N_B}{10}$$

$$t_{ox} \geq R_p + \Delta R_p \sqrt{2 \ln\left(\frac{10N_p}{N_B}\right)}$$

**Table of Physical Constants**

Physical Constant	Symbol	Value	Units
Electronic charge	$q$	$1.6 \times 10^{-19}$	C
Boltzmann's constant	$k$	$8.62 \times 10^{-5}$ $1.38066 \times 10^{-23}$	eV/K J/K
Planck's constant	$h$	$6.626 \times 10^{-34}$	J·s
Permittivity of free space	$\epsilon_0$	$8.85 \times 10^{-14}$	F/cm
Dielectric constant of Si	$\epsilon_{Si}$	11.7	-
Dielectric constant of $SiO_2$	$\epsilon_{ox}$	3.9	-
Electron Mass	$m$	$9.11 \times 10^{-31}$	kg
Speed of Light	$c$	$3 \times 10^8$	m/s
Bandgap of Si at 300 K	$E_g$	1.12	eV
Intrinsic carrier concentration in Si at 300 K	$n_i$	$1 \times 10^{10}$	$cm^{-3}$

END OF PAPER







## **EE3013 SEMICONDUCTOR DEVICES & PROCESSING**

Please read the following instructions carefully:

- 1. Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**
2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.
3. Please write your Matriculation Number on the front of the answer book.
4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.

# EE3013 – SEMICONDUCTOR DEVICES AND PROCESSING

## Semester 1, AY2021/2022

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1)

- a) Resolution  $W$  of a lithography system is defined as  $W = k \frac{\lambda}{NA}$ , lower is better.
  - i) Decrease  $\lambda$ . Use UV sources of smaller wavelength, e.g. extreme UV or e-beam.
  - ii) Decrease  $k$ . Use optical resolution enhancement techniques, e.g. optical proximity correction.
  - iii) Increase  $NA$ . Use immersion lithography with modified lens column design, to exploit the larger  $n$  of different medium as  $NA = n \sin \theta$ .
- b)
  - i) To act as mask for subsequent ion implantation and/or etching.
  - ii) Vapour prime, spin coat.
  - iii) Resist adhesion promotor is hydrophobic. This seals off the wafer surface from any water molecule, and ensures that the resist (compatible with the hydrocarbon group of the adhesion promotor) will stick to the promotor (and wafer) instead of layer of water molecules.
- c) Phase shift mask: include a layer of transparent material on alternating regions of the mask. This cause a phase shift of the light that passes through it and cause destructive interference in regions that are not supposed to be exposed.

Optical proximity correction: by sophisticated software, extra features (e.g. bumps) are introduced at edges, sharp turns of the mask to compensate for the high frequency information lost due to diffraction.

- d) Resolution is given as  $W = k_1 \frac{\lambda}{NA}$ , whereas depth of focus is given as  $\sigma = k_2 \frac{\lambda}{(NA)^2}$

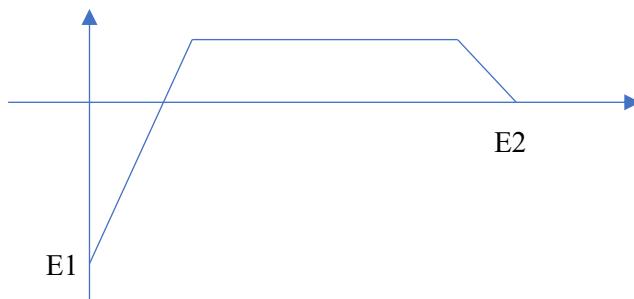
$$\text{Given } \sigma = 1 \mu\text{m}: 1 \times 10^{-6} = 0.8 \frac{365 \times 10^{-9}}{(NA)^2} \Rightarrow NA = 0.540$$

$$\text{Therefore, } W = 1 \frac{365 \times 10^{-9}}{0.540} = 675 \text{ nm}$$

2)

a)

i)



- ii) E1 is the cathode, E2 is the (grounded) anode.  $V_a$  is taken w.r.t the plasma potential, whereas  $V_C$  can be taken as w.r.t ground due to it being several orders of magnitude greater than the plasma potential:

$$V_C = V_a \left( \frac{A_{E2}}{A_{E1}} \right)^4 \Rightarrow V_C = -50 \times 10^{-3} \times 8^4 = -204.8 \text{ V}$$

- iii) There is more contamination from aluminium (possibly rust). These unwanted particles deposit on the wafer surface and acts as mask which blocks subsequent etching to the wafer surface below. This causes an uneven surface after etching, where certain parts are not etched due to this masking effect.
- iv) Power delivered to the etchants is reduced. Etchant ions are less energetic, which decreases the etch rate.

Higher temperature translates to higher kinetic energy of etchant ions, which increases the etch rate.

b)

- i) Step A: Diffusion and condensation. Step B: Nucleation.
- ii) Thermal evaporation uses thermal heating generated by passing large amount of current through a resistive metal. Electron beam evaporation achieves heating through concentrated electron beam. As such, localised heating of e-beam evaporation causes less contamination, especially compared to crucible contamination in thermal evaporation due to uniform heating of all substances in the chamber. Electron beam evaporation is more expensive compared to thermal evaporation.

c)

- i) Cathode.
- ii) Magnetic field helps to trap electrons near the target surface in a spiral motion. This increases the chances of encountering a neutral argon (etchant) atom and causes ionization. The generated secondary electrons will also be trapped in a spiral motion to cause subsequent ionizations. More argon ions will greatly enhance the sputter rate and increase the efficiency of the sputtering system.
- iii) Through high frequency oscillations of the rf supply, a slight increase in sputter rate will be observed. More importantly, it avoids charge build-up on the target, as it is the case if dc power supply is used to sputter insulators. As such, using rf supply allows insulators to be sputtered in addition to metals.

3)

a)

- i) Under dry oxidation, first calculate  $\tau$ .  $\tau = \frac{0.025^2}{0.024} + \frac{0.025}{\frac{0.024}{0.140}} = 0.171875 \text{ hr}$

After 30 mins (0.5 hr) of dry oxidation,

$$t_{ox} = \frac{-0.14 + \sqrt{0.14^2 + 4 \times 0.024 \times (0.5 + 0.171875)}}{2} = 0.075 \mu\text{m}$$

Now,  $t_{oxi} = 0.075 \mu\text{m}$  for wet oxidation.  $\tau = \frac{0.075^2}{0.529} + \frac{0.075}{\frac{0.529}{0.183}} = 0.0366 \text{ hr}$

After 120 mins (2 hr) of wet oxidation,

$$t_{ox} = \frac{-0.183 + \sqrt{0.183^2 + 4 \times 0.529 \times (2 + 0.0366)}}{2} = 0.9505 \mu\text{m}$$

Final oxide thickness is 0.9505  $\mu\text{m}$ .

- ii) Dry oxidation produces oxide with higher quality that is suitable as the gate oxide of MOSFETs (high breakdown voltage, high resistivity, etc.). Its slow oxidation rate also allows the film thickness to be controlled relatively easier.

b)

- i) When bombardment damage from ion implantation is unacceptable, or when a cheap and easy solution is required. It is also suitable if the total dose is not critical.
- ii) Step 1: pre-deposition of dose  $Q = \frac{2}{\sqrt{\pi}} N_s \sqrt{Dt}$   
Step 2: drive-in

$$N = \frac{Q}{\sqrt{\pi Dt}} \exp\left[-\frac{z^2}{4Dt}\right] = \frac{2}{\pi} N_s \exp\left[-\frac{z^2}{4Dt}\right]$$

Junction at  $z = 2 \mu\text{m}$ , boron concentration equals background concentration of  $2 \times 10^{16} \text{ cm}^{-3}$ .

$$2 \times 10^{16} = \frac{2}{\pi} \times 2 \times 10^{17} \times \exp\left[-\frac{(2 \times 10^{-4})^2}{4 \times 1 \times 10^{-12} \times t}\right] \Rightarrow t = 1.5 \text{ hr}$$

c)

- i) Ion channelling refers to a condition where implanted ions do not encounter any nuclei in a particular crystal direction. As the only stopping force is Coulombic interaction of electrons of the host atom, the implanted ions travel unusually far before stopping. This may cause the actual implanted depth to be larger than expected.

This can be avoided by surface amorphization to ensure nuclei will be available to slow down the implanted ions. Furthermore, tilting the surface at a small angle also randomizes the implant direction.

- ii) Ion implantation is preferred in the case of low temperature requirements. Complex profiles are easily achieved through multi-energy implants, which are unfeasible or impossible in thermal diffusion. Wider selection of masking materials are available.

4)

a)

- i) Diode current can be expressed as:

$$I = I_s \exp \frac{V_A}{V_T}$$

where  $I_s$  is the reverse saturation current,  $V_A$  is the applied voltage and  $V_T$  is the thermal voltage, assumed to be 25 mV at 300 K.

Given  $I = 0.9I_s$ ,  $V_A$  can be calculated as:

$$V_A = 25 \times 10^{-3} \times \ln(0.9) = -2.63 \text{ mV}$$

b)

- i)  $W_B \ll L_p$  is required to avoid recombination of holes injected into the base. Transistor action will not be observed if all injected minority carriers (holes) recombined in the n-type base region.
- ii) Advantage: high emitter current due to higher concentration gradient.  
Disadvantage: punch-through breakdown is more likely to happen, as the depletion regions on the base-emitter junction and base-collector junction meet more easily under smaller neutral base width.

c)

- i) Maximum capacitance is when there is no depletion capacitance (more capacitor in series means smaller capacitance).

Capacitance is only due to oxide capacitance.

$$C_{max} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{12 \times 10^{-7}} = 2.87625 \times 10^{-7} = 287.625 \text{ nF cm}^{-2}$$

- ii) Minimum capacitance includes depletion capacitance.

$$\frac{1}{C_{min}} = \frac{t_{ox}}{\epsilon_{ox}} + \frac{W_m}{\epsilon_s} \Rightarrow C_{min} = 8.501 \text{ nF cm}^{-2}$$

d)

- i) Given the gate is connected to the drain terminal:  $V_{GS} = V_{DS}$ . Therefore,  $V_{DS} > V_{GS} - V_T$  is always true for a positive  $V_T$ . Under such condition, MOSFET is in saturation.
- ii) Given  $V_{DS} = V_{GS} = 3$ . As  $V_{GS} < V_T$ , MOSFET is in cutoff region. Assuming no leakage current, ideal drain current of the MOSFET is 0.