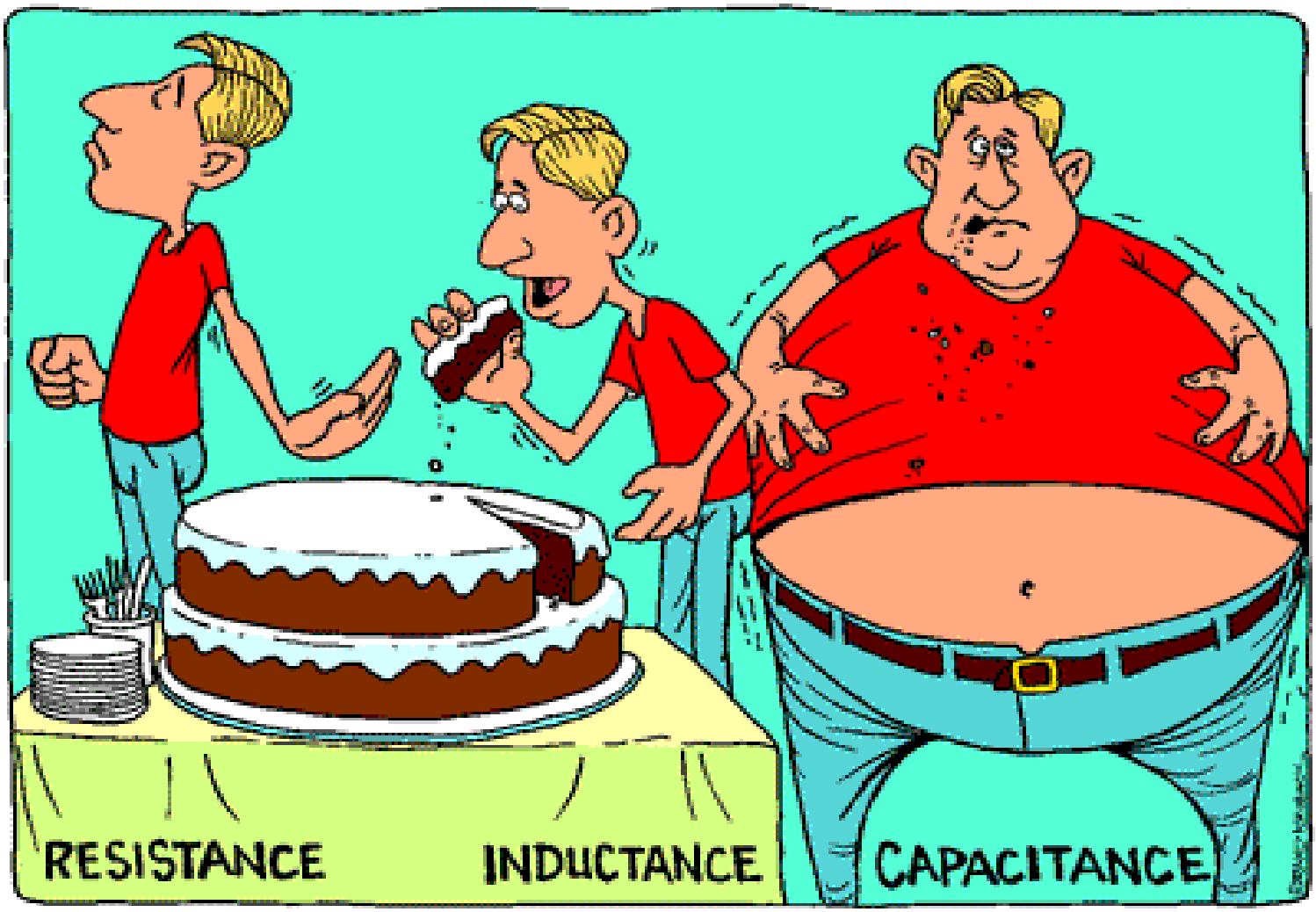
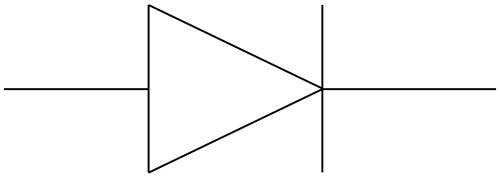
Capacitance of the P-N Junction

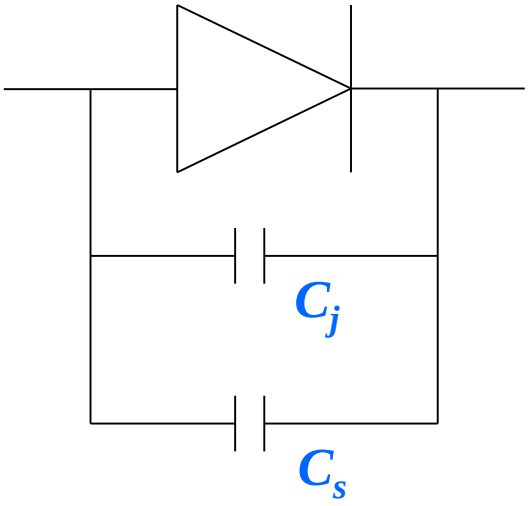


Capacitance of the P-N Junction

Two kinds of capacitances are associated with pn junctions. These are junction capacitance (or transition capacitance) and charge storage capacitance (or diffusion capacitance). These are modeled by two capacitors, C_j and C_s respectively, connected parallel to the p-n junction.



Ideal p-n junction



Practical p-n junction

Junction capacitance has physical characteristics similar to that of a parallel-plate capacitor and the expression that defines this capacitance is identical to that of a parallel-plate capacitor.

The storage capacitance also possesses the charge storing property of a capacitor but has no characteristics similar to those of a parallel-plate capacitor.

Capacitance is present in any device if a small change in the applied voltage ***dV*** across it results in a change in some charge ***dQ*** stored in it. By definition, the capacitance ***C*** is given by

$$C = \frac{dQ}{dV}$$

In the special case of a parallel plate capacitor, since ***Q*** is proportional to ***V***,

$$C = \frac{Q}{V}$$

$$Q \propto V \Rightarrow Q = kV$$

$$C = \frac{dQ}{dV} = k = \frac{Q}{V}$$

As the voltage ***V*** across a p-n junction varies, there are two stored charges in it, Q_j and Q_s, that will be affected. Hence, there are two associated capacitances.

$$C_j = \frac{dQ_j}{dV} \quad , \quad C_s = \frac{dQ_s}{dV}$$

From circuit point of view, the voltage across the p-n junction cannot change instantaneously due to the presence of C_j and C_s. This implies that there will be delay in circuits involving p-n junctions as the capacitors C_j and C_s will need time to be charged up or discharged.

Physically, this delay is related to the fact that a finite time is required for current to flow and charges to be transported to or away from the p-n junction, so that the stored charge Q_j and Q_s can be built-up or reduced to their new value upon changing ***V***.

Let's look at the source of Q_j and Q_s that give rise to C_j and C_s.

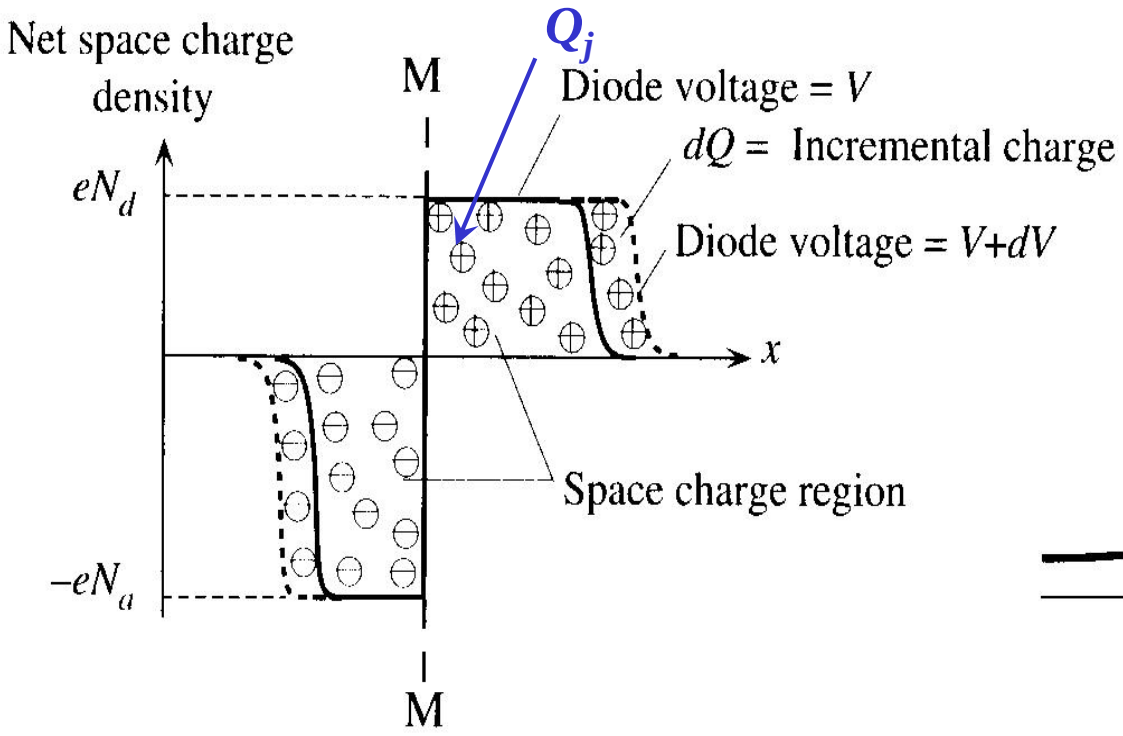
a) Junction Capacitance C_j

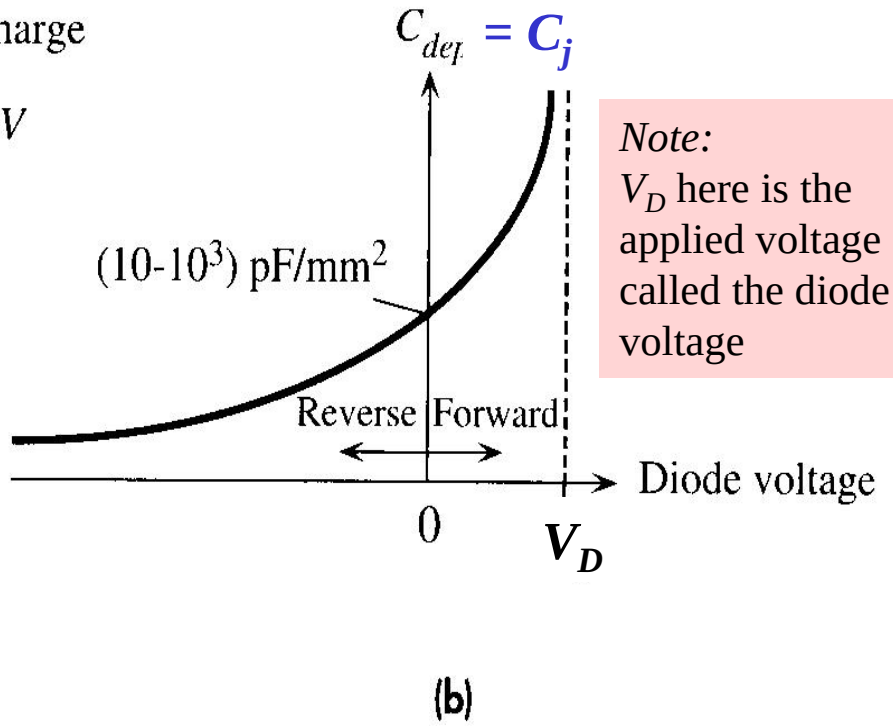
Upon changing the bias ***V*** across a p-n junction, the depletion width ***W*** and hence the amount of space charge in the depletion region will be affected.

The space charge Q_j in the depletion region ***W*** is given by

$$Q_j = |Q| = qAx_pN_a = qAx_nN_d$$

Under FB, ***W*** decreases and hence Q_j decreases. Under RB, ***W*** increases and hence Q_j increases. Thus, there is a capacitive effect associated with this change of charge Q_j. Unlike the parallel plate capacitor, Q_j is not proportional to ***V***, viz., non-linear, and hence the above eqn. must be used to determine C_j.





Note:
V_D here is the applied voltage called the diode voltage

The depletion region behaves like a capacitor.

(a) The charge in the depletion region depends on the applied voltage just as in a capacitor.
(b) The incremental capacitance of the depletion region increases with forward bias and decreases with reverse bias. Its value is typically in the range of picofarads per mm^2 of device area.

With applied bias V (+ve when FB and –ve when RB)

$$W = \left[\frac{2\varepsilon(V_o - V)}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) \right]^{1/2}$$

Now, recall the expressions for x_n and x_p

$$x_n = \frac{WN_a}{N_a + N_d} \qquad \text{and} \qquad x_p = \frac{WN_d}{N_a + N_d} \qquad \left(\begin{array}{l} x_n N_d = x_p N_a \\ x_n + x_p = W \end{array} \right)$$

Thus, the space charge Q_j can now be written as

$$Q_j = qA \frac{N_a N_d}{N_a + N_d} W = qA \frac{N_a N_d}{N_a + N_d} \left[\frac{2\varepsilon(V_o - V)}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) \right]^{1/2}$$

$$= A \left[2q\varepsilon(V_o - V) \frac{N_a N_d}{N_a + N_d} \right]^{1/2}$$

The junction capacitance C_j is thus given by

$$C_j = \left|\frac{dQ_j}{dV}\right| = \left|\frac{dQ_j}{d(V_o - V)}\right| = \frac{A}{2}\left[\frac{2q\varepsilon}{(V_o - V)}\;\frac{N_a N_d}{N_a + N_d}\right]^{1/2}$$

Note that C_j is voltage dependent ($\boldsymbol{C_j \propto (V_o - V)^{-1/2}}$).

Rearranging,

$$W = \left[\frac{2\varepsilon(V_o - V)}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2}$$

$$C_j = \varepsilon A\left[\frac{q}{2\varepsilon(V_o - V)}\;\frac{N_a N_d}{N_a + N_d}\right]^{1/2} = \frac{\varepsilon A}{W}$$

The expression for $\boldsymbol{C_j}$ is an exact analogy with that of a parallel plate capacitor, with the depletion width $\boldsymbol{W}$ corresponding to the plate separation of the capacitor.

Physically as we change the bias ***V*** across the p-n junction, it takes time for the majority carriers to respond in order to expose a larger space charge region under RB, or a smaller space charge region under FB.

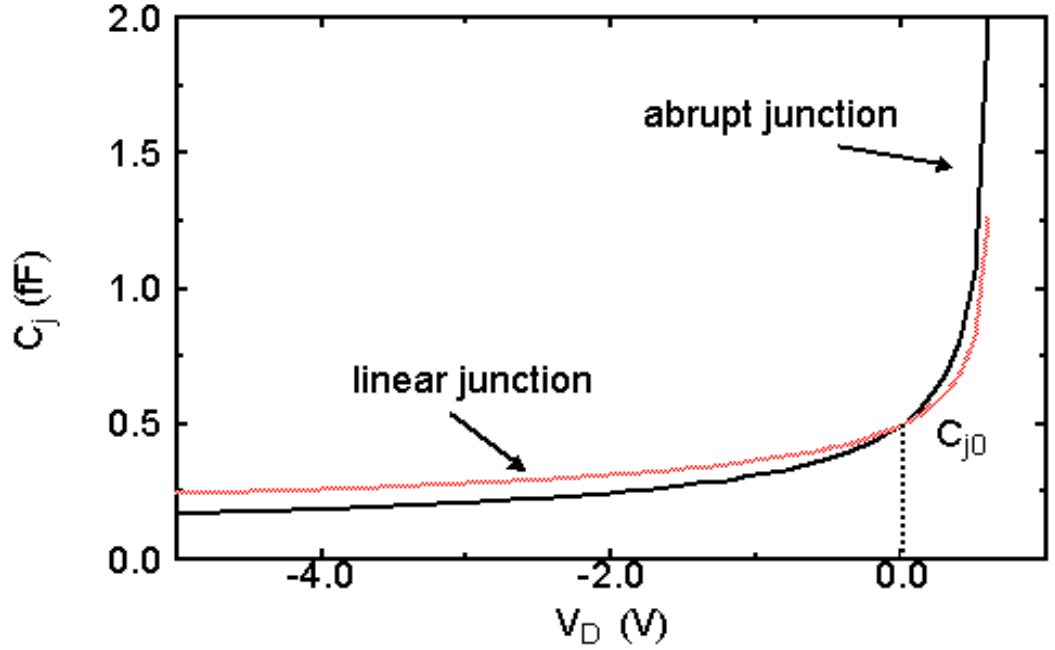
C_j is associated with this delay time for ***W*** to reach its steady state width. In other words, ***W*** cannot change instantaneously in response to a sudden change in the bias.

It is quite common to write the expression for C_j as a function of applied voltage. C_j is often written as

$$C_j(V) = C_{j0}\left[\frac{V_o}{V_o - V}\right]^{1/2} = \varepsilon A\left[\frac{q\boldsymbol{V_o}}{2\varepsilon \boldsymbol{V_o}(V_o - V)}\left(\frac{N_a N_d}{N_a + N_d}\right)\right]^{1/2}$$

where C_{j0} is the zero-bias junction capacitance, given by

$$C_{j0} = \varepsilon A\left[\frac{q}{2\varepsilon}\frac{1}{V_o}\frac{N_a N_d}{N_a + N_d}\right]^{1/2}$$



$$C_j(V) = C_{jo}\left[\frac{V_o}{V_o - V}\right]^m$$

m = 0.5: abrupt junction
m = 0.33: linear junction

Work Example

The doping densities of an abrupt-junction silicon P-N diode are N_a = $10^{17}/cm^3$ and $N_d = 8\times10^{15}/cm^3$ and the area of the junction is 2×10^{-5} cm^2. Calculate the junction capacitance at (a) zero bias, (b) RB of 6 V and (c) FB of 0.7 V. Assume $n_i = 10^{10}\,cm^{-3}$.

Solution: First, we have

$$C_j = \varepsilon A \left[\frac{q}{2\varepsilon(V_o - V)} \frac{N_a N_d}{N_a + N_d} \right]^{1/2} = \frac{\varepsilon A}{W}$$

Also, the equilibrium contact potential V_o is

$$V_o = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2} \right)$$

Calculate V_o as

$$V_o = 0.0259 \ln[(10^{17} \times 8 \times 10^{15})/(10^{10})^2] = 0.77 \text{ V}$$

(a) At zero bias

$$C_j = 11.8 \times 8.85 \times 10^{-14} \times 2 \times 10^{-5} \times \left[\frac{1.6 \times 10^{-19}}{2 \times 11.8 \times 8.85 \times 10^{-14} \times (0.77 - 0)} \cdot \frac{10^{17} \cdot 8 \times 10^{15}}{10^{17} + 8 \times 10^{15}} \right]^{1/2}$$

$$C_j = 0.56 \text{ pF}$$

(b) With RB of 6 V,

$$C_j = 11.8\times8.85\times10^{-14}\times\ 2\times10^{-5}\times \left[\frac{1.6\times10^{-19}}{2\times11.8\times8.85\times10^{-14}\,(\,0.77\ +\ 6)}\cdot\frac{10^{17}\cdot8\times10^{15}}{10^{17}\ +\ 8\times10^{15}}\right]^{1/2}$$

$$C_j = 0.188 \text{ pF}$$

(c) With FB of 0.7 V,

$$C_j = 11.8 \times 8.85 \times 10^{-14} \times \ 2 \times 10^{-5} \times \left[\frac{1.6 \times 10^{-19}}{2 \times 11.8 \times 8.85 \times 10^{-14} \cdot (\ 0.77 - 0.7\ )} \cdot \frac{10^{17} \cdot 8 \times 10^{15}}{10^{17} + 8 \times 10^{15}} \right]^{1/2}$$

$$C_j \ = 1.85 \text{ pF}$$

Note that junction capacitance in FB is much larger than that in RB as the width of the depletion region is much smaller in FB.

b) Charge Storage Capacitance C_s

The application of FB to a diode results in a reduction in the barrier height, a reduction in the depletion region width, and an injection of majority carriers across the depletion region into the opposite region, where they are stored as excess minority carriers. The **density of the excess minority carriers increases with increase in the FB.**

Note that with changing bias ***V***, there will be a change in the concentration of the excess minority carriers stored at both sides of the junction, near the depletion region edges. The concentration is increased upon increasing the FB and decreased upon decreasing the FB.

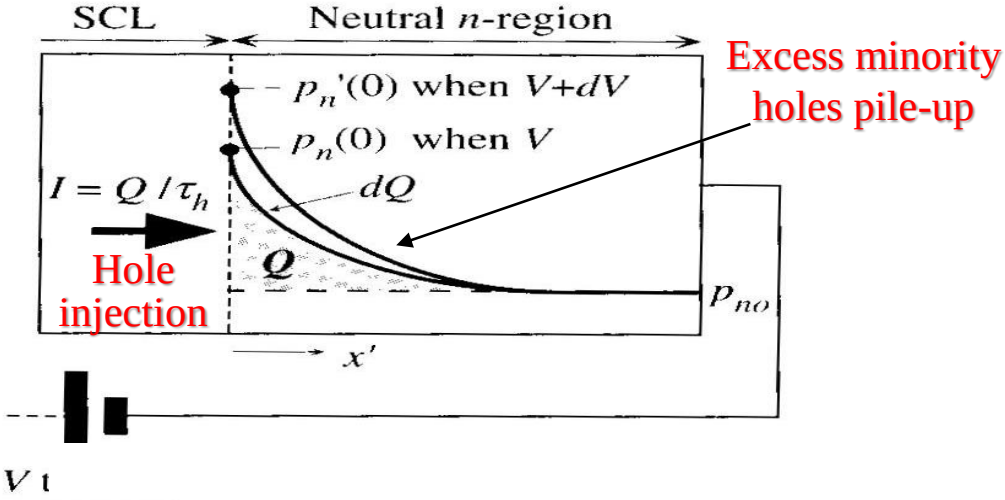


Figure 6.12 Consider the injection of holes into the *n*-side during forward bias. Storage or diffusion capacitance arises because when the diode voltage increases from *V* to *V* + *dV*, more minority carriers are injected and more minority carrier charge is stored in the *n*-region.

The increase in the minority carrier concentration does not take place instantaneously with a sudden change in FB.

A delay time is involved in the minority carrier concentration attaining a steady-state. This delay is due to capacitive effect as a result of stored minority carrier charges in the neutral n and p regions. This is the origin of storage capacitance.

The <u>total excess stored charge for minority holes at n-side</u> $\boldsymbol{Q_p}$ is

$$Q_p = qA\int_0^\infty \Delta p_n\,(x')\,dx' = qA\Delta p_n\left(x'=0\right)\int_0^\infty e^{-x'/L_p}\,dx'$$

$$= qAL_p\Delta p_n\left(x'=0\right) \qquad \left(\Delta p_n(x')=\Delta p_n\left(x'=0\right)e^{-x'/L_p}=p_{n0}\left(e^{qV/kT}-1\right)e^{-x'/L_p}\right)$$

The <u>total excess stored charge for minority electron at p-side</u> $\boldsymbol{Q_n}$ is

$$Q_n = -qA\int_0^\infty \Delta n_p\,(x'')\;dx_p = -qA\Delta n_p\left(x''=0\right)\int_0^\infty e^{-x''/L_p}\,dx''$$

$$= -qAL_n\Delta n_p\left(x''=0\right) \qquad \left(\Delta n_p(x'')=\Delta n_p\left(x''=0\right)e^{-x''/L_n}=n_{p0}\left(e^{qV/kT}-1\right)e^{-x''/L_n}\right)$$

Here, $\Delta p_n(x')$ and $\Delta n_p(x'')$ are the steady state profiles of the minority holes and electrons respectively, given by

$$\Delta p\,(x') \;=\; \Delta p_n\left(x'=0\right)e^{-x'/L_p} \;=\; p_{n0}\left(\,e^{qV/kT}-1\,\right)e^{-x'/L_p}$$

$$\Delta n\,(x'') \;=\; \Delta n_p\left(x''=0\right)e^{-x''/L_n} \;=\; n_{p0}\left(\,e^{qV/kT}-1\,\right)e^{-x''/L_n}$$

Let Q_s denote the total excess charge stored associated with the minority carriers, viz., $Q_s = Q_p + Q_n$.

Consider the case of a p^+n junction under FB. Recall that the hole injection current will dominate. This transforms to $\Delta p_n >> \Delta n_p$, and hence $Q_p >> Q_n$. (and $I_p(x' = 0) >> I_n(x'' = 0)$ generally).

Hence,

$$C_s = \frac{dQ_s}{dV} \approx \frac{dQ_p}{dV}$$

Recall $\Delta p_n\left(x'=0\right) = p_n(x'=0) - p_{n0} = p_{n0}\left(e^{qV/kT} - 1\right)$

$$\approx p_{n0}\, e^{qV/kT}$$

Thus, the storage charge capacitance C_s associated with this change of storage charge is

$$C_S = \frac{d\,Q_p}{d\,V} = \frac{q^2}{kT} AL_p p_{n0} e^{qV/KT} \approx \frac{q}{kT} Q_p$$

Note: $\boldsymbol{Q_p = qAL_p \Delta p_n\left(x'=0\right)}$

$$I_p\left(x'=0\right)_{diff} = qA\frac{D_p}{L_p}\Delta p_n\left(x'=0\right)e^{-x'/L_p} = qA\frac{D_p}{L_p}\Delta p_n\left(x'=0\right)$$

For p^+n junction hole injection current will dominate and hence the total current I is given by

$$I \approx \frac{q\ A\ D_p}{L_p}\ \Delta p_n\left(x'=0\right) = \frac{qAL_p\Delta p_n\left(x'=0\right)}{\tau_p} \approx \frac{Q_p}{\tau_p}$$

since $L_p = (D_p \tau_p)^{1/2}$

Thus, $Q_p \approx I\tau_p$.

Hence, C_s can also be expressed in terms of I and τ_p as

$$C_s = \frac{q}{kT} I\tau_p$$

It can be seen that C_s can be very large under FB due to the large I. Physically, this can be understood because the storage charge depends exponentially on the bias voltage V under FB, meaning that there will be a large change in the amount of storage charge (dQ_s) of the minority carriers with changing bias (dV), resulting in a large C_s. The C_s will impose a serious limitation for a FB biased p-n junction in high frequency applications.

The total capacitance across the pn junction is $C_T = C_j + C_s$.

During FB, C_s is dominant ($C_s >> C_j$) due to the large change in the amount of storage charge of the minority carriers, hence $C_T \approx C_s$.

During RB, C_s is not critical ($C_s << C_j$) since there is only very small change in the amount of storage charge of the minority carriers. In comparison, the junction capacitance C_j dominates under RB, viz., $C_T \approx C_j$.

The presence of these capacitances will limit the speed of operation of any circuits using p-n junction diodes.

Work Example

The doping densities of an abrupt-junction silicon PN diode are N_a = 10^{17}/cm^3 and $N_d = 8 \times 10^{15}$/cm^3 and the area of the junction is 2×10^{-5} cm^2. The lifetime of holes in the n region is 0.1 μs. Given the diffusion constant for holes in N is 16 cm^2/s, calculate, at room temperature, the storage capacitance at (a) FB of 0.6 V and (b) 0.65 V. Assume $n_i = 10^{10}$ cm^{-3}.

Solution: Recall

$$C_S = \frac{q^2}{kT} AL_p p_{n0} e^{qV/kT}$$

Equilibrium density of holes in the N region is

$p_{n0} = n_i^2/N_d = 10^{20}/8 \times 10^{15} = 1.25 \times 10^4$ /cm^3

Also, $L_p = (D_p \tau_p)^{1/2} = (16 \times 0.1 \times 10^{-6})^{1/2} = 1.26 \times 10^{-3}$ cm

(a) When the FB is 0.6 V, storage capacitance is $C_S = \frac{q^2}{kT} AL_p p_{n0} e^{qV/kT}$

$$C_s = \frac{(1.6\times10^{-19})^2}{0.026\times1.6\times10^{-19}} \cdot 2\times10^{-5} \times 1.26\times10^{-3} \times 1.25\times10^{4} \cdot e^{0.6/0.026}$$

$$C_s = 20.4 \text{ pF}$$

(b) Similarly, at FB of 0.65 V

$$C_s = \frac{(1.6\times10^{-19})^2}{0.026\times1.6\times10^{-19}} \cdot 2\times10^{-5} \times 1.26\times10^{-3} \times 1.25\times10^{4} \cdot e^{0.65/0.026}$$

$$C_s = 139.6 \text{ pF}$$

Note the large value of C_s. It is in fact much larger than C_j in FB (compare with the previous example for C_j value. It was 1.85 pF at a FB of 0.7 V).