NANYANG TECHNOLOGICAL UNIVERSITY SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

ACADEMIC YEAR 2020-2021
SEMESTER 1

EE3019 INTEGRATED ELECTRONICS

TUTORIAL 5

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1. (a) Draw a circuit schematic of a SRAM cell based on 2-MOS transistor 2-polysilicon resistor load structure.

   (b) A 16K SRAM is realized by the cells given in (a). This SRAM IC dissipates 0.1W. Determine the resistance of the polysilicon load resistor. Assume that the MOS transistors are ideal, and that V_{DD} = 5V.

   (Ans: 4.096MΩ)

   Hint : Work out the operating region of the transistors

   (c) A 16K x 1 SRAM memory (each cell comprises 4 MOS transistors and the select line comprises 2 MOS transistors) is organised as a square matrix with 128 cells on each side, occupying a total IC area of 2 mm x 2 mm. The select line is 2μm wide and the select transistor gates are 2μmx2μm. The polysilicon select line is 22 Ω/□, the capacitance to substrate for the polysilicon is 0.08fF/μm² and the data capacitance is 1fF/μm². The select line is driven from one end.

   Assuming a simplistic model with the total select line resistance and capacitance represented as a lowpass *RC* circuit, determine the select line delay. For this simple model, assume that this delay is equal to the 10% -90% rise time at the far end (of the select line) and assume that the select line is driven by an ideal voltage step. (61.2 ns).

   Note: Data capacitance is the capacitance between the polysilicon gate and the channel of the transistor under the gate

   Hint: Determine the equivalent R and C and determine the 10% -90% rise time.

2. A dynamic CMOS Read Only Memory (ROM) has been designed with a core array consisting of 64 rows with a pitch of 12μm and 64 columns with a pitch of 10μm, as shown in Figure 1. All of the nMOS transistors have channel widths *W*=4μm, channel length *L*=2μm and source/drain lengths Y=5μm. As a designer, determine the row access time of the row 64 in the ROM. Assume that row 64 is running over 30 nMOS transistors and column 64 has 20 nMOS transistors connected to it. Also assume that the row capacitance of each cell is dictated primarily by the thin oxide capacitance of the nMOS transistor (i.e. the polysilicon capacitance outside the active region is negligible). Device parameters are as follows:

$C_{ox} = 350\mu F/m^2$

$C_{poly} = 2.2pF/cm^2$ *and* $R_{poly} = 25\Omega$ / sq

Polysilicon line width = 2μm

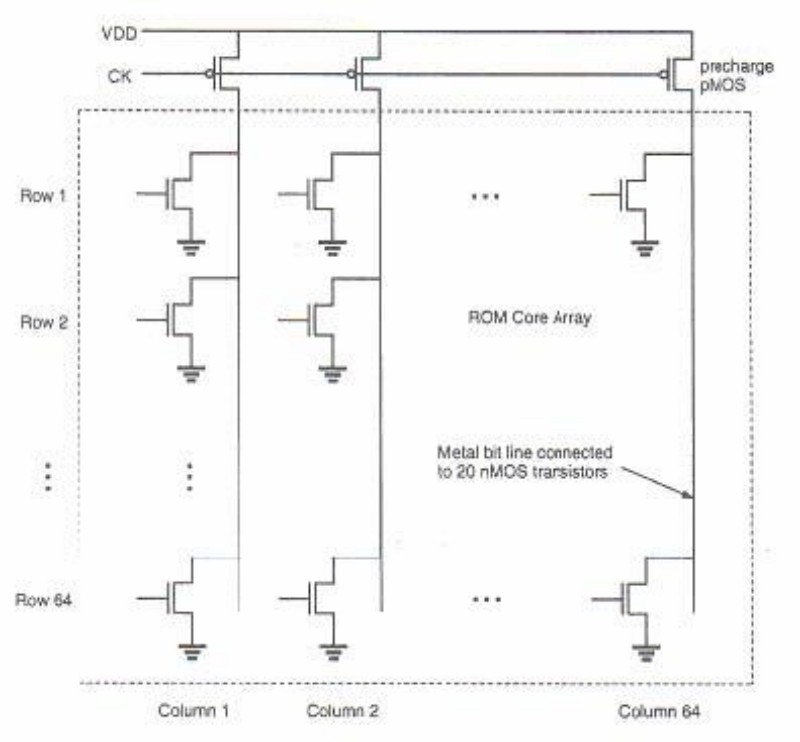

Figure 5.1 A dynamic CMOS Read Only Memory (ROM)