NANYANG TECHNOLOGICAL UNIVERSITY

EE2073

Introduction to EEE Design and Project

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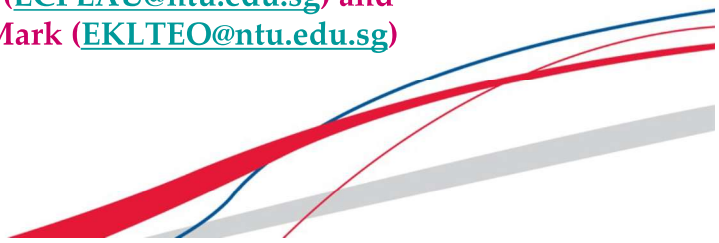
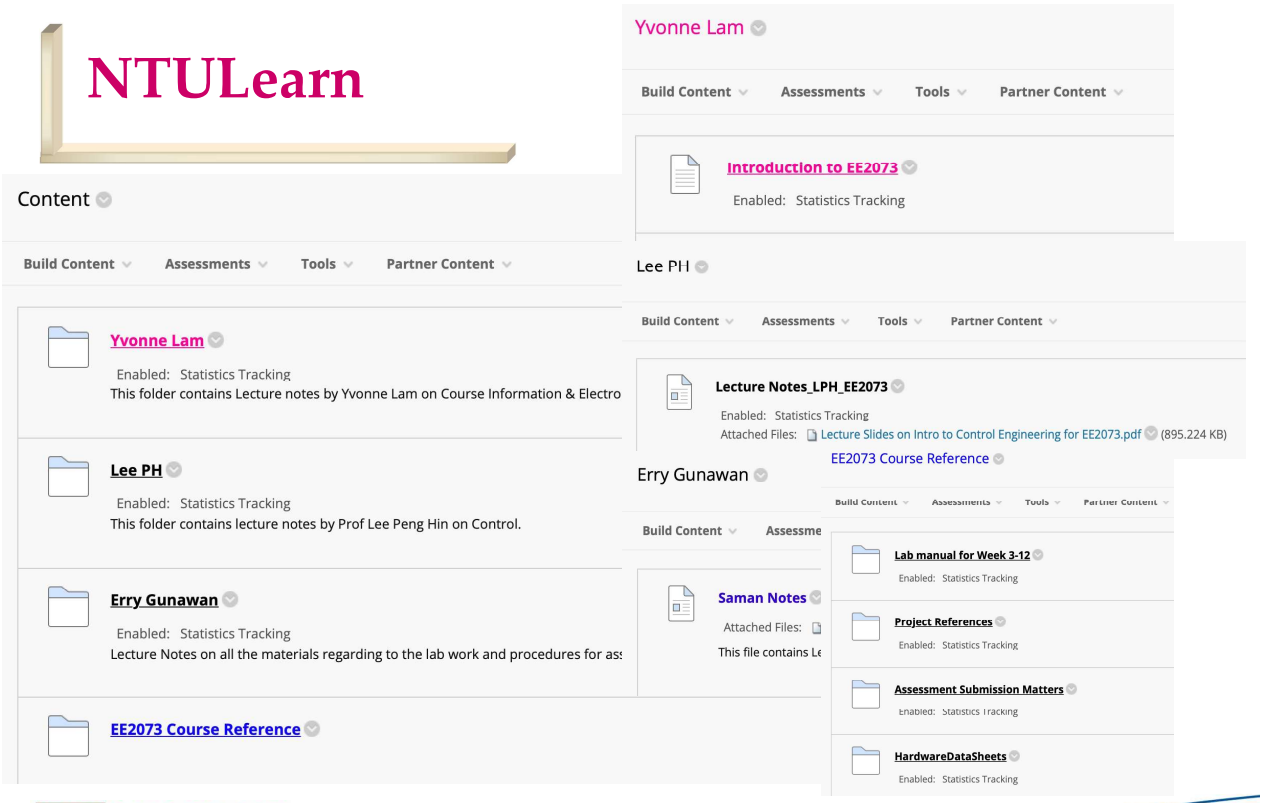


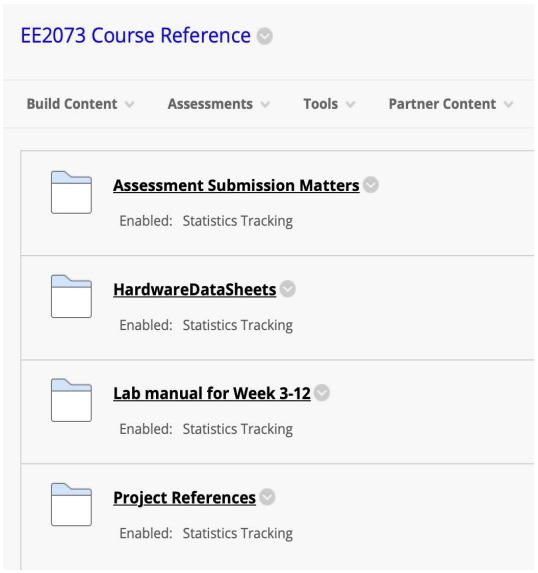
Course Structure

- Number of Academic Units - 2 AU
- Course duration - 36 Hours
- Course schedule
  - Week 1-2: Lectures. (**YL**/LPH, **YL**/EG)
  - Week 3,5: Design classes – LabVIEW programming and exercise, ELVIS instrumentation and exercise.
  - Week 6: LabVIEW/ELVIS simulation and **Quiz**.
  - Week 7-12: Project classes – Project activities including design, development, test and evaluation of subsystems and the integration of hardware and software subsystem modules to form a complete system.
  - Week 13: Project demonstration and report.

NTULearn



Reference Materials



Report template; How to upload weekly logbooks; and Turnitin Guide for EE2073 Students

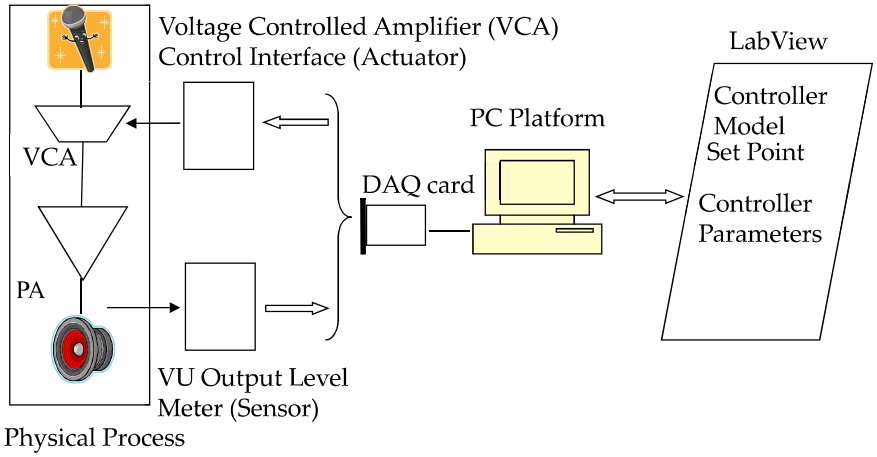
OP275; CA3140; LM380 and THAT_2180_Series_Datasheet

Lab Manual

Data Acquisition Using LabVIEW and ELVIS; Extra Notes on EE2073; Introduction to LabVIEW and Introduction to NI ELVIS II

Syllabus – Project Classes (3 Hours per week, week 3 – 13)

- Automatic Volume Control for Audio Amplifier System
- A discrete-time sampled-data digital control system based on **LabVIEW** and **ELVIS**



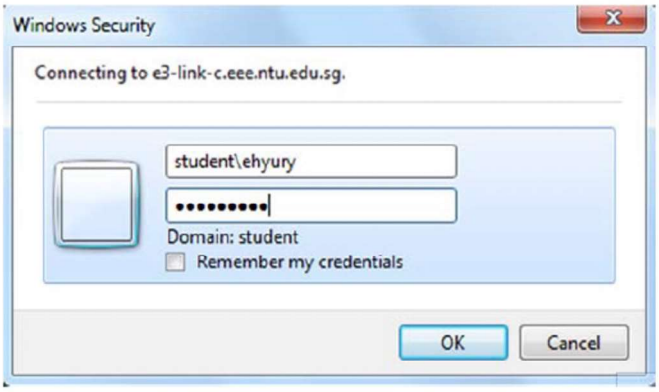
Assessment Scheme

- Design/project practical assessment (**75%** of final mark)
  - Week 3-12: practical skills, understanding, participation, plus …
  - Week 3-12: results/progress on-site, in weekly eLog uploaded
  - Week 13: project demonstration, Q&A
- LabVIEW/ELVIS assessment (**10%** of final mark)
  - LabVIEW/ELVIS quiz will be conducted in week 6
  - Closed book quiz must be done with the lab computer
  - Students must submit their solutions within the allocated time
- Project report assessment (**15%** of final mark)
  - Individual project report for project activities
  - Content should be consistent with weekly logbook uploaded
  - Subjected to Turnitin originality checking on NTULearn
- Necessary conditions to **PASS** the course:
  - Attendance of at least **80%** in design/project practical sessions
  - Individual project report must be submitted by 5pm Mon of week 14

eLog system

1. Login to https://eeen40003.eee.ntu.edu.sg/elogs
2. Key in your CITS username and password

   (*to access the system from outside NTU, user name to use VPN application as specified by CITS web)



Upload INDIVIDUAL Weekly Logbook

- Before END of each session, upload your logbook file(s) to file server. (Regardless whether all tasks are completed)
- Each file **< 4MB** in file size. PDF and WORD are supported.
- Upload all your achievement for the day and no further changes can be made until the next new session.
- Any further changes / revised logbook can only be uploaded at the next new session.
- After upload, download the file to check – ensure your supervisor is able to access.
- If you fail to upload the logbook by the end of each practical session, you may be deemed to have attained unsatisfactory progress for that particular session.

Upload INDIVIDUAL Weekly Logbook

- Schematics or snap photos of circuits and instrument setups.
- Screen/window capture of waveforms and run-time outputs.
- Tabulation/graphs of measurement results and theoretical calculations.
- Record of observation key points during experiments.
- LabVIEW/other programs, block diagrams, front panels, etc.

Week 13: Project Report

- Upload softcopy in **Word** doc to NTULearn for Turnitin originality checking https://NTULearn.ntu.edu.sg
- NTULearn can be accessed via NTU Intranet, iNTU (https://iNTU.ntu.edu.sg).
- Refer to "Turnitin Guide for EE2073 Students.pdf" for procedure.
- The submission requires each student to attach a similarity report generated by TURNITIN for checking similarity. You need to revise the report if the similarity is more than 20%.
- If requested by your lab supervisor, you may also need to submit hardcopy (double-sided, stapled) to the lab, attached with the first page of Turnitin originality report.
- Submit report (via NTUlearn.ntu.edu.sg) by 5pm Mon of week 14.

Lab Locations

- Computer Engineering: S2-B4c-15, or
- Electric Power Research: S2-B5c-02



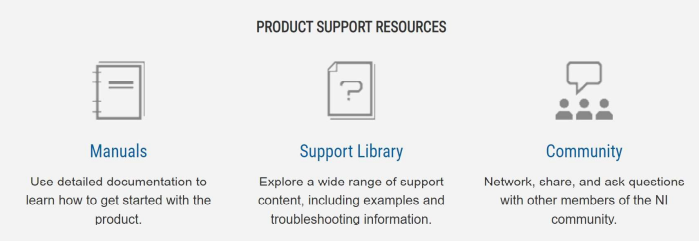
- Tel: +65 6790 5446
- To spend extra time on the project, arrangement can be made with lab staff in advance – subject to availability.
- There will be no supervision for these arrangements.

Useful Information

- Briefing videos @ youtube
- Lab Sessions @ S2-B4c-15 / S2-B5c-02
- eLog submission: https://eeen40003.eee.ntu.edu.sg/elogs
- Week 6: Quiz (MCQ) – all materials from week 1-5
- Formal Report Submission Deadline: 5pm Mon, Week 14.
- Formal reports are to be submitted online as Assignment from NTULearn for plagiarism check (do not submit to eLog system).
- Makeup should be arranged and performed for the student with any valid reasons, such as absence due to school approved activities or medical reasons.
- The absentee need to contact lab staff for make-up arrangement.
- Absent more than TWO lab sessions means FAIL of this subject.
- Non-submission of final project report means FAIL of this subject.

Download LabVIEW: Please explore!

- Latest download (trial, 45 days validity) available from: http://www.ni.com/download-labview/?gclid=Cj0KEQjwo7auBRCOtoqn_s-G7aMBEiQAxArNrOzGlQmJoubZtT8FqfouS0IeqCRMmEFNt5PC3zxSzqIaAjy48P8HAQ
- There are many tool boxes that support specific applications.
- There are also many sources for beginner to learn.
- Many working sample programs are also available for each function provided by the software.

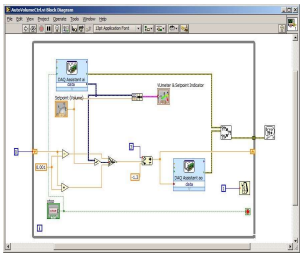


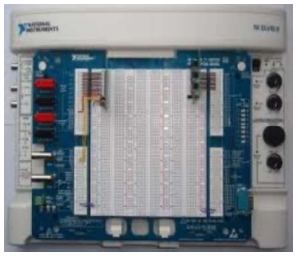
Syllabus – Lectures (3 Hours per week, Week 1 – 2)

- Topic 1: Introduction and detailed information on this project.
- Topic 2: Principle of feedback control system (LPH)
- Topic 3: Electronic Circuit and System Design
  - Electronic circuit and system designs for typical electrical/electronic system functionalities
  - Using OP AMPS and other commercially available IC building blocks.
- Topic 4: Data Acquisition System and Application (EG/SS)
  - Data acquisition by sampling for realizing discrete-time signals and sampled-data systems
  - Application to digital control and signal processing system designs

Syllabus – Design Classes (3 Hours per week, week 3 – 6)

- LabVIEW as the graphical programming system and application software development environment.
- Students need to learn the basic LabVIEW programming skills from "Introduction to LabVIEW", which is in the NTULearn folder.
- Data acquisition system, setup and practical applications using ELVIS (Educational Laboratory Virtual Instrumentation Suite).
- Use of LabVIEW and ELVIS for data acquisition application development.



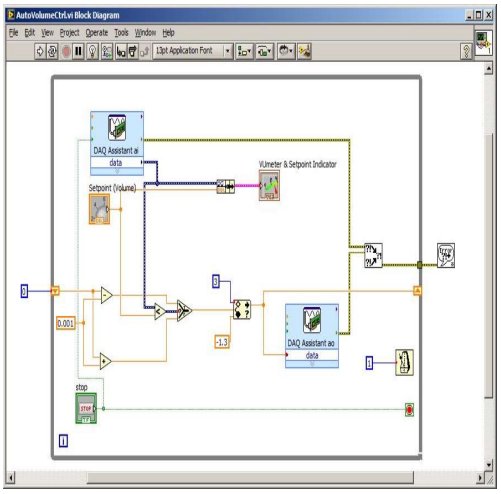


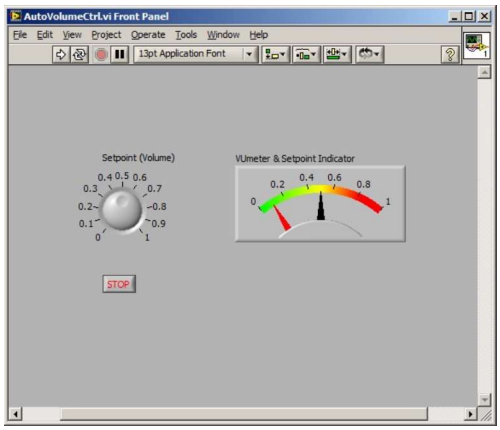
Project Overview

- Objective: design a controller that automatically adjusts the gain of audio amplifier system to give constant level of audio output.
- Discrete-time sampled-data digital control system design using LabVIEW and ELVIS (Software/Hardware)
- Circuit design and implementation (Hardware)
  - Voltage controlled amplifier (VCA)
  - Power amplifier (PA)
  - Volume unit (VU) meter
- Manual and automatic volume control system design using LabVIEW and ELVIS (Software/Hardware)
- Test, evaluation and demonstration of project using LabVIEW and ELVIS (Software/Hardware)
- Refer EE2073 Project Manual.pdf

LabVIEW and ELVIS

- LabVIEW Programming
- Automatic Volume Control





Reminders

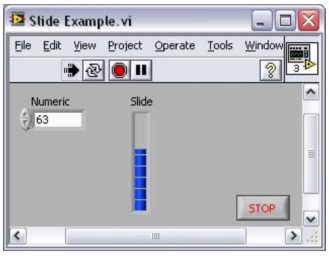
- Bring smartphones to take photos of your work, which may be used for your weekly logbook.
- Bring thumb drive to store your work and the weekly logbook.
- Study the instruction manual before and during class.
- Students are allowed to take home the breadboard and/ PCB, which should be carefully kept.
- Return all boards and components after demo done in week 13.
- Any problem, please first contact your lab supervisor.
- Safety first! Follow lab rules (proper attire/shoes)

Lab Work in Each Week

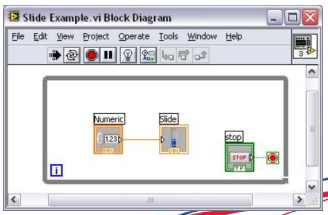
- The lab manual provides detailed instructions for students to follow.
- Carefully read the manual and know EXACTLY what to do.
- At the end of instructions for each week, there are open questions to answer, which is OPTIONAL.

Week 3: LabVIEW Programming

- LabVIEW programs are called Virtual Instruments (VIs) and Each VI has 2 Windows
- Front Panel
  - User Interface (UI)
    - Controls = Inputs
    - Indicators = Outputs



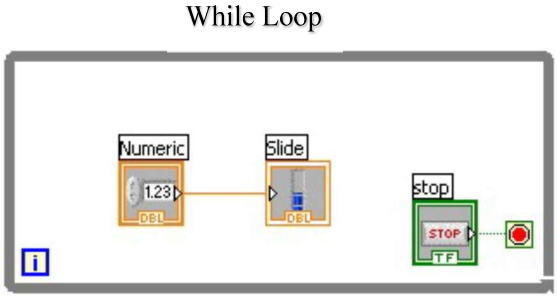
- Block Diagram
  - Graphical Code
    - Data travels on wires from controls through functions to indicators
    - Blocks execute by Dataflow



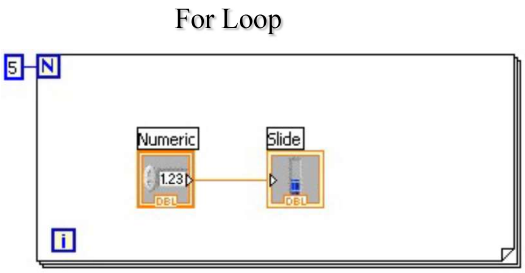
Introduction to LabVIEW.pdf

Week 3: LabVIEW Programming

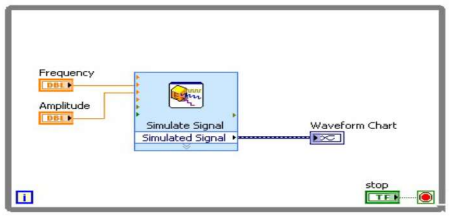
- Loops
  - While Loops
    - * terminal counts iterations
    - * Always runs at least once
    - * Runs until stop condition is met

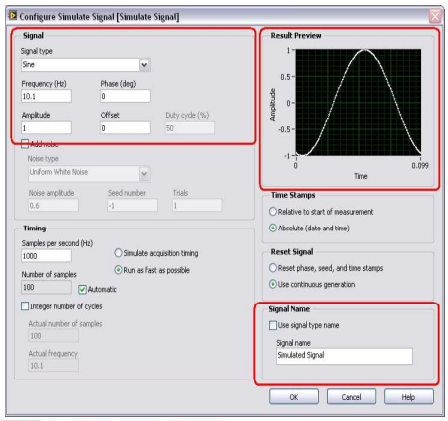


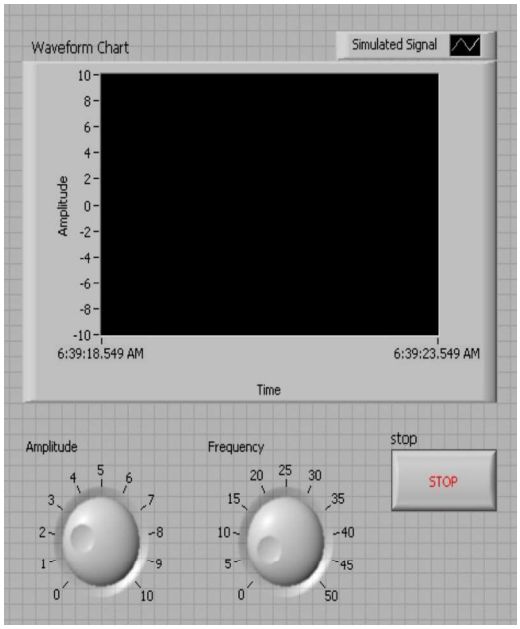
- For Loops
  - * terminal counts iterations
  - * Run according to input of count terminal



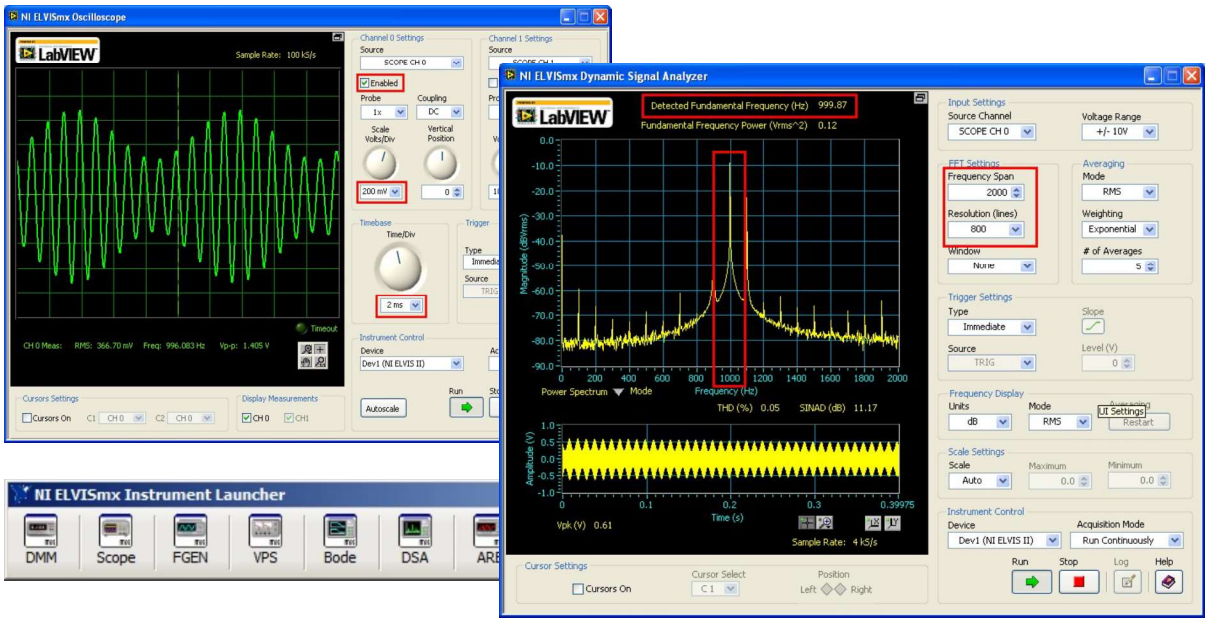
Week 3: LabVIEW Exercise







Week 3: ELVIS Instrumentation+Exercise



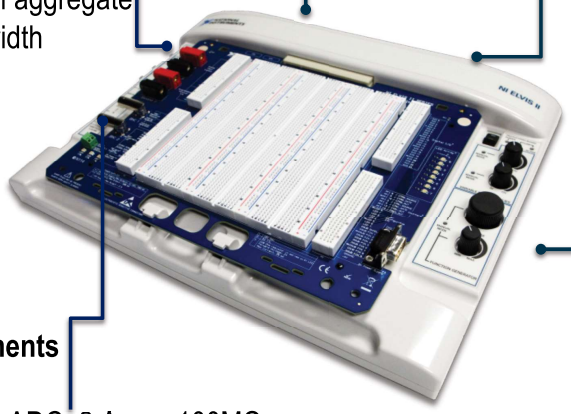
Week 3: ELVIS Instrumentation
Hardware Specifications

Introduction to NI ELVIS II.pdf

Oscilloscope
- 16 bit resolution
- 1.25 MS/s single channel, 500kS/s two channel aggregate
- 1 to 1.5 MHz Bandwidth
- 1x and **10x probe**
- ±10 V input range
- AC/DC coupling
- BNC connection

Internal Circuit Protection
- Resettable fuses

USB Connectivity
- Plug-and-play capability
- USB 2.0 Connection

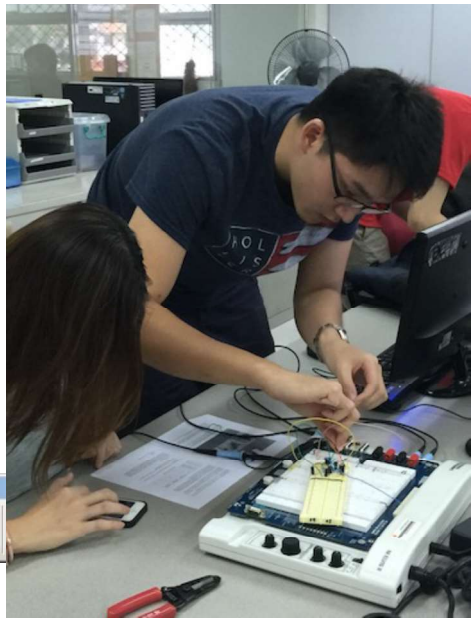


Function Generator
- **10-bit**
- **±5V range**
- **0.2 Hz to 5 MHz Sine**
- **0.2 Hz to 1 MHz Triangle/Square**
- Software or manual control
- BNC or prototyping board connection

Digital Multimeter
- **Isolated measurements**
- **5 digit resolution**
- 60 VDC, 20Vrms, 2 ADC, 2 Arms, 100MΩ

Week 3: ELVIS Instrumentation
NI ELVISmx Instrument Launcher

- Digital Multimeter (DMM)
- Oscilloscope (Scope)
- Function Generator (FGEN)
- Variable Power Supplies (VPS)
- Bode Analyzer (Bode)
- Dynamic Signal Analyzer (DSA)



Week 3: ELVIS Exercise

- Amplitude Modulation (AM) – analog modulation scheme where the amplitude of a fixed-frequency carrier signal is continuously varied to represent data

$$y(t) = C\sin(\omega_c t) + M\frac{\cos(\phi - (\omega_m - \omega_c)t)}{2} - M\frac{\cos(\phi + (\omega_m + \omega_c)t)}{2}$$

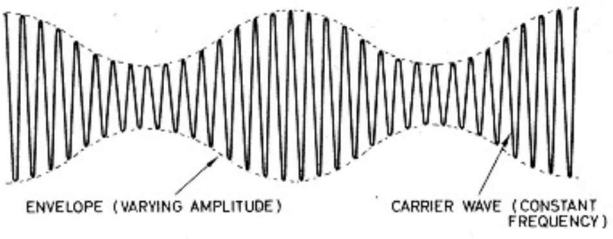


Figure 1. Time domain of an AM signal

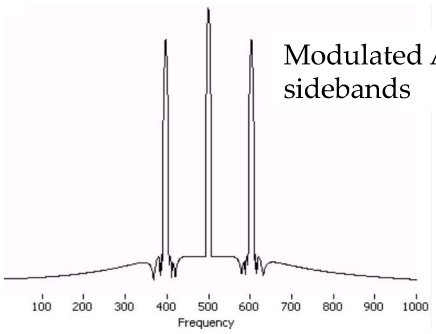
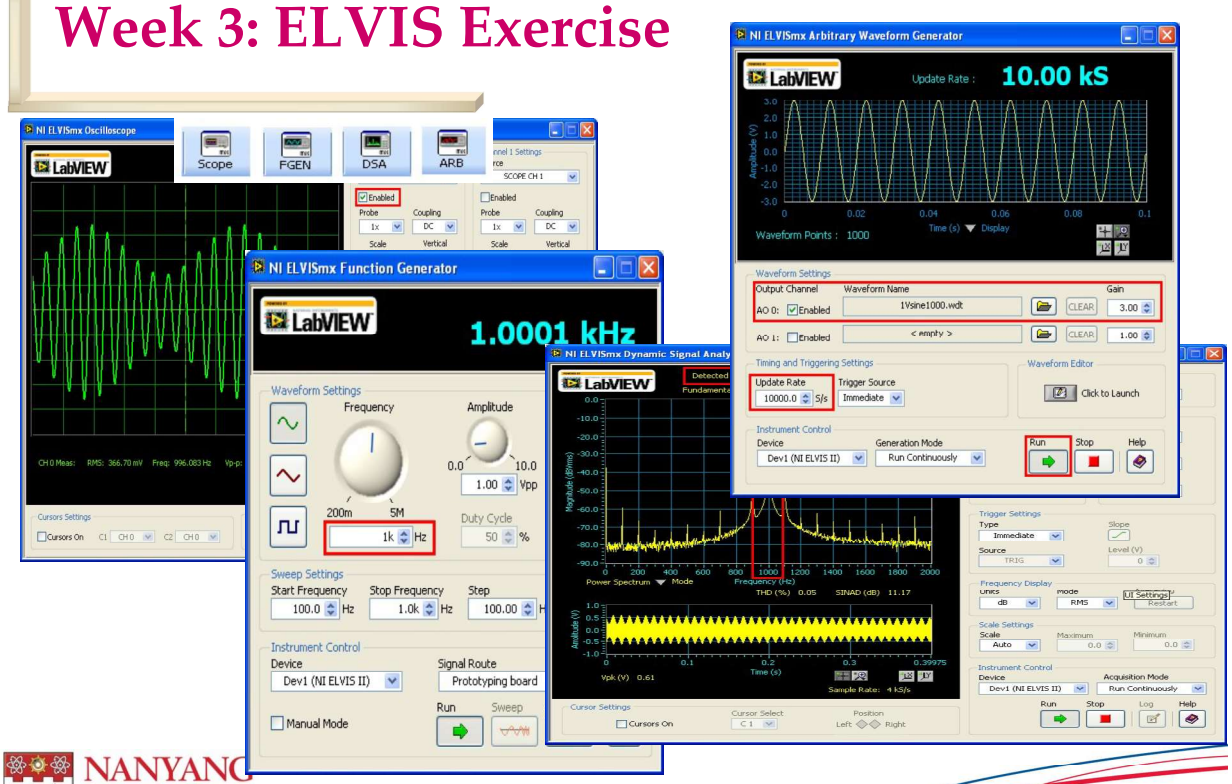
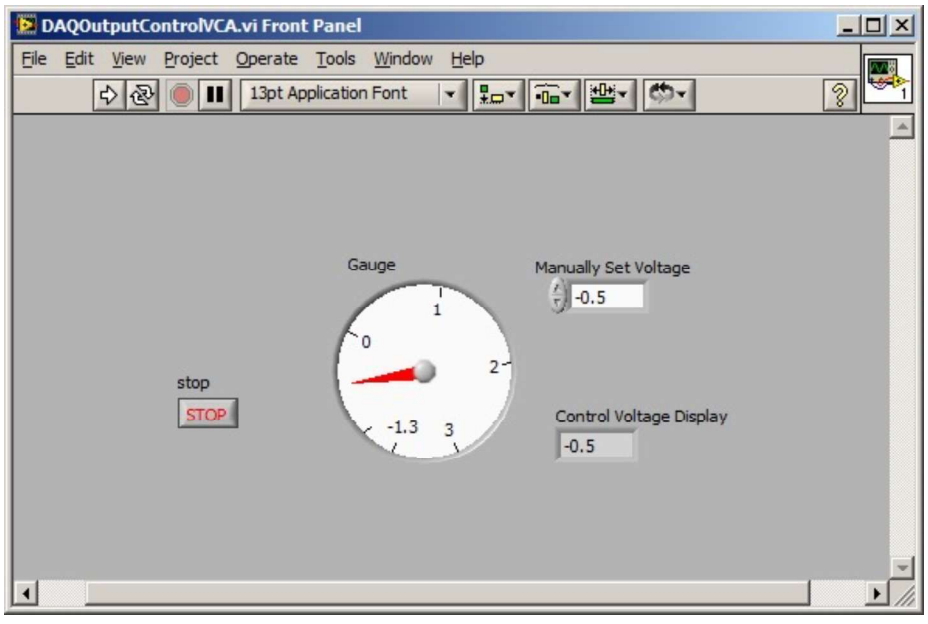


Figure 2. Frequency domain of an AM signal

Week 3: ELVIS Exercise



Week 5: DAQ using LabVIEW/ELVIS

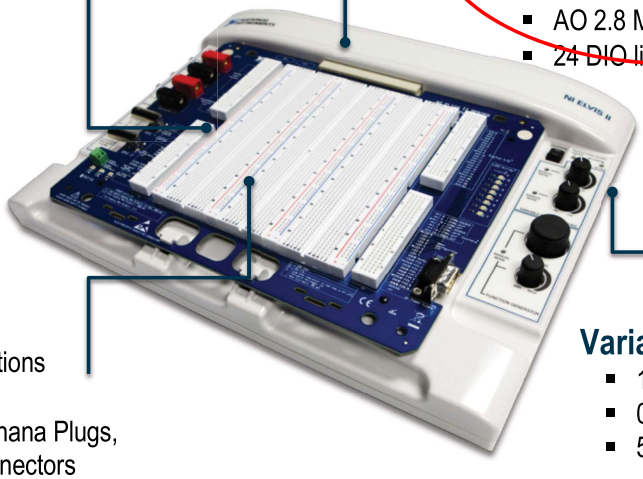


Week 5: DAQ using LabVIEW/ELVIS
Integrated DAQ on ELVIS

Integrated DAQ
- AI sampling rate 1.25 MS/s single channel, 500kS/s two channel
- 16 bit resolution
- AO 2.8 MS/s update rate
- 24 DIO lines, 15 PFI, 2 CTR

Impedance Analyzer
- 0.2 Hz to 35 kHz Range
- NPN, PNP, Diode

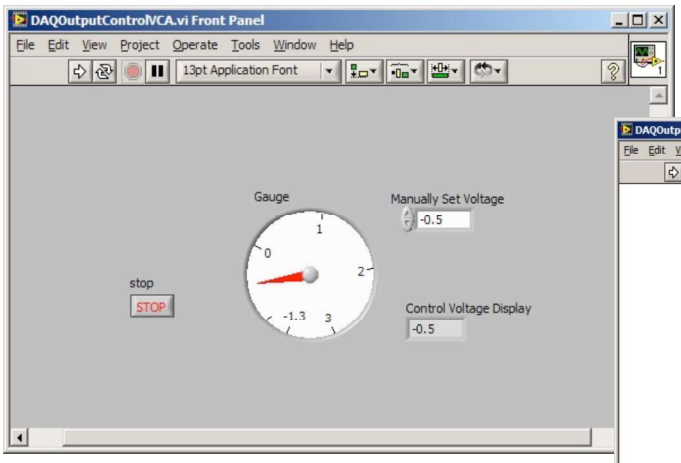
Other Analyzers:
- Bode Analyzer
- 2-wire Current Voltage Analyzer
- 3-Wire Current Voltage Analyzer



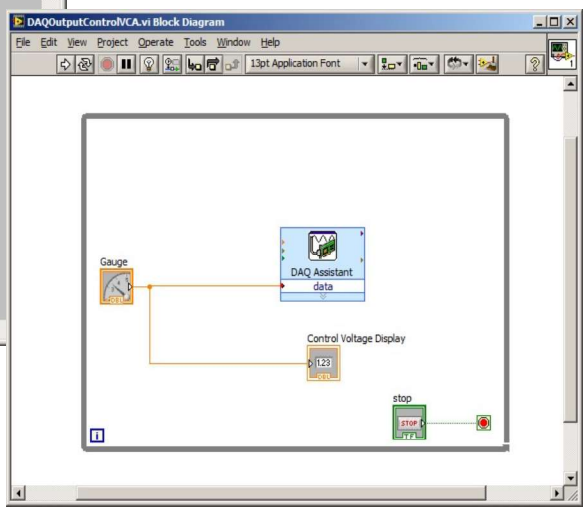
Prototyping Board
- Updated connections
- Detachable
- User-defined Banana Plugs, BNC, D-Sub connectors

Variable Power Supply
- 10 bit resolution
- 0 to +12V, 0 to -12V
- 500 mA current range

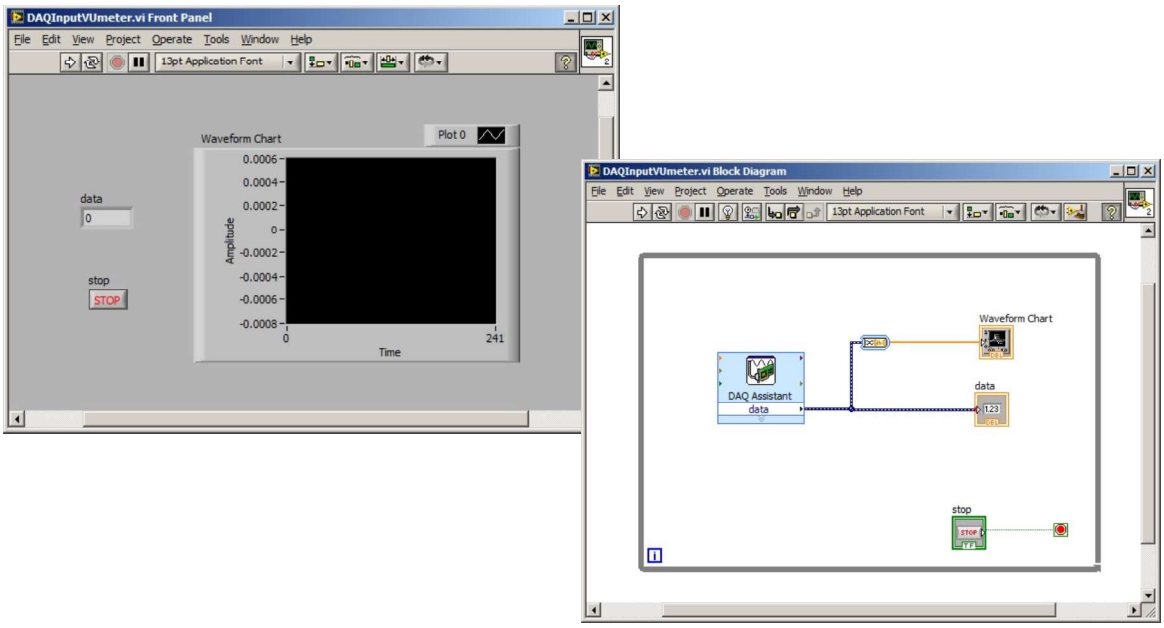
Week 5: DAQ Exercise:
DAQOutputControlVCA



Gauge for VCA: -1.3 – 3 V



Week 5: DAQ Exercise: DAQInputVUmeter



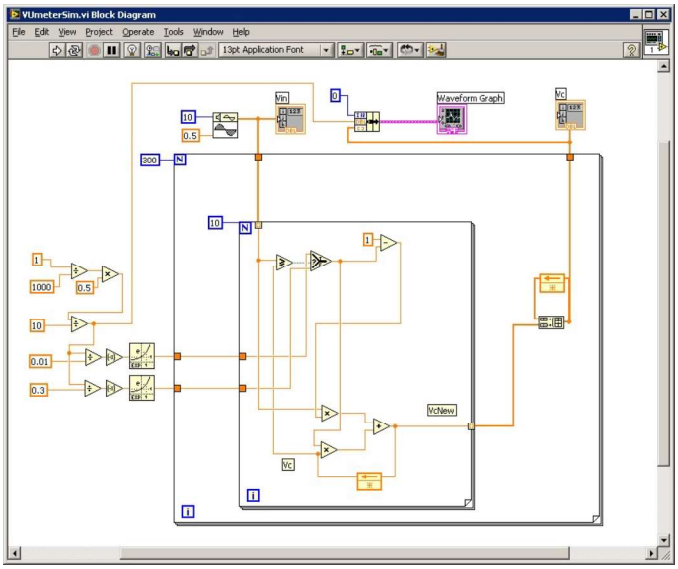
Week 6: LabVIEW/ELVIS Simulation

- To perform simulation of a volume unit (VU) meter using LabVIEW
- VU meter = envelope detector for audio signals
- The peak envelope detector (capacitor) output V_c for the rectified full-wave input waveform $|V_{in}|$ can be simulated using the simplified dual time constant model as (τ_1=0.01 s and τ_2=0.3 s)

$$V_c(t_{n+1}) = (1 - T_c)|V_{in}(t_n)| + T_c V_c(t_n)$$

$$T_c = \begin{cases} T_{c1} = e^{-\frac{\Delta t}{\tau_1}}, & \text{attack mode: } |V_{in}(t_n)| \geq V_c(t_n) \\ T_{c2} = e^{-\frac{\Delta t}{\tau_2}}, & \text{release mode: } |V_{in}(t_n)| < V_c(t_n) \end{cases}$$

Week 6: LabVIEW/ELVIS Simulation



VUmeterSim VUmeterModel

Week 6: About the Quiz

- Quiz assessment on LabVIEW programming
- Different MCQs for different students
- 25 minutes to complete 5 questions by using the computer in the lab

Week 7: VCA Breadboard

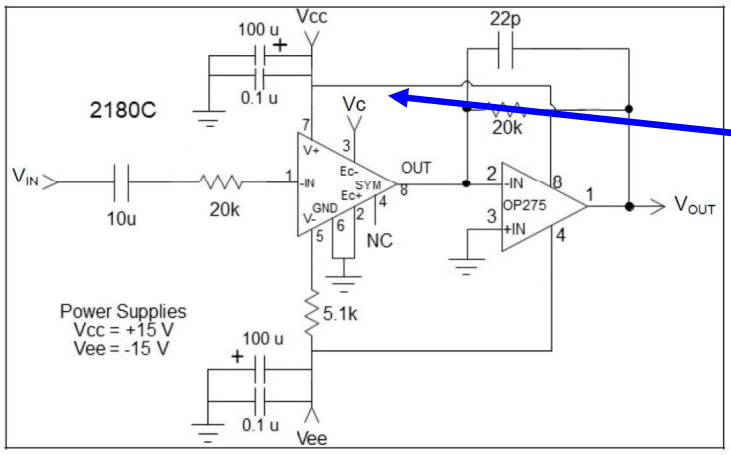


Figure 2: VCA Circuit Configuration and Gain Measurement Setup

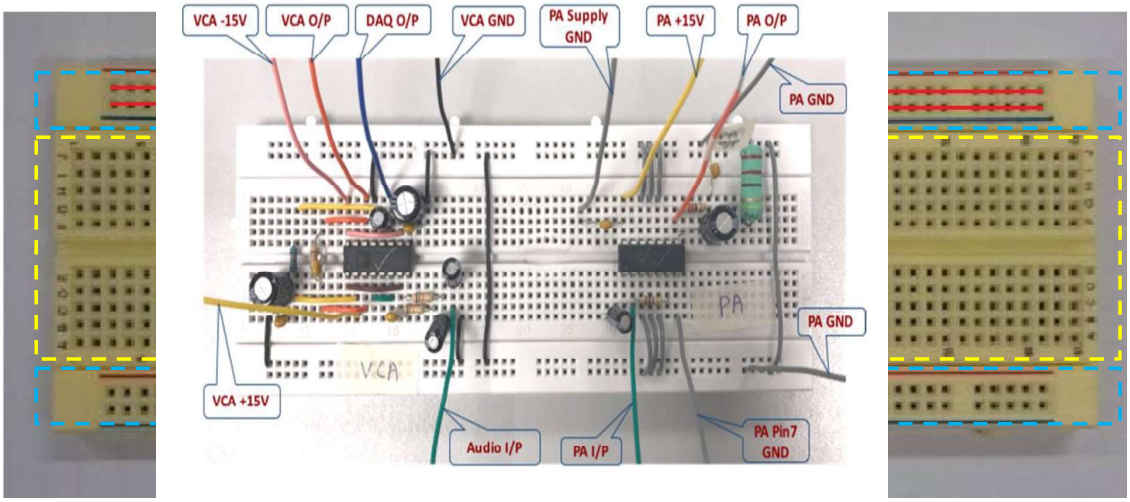
- Gain controlled by Vc (from DAQ O/P):

$$G = e^{-aV_C}$$

- Need dual supplies ±15V.

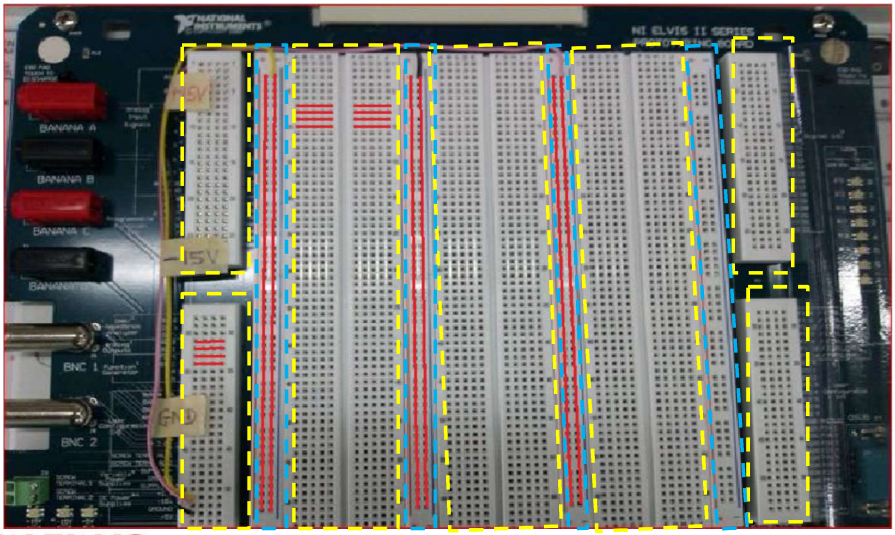
Breadboard

- Use for your circuits (to bring home)
- The connections of holes are illustrated by the red lines below

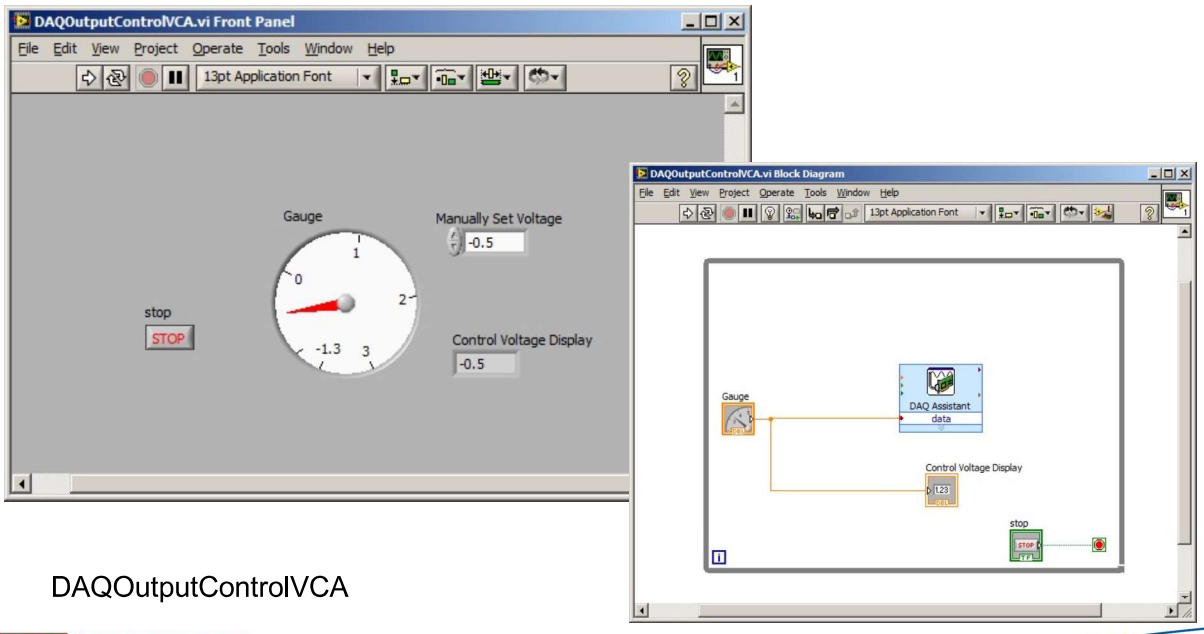


ELVIS Prototyping Board

- Use only for supplies, I/O and instrumentation, not your circuits
- The connections of holes are illustrated by the red lines below



Week 7: VCA DAQ Vc



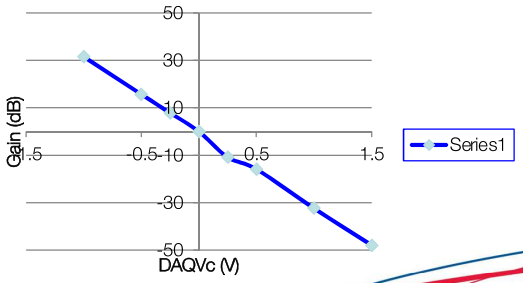
DAQOutputControlVCA

Week 7: VCA Gain Measurement

- Plot Gain (dB) versus V_C
- Deduce V_C sensitivity which is the inverse of the slope

Vin_pp (V) (Use matric no. U1120736A each digit from left to right)	DAQVc (V)
1.x = 1.1	1.50
1.x = 1.1	1.00
1.x = 1.2	0.50
1.x = 1.0	0.25
1.x = 1.7	0.00
0.1x = 0.13	−0.25
0.1x = 0.16	−0.50
0.1x = 0.11	−1.00

Vin_pp (V)	DAQVc (V)	Vout_pp (V)	Gain=Vout_pp/Vin_pp	Gain (dB)
1	1.5			
1	1			
1	0.5			
0.3	0.25			
0.3	0			
0.1	-0.25			
0.1	-0.5			
0.1	-1			

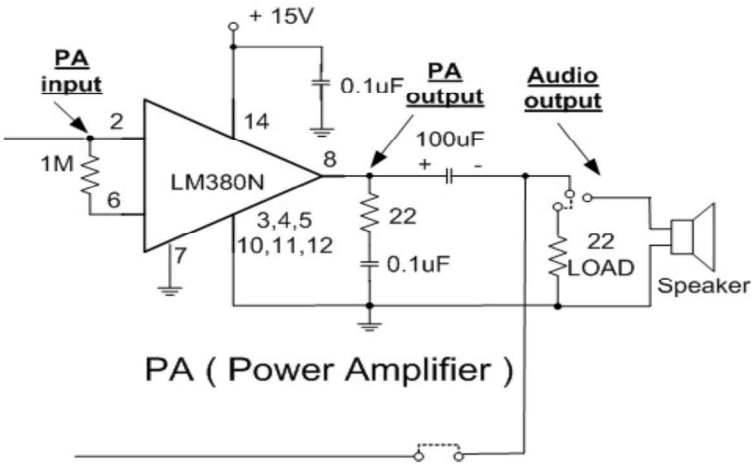


Week 7: Caution

- Connect up your circuit while ELVIS is OFF.
- Be extremely careful on wire connections, especially for biasing on ELVIS: +15V, −15V, ground, e.g. with only +15V and no/wrong −15V, the IC may get hot quickly.
- Be extremely careful on wire connections, especially for nearby pins.
- Check biasing first if circuit is not working.
- Use consistent wire color if available, e.g. black/blue/brown for ground, yellow/orange for +15V, pink/violet for −15V, red/green/grey/white for DAQ I/O etc.
- Check supply current flow if possible.

Week 8: PA Breadboard

- Provide the required power gain to drive speaker: ~34dB (50)
- Need single +15V, pay attention to groundings (7).



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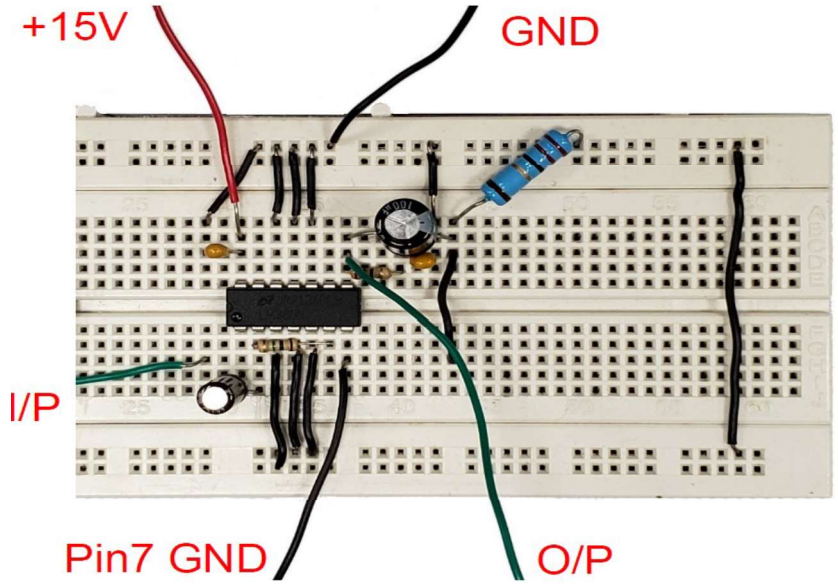
Read Datesheet LM380.pdf

Week 8: PA final Breadboard



Week 8: PA Freq Response Measurement

- Bode plot: gain and phase response vs freq

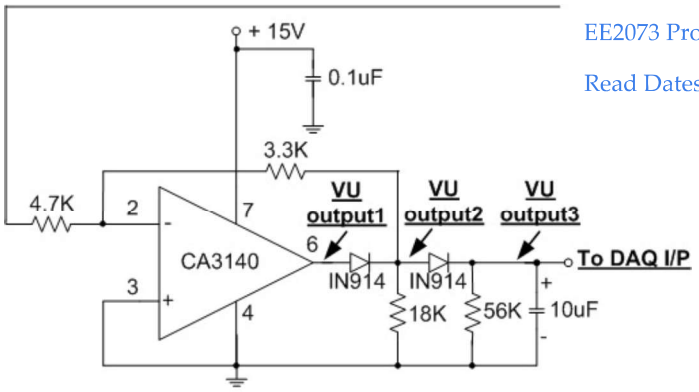
Peak Amplitude (Vp) (Use matric no. U1120736A each different non-zero digit)
0.02
0.0x = 0.01
~~0.0x = 0.02~~
0.0x = 0.07
0.0x = 0.03
0.0x = 0.06
0.1x = 0.11
0.1x = 0.12
0.1x = 0.17
0.1x = 0.13
0.1x = 0.16

Week 8: Caution

- Connect up your circuit while ELVIS is OFF.
- Be extremely careful on wire connections, especially for biasing on ELVIS: +15V, ground.
- Ground all the ground pins 3,4,5,10,11,12 to help dissipate heat.
- Separate the ground pin 7 from other grounds.
- Switch off ELVIS & PA as soon as measurements done.
- Check biasing first if circuit is not working.
- Use consistent wire color if available, e.g. black/blue/brown for ground, yellow/orange for +15V, pink/violet for −15V, red/green/grey/white for DAQ I/O etc.
- Check supply current flow if possible.

Week 9: VU Meter Breadboard+Soldering

- Based on rectifier concepts.
- Used for measurement of signal amplitude (envelope).
- Capture $VU_{output1}$, $VU_{output2}$ and $VU_{output3}$.



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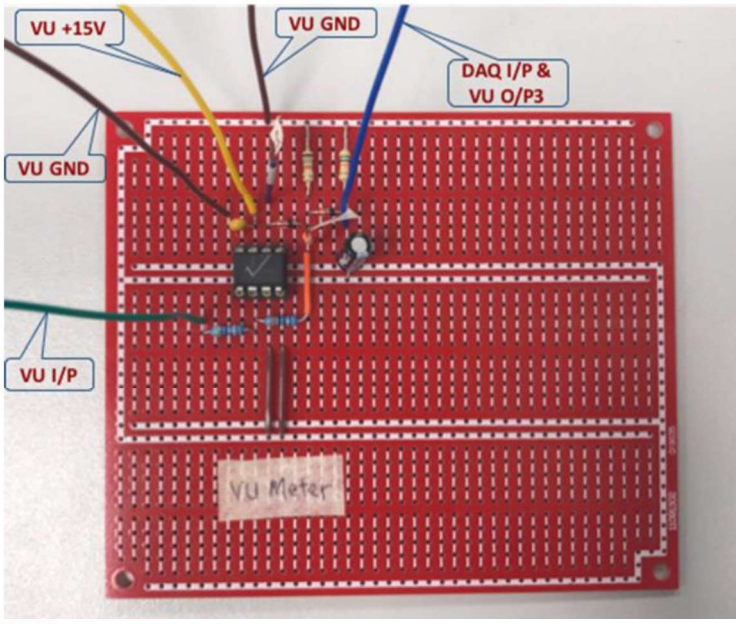
Read Datesheet CA3140.pdf

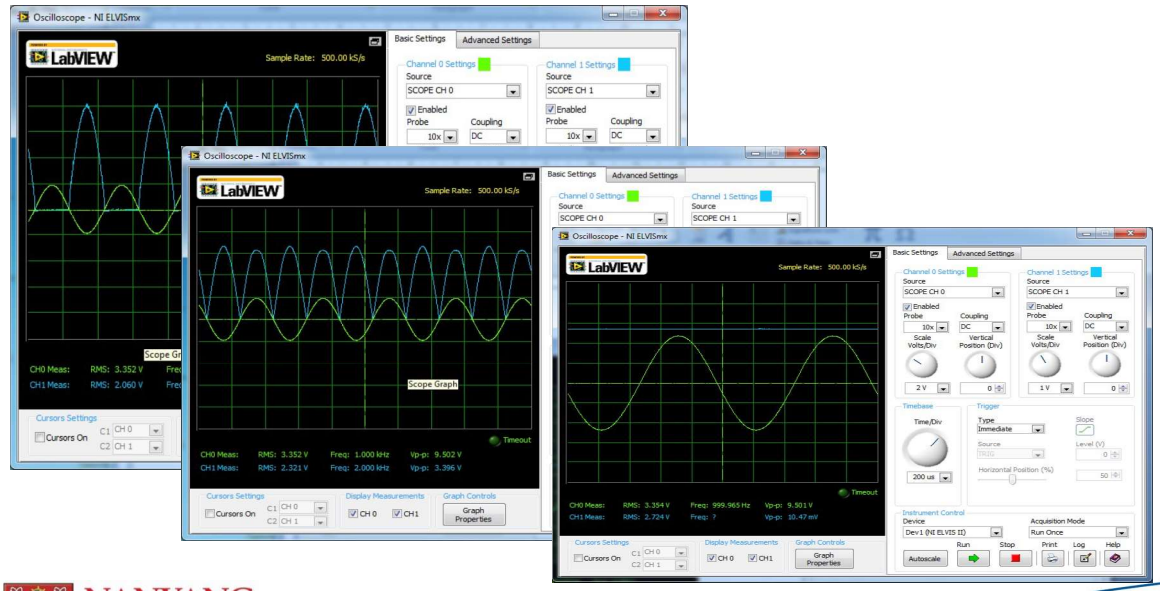
VU (Volume Unit) Meter

Week 9: Final circuit



Week 9: VU Meter Outputs

- Observing input and output waveforms.

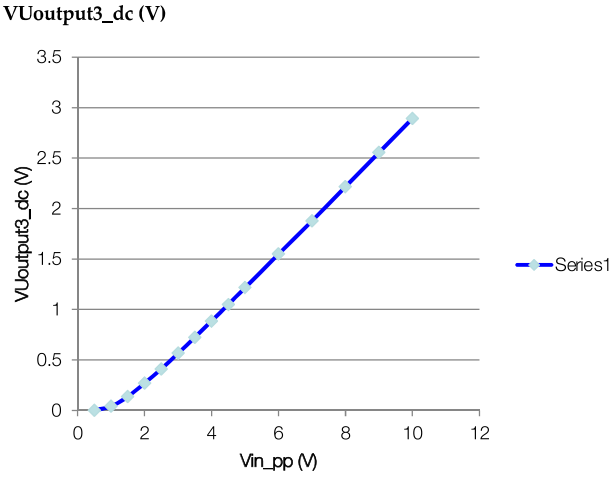


Week 9: VU Meter Response

- Plot Measured Gain versus VU_{input}
- Plot $VU_{output3}$ versus VU_{input}

VUinput Vin_pp (V) (Use matric no. U1120736A each digit from left to right)
5
9.x = 9.1
4.5x = 4.51
3.5x = 3.52
2.5x = 2.50
1.5x = 1.57
0.5x = 0.53
0.2x = 0.26

Vin_pp (V)
10
9
8
7
6
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5

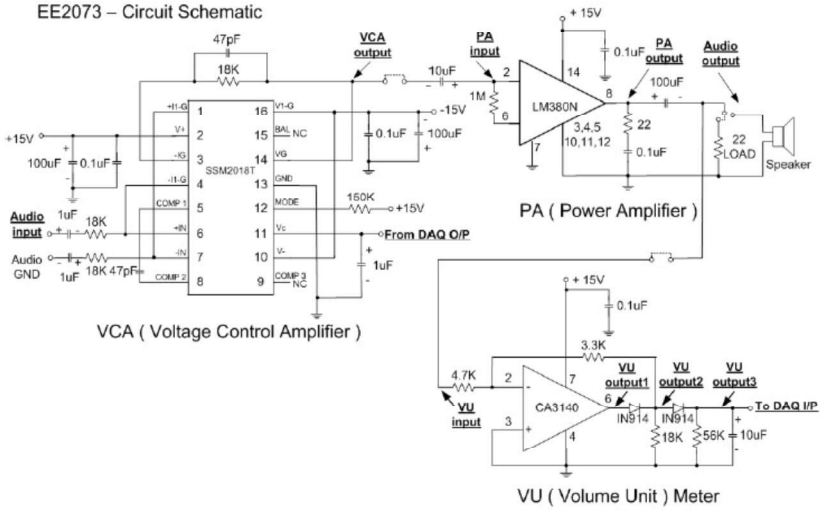


Week 9: Caution

- Connect up your circuit while ELVIS is off.
- Be extremely careful on wire connections, especially for biasing on ELVIS: +15V, ground.
- Check biasing first if circuit is not working.
- Use consistent wire color if available, e.g. black/blue/brown for ground, yellow/orange for +15V, pink/violet for −15V, red/green/grey/white for DAQ I/O etc.
- Check supply current flow if possible.

Week 10: Integration and Testing

- Testing gain controlled by Vc (from DAQ O/P)



Week 10: Integration and Testing

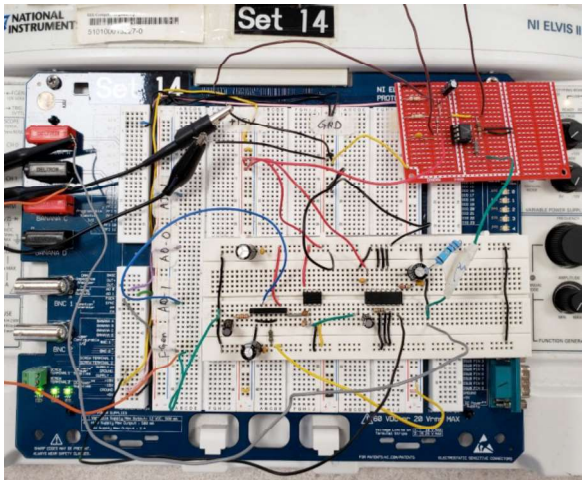
- Plot Gain (dB) versus V_C
- Change frequency and explain

Audio Input (V_{pp})	V_C (V)	Audio Output (V_{pp})	Gain (dB)
1.x	1.50		
1.x	1.00		
1.x	0.50		
1.x	0.25		
0.0x	0.00		
0.1x	−0.25		
0.1x	−0.50		
0.1x	−1.00		

Vin_pp (V) (Use matric no. U1120736A each digit from left to right)	DAQVc (V)
1.x = 1.1	1.50
1.x = 1.1	1.00
1.x = 1.2	0.50
1.x = 1.0	0.25
0.0x = 0.07	0.00
0.1x = 0.13	−0.25
0.1x = 0.16	−0.50
0.1x = 0.11	−1.00

Week 10: Final board

- To identify the location of any possible errors, you may need to test each individual sub-system as you did the testings in the previous weeks.



Week 11: Manual Volume Control

- VCA (Vc) = actuator
- VU meter (VUoutput3) = sensor
- No feedback path in the system = open-loop system

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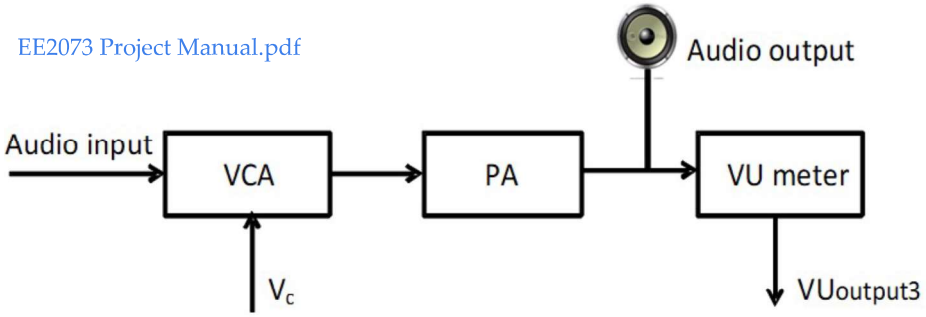
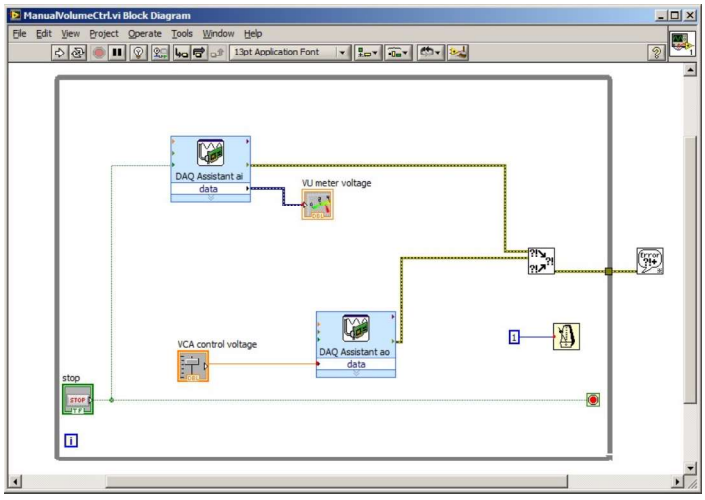


Block Diagram Representation of Open-Loop System

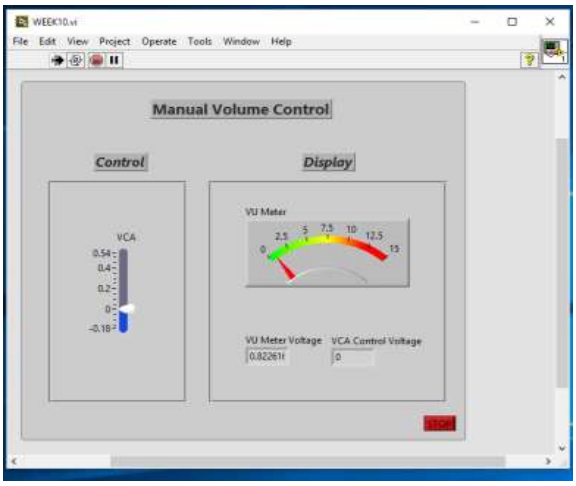
Week 11: Manual Volume Control

- Refer to DAQOutputControlVCA and DAQInputVUmeter



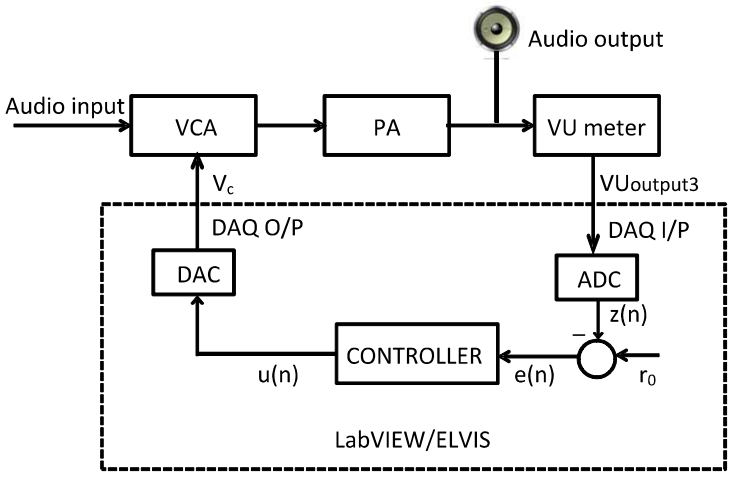
Week 11: Manual Volume Control

- Operator-assisted (manual) volume control system
- Adjust volume knob based on VU meter reading (loudness)



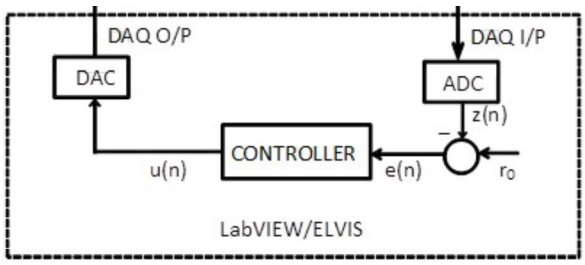
Week 12: Automatic Volume Control

- Feedback path thru' controller = closed-loop system



Block Diagram Representation of Closed-Loop System

Week 12: Automatic Volume Control



Step-Up-Down Controller:

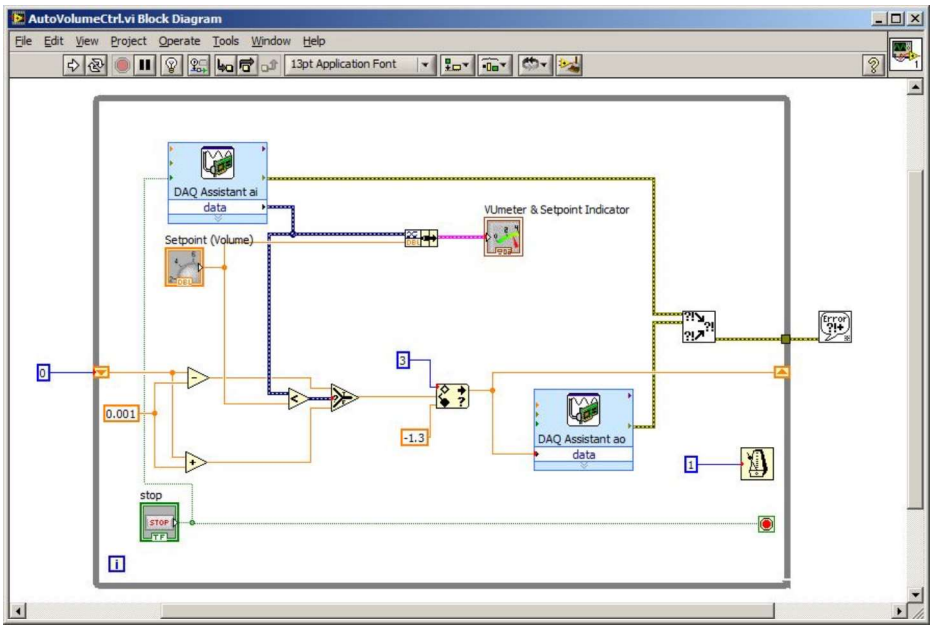
$$u(n) = \begin{cases} u(n-1) - \Delta, & e(n) > 0,\ z(n) < r_0 \\ u(n-1) + \Delta, & e(n) < 0,\ z(n) > r_0 \end{cases}$$

$$e(n) = r_0 - z(n)$$

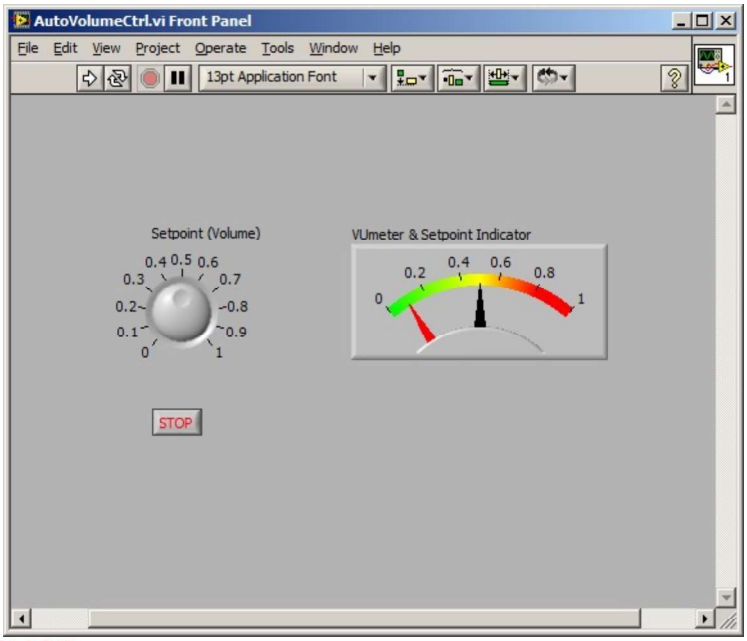
where

Δ is the controller parameter variable (step size),
u(n) is the actuator control voltage for VCA,
z(n) is the VU meter envelope detector output sensor value
r_0 is the set point value.

Week 12: Automatic Volume Control



Week 12: Automatic Volume Control



Project Report (Drafting)

- After Week 11, start drafting to submit individual project report.
- Extract from the weekly logbook: VCA, PA, VU meter, integrated system, manual and automatic volume control; schematics or snap photos of final circuits and instrument setups, screen/window capture of final waveforms and run-time outputs, main LabVIEW block diagrams and front panels, etc.

- See slides 7 and 8 for more information.

Report format

NANYANG TECHNOLOGICAL UNIVERSITY

EE2073 Report Template.docx

EE2073 Project Report

Automatic Volume Control for Audio Amplifier System

Student Name: Xxx Xxx Xxx
Matric No.: XXXXXXXXX
Project Group: XXX

School of Electrical and Electronic Engineering
Academic Year 20xx/xx
Semester 2

Week 13: Project Demo & Report

Formal report due on Monday Week 14 (18 Apr 2022) 5pm

Week 13: Demo

- The demo should be properly prepared.
- Explain your main achievements, comments on the quality of the work, or any problems, possible further improvements...
- Questions will be asked and both students should provide the answers.

Other References

- More LabVIEW/ELVIS/DAQ, download temp license:
  http://www.ni.com/
- Basic soldering:
  http://www.aaroncake.net/electronics/solder.htm
  http://www.youtube.com/watch?v=BLfXXRfRIzY
- EEE safety video:
  http://nocw10.eee.ntu.edu.sg/safety-videos/safety_video_undergraduate.wmv
- EEE courses:
  - EE2001 Circuit Analysis
  - EE2002 Analog Electronics
  - EE2010 Signals and Systems

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THE END