NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2017-2018

EE2002 - ANALOG ELECTRONICS

November / December 2017

Time Allowed: 21/2 hours

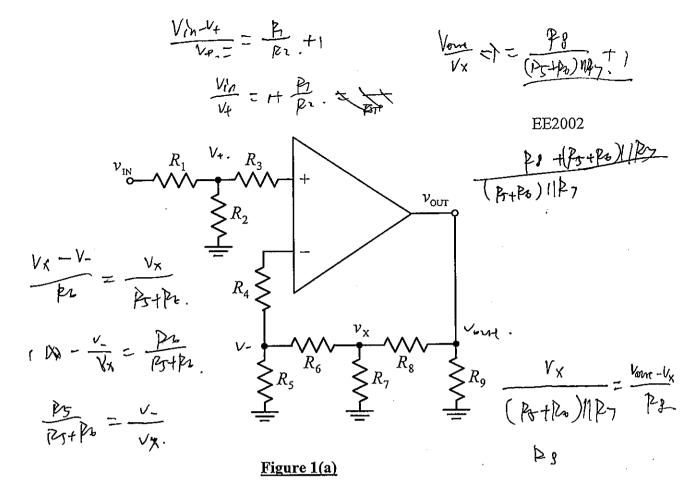
INSTRUCTIONS

- 1. This paper contains 5 questions and comprises 10 pages.
- 2. Answer ALL questions.
- 3. All questions carry equal marks.
- 4. This is a closed book examination.
- 5. Unless specifically stated, all symbols have their usual meanings.
- 6. A List of Formulae is provided in Appendix A on pages 8 to 10.
- 1. (a) For the ideal Op-Amp in negative feedback shown in Figure 1(a) on page 2, derive the expression for the closed-loop gain $A_{VCL} = (v_{OUT}/v_{IN})$.

Note: Parallel resistance of R_a and R_b can be written as R_a // R_b without expanding it.

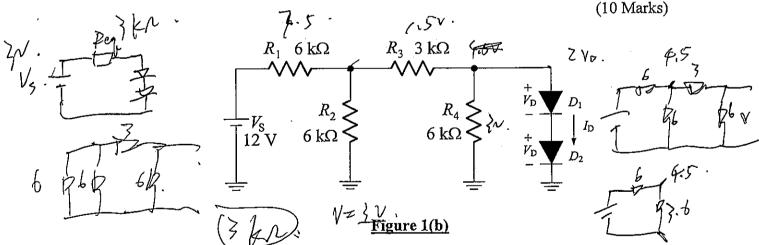
(10 Marks)

Note: Question No. 1 continues on page 2.



(b) In Figure 1(b), the empirical diode junction equation $V_D = nV_T \ln(I_D/I_S)$ for both diodes D_1 and D_2 where V_T is 26 mV, $I_S = 5 \times 10^{-15}$ A, n = 1 and $V_S = 12$ V. Find the quiescent point(s) or Q-point(s) (I_D, V_D) of the diodes D_1 and D_2 (in mA and V, respectively, up to 3 significant decimal places).

Hint: The diodes are identical.



2. For the MOSFET amplifier shown in Figure 2 on page 3, assume that $V_{DD} = 10 \text{ V}$, $V_{TN} = 1 \text{ V}$, $K_n = 2 \text{ mA/V}^2$, $r_o = \infty$, $R_S = 1 \text{ k}\Omega$, $R_{GI} = 6.5 \text{ M}\Omega$, $R_{G2} = 3.5 \text{ M}\Omega$, $R_D = 1 \text{ k}\Omega$, $R_M = 1 \text{ M}\Omega$, and $R_L = 5 \text{ M}\Omega$. Assume that the capacitors have infinite values.

Note: Question No. 2 continues on page 3. $\frac{1}{2} = \frac{4}{2} \left(\sqrt{G_5 - V_{TM}} \right)^2 \cdot P_b$.

(a) Determine the Q-point for the transistor.

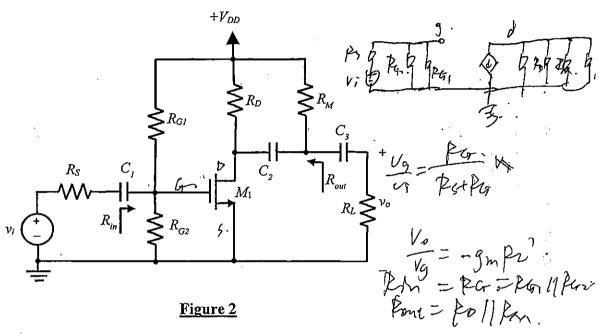
(5 Marks)

(b) Determine the voltage gain $A_{\nu} = \frac{v_0}{v_i}$, the input resistance R_{in} and the output resistance R_{out} of the amplifier.

(12 Marks)

(c) Determine the input small signal range for this amplifier.

(3 Marks)



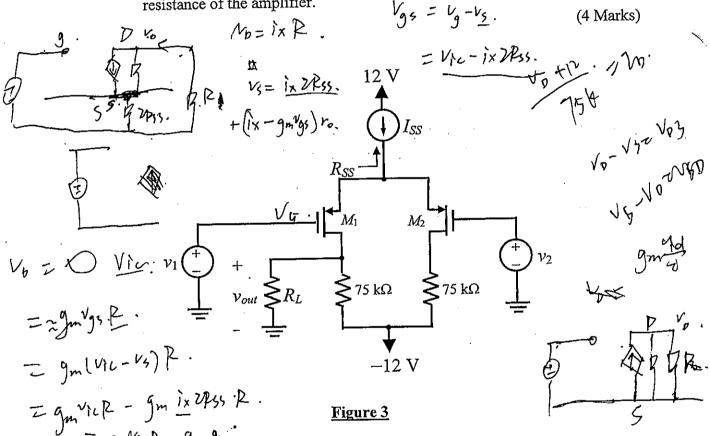
3. For the differential amplifier circuit shown in Figure 3 on page 4. The voltage sources, v_1 and v_2 , represent the ground referenced ac input signals such that the differential input signal $v_{id} = v_1 - v_2$ and the common-mode input signal $v_{ic} = \frac{v_1 + v_2}{2}$. The differential amplifier is biased by a constant current source with a DC current I_{SS} of 300 μ A and an ac resistance R_{SS} of 175 k Ω . The matched pMOS transistors, M_1 and M_2 , have $K_p = 250 \ \mu$ A/V², $V_{TP} = -1.5 \ V$ and $\lambda = 0.01 \ V^{-1}$. The output v_{out} is taken from the drain terminal of M_1 to drive the load resistance R_L .

Note: Question No. 3 continues on page 4.

$$\frac{Vp}{Vg} = \frac{-1dP}{Vg}$$
(a) If the DC voltages at the gates of M_1 and M_2 are both zero, determine the Q-point of the transistors. Verify that the pMOS transistors are operating in the saturation mode.

(6 Marks)

- For single-ended output and $R_L = \infty$, determine the differential-mode gain, common-mode gain and common-mode rejection ratio (CMRR) of the amplifier. (10 Marks)
 - (c) Determine the differential-mode input resistance and single-ended output resistance of the amplifier.



4. (a) Consider the current mirror circuit shown in Figure 4(a) on page 5. Assume all transistors are in saturation and ignore Early effect. It is given that $I_{REF} = 100 \, \mu\text{A}, \, V_{DD} = 10 \, \text{V}, \, K_n' = K_p' = K' = 10 \, \mu\text{A}/\text{V}^2, \, |V_{TP}| = |V_{TN}| = |V_T| = 0.6 \, \text{V}$ and (W/L) sizes of the transistors are written next to each of them in the figure. Also, the drain current equation for a MOSFET is given by:

$$I_D = \frac{K'}{2} \left(\frac{W}{L}\right) \left(|V_{GS}| - |V_T| \right)^2 \cdot \qquad \Longrightarrow \qquad \bigvee_{GS} = \left(V_T \right) + \left(\frac{2}{|L|W} \right) = 1$$

Note: Question No. 4 continues on page 5.

ANOOF AWORK

(i) Find the values of I_{out1} and I_{out2} .

(2 Marks)

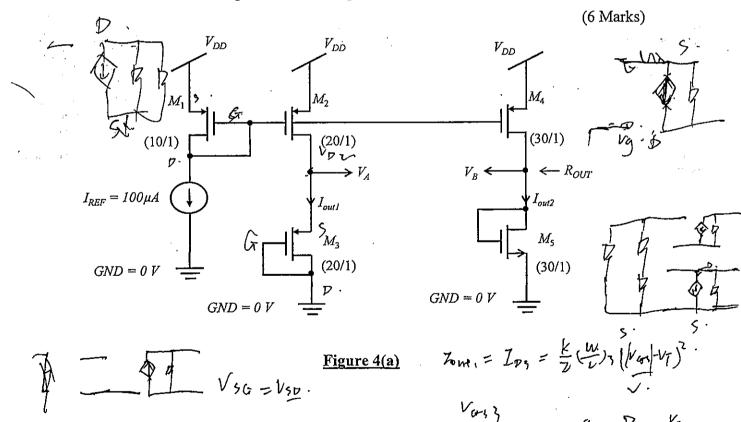
(ii) What are the values of V_A and V_B ? $\mathcal{V}^{\circ} \mid \psi$.

(5 Marks)

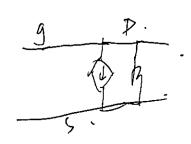
(b) For the same circuit in Figure 4(a), include Early effect now and do a small signal analysis to find an algebraic expression of the impedance R_{OUT} on the drain node of M_4 (with voltage V_B). Your answer should be in terms of g_m and r_o of the MOSFET. Indicate clearly the g_m and r_o of the i-th transistor as $g_{m,i}$ and $r_{o,i}$, respectively. For example, the g_m and r_o for transistor M_2 should be written as $g_{m,2}$ and $r_{o,2}$, respectively.

(7 Marks)

(c) Consider the circuit in Figure 4(b) on page 6. If $V_{BE} = 0.7 \text{ V}$, $V_A = 50 \text{ V}$, $\beta = 60$ and $A_{E2} = 5A_{EI}$ where A_E denotes emitter area, find the value of I_{out} in mA correct up to two decimal places.



Note: Question No. 4 continues on page 6.



1x= gm vgs.

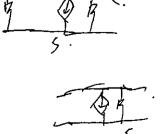
1x= gm vgs.

1x= gm vgs.

2 = gm vx.

3 = gm vx.

4 =



11

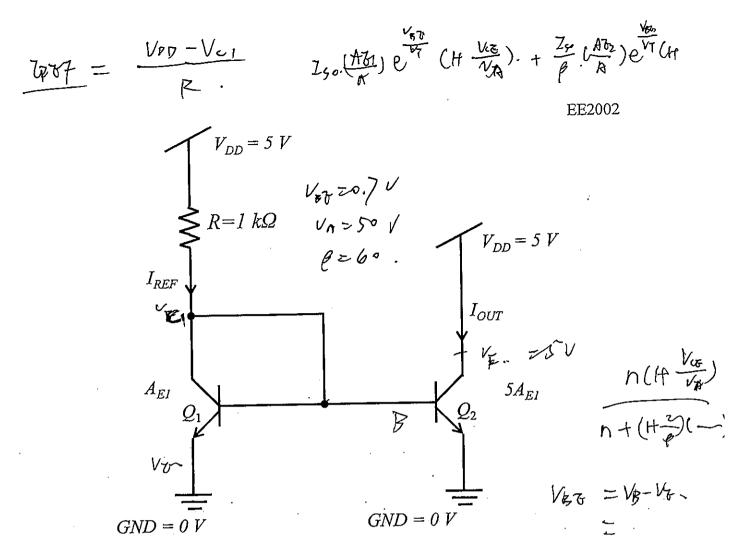


Figure 4(b)

- 5. (a) Consider the filter circuit shown in Figure 5(a) on page 7 and assume that the Operational Amplifier is ideal. Find an algebraic expression of the transfer function $H(s) = V_{out}/V_{in}$ of this circuit in terms of the resistors and capacitors R_1 , R_2 , R_3 , C_1 and C_2 . (6 Marks)
 - (b) How many poles and zeros are there in the transfer function H(s) in part (a)? What are their (values) in terms of the resistors and capacitors R_1 , R_2 , R_3 , C_1 and C_2 ?

 (6 Marks)
 - (c) If $R_1 = 100 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $R_3 = 1 \text{ k}\Omega$, $C_1 = 10 \text{ nF}$ and $C_2 = 1 \text{ nF}$, find the magnitudes of poles and zeros found in part (b) of this question.

(3 Marks)

Note: Question No. 5 continues on page 7.

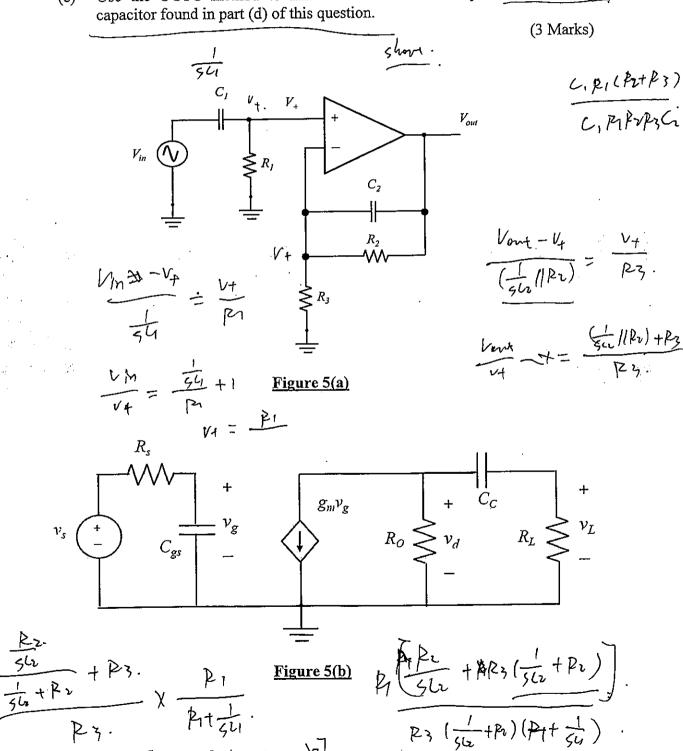
$$as[b+c(l+ds)].$$

$$s[Pi+Ps)(lPl+c|RlPs).$$

$$abs+abs(l+ds).$$

$$abs+acs+acds$$
EE2002

- For the circuit in Figure 5(b) with input at v_s and output at v_L , determine which (d) capacitor contributes to the upper or higher cut-off frequency and explain the SCIPIPIT SCIPIFIT S'CIPIPIPICE. reason for your choice. (Pr+P3) 54R1 + 52GP1 (2 Marks)
- Use the OCTC method to find the resistance seen by the contributing (e)



821 P1 (P2 + R3 (1+ R25C2)7)

P3 [1+5C2P2] (5 P14+ 36)

SCIPIEZ + SCIPIEZ + SECIEZENPOPS:

R3 (1/5/2+Pr) (P1+ 1/54

PIPT C1 + PIP3 (C++ SCILVP2).

P3 (+ SLYP2) (P1SC24 + C2)

P1PT + P1P3 (1+ SC2P2)

D2 1 1+ S/200 P2) (P1SC261+102)

Appendix A

List of Selected Formulae

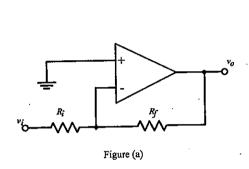
Op-Amps:

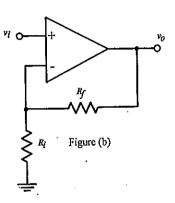
Closed-Loop Negative Feedback Inverting Gain, $A_{VCL} = \frac{v_o}{v_i} = -\frac{R_f}{R_i}$

Figure (a)

Closed-Loop Negative Feedback Non-Inverting Gain, $A_{VCL} = \frac{v_o}{v_I} = \left(1 + \frac{R_f}{R_i}\right)$ Figure 1.

Figure (b)





Op-Amp's Slew Rate,
$$SR \ge \left| \frac{dv_o}{dt} \right|_{max} = A_{VCL} \omega a_m = A_{VCL} a_m 2\pi f$$
,

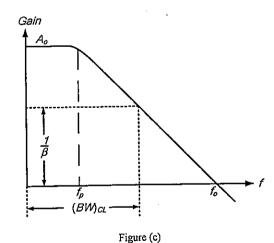
where
$$v_t = a_m \sin(\omega t)$$
, $v_o = A_{VCL} a_m \sin(\omega t)$ and $\left| \frac{dv_o}{dt} \right| = A_{VCL} \omega a_m \cos(\omega t)$

Op-Amp's frequency response:
$$A_{VOL}(jf) = \frac{A_o}{\left(1 + \frac{jf}{f_p}\right)}$$

Gain-Bandwidth Product: $A_o f_p = f_o = \frac{1}{\beta} (BW)_{CL}$

where
$$\frac{1}{\beta} = \frac{R_f + R_i}{R_i}$$

 $t_r = \frac{0.35}{(BW)_{CL}}$



Diodes:

$$\overline{v_D \approx nV_T \ln \left(\frac{i_D}{I_S}\right)} \text{ or } i_D \approx I_S e^{\left(\frac{v_D}{nV_T}\right)}$$

where
$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \dots$$

Diode conductance: $g_D = \frac{1}{r_D} = \frac{I_D}{nV_T}$

BJT in Forward Active Region:

Ignore early effect:
$$i_C = I_S \exp\left(\frac{|v_{BE}|}{V_T}\right)$$

With early effect:
$$i_C = I_S \exp\left(\frac{\left|v_{BE}\right|}{V_T}\right) \left(1 + \frac{\left|v_{CE}\right|}{V_A}\right)$$

Is: Saturation current,

 V_T : Thermal voltage, assume 25 mV at room temperature,

 V_A : Early voltage.

For npn transistor, $|v_{BE}| = v_{BE}$ and $|v_{CE}| = v_{CE}$;

For pnp transistor, $|v_{BE}| = v_{EB}$ and $|v_{CE}| = v_{EC}$.

Small-signal model parameters of BJT:

$$g_m = \frac{I_C}{V_T}$$
, $r_\pi = \frac{\beta}{g_m}$ and $r_o = \frac{V_A + |V_{CE}|}{I_C} \approx \frac{V_A}{I_C}$

where I_C : DC collector current at Q-point

VCE: DC collector-emitter voltage at Q-point

Criterion for small-signal operation of BJT: $|v_{be}| \le 0.2 \ V_r$

MOSFET in Saturation Region:

Criterion: $V_{DS} \ge V_{GS} - V_{TN}$ for NMOS;

 $|V_{DS}| \ge |V_{GS}| - |V_{TP}|$ for PMOS

VTN, VTP: Threshold voltage,

VDS: DC drain-source voltage,

V_{GS}: DC gate-source voltage.

 $i_D = \frac{K_n}{2} (v_{GS} - V_{TN})^2$ for NMOS, Ignore channel-length modulation effect:

 $i_D = \frac{K_p}{2} (|v_{GS}| - |V_{TP}|)^2$ for PMOS.

With channel-length modulation effect:

 $i_D = \frac{K_n}{2} (v_{GS} - V_{TN})^2 (1 + \lambda v_{DS})$ for NMOS,

$$i_D = \frac{K_p}{2} \left(\left| v_{GS} \right| - \left| V_{TP} \right| \right)^2 \left(1 + \lambda \left| v_{DS} \right| \right) \text{ for PMOS.}$$

where λ : channel length modulation parameter,

For NMOS
$$K_n = K'_n \left(\frac{W}{L}\right)$$
 and $K'_n = \mu_n C_{ox}$; For PMOS $K_p = K'_p \left(\frac{W}{L}\right)$ and $K'_p = \mu_p C_{ox}$.

MOSFET in Triode Region:

Criterion:

 $V_{DS} < V_{GS} - V_{TN}$ for NMOS; $|V_{DS}| < |V_{GS}| - |V_{TP}|$ for PMOS

Ignore channel-length modulation effect:

 $i_D = K_n \left(\nu_{GS} - V_{TN} - \frac{\nu_{DS}}{2} \right) \nu_{DS}$ for NMOS,

 $i_D = K_p \left(\left| \nu_{GS} \right| - \left| V_{TP} \right| - \frac{\left| \nu_{DS} \right|}{2} \right) \left| \nu_{DS} \right| \text{ for PMOS.}$

With channel-length modulation effect:

$$i_D = K_n \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \left(1 + \lambda v_{DS} \right) \text{ for NMOS,}$$

$$i_{D} = K_{p} \left(\left| \nu_{GS} \right| - \left| \mathcal{V}_{TP} \right| - \frac{\left| \nu_{DS} \right|}{2} \right) \left| \nu_{DS} \right| \left(1 + \lambda \left| \nu_{DS} \right| \right) \text{ for PMOS.}$$

Small-signal model parameters of MOSFET

For NMOS:
$$g_m = \sqrt{2K_n I_D (1 + \lambda V_{DS})} \approx \sqrt{2K_n I_D}$$
 and $r_o = \frac{\frac{1}{\lambda} + V_{DS}}{I_D} \approx \frac{1}{\lambda I_D}$

For PMOS:
$$g_m = \sqrt{2K_p I_D (1 + \lambda |V_{DS}|)} \approx \sqrt{2K_p I_D}$$
 and $r_o = \frac{\frac{1}{\lambda} + |V_{DS}|}{I_D} \approx \frac{1}{\lambda I_D}$

where I_D : DC drain current at Q-point

 V_{DS} : DC drain-source voltage at Q-point

Criterion for small-signal operation:

For NMOS:
$$\left|v_{gs}\right| \le 0.2 \left(V_{GS} - V_{TN}\right)$$

For NMOS:
$$\left|v_{gs}\right| \le 0.2 \left(\left|V_{GS}\right| - \left|V_{TP}\right|\right)$$

where VGS: DC gate-source voltage at Q-point.

Miller Effect

The equivalent shunt input capacitance: $C_X = C \times (1 + A_V)$

The equivalent shunt output capacitance: $C_r = C \times (1 + \frac{1}{A_r})$

where $-A_{\nu}$: the gain of the voltage amplifier

C: the original capacitance between the input and output terminals of the voltage amplifier

Frequency Response

By using OCTC and SCTC methods, the upper cut-off frequency is estimated by $\omega_{H_{-3dB}} \approx \frac{1}{\sum C_i R_i}$

and the lower cut-off frequency is estimated by $\omega_{L_{-3dB}} \approx \sum_{i} \frac{1}{C_{i}R_{i}}$

where C_i : the contributing capacitor for the cut-off frequency

R: the equivalent resistance seen by the capacitor C_i

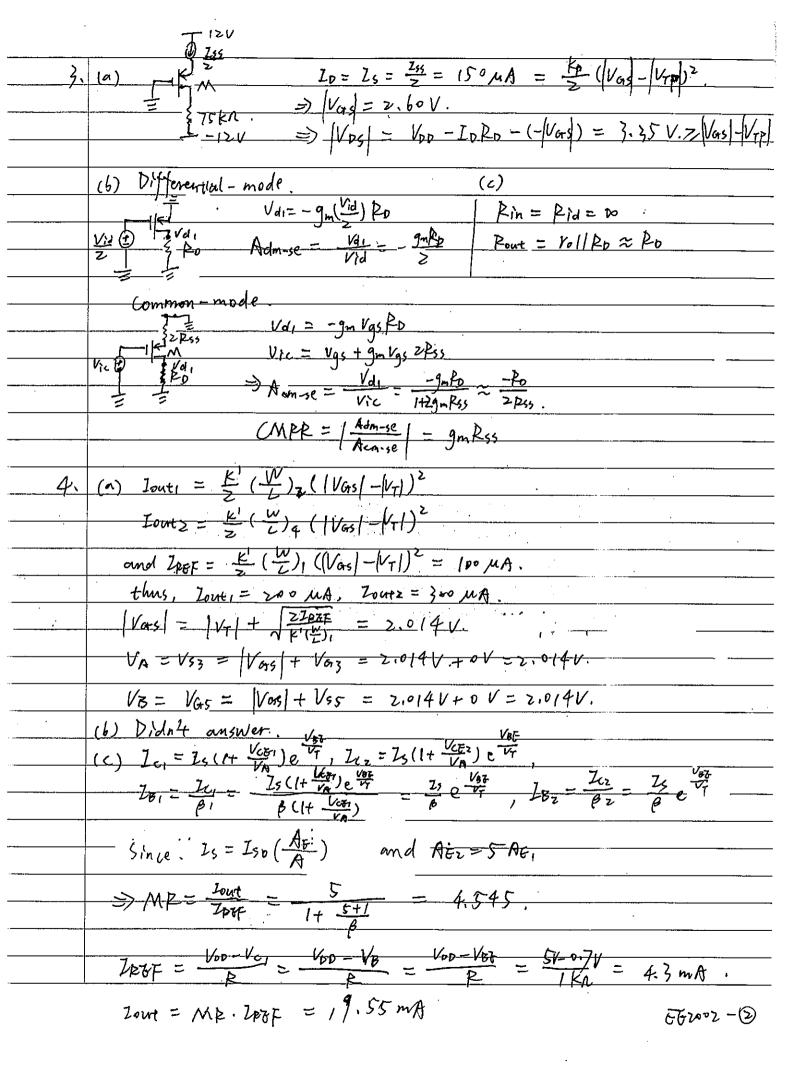
END OF PAPER

EErooz Nov/Dec, 17 $\frac{V_{1}(a) \quad V_{1} - V_{+}}{V_{+}} = \frac{P_{1}}{P_{2}}, \quad \frac{V_{x} - V_{-}}{P_{6}} = \frac{V_{x}}{P_{5} + P_{6}}, \quad \frac{V_{0} + V_{x}}{P_{8}} = \frac{V_{x}}{(P_{5} + P_{6})/(P_{7})}$ =) Vout = (P1+P2) Ps [P3+P6)1/P7]

| Vin = | R2 (P5+P6) [(P5+P6)1/P7] According to Thevenin Theorem.

Veg = Pr/(P3+P4) Vs. P4 = 3 V.

P1+P2/(P3+P4) Vs. P3+P4 = 3 V. () Peg = ((P, 1/P2)+ P3) 1/ Pa = 3 KA. Then, $L_0 = \frac{3V - 2V_D}{3KR}$ and $V_D = nV_T \ln(\frac{L_D}{L_S}) = 0.026 \ln \frac{L_D}{15 \times 650}$ Vo=0.7 V > 20=57.9 mA > Vo=0.6}2V > 20=57.9 mA $\Rightarrow V_0 = 0.634 V \Rightarrow I_0 = 57.7 \text{ mA} \Rightarrow V_0 = 0.634 V \Rightarrow I_0 = 57.7 \text{ mA}.$ $\downarrow V_{PD}$ $\downarrow V_{PD}$ Forz PG, Vgmvgs Fro JPD JPM JRL $\frac{Vo}{Vq} = \frac{Vd}{Vq} = \frac{-gmV_{45}Rc^2}{Vqs} = -gmRc^2, \quad Avt = \frac{Vo}{Vg} \frac{Vq}{Vi} = -gmRc^2, \quad Rar$ Rin = Pa=Pa,1/Paz, Pout = Pol/Pm llro & Pol/Pm (c) |Vin | < 0,2 (Vas - VTN) (14 gm Ps,) (Pint. Ps)



<u> </u>	(a) Vin-V+ V+ Vout-V+ V+
	$\frac{1}{\sqrt{1-\frac{1}{2}}} = \frac{1}{R_1}, \frac{1}{\sqrt{1-\frac{1}{2}}} = \frac{1}{R_2}$
	5C1 5C2 F3
	- V+ 5C1P1 Vout Pz+P3(1+3(2Pz)
	$=) \frac{V_{+}}{V_{in}} = \frac{sC_{i}R_{i}}{l+sC_{i}R_{i}} \frac{V_{out}}{l} \frac{R_{2}+R_{3}(l+sC_{2}R_{2})}{V_{1}}$
	=) H(5) = V+ Vout 5(1P1 P2+P3(1+5(2P2)) =) H(5) = V+ Vout 5(1P1 P3(1+5(2P2))
	_ SCIRI (RETPZ + SCZRZPZ)
	P3 (1+59P1)(1+5C2P2)
	5
0	$\frac{C_1P_1(P_2+P_3)}{P_3} = \frac{S(1+\frac{F_2+P_3}{C_2+C_2})}{(1+\frac{S}{C_2})(1+\frac{S}{C_2})}$
	$\frac{2}{2} \frac{1}{1/4} \frac{1}{1$
	cb) zeros, 0, - Pz++3 CzRzf3
	CrR2F3
•	poles:
	poles: - 1 Crer.
	(d) Short (gs, Vg = 0. =) reduce voltage goin. =) Cgs contributor. Short (cc, VL = Vd, increases. =) increase voltage gain =) (cc helper.
	Short Cc, V1 = Vd, increases. => increase voltage gain => Cc helper.
27	J. J
	(e) P = P
	,
PARTY	·
No. 6 dates as about the control of	
,	
V	

F62002-3