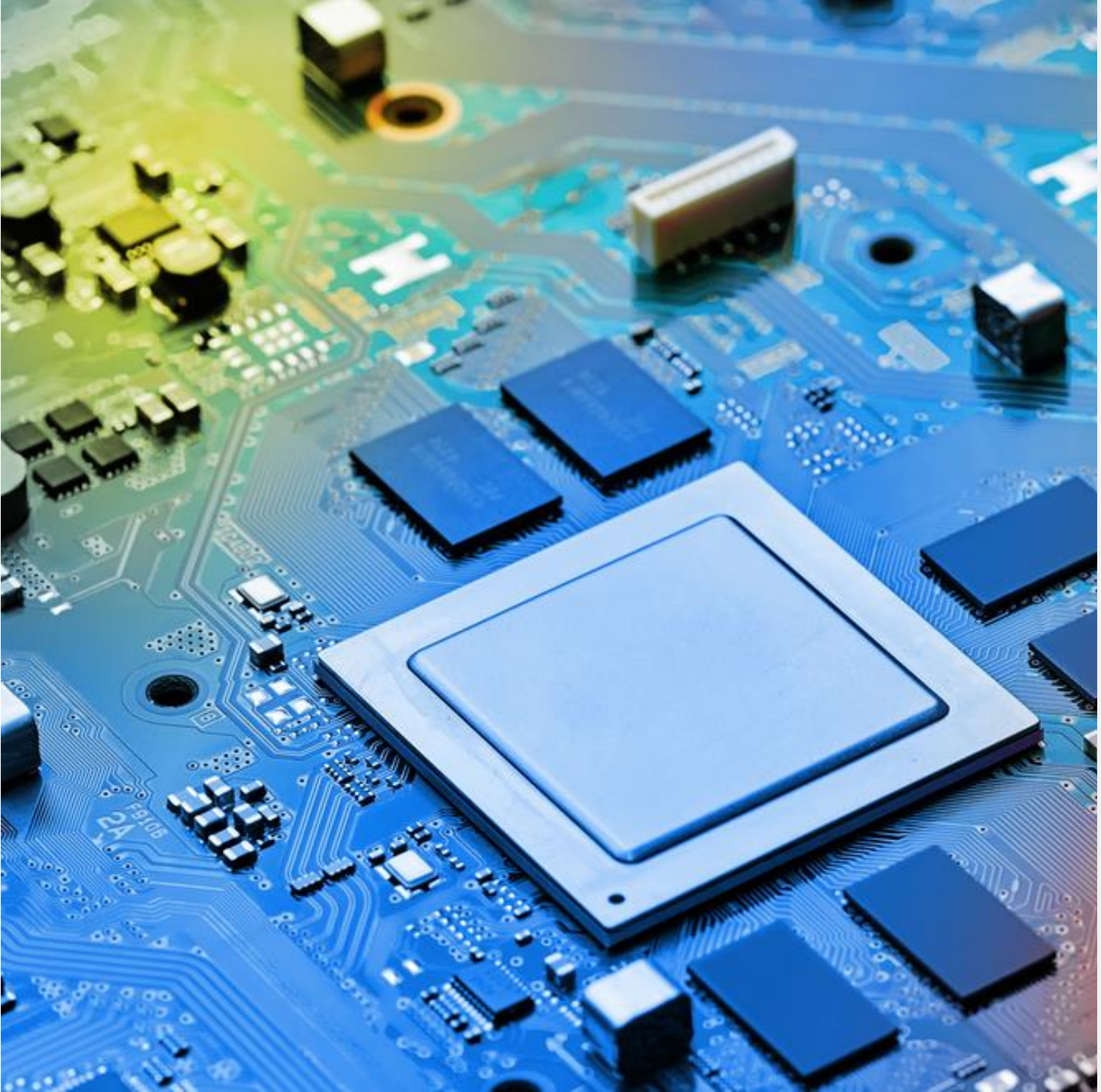


NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE

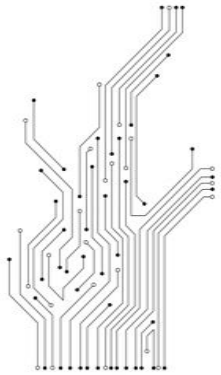
EE3019 – Integrated Electronics

Latches and Flip Flops

Learning Objectives

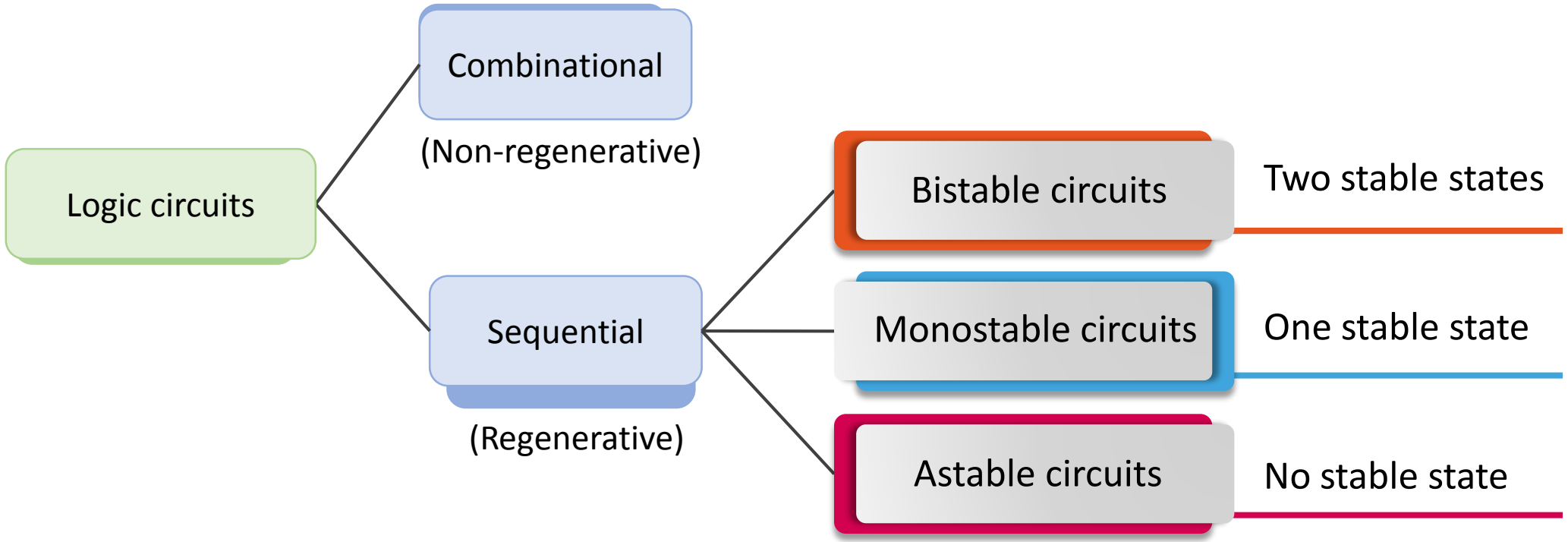
By the end of this lesson, you should be able to:

- Explain latches and flip-flops.
- Discuss Set Reset latch (SR) – circuit and parasitic.
- Explain clocked JK latch.



Latches and Flip-Flops

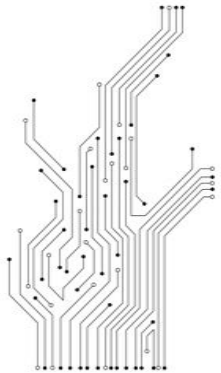
There are three critical components in sequential circuits:



Latches and Flip-Flops

There are three critical components in sequential circuits:

- Bistable circuits
- Monostable circuits
- Astable circuits



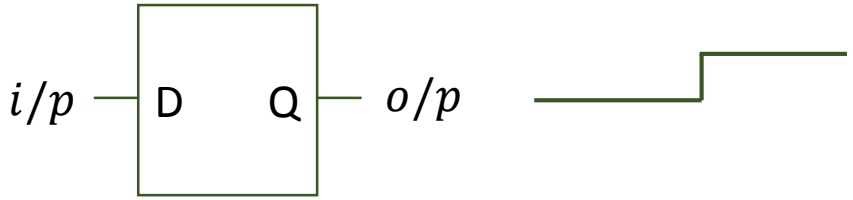
Latches and Flip-Flops

There are three critical components in sequential circuits:

- **Bistable circuits**
- Monostable circuits
- Astable circuits

They have two stable states or operation modes, each of which can be obtained under certain current input and previous output conditions.

Flip flop



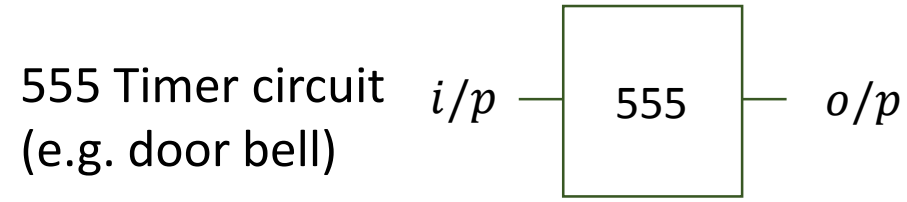
Latches and Flip-Flops

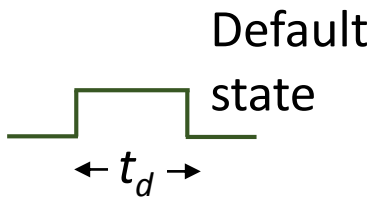
There are three critical components in sequential circuits:

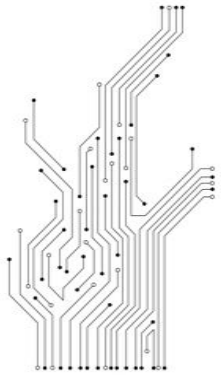
- Bistable circuits
- Monostable circuits
- Astable circuits

They only have one stable operating point (state). The output eventually returns to the single stable state after a certain time duration.

555 Timer circuit (e.g. door bell)







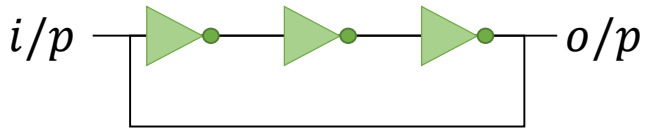
Latches and Flip-Flops

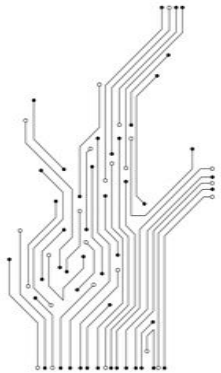
There are three critical components in sequential circuits:

- Bistable circuits
- Monostable circuits
- Astable circuits

The is no stable operating point (state) which the circuit can preserve for a certain time period.

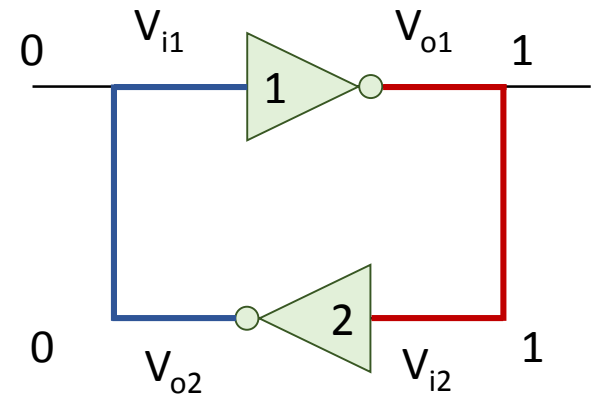
Ring oscillator

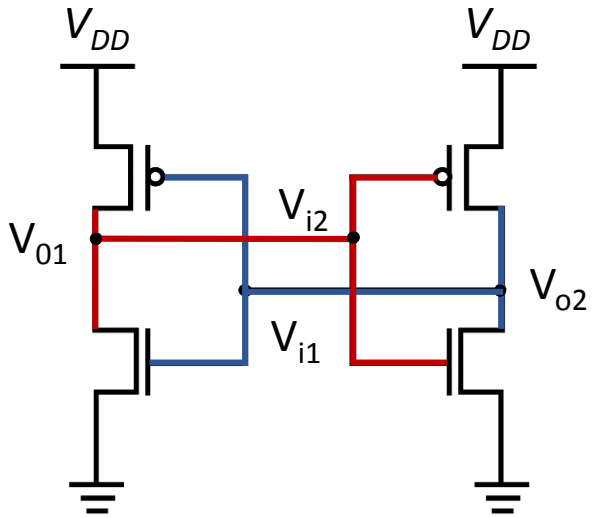




Behaviour of Bistable Elements – Cross-coupled Inverters

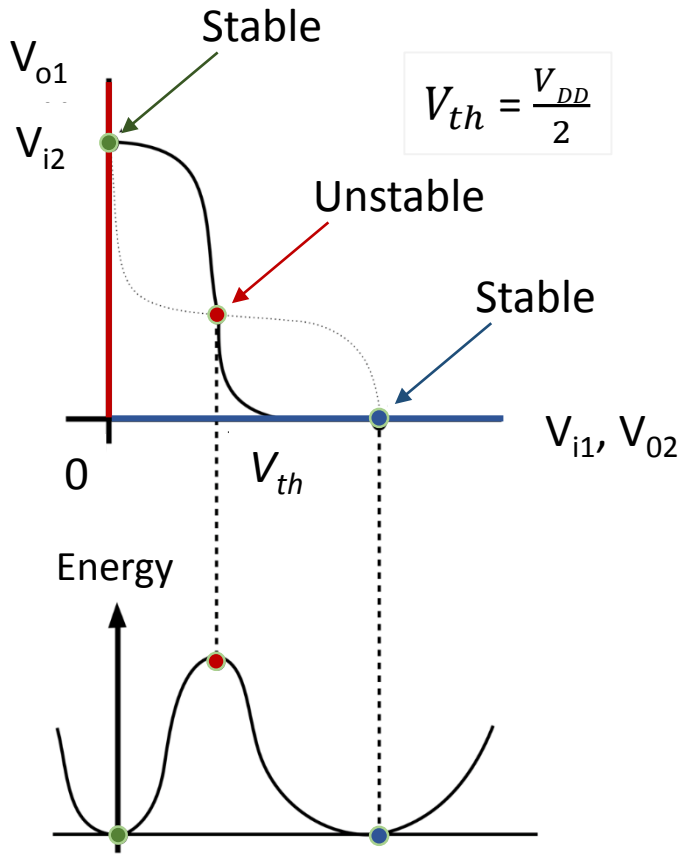
a Gate-level schematic

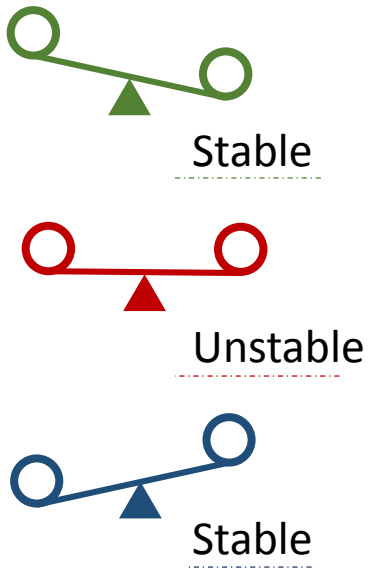




b Transistor-level schematic

c Intersecting voltage transfer curves of the two inverters

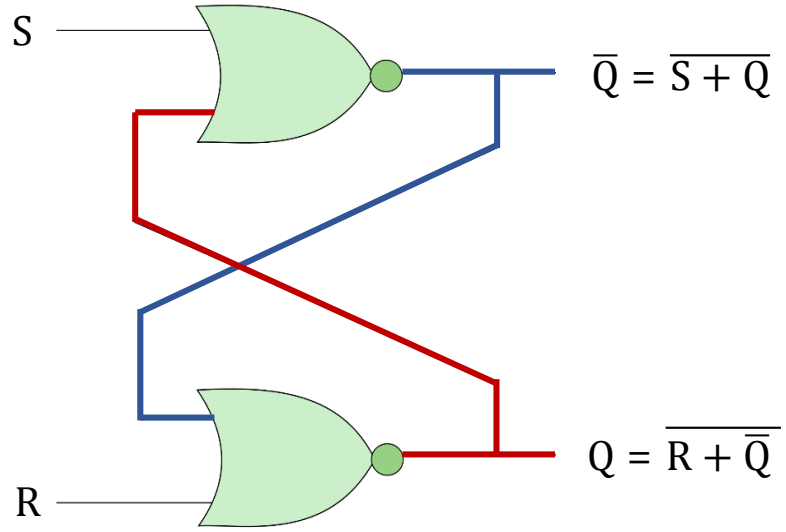


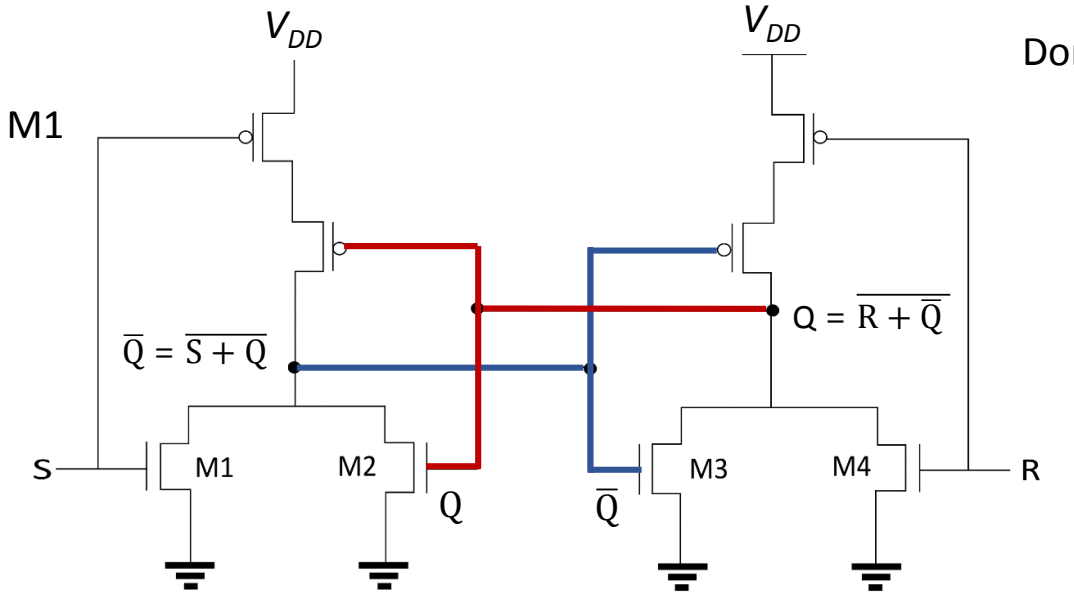


d Qualitative view of the potential energy levels corresponding to the three operating points

CMOS SR Latch Based on NOR Gates

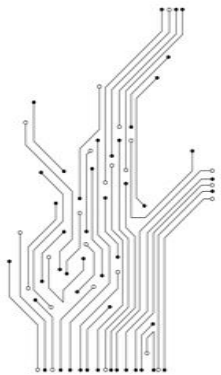
SR: Set - Reset





Dominant i/p is '1'

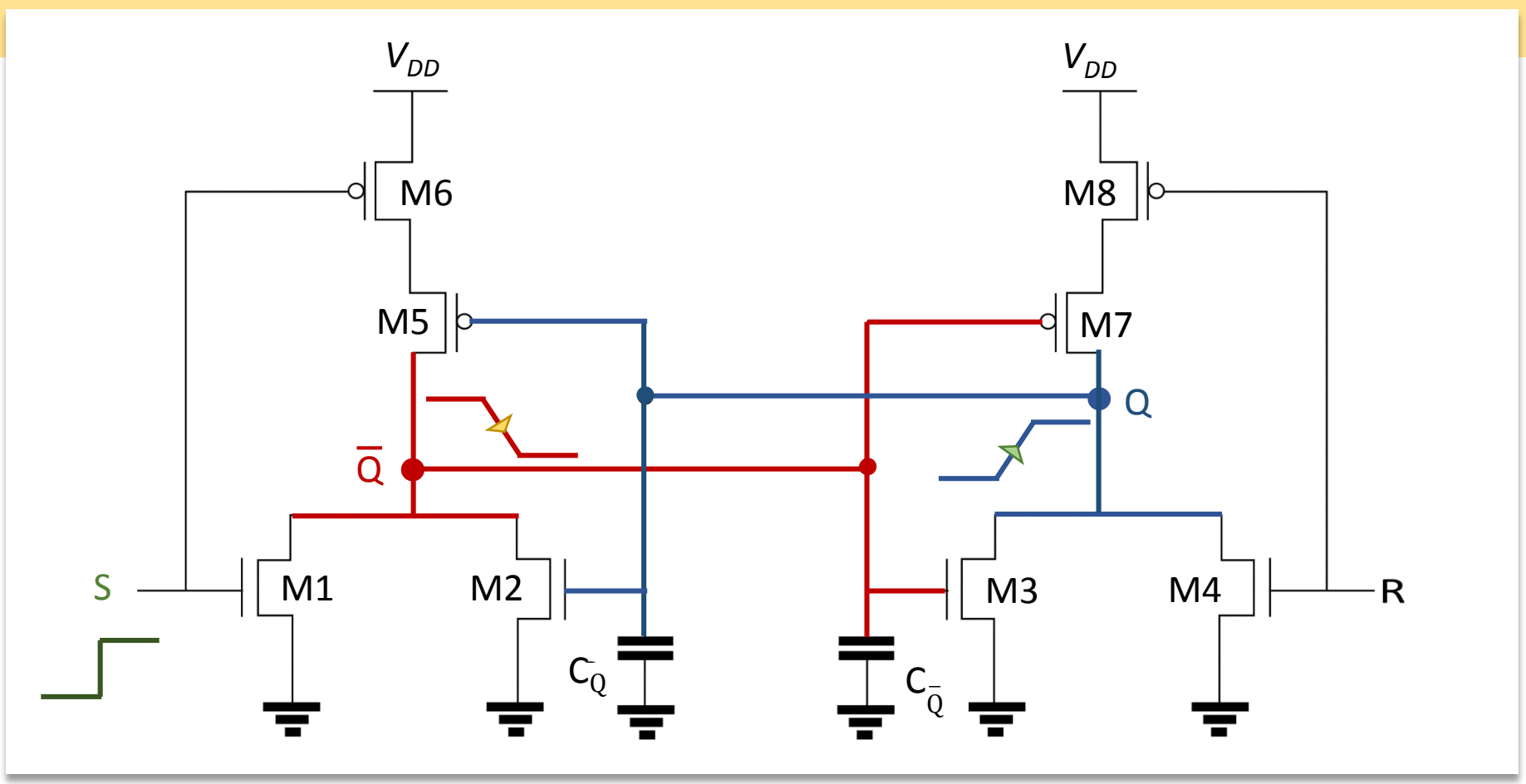
NOR		
0	0	1
0	1	0
1	0	0
1	1	0



Dominant i/p is '1'

SR Flip-flop			
Inputs		Next state (Q_{n+1})	Action
S	R		
0	0	Q_n	Hold
0	1	0	Reset
1	0	1	Set
1	1	?	Not allowed

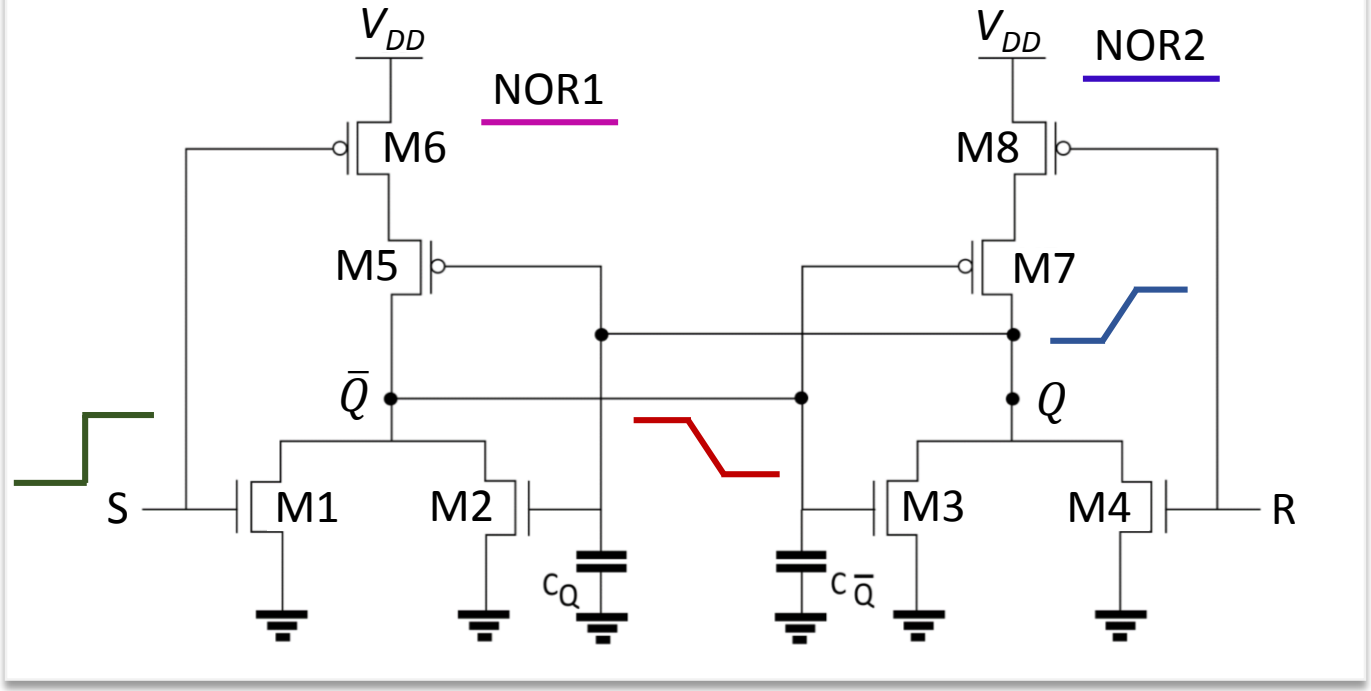
SR Latch - Parasitic Capacitance



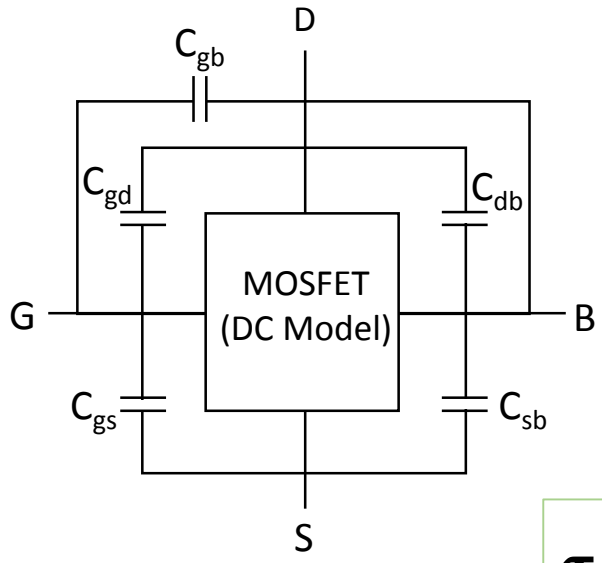
CMOS SR Latch with lumped load capacitance at both output nodes.

SR Latch - Parasitic Capacitance (Contd.)

Assume RESET ➔ SET



$$\tau_{riseQ(Latch)} = \tau_{fall\ \bar{Q}(NOR1)} + \tau_{riseQ\ (NOR2)}$$



$$\tau = \frac{C\Delta V}{i}$$

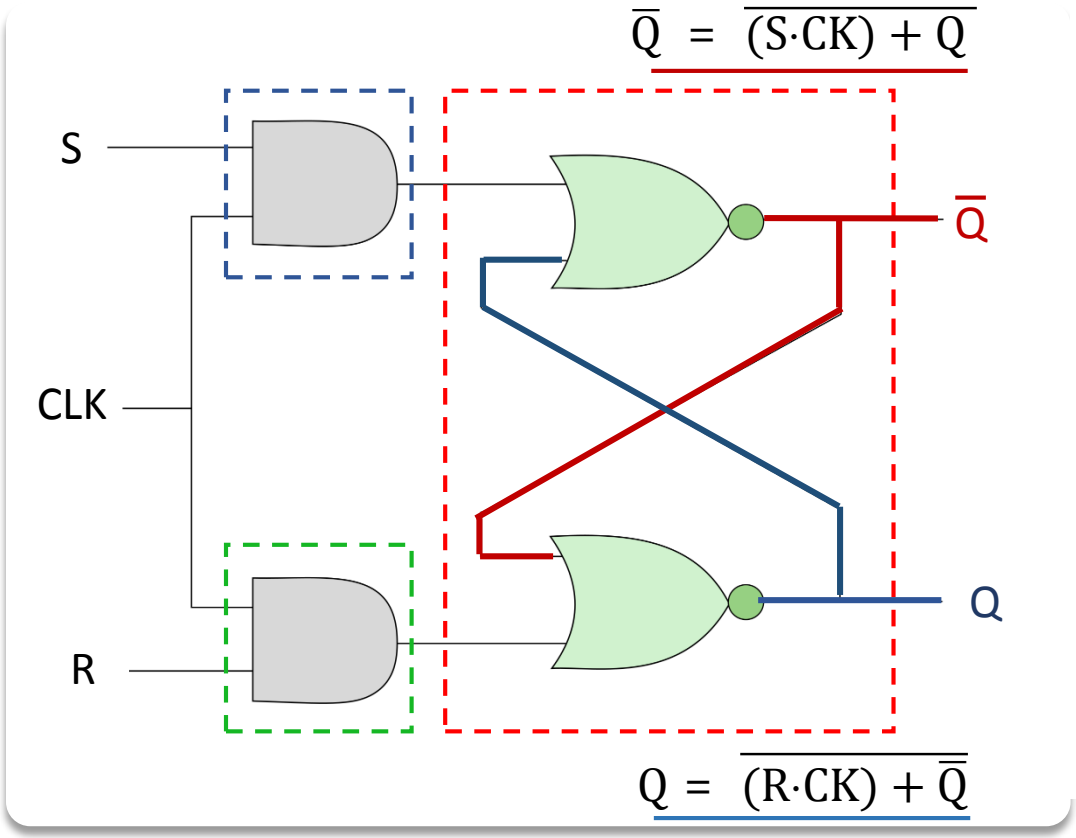
Total parasitic capacitance at $\bar{Q}$ and Q:

$$C_{\bar{Q}} = C_{gb3} + C_{gb7} + C_{db1} + C_{db2} + C_{db5} + C_{sb5} + C_{db6}$$

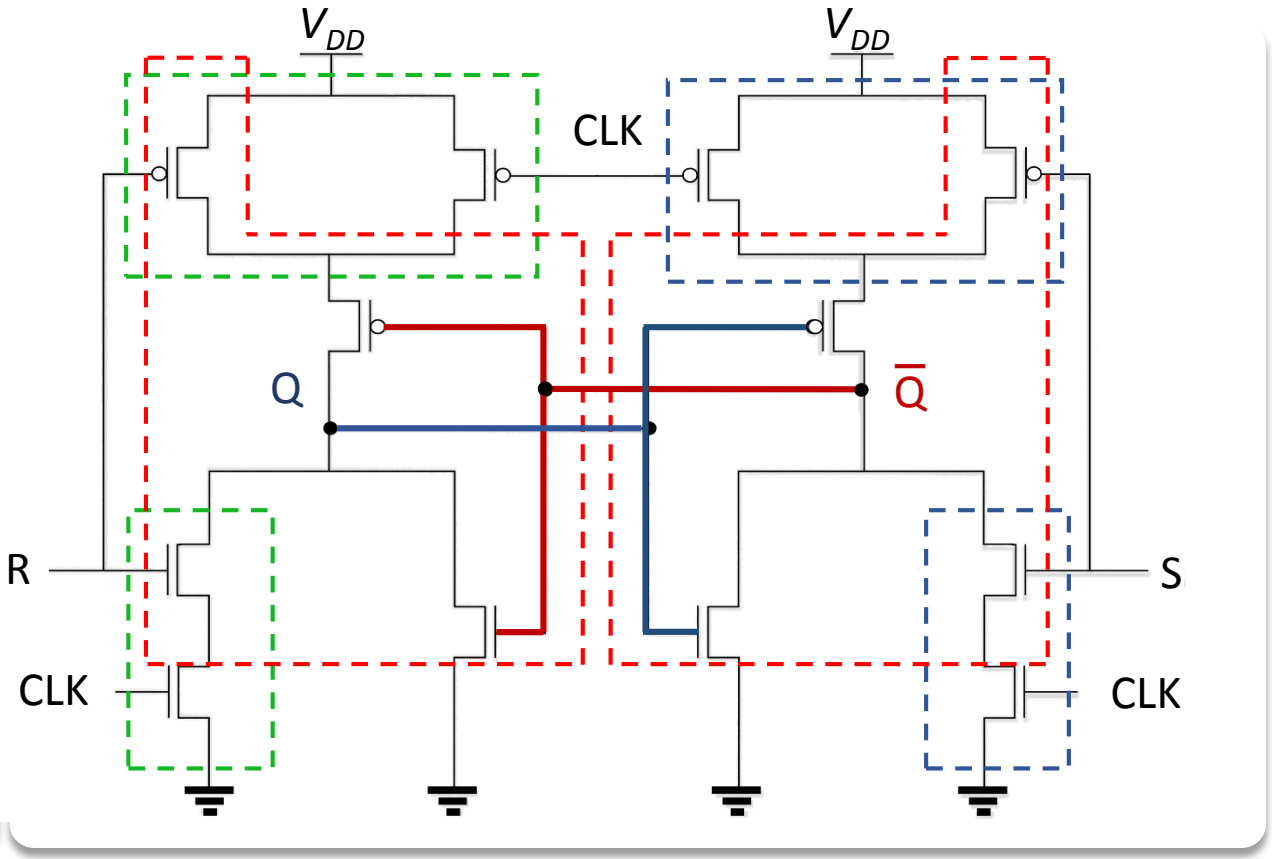
$$C_{Q} = C_{gb2} + C_{gb5} + C_{db3} + C_{db4} + C_{db7} + C_{sb7} + C_{db8}$$

Clocked SR Latch based on NOR Gates

CLK: Enable signal

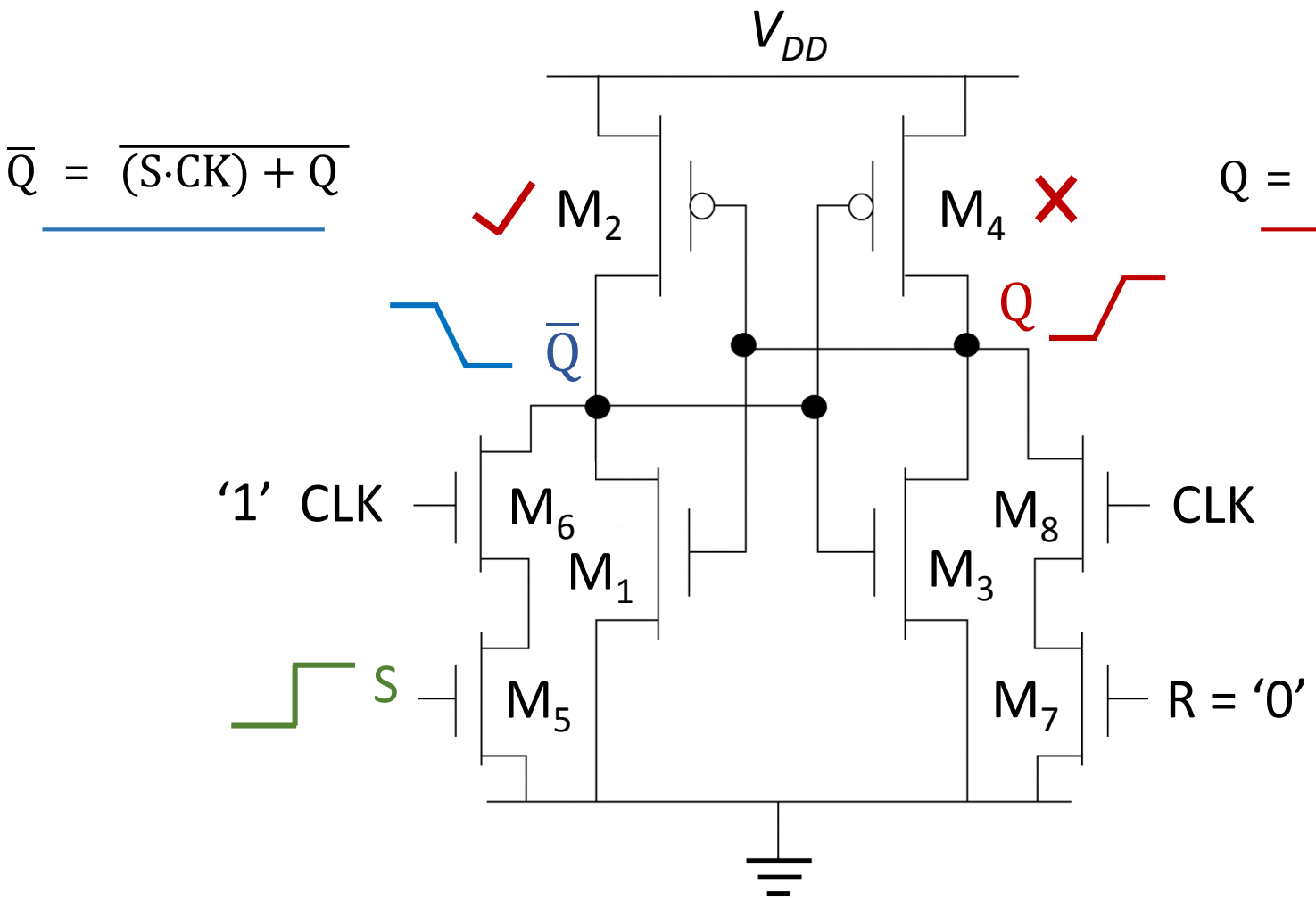


(a) Gate-level schematic

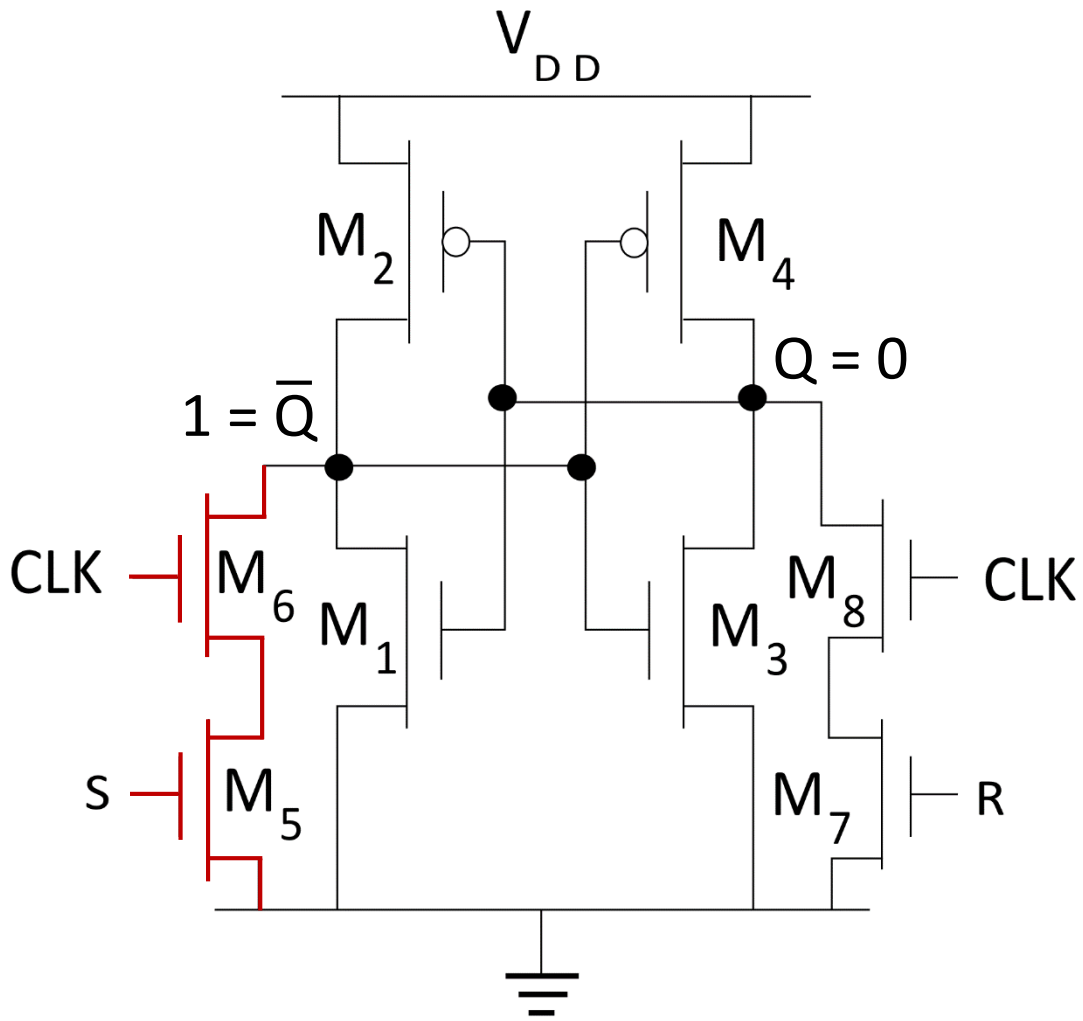


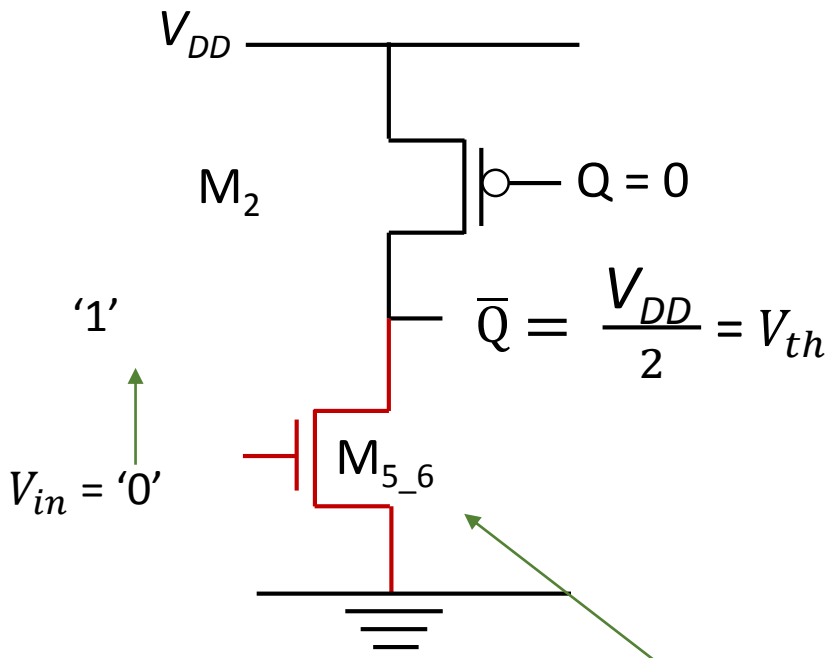
(b) Transistor-level schematic

8 - Transistor Clocked SR Latch



6 - Transistor Clocked SR Latch





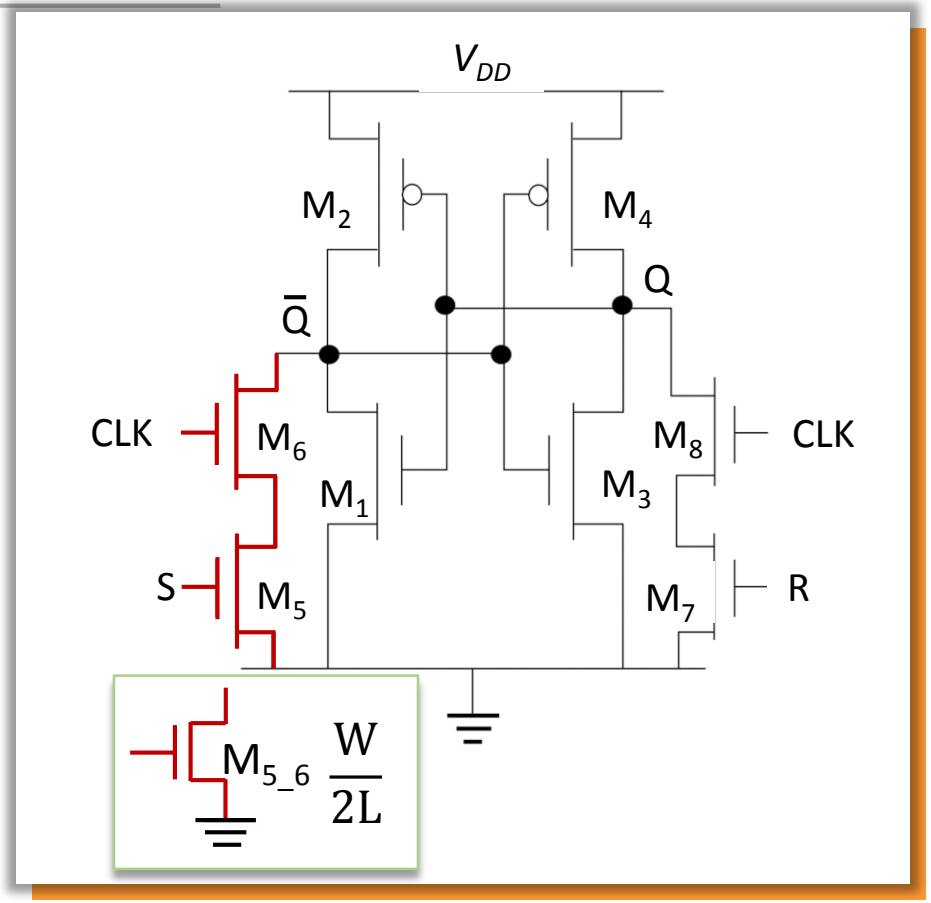
$$\left(\frac{W}{L}\right)_{M5\_6} = \frac{1}{2}\left(\frac{W}{L}\right)_5 = \frac{1}{2}\left(\frac{W}{L}\right)_6$$

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6$$

Transistor Sizing the SR Flip Flop

Example: $\mu_n C_{ox} = 50\mu A/V^2$; $\mu_p C_{ox} = 20\mu A/V^2$

$V_{tn} = 0.6V$; $V_{tp} = -0.8V$; $V_{DD} = 5V$



Assuming 0.25µm CMOS technology, Q=0:

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_3 = \left(\frac{0.5\mu m}{0.25\mu m}\right) \qquad \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_4 = \left(\frac{1.5\mu m}{0.25\mu m}\right)$$

Determine the minimum size of M_5, M_6, M_7 and M_8 to make the SR latch switchable.

Assume M_5 is identical to M_6, i.e. $M_5 = \frac{W}{L}$ and $M_6 = \frac{W}{L}$; $M_{5\_6} = \frac{W}{2L}$

Under this condition, the pull-down network can be modelled by a single transistor M_{5_6}, whose width is half the width of the individual devices, M_5 and M_6.

Contd.

Transistor Sizing the SR Flip Flop (Contd.)

Example: $\mu_n C_{ox} = 50\mu A/V^2$; $\mu_p C_{ox} = 20\mu A/V^2$

$V_{tn} = 0.6V$; $V_{tp} = -0.8V$; $V_{DD} = 5V$

To switch latch from $Q = 0$ to $Q = 1$,

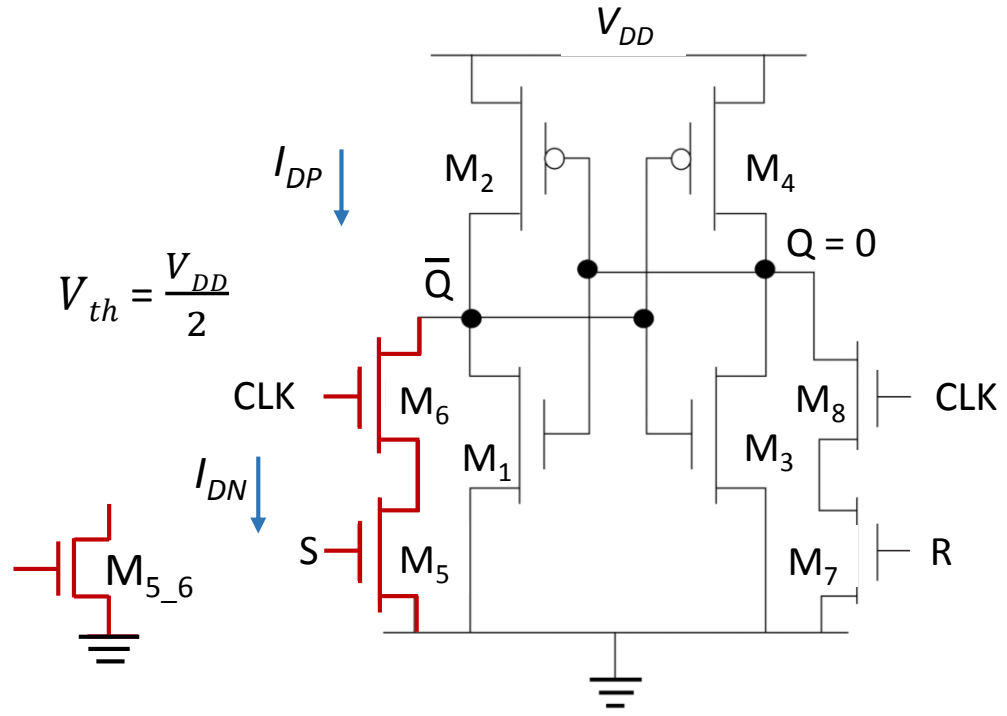
we equate the current in the inverter

for $V_{\bar{Q}} = \frac{V_{DD}}{2}$ as given below:

M_{5_6} and M_2 are in linear region.

$|V_{DS}| < |V_{GS}| - |V_t|$

$\frac{V_{DD}}{2}$ V_{DD}



$$\underbrace{I_{DN}}_{k'_n\left(\frac{W}{L}\right)_{5\_6}\left((V_{DD}-Vt_n)V_{DSn}-\frac{V_{DSn}^2}{2}\right)} = \underbrace{I_{DP}}_{k'_p\left(\frac{W}{L}\right)_{2}\left((-V_{DD}-Vt_p)V_{DSp}-\frac{V_{DSp}^2}{2}\right)}$$

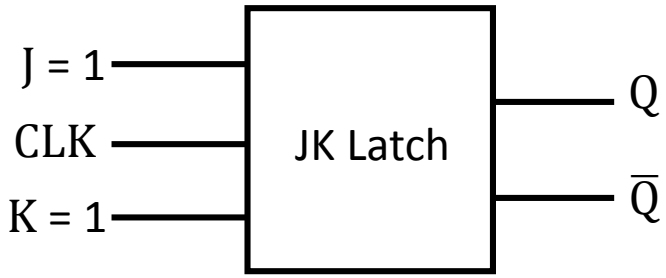
This implies that $\left(\frac{W}{L}\right)_{5\_6} \geq 2.25$ and $\left(\frac{W}{L}\right)_5$ and $\left(\frac{W}{L}\right)_6 \geq 4.5$

Clocked JK Latch based on NOR Gates

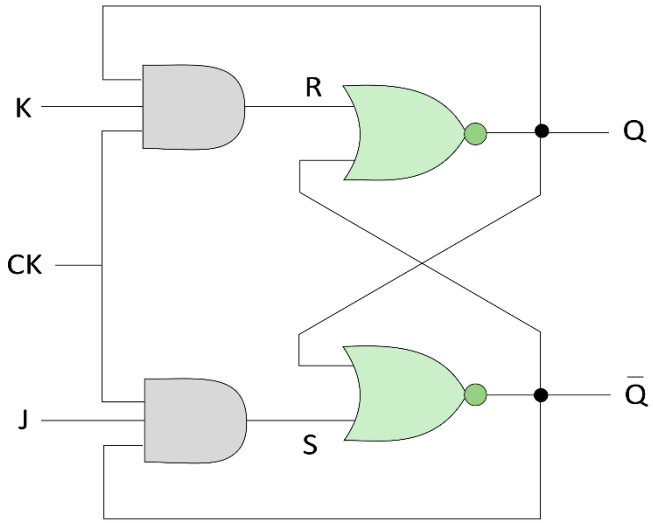
CLK: Enable

JK Latch

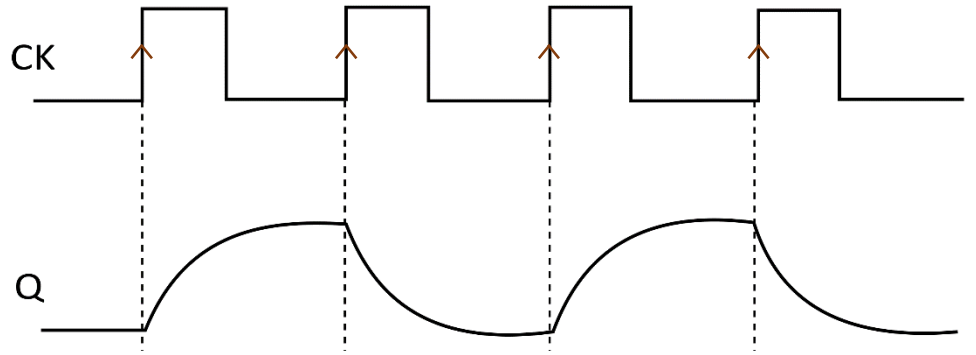
SR



J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$



Gate-level schematic

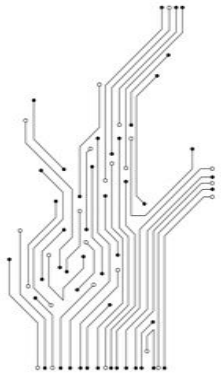


Input output graph of JK latch

Summary

Here are the key takeaways from this lesson.

- There are three critical components in sequential circuits, bistable circuits, monostable circuits and astable circuits.
- The behaviour of cross-coupled inverters is such that it switches the output from one stable state to another stable state through an unstable state.
- The CMOS SR Latch is based on NOR Gates where the delay of the latch is the total delay of NOR 1 and NOR 2 can be calculated based on the lump capacitance, $C_{\bar{Q}}$ and C_Q.
- The lump capacitance of $C_{\bar{Q}}$ and C_Q are the total parasitic capacitance of all the transistors connected to $\bar{Q}$ and Q.
- The number of transistors are reduced from 20 to 12 to 8 and finally to 6 in clocked NOR based SR latch.
- The transistor sizing of the transistors can be calculated in the 6-transistor clocked SR latch.



Thank You

Latches and Flip Flops