EE3019 - Integrated Electronics Tutorial 12

1. Determine the transfer function for the following filters:

(a) A first-order low-pass filter with a dc gain of 10 and a pole frequency at 25kHz.

(b) A first-order high-pass filter with a passband gain of 10 and a corner frequency at 100kHz.

(c) A second-order bandpass filter with a center frequency of 10^8 rad/s, a center-frequency gain of 10, and a 3-dB bandwidth of 10^6 rad/s.

2. Figure 12.1 depicts a switched capacitor integrator in which ϕ_1 and ϕ_2 are two non-overlapping clock signals. The switch is closed when the clock signal is high and opened when the clock signal is low. Assume that the initial output voltage V_{out} is 0V. Given that $C_2=2C_1$, sketch the time domain V_{out} for a dc input voltage V_{in} = 0.2V with reference to ϕ_1 and ϕ_2.

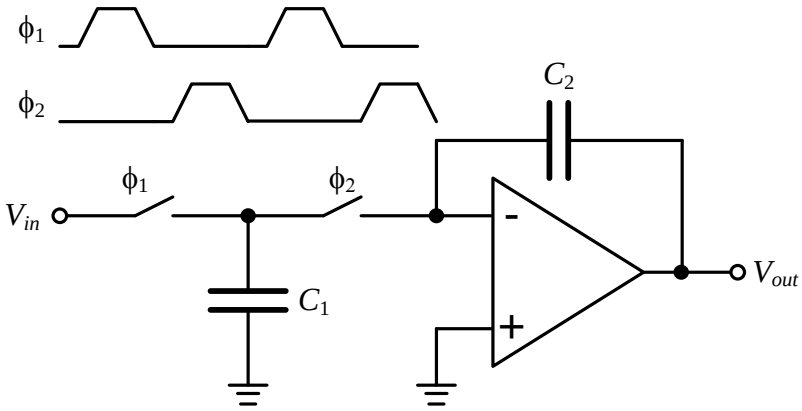

Figure 12.1

3. Figure 12.2 depicts a stray-insensitive noninverting switched capacitor integrator in which ϕ_1 and ϕ_2 are two non-overlapping clock signals. The switch is closed when the clock signal is high and opened when the clock signal is low. C_{P1} and C_{P2} are the total parasitic capacitances associated with node A and node B respectively. Show that circuit performance is not affected by the presence of C_{P1} and C_{P2}.

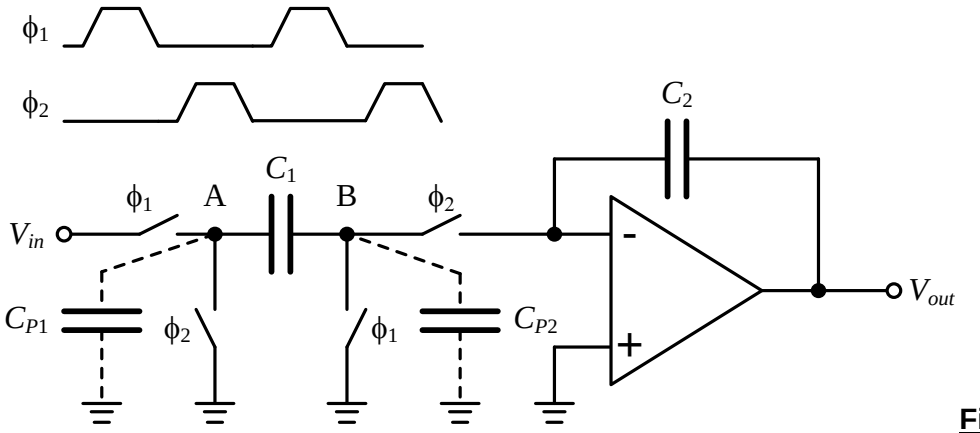

Figure 12.2

4. An inverting Schmitt trigger having dependable and symmetric characteristics is shown in Figure 12.3. Design the inverting Schmitt trigger circuit based on the following:

- **Op amp LM301 has saturation limits of ±13V**
- **Output voltage V_O= ±5V**
- **Threshold voltage = ±1V**
- **Load impedance = 10kΩ**
- **Minimum Zener diode current = 2mA**

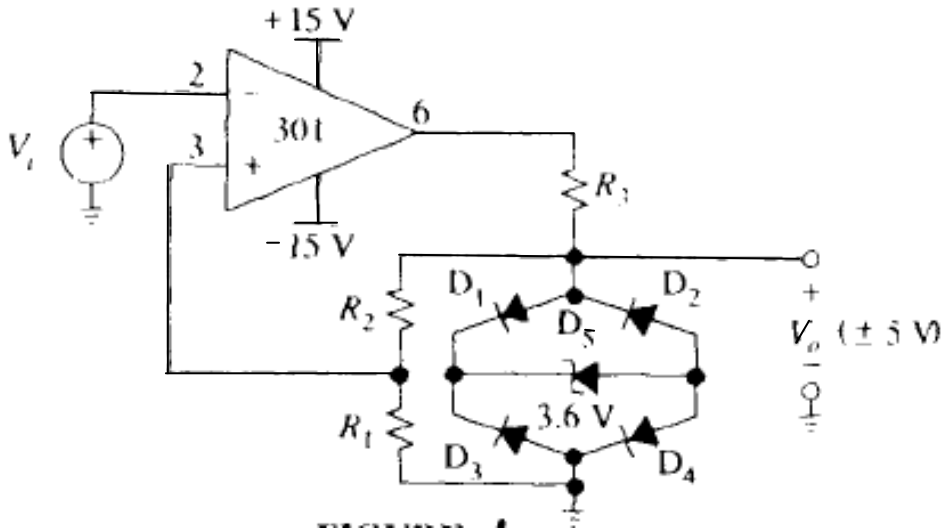

Figure 12.3