**NANYANG TECHNOLOGICAL UNIVERSITY SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING**

**ACADEMIC YEAR 2020-2021**
**SEMESTER 2**

**EE3019 INTEGRATED ELECTRONICS**

**TUTORIAL 1**

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1. Figure 1.1 depicts the schematic diagram of a CMOS inverter. Draw the top view and cross sectional view of an integrated CMOS inverter. Indicate clearly the Drain (D), Source (S), Gate (G), Body (B), Channel Width (*W*) and Channel Length (*L*) of the pMOS and nMOS transistors. List two types of interconnects commonly used for integrated circuits.

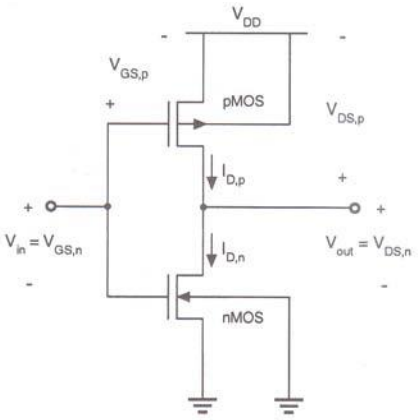


Figure 1.1

2. Find the quiescent point of the PMOS transistor in Figure 1.2 given that $V_{t0}$ = -2V and $\frac{1}{2}\mu_p C_{ox}(W/L)$ = 50uA/V$^2$.

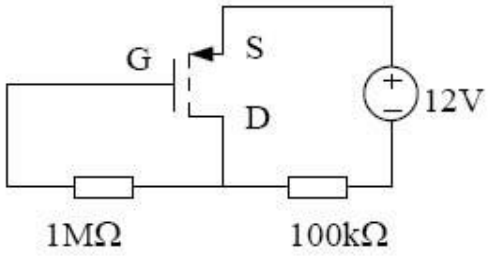


Figure 1.2

[ Answer: $v_{SG}$ = 3.32 V, $i_D$ = 86.8 μA]

3. Determine the region of operation for the transistor in Figure 1.3, given that $V_{t0}$ = -1V and $\frac{1}{2}\mu_p C_{ox}(W/L)$ = 125uA/V$^2$.

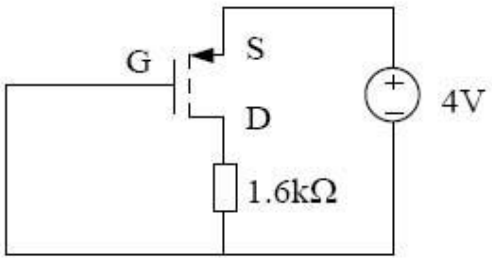


Figure 1.3

[ Answer: *Triode* ]

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**TUTORIAL 2**

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1. Consider a CMOS inverter working on $V_{DD} = 3.3$ V and with the following device parameters:

   nMOS $V_{t0n} = 0.6$ V $\mu_n C_{ox} = 60\ \mu A/V^2$ $(W/L)_n = 8$
   pMOS $V_{t0p} = -0.7$ V $\mu_p C_{ox} = 25\ \mu A/V^2$ $(W/L)_p = 12$

   (a) Calculate the noise margins and the switching threshold, $V_{th}$, of this circuit.
   (b) If the channel length of both transistors is $L_n = L_p = 0.8\ \mu m$, determine the $(W_n/W_p)$ ratio so that the switching threshold is changed to 1.4V.

   [ Answer: $NM_L = 1.1985$ V, $NM_H = 1.6042$ V, $V_{th} = 1.483$ V, $W_n/W_p = 0.94$ ]

2. Find the propagation delay for a minimum-size CMOS inverter using the average current method. Given that $\mu_n C_{ox} = 3\ \mu_p C_{ox} = 75\ \mu A/V^2$ and $(W/L)_n = (W/L)_p = 1.2\mu m/0.8\mu m$.

   $V_{DD} = 3.3$V, $|V_t| = 0.2V_{DD}$, and the unit capacitance is roughly 2 $f$F/$\mu m$ of device width plus 1 $f$F/device.

   [Answer: $t_p = 62.3$ *psec*]

3. A CMOS microprocessor chip containing the equivalent of 1 million gates operates from a 5V supply. The power dissipation is found to be 9W when the chip is operating at 120MHz and 4.7W when operating at 50MHz. What is the power lost in the chip due to clock-independent role? If 70% of the gates are assumed to be active at any time, what is the average gate capacitance in such a design?

   [ Answer: $P_S = 1.629$W, $C_{gate} = 3.51\ f$F]

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**TUTORIAL 3**

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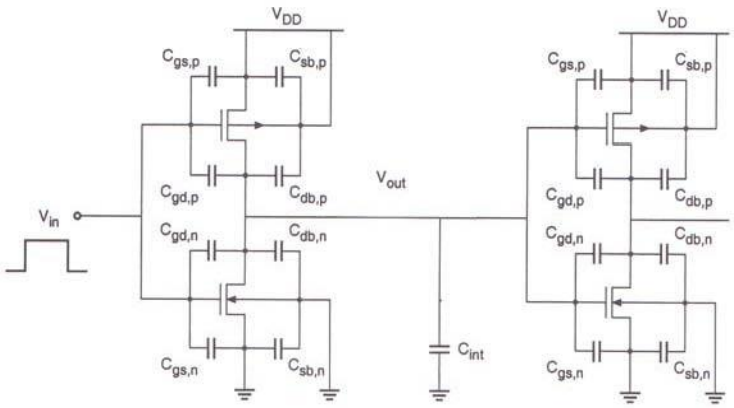
1. Consider a CMOS inverter fabricated in a 0.25μm process as depicted in Figure 3.1. Based on the parameters given below, calculate the dynamic power dissipation of inverter 1 when the inverter is clocked at 500MHz:

   *nMOS:* $C_{gsn}$= 0.7875 fF, $C_{gdn}$= 0.1125 fF, $C_{sbn}$= 1 fF, $C_{dbn}$= 1 fF,
   *pMOS:* $C_{gsp}$= 2.3625 fF, $C_{gdp}$= 0.3375 fF, $C_{sbp}$= 1 fF, $C_{dbp}$= 1 fF,
   Interconnect capacitance: $C_{int}$=0.2 fF, Supply Voltage, $V_{DD}$=2.5V




**Inverter 1** **Inverter 2**

Figure 3.1 [Answer: 19.5 μW]

2. Consider the logic gate given in Figure 3.2.
   (a) What is the logic function implemented by this CMOS transistor network?
   (b) Label the sizes of nMOS and pMOS devices such that the gate has the same drive as the inverter with $W_n$ = 0.25 μm and $W_p$ = 0.5 μm.

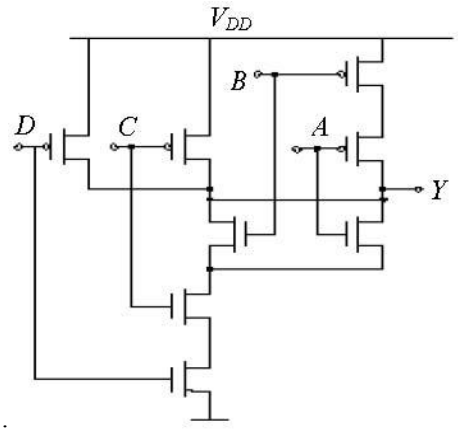



Figure 3.2

3. The transmission gate of Figure 3.2(a) and 3.2(b) is fabricated using a CMOS process technology for which $\mu_n C_{ox} = 50\mu A/V^2$ and $\mu_p C_{ox} = 20\mu A/V^2$. $V_{tn} = |V_{tp}|$, $V_{t0} = 1$ V, $\gamma = 0.5\ V^{1/2}$, $2\varphi_f = 0.6$ V, and $V_{DD} = 5$ V. Let $Q_N$ and $Q_P$ be the minimum size possible with this process, $(W/L)_n = (W/L)_p = 4\mu m/2\mu m$. The total capacitance at the output node is 70fF.

   (a) Find $i_{DN(0)}$, $i_{DP(0)}$, $i_{DN(tPLH)}$, $i_{DP(tPLH)}$, and $t_{PLH}$ for Figure 3.3(a).

   (b) Find $i_{DN(0)}$, $i_{DP(0)}$, $i_{DN(tPHL)}$, $i_{DP(tPHL)}$, and $t_{PHL}$ for Figure 3.3(b). At what value of $v_o$ will $Q_P$ turn off?

   (c) Find $t_p$.

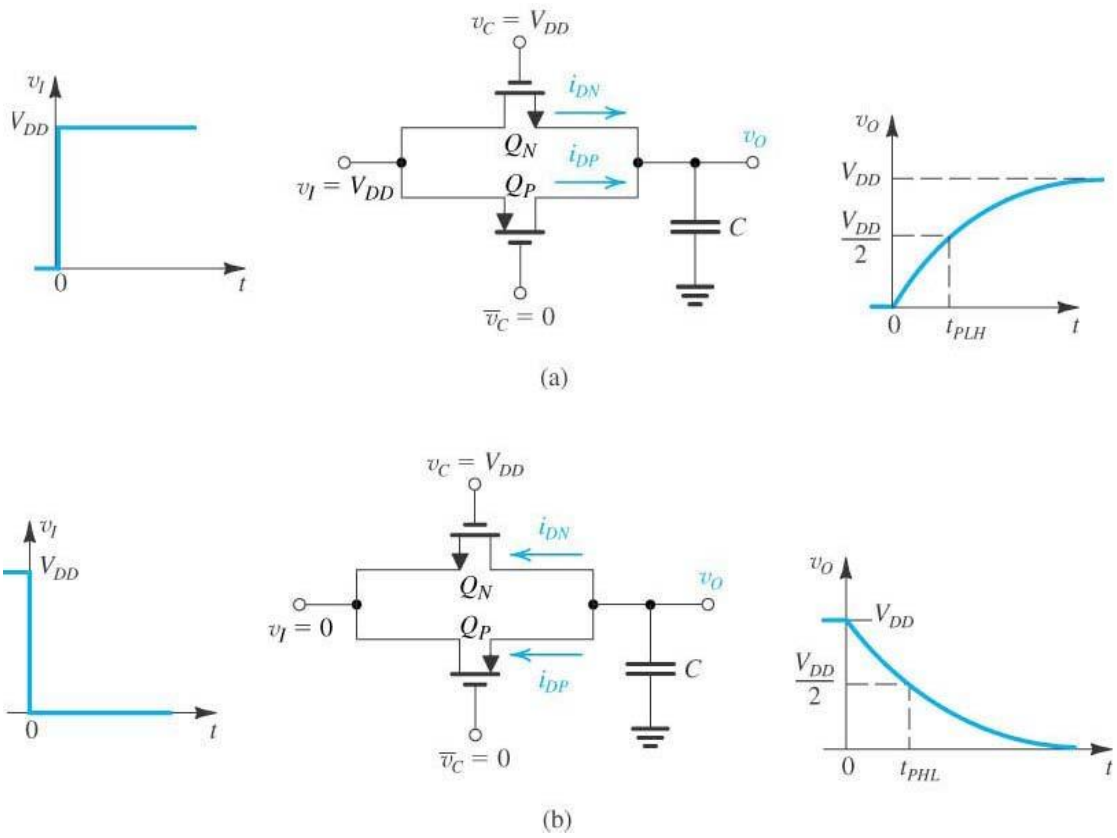



Figure 3.3

[Answer: 0.24ns, 0.19ns, 1.6V, 0.215ns ]

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**TUTORIAL 4**

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1. For the gate-level schematic of the level-triggered Clocked NOR based SR latch depicted in Figure **4.**1, realize the level-triggered Clock NOR based SR latch in transistor level with not more than 12 transistors. In integrated circuit design, two important design criteria are small IC area and low power dissipation. Try to implement the level-triggered Clocked NOR based SR latch using not more than 8 transistors.

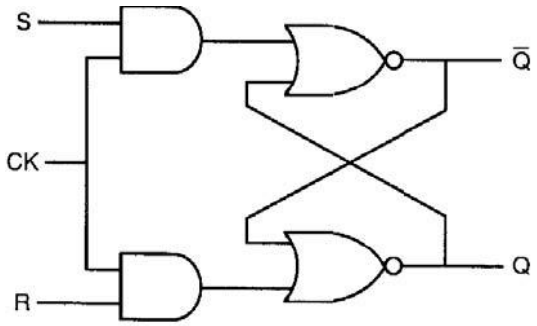


Figure **4.**1

2. The Clock SR latch depicted in Figure **4.**2 is fabricated in a process technology for which $\mu_n C_{ox}$ = 2.5$\mu_p C_{ox}$ = 50μA/V$^2$, $V_{tn}$ = $|V_{tp}|$=1V and $V_{DD}$= 5V. Given that $(W/L)_1$ =$(W/L)_3$ = 6μm/2μm and $(W/L)_2$ =$(W/L)_4$ = 15μm/2μm, determine the W/L ratio of $M_5$, $M_6$, $M_7$ and $M_8$.

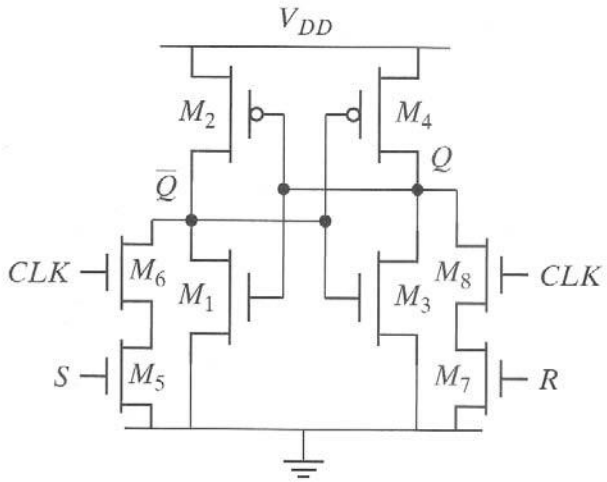


Figure **4.**2

[Ans: $(W/L)_5$ & $(W/L)_6 \geq 6$]

3. A 256K x 1 MOS DRAM is organised as a 512 row x 512 column matrix of memory cells. The cycle time comprising a read/write and refresh takes 200 ns. The refresh period is 2 ms.

   (a) Determine the time (in %) spent in the refresh activity.

   (b) A microprocessor is to be connected a number of 256K memory ICs. This microprocessor outputs a refresh cycle every 1 μs. Assuming that no additional DRAM refresh circuitry is used, determine the number of 256K memory ICs that can be connected to this microprocessor.

[Answer: *5.12%*, *3ICs*]

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# EE3019 INTEGRATED ELECTRONICS

## TUTORIAL 5

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1. (a) Draw a circuit schematic of a SRAM cell based on 2-MOS transistor 2-polysilicon resistor load structure.

   (b) A 16K SRAM is realized by the cells given in (a). This SRAM IC dissipates 0.1W. Determine the resistance of the polysilicon load resistor. Assume that the MOS transistors are ideal, and that $V_{DD}$ = 5V.

   (Ans: 4.096MΩ)

   ***Hint : Work out the operating region of the transistors***

   (c) A 16K x 1 SRAM memory (each cell comprises 4 MOS transistors and the select line comprises 2 MOS transistors) is organised as a square matrix with 128 cells on each side, occupying a total IC area of 2 mm x 2 mm. The select line is 2μm wide and the select transistor gates are 2μmx2μm. The polysilicon select line is 22 Ω/□, the capacitance to substrate for the polysilicon is 0.08fF/μm² and the data capacitance is 1fF/μm². The select line is driven from one end.

   Assuming a simplistic model with the total select line resistance and capacitance represented as a lowpass *RC* circuit, determine the select line delay. For this simple model, assume that this delay is equal to the 10% -90% rise time at the far end (of the select line) and assume that the select line is driven by an ideal voltage step. (61.2 ns).

   Note: Data capacitance is the capacitance between the polysilicon gate and the channel of the transistor under the gate

   *Hint: Determine the equivalent R and C and determine the 10% -90% rise time.*

2. A dynamic CMOS Read Only Memory (ROM) has been designed with a core array consisting of 64 rows with a pitch of 12μm and 64 columns with a pitch of 10μm, as shown in Figure 1. All of the nMOS transistors have channel widths *W*=4μm, channel length *L*=2μm and source/drain lengths Y=5μm. As a designer, determine the row access time of the row 64 in the ROM. Assume that row 64 is running over 30 nMOS transistors and column 64 has 20 nMOS transistors connected to it. Also assume that the row capacitance of each cell is dictated primarily by the thin oxide capacitance of the nMOS transistor (i.e. the polysilicon capacitance outside the active region is negligible). Device parameters are as follows:

$C_{ox} = 350\mu F/m^2$
$C_{poly} = 2.2pF/cm^2$ *and* $R_{poly} = 25\Omega$ / sq
Polysilicon line width = 2μm

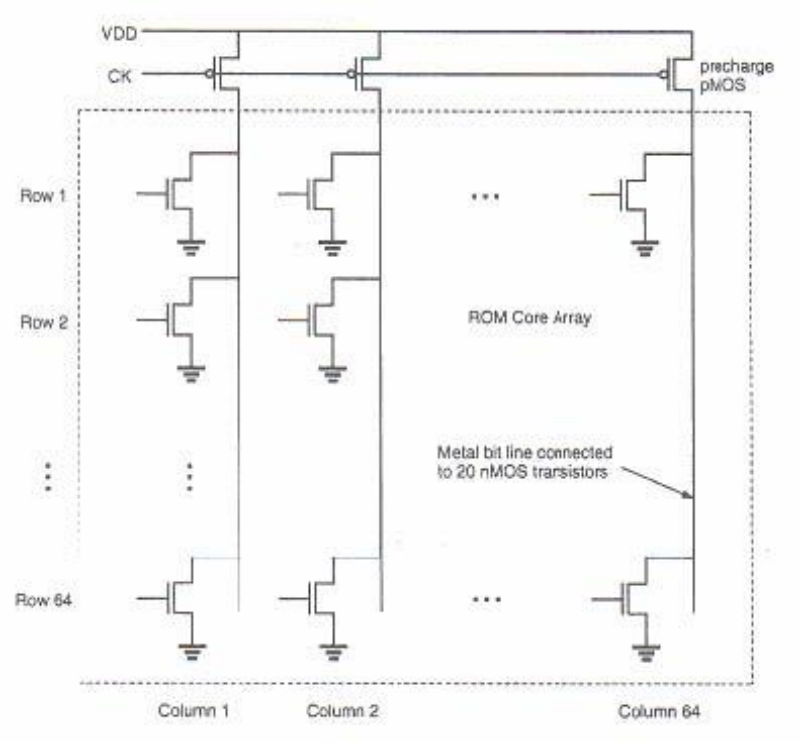


**Figure 5.1** A dynamic CMOS Read Only Memory (ROM)

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# EE3019 INTEGRATED ELECTRONICS

## TUTORIAL 6

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1. Figure **6**.1 shows a non-inverting buffer op-amp configuration. Assuming that the op-amp has $A = 10$, infinite input resistance and zero output resistance, what is $\beta$? What is the closed-loop voltage gain? What is the amount of feedback in dB? For $v_S = 1$ V, find $v_o$, and $V_i$. If $A$ decreases by 10%, what is the corresponding decrease in $A_f$?

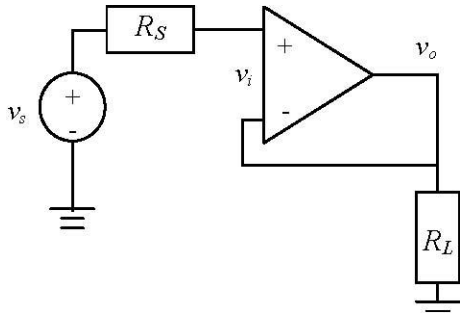
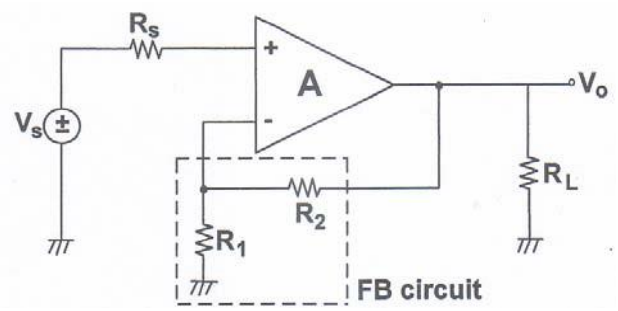



Figure **6**.1

2. An amplifier has an open loop gain of 5000 ± 500 V/V, and a dominant pole at 4 kHz. If the amplifier is used in the design of a feedback amplifier with a gain variation of no more than ± 1%, find the feedback factor of the feedback network used, the closed-loop gain, and the bandwidth of the feedback amplifier.

[Answer: $1.8 \times 10^{-3}$, 500, 40 kHz]

3. Figure **6**.2 shows a non-inverting op-amp. If the open loop voltage gain $A = 10^5$, find the ratio of $R_2/R_1$ to obtain a closed-loop voltage gain of 100. If there is a 15% change in the value of $A$, find the corresponding change in the closed-loop gain.




[Answer: 99, 0.015%]

Figure **6**.2

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**TUTORIAL 7**

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1. For the circuit shown in Figure 7.1, use the feedback method to find the voltage gain $V_o/V_s$, the input resistance $R_{in}$ and the output resistance $R_{out}$. Given that the op-amp has open-loop gain $\mu = 10^4$ V/V, $R_{id} = 100$ kΩ, and $r_o = 1$ kΩ.

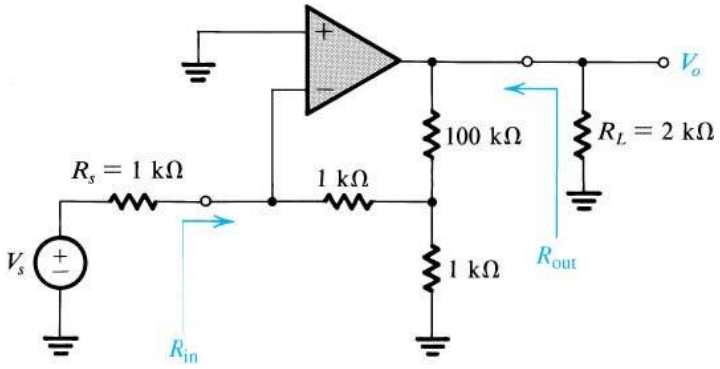



Figure 7.1

[Answer: -192V/V, 29.9Ω, 29.5Ω]

## EE3019 - Integrated Electronics Tutorial 8 – **Revision**

***If you have difficulty with this tutorial, please revise EE2002***

**1. The BJT-based Wilson Current Mirror is depicted in Figure 8.1.**

**(a) Show that the current gain is given by** $\frac{I_o}{I_{REF}} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$

**and discuss the implication of this current gain (with respect to the simple current mirror).**

**(b) Design an equivalent CMOS Wilson Current Mirror circuit with an output current of 0.2 mA. Assume that $V_{DD}$ = 9V, and the MOSFET parameters are $\mu_n C_{ox} W/L$ = 1.0 x $10^{-4}$ A/$V^2$, $V_t$ = 0.4 V.**

**(c) Determine the minimum output voltage of your Current Mirror design.**

**[(b) $R$ = 21 kΩ; (c) $V_{out} \geq$ 4.4 V]**

**2. The transistor in Figure 8.2 has the following parameters: $\beta$ =100, $r_o = \infty$, $V_{BE}$ = 0.7V and $V_{CEQ}$ = 2V. Assume that $V_T$ = 25mV. The input source has an internal impedance $R_S$.**

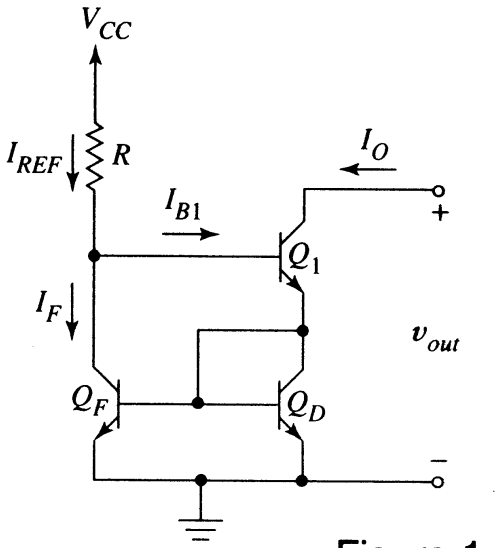
**(a) Determine the value of $R_C$. [1.05 k Ω]**

**(b) Determine the transconductance $g_m$ and $r_\pi$. [334mA/V, 299.5Ω]**

**(c) Determine the voltage gain as a common collector amplifier and as a common emitter amplifier. [0.975V/V, -2.05V/V]**

**(d) Determine the input resistance seen by the input signal source (this includes $R_S$). [51.8 kΩ]**

**(f) Determine the output resistances taken at the common collector amplifier output and at the common emitter amplifier output. [12.54 Ω, 1.05 kΩ]**



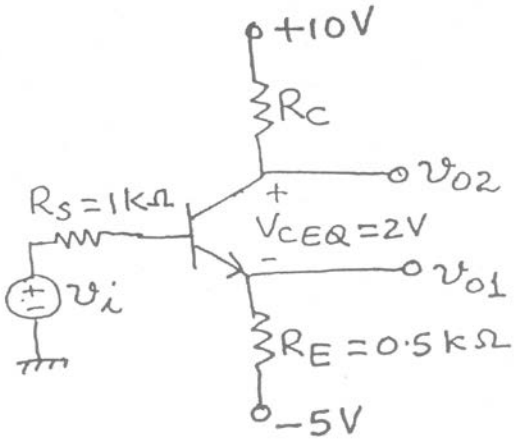



Figure 8.1 Figure 8.2

3. **A BJT differential amplifier is depicted in Figure 8.3. The current source $I$ = 100μA and the transistor parameters are: npn: $V_A$ = 200V, $\beta$ = 100; pnp: $V_A$ = 100V, $\beta$ = 50. Assume $V_T$ = 26mV. Determine (or by inspection, state) the following:**

   **(a) differential input resistance (assume that the current source is ideal),**

   **(b) output resistance,**

   **(c) equivalent transconductance,**

   **(d) differential voltage gain, and**

   **(e) differential voltage gain when the output is connected to a subsequent stage with an input resistance of 1 MΩ.**

   **[(a) 104 kΩ; (b) 1.33 MΩ; (c) 1.92 mA/V; (d) 2554 V/V; 1096 V/V]**

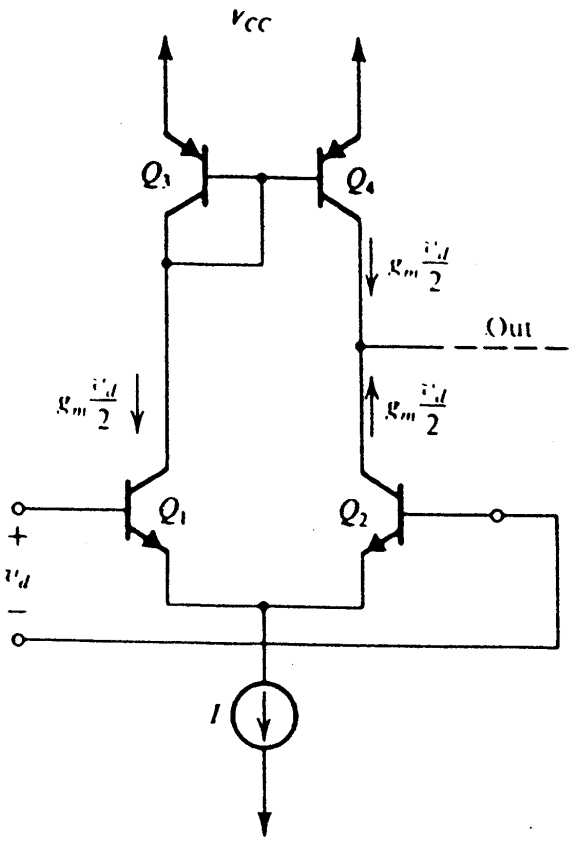



Figure 8.3

# EE3019 - Integrated Electronics Tutorial 9

**1.** For the circuit of Figure 9.1, the BJT ($Q_1$) has $\beta = 100$ and $V_{BE} = 0.7V$, and the (ideal) Zener diode has a breakdown current $I_{zk} = 10mA$. The unregulated supply voltage $V_{UR}$ is a sawtooth signal that ripples between 19V and 21V.

(a) If the circuit is designed to provide a 10V-1A regulated power supply to a load $R_L$, determine the Zener voltage $V_Z$ required and the maximum value of $R_1$ allowable.

(b) If this maximum value of $R_1$ is used, find the required minimum power ratings of the Zener diode and the series pass transistor $Q_1$.

**[(a) 10.7V, 417Ω; (b) 264.3mW, 11W]**

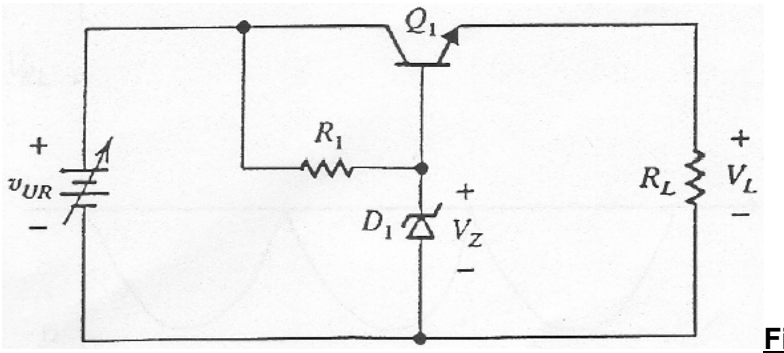



Figure 9.1

**2.** For the series regulator shown in Figure 9.2, assume that $R_L = 32\Omega$, $V_Z = 10V$, and for the BJTs, $\beta = 100$ and $V_{BE} = 0.7V$.

(a) Calculate the power efficiency of the regulator. (*Hint*: Express $V_L$ in terms of $V_Z$ and other components in the circuit. Verify the assumptions made in deriving $V_L$).

(b) The Zener diode voltage thermal coefficient is +3mV/K and the base-emitter voltage thermal coefficient is -2mV/K. Assuming that the Zener diode and base-emitter voltages as well as their thermal voltages have negligible change with their existing operating currents. Calculate the thermal coefficient of the output voltage.

**[(a) 52.6%; (b) +1.5mV/K]**

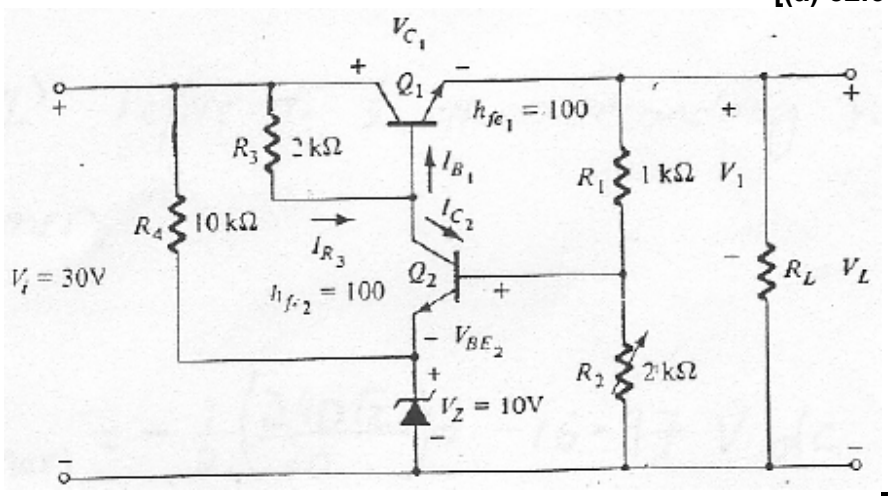



Figure 9.2

3. **A simple current bias reference circuit based on the base-emitter junction voltage is depicted in Figure 9.3. Determine the sensitivity *S* of the output current to supply voltage $V_{CC}$. It is given that $I_S = 5 \times 10^{-15}$A and assume that $V_T = 26$ mV.**

   **(*Hint*: Assume that $V_{CC} >> V_{BE(on)}$ and use this to simplify the calculation.)**

   **[0.04]**

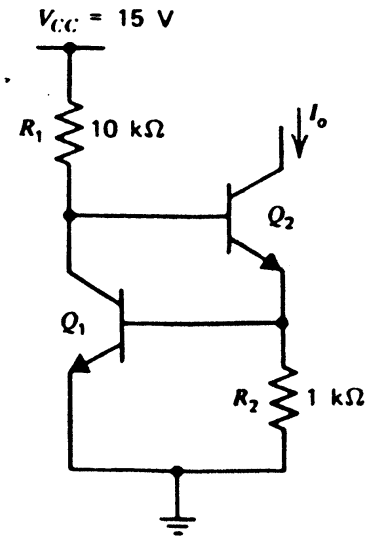



**Figure 9.3**

# EE3019 - Integrated Electronics Tutorial 10

1. A bias source is depicted in Figure 10.1 where $Q_2$ is twice the size of $Q_1$. The other transistors are the same size as $Q_1$.
   (a) State the basic mechanism of this bias source.
   (b) Derive the variation of the fractional temperature coefficient for the output current.
   (c) Determine the resistance $R_2$ for the current bias reference circuit to obtain an output of 100μA and the resultant $TC_F$ at room temperature ($T$=300K). Assume that the resistor temperature coefficient is 1500 ppm/°C.

   **[(c) 180Ω, 1800ppm/°C]**

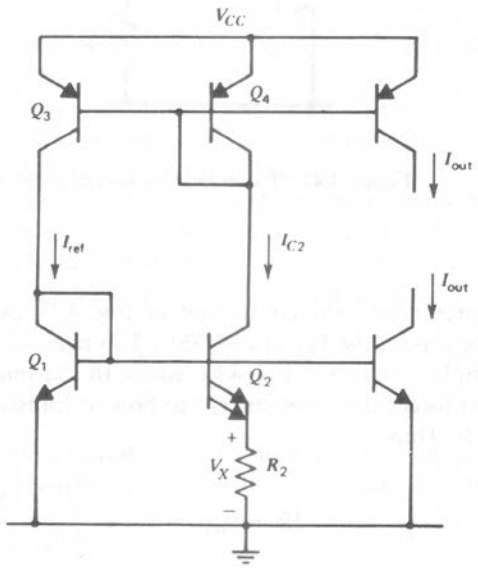



**Figure 10.1**

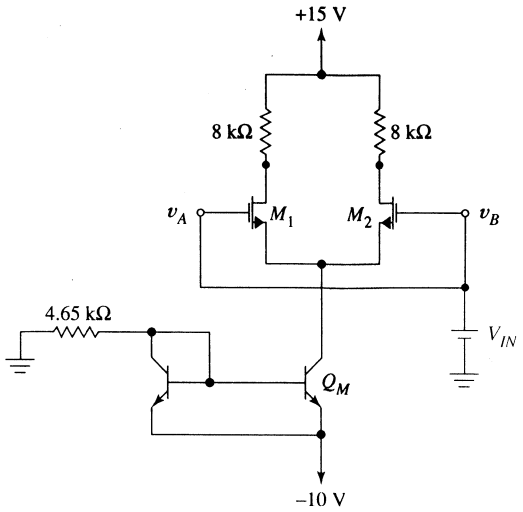


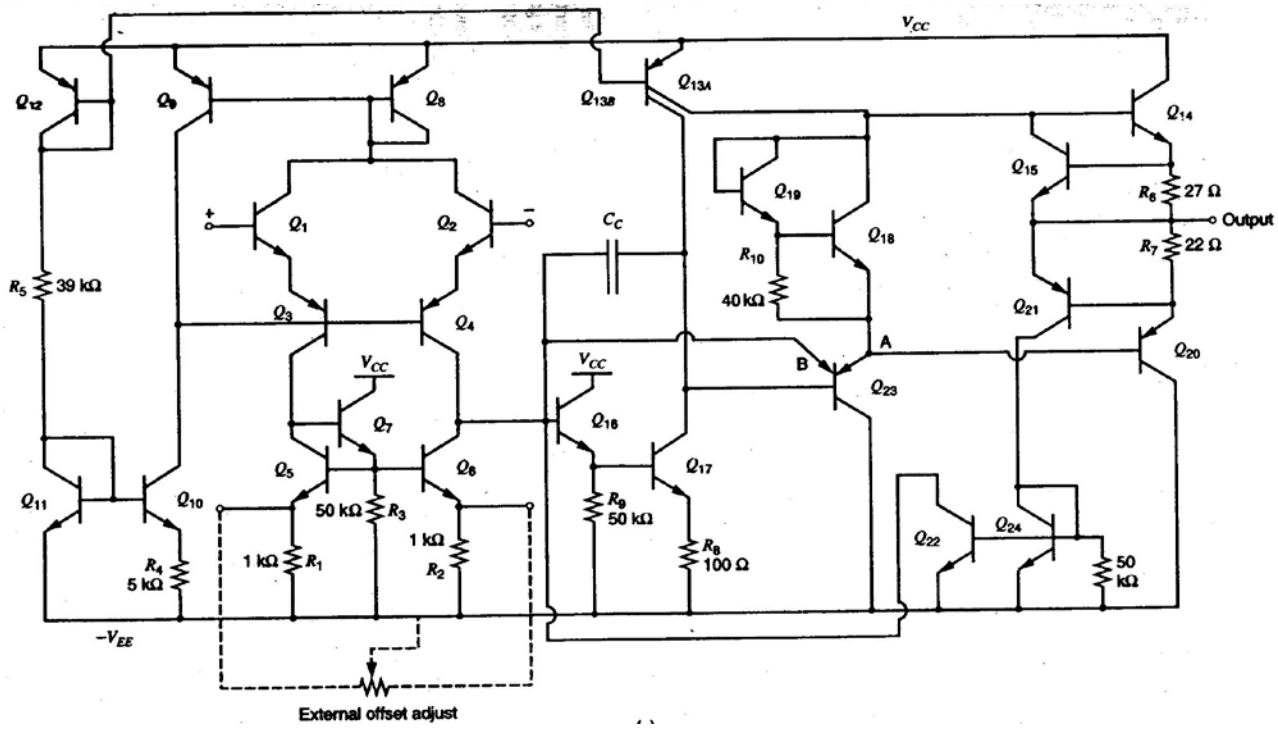

**Figure 10.2**

2. A differential amplifier depicted in Figure 10.2 comprises 4 transistors where
   MOS transistors: $\mu_n C_{ox} W/L = 0.2 \times 10^{-3}$ A/V$^2$, $V_t = 0.5$ V
   Bipolar transistors: $V_{CE(sat)} = 0.2$ V.
   Assume that the two MOSFETs have an identical aspect (i.e. $W/L$) ratio and that the two BJTs have identical emitter areas.
   (d) Show that all the MOSFETs and BJTs are active for the zero-input condition, i.e. $V_{in} = 0$.
   (e) Find the maximum and minimum common-mode input voltages, i.e. the limits of operation where the circuit remains in active operation.

   **[(b) -6.14V ≤ $V_{in}$≤ 7.5V]**

3. Explain the function of each transistor in the op amp shown in Figure 10.3.

**Figure 10.3**


$V_{CC}$
$Q_{13A}$
$Q_{13B}$
$Q_{14}$
$Q_{15}$
$R_6$ 27 Ω
Output
$R_7$ 22 Ω
$Q_{12}$
$Q_9$
$Q_8$
$Q_1$
$Q_2$
$C_C$
$Q_{19}$
$Q_{18}$
$R_{10}$
40 kΩ
$R_5$ 39 kΩ
$Q_3$
$Q_4$
$Q_{21}$
$Q_{20}$
A
B
$Q_{23}$
$V_{CC}$
$Q_7$
$Q_{16}$
$Q_{17}$
$Q_5$
$Q_6$
$Q_{11}$
$Q_{10}$
50 kΩ $R_3$
1 kΩ $R_1$
1 kΩ $R_2$
$R_9$ 50 kΩ
$R_8$ 100 Ω
$Q_{22}$
$Q_{24}$
50 kΩ
$R_4$ 5 kΩ
$-V_{EE}$
External offset adjust

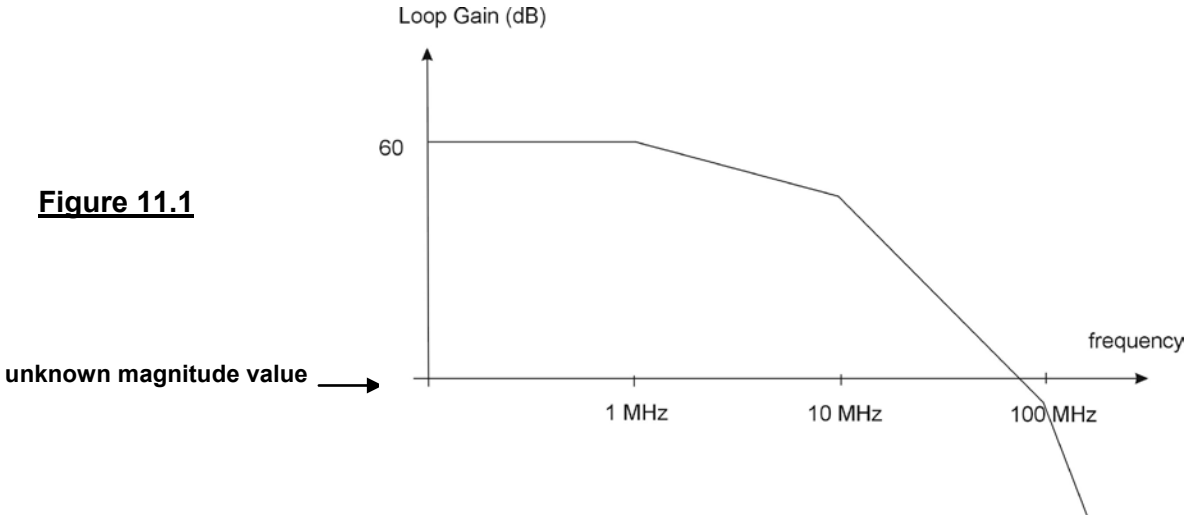
# EE3019 - Integrated Electronics Tutorial 11

**1.** **A Bode diagram depicting the magnitude loop gain, $|T(j\omega)|$, of a feedback amplifier is depicted in Figure 11.1.**

**(a)** **By inspection, write an expression for $|T(j\omega)|$ and for $\angle T(j\omega)$.**
**(b)** **Estimate the frequency where $|T(j\omega)|=1$ and determine the phase angle at this frequency.**
**(c)** **Determine the frequency where the $\angle T(j\omega) = -180°$.**

**[(b) ~86.5 MHz, ~213°; (c) ~33 MHz]**

**Figure 11.1**




**2.** **The DC open loop of an op amp is 2 x $10^6$ and the three dominant poles are 10 kHz, 1 MHz and 100 MHz. The op amp is used as a unity gain inverting amplifier with an input resistance of 100 kΩ. Draw the schematic of the amplifier and determine if the amplifier is stable.**

**[unstable]**

**3.** **(a)** **Draw the circuit schematic of an inverting amplifier with an ideal closed-loop gain of $-R_2/R_1$.**
**(b)** **Draw the feedback model of your design in part (a).**
**(c)** **Assuming that the open-loop gain of the op amp is given by**

$$a(j\omega) = \frac{a_0}{1 + j(\omega/\omega_a)}$$ **, show that the closed loop response is**

$$A(j\omega) = \frac{A_0}{1 + j(\omega/\omega_A)}$$ **where**

$$\left.\begin{aligned} A_0 &= \frac{b-1}{b}\,\frac{1}{1+\frac{1}{a_o b}} \\ \omega_A &= \omega_a(1 + a_0 b) \end{aligned}\right\} \quad \text{where } b = \frac{R_1}{R_1 + R_2}$$

**(d)** **Interpret your derivations in part(c).**

# EE3019 - Integrated Electronics Tutorial 12

**1. Determine the transfer function for the following filters:**

**(a) A first-order low-pass filter with a dc gain of 10 and a pole frequency at 25kHz.**

**(b) A first-order high-pass filter with a passband gain of 10 and a corner frequency at 100kHz.**

**(c) A second-order bandpass filter with a center frequency of $10^8$ rad/s, a center-frequency gain of 10, and a 3-dB bandwidth of $10^6$ rad/s.**

**2. Figure 12.1 depicts a switched capacitor integrator in which $\phi_1$ and $\phi_2$ are two non-overlapping clock signals. The switch is closed when the clock signal is high and opened when the clock signal is low. Assume that the initial output voltage $V_{out}$ is 0V. Given that $C_2=2C_1$, sketch the time domain $V_{out}$ for a dc input voltage $V_{in}$ = 0.2V with reference to $\phi_1$ and $\phi_2$.**

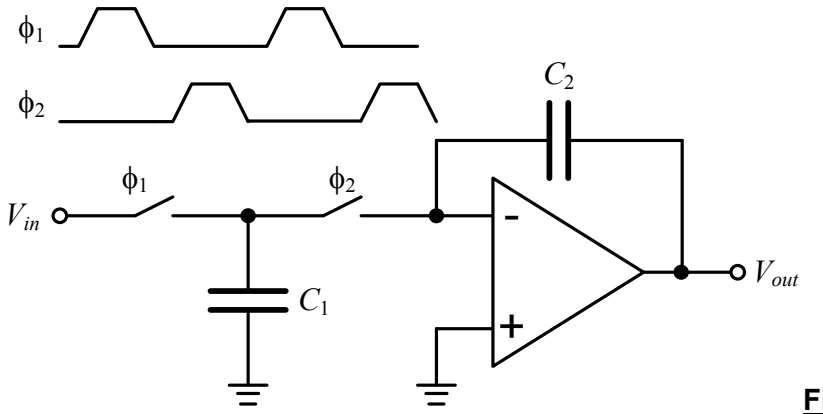



**Figure 12.1**

**3. Figure 12.2 depicts a stray-insensitive noninverting switched capacitor integrator in which $\phi_1$ and $\phi_2$ are two non-overlapping clock signals. The switch is closed when the clock signal is high and opened when the clock signal is low. $C_{P1}$ and $C_{P2}$ are the total parasitic capacitances associated with node A and node B respectively. Show that circuit performance is not affected by the presence of $C_{P1}$ and $C_{P2}$.**

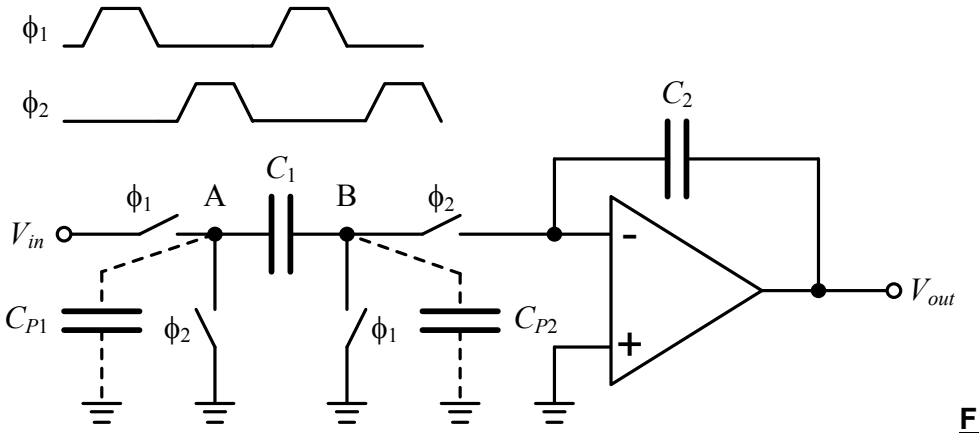



**Figure 12.2**

**4. An inverting Schmitt trigger having dependable and symmetric characteristics is shown in Figure 12.3. Design the inverting Schmitt trigger circuit based on the following:**

- **Op amp LM301 has saturation limits of ±13V**
- **Output voltage $V_O$= ±5V**
- **Threshold voltage = ±1V**
- **Load impedance = 10kΩ**
- **Minimum Zener diode current = 2mA**

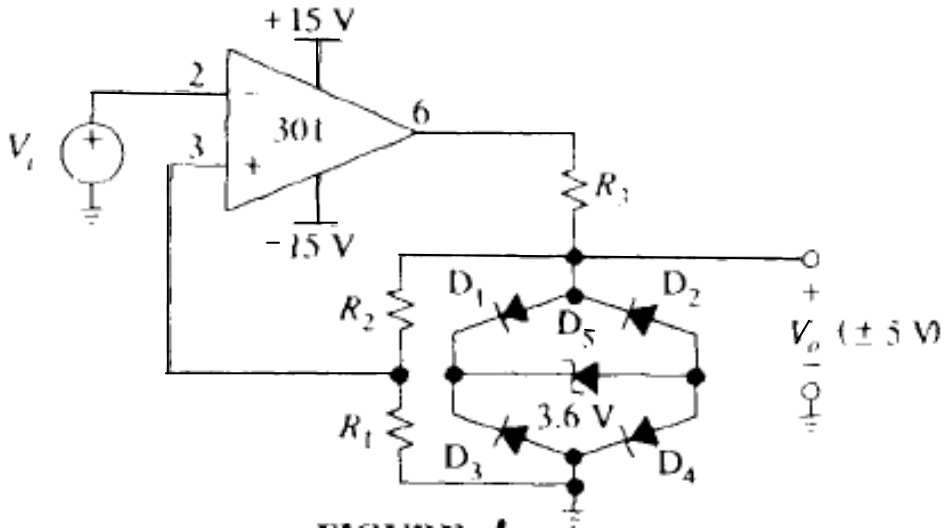



**Figure 12.3**