EE2002

TUTORIAL 1 (with answers at the back)

1. Find an expression for v_{OUT} as a function of v_1 and v_2 in each of the op-amp circuits of Fig.T1-1 and also determine the input resistance(s) for each of the op-amp circuits. Assume op-amps used are ideal.

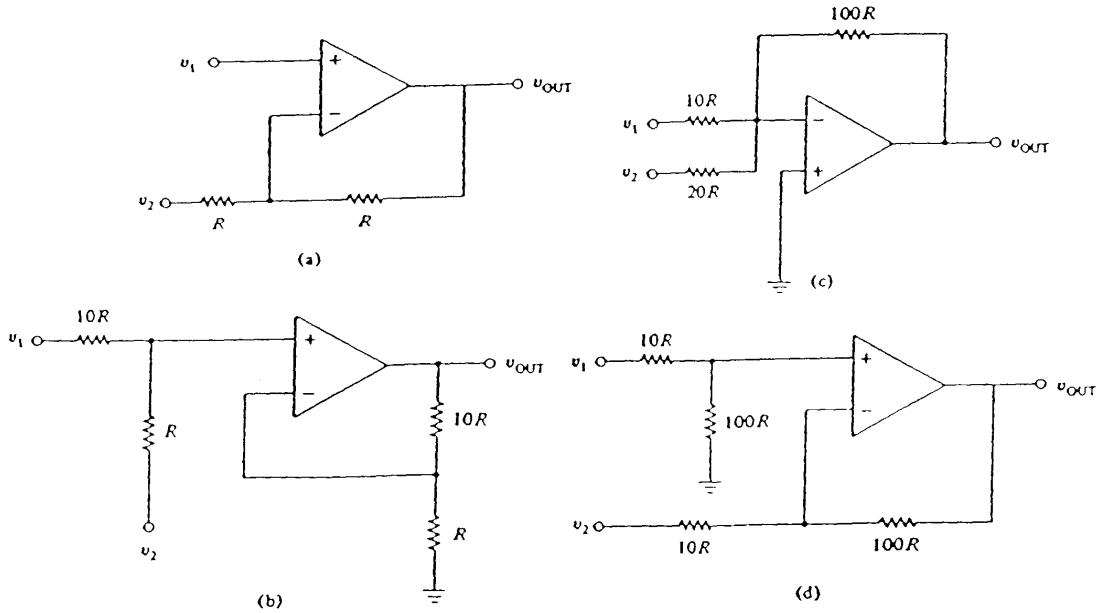

Fig T.1-1

2. Consider an op-amp follower (i.e. the output is connected to the negative input) powered by ±l5V supplies. The input voltage is set to 1V and the output feeds a 100 Ω resistive load R_L. With R_L disconnected, the current I_p from V_{CC} into the op-amp equals the current I_N from the op-amp into V_{EE}. The op-amp used is assumed to be ideal.

   a) Draw a diagram of this circuit. Label the current I_p and I_N.
   b) What is the difference between the power supply currents I_p and I_N when R_L is connected?
   c) Find the additional power drawn from the power supplies when R_L is connected.

3. A high-gain op-amp circuit is formed by cascading two inverting amplifiers in series. Both op-amps are connected to ±l5V power supplies. The first stage has gain of 20. The cascade is to be designed so that the peak output voltage of the second stage comes no closer than 1 V to either power supply voltage. If the input is equal to a 25-mV peak sinusoid, what is the maximum permissible gain of the second stage if its output is to remain within its allowed swing limits? Assume op-amps used are ideal.

4. Find an expression for v_{OUT} in the circuit shown in Fig Tl-2. Assume the op-amp used is ideal.

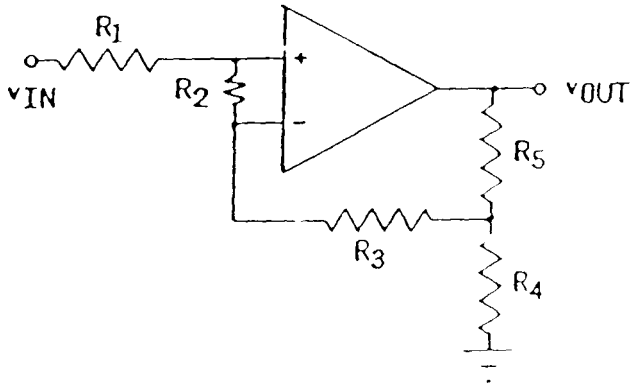

Fig. T 1-2

5. An inverting amplifier with a gain of -10 is made from a nonideal op-amp having an input offset voltage of lmV. A sinusoidal input voltage of 0.1mV peak amplitude is applied. What are the resulting ac and dc components of the output voltage?

6. A difference amplifier with a gain of 2 is made from an op-amp with the following parameters: V_{IO}=2mV maximum; I_{BIAS}=100nA; I_{IO}=0. If both inputs are set to zero, what is the maximum expected offset value of v_{OUT}?

Partial Answers to Tutorial 1

1

(a) $V_{OUT} = 2v_1 - v_2$
$R_{in1} = \infty$
$R_{in2} = R$

(b) $V_{OUT} = v_1 + 10\ v_2$
$R_{in1} = 11R$
$R_{in2} = 11R$

(c) $V_{OUT} = -(10v_1 + 5\ v_2)$
$R_{in1} = 10R$
$R_{in2} = 20R$

(d) $V_{OUT} = 10(v_1 - v_2)$
$R_{in1} = 110R$
$R_{in2} = 10R$

2. (b) $I_P - I_N = 10$ mA
(c) The additional power drawn from V_{CC} is
$\triangle P = 150$ mW
No additional power is drawn from V_{EE}, the negative supply.
3. The maximum permissible gain of the second stage is 28.

4. $\mathbf{v_{OUT} = (\frac{R_5 + R_4}{R_4})v_{IN}}$

5. $\mathbf{v_{OUT} = \sum_{i=1}^{2} (v_{OUT})_i = (-1\sin\omega t + 11)\ mV}$

6. $v_{OUT} = 6$ mV

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TUTORIAL 2 (with answers at the back)

1. An op-amp is connected in the noninverting amplifier configuration. A voltage source of value v_S is connected via a series resistance R_S to the v_+ terminal.

   a) Find an expression for v_{OUT} as a function of v_s if the op-amp is ideal.

   b) If the op-amp is nonideal and has input bias currents I_+ and I_- and input offset voltage V_{IO}, find an expression for v_{OUT} when v_S=0.

   c) Combine the answers to parts (a) and (b) to find the total output when v_S is nonzero.

   d) The feedback resistors in the amplifier are set to 25kΩ and 100 kΩ, so that the amplifier has a gain of 5. If $I_{BIAS}=(I_+ + I_-)/2$=100 nA, I_{IO}=-40nA, and V_{IO}=2mV, what value of R_S will minimize the total dc offset component to v_{OUT}?

2. A high-gain op-amp circuit is formed by cascading two inverting amplifiers in series. Both op-amps are connected to ±15V power supplies. The first stage has a gain of -20. The cascade is to be designed so that the peak output voltage of the second stage comes no closer than 1V to either power supply voltage. The cascade is built from nonideal op-amps with V_{IO}=2mVand $I_{BIAS}\approx 0$, I_{IO}=0.

   a) If both stages remain in the linear region, find an expression for the output voltage that includes the effect of V_{IO}. Express the gain of each stage in terms of the ratio of its resistor values. (Stage 1 gain = $-R_2/R_1$; stage 2 gain = $-R_4/R_3$.)

   b) If v_{IN} is a sinusoid of 25mV peak magnitude, what is the maximum gain of the second stage if v_{OUT} is to remain within the specified swing limits?

3. An op-amp is connected in the inverting amplifier configuration. The gain of the amplifier is set to –50 by using 100kΩ and 2 kΩ resistors in the feedback circuit. The v+ terminal is connected to ground. The op-amp is non-ideal and has parameters I_{BIAS}=0; I_{IO}=0, V_{IO}=0, and slew rate=1V/us.

   a) If the input voltage is a 10-mV peak sinusoid, what is the maximum frequency that can be applied before the slew rate limitation is reached?

   b) Repeat part((a))for an input voltage that consists of a 10 mV peak triangular waveform.

   c) Sketch the output voltage versus time if the input is a 10 mV peak square wave.

4. An op-amp is connected in the non-inverting amplifier configuration. A gain of 11 is achieved by using 500 kΩ and 50 kΩ resistors in the feedback circuit. The signal source connected to the v_+ input terminal has a 50 Ωseries Thevenin resistance.

   a) If the op-amp has an input bias current of luA, calculate the dc value of v_{OUT} when v_{IN}=0. Assume I_{IO}=0.

   b) Choose an additional resistor to be put in series with the input source so that dc offset found in part (a) is forced to zero.

5. An op-amp circuit with a dc gain of 400 is formed by cascading in series two inverting amplifiers with gains of -20. Both op-amps are connected to ±l5V power supplies and have slew rates of 1V/us.

   a) If the input is a sinusoidal voltage, what peak magnitude drives the output to its full swing range if $V_{sat\text{-}pos}$=14.3 $V_{sat\text{-}neg}$=-14V?

   b) For the input voltage found in part (a), what is the maximum frequency in hertz that the input voltage can have before slew rate limitation becomes important ?

6 .a) The op-amp in Fig. 1 has a unity-gain frequency of l.2MHz.
   i) What is the closed loop BW?
   ii) What is the closed-loop gain at 600kHz ?

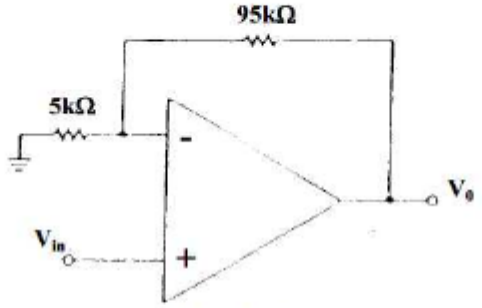

Fig. 1

6 .b)The op-amp shown in Fig. 2 has a SR of 4 V/μS and a unity-gain frequency of 2MHz. Determine whether the amplifier will distort the input signal shown.

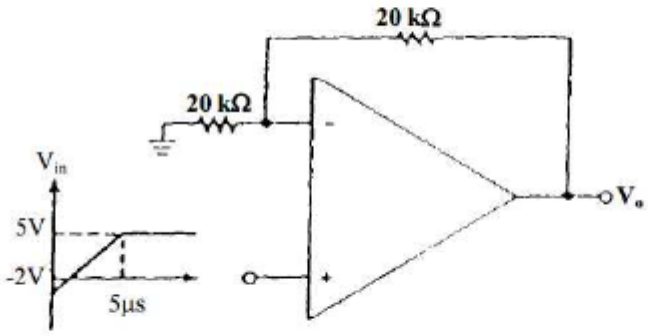

Fig. 2

Answers to Tutorial 2

1. (a) $\mathbf{v_{OUT}} = \left(\frac{\mathbf{R_2 + R_1}}{\mathbf{R_1}}\right)\mathbf{v_s}$

   (b) $\mathbf{v_{OUT}} = \mathbf{V_{IO}}\left(\mathbf{1} + \frac{\mathbf{R_2}}{\mathbf{R_1}}\right) + \mathbf{I_{-}R_2} - \mathbf{I_{+}R_S}\left(\mathbf{1} + \frac{\mathbf{R_2}}{\mathbf{R_1}}\right)$

   (c) $\mathbf{v_{OUT}} = \left(\mathbf{1} + \frac{\mathbf{R_2}}{\mathbf{R_1}}\right)\left(\mathbf{v_s} + \mathbf{V_{IO}} - \mathbf{I_{+}R_S}\right) + \mathbf{I_{-}R_2}$

   (d) R_s = 55 kohm

2. (a)

$$\mathbf{v_{OUT1}} = -\frac{\mathbf{R_2}}{\mathbf{R_1}}\mathbf{v_s} + \mathbf{V_{IO}}\left(\mathbf{1} + \frac{\mathbf{R_2}}{\mathbf{R_1}}\right)\#$$

$$\mathbf{v_{OUT2}} = \frac{\mathbf{R_4}}{\mathbf{R_3}}\left[\frac{\mathbf{R_2}}{\mathbf{R_1}}\mathbf{v_s} - \frac{\mathbf{R_2}}{\mathbf{R_1}}\mathbf{V_{IO}}\right] + \mathbf{V_{IO}}$$

   (b)The maximum permissible gain of the second stage is 26.

3. (a) f_{max} = 318 kHz
   (b) f ≤ 500 kHz

4. (a) V_{OUT} = 499.45 mV
   (b) R_s = 45.4 kohm

5. (a) v_{IN} = ±35 mV_p
   (b) f_{max} = 11.4 kHz

6. (a)
   (i) BWCL = 60 kHz
   (ii) Closed Loop Gain (600kHz) = 2.0 V/V

   (b) No distortion will occur

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TUTORIAL 3 (with answers at the back)

1. The op-amp in Fig 1 has a slew rate of 0.50V/μS. The amplifier must be capable of amplifying the following input signals:

   $v_1 = 0.01\sin(10^6 t)$
   $v_2 = 0.05\sin(350 \times 10^3 t)$
   $v_3 = 0.10\sin(200 \times 10^3 t)$
   $v_4 = 0.20\sin(50 \times 10^3 t)$

   a) Determine whether the output will be distorted due to slew-rate limitations on any input.
   b) If so, find a remedy (other than changing the input signals).

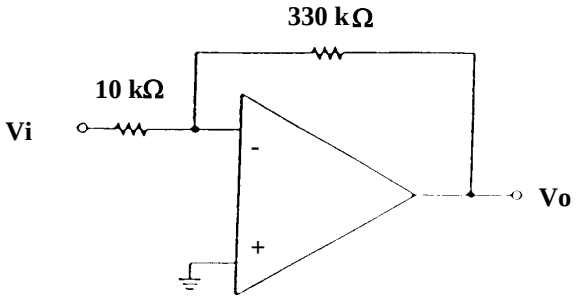


Fig. 1

2.a) What minimum SR is necessary for a unity-gain amplifier that must pass, without distortion, the input waveform shown in Fig 2.

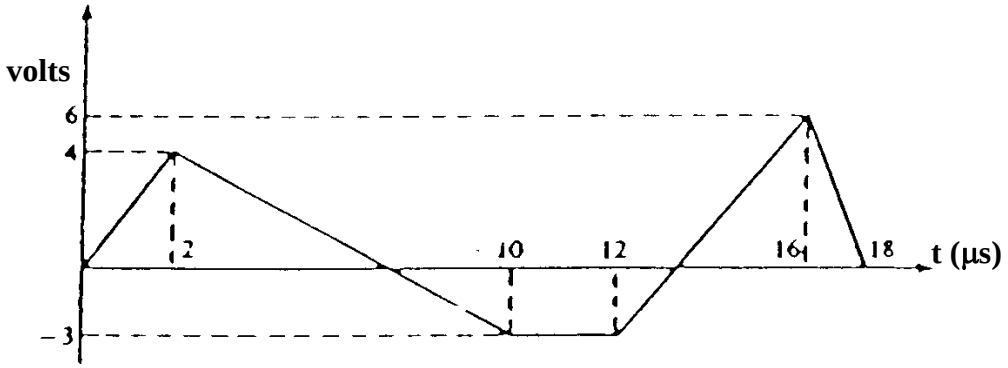


Fig. 2

2.b)Repeat (a), if the amplifier is in a noninverting configuration with R_I=50kΩ and R_f=100kΩ.

3. In a certain application, a signal source having 60kΩ of source resistance produces a 1-V-rms signal. The signal must be amplified to 2.5V rms and drive a 1kΩ load. Assuming that the phase of the load voltage is of no concern, design an op-amp circuit for the application.

4.a) Determine the empirical diode junction equation for a 1N4005 diode given the following voltage and current values:

V_{Dl} = 0.6V @ I_{Dl} = 2.3mA
V_{D2} = 0.8V @ I_{D2} = 245mA

4.b) Use the empirical diode junction equation, obtained in 4(a), to calculate the diode voltage V_D for a 1N4005 diode when the diode currents is

i) I_D = 20 mA
ii) I_D = 300 mA

4.c) A 1N4005 diode is used in the circuit shown in Fig. 3, determine the diode voltage and current by means of successive iteration method.

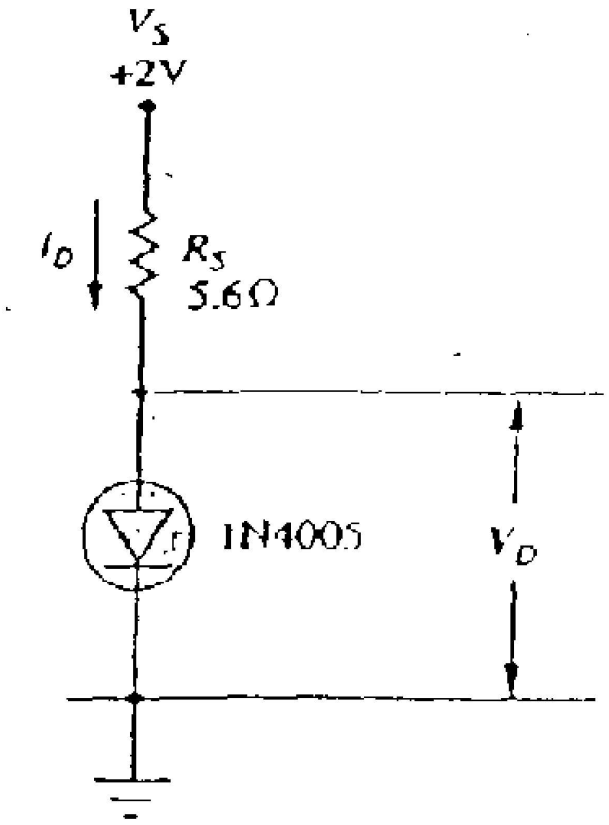


Fig. 3

5. Determine the AC component of the output voltage, v_{OUT}, for the circuit in Fig. 4 when V_{SDC}=5V DC.

The data sheet for the 1N4305 diode has the following voltage and current values:

$V_D = 0.50V$ at $I_D = 250\mu A$
$V_D = 0.70V$ at $I_D = 10mA$

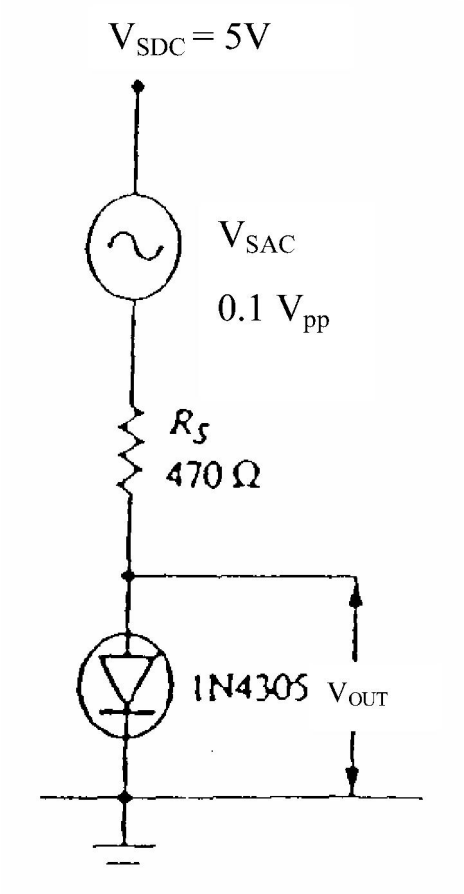


Fig. 4

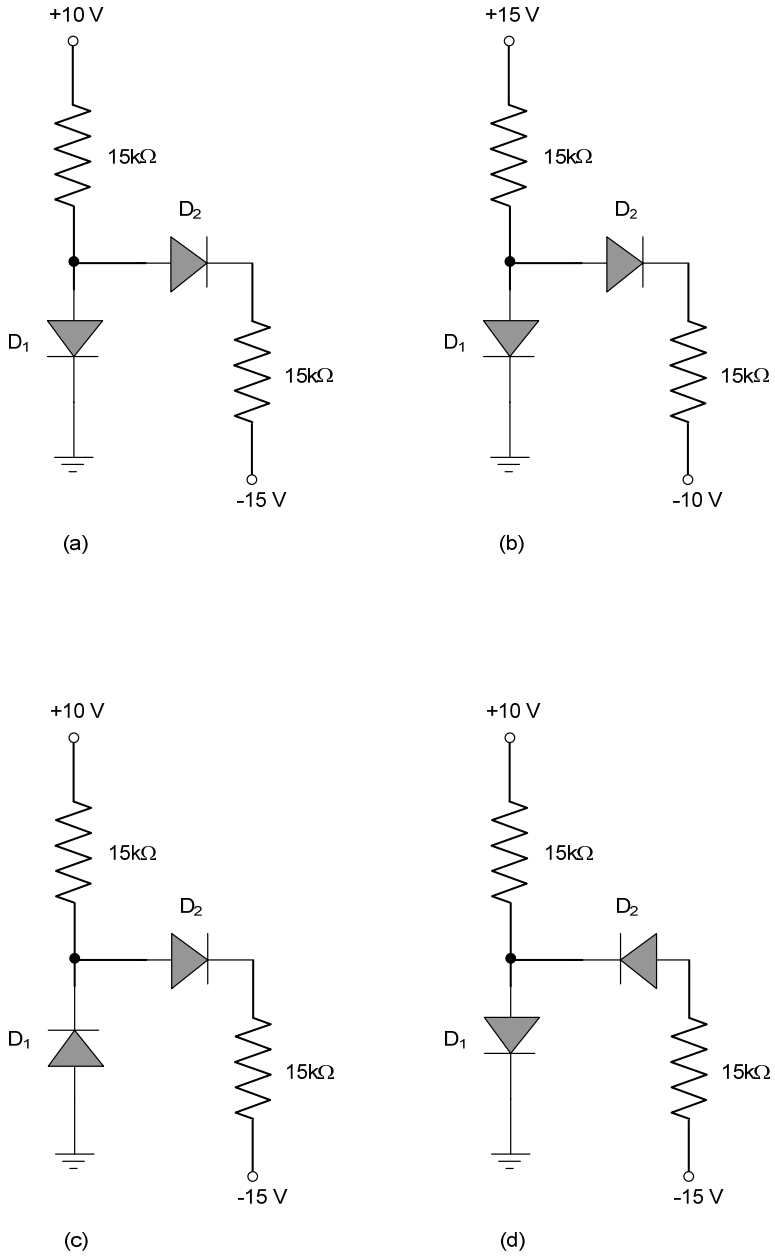


Fig. 5

6. Find the Q points of the diodes in the circuits of Fig. 5. For forward biased diode, the diode voltage is given as 0.75V.

Answers to Tutorial 3

1. (a) The output due to v_2 and v_3 will be distorted.

   (b) There are only two remedies:
   - (i) find an amp with greater SR, a SR of at least 0.66 V/μs
   - (ii) reduce the A_{CL} of the present amplifier to 25 V/V.

2. (a) The minimum SR is 3.0 V/μs
   (b) The $(SR)_{min}$ = 9 V/μs

3. Many right answers.

4. (a) The empirical junction equation for the IN4005 diode is

$$i_D \approx (1.90nA)e^{v_D/42.8mV}$$

$$\text{or} \quad v_D = (42.8mV)\ln\left(\frac{i_D}{1.90nA}\right)$$

   (b)
   - (i) For I_D=20 mA, V_D=0.692 V
   - (ii) For I_D=300 mA, V_D=0.808 V

   (c) V_D=0.794 V
   I_D = 215 mA

5. v_{OUT} = 1.24 mV_{PP}

6.

	D1	D2
(a)	-2.13V, 0A	0.75V, 0.808mA
(b)	0.75V, 0.283mA	0.75V, 0.667mA
(c)	0.75V, 0.183mA	0.75V, 0.9mA
(d)	0.75V, 0.617mA	-15.75V, 0A

EE2002 Tutorial 4

1. Plot the output, v_{out}, of the inverting integrator in Fig. 1(a) using an ideal op-amp if v_{in} is a ramp that levels off at the value $v_{in} = 4$ V after 20 mS as in Fig 1(b). For the inverting integrator, $R_1 = 5$ kΩ and $C = 1$ μF. Assume the initial output is zero and the power supply voltages for the op-amp are ±10V.

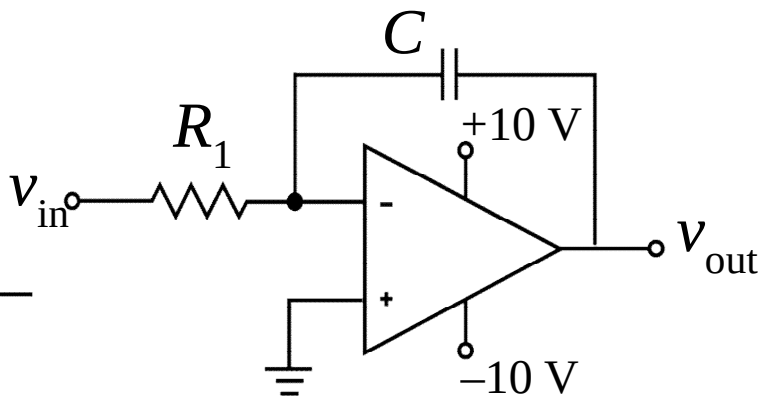


Fig.1 (a)

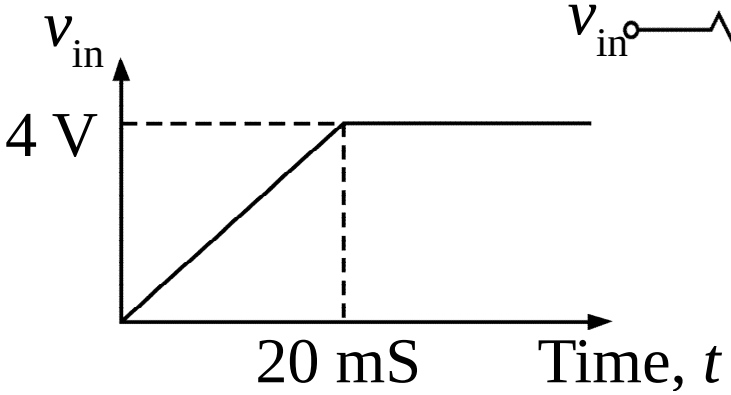


Fig.1 (b)

2. Find the closed loop Gain of the negative feedback opamp circuit, $A_{VCL} = v_o/v_i$ in Fig. 2.

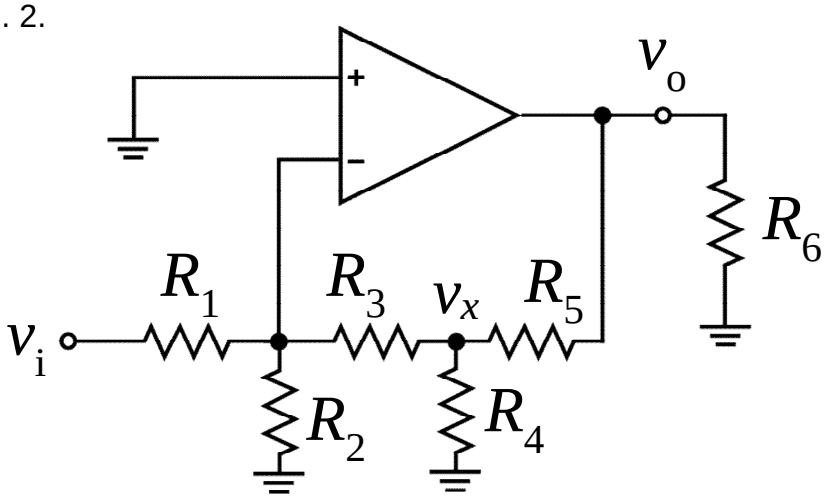


Fig. 2

3. For the circuit in Fig. 3 commonly known as an absolute value circuit, given that R_1, R_2 and R_3 are of the same value R, and R_4 and R_5 are of value 2R. Determine the peak magnitude of v_{out} and also sketch the expected waveform of v_{out} , given that the sinewave input voltage, v_{in} is $2V_{pk\text{-}pk}$ at an arbitrary frequency. The OpAmps are ideal and the diodes are treated in simple diode model with V_D = 0.7V.

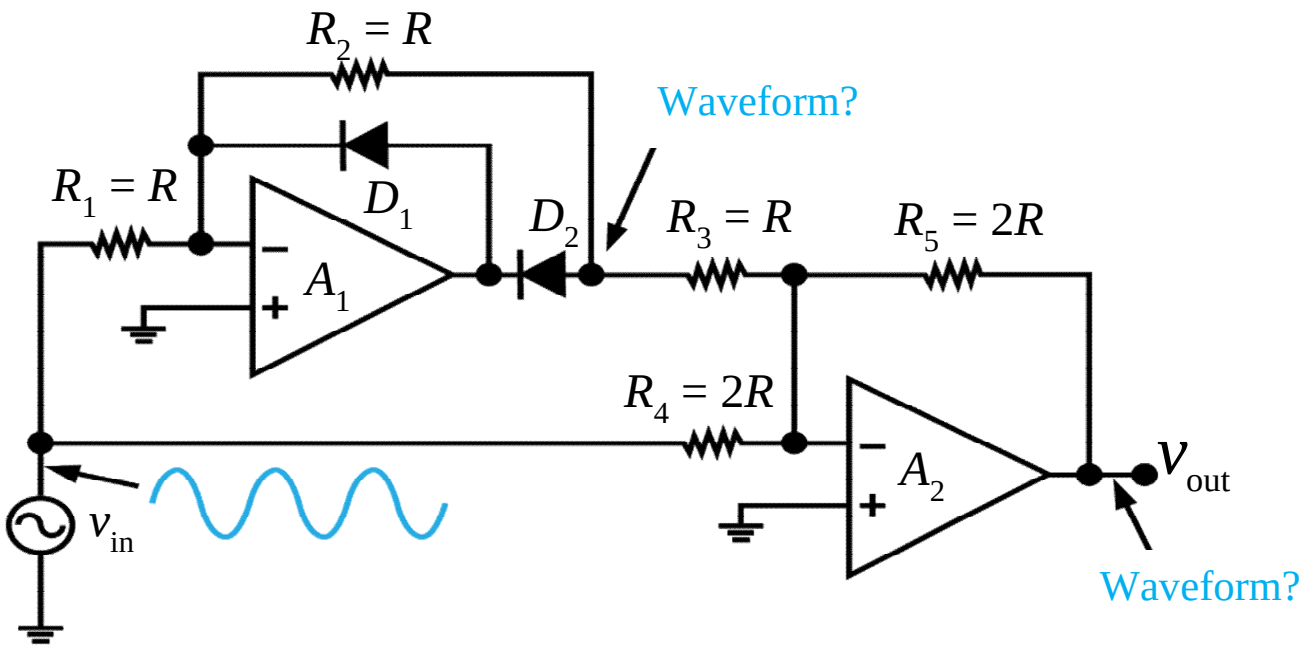
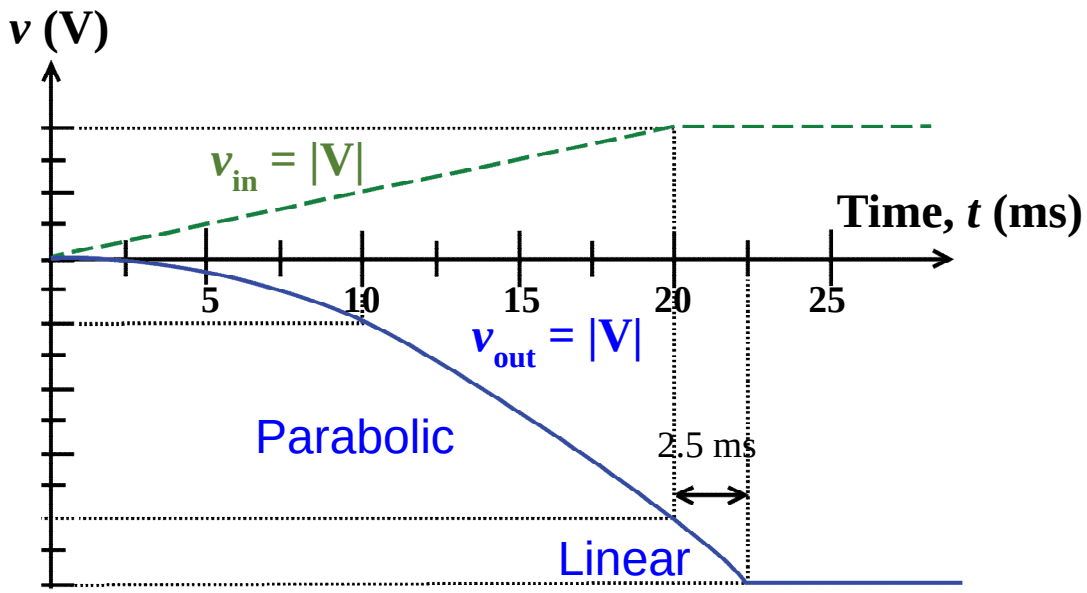


Fig. 3

Answers to Tutorial 4

1.



2.

$$\frac{v_o}{v_i} = -\frac{R_3}{R_1} \times \frac{R_5 + R_3 // R_4}{R_3 // R_4}$$

3.

$v_{out} = |v_{in}|$ = rippled DC output voltage with 1 V peak 

Nanyang Technological University
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E2002 Analog Electronics – Tutorial 5

1. Identify the region of operation for the following circuits. What is the V_C, V_E, I_B, I_C and I_E in each case. If active, what is the collector voltage? Assume $|V_{BE}| = 0.7$ V and $\beta = 100$.

   (Ans: (a) Saturation, $V_C = 1.4$ V, $V_E = 1.7$ V, $I_B = 0.29$ mA, $I_C = 0.14$ mA, $I_E = 0.43$ mA; (b) Active, $V_C = -13.68$ V, $V_E = -20.7$ V, $I_B = 18.4$ μA, $I_C = 1.86$ mA, $I_E = 1.86$ mA)

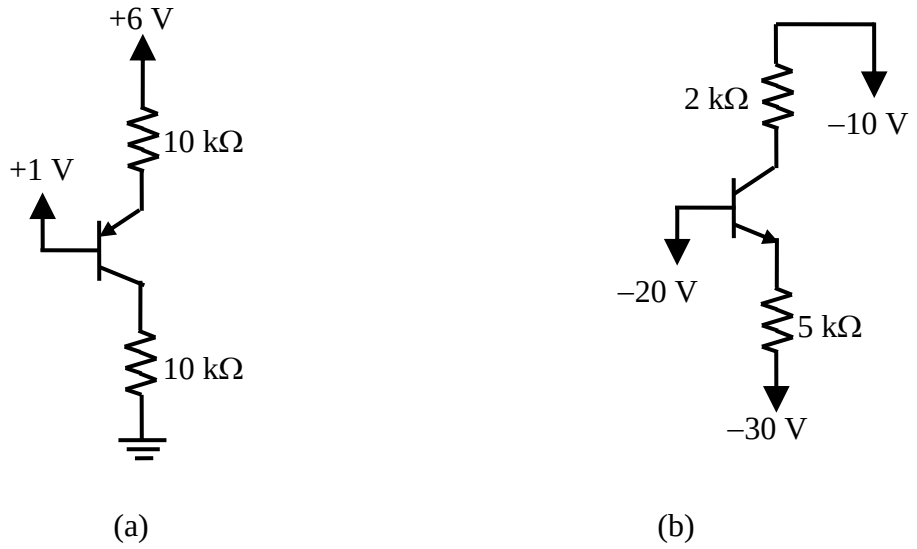

Figure 1

2. A common-emitter amplifier circuit is shown in Figure 2. Assume that the capacitors have infinite value, $\beta = 100$, $V_{CC} = V_{EE} = 15$ V, $R_I = 750$ Ω, $R_1 = R_2 = 200$ kΩ, $R_L = 100$ kΩ, $R_E = 280$ kΩ, and $R_C = 100$ kΩ. Calculate the DC operating point of the amplifier. (Ans: $I_C = 50$ μA, $V_{EC} = 10.86$ V).

   Calculate the dc power dissipation in each element in the amplifier circuit. Compare the result to the total power delivered by the sources.
   (Ans: $P_{R1} = 1.125$ mW, $P_{R2} = 1.125$ mW, $P_{Rc} = 0.25$ mW, $P_{RE} = 0.71$ mW, $P_{BJT} = 0.54$ mW. $P_S = 3.76$ mW)

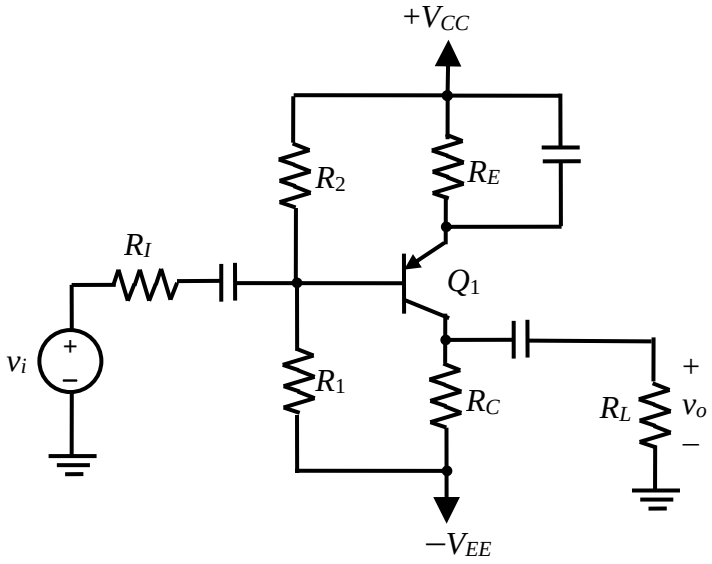

Figure 2

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1. The DC operating point of the common-emitter amplifier in Figure 1 has been calculated in Question 2 of Tutorial 5 to be I_C = 50 μA and V_{EC} =10.86 V. The pnp transistor Q_1 has β = 100 and V_A = 75V. Assume that the capacitors have infinite value, what are the voltage gain, input resistance, output resistance and current gain if $V_{CC} = V_{EE}$ = 15 V, R_I = 750 Ω, $R_1 = R_2$ = 200 kΩ, R_L = 100 kΩ, R_C = 100 kΩ, R_{E1} = 30 kΩ and R_{E2} = 250 kΩ.
(Ans: A_v = –1.62, R_{in} = 96.86 kΩ, $R_{out} \approx$ 100 kΩ, A_i = –1.58).

What is the amplitude of the largest ac signal that can appear at the output that satisfies the small-signal limit?
(Ans: 505.12 mV)

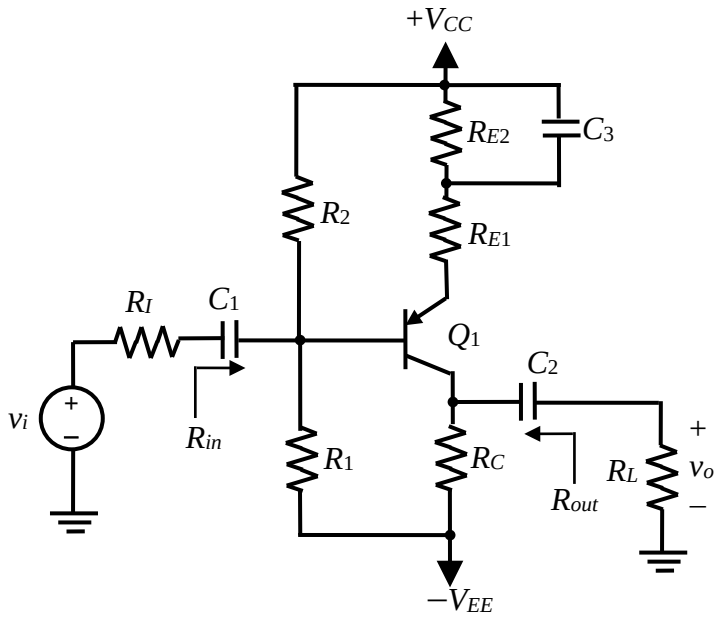

Figure 1

2. For the single stage amplifier in the Figure 2, find the mid-band voltage gain, input resistance and output resistance of this amplifier. What is the input signal range for this amplifier? Use β = 100, V_A = 70V for the BJT transistors.
(Ans: A_v = -8.94, R_{in} = 7.18 kΩ, R_{out} = 1.67 kΩ, $v_i \leq$ 11.96 mV)

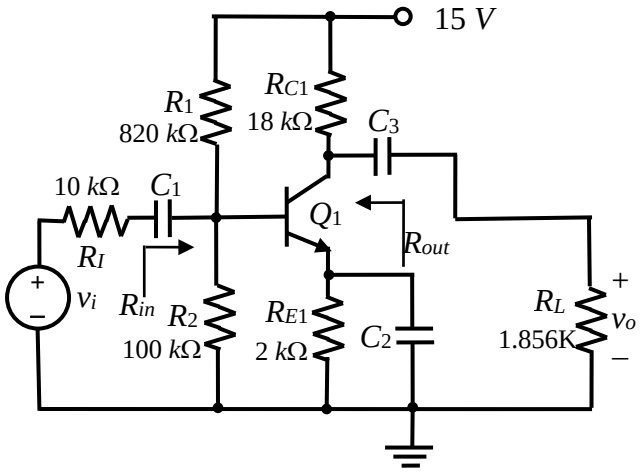
15 V
R1
820 kΩ
RC1
18 kΩ
C3
10 kΩ
C1
Q1
Rout
RI
vi
Rin
R2
100 kΩ
RE1
2 kΩ
C2
RL
1.856K
vo
+
–

Figure 2

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1. Check if the region of operation for the following circuits. Determine the operating point if it is in saturation. Assume $\lambda = 0$. $V_{TN} = 1$ V and $K_n = 0.5$ mA/V^{-1} for NMOS and $V_{TP} = -1$ V and $K_p = 250$ μA/V^{-1} for PMOS.

   (Ans: (a) Saturation region, $V_{DS} = 16.28$ V, $I_D = 3.43$ mA; (b) triode region)

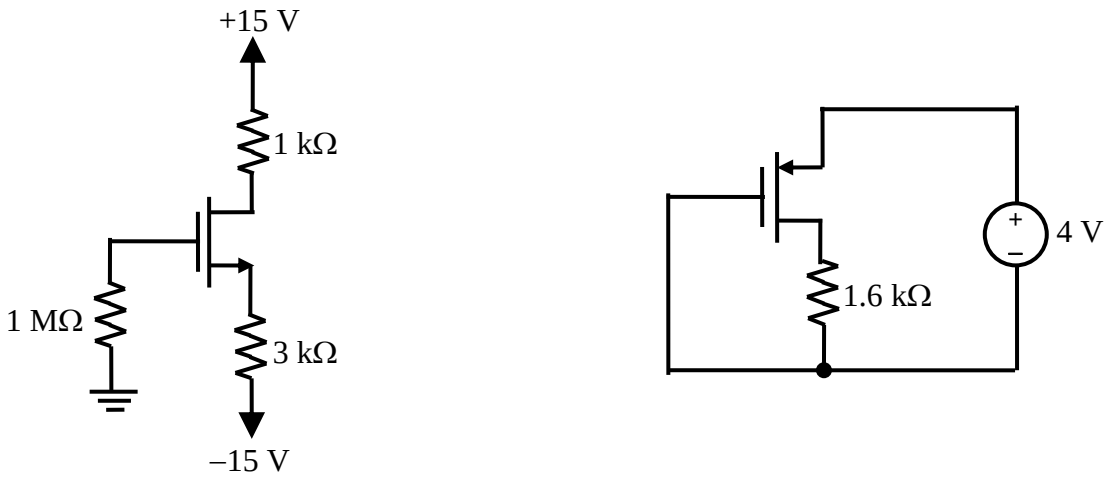

Figure 1

2. Draw the DC equivalent circuit for the common drain amplifier of Figure 2. Assume that the capacitors have infinite value, $K_n = 1$ mA/V^2, $V_{TN} = 1$V, $R_I = 100$ Ω, $R_1 = 1.2$ MΩ, $R_2 = 910$ kΩ, $R_L = 250$ Ω, $R_S = 3$ kΩ and $V_{DD} = 15$ V, calculate the DC operating point of the amplifier.
   (Ans: $I_D = 1.87$ *mA*, $V_{DS} = 9.39$ V).

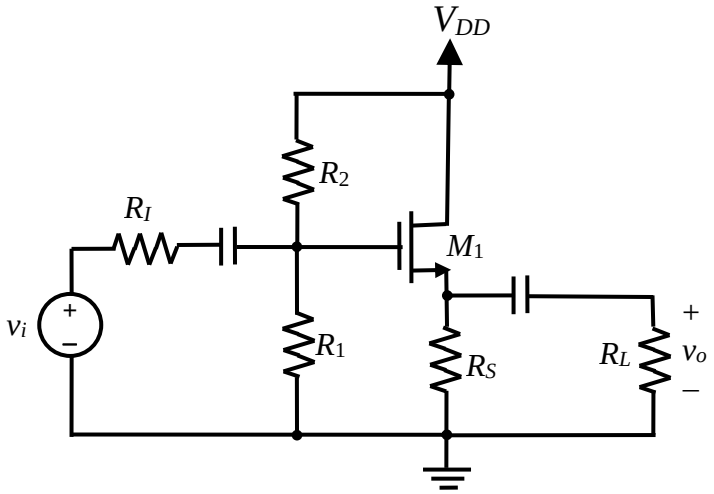

Figure 2

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E2002 Analog Electronics – Tutorial 8

1. The DC operating point of the common-drain amplifier in Figure 1 has been calculated in Question 2 of Tutorial 7 to be $I_D = 1.87\ mA$ and $V_{DS} = 9.39$ V. The *n*-MOS transistor M_1 has $K_n = 1$ mA/V^2, $V_{TN} = 1$ V and $\lambda = 0.02$ V^{-1}. Assume that the capacitors have infinite value, $R_I = 100\ \Omega$, $R_1 = 1.2$ MΩ, $R_2 = 910$ kΩ, $R_S = 3$ kΩ, $R_L = 250\ \Omega$ and $V_{DD} = 15$ V, calculate the voltage gain, input resistance and output resistance of the amplifier.
(Ans: $A_v = 0.31$, $R_{in} = 517.54$ kΩ, $R_{out} = 434.6\ \Omega$)

What is the maximum input signal amplitude for small signal operation?
(Ans: 556.52 mV)

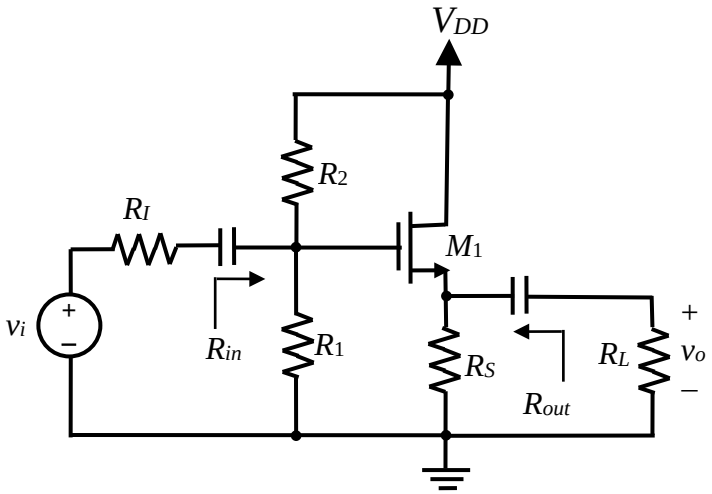

Figure 1

2. What are the voltage gain, input resistance and output resistance for the amplifier in Figure 2. if $R_I = 250\Omega$, $R_S = 68$ kΩ, $R_L = 200$ kΩ, $R_D = 43$ kΩ and $V_{DD} = V_{SS} = 15$ V? What is the maximum input signal for the amplifier that satisfies the small-signal limit? Use $K_p = 200\ \mu$A/V^2 and $V_{TP} = -1$V for your calculation.
(Ans: $A_v = 8.98$, $R_{in} = 3.47$ kΩ, $R_{out} = 43$ kΩ, $v_i \le 0.292$ V)

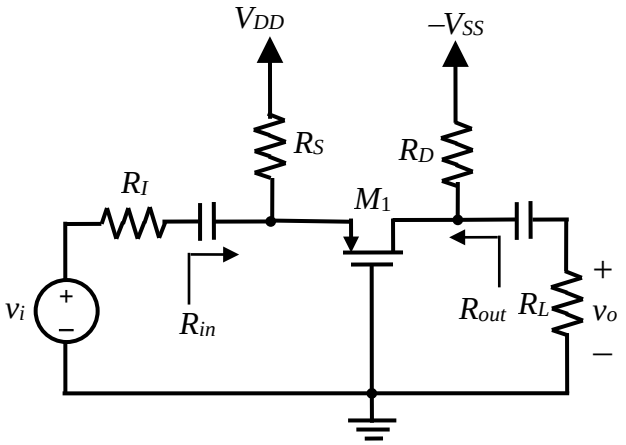

Figure 2

3. The gate resistor R_G in Figure 3 is said to be "bootstrapped" by the action of the source follower.

   a. Assume that the MOSFET is operating with g_m = 3.54 mS and r_o can be neglected. Draw the small signal model and find the voltage gain, input resistance and output resistance for the amplifier if R_G = 1 MΩ, R_S = 2 kΩ, R_L = 100 kΩ and $V_{DD} = V_{SS}$ = 10 V.
   (Ans: A_v = 0.874, R_{in} = 7.94 MΩ, R_{out} = 247 Ω)

   b. What would R_{in} be if A_v were exactly +1?
   (Ans: ∞)

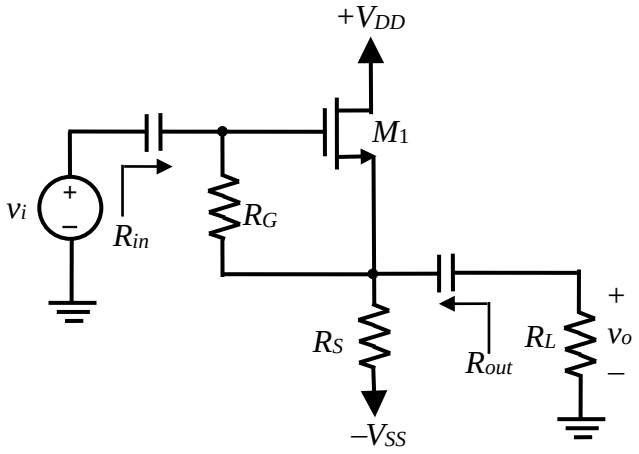

Figure 3

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Tutorial 9

1. An amplifier has a transfer function:

$$T(s)=\frac{10^{12}s^2}{(s+10)(s+10^3)(s+10^6)}$$

Sketch the Bode magnitude plot for the gain response. Use the plot to estimate the values for the amplifier gain at 10^3 rad/s and 10^6 rad/s respectively. What should be the actual values of the gain at these frequencies? Determine the bandwidth of the response.

(Ans: 120 dB, 120 dB, 117 dB, 0.999x10^6 rad/s)

2. Using the following catalog of filters at your disposal:

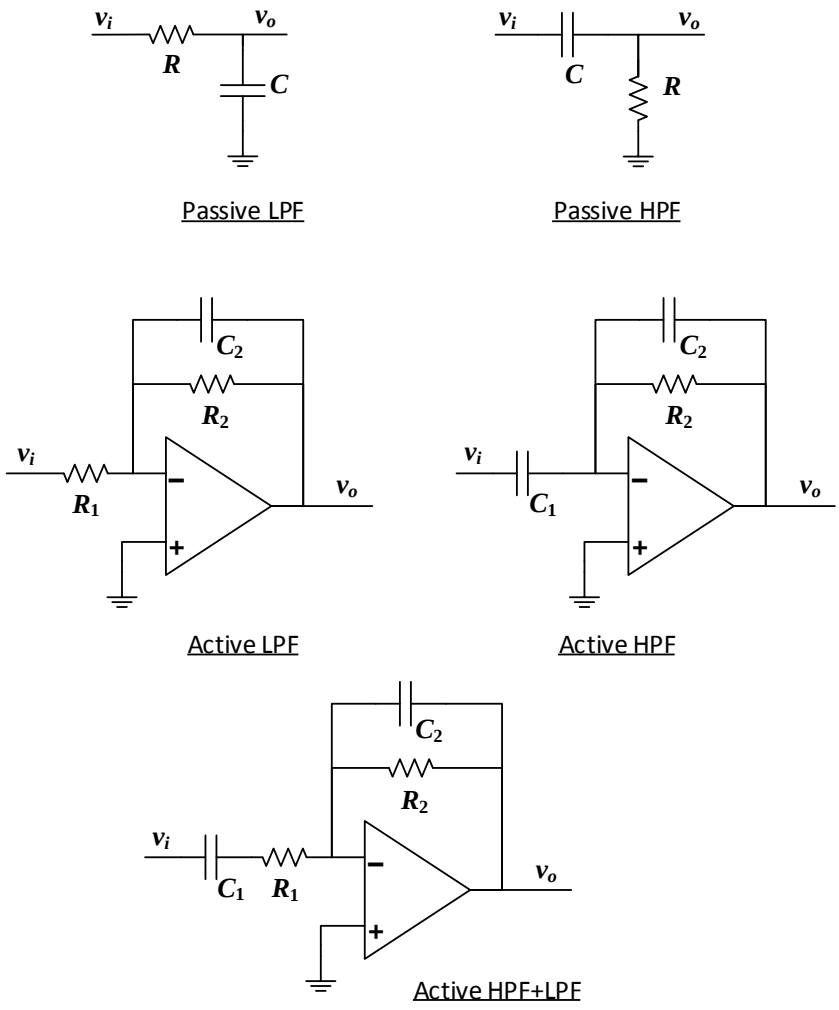
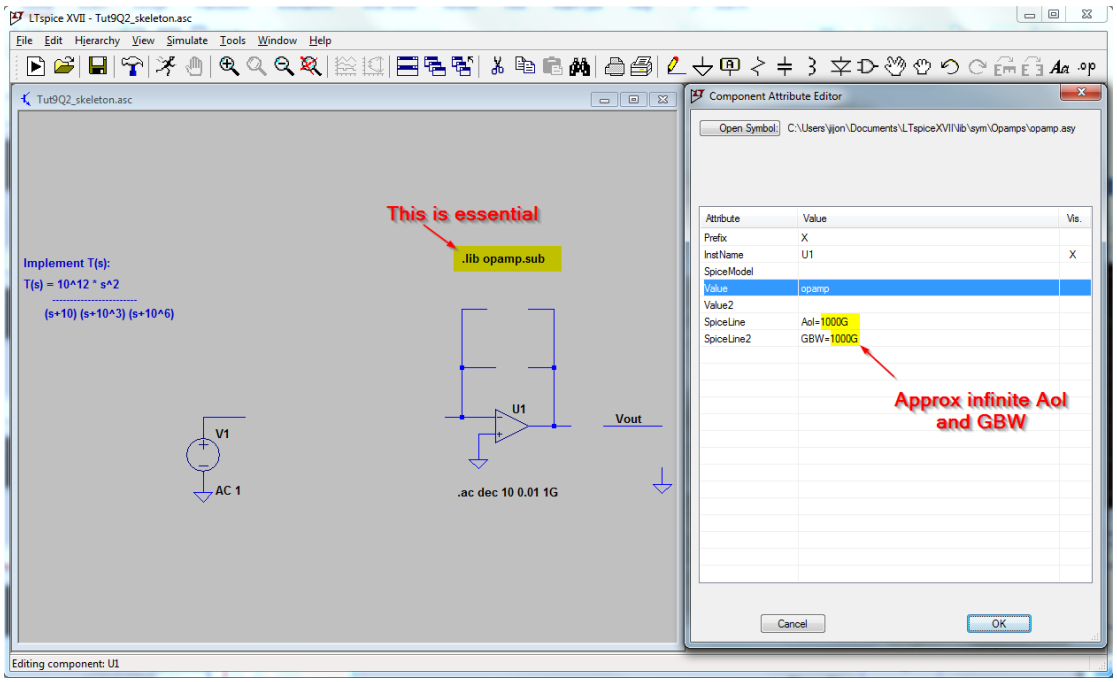


Figure 1

Design a filter cascade (e.g. Active HPF + Active LPF + Passive HPF) that will implement the transfer function *T(s)* in Question 1.

Use resistance values from 1Ω - 1GΩ, and capacitance values from 1pF – 1mF.

Run a .AC simulation in LTspice using an ideal Opamp (set Aol=GBW=1000G), to verify if the Bode plot matches with your answer to Question 1.



(Many correct answers)

In practice, why might a cascade of two (Active HPF + Active LPF) filters be preferred over a single (Active HPF+LPF) filter?

(Ans: a single Opamp in this case will require larger GBW product)

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Tutorial 10

1. In the AC model of the common-base circuit shown in Figure 1, the transistor Q_1 has $\beta = 100$, $V_A = \infty$, $C_\mu = 1$pF and $C_\pi = 10$pF. AC coupling capacitors $C_{c1} = C_{c2} = 1$uF. Assume $V_T = 25$ mV and DC collector current $I_C = 0.5$ mA. Using the OCTC and SCTC methods, determine the upper and lower 3-dB frequency of the amplifier, ω_H and ω_L respectively, and hence the amplifier bandwidth.

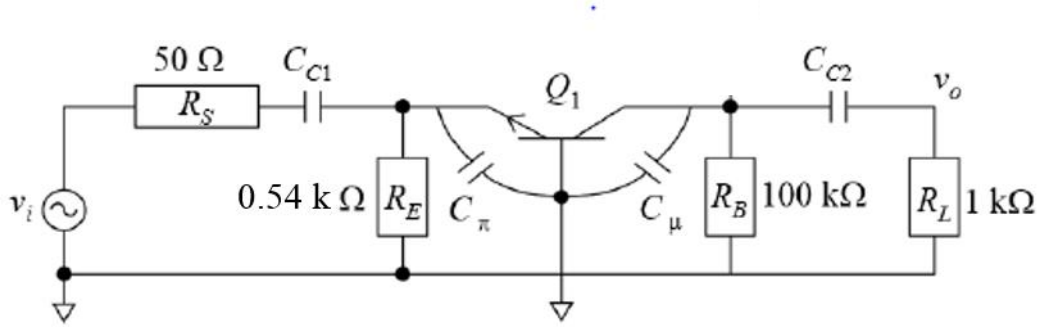

Figure 1

(Ans: ω_H=813 Mrad/s; ω_L=10.5 krad/s; BW=$\omega_H-\omega_L$ =813 Mrad/s)

2. Using the short-circuit time constant method, determine the lower -3dB frequency (ω_L) for the amplifier circuit shown in Figure 2. M2 is a PMOS while M1 is a NMOS. A signal source v_s with a series resistance R_S =1 MΩ is connected to the input at G through a coupling capacitor C_1 = 1μF, while a load resistor R_L = 10 kΩ is connected to the output at D through a coupling capacitor C_2 = 1μF. The resistance R_1 = 5 MΩ. For the transistors M_1 and M_2, $\mu_n C_{ox1}(W_1/L_1) = \mu_p C_{ox2}(W_2/L_2) = 50\ \mu A/V^2$, $|V_{TP}| = V_{TN} = 2V$, and $\lambda = 0.005\ V^{-1}$.

Ans: 34.9 rad/s

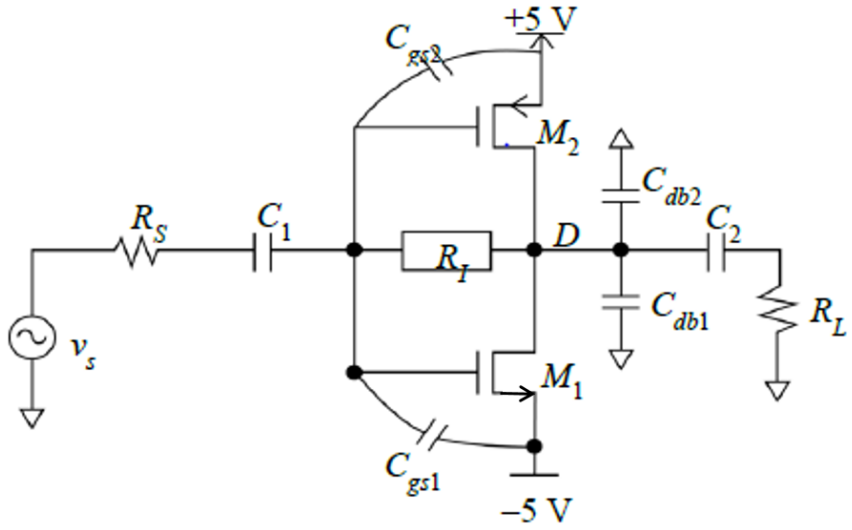

Figure 2