NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2021-2022

EE3019 – INTEGRATED ELECTRONCIS

November / December 2021 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 5 pages.
2. Answer all 4 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.
6. A List of Formulae is provided in Appendix A on page 5.

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1. The parameters of the pMOS and nMOS transistors are given below:

pMOS	V_{tp} = –0.6 V	$\mu_p C_{ox}$ = 100 μA/V^2	$(W/L)_p$ = 2
nMOS	V_{tn} = 0.6 V	$\mu_n C_{ox}$ = 200 μA/V^2	$(W/L)_n$ = 2

V_{DD} = 1.8 V

(a) Determine V_{IH}, V_{IL}, and the noise margin of a 2-input NAND gate and an inverter using the equivalent device sizes of the best case. Assume that the logic gate outputs are 1.71 V for V_{IL} and 0.09 for V_{IH}, respectively. Explain how to make the noise margin of the 2-input NAND gate equal to that of the inverter.

(10 Marks)

(b) A 2-input NOR gate is designed using the given parameters above. The 2-input NOR gate is driving a capacitive load. The capacitance of the load is 1pF when the NOR gate input is '0'. The capacitance decreases by 20% when the NOR gate input is '1'. Determine the propagation delays (τ_{PHL} and τ_{PLH}) of the 2-input NOR gate using the best case.

(10 Marks)

Note: Question No. 1 continues on page 2.

(c) An inverter, a 2-input NAND gate, and a 2-input NOR gate are designed using the given parameters above. Compare the switching threshold voltages of the logic gates using the best case and explain how to make the switching threshold voltages of the logic gates identical.

(5 Marks)

2 (a) Figure 1 shows a schematic diagram of the 8-transistor clocked SR latch. The device parameters of the pMOS and nMOS transistors for M_1, M_2, M_3, and M_4 are given below:

pMOS	Vtp = –0.6 V	$\mu pCox$ = 100 μA/V²	$(W/L)p$ = 4
nMOS	Vtn = 0.6 V	$\mu nCox$ = 250 μA/V²	$(W/L)n$ = 2
		V_{DD} = 1.8 V	

For reliable set and reset operations, the storage nodes need to be pulled down to the switching threshold of the cross coupled inverters formed by M1, M2, M3, and M4. Determine the minimum size (W/L) of M5, M6, M7, and M8 for reliable set and reset operations.

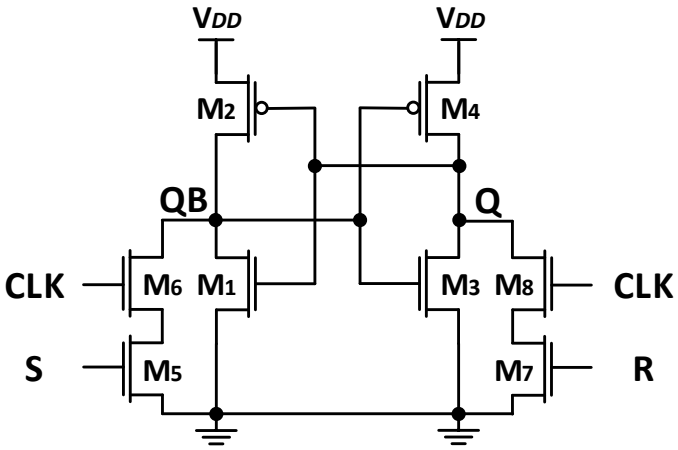

Figure 1

(10 Marks)

(b) The clocked SR latch designed in Question 2(a) needs to be redesigned to give more reliable set and reset operations and also to have a smaller circuit. Explain how to redesign the clocked SR latch to achieve the above goals.

(5 Marks)

Note: Question No. 2 continues on page 3.

(c) Using the amplifier shown in Figure 2 where R_S = 1kΩ, R_1 = R_2 = R_3 = 5kΩ, and R_L = 10kΩ, determine the closed loop gain of the amplifier when the open loop gain (A) of the amplifier is 1000.

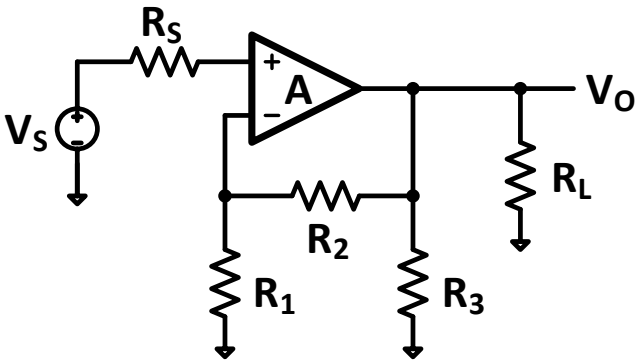

Figure 2

(5 Marks)

(d) Determine the change in the open loop gain (A) that will lead to 0.02% change in the closed loop gain.

(5 Marks)

3. (a) Draw the schematic diagram for a voltage regulator with a bipolar junction transistor, a Zener diode, and a resistor.

(7 Marks)

(b) Use the transistor with β = 100 and V_{BE} = 0.7 V and the Zener diode with breakdown current I_{zk} = 20 mA to design the voltage regulator to provide 10 V-1 A regulated power supply to a load from the unregulated input voltage between 15 V and 18 V.

(12 Marks)

(c) Find the required minimum power ratings of the transistor and the Zener diode.

(6 Marks)

4. (a) Draw the schematic diagram for the basic switched-capacitor integrator with two switches, two capacitors, and one operational amplifier. State the requirements for the clock signals applied to the two switches.

(7 Marks)

Note: Question No. 4 continues on page 4.

(b) Determine the capacitance ratio of the two capacitors so that the output voltage changes one quarter of the input voltage once at a time.

(9 Marks)

(c) Assume that the initial output voltage is 0 V, sketch the time domain output voltage waveform for a constant input voltage of 1 V with reference to the clock signals.

(9 Marks)

APPENDIX A

$$V_{IH} = \frac{V_{DD} + V_{tp} + k_R(2V_{out} + V_{tn})}{1 + k_R}$$

$$V_{IL} = \frac{2V_{out} + V_{tp} - V_{DD} + k_R V_{tn}}{1 + k_R}$$

$$V_{th} = \frac{V_{tn} + \sqrt{\frac{1}{k_R}}(V_{DD} + V_{tp})}{1 + \sqrt{\frac{1}{k_R}}}$$

$$v_t = V_{to} + \gamma(\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f})$$

END OF PAPER