

**NANYANG TECHNOLOGICAL UNIVERSITY****SEMESTER 1 EXAMINATION 2020-2021****EE3019 - INTEGRATED ELECTRONICS**

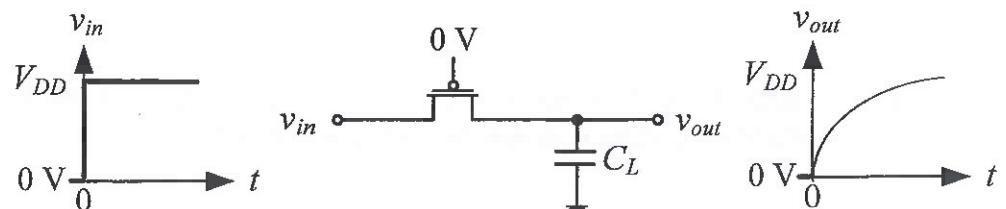
November / December 2020

Time Allowed: 2 hours

**INSTRUCTIONS**

1. This paper contains 4 questions and comprises 7 pages.
  2. Answer all 4 questions.
  3. All questions carry equal marks.
  4. This is a closed book examination.
  5. Unless specifically stated, all symbols have their usual meanings.
  6. A list of Formulae is provided in the Appendix A on page 7.
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1. (a) The pMOS pass-transistor circuit is depicted in Figure 1. Assume that  $\mu_p C_{ox} = -50 \mu\text{A/V}^2$ ,  $\left(\frac{W}{L}\right)_p = \frac{56\text{nm}}{28\text{nm}}$ ,  $V_{DD} = 1.2 \text{ V}$ ,  $V_{tp} = -0.47 \text{ V}$ ,  $C_L = 25 \text{ fF}$  and  $v_{out}$  changes from  $0 \text{ V}$  to  $1.2 \text{ V}$ .
  - (i) Identify the regions of operation and determine the drain current,  $i_{DP}$ , of the pMOS transistor when  $v_{out} = 0 \text{ V}$  and  $v_{out} = 0.6 \text{ V}$ .
  - (ii) Determine the propagation delay,  $t_{PLH}$ , of the circuit.

**Figure 1**

(11 Marks)

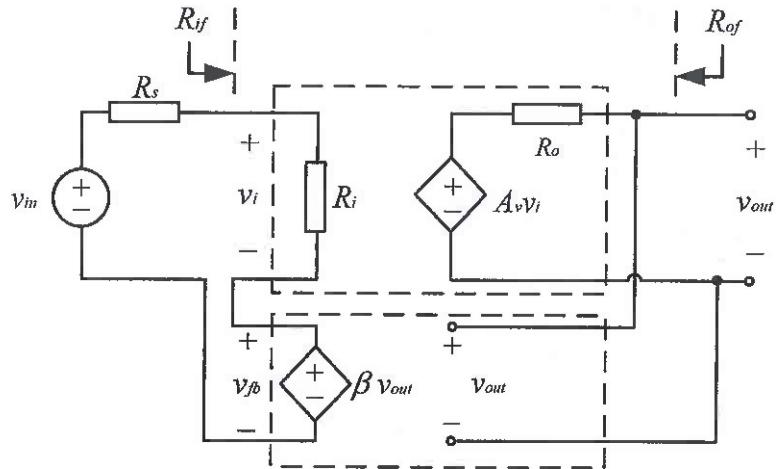
Note: Question No. 1 continues on page 2.

2. (a) Draw a circuit schematic of a 2-nMOS transistor with 2-polysilicon resistor SRAM cell and a 4-transistor CMOS SRAM cell. Briefly compare their circuit area, power dissipation and operating speed.

(10 Marks)

- (b) The equivalent circuit of a feedback amplifier is depicted in Figure 3. Assume that  $R_i = 5 \text{ k}\Omega$ ,  $R_o = 4 \text{ k}\Omega$ ,  $R_s$  is negligible,  $v_{in} = 80 \text{ mV}$ ,  $v_{fb} = 99 \text{ mV}$  and  $v_{out} = 4 \text{ V}$ .

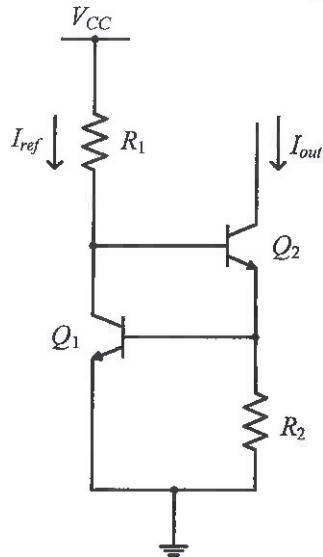
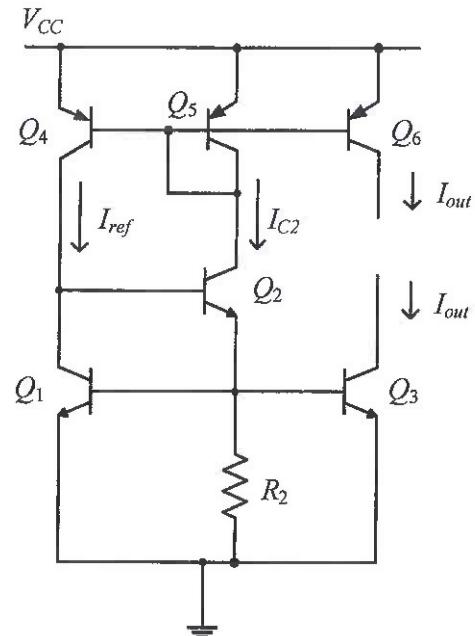
- (i) Identify the feedback configuration and determine the feedback factor,  $\beta$ .
- (ii) Determine the open-loop gain and closed-loop gain of the amplifier.
- (iii) Determine the input impedance,  $R_{if}$ , and the output impedance,  $R_{of}$ .

**Figure 3**

(12 Marks)

- (c) Explain why the open-loop gain of the negative feedback amplifier should be large.

(3 Marks)

**Figure 4(a)****Figure 4(b)**

4. A simple current mirror and a two-stage op-amp are depicted in Figures 5(a) and 5(b), respectively, on page 6.

- (a) State two important parameters of the simple current mirror.

(3 Marks)

- (b) (i) Explain why it is inappropriate to design the differential input stage of the op-amp with load resistors,  $R_3$  and  $R_4$ .

- (ii) Replace the load resistors,  $R_3$  and  $R_4$ , with the simple current mirror. Draw the schematic of the redesigned input stage of the op-amp.

(8 Marks)

- (c) Assume the following for the redesigned op-amp in part (b)(ii):

- Three poles are located at 100 kHz, 10 MHz and 100 MHz;
- DC open-loop voltage gain of the op amp is  $10^4$ ; and

- The parameters of the transistors are:

$$|V_t| = 0.8 \text{ V}, \mu_n C_{ox} = 30 \mu\text{A/V}^2, \mu_p C_{ox} = 20 \mu\text{A/V}^2, \text{ and } |V_A| = 50 \text{ V}.$$

Note: Question No. 4 continues on page 6.

**Appendix A**List of Formulae

$$V = I Z$$

$$P = I V$$

$$Z_L = j\omega L$$

$$Z_C = \frac{1}{j\omega C}$$

$$\sum_{m=1}^M v_m = 0$$

$$\sum_{n=1}^N i_n = 0$$

$$v = L \frac{di}{dt}$$

$$i = C \frac{dv}{dt}$$

$$S = V I^*$$

$$i_D = I_S \left[ \exp \left( \frac{v_D}{nV_T} \right) - 1 \right]$$

$$V_T = \frac{kT}{q}$$

$$i_C \approx I_S \left[ \exp \left( \frac{v_{BE}}{V_T} \right) \right]$$

$$i_E = i_C + i_B$$

$$\beta = \frac{i_C}{i_B}$$

$$\alpha = \frac{\beta}{1+\beta}$$

$$A + B + C = \overline{\overline{A} \ \overline{B} \ \overline{C}}$$

$$ABC = \overline{\overline{A} + \overline{B} + \overline{C}}$$

$$\tau_p = \frac{C_{load} \times \Delta V}{I_{avg}}$$

$$i_{Dn(LIN)} = (\mu_n C_{ox}) \left( \frac{W}{L} \right) ((v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2)$$

$$A_f = \frac{A}{1+A\beta}$$

$$i_{Dn(SAT)} = \frac{1}{2} (\mu_n C_{ox}) \left( \frac{W}{L} \right) (v_{GS} - V_t)^2$$

$$f = \frac{1}{2n \tau_p}$$

$$A(s) = A_m F_H(s) = \frac{A_m}{\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{s}{\omega_{P2}}\right)}$$

$$V_o = A_1 A_2 (V_i - \beta V_o) + A_1 V_n$$

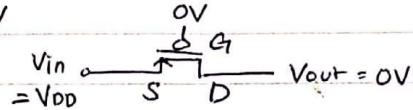
$$g_m = 2 \frac{I_D}{(V_{GS} - V_t)}$$

$$r_o = \frac{V_A}{I_D}$$

END OF PAPER

1.) a.)  $\mu_p C_{ox} = -50 \mu A/V^2$ ,  $(\frac{W}{L})_p = \frac{56 \text{ nm}}{28 \text{ nm}}$ ,  $V_{DD} = 1.2 \text{ V}$ ,  $V_{tp} = -0.47 \text{ V}$ ,  $C_L = 25 \text{ fF}$

i.) when  $V_{out} = 0 \text{ V}$



$$|V_{GSp}| = V_{DD} - 0 = V_{DD} = 1.2 \text{ V}$$

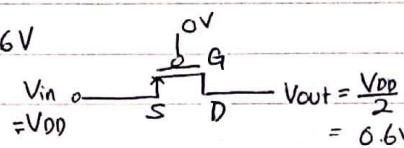
$$|V_{DSp}| = V_{DD} - 0 = V_{DD} = 1.2 \text{ V}$$

$$|V_{nspl}| \geq |V_{GSp}| - |V_{tp}| \rightarrow 1.2 \geq 0.73$$

\* current is flowing from Vin to Vout since Vin @ t=0 is VDD.

$\therefore$  Saturation Region //

When  $V_{out} = 0.6 \text{ V}$



$$|V_{GSp}| = V_{DD} - 0 = V_{DD} = 1.2 \text{ V}$$

$$|V_{DSp}| = V_{DD} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} = 0.6 \text{ V}$$

$$|V_{nspl}| < |V_{GSp}| - |V_{tp}| \rightarrow 0.6 < 0.73$$

$\therefore$  Triode/Linear/Ohmic Region //

ii.)  $T_{PLH} = \frac{C_L (V_{50\% VOL})}{I_{avg} |LH|}$

$$\text{where } I_{avg} = \frac{1}{2}(I_{50\%} + I_{OL})$$

$$I_{OL} (\text{Sat}) = \frac{1}{2} (\mu_p C_{ox}) \left( \frac{W}{L} \right)_p (|V_{GSp}| - |V_{tp}|)^2 = \frac{1}{2} (50) \left( \frac{56}{28} \right) (0.73)^2 = 26.645 \mu \text{A}$$

$$I_{50\%} (\text{Linear}) = (\mu_p C_{ox}) \left( \frac{W}{L} \right)_p ((|V_{GSp}| - |V_{tp}|) |V_{DSp}| - \frac{1}{2} |V_{DSp}|^2)$$

$$= 50 \left( \frac{56}{28} \right) ((0.73)(0.6) - \frac{1}{2}(0.6)^2) = 25.8 \mu \text{A}$$

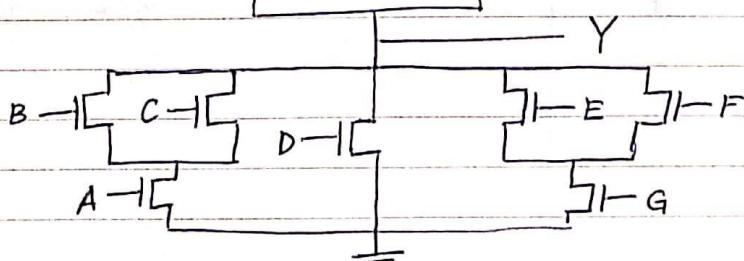
$$I_{avg} = \frac{1}{2} (25.8 \mu + 26.645 \mu) = 26.223 \mu \text{A}$$

$$T_{PLH} = \frac{25f(0.6-0)}{26.223\mu} = 5.72 \times 10^{-10} = 0.572 \text{ ns}$$

b.) i.) PDN :

Pull-up network (PUN)

$$Y = A(B+C) + D + (E+F)G$$



ii.)  $(\frac{W}{L}) = \frac{2}{1}$ ,  $L = 28 \text{ nm}$  For worst case:

$$\frac{1}{(\frac{W}{L})_{ABC}} + \frac{1}{(\frac{W}{L})_D} + \frac{1}{(\frac{W}{L})_{EFG}} = (\frac{W}{L}) = \frac{2}{1} \rightarrow \frac{1}{\frac{L}{3W}} = \frac{2}{1} \rightarrow (\frac{W}{L}) = \frac{6}{1} = (\frac{W}{L})_{ABC} = (\frac{W}{L})_{EFG}$$

$$(\frac{W}{L})_A + (\frac{W}{L})_{BC} = (\frac{W}{L})_{ABC} = \frac{6}{1} \rightarrow (\frac{W}{L})_A = \frac{3}{1} = (\frac{W}{L})_{BC}$$

$$\frac{1}{(\frac{W}{L})_B} + \frac{1}{(\frac{W}{L})_C} = (\frac{W}{L})_{BC} = \frac{3}{1} \rightarrow \frac{W}{2L} = \frac{3}{1} \rightarrow (\frac{W}{L})_B = (\frac{W}{L})_C = 6$$

$$\left(\frac{W}{L}\right)_{EF} + \left(\frac{W}{L}\right)_G = \left(\frac{W}{L}\right)_{EFG} = \frac{6}{1} \rightarrow \frac{2W}{L} = \frac{6}{1} \rightarrow \left(\frac{W}{L}\right)_G = \frac{3}{1} = \left(\frac{W}{L}\right)_{EF}$$

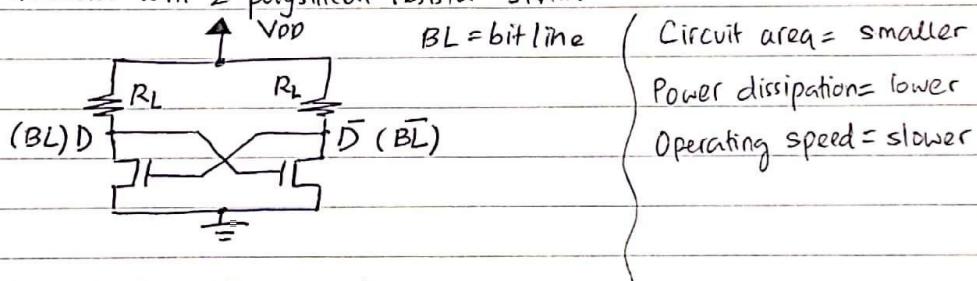
$$\frac{1}{\left(\frac{W}{L}\right)_E} + \frac{1}{\left(\frac{W}{L}\right)_F} = \left(\frac{W}{L}\right)_{EF} = \frac{3}{1} \rightarrow \frac{W}{2L} = \frac{3}{1} \rightarrow \left(\frac{W}{L}\right)_E = \left(\frac{W}{L}\right)_F = 6$$

$$\therefore \left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_G = \frac{3}{1}, \quad \left(\frac{W}{L}\right)_B = \left(\frac{W}{L}\right)_C = \left(\frac{W}{L}\right)_D = \left(\frac{W}{L}\right)_E = \left(\frac{W}{L}\right)_F = \frac{6}{1}$$

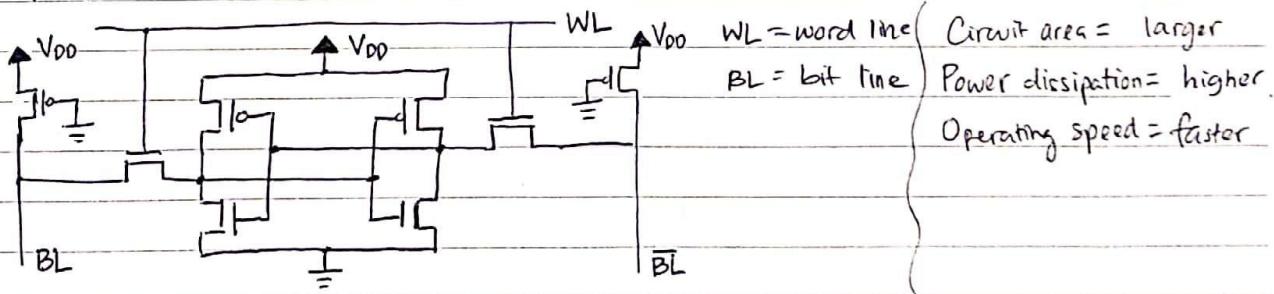
c.) Pass-transistor circuit without resorting to a transmission gate circuit:

- Making sure gate voltage is supplied correctly ( $V_{GP} = 0V$ ,  $V_{GN} = V_{DD}$ ) &  $V_{IN}$  not reaching  $0V$  since PTL: , there is no pMOS present for current to flow when nMOS is cut off, vice versa (not sure)

2.) a.) 2nMOS transistor with 2-polysilicon resistor SRAM



4-transistor CMOS SRAM cell



b.) i) feedback configuration: Series-Shunt (Voltage mixing - Voltage sampling)

$$V_{fb} = \beta V_o \rightarrow \beta = \frac{V_{fb}}{V_o} = \frac{99m}{4} = \underline{\underline{24.75m}}$$

ii.) open-loop gain ( $A_v$ )      ( $R_s$  is negligible)

$$\text{ideally, } V_o = A_v V_i \rightarrow A_v = \frac{V_o}{V_i}, \text{ where } V_{in} = V_i + V_f \rightarrow V_i = V_{in} - V_f = -19m$$

• closed-loop gain ( $A_f$ )

$$A_f = \frac{A_v}{1 + A_v \beta} = \underline{\underline{50}}$$

$$A_v = \frac{4}{-19m} = \underline{\underline{-210.526}}$$

$$\text{iii.) } R_{if} = R_i(1 + A_v \beta) = 5k(1 + (-210.526)(24.75m)) = \underline{\underline{-21k\Omega}}$$

$$R_{of} = \frac{R_o}{1 + A_v \beta} = \frac{4k}{1 + (-210.526)(24.75m)} = \underline{\underline{-950\Omega}}$$

\* I am not sure how  $V_{fb}$  is larger than  $V_{in}$ , making  $A_v$  negative. I just used equations that is derived in the Lecture Notes (Feedback circuit)

c.) An ideal op-amp (feedback amplifier) is infinite. When it's not infinite, there's some small amount of current that flows into the input terminals, & there's a small voltage difference between inverting (-) & non-inverting inputs.

•  $A_f = \frac{A}{1+A\beta}$  where  $A_f$  = closed-loop gain,  $A$  = open-loop gain.

for  $A_f$  to be accurate,  $A_f = \frac{1}{1+\beta} \rightarrow A$  needs to approach infinite ( $A \rightarrow \infty$ )  
(only depends on  $\beta$ ) such that  $A_f = \frac{1}{\beta}$ .

3.) a.) Figure 4(a) : reference parameter is  $V_{BE}$  since  $T_C F$  depends on  $V_{BE}$ . In this figure however, it's not bootstrapped.  $V_{BEQ1}$  will change slightly with supply voltage it still depends on supply voltage. ( $V_{BEQ1}$  will affect  $I_o$ )

Figure 4(b) : reference parameter is also  $V_{BE}$  but in this figure it's bootstrapped. The  $I_o$  won't be affected by the supply voltage.

2 important attributes: •) circuit provides constant bias current and/or voltage so that parameters don't depend on supply voltages, temperatures, etc.  
•) reference parameter is present for bias circuits

b.) Figure 4(a) depicts the simple bias circuit.

Assumptions :  $I_B = 0$  for all transistor making  $I_{out} = I_{EQ2} = I_{R2}$

$I_{out} = \frac{V_{R2}}{R_2} = \frac{V_{BEQ1}}{R_2}$  using the transistor equation  $V_{BE} = V_T \ln \left( \frac{I_c}{I_s} \right)$ , ( $I_{ref} = I_{CQ1}$ )

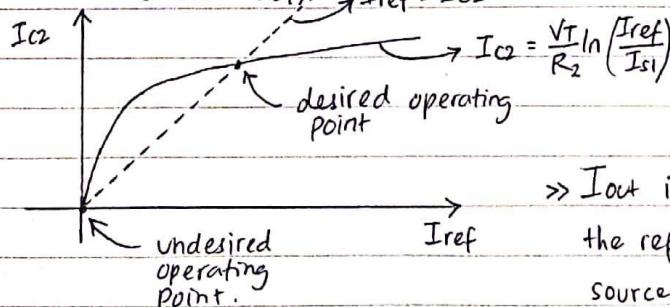
$$I_{at} = \frac{V_T}{R_2} \ln \left( \frac{I_{ref}}{I_{S1}} \right)$$

//  $\Rightarrow I_{at}$  is dependent with the supply voltage since  $V_{BEQ1}$  will change slightly with the supply voltage because  $I_{CQ1}$  ( $= I_{ref}$ ) is approximately proportional to  $V_{cc}$ .  
 $(I_{CQ1} = \frac{V_{cc} - (V_{BEQ2} + V_{BEQ1})}{R_1})$

c.) Figure 4(b) depicts the improved bias circuit

Assumptions :  $V_A = \infty$ ;  $I_B = 0$  for all transistors;  $Q1, Q2, R_2$  are the same as 4(a)

$Q3$  is the current mirror of  $Q1$ ;  $Q4, Q5, Q6$  are part of a simple current mirror ( $I_{out} = I_{CQ1}$ ),  $I_{ref} = I_{C2}$  ( $I_{ref} = I_{C2} = I_{out}$ ), hence  $I_{ref} = I_{C2}$ .



\* note that the formula from (b)'s  $J_{out}$  is now  $I_{C2}$  for Figure 4(b)..

$\Rightarrow I_{out}$  is now independent of supply voltage  $V_{cc}$  since the reference circuit is made to depend on the current source itself (not through a resistor which depends on  $V_{cc}$ )

d.)  $T_{CF} = \frac{\partial X}{\partial T}$  where  $X$  is a variable,  $T$  is temperature

$$\text{for } T_{CF}(I_{out}) = \frac{1}{I_{out}} \frac{\partial I_{out}}{\partial T}$$

$$\text{since } I_{out} = \frac{V_{BEI}}{R_2}, \quad \frac{\partial I_{out}}{\partial T} = \frac{\frac{\partial V_{BEI}}{\partial T} R_2 - V_{BEI} \frac{\partial R_2}{\partial T}}{R_2^2} = \frac{1}{R_2} \frac{\partial V_{BEI}}{\partial T} - \frac{V_{BEI}}{R_2^2} \frac{\partial R_2}{\partial T}$$

$$= \frac{V_{BEI}}{R_2} \left( \frac{1}{V_{BEI}} \frac{\partial V_{BEI}}{\partial T} - \frac{1}{R_2} \frac{\partial R_2}{\partial T} \right) = I_{out} \left( \frac{1}{V_{BEI}} \frac{\partial V_{BEI}}{\partial T} - \frac{1}{R_2} \frac{\partial R_2}{\partial T} \right)$$

$$T_{CF}(I_{out}) = \frac{1}{I_{out}} \left[ I_{out} \left( \frac{1}{V_{BEI}} \frac{\partial V_{BEI}}{\partial T} - \frac{1}{R_2} \frac{\partial R_2}{\partial T} \right) \right] \quad (\text{just let } V_{BEI} = V_{BE} \text{ & } R_2 = R)$$

$$T_{CF}(I_{out}) = \frac{1}{V_{BE}} \frac{\partial V_{BE}}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \quad \text{where } T_{CF}(V_{BE}) = \frac{1}{V_{BE}} \frac{\partial V_{BE}}{\partial T} \text{ & } T_{CF}(R) = \frac{1}{R} \frac{\partial R}{\partial T}$$

As  $T_{CF}(V_{BE})$  is negative &  $T_{CF}(R)$  is positive, the net  $T_{CF}$  is large. Hence, sensitive to temperature with a negative gradient (i.e. as  $T \uparrow$ ,  $I_{out} \downarrow$ )  
 $\rightarrow T_{CF}(I_{out}) = -ve - (+ve) = -ve \text{ net.}$

e.) Bandgap bias circuit utilizes both  $V_{BE}$ -based and  $V_T$ -based reference circuit.

$V_{BE}$ -based  $\rightarrow$  negative net gradient,  $V_T$ -based  $\rightarrow$  positive net gradient.

$\hookrightarrow$  obtain a reference current that is a weighted sum of both of reference currents.

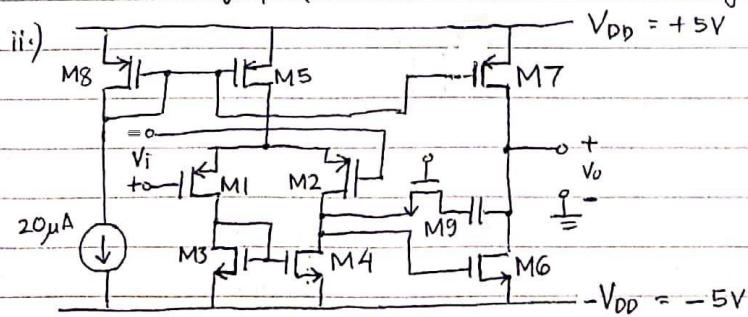
The op-amp has the property  $V_+ = V_-$  making  $V_{R1} = V_{R2}$  (refer to bandgap bias circuit).

$V_{out} = V_{BEI} + KV_T$  is the formula resulted from this where  $K = \frac{R_2}{R_3} \ln \left( \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \right)$

By proper choice of  $K$ ,  $V_{out}$  can be made virtually independent of temperature & supply voltage.

- 4.) a.) •  $V_{GSA} = V_{GSB}$  (not sure)  
•  $I_{ref} = I_{out}$ , so that current mirror ratio = 1 ( $I_G$  for both nMOS is 0)

b.) i.)  $R_3$  &  $R_4$  are passive loads, we want to minimize using passive loads and use more active loads (transistors) because using active loads can produce very high gain in one stage, & inherent differential-to-single-ended conversion



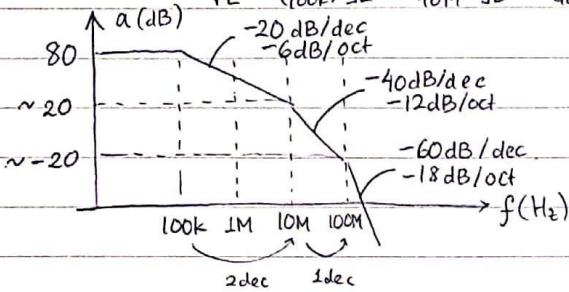
Now  $R_3$  &  $R_4$  becomes current mirror of M3 & M4. (They're both nMOS)

$$c.) \omega_1 = 100\text{kHz}, \omega_2 = 10\text{MHz}, \omega_3 = 100\text{MHz}, a_0 = 10^4, a(j\omega) = \frac{10^4}{(1+j\frac{\omega}{100k})(1+j\frac{\omega}{10M})(1+j\frac{\omega}{100M})}$$

2 dec                    1 dec

i.) Since the op-amp is open loop, we don't need to concern about closed loop parameters such as  $b(j\omega)$  and  $T(j\omega)$ .

$$|a(j\omega)| = \frac{10^4}{\sqrt{[1 + (\frac{\omega}{100k})^2][1 + (\frac{\omega}{10M})^2][1 + (\frac{\omega}{100M})^2]}} \quad a_0 \text{ in dB} = 20 \log_{10}(10^4) = 80 \text{ dB}$$



Phase Margin  $|a(j\omega_{loopgain=1})| = 1$ :  
 $|a(j50M)| = 3.508$

$|a(j60M)| = 2.350$

$|a(j80M)| = 1.211$

$|a(j85M)| = 1.047 \approx 1 \rightarrow \omega_{loopgain=1} = 85\text{MHz}$ 
 $\rightarrow \angle a(j85M) = -[\tan^{-1}(\frac{85M}{100k}) + \tan^{-1}(\frac{85M}{10M}) + \tan^{-1}(\frac{85M}{100M})] = -213.587^\circ$

Since  $\angle a(j85M) < -180^\circ$ , the op-amp is unstable.

ii.)  $|Vt| = 0.8V, \mu_nCox = 30\mu\text{A/V}^2, \mu_pCox = 20\mu\text{A/V}^2, |VA| = 50V$

all simple current mirror for input stage (first stage) is  $\frac{40}{8}$  ratio.  
 redesigned.

$$|Av_1| = -g_{m2}(r_o2 // r_o4)$$

$\text{where } g_{m2} = \frac{2ID_2}{V_{GS2} - V_t}, r_o = \frac{V_A}{ID}$

- $I_{M8} = I_{M5} = 20\mu\text{A}$  same with  $I_{M7} = 20\mu\text{A}$  since M8, M5, M7 form a current mirror with the same aspect ratio of  $100/8$ .

- Using KCL,  $I_{M1} = I_{M2} = \frac{20\mu\text{A}}{2} = 10\mu\text{A}$  same goes with  $I_{M3} = I_{M4} = 10\mu\text{A}$ .

- To find  $V_{as2}$  (assume saturation first)

$ID_2 = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_2 (|V_{as2}| - V_{tn})^2 \rightarrow \frac{8}{100} = (|V_{as2}| - 0.8)^2$

$10\mu\text{A} = \frac{1}{2} 30\mu\text{A} \left(\frac{100}{8}\right) (|V_{as2}| - 0.8)^2 \rightarrow \frac{\sqrt{2}}{5} = |V_{as2}| - 0.8 \rightarrow |V_{as2}| = \frac{1.083V}{V_{GSn1}}$

- Since  $V_G$  of M1 & M2 = 0, (ground all AC)

$V_g - V_s = 1.031 \rightarrow V_s = -1.031V$

- For M3, M4,

$ID_{3,4} = \frac{1}{2} (30\mu\text{A}) \left(\frac{40}{8}\right) (V_{GSn3,4} - 0.8)^2 \rightarrow \frac{8}{60} = (V_{GSn} - 0.8)^2$

$10\mu\text{A} = \frac{1}{2} 30\mu\text{A} \left(\frac{10}{8}\right) (V_{GSn} - 0.8)^2 \rightarrow \frac{\sqrt{10}}{15} = V_{GSn} - 0.8 \rightarrow V_{GSn3,4} = 1.165V$

- $V_s$  of M3 & M4 = -5V,  $V_{G3} = V_{G4} = -3.835V$

- $V_{D1} = V_{D2} = V_{G3} = V_{G4} = -3.835V$

$|V_{Dsp1,2}| = |V_{D1,2} - V_{S1,2}| = |-3.835 - (-1.031)| = |-2.804V| = 2.804V$

$\therefore |V_{Dsp2}| \geq |V_{as1}| - |V_{D1}|$

Saturation region

$2.804 \geq 1.083 - 0.8 = 0.283$

No. ....

Date \_\_\_\_\_

$$\text{Finding } g_{m2} = \frac{2(10\mu)}{1.083 - 0.8} = 70.671\mu, r_{o2} = \frac{50}{10\mu} = 5M = r_{o4}$$

$$A_{v1} = -70.671\mu (5M // 5M) = -176.678 \frac{V}{V} //$$

- d.) Power Supply Rejection Ratio (PSRR) could be improved by increasing the impedance between the supply node & the output node (that's why we use current mirrors too to increase impedance).  
(not sure)