NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2019-2020

EE2002 – ANALOG ELECTRONICS

November / December 2019 Time Allowed: 2½ hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 10 pages.
2. Answer all 4 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.
6. A List of Formulae is provided in Appendix A on pages 7-10.

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1. (a) A non-ideal Op-Amp configured with resistors is shown in Figure 1(a) on page 2. The Op-Amp is powered by $\pm V_{CC}$ power supplies. It has 2 non-ideal sources, I_+ and I_- in the absence of the input offset voltage, $V_{IO} \approx 0$.

   Derive the expression for the output voltage v_{OUT} when $v_a = v_b = 0$, in terms of R_1, R_2, R_3, R_4, R_5, R_6, R_7, R_8, I_+ and I_-.

   Note: *Parallel resistance of R_x and R_y can be written as $R_x//R_y$ without expanding it.*

   (10 Marks)

Note: Question No. 1 continues on page 2.

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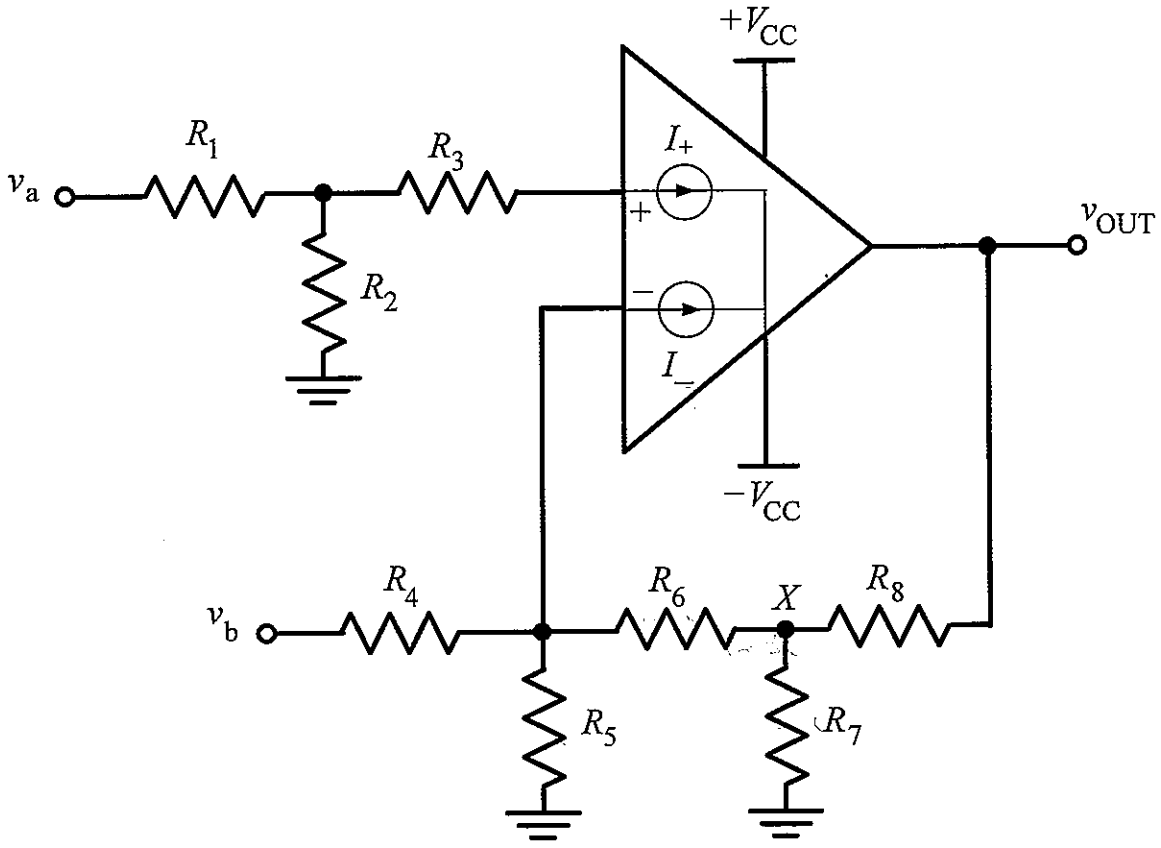

Figure 1(a)

(b) In Figure 1(b) on page 3, the empirical junction diode equation is:

$$V_D = nV_T \, ln[I_D/I_S]$$

for diodes D_1 and D_2 , given that

$V_{D1} = 0.674$ V at $I_{D1} = 426$ μA and
$V_{D2} = 0.794$ V at $I_{D2} = 4.28$ mA.

Also, given that $V_1 = 6$ V and $V_2 = 4.5$ V, $R_1 = R_2 = 8$ kΩ , $R_3 = 16$ kΩ , $R_4 = 24$ kΩ , $R_5 = R_6 = 6$ kΩ, find the DC operating point or quiescent (Q) - point (I_D, V_D) for the diodes D_1 and D_2 (to 3 decimal places in mA and V, respectively).

Note: D_1 and D_2 have the same nV_T and I_S.

(15 Marks)

Note: Question No. 1 continues on page 3.

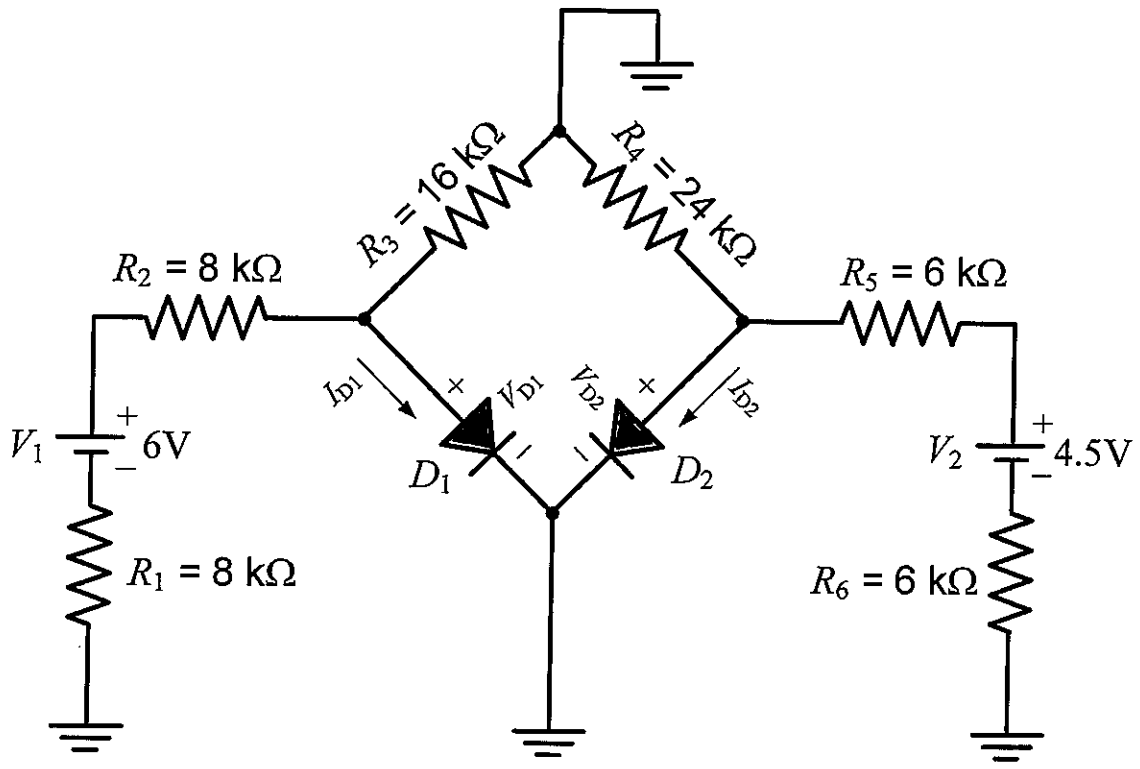

Figure 1(b)

2. Consider the source-follower circuit showing a "bootstrapped" resistor R_G as shown in Figure 2 on page 4. Assume all capacitors have infinite value (open circuit at DC, short circuit at AC). The inductor L is likewise infinite in value (short circuit at DC, open circuit at AC).

(a) Given $R_G = R_S = 2$ kΩ, $K_n = 2$ mA/V², $V_{TN} = 1$V, and $\lambda = 0.01$ V⁻¹, solve for the DC operating point (I_D, V_{DS}), and hence calculate the small signal parameters g_m and r_o.

(5 Marks)

(b) Determine the AC voltage gain $A_v = v_o / v_i$.

(5 Marks)

(c) Make use of part (b) to determine the AC input resistance R_{in}.

(5 Marks)

(d) Determine the AC output resistance R_{out}.

(5 Marks)

Note: Question No. 2 continues on page 4.

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(e) Determine the maximum AC input amplitude v_i that will satisfy the small signal limit.

(5 Marks)

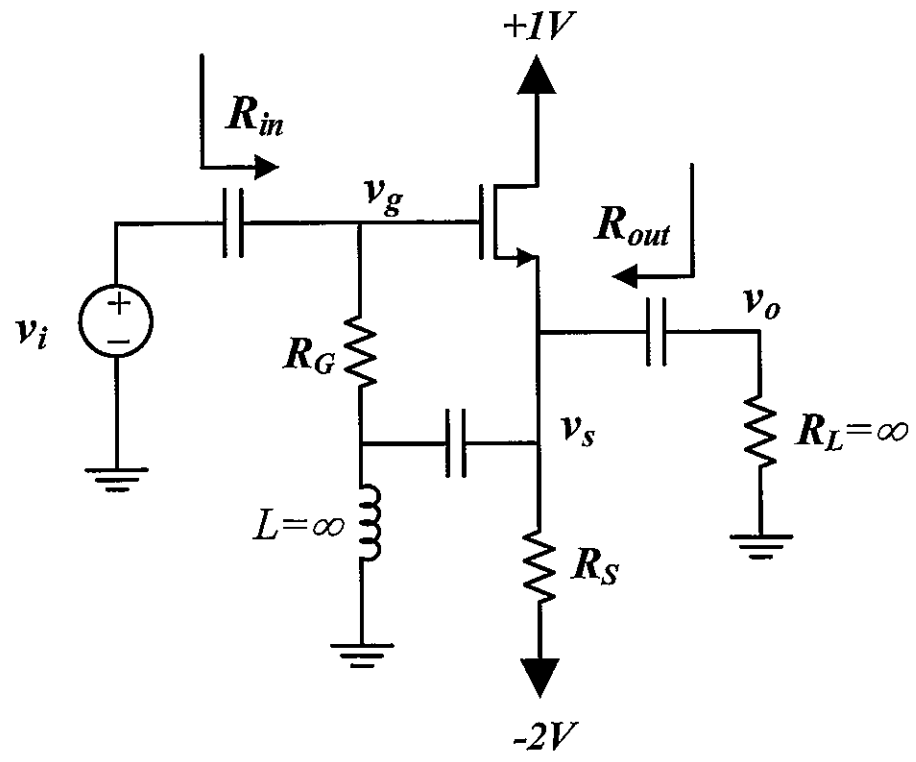


Figure 2

3. For the differential circuit in Figure 3 on page 5, assume V_{DD} = 12 V, V_{SS} = −12 V, R_{G1} = 100 kΩ, R_{G2} = 50 kΩ, R_S = 5 kΩ, R_D = 8 kΩ, K_n = 200 μA/V² and V_{TN} = 2 V. Here v_{i1} and v_{i2} represent the differential inputs, and v_{o1} and v_{o2} represent the differential outputs. Assume all the capacitors have infinite values and $\lambda = 0$.

   (a) Determine the Q-points (I_D , V_{DS}) for the transistors.

   (5 Marks)

   (b) Determine the differential-mode gains and common-mode gains for the cases of both single-ended and differential outputs.

   (10 Marks)

Note: Question No. 3 continues on page 5.

(c) Determine the common-mode rejection ratios (CMRRs) for the cases of both single-ended and differential outputs. In addition, discuss the effect of variation of R_S to the CMRRs.

(4 Marks)

(d) Determine the differential-mode and common-mode input resistances and output resistances.

(6 Marks)

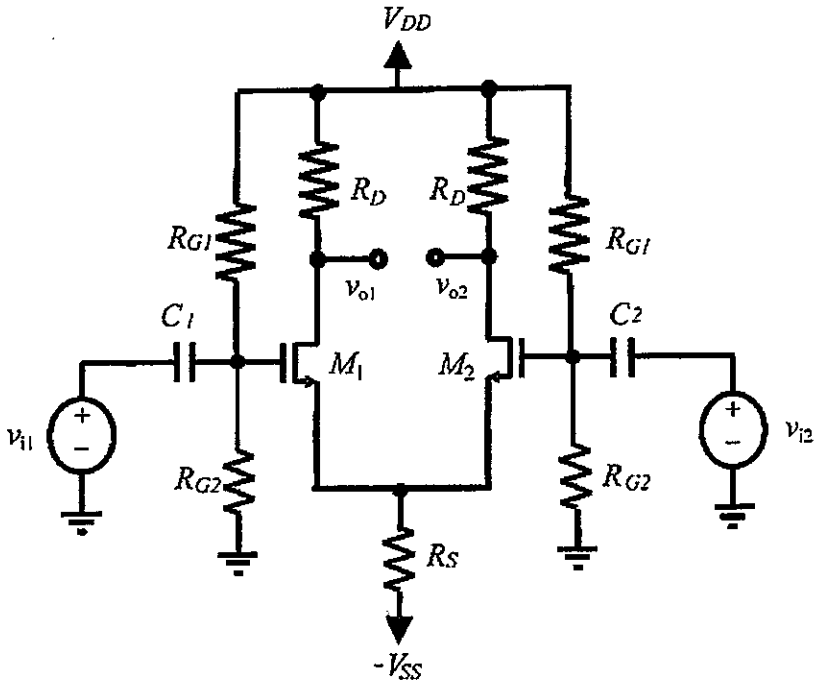


Figure 3

4. (a) Consider the current mirror circuit shown in Figure 4(a) on page 6. Assume all NMOS transistors are identical with parameters K_n = 200 μA/V², V_{TN} = 0.5 V, λ = 0.05 V^{-1} and the power supply voltage V_{DD} is 5 V. If I_{REF} = 100 μA, find the gate voltages of M_1 and M_2 denoted by V_A and V_B respectively by ignoring the Early effect. Also, find the output current I_{out} by including the Early effect.

(15 Marks)

(b) Consider the active filter circuit shown in Figure 4(b) on page 6 comprising an ideal operational amplifier, resistors and capacitors.

(i) Find the transfer function $H(s) = v_{out} / v_s$ for the circuit in terms of the resistors and capacitors.

(5 Marks)

Note: Question No. 4 continues on page 6.

(ii) How many poles and zeros are there in this transfer function? Write down algebraic expressions for these poles and zeros in terms of the resistors and capacitors.

(5 Marks)

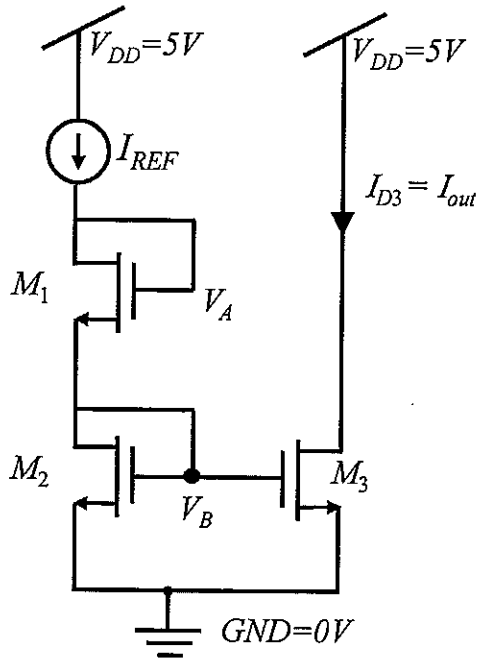


Figure 4(a)

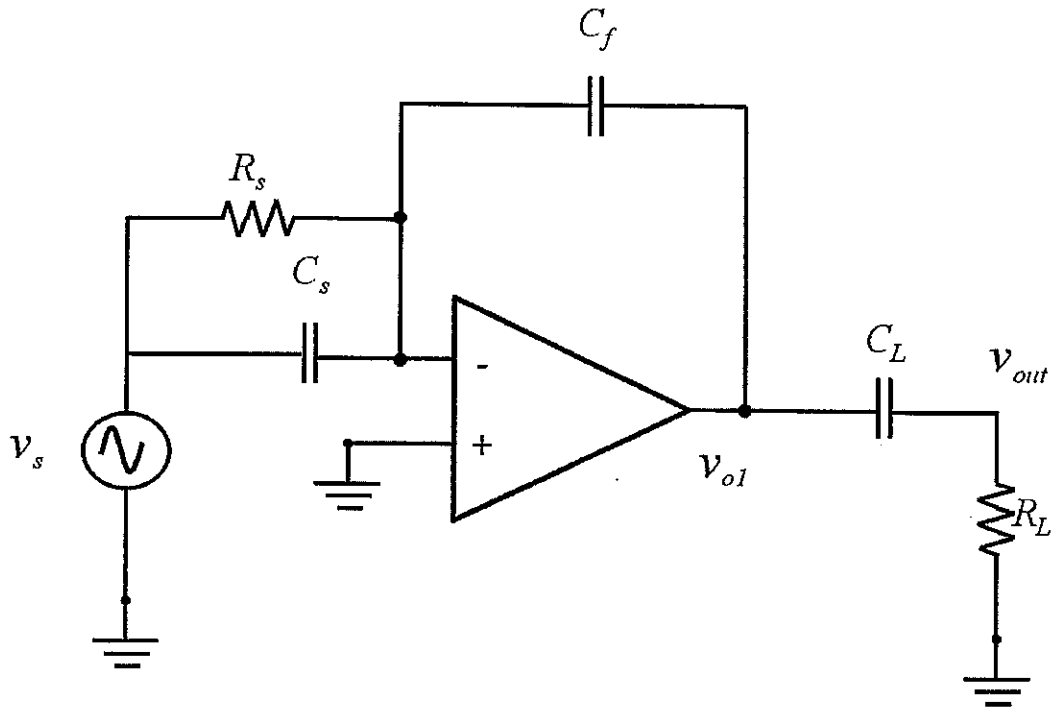


Figure 4(b)

Appendix A

List of Formulae (with the usual notations)

Op-Amps:

Closed-Loop Negative Feedback Inverting Gain, $A_{VCL} = \frac{v_o}{v_i} = -\frac{R_f}{R_i}$ Figure (a)

Closed-Loop Negative Feedback Non-Inverting Gain, $A_{VCL} = \frac{v_o}{v_i} = \left(1 + \frac{R_f}{R_i}\right)$ Figure (b)

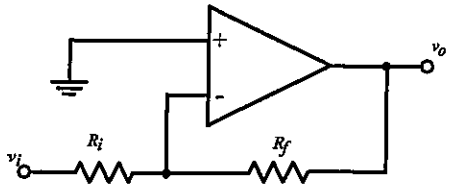


Figure (a)

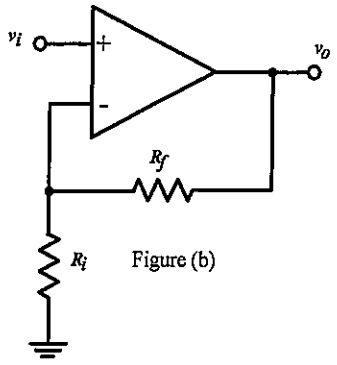
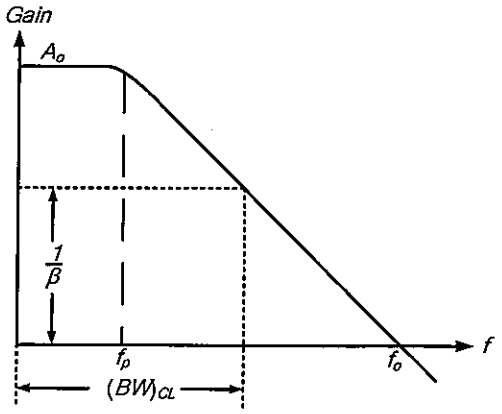


Figure (b)

Op-Amp's Slew Rate, $SR \geq \left|\frac{dv_o}{dt}\right|_{max} = A_{VCL}\omega a_m = A_{VCL} a_m 2\pi f$,

where $v_i = a_m \sin(\omega t)$, $v_o = A_{VCL} v_i$, $v_o = A_{VCL} a_m \sin(\omega t)$ and $\left|\frac{dv_o}{dt}\right| = A_{VCL}\omega\, a_m \cos(\omega t)$

Op-Amp's frequency response: $A_{VOL}(jf) = \frac{A_o}{\left(1 + \frac{jf}{f_p}\right)}$



Gain-Bandwidth Product: $A_o f_p = f_o = \frac{1}{\beta}(BW)_{CL}$

where $\frac{1}{\beta} = \frac{R_f + R_i}{R_i}$

$t_r = \frac{0.35}{(BW)_{CL}}$

Diodes:

$v_D \approx nV_T \ln\left(\frac{i_D}{I_S}\right)$ or $i_D \approx I_S e^{\left(\frac{v_D}{nV_T}\right)}$

where $e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \ldots\ldots$

Diode conductance: $g_D = \frac{1}{r_D} = \frac{I_D}{nV_T}$

BJT in Forward Active Region:

Ignore early effect: $i_C = I_S \exp\left(\frac{|v_{BE}|}{V_T}\right)$

With early effect: $i_C = I_S \exp\left(\frac{|v_{BE}|}{V_T}\right)\left(1+\frac{|v_{CE}|}{V_A}\right)$

where I_S: Saturation current,
V_T: Thermal voltage, assume 25 mV at room temperature,
V_A: Early voltage.
For npn transistor, $|v_{BE}| = v_{BE}$ and $|v_{CE}| = v_{CE}$;
For pnp transistor, $|v_{BE}| = v_{EB}$ and $|v_{CE}| = v_{EC}$.

Small-signal model parameters of BJT:

$g_m = \frac{I_C}{V_T}$, $r_\pi = \frac{\beta}{g_m}$ and $r_o = \frac{V_A + |V_{CE}|}{I_C} \approx \frac{V_A}{I_C}$

where I_C : DC collector current at Q-point
V_{CE}: DC collector-emitter voltage at Q-point

Criterion for small-signal operation of BJT: $|v_{be}| \le 0.2V_T$

MOSFET in Saturation Region:

Criterion: $V_{DS} \ge V_{GS} - V_{TN}$ for NMOS;
$|V_{DS}| \ge |V_{GS}| - |V_{TP}|$ for PMOS

where V_{TN}, V_{TP}: Threshold voltage,
V_{DS}: DC drain-source voltage,
V_{GS}: DC gate-source voltage.

Ignore channel-length modulation effect: $i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2$ for NMOS,

$i_D = \frac{K_p}{2}(|v_{GS}| - |V_{TP}|)^2$ for PMOS.

With channel-length modulation effect: $i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2(1+\lambda v_{DS})$ for NMOS,

$i_D = \frac{K_p}{2}(|v_{GS}| - |V_{TP}|)^2(1+\lambda |v_{DS}|)$ for PMOS.

where λ: channel length modulation parameter,

For NMOS $K_n = K_n'\left(\frac{W}{L}\right)$ and $K_n' = \mu_n C_{ox}$; For PMOS $K_p = K_p'\left(\frac{W}{L}\right)$ and $K_p' = \mu_p C_{ox}$.

MOSFET in Triode Region:

Criterion: $V_{DS} < V_{GS} - V_{TN}$ for NMOS;
$|V_{DS}| < |V_{GS}| - |V_{TP}|$ for PMOS

Ignore channel-length modulation effect: $i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}$ for NMOS,

$i_D = K_p\left(|v_{GS}| - |V_{TP}| - \frac{|v_{DS}|}{2}\right)|v_{DS}|$ for PMOS.

With channel-length modulation effect: $i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}(1+\lambda v_{DS})$ for NMOS,

$i_D = K_p\left(|v_{GS}| - |V_{TP}| - \frac{|v_{DS}|}{2}\right)|v_{DS}|(1+\lambda|v_{DS}|)$ for PMOS.

Small-signal model parameters of MOSFET

For NMOS: $g_m = \sqrt{2K_n I_D(1+\lambda V_{DS})} \approx \sqrt{2K_n I_D}$ and $r_o = \frac{\frac{1}{\lambda} + V_{DS}}{I_D} \approx \frac{1}{\lambda I_D}$

For PMOS: $g_m = \sqrt{2K_p I_D(1+\lambda|V_{DS}|)} \approx \sqrt{2K_p I_D}$ and $r_o = \frac{\frac{1}{\lambda} + |V_{DS}|}{I_D} \approx \frac{1}{\lambda I_D}$

where I_D : DC drain current at Q-point
V_{DS}: DC drain-source voltage at Q-point

Criterion for small-signal operation:
For NMOS: $|v_{gs}| \le 0.2(V_{GS} - V_{TN})$
For PMOS: $|v_{gs}| \le 0.2(|V_{GS}| - |V_{TP}|)$
where V_{GS} : DC gate-source voltage at Q-point.

Frequency Response: OCTC and SCTC

0) DISABLE DC sources…
voltage sources -> SHORT CIRCUIT, current sources -> OPEN CIRCUIT

1) Identify capacitors contributing (reducing V_o or causing trouble) to the frequency of interest (i.e. lower or higher cut-off).

2) DISABLE all independent AC sources...
voltage sources -> SHORT CIRCUIT, current sources -> OPEN CIRCUIT
DO NOT remove or "disable" dependent sources!

↓ higher cut-off (OCTC)

3) Idealize irrelevant capacitors by SHORT CIRCUIT (because at high f, cap → short)

Next step to find time constant
4) For each contributing capacitor C_i, set all other capacitors (other than the one you are looking at) removed (i.e. OPEN CIRCUITS) and determine the resistance, R_i seen by C_i
5) Higher cut-off frequency is estimated as:

$$\omega_{H-3dB} \approx \frac{1}{\sum_i C_i R_i} = \frac{1}{C_1 R_1 + C_2 R_2 + \ldots}$$

↓ lower cut-off (SCTC)

3) Idealize irrelevant capacitors by OPEN CIRCUIT (because at low f, cap → open)

Next step to find time constant
4) For each contributing capacitor C_i, set all other capacitors (other than the one you are looking at) removed (i.e. SHORT CIRCUITS) and determine the resistance, R_i seen by C_i
5) Lower cut-off frequency is estimated as:

$$\omega_{L-3dB} \approx \sum_i \frac{1}{C_i R_i} = \frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} + \ldots$$

END OF PAPER

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1-(a) Use superposition theorem

$V_{out} = V_{out}|_{I_1} + V_{out}|_{I_2}$

$= -\underbrace{(R_3 + R_1 // R_2)\left(\frac{R_4 // R_5 + R_6}{R_4 // R_5}\right)}_{V_{1k}}\left(\frac{R_8 + (R_4 // R_5 + R_6) // R_7}{(R_4 // R_5 + R_6) // R_7}\right) I_1 + \underbrace{I_2 (R_6)}_{V_{1k}}\left(\frac{R_8 + R_6 // R_7}{R_6 // R_7}\right)$

(b) First find the valve of the 2 constants. nV_T and I_S.

$$0.674 = nV_T \ln \frac{426 \times 10^{-6}}{I_S} \quad (1)$$

$$0.794 = nV_T \ln \frac{4.28 \times 10^{-3}}{I_S} \quad (2)$$

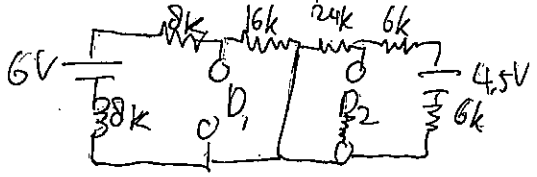
Sub (1) to (2)

$$0.794 = 0.674 + nV_T \ln \frac{4.28 \times 10^{-3}}{426 \times 10^{-6}}$$

$nV_T = 0.052\ V$

$I_S = 1.003 \times 10^{-9}\ A$

Find V_{th} and R_{th} for D_1 and D_2

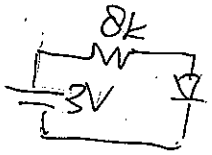


$V_{D1} = \frac{16k}{8k+8k+16k} \cdot 6V$ $\quad V_{D2} = \frac{24k}{24k+6k+6k} \cdot 4.5V$

$= 3V$ $\quad = 3V$

$R_{D1} = 16k // 16k = 8k$ $\quad R_{D2} = 24k // 12k = 8k$

Since $V_{D1} = V_{D2}$ and $R_{D1} = R_{D2}$, we just need to find V and I once



$I_D = \frac{3 - V_D}{8k}$

$V_D = nV_T \ln \frac{I_D}{I_S}$

start with $V_D = 0.7$

$I_D = 0.288mA$ $\quad V_D = 0.653$

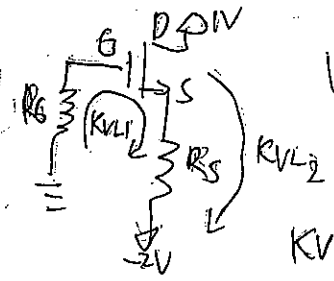
$I_D = 0.293mA$ $\quad V_D = 0.654$

$I_D = 0.293mA$ $\quad V_D = 0.654$

Q point (0.293mA, 0.654V) for both D_1 and D_2

(1)

2.(a)



$V_G = 0$ since $I_G = 0$

KVL 1

$$V_{GS} + I_D R_S = 2V$$

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2$$

$$V_{GS} + \frac{K_n}{2}(V_{GS} - 1)^2 \cdot 2k = 2$$

$$V_{GS} + 2(V_{GS}^2 - 2V_{GS} + 1) = 2$$

$$2V_{GS}^2 - 3V_{GS} = 0$$

$$V_{GS} = 0 \text{ (X)}, \ \frac{3}{2}V$$

$$I_D = 0.25mA$$

KVL 2

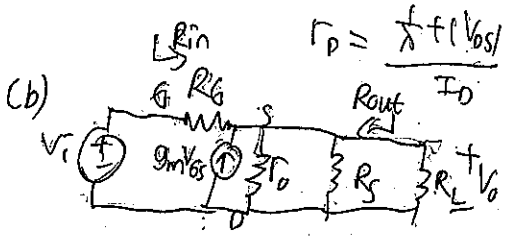
$$V_{DS} + I_D R_S = 3V$$

$$V_{DS} = 2.5V$$

$$g_m = \sqrt{2K_n I_D} = 10^{-3}\ \Omega^{-1}$$

$$r_o = \frac{\lambda^{-1} + |V_{DS}|}{I_D} = 410000\ \Omega$$

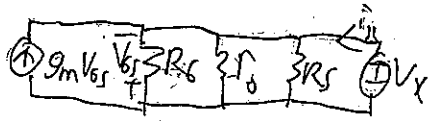
(b)



$$\text{gain} = \frac{V_o}{V_i} = \frac{(g_m V_{GS} + \frac{V_{GS}}{R_G})(R_G \| R_S \| R_L)}{V_{GS} + (g_m V_{GS} + \frac{V_{GS}}{R_G})(r_o \| R_S \| R_L)} \xrightarrow{R_L \to \infty} \frac{(g_m + \frac{1}{R_G})(r_o \| R_S)}{1 + (g_m + \frac{1}{R_G})(r_o \| R_S)} = 0.799$$

(c) $$R_{in} = \frac{V_i}{\frac{V_{GS}}{R_G}} = \frac{V_i}{\frac{V_i - V_o}{R_G}} = \frac{V_i}{V_i - V_o} \times R_G = 4R_G = 8k\Omega$$

(d)



use KCL

$$-g_m V_X + i_X = \frac{V_X}{R_G} + \frac{V_X}{r_o} + \frac{V_X}{R_S}$$

$$i_X = V_X\left(g_m + \frac{1}{R_G} + \frac{1}{r_o} + \frac{1}{R_S}\right)$$

$$R_{out} = \frac{1}{g_m + \frac{1}{R_G} + \frac{1}{r_o} + \frac{1}{R_S}} = 499.39\Omega$$

(c) $|V_{gs}| \leq 0.2(V_{GS} - V_{TN})$ ①

$V_{ri} = V_{GS} + (g_m V_{GS} + \frac{V_{GS}}{R_G})(r_o // R_S)$

$V_i = V_{GS}(1 + (g_m + \frac{1}{R_G})(r_o // R_S))$

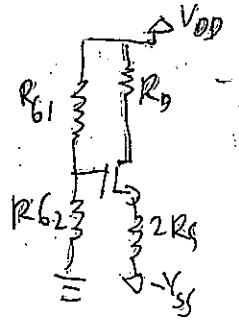
$V_{GS} = \dfrac{V_i}{1 + (g_m + \frac{1}{R_G})(r_o // R_S)}$

Sub back to ①

$V_i \leq 0.2(0.5)(1 + (g_m + \frac{1}{R_G})(r_o // R_S))$

$V_i \leq 0.4 \quad V$

3 (a) Consider only half of the differential amplifier since it is symmetrical

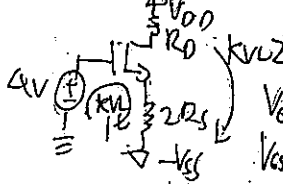


Replace R_{G1} and R_{G2} with V_{th} for gate of ~~the transistor~~

$V_{th} = \dfrac{R_{G2}}{R_{G1}+R_{G2}}(V_{SS} - 0)$

$= 4V$

No need R_{th} since no current flows through gate



KVL2 KVL1

$V_{GS} + I_D \cdot 2R_S = 4 - (-12)$

$V_{GS} + I_D \cdot 2R_S = 16$

$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2$

$V_{GS} + K_n \cdot R_S (V_{GS} - V_{TN})^2 = 16$

$V_{GS} + V_{GS}^2 - 4V_{GS} + 4 = 16$

$V_{GS}^2 - 3V_{GS} - 12 = 0$

$V_{GS} = \dfrac{3 + \sqrt{57}}{2} V = 5.275\ V$

$I_D = 1.0725\ mA$

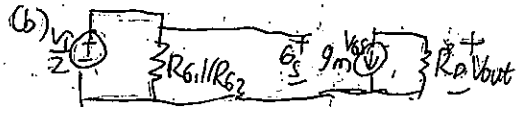
KVL 2

$I_D(R_G + 2R_S) + V_{DS} = 24$

$V_{DS} = 4.695\ V$

Q points (1.0725 mA, 4.695 V)

(b)

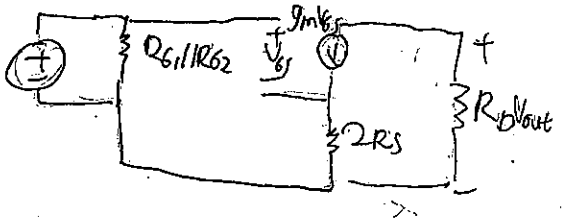


$g_m = \sqrt{2K_n I_D} = 6.55 \times 10^{-4}$

diff mode

single ended gain $= \dfrac{-g_m \frac{V_i}{2} \cdot R_D}{V_i} = -\frac{1}{2} g_m R_D = -2.62$

③ diff output gain $= \dfrac{-g_m \frac{V_i}{2} R_D - \frac{1}{2} g_m \frac{V_i}{2} R_D}{V_i} = -g_m R_D = -5.24$



Common mode gain

single ended $\text{gain} = \dfrac{-g_m V_{GS} R_D}{V_{GS} + g_m V_{GS}(2\|R_S)}$

$= \dfrac{-g_m R_D}{1 + g_m \cdot 2R_S} = -0.694$

differential mode gain $= 0$ since V_{o1} and V_{o2} are the same

(c) $\text{CMRR (single ended)} = \dfrac{\text{diff mode se}}{\text{common mode se}} = \left| \dfrac{\frac{-g_m R_D}{2}}{\frac{-g_m R_D}{1 + g_m 2R_S}} \right| = \dfrac{1 + 2g_m R_S}{2} = 3.775$

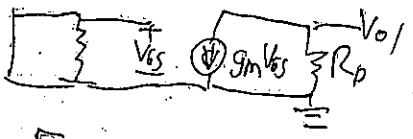
$\text{CMRR (differential output)} = \dfrac{\text{diff mode}_{\text{diff}}}{\text{common mode}_{\text{diff}}} = \left| \dfrac{-g_m R_D}{0} \right| = \infty$

If R_S is increased, V_{GS} (in DC) will decrease and as a result g_m will decrease and the gain for all mode will be uncertain and a better configuration is to add a current source to replace R_S so that I_D is constant and g_m is constant

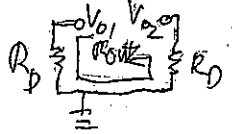
(d) input resistance for all mode is ∞

Output resistance

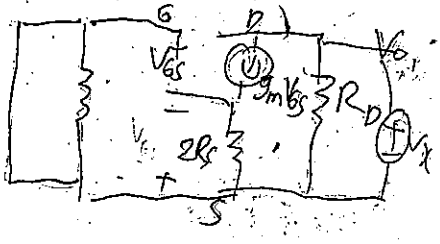
For diff mode



$R_{out} = R_D + R_D = 2R_D$



For common mode

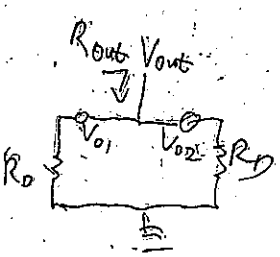


Since V_G and $V_S = 0$

$-V_{GS} = g_m V_{GS} \cdot 2R_S$

$V_{GS} = 0$ since $-1 \neq g_m \cdot 2R_S$

$R_{out} = R_D \| R_D = \dfrac{R_D}{2}$



4. (a) $I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2$

$$V_{GS} = \sqrt{\frac{2I_D}{K_n}} + V_{TN} = 1.5$$

$M_1 = 1.5\ V = V_A$

$M_2 = M_1 + V_{GS}$

$= 3\ V = V_B$

$M_2 = M_3$ $\quad V_{DS} = 5\ V$

$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2 (1 + \lambda V_{DS})$

$= 0.125\ mA$

(b) i. $V_{out} = \frac{R_L}{R_L + \frac{1}{sC_L}} \cdot \frac{-\frac{1}{sC_f}}{\frac{\frac{R_S}{sC_S}}{R_S + \frac{1}{sC_S}}} V_S$

$= \frac{sC_L R_L}{sC_L R_L + 1} \cdot \frac{-\frac{1}{sC_f}}{\frac{R_S}{sC_S R_S + 1}}$

$= \frac{sC_L R_L}{sC_L R_L + 1} \cdot \frac{sC_S R_S + 1}{-sC_f R_S}$

$= \frac{C_L R_L}{C_f R_S} \cdot \frac{sC_S R_S + 1}{sC_L R_L + 1}$

= 1 pole and 1 zero

$pole = \frac{1}{C_L R_L}$

$zero = \frac{1}{C_S R_S}$

Tips & Trick

1. The structure of the question will always be the same
   a- No 1 will always be op amp and diode
   b- No 2 will always be single stage BJT/MOSFET
   c- Differential amplifier, multistage amplifier and current mirror, 2 of them will come out at number 3 & 4.
   d. Transfer function will come out in the last part
2. Always do number 1 first since it's the easiest
3. Do multistage amplifier last (if it comes out)
4. Practice PYP a lot since the structure of the questions are very similar each year