NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2018-2019

EE3019 – INTEGRATED ELECTRONICS

November / December 2018 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer ALL questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.
6. A list of Formulae is provided in Appendix A on page 6.

---

1. (a) Sketch the Voltage Transfer Characteristics of a symmetrical CMOS inverter. Identify the regions of operation of both the pMOS and nMOS transistors of the CMOS inverter when the input changes from 0 V to V_{DD}. Briefly discuss how the variations of V_{IL}, V_{IH}, V_{OL}, V_{OH} and V_{th} can affect the noise margin of the inverter.

(9 Marks)

(b) Consider a CMOS inverter in Figure 1 on page 2. Assume V_{DD} = 1.2 V, V_{OH} = 1.1 V, V_{OL} = 0.1 V, C_o = 5 fF and C_g = 9 fF. The falling time, τ_f, for V_{in} is 530 ps. The parameters of the pMOS and nMOS transistors are given below:

pMOS $V_{tp} = -0.45$ V, $\mu_p C_{ox} = 20\ \mu A/V^2$, $(W/L)_p = 4.5$

nMOS $V_{tn} = 0.46$ V, $\mu_n C_{ox} = 50\ \mu A/V^2$, $(W/L)_n = 2$

For parts (i) and (ii) below, state all your assumptions clearly.

Note: Question No. 1 continues on page 2.

(i) Identify the regions of operation of both the pMOS and nMOS transistors, and determine the drain current i_L when V_{out} is at 20% and 80% of its full value.

(ii) Determine the rising time, t_r, for V_{out} to rise from 20% to 80% of its full value.

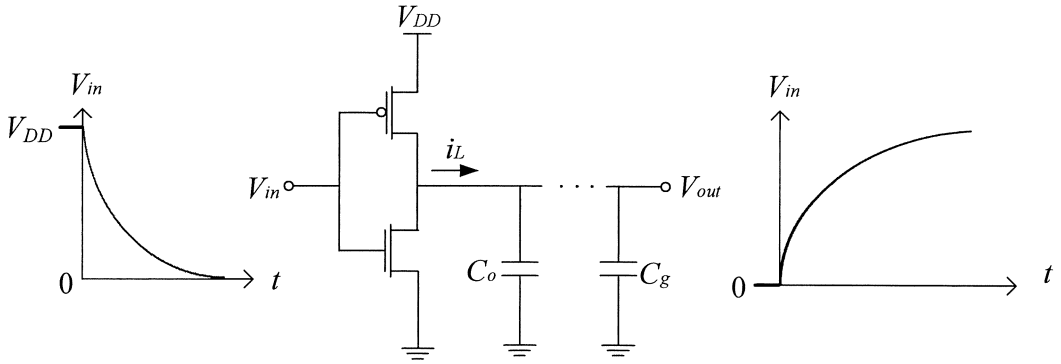

Figure 1

(13 Marks)

(c) Discuss how the noise margin and operating speed of a CMOS logic circuit could be affected by the transistor body effect.

(3 Marks)

2. (a) Consider the 1-T DRAM cell which is constructed using an nMOS transistor. Assume that V_{DD} = 1.2 V and the threshold voltage, V_{tn} = 0.46 V. The bit-line precharge voltage is 0.5 V_{DD}, bit-line capacitance is 0.52 pF and the storage capacitance per cell is 33 fF. Determine the voltage swing of the bit-line for a READ operation when accessing stored data values of '0' and '1'. Briefly discuss the purpose of the Sense Amplifier for the DRAM.

(8 Marks)

(b) A feedback amplifier is shown in Figure 2 on page 3. It is given that R_L = 10 kΩ, R_1 = 7 kΩ, R_2 = 53 kΩ , R_3 = 70 kΩ and R_4 = 60 kΩ,

(i) Identify the feedback topology, and determine the feedback factor, β.

(ii) Determine the closed-loop voltage gain, v_o/v_s, if the op-amp has an open-loop gain of $A = \infty$ and $A = 10^4$.

(iii) If the closed-loop gain changes by 0.5%, determine the corresponding change in the open-loop gain.

Note: Question No. 2 continues on page 3.

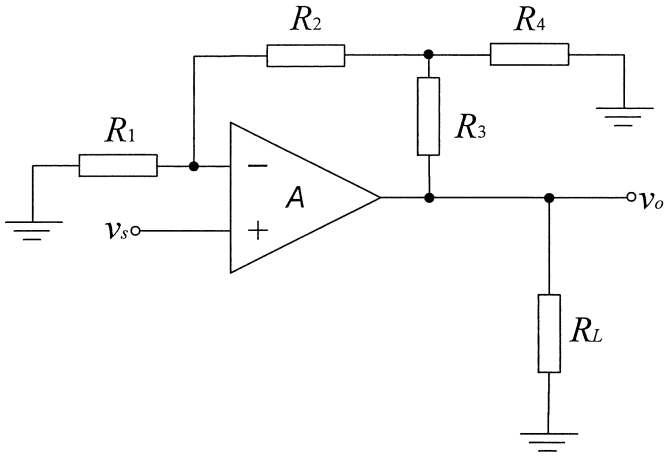

Figure 2

(14 Marks)

(c) Explain why the gain of the negative feedback amplifier decreases at high frequencies.

(3 Marks)

3. The circuit schematic of a Bandgap voltage reference with low Fractional Temperature Coefficient (TC_F) is depicted in Figure 3 on page 4. Resistor R_4 serves to improve the insensitivity to temperature and can be assumed to be a short circuit.

(a) Define the following two parameters:

(i) TC_F, and

(ii) $S_{V_{CC}}^{V_{REF}}$, the sensitivity of the output reference voltage with respect to the supply rail voltage, V_{cc}.

(4 Marks)

(b) Draw a conceptual block diagram of the Bandgap voltage reference and explain the phenomena that provide for low TC_F and low $S_{V_{CC}}^{V_{REF}}$.

(6 Marks)

(c) Derive the expression for the output voltage, V_{REF}, of the Bandgap voltage reference depicted in Figure 3.

(12 Marks)

(d) An engineer chose to employ the fully-bipolar LM741 op-amp in Figure 3. Explain and discuss if this op-amp choice is practically appropriate.

(3 Marks)

Note: Question No. 3 continues on page 4.

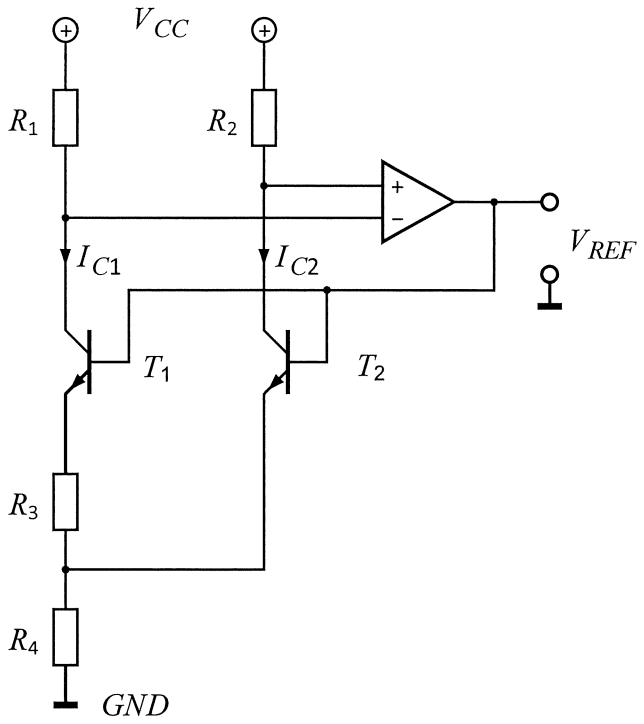

Figure 3

4. The hybrid BJT-CMOS op-amp depicted in Figure 4 on page 5 has three poles located at 10 kHz, 1 MHz and 100 MHz. Assume $R = 465$ kΩ and the following parameters for the transistors in the op amp:

MOS transistors: $|V_t| = 0.8$ V, $\mu_n C_{ox} = 30\mu$A/V^2, $\mu_p C_{ox} = 15\mu$A/V^2, $|V_A| = 50$ V

BJT transistors: $V_{BE(on)} = 0.7$ V, $|V_A| = 50$ V

(a) Explain the function of transistors M_6 and T_9.

(4 Marks)

(b) Assume that the emitter area of the BJT transistors is equal. Determine the drain and collector bias currents in the MOS and BJT transistors, respectively. Complete the following table in your answer script.

Transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	T_9	T_{10}
Current										

(7 Marks)

Note: Question No. 4 continues on page 5.

(c) Determine the voltage gain of the first stage of the op-amp. Assuming that the voltage gain of the second stage of the op-amp is 500, determine if the op-amp is stable.

(12 Marks)

(d) In present-day electronic devices where the integrated circuits are very densely placed, the op-amp is required to feature very high power supply rejection ratio (PSRR). Explain how you would design the op-amp in Figure 4 to obtain high PSRR, and discuss the implication of your design.

(2 Marks)

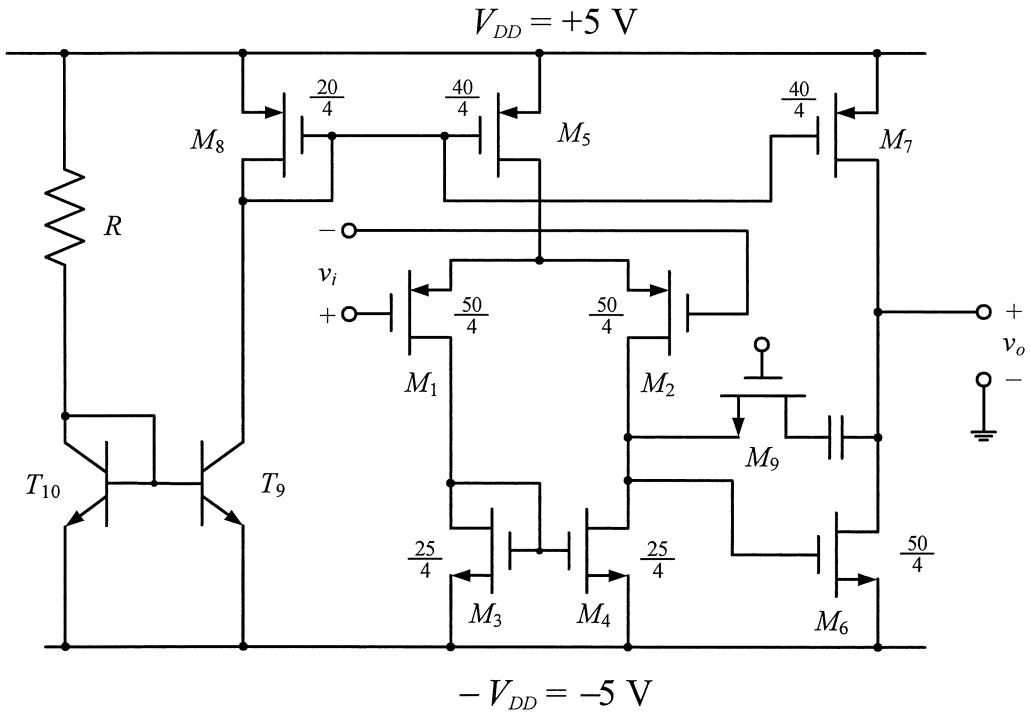

Figure 4

APPENDIX A: List of Formulae for EE3019

$$V = I\,Z \qquad P = I\,V$$

$$Z_L = j\omega L \qquad Z_C = \frac{1}{j\omega C}$$

$$\sum_{m=1}^{M} v_m = 0 \qquad \sum_{n=1}^{N} i_n = 0$$

$$v = L\frac{di}{dt} \qquad i = C\frac{dv}{dt}$$

$$\boldsymbol{S} = \boldsymbol{V}\,\boldsymbol{I}^{*} \qquad i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

$$V_T = \frac{kT}{q} \qquad i_C \approx I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]$$

$$\beta = \frac{i_C}{i_B}$$

$$i_E = i_C + i_B \qquad A + B + C = \overline{\overline{A}\,\overline{B}\,\overline{C}}$$

$$\alpha = \frac{\beta}{1+\beta} \qquad \tau_p = \frac{C_{load} \times \Delta V}{I_{avg}}$$

$$ABC = \overline{\overline{A} + \overline{B} + \overline{C}} \qquad A_f = \frac{A}{1 + A\beta}$$

$$i_{Dn(LIN)} = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left((v_{GS} - v_t)v_{DS} - \frac{1}{2}{v_{DS}}^2\right) \qquad f = \frac{1}{2n\,\tau_p}$$

$$i_{Dn(SAT)} = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - v_t)^2 \qquad V_1 = A_1 A_2\left(V_i - \beta V_o\right) + A_1 V_n$$

$$A(s) = A_m F_H(s) = \frac{A_m}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \qquad r_o = \frac{V_A}{I_D}$$

$$\tau_{PLH} = \sqrt{{\tau_{PLH}}^2(\text{Step Input}) + \left(\frac{\tau_f}{2}\right)^2} \qquad g_m = 2\frac{I_D}{(V_{GS} - V_t)}$$

$$\frac{dA_f}{A_f} = \frac{1}{1 + A\beta} \cdot \frac{dA}{A}$$

END OF PAPER

EE3019 INTEGRATED ELECTRONICS

Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.