INTEGRATED ELECTRONICS

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Topics

1. Power Supplies
2. Bias Circuits
3. Operational Amplifiers
4. **Applications of Operational Amplifiers**

Reference Textbooks

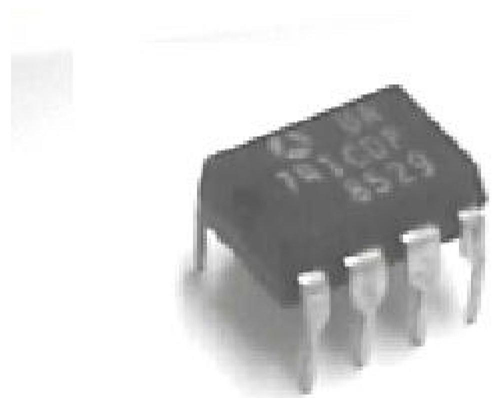
1. Sedra and Smith, *Microelectronic Circuits*, 5th Edition, Oxford University Press, 2004.
2. Gray, Hurst, Lewis and Meyer, *Analysis and Design of Analogue Integrated Circuits*, 4th Edition, John Wiley & Sons, 2001.
3. Franco S, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd Edition, McGraw-Hill, 2002.

Applications of Operational Amplifiers

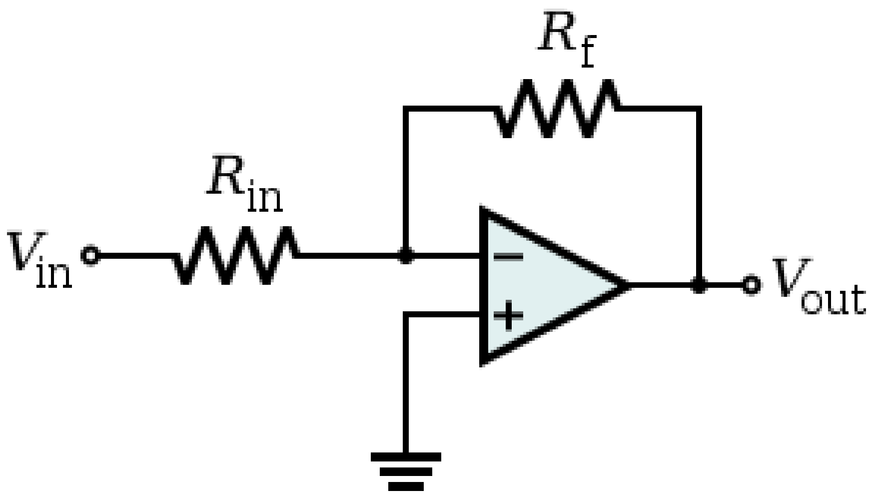
1. Introduction
2. Amplifier
3. Summer and Subtractor
4. Integrator and Differentiator
5. Active filter
6. Switched capacitor filter
7. Precision rectifier
8. Comparator
9. Schmitt Trigger
10. Oscillator
11. Sample-and-Hold

Introduction

As we know that the term operational amplifier is presently applied to a general class of high-gain, direct coupled, monolithic integrated circuit amplifiers. These Op Amps can be easily used in many applications such as inverting, non-inverting, and differential amplifiers, summer, integrator, differentiator, filter, comparator, and etc.

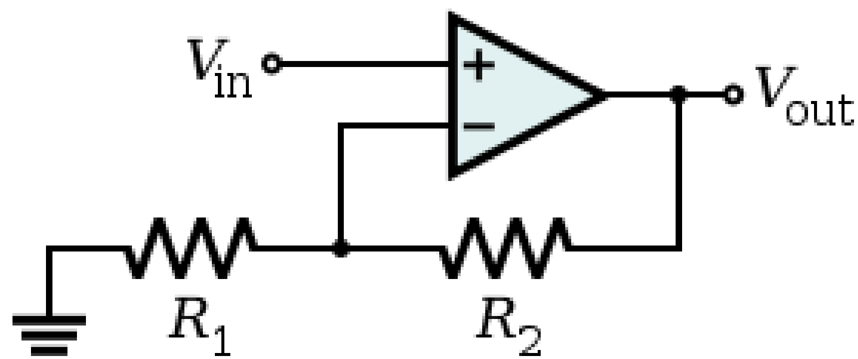


Amplifier



$$V_{\text{out}} = -V_{\text{in}}(R_{\text{f}}/R_{\text{in}})$$

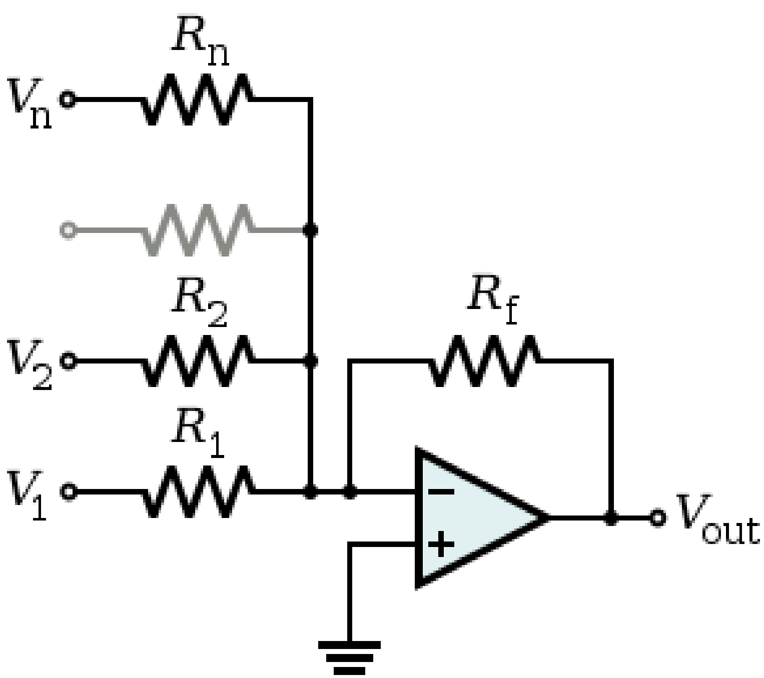
Inverting configuration



$$V_{\text{out}} = V_{\text{in}}\left(1 + \frac{R_2}{R_1}\right)$$

Non-inverting configuration

Summer and Subtractor



Summer

$$V_{out} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots + \frac{V_n}{R_n}\right)$$

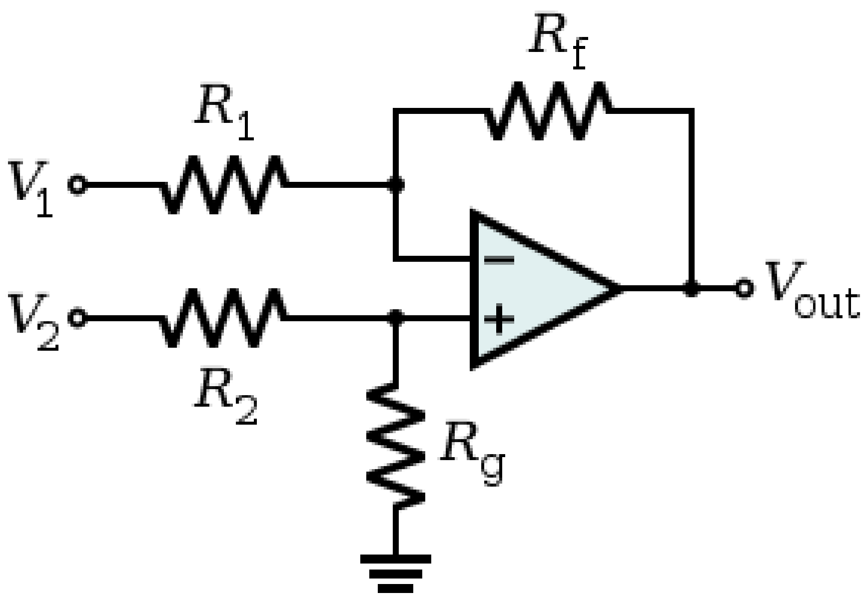
When $R_1 = R_2 = \ldots = R_n$, *and* R_f independent

$$V_{out} = -\frac{R_f}{R_1}(V_1 + V_2 + \cdots + V_n)$$

When $R_1 = R_2 = \ldots = R_n = R_f$

$$V_{out} = -(V_1 + V_2 + \cdots + V_n)$$

Summer and Subtractor



Subtractor

$$V_{out} = V_2 \left(\frac{(R_f + R_1)\, R_g}{(R_g + R_2)\, R_1} \right) - V_1 \left(\frac{R_f}{R_1} \right)$$

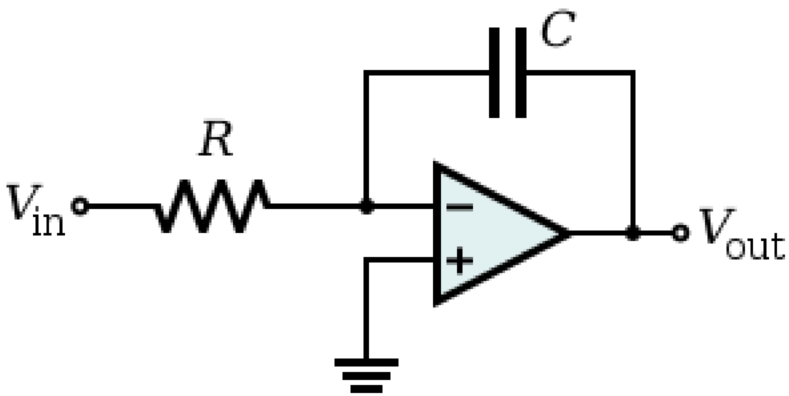
When $R_1 = R_2$ and $R_g = R_f$

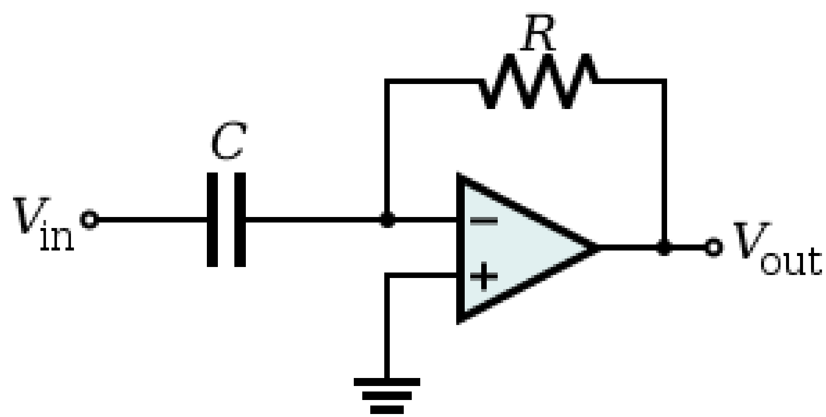
$$V_{out} = \frac{R_f}{R_1}(V_2 - V_1)$$

When $R_1 = R_f$ and $R_2 = R_g$

$$V_{out} = (V_2 - V_1)$$

Integrator and Differentiator





$$V_{\mathrm{out}} = -\int_0^t \frac{V_{\mathrm{in}}}{RC}\,\mathrm{d}t + V_{\mathrm{initial}}$$

$$V_{out} = -RC\frac{dV_{in}}{dt}$$

Integrator

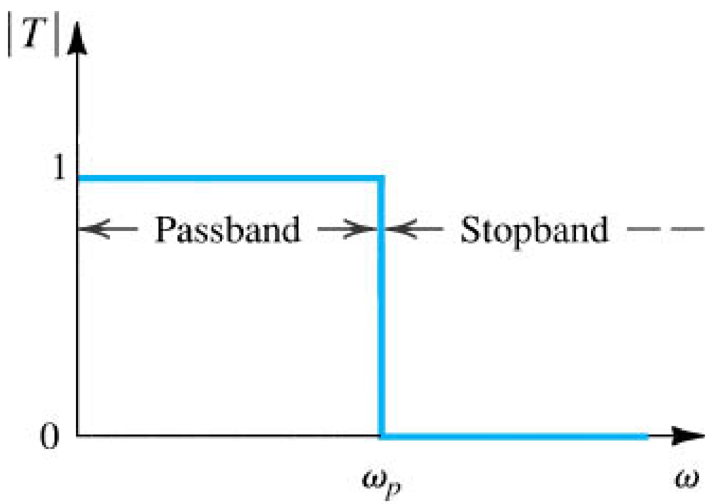
Differentiator

Active Filter

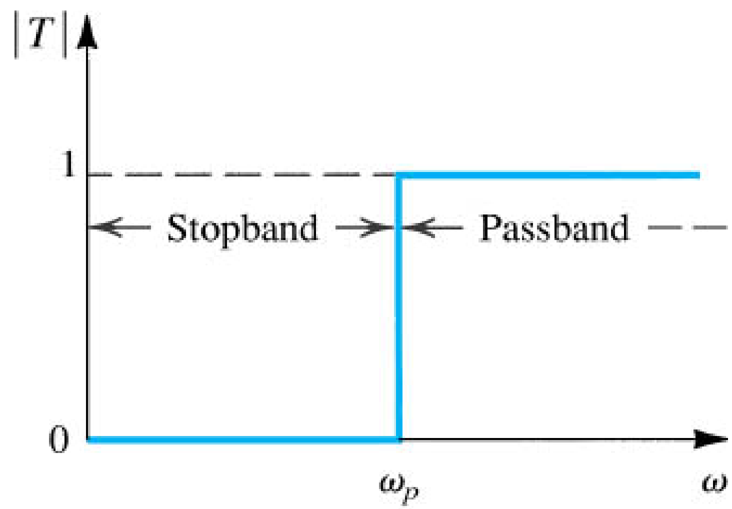
A filter separates signal from additive noise or competing signals by selectively passing the desired frequencies while attenuating undesired frequencies. The active-RC filters and switched-capacitor (SC) filters make use of op amp. Most integrated monolithic filters are based on switched-capacitor technique.

Active Filter

Frequency selection function: Passband (unity transmission); Stopband (zero transmission). Low-pass (LP), high-pass (HP), bandpass (BP) and bandstop (BS).



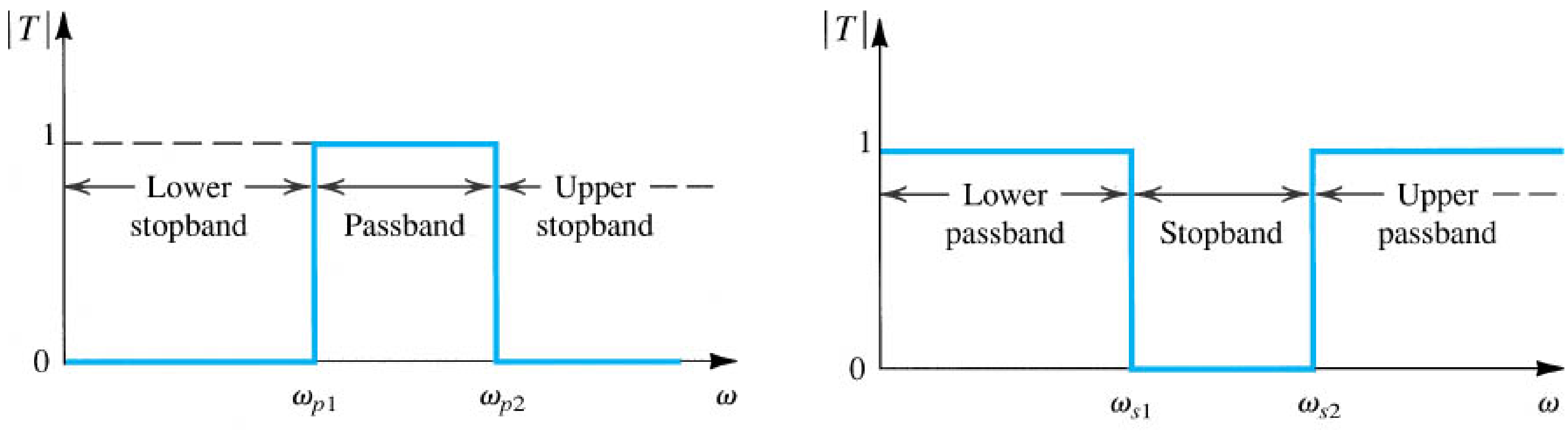
(a) Low-pass (LP)



(b) High-pass (HP)

Active Filter

These idealized features as demonstrated in the vertical edges are known as brick-wall responses. Can never be realized with physical circuits.



(c) Bandpass (BP) (d) Bandstop (BS)

Active Filter

The 4 main parameters:

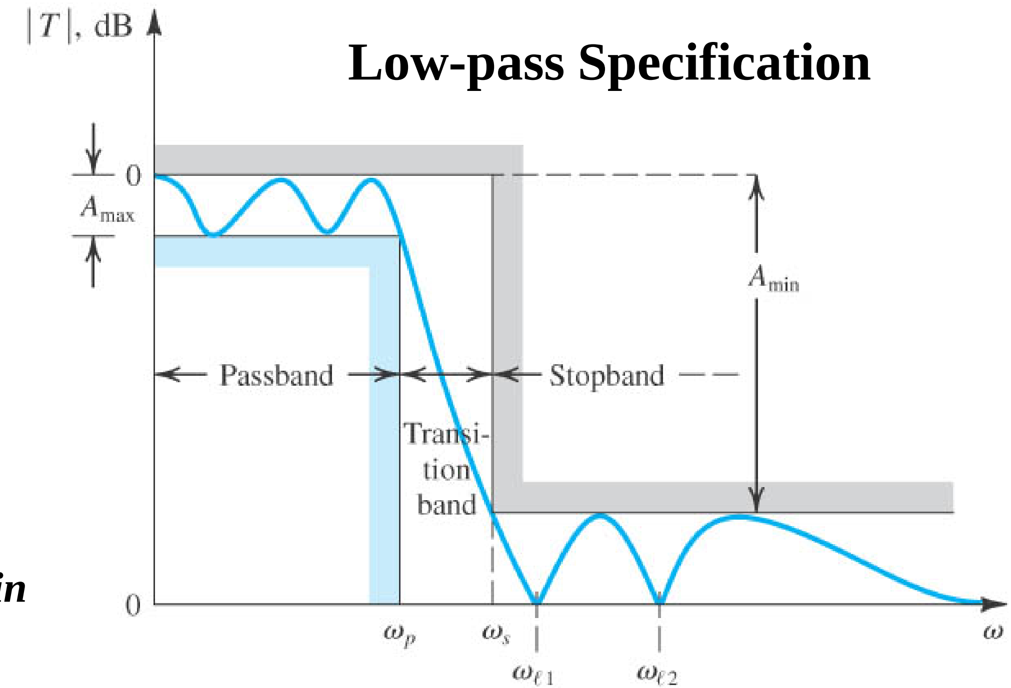
Passband edge: ω_p

Max. passband ripple: A_{max}

Stopband edge: ω_s

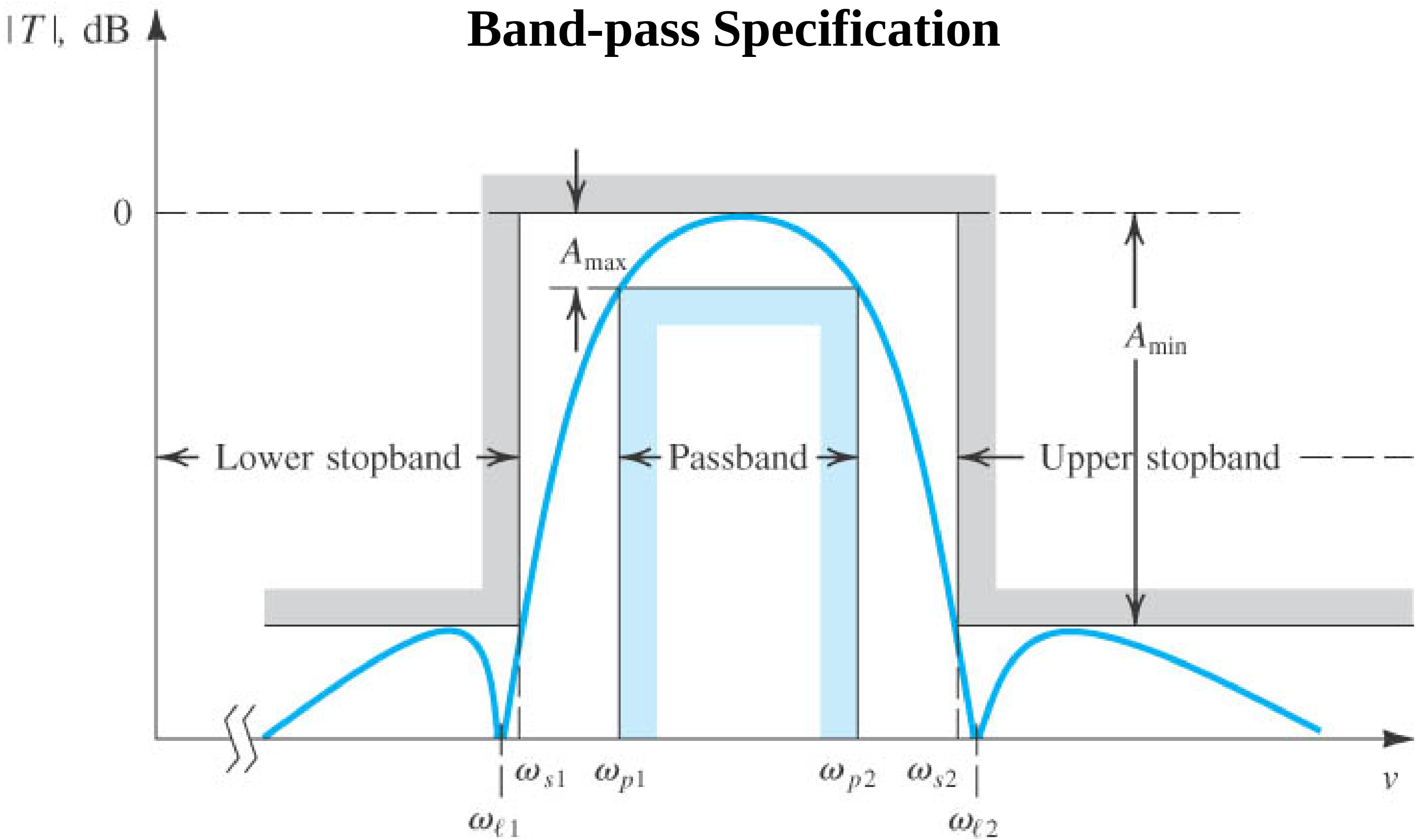
Min. stopband attenuation: A_{min}

Low-pass Specification



Active Filter

Band-pass Specification



Active Filter

The filter transfer function $T(s)$ can be written as a ratio of two polynomials:

$$T(s) = \frac{a_M s^M + a_{M-1} s^{M-1} + \cdots + a_0}{s^N + b_{N-1} s^{N-1} + \cdots + b_0}$$

The degree of denominator, N, is the filter order. For filter to be stable, $M \leq N$. The coefficients $a_0, a_1, \ldots, a_M$ and $b_0, b_1, \ldots, b_{N-1}$ are real numbers.

Active Filter

The polynomials can be factored and $T(s)$ can also be expressed as:

$$T(s) = \frac{a_M(s-z_1)(s-z_2)\cdots(s-z_M)}{(s-p_1)(s-p_2)\cdots(s-p_N)}$$

The numerator roots, z_1, z_2,…, z_M, are the transfer function zeros or transmission zeros. The denominator roots, p_1, p_2,…, p_M, are the transfer function poles or natural modes. For filter to be stable, all poles must lie in the left half of the s plane.

Active Filter

Example 1: A fourth-order filter has zeros ±*j*2. The poles are -0.6±*j*0.8 and -0.9±*j*1.2. The dc gain is 8. Find *T*(*s*).

From the given information,

$$T(s)=\frac{a_2(s+j2)(s-j2)}{(s+0.6-j0.8)(s+0.6+j0.8)(s+0.9-j1.2)(s+0.9+j1.2)}$$

$$=\frac{a_2(s^2+4)}{(s^2+1.2s+1)(s^2+1.8s+1.5)}$$

Active Filter

At dc, ω=0 and solving for dc gain=8 we have:

$$T(s=0)=\frac{a_2(0+4)}{(0+0+1)(0+0+1.5)}=8\Rightarrow a_2=3$$

Hence the overall transfer function *T*(*s*) is:

$$T(s)=\frac{3(s^2+4)}{(s^2+1.2s+1)(s^2+1.8s+1.5)}$$

Active Filter

The general first-order filter transfer function is given by:

$$T(s) = \frac{a_1 s + a_0}{s + \omega_0}$$

Pole at s=-ω_0 and transmission zero at s=-a_0/a_1. The high frequency gain approaches a_1. The numerator coefficients a_1 and a_0 determine whether the filter is low pass or high pass.

The general second-order filter transfer function is given by:

$$T(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + (\omega_0 / Q)s + \omega_0^2}$$

Active Filter

The numerator coefficients a_2, a_1 and a_0 determine the filter types.

If $a_2=a_1=0$ and $a_0\neq0 \rightarrow$ low-pass filter.

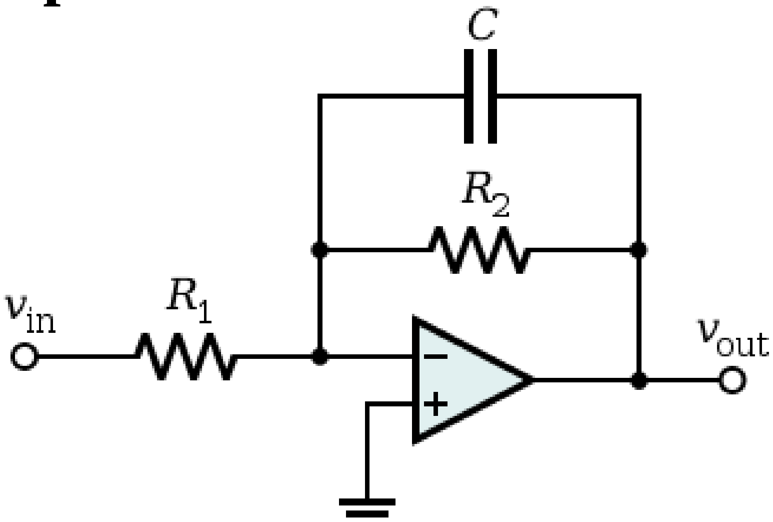
If $a_1=a_0=0$ and $a_2\neq0 \rightarrow$ high-pass filter.

If $a_2=a_0=0$ and $a_1\neq0 \rightarrow$ band-pass filter.

We can cascade a number of first-order and/or second-order filters to realize high-order ($N\geq3$) filters. For example, to realize a 5^{th}-order filter, we can cascade a first-order and two second-order filters.

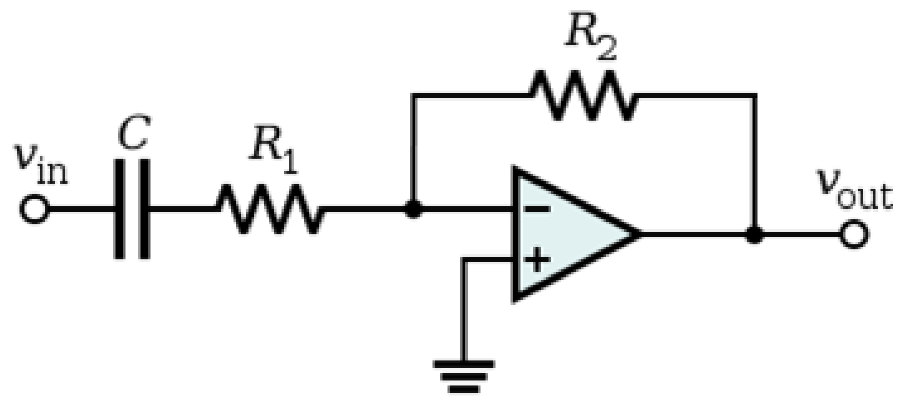
Active Filter

Implementation of the first-order active filter



$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{R_2 // \frac{1}{SC}}{R_1} = -\frac{R_2}{R_1}\frac{\omega_c}{S+\omega_c}$$

$$\omega_c = \frac{1}{R_2 C}$$

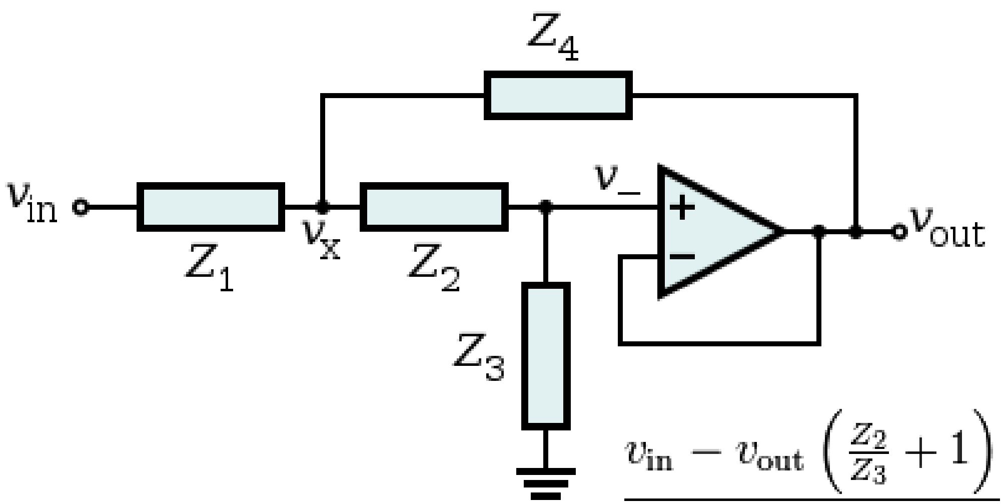


$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{R_2}{R_1 + \frac{1}{SC}} = -\frac{R_2}{R_1}\frac{S}{S+\omega_c}$$

$$\omega_c = \frac{1}{R_1 C}$$

Active Filter

Implementation of the second-order active filter



$$\frac{v_{in}-v_x}{Z_1}=\frac{v_x-v_{out}}{Z_4}+\frac{v_x-v_{out}}{Z_2}$$

$$\frac{v_x-v_{out}}{Z_2}=\frac{v_{out}}{Z_3},\ v_x=v_{out}\left(\frac{Z_2}{Z_3}+1\right).$$

$$\frac{v_{in}-v_{out}\left(\frac{Z_2}{Z_3}+1\right)}{Z_1}=\frac{v_{out}\left(\frac{Z_2}{Z_3}+1\right)-v_{out}}{Z_4}+\frac{v_{out}\left(\frac{Z_2}{Z_3}+1\right)-v_{out}}{Z_2}.$$

$$v_+=v_-=v_{out}.$$

$$\frac{v_{in}-v_x}{Z_1}=\frac{v_x-v_{out}}{Z_4}+\frac{v_x-v_-}{Z_2}.$$

$$\frac{v_{out}}{v_{in}}=\frac{Z_3Z_4}{Z_1Z_2+Z_4(Z_1+Z_2)+Z_3Z_4},$$

Active Filter

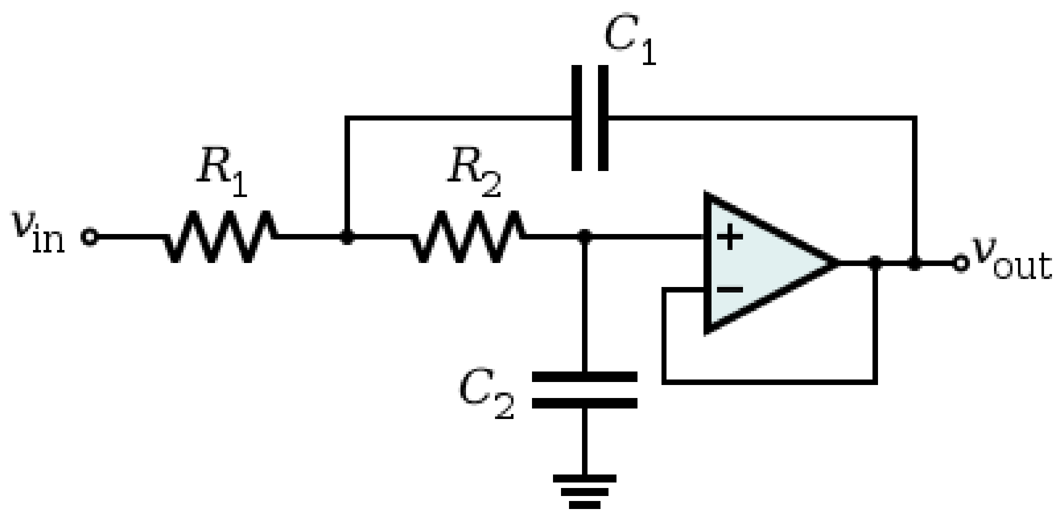
Implementation of the second-order active filter

Let $Z_1 = R_1$

$Z_2 = R_2$

$Z_3 = \dfrac{1}{SC_2}$

$Z_4 = \dfrac{1}{SC_1}$



$$T(s) = \frac{V_{out}}{V_{in}} = \frac{\omega_0^2}{s^2 + (\omega_0 / Q)s + \omega_0^2} \qquad Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2 (R_1 + R_2)} \qquad \omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

It is the second-order Sallen-Key low-pass filter.

Active Filter

Implementation of the second-order active filter

Let $Z_1 = \frac{1}{SC_1}$ $Z_2 = \frac{1}{SC_2}$ $Z_3 = R_2$ $Z_4 = R_1$

We have $T(s) = \frac{V_{out}}{V_{in}} = \frac{s^2}{s^2 + (\omega_0 / Q)s + \omega_0^2}$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 (C_1 + C_2)} \qquad \omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

Swap R_1 and C_1 positions as well as R_2 and C_2 positions, the filter changes from low-pass to high-pass.

Switched-Capacitor Filter

Disadvantages of active-RC filter circuits:

Need for large value capacitors

Requirement of accurate RC time constants

Active-RC filter is impractical for monolithic IC implementation.

Switched-capacitor circuits could overcome these disadvantages.

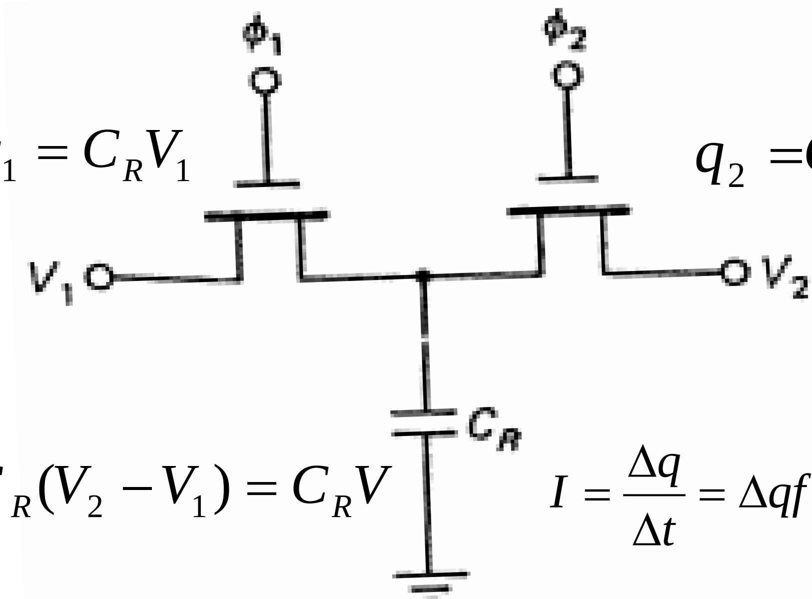
Switched-Capacitor Filter

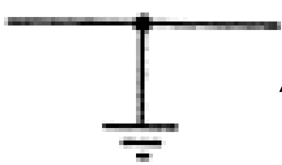
The idea: a capacitor switched between two circuit nodes at a sufficiently high rate is equivalent to a resistor connecting these two nodes.

$$R = \frac{1}{fC_R}$$

$$\equiv$$

$$q_1 = C_R V_1 \qquad q_2 = C_R V_2$$



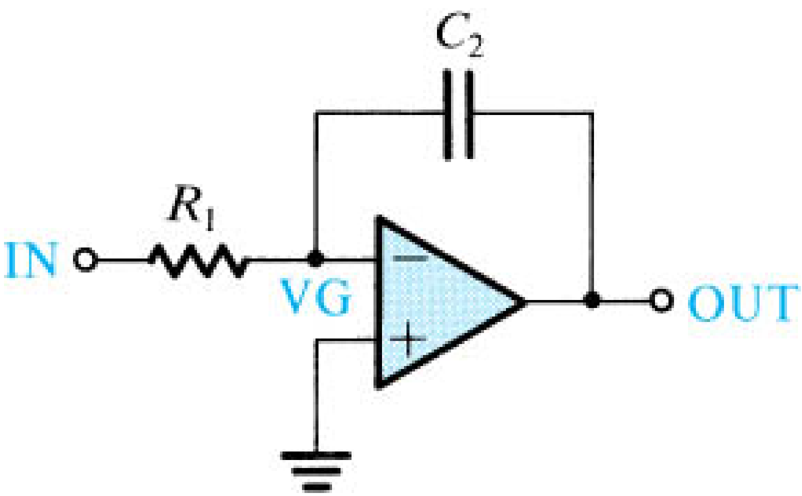


$$\Delta q = q_2 - q_1 = C_R(V_2 - V_1) = C_R V$$

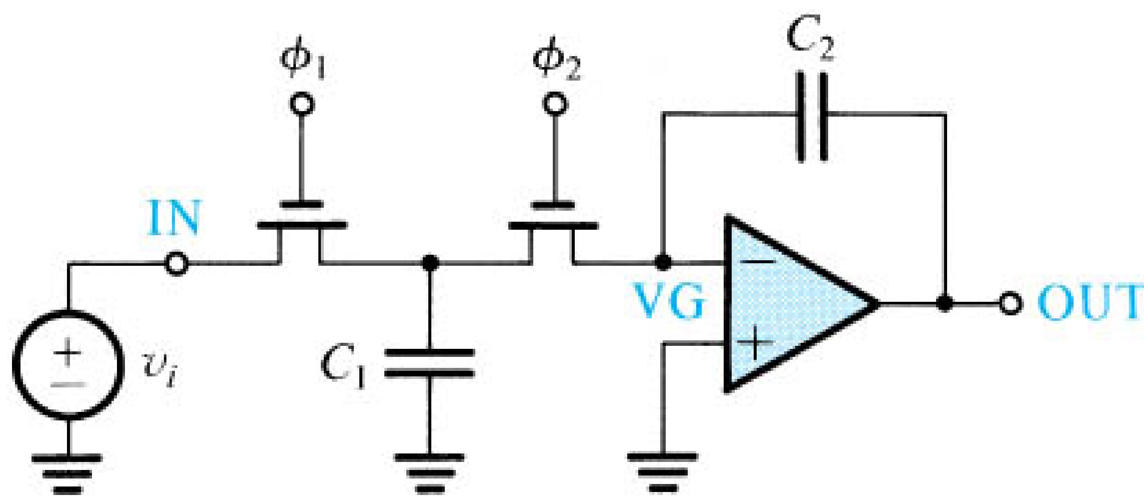
$$I = \frac{\Delta q}{\Delta t} = \Delta q f = C_R V f$$

Switched-Capacitor Filter

Consider an active-RC integrator: R_1 is replaced by C_1 together with two MOS transistors acting as switches.



(a)

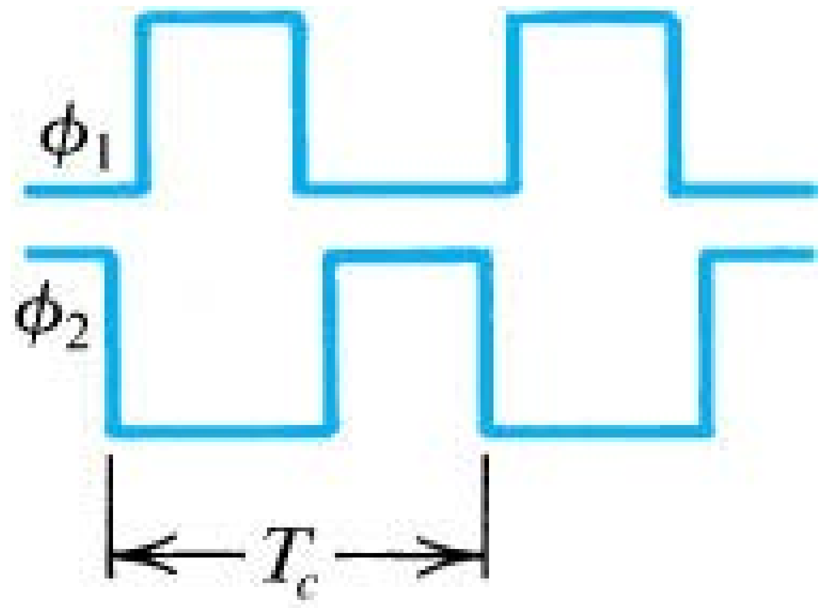


(b)

Switched-Capacitor Filter

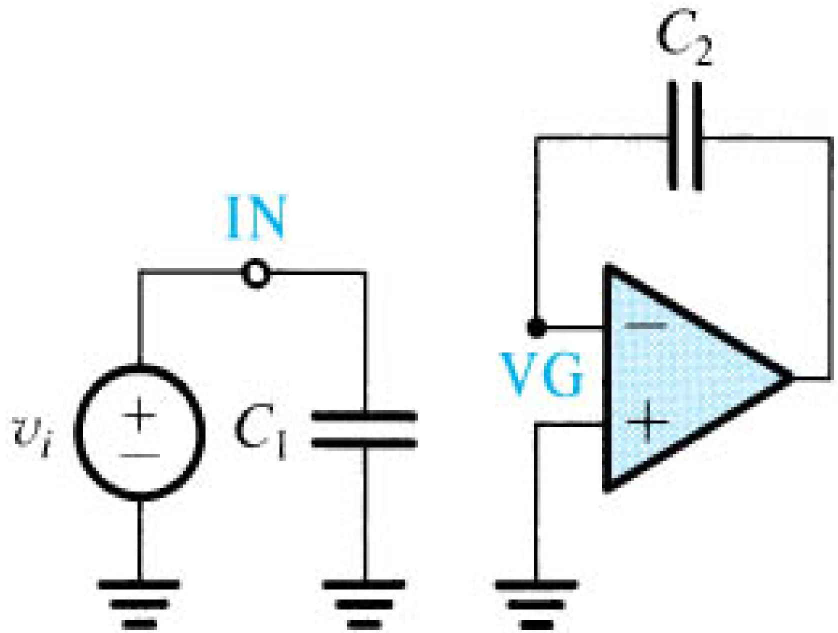
The two MOS switches are driven by a *non-overlapping* two-phase clock.

The clock frequency f_C (f_C=1/T_C) is much higher than the signal bandwidth. When the clock signal applied to the gate terminal of MOS is high, the MOS switch is "ON", else it is "OFF".



Switched-Capacitor Filter

During clock phase ϕ_1, the variations in v_i connected across C_1 is negligibly small. C_1 is charged to the voltage v_i: $q_{C1} = C_1 v_i$

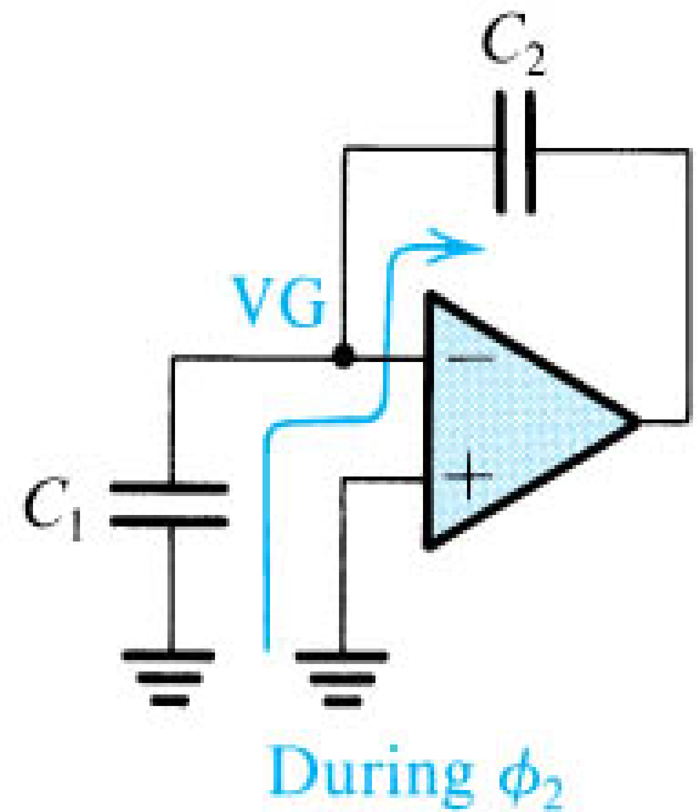


During ϕ_1

Switched-Capacitor Filter

During clock phase ϕ_2, C_1 is connected to the virtual ground input of op amp.

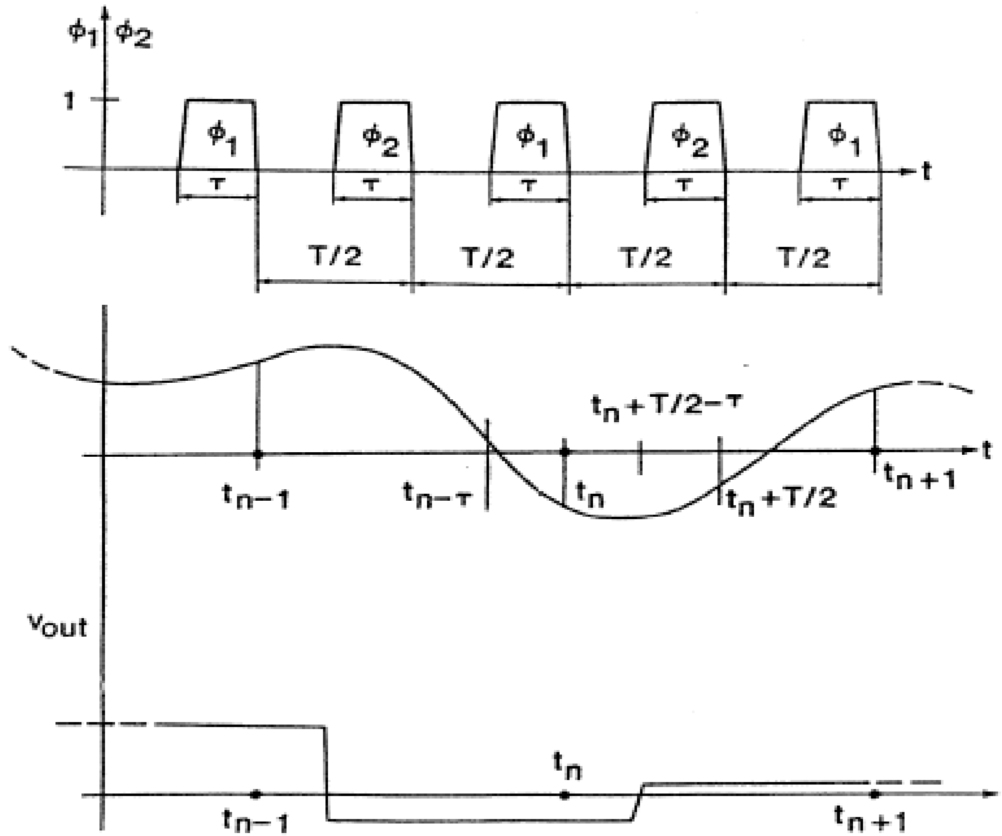
C_1 is thus discharged and its previous stored charge q_{C1} is transferred to C_2, in the direction indicated.



Switched-Capacitor Filter

The input could be a continuous time signal.

The output is a sampled-data signal which only changes at the beginning of ϕ_2 when charge transfer takes place.



Switched-Capacitor Filter

During each clock period T_C an amount of charge $q_{C1}= C_1 v_i$ is transferred from the input source to the integrator capacitor C_2.

Hence the average current flowing between the input node (IN) and the virtual ground node (VG) is: $i_{av} = C_1 v_i / T_c$.
If T_C is sufficiently short, the charge transfer is almost continuous and we can define an equivalent resistance R_{eq} that is in effect present between nodes IN and VG as: $R_{eq} = T_c / C_1$.
The equivalent time constant for the integrator: $R_{eq} C_2$.

Switched-Capacitor Filter

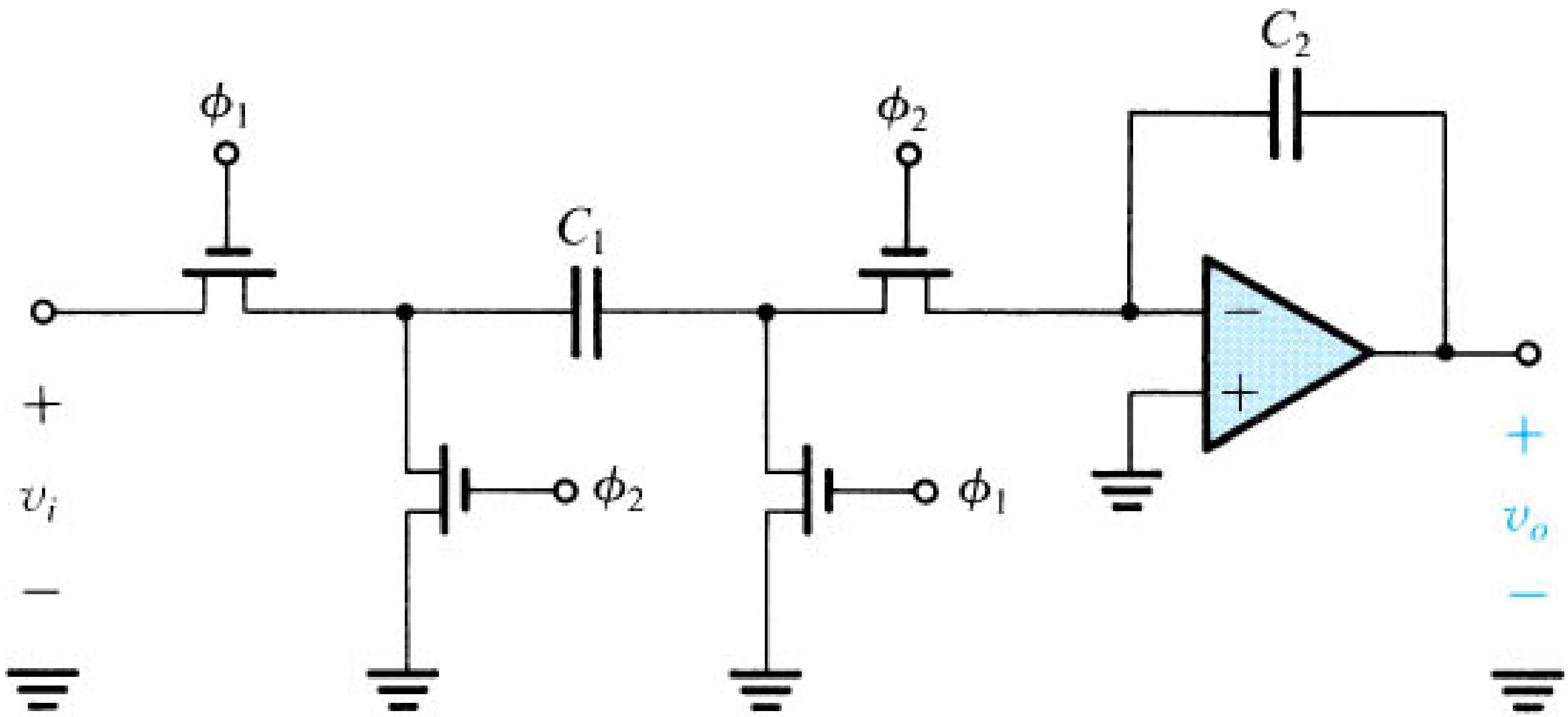
Thus the time constant that determines the frequency response of a filter is governed by the clock period T_C and the capacitor ratio C_2/C_1.

Both these parameters can be well controlled in an IC process.

The accuracy of capacitor ratios in MOS technology can be controlled to within 0.1%.

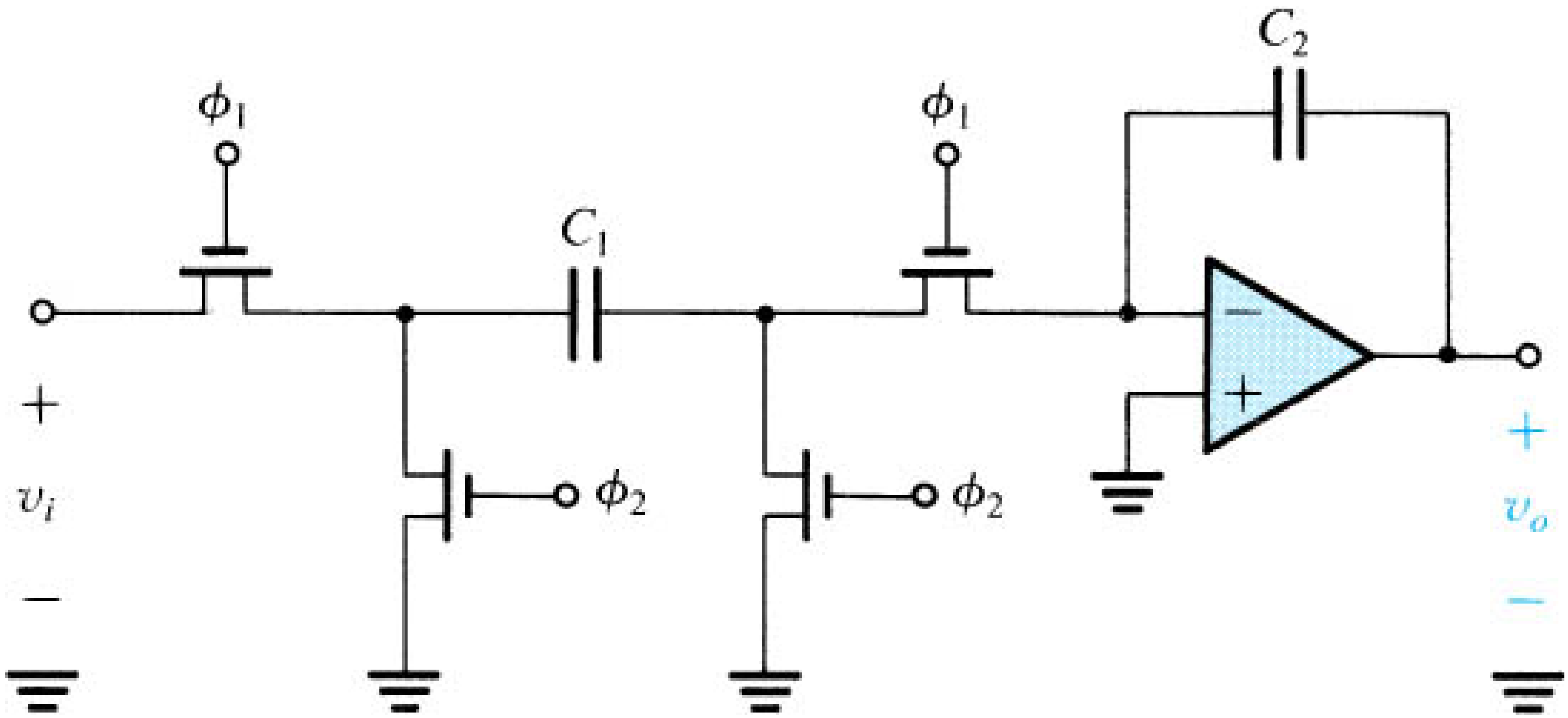
Another advantage is that large time constant can be realized with small capacitor.

Switched-Capacitor Filter



Non-inverting switched-capacitor integrator

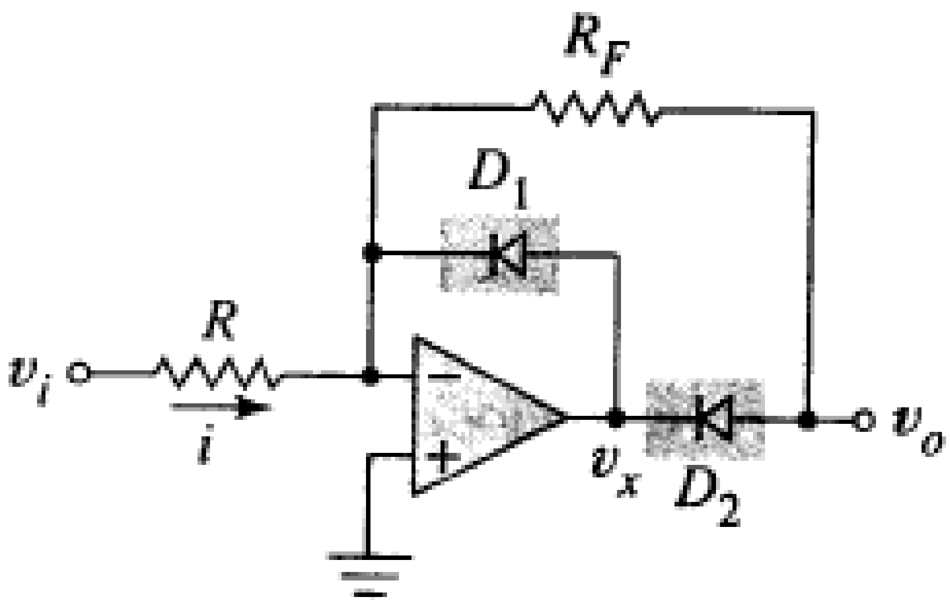
Switched-Capacitor Filter



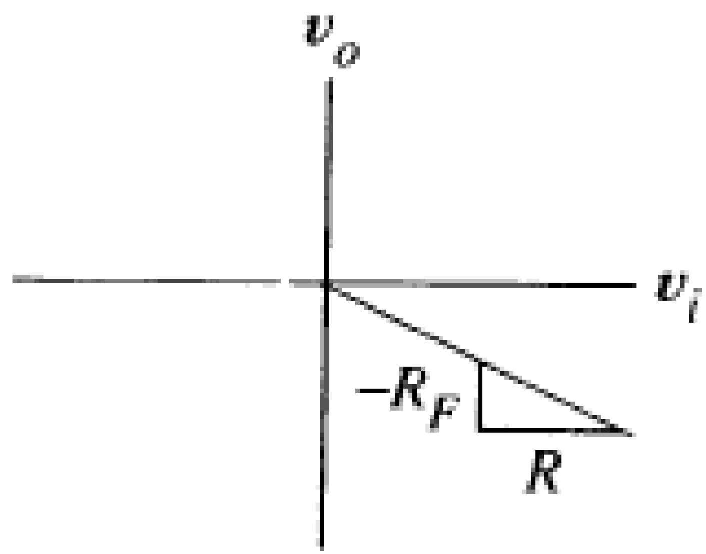
Inverting switched-capacitor integrator

Precision Rectifier

Precision Half-Wave Rectifier



Circuit



Transfer Characteristic

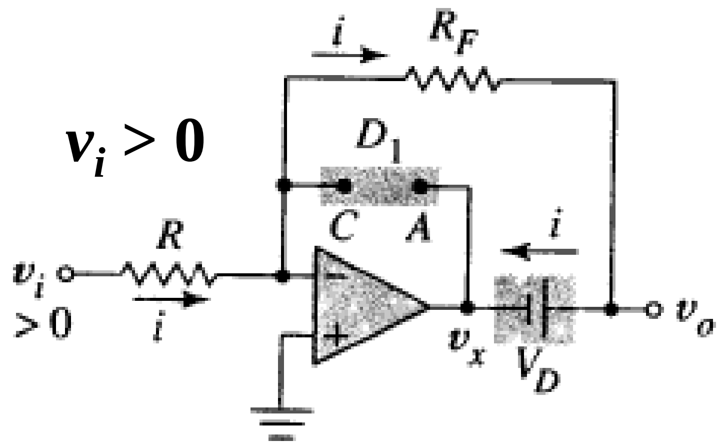
Precision Rectifier

For $v_i > 0$, current i can only flow through R_F and D_2 but not D_1.

We have

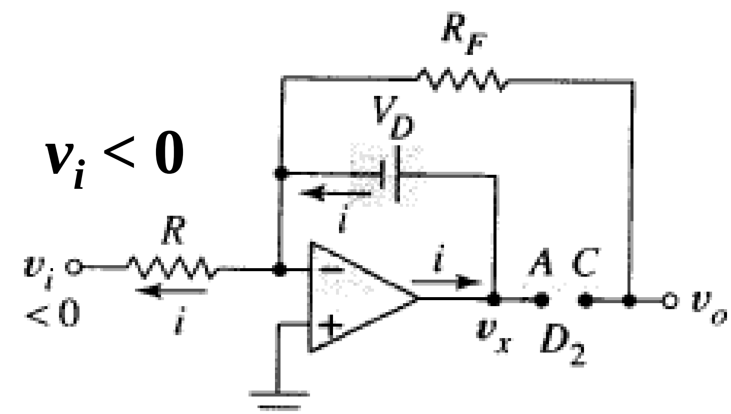
$$i = \frac{v_i - 0}{R} = \frac{0 - v_o}{R_F}$$

$$\Rightarrow v_o = -\frac{R_F}{R} v_i \quad \text{for } v_i \geq 0$$



For $v_i < 0$, D_2 turns OFF and D_1 turns ON.

The virtual ground requires that $v_o = 0$ for $v_i < 0$.

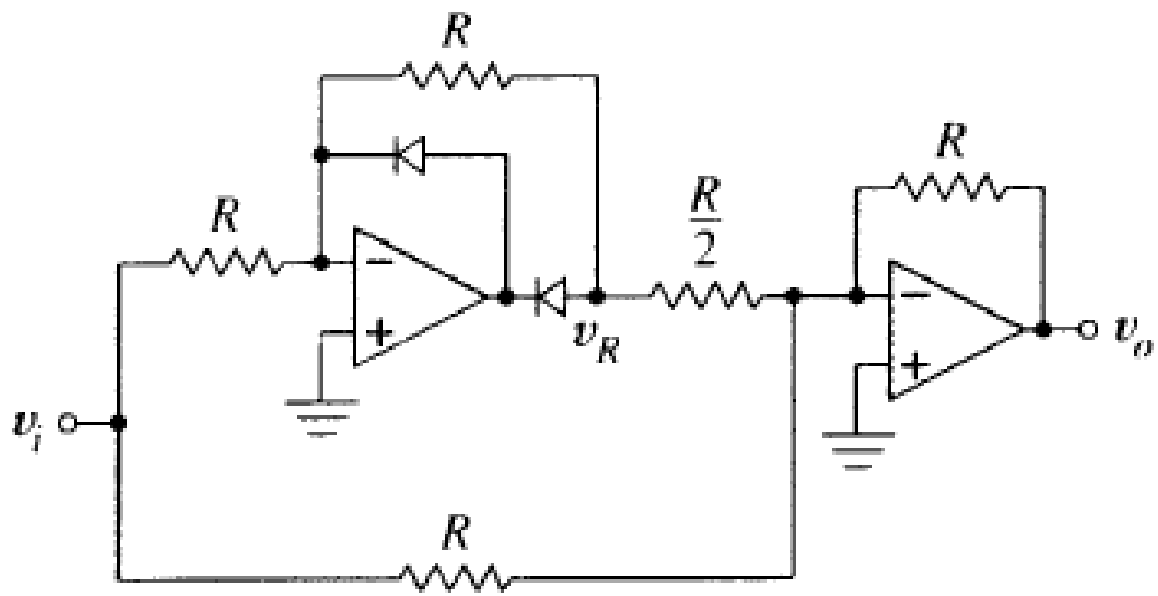


Precision Rectifier

The precision full-wave rectifier is formed by a precision half-wave rectifier and a summing amplifier.

$$\Rightarrow v_o = -(v_i + 2v_R)$$

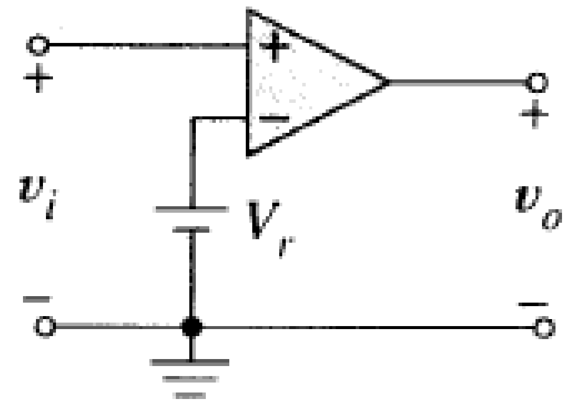
where v_R is the output of the precision half-wave rectifier



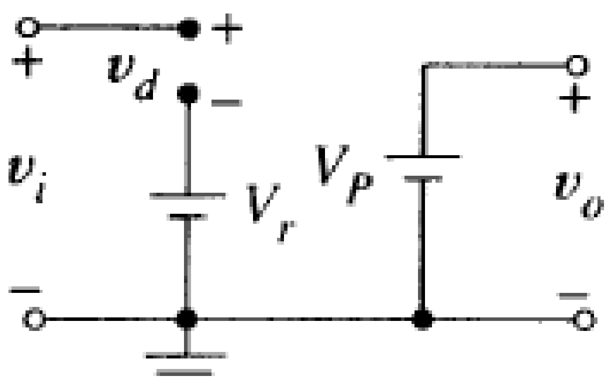
When $v_i > 0$, $v_R = -v_i$ => $v_o=-(v_i+2v_R)= v_i$

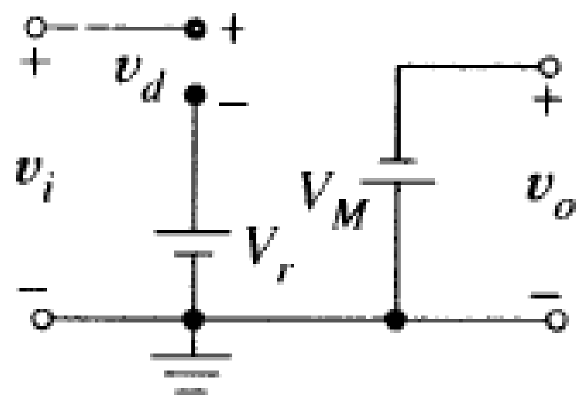
When $v_i < 0$, $v_R = 0$ => $v_o=-(v_i+2v_R)= -v_i$

Comparator



The comparator circuit compares signal $v_i(t)$ with reference voltage V_r. It produces a binary output, one value for $v_i(t)>V_r$ and another for $v_i(t)<V_r$. $v_d=v_i-V_r$





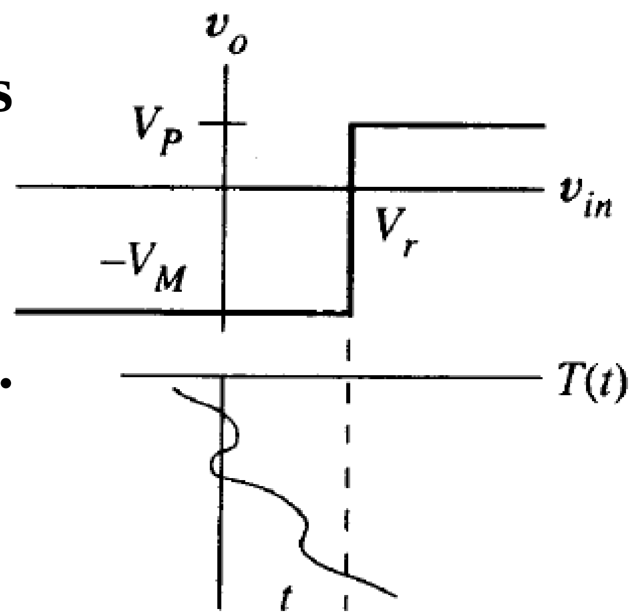
When $v_i>V_r$, $v_d>0$ the output is V_P, the positive saturation of op amp.

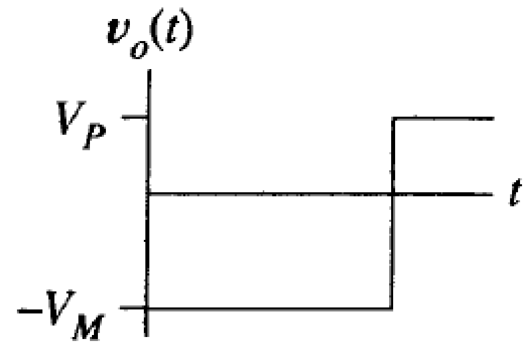
When $v_i<V_r$, $v_d<0$ the output is $-V_M$, the negative saturation of op amp.

Comparator

The comparator extracts binary information from its analog input. One possible application is the temperature warning system shown in this figure.

In comparator circuit op amp is used in open-loop mode => non-linear.

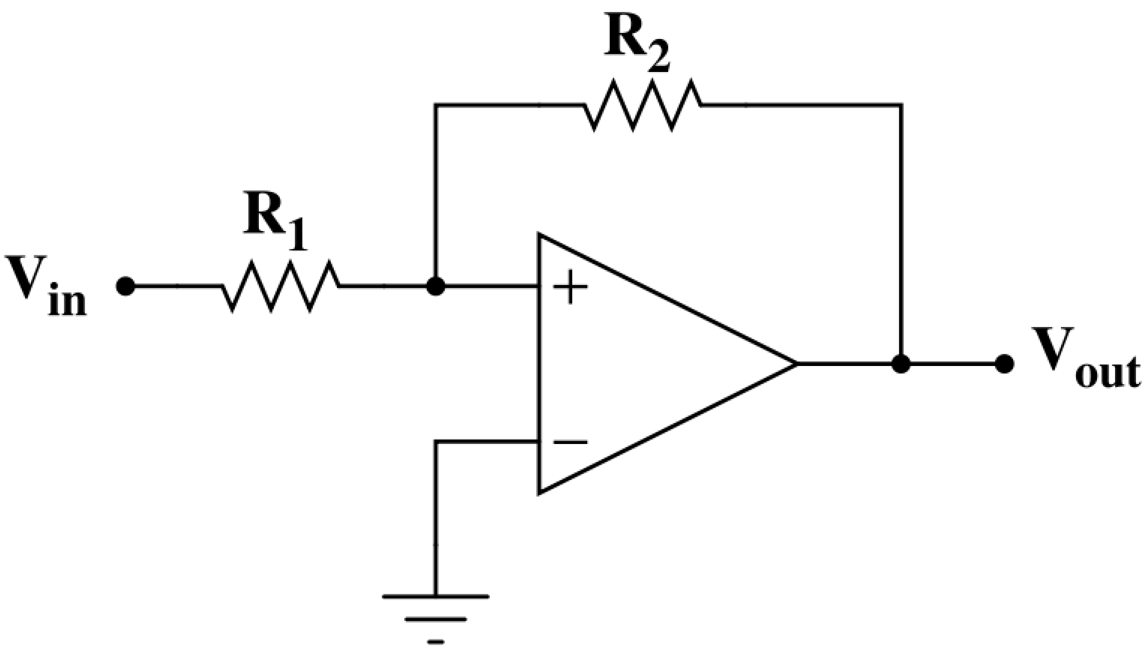




In some applications high slew rate is important to ensure rapid transitions.

Schmitt Trigger

Invented by Otto Schmitt, a biomedical engineer. The circuit employs positive feedback.



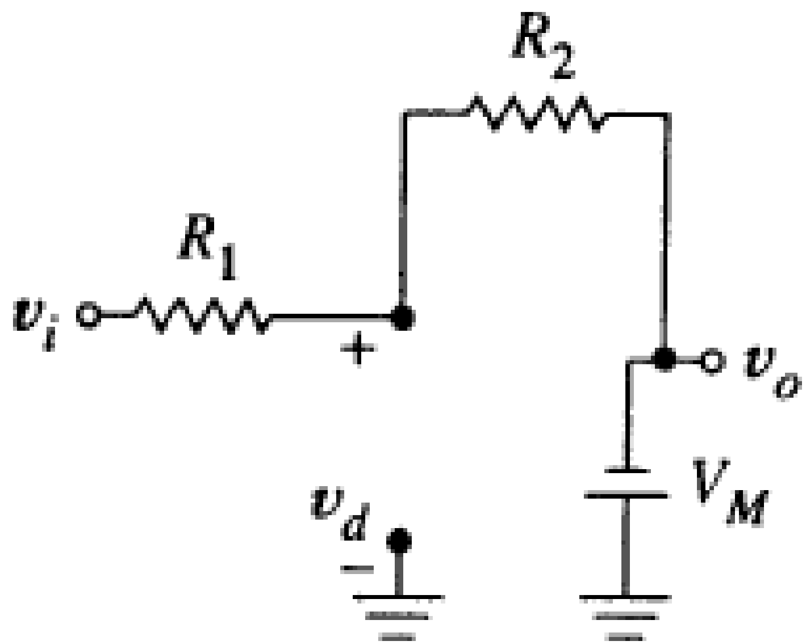
Schmitt Trigger

Assuming v_i is very negative, then v_d<0 and output saturates at $-V_M$. By superposition,

$$v_d = \frac{R_2}{R_1 + R_2} v_i + \frac{R_1}{R_1 + R_2}(-V_M)$$

This implies that v_i must attain some +ve value before v_d goes positive. By setting v_d=0, we obtain the critical value as

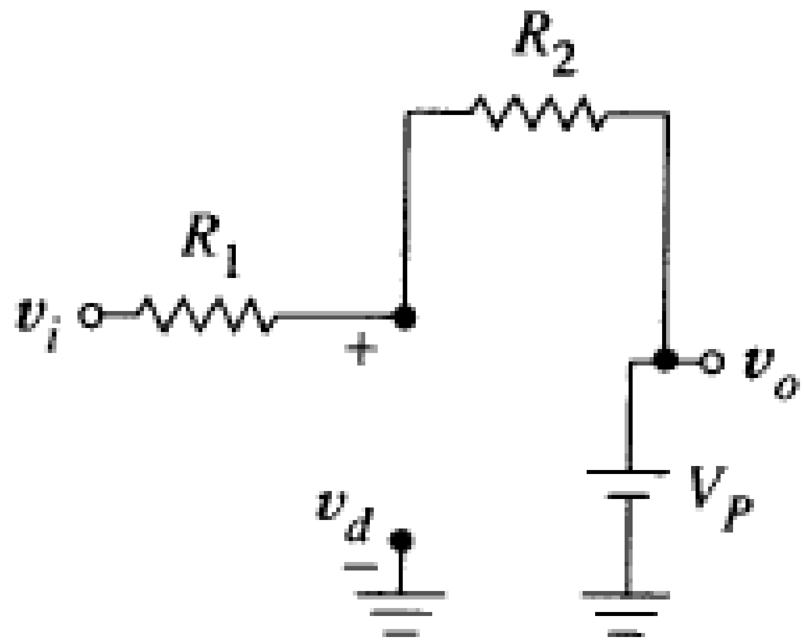
$$v_i = \frac{R_1}{R_2} V_M = v^+$$



Schmitt Trigger

Once $v_i > v^+$, v_o=-$V_M \rightarrow V_P$, i.e. op amp changes state to that as shown on the right. Now v_d is given by:

$$v_d = \frac{R_2}{R_1 + R_2} v_i + \frac{R_1}{R_1 + R_2} (V_P)$$

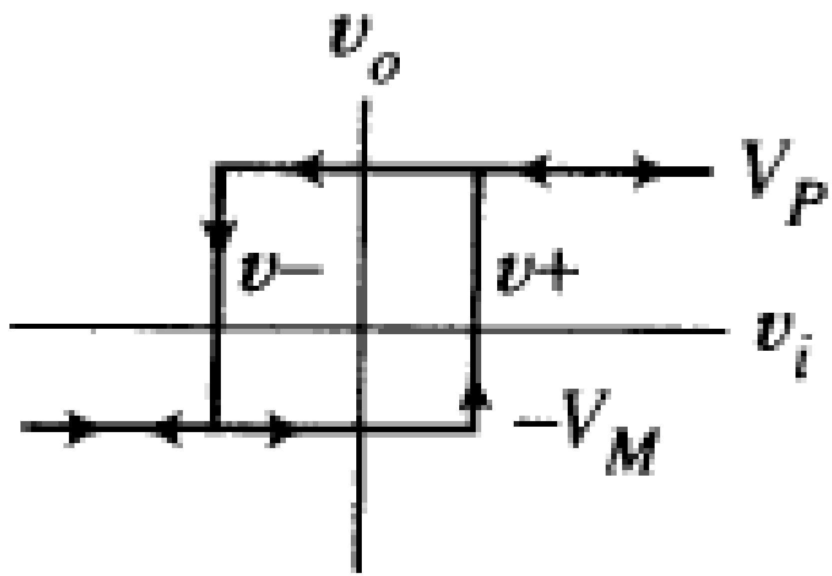


This implies that v_i must attain some -ve value before v_d goes –ve. By setting v_d=0, we obtain the critical value as

$$v_i = -\frac{R_1}{R_2} V_P = v^-$$

Schmitt Trigger

The transfer characteristic of the circuit is as shown. In effect, the circuit has memory. The Schmitt circuit is a comparator with hysteresis. The width of hysteresis region is



$$W = v^+ - v^- = \frac{R_1}{R_2}\left(V_P + V_M\right)$$

Schmitt Trigger

The width of the hysteresis region can be determined by the ratio of R_1 and R_2. By adding a positive reference V_R between the inverting node and the ground, the transfer characteristic can be shifted to the right by

$$\left(\frac{R_1 + R_2}{R_2}\right)V_R$$

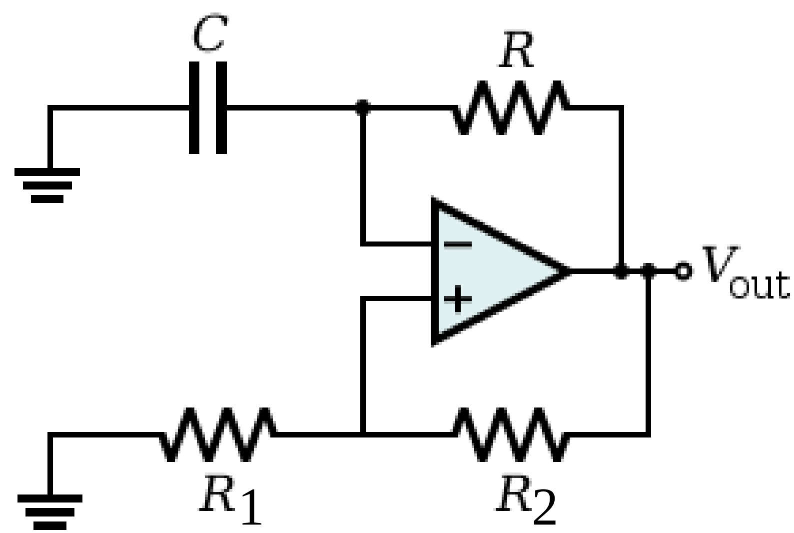
while the hysteresis W remains the same. Adding a negative reference V_R shift the transfer characteristic can be shifted to the left.

Oscillator

A square-wave oscillator can be built using an integrator plus a comparator with controlled hysteresis. The period of the oscillator output is given as:

$$T = 2RC\ln\left(\frac{1+B}{1-B}\right)$$

where $$B = \frac{R_1}{R_1 + R_2}$$

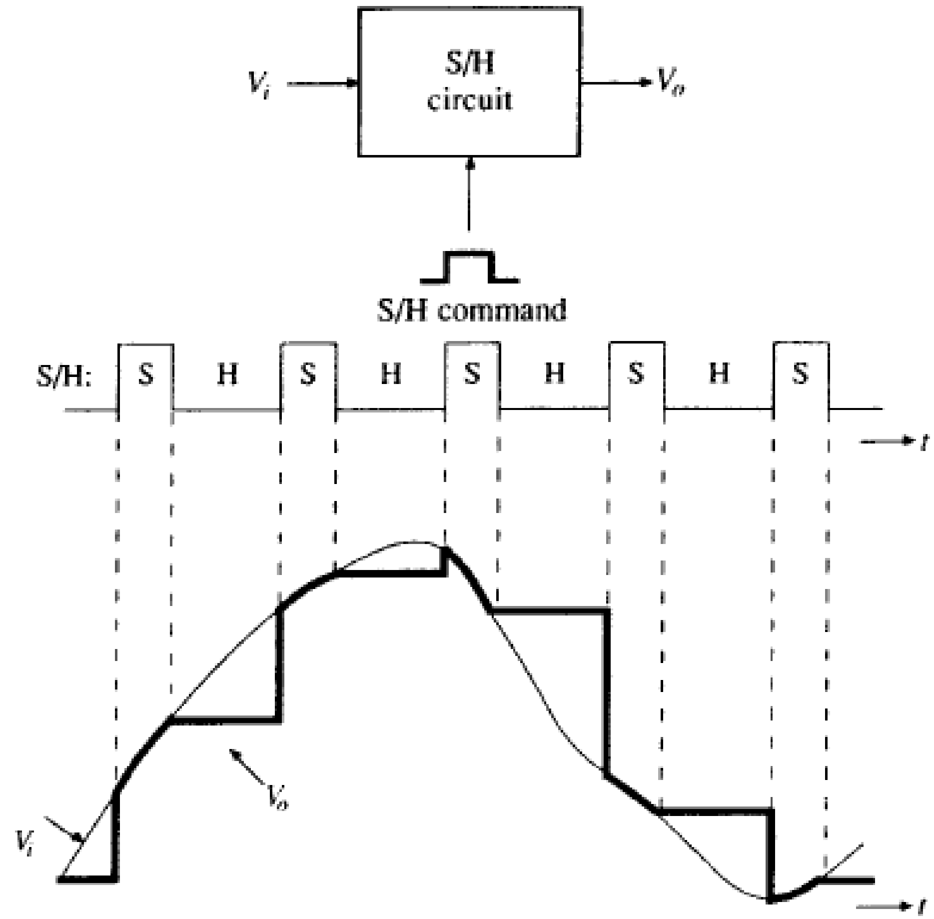


Oscillator

Sample-and-Hold

The function of a S/H circuit is to capture the value of the input signal in response to a sampling command and hold it at the output until the arrival of the next command.

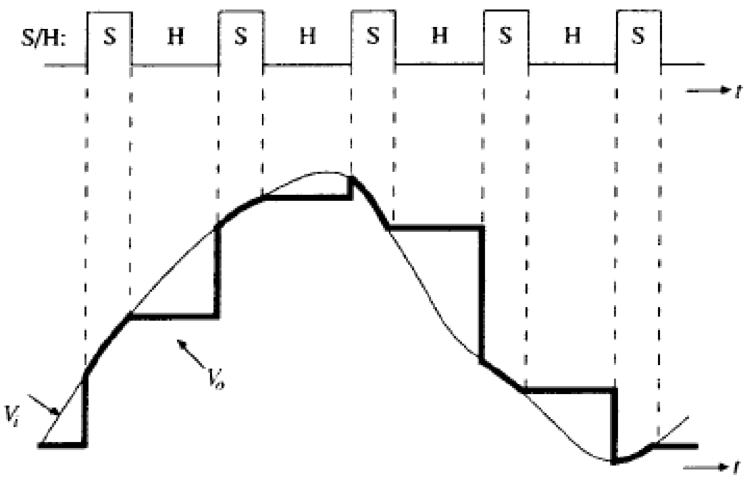
The figures depict the block diagram and the idealized response.



Sample-and-Hold

Track mode: Once S/H command is received, the circuit swings V_o towards V_i and then forces V_o to track or follow V_i for the remainder of the pulse.

Hold mode: After the S/H pulse is removed, the circuit holds V_o at the value V_i had at the instant of pulse deactivation.



Sample-and-Hold

The most popular S/H configuration.
During the sampling interval, the driver closes the switch, and

$V_o = V_i$

At the end of the sampling interval, the driver opens the switch, and $V_o = V_{CH}$ = value of V_i at the instant of switch.