

NANYANG TECHNOLOGICAL UNIVERSITY**SEMESTER 2 EXAMINATION 2020-2021****EE3013 – SEMICONDUCTOR DEVICES AND PROCESSING**

April / May 2021

Time Allowed: 2 hours

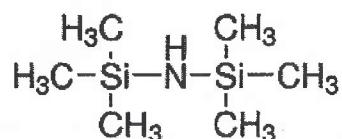
INSTRUCTIONS

1. This paper contains 4 questions and comprises 8 pages.
 2. Answer all 4 questions.
 3. All questions carry equal marks.
 4. This is a closed book examination.
 5. A List of Selected Formulae and a Table of Physical Constants are provided in Appendices A and B on pages 6 - 8.
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1. (a) In photolithography when people say their photoresist has “opposite polarity” to the pattern obtained, what does that mean? Sketch and explain the process.

(6 Marks)

- (b) Explain why hexa-methyl-di-silazane (HMDS) primer coated on Si surface can make the Si surface more hydrophobic. The molecular structure of HMDS is shown in Figure 1.

**Figure 1**

(6 Marks)

Note: Question No. 1 continues on page 2.

- (c) A dry Step-and-Scan Exposure system designed to use in air was fitted with an ArF 193 nm DUV excimer laser as the light source. The Numerical Aperture of the exposure lens was $NA_{dry} = 0.68$. Note : $NA = n \sin \theta$, where θ is the exit angle of the lens.

The exposure system was then retrofitted with a Deionized Water Immersion stage without changing the lens column. Assume that the NA in the immersion system did not change, $NA_{wet} = 0.68$. The refractive index of Deionized water $n = 1.437$ for the ArF 193 nm DUV laser light. The final wet process parameters were: k_1 (wet) = 0.45 and k_2 (wet) = 0.65.

Calculate the Exit Angle for the wet immersion system. Calculate the Resolution W_{min} and Depth of Focus DOF for the wet operation of the exposure system.

(8 Marks)

- (d) In order to obtain high quality uniform thin films in cases (i), (ii) and (iii) below, choose the appropriate deposition methods: thermal evaporation, DC sputtering, Low Pressure Chemical Vapour Deposition (LPCVD). Specify the reasons for your answers.

(i) 50 nm SiO_2 film on a silicon wafer.

(ii) 500 nm tungsten film on a quartz slide.

(iii) 200 nm titanium film on a stainless steel cylinder.

(5 Marks)

2. (a) Briefly discuss wet etching process on Si (100) according to Figure 2. In the figure, $\delta = 2 \mu\text{m}$ and $D = 350 \mu\text{m}$ when the etching process is stopped after 5 minutes. What are the etch rates in the $<100>$ and $<111>$ directions?

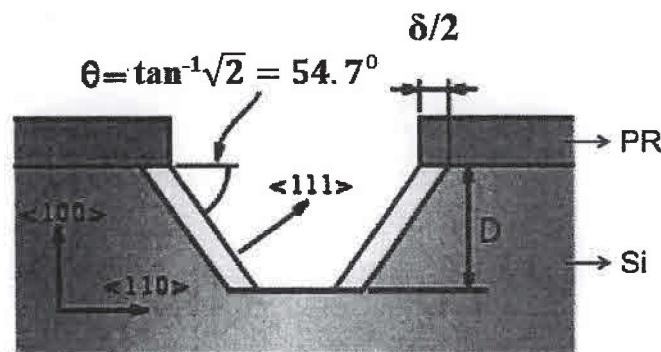


Figure 2

(7 Marks)

Note: Question No. 2 continues on page 3.

- (b) Figure 3 below illustrates a Reactive Ion Etching (RIE) system. Identify places numbered 1 through 8 and explain how the etching is done.

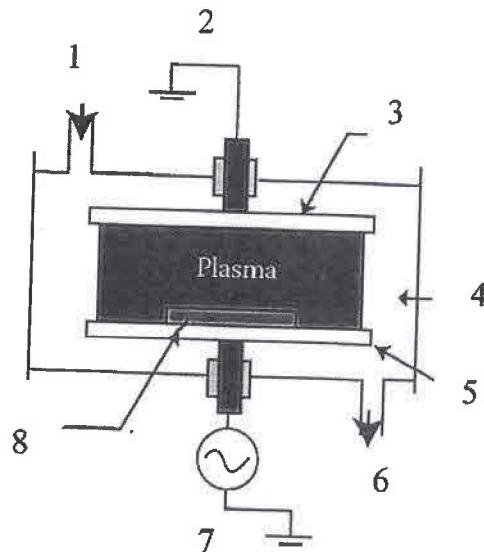


Figure 3

(6 Marks)

- (c) The high ion bombardment energy of the RIE causes damages to the material, and considerable degradation to the electrical and optical properties of devices.
- What are factors affecting the degree of the damages?
 - What are the types of the RIE plasma damages that can be inflicted on a material surface with patterned edges?
 - How could one overcome the device degradation caused by the damages?

(6 Marks)

- (d) In a sputtering deposition run, 20 sccm pure argon gas is released into the sputter chamber and the resulting sputtering pressure is 2.0 mTorr. Given the volume of the chamber is 30 litres, calculate the effective pumping needed to maintain the 2.0 mTorr sputtering pressure. Given 1 torr litre / s = 78.9 sccm.

(6 Marks)

3. (a) A Si (100) wafer has two oxide layers. The first oxide layer of 500 nm was grown by the wet oxidation process at 1000°C while the second oxide layer was grown by the dry oxidation process at 1200°C for 30 minutes. Table 1 shows the data of the oxidation processes.
- (i) Find the time required for the growth of the first oxide layer.
 - (ii) Calculate the total thickness of the two oxide layers.

Temperature (°C)	Dry Oxidation		Wet Oxidation	
	A(μm)	B(μm ² /hr)	A(μm)	B(μm ² /hr)
1000	0.165	0.0117	0.226	0.287
1100	0.090	0.0270	0.110	0.510
1200	0.040	0.0450	0.050	0.720

Table 1. Data of oxidation

(10 Marks)

- (b) A *p*-Si wafer is used to form a *p-n* junction by the thermal diffusion.
- (i) What impurity atoms should be used and how to determine the junction position?
 - (ii) What are the electron and hole concentrations at the junction position? Sketch the carrier concentration profile as a function of position.
- (6 Marks)
- (c) Consider a *n-p-n* transistor at common emitter configuration. The biased voltage between the emitter and the base is V_{be} and the biased voltage between the emitter and the collector is V_{ce} .
- (i) If the transistor is at active mode, explain why the collector current increases with the bias voltage V_{ce} . Describe the breakdown mechanism of the *n-p-n* transistor.
 - (ii) If the transistor is at saturation mode, plot the energy band diagram and the minority carrier distributions of the device. Show the expression of the minority carrier concentrations at all boundaries.
- (9 Marks)

4. (a) A *p*-Si wafer has a doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$ covered by a 300 nm thick oxide. Arsenic was implanted with a dose of $1 \times 10^{13} \text{ atoms/cm}^2$. Given $R_p = 550 \text{ nm}$ and $\Delta R_p = 120 \text{ nm}$.

- (i) Find the implanted dopant concentration at the Si/oxide interface.
- (ii) Calculate the junction position.
- (iii) Explain how many junctions can be formed.

(11 Marks)

- (b) (i) For an ideal metal-oxide-Semiconductor (MOS) diode on *n*-Si substrate, state the polarity of voltage which should be applied to the metal gate to make it in accumulation condition. Sketch the energy band diagram.
- (ii) For a real MOS diode fabricated on a *p*-Si substrate, if the work function of metal is 0.5 eV less than that of Si, sketch the energy band diagram of the diode when it is at thermal equilibrium.
- (iii) For a real MOS diode fabricated on a *p*-Si substrate, if there are negative charges in the oxide, will the threshold voltage increase or decrease? Explain why.
- (iv) Taking a MOS diode on *p*-Si as an example, describe how the threshold voltage is defined and what are the factors that will affect the value of threshold voltage?

(14 Marks)

APPENDIX AList of Selected Formulae**P-n junction**

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}; \quad N_A x_p = N_D x_n; \quad W = x_p + x_n; \quad C_j = \frac{\epsilon_s}{W};$$

$$W = \sqrt{\frac{2\epsilon_s}{q} \left[\frac{1}{N_A} + \frac{1}{N_D} \right] (V_{bi} - V)}; \quad L_p = \sqrt{D_p \tau_p}.$$

Bipolar junction transistors

$$\gamma \equiv \frac{I_{Ep}}{I_E} = \frac{I_{Ep}}{I_{Ep} + I_{En}}; \quad \alpha_T \equiv \frac{I_{Cp}}{I_{Ep}}; \quad \alpha_0 = \gamma \alpha_T; \quad \beta_0 = \frac{\alpha_0}{1 - \alpha_0}; \quad I_C = \alpha_0 I_E + I_{CBO};$$

$$I_{CEO} = (1 + \beta_0) I_{CBO}; \quad p_n(x) = p_{no} e^{qV_{EB}/kT} (1 - \frac{x}{W}); \quad \gamma = \frac{1}{1 + \frac{D_E}{D_p} \cdot \frac{N_B}{N_E} \cdot \frac{W}{L_E}};$$

$$I_{Ep} = qA \frac{D_p p_{no}}{W} e^{(qV_{EB}/kT)}; \quad I_{En} = qA \frac{D_E n_{E0}}{L_E} (e^{qV_{EB}/kT} - 1); \quad I_{Cn} = qA \frac{D_C n_{C0}}{L_C};$$

$$p_{no} \cdot N_B = n_{E0} \cdot N_E = n_{C0} \cdot N_C = n_i^2; \quad \tau_B = \frac{W^2}{2D_p}; \quad f_T = \frac{1}{2\pi\tau_B}.$$

MOS devices

$$\psi_s = 2\psi_B = \frac{2kT}{q} \ln \left(\frac{N_A}{n_i} \right); \quad W_m^2 = \frac{2\epsilon_s (2\psi_B)}{qN_A} = \frac{4\epsilon_s kT}{q^2 N_A} \ln \left(\frac{N_A}{n_i} \right); \quad V_T = \frac{qN_A W_m}{C_o} + 2\psi_B;$$

$$\frac{C}{C_0} = \frac{1}{\sqrt{1 + \frac{2\epsilon_{ox}^2 V}{qN_A \epsilon_s d^2}}}; \quad \frac{1}{C_{min}} = \frac{d}{\epsilon_{ox}} + \frac{W_m}{\epsilon_s}; \quad V_{FB} = \phi_{ms} - \frac{(Q_f + Q_m + Q_{ot})}{C_0}.$$

$$I_D = K_n [(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}] \text{ for } V_{DS} < V_{GS} - V_T; \quad V_T = \frac{qN_A W_m}{C_0} + 2\psi_B \text{ when } V_{FB} = 0;$$

$$I_D = \frac{K_n}{2} (V_{GS} - V_T)^2 \text{ for } V_{DS} \geq V_{GS} - V_T; \quad K_n = \mu_n C_{ox} \frac{W}{L}.$$

Thermal oxidation

$$t_{ox}^2 + At_{ox} = B(t + \tau); \quad \tau = \frac{t_{ox}^2}{B} + \frac{t_{ox}}{B/A}. \quad t_{ox} = \frac{-A + \sqrt{A^2 + 4B(t + \tau)}}{2}$$

$$D = D_o \exp \left(-\frac{E_a}{kT} \right)$$

APPENDIX A (continued)List of Selected Formulae (continued)**Thermal diffusion**

Constant source diffusion:

$$N(z, t) = N_s \operatorname{erfc}\left(\frac{z}{2\sqrt{Dt}}\right)$$

Limited source diffusion:

$$N(z, t) = \frac{Q}{\sqrt{\pi Dt}} \exp\left[-\frac{z^2}{4Dt}\right], \quad Q = \frac{2}{\sqrt{\pi}} N_s \sqrt{Dt}.$$

Ion implantation

Before Annealing

$$N(x) = \frac{Q}{\sqrt{2\pi \Delta R_p}} \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right]$$

$$Q = \int_0^\infty N(x) dx = \sqrt{2\pi} N_p \Delta R_p$$

After annealing

$$N(x) = \frac{Q}{\sqrt{2\pi (\Delta R_p^2 + 2Dt)^{1/2}}} \exp\left[-\frac{(x - R_p)^2}{2(\Delta R_p^2 + 2Dt)}\right]$$

APPENDIX BTable of Physical Constants

Physical Constant	Symbol	Value	Units
Electronic charge	q	1.6×10^{-19}	C
Boltzmann's constant	k	8.62×10^{-5} 1.38066×10^{-23}	eV/K J/K
Planck's constant	h	6.626×10^{-34}	J·s
Permittivity of free space	ϵ_0	8.85×10^{-14}	F/cm
Dielectric constant of Si	ϵ_{Si}	11.7	-
Dielectric constant of SiO ₂	ϵ_{ox}	3.9	-
Electron Mass	m	9.11×10^{-31}	kg
Speed of Light	c	3×10^8	m/s
Bandgap of Si at 300 K	E_g	1.12	eV
Intrinsic carrier concentration in Si at 300 K	n_i	9.65×10^9	cm ⁻³

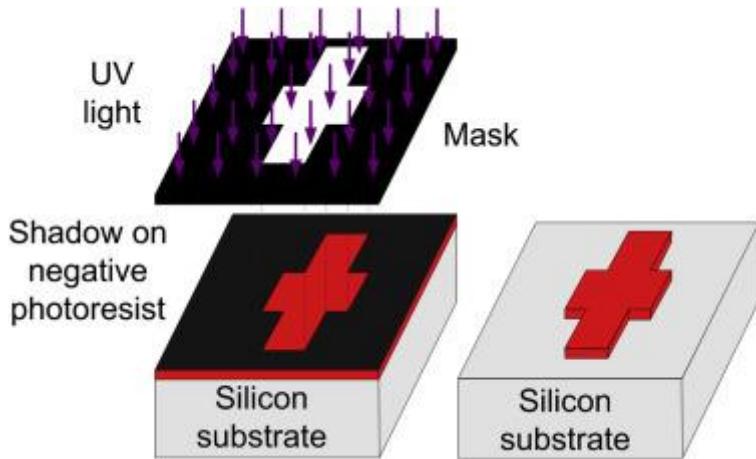
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EE3013 – SEMICONDUCTOR DEVICES AND PROCESSING

Semester 2, AY2020/2021

1)

- a) This refers to negative photoresist, in which the regions on the substrate exposed to UV light will develop cross-linkage between molecules. This causes the unexposed/masked region to be washed away by the organic developer. Therefore, the intended pattern (to be dissolved) is opposite to that of the mask.



- b) Prior to coating, there might be some water molecules attached to the substrate surface. After applying HMDS, the hydrogen atoms of the water molecules on the substrate surface will break free to bond with the NH- group of HMDS, forming ammonia (NH_3). The $\text{Si}(\text{CH}_3)_3$ group of the HMDS molecule will then be bonded the remaining oxygen atom on the wafer surface. This essentially covers the wafer surface with $\text{Si}(\text{CH}_3)_3$ group, which is hydrophobic and compatible with the resist that will be applied.
- c) Same lens column design $\Rightarrow NA_{wet} = NA_{dry}$
$$0.68 = 1.437 \sin \theta_{wet} \Rightarrow \theta_{wet} = 28.2^\circ$$

$$\text{Resolution of stepper aligner is given as } W_{min} = k_1 \frac{\lambda}{NA} = 0.45 * \frac{193 \text{ nm}}{0.68} = 127.72 \text{ nm}$$

$$\text{DOF of stepper aligner is given as } \sigma = \pm k_2 \frac{\lambda}{(NA)^2} = \pm 0.65 * \frac{193 \text{ nm}}{(0.68)^2} = 137.30 \text{ nm}$$

d)

- i) SiO_2 is a dielectric material, therefore DC sputtering will lead to trapped charges in the sample to be sputtered. Due to the low thickness, a low growth rate to ensure uniformity is required. **LPCVD** is the best choice.
- ii) Tungsten has high melting and boiling point, therefore thermal evaporation is unfeasible. **DC sputtering** is the best choice.
- iii) To avoid damage to the stainless steel cylinder due to energetic ions, sputter deposition should be avoided. **Thermal evaporation** is the best choice.

2)

- a) There are three components required for the wet etching of silicon, namely oxidiser (HNO_3 , to oxidise the Si to form SiO_2), solvent (HF, to dissolve the SiO_2) and diluent (H_2O or acetic acid). The rate of reaction can be determined by all three components above: if the concentration of the oxidiser is in excess compared to the solvent, then the reaction is said to be “solvent-limited”. The same also applies to the opposite. Using acetic acid instead of water as diluent usually give higher rate of reaction, due to the lower dissolution rate of HNO_3 in an acidic environment.

The etching rate also depends on the crystal plane due to difference surface concentration of atoms. In particular, in the $<111>$ direction, the etching rate is the slowest due to the highest concentration of Si atoms in the (111) plane. This causes the sloping (111) plane formed in the figure.

Etch rate is defined as the change in thickness over time.

$$<100> \text{ direction: } \frac{D_{<100>}}{t} = \frac{350 \mu\text{m}}{5 \text{ min}} = 70 \mu\text{m/min}$$

$$<111> \text{ direction: } \frac{D_{<111>}}{t} = \frac{\frac{\delta}{2} \sin \theta}{t} = 0.164 \mu\text{m/min}$$

- b) In order of 1 to 8: gas flow inlet, ground connection, anode, gas vacuum chamber, cathode biased by RF, RF source with impedance matching network, Si substrate.

First, electrons in the chamber gain energy from the RF oscillation. By virtue of its negative charge, it is attracted to the bottom electrode, hence building up negative charge. (Positive) ions are in turn attracted to the bottom electrode to etch the material away by momentum transfer. However, since the heavy ions are much less energetic than electrons, the bottom electrode maintains an overall negative charge (hence the cathode designation). The high electric field near the cathode is termed “plasma sheath” or “dark space”, where ion acceleration occurs.

c)

- i) The mass of accelerated ions and the accelerating RF potential. The degree of damage increases with either of these factors.
 - ii) Sidewall damage: Due to the rebound of energetic ions, the side walls of the patterned region may also be etched inwards.
Edge damage: At the patterned edge, where rebound of ions occur, there will be some deviations from the expected pattern.
 - iii) By annealing the substrate in a rapid thermal processor (RTP) at 450-800 °C for a few seconds/minutes. Most of the damaged crystal structure (including dopants) is then electrically reactivated and repaired.
- d) The throughput Q , in sccm or torr*litre / s, is given by $Q = pS$, where p is the pressure in torr, and S is the pumping speed in litre / s.

$$Q = pS \Rightarrow S = \frac{Q}{p} = \frac{20}{78.9} * \frac{1}{0.002} = 126.74 \text{ litre/s}$$

$$\text{Pumping speed, in } 1/\text{s, is given by } \frac{S}{V} = \frac{126.74}{30} = 4.22 \text{ s}^{-1}$$

3)

a)

- i) Oxide thickness is related to process parameters A, B and time t, τ as follows:

$$t_{ox,wet} = \frac{-A_{wet} + \sqrt{(A_{wet}^2 + 4B_{wet}(t+\tau))}}{2}, \text{ where } \tau = 0 \text{ for zero initial oxide thickness.}$$

$$0.5 = \frac{-0.226 + \sqrt{0.226^2 + 4 * 0.287t}}{2} \Rightarrow t = 0.87 \text{ hr} = 52.3 \text{ min}$$

- ii) For dry oxidation at 1200°C , $A_{dry} = 0.040, B_{dry} = 0.045$.

$$t_{ox,dry} = \frac{-A_{dry} + \sqrt{(A_{dry}^2 + 4B_{dry}(t+\tau))}}{2}, \text{ where } \tau = \frac{t_{oxi}^2 + A_{dry} * t_{oxi}}{B_{dry}} = \frac{0.5^2 + 0.04 * 0.5}{0.045} = 6$$

$$t_{ox,dry} = \frac{-0.040 + \sqrt{0.040^2 + 4 * 0.045 * (0.5 + 6)}}{2} = 0.521 \mu\text{m}$$

Total thickness, $t_{ox} = t_{ox,wet} + t_{ox,dry} = 0.5 + 0.521 = 1.021 \mu\text{m}$

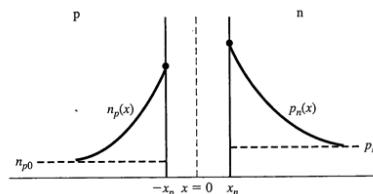
b)

- i) n-type impurities are required to counter-dope selected region of the substrate into n-type. The boundary between the initial p-type region and the obtained n-type region forms a p-n junction. After the diffusion, the junction position/depth can be characterized by either the angle-lap or groove-and-stain method.
- ii) An abrupt, linear junction is assumed. The concentration of minority carriers is given as such, where V_C is the contact potential and V_T is the thermal voltage.

$$\text{p-region: } n_p(x) = n_{p0} \left(e^{\frac{V_C}{V_T}} - 1 \right) e^{\frac{x+x_p}{L_n}} + n_{p0}$$

$$\text{n-region: } p_n(x) = p_{n0} \left(e^{\frac{V_C}{V_T}} - 1 \right) e^{\frac{x_n-x}{L_p}} + p_{n0}$$

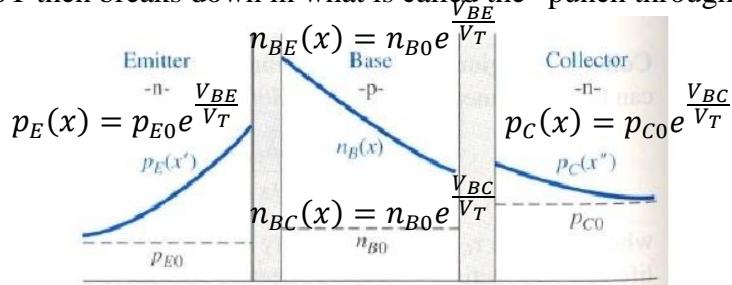
The carrier concentration profile under a forward-biased p-n junction is shown:



c)

- i) As V_{ce} increases, the base (p) - collector (n) junction becomes increasingly reverse-biased. This causes the space charge region to extend more into the neutral base region. As the neutral base width decreases and the minority concentration at either end remains constant, there is a higher concentration gradient. Diffusion current component of the collector current then increases. This leads to Early effect, where collector current I_C increases with V_{ce} . As V_{ce} increases further until the neutral base width is effectively zero, the two space charge regions "merge" into one, causing shorting of the collector and emitter. The BJT then breaks down in what is called the "punch through effect".

ii)



4)

a)

- i) At the interface, implanted concentration is maximum.

$$N_p = \frac{Q}{\sqrt{2\pi}\Delta R_p} = 3.325 \times 10^{17} \text{ cm}^{-3}$$

- ii) Junction depth can be calculated as such: $x_j = R_p \pm \Delta R_p \sqrt{2 \ln \frac{N_p}{N_B}}$, where N_p is the implanted concentration calculated in (i), and N_B is the substrate doping concentration.

$$x_j = 550 \times 10^{-9} \pm 120 \times 10^{-9} \sqrt{2 \ln \left(\frac{3.325 \times 10^{17}}{1 \times 10^{15}} \right)}$$

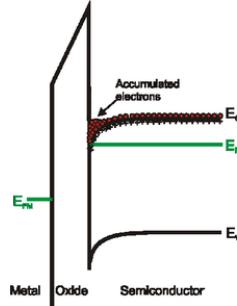
$$= 1.94 \mu\text{m} \text{ (Positive solution)}$$

- iii) Theoretically, two junctions can be formed, as x_j can form a quadratic equation.

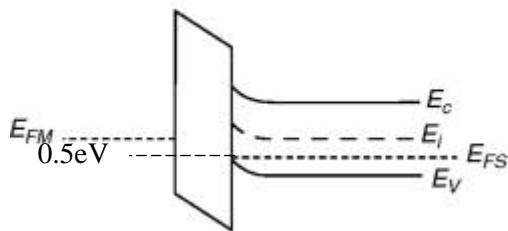
However, if R_p is smaller than the second term ($\Delta R_p \sqrt{2 \ln \frac{N_p}{N_B}}$), then only one junction can be formed since $x_j > 0$ as it indicates the depth into the substrate.

b)

- i) For accumulation of electrons near the gate oxide, positive voltage needs to be applied to the gate.



- ii)



- iii) Threshold is defined at the point where strong inversion begins. For p-type substrate, a sufficiently positive gate voltage is needed to achieve inversion and creation of a n-type channel. Intuitively, since there is negative charge trapped in the oxide, a more positive potential is required to generate the same effective bias as in an ideal diode. Therefore the threshold voltage increases.
- iv) Threshold voltage is quantitatively defined as $V_o + 2\Phi_B$, where V_o is related to the stored charge in the space charge region, and Φ_B is the built-in potential. Some factors that affect the threshold voltage include dopant concentration, oxide capacitance and temperature.