NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2021-2022

EE3019 – INTEGRATED ELECTRONICS

April / May 2022 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer all 4 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.
6. A List of Formulae is provided in the Appendix on page 7.

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1. (a) Consider a CMOS NAND gate depicted in Figure 1(a) on page 2 where both inputs are connected to V_{in}. Assume that V_{DD} = 1.5V, $C_{parasitic}$ = 3fF and C_{gate} = 7fF. The parameters of the pMOS and nMOS transistors are given below:

pMOS	$V_{tp} = -0.47$ V	$\mu_p C_{ox} = 25$ μA/V^2	$\left(\frac{W}{L}\right)_p = 2$
nMOS	$V_{tn} = 0.52$ V	$\mu_n C_{ox} = 65$ μA/V^2	$\left(\frac{W}{L}\right)_n = 1$

(i) Identify the regions of operation of both the pMOS and nMOS transistors when V_{out} is at $V_{OH(10\%)}$ and determine the output current, i_{out}, at $V_{OH(10\%)}$.

(ii) Identify the regions of operation of both the pMOS and nMOS transistors when V_{out} is at $V_{OH(90\%)}$ and determine the output current, i_{out}, at $V_{OH(90\%)}$.

Note: Question No. 1 continues on page 2.

(iii) Determine the rise time, t_r, when V_{out} changes from $V_{OH(10\%)}$ to $V_{OH(90\%)}$.

State all your assumptions clearly.

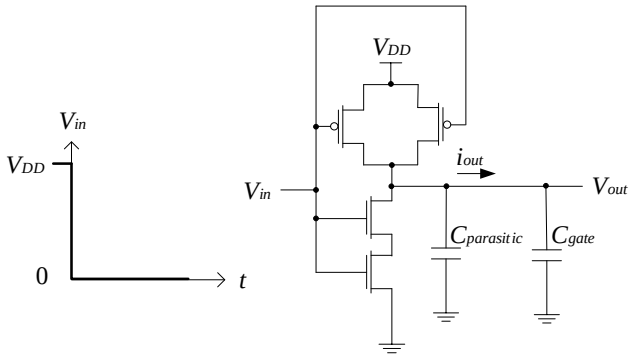

Figure 1(a)

(12 Marks)

(b) A pull-down network of a CMOS logic circuit is depicted in Figure 1(b).

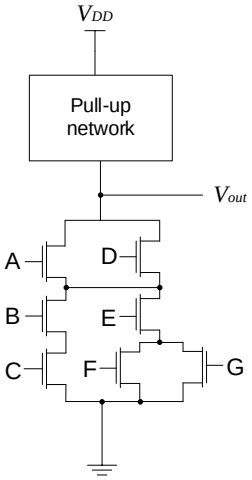

Figure 1(b)

(i) Complete the CMOS logic circuit by designing the corresponding pull-up network (PUN). Derive the logic function of the circuit.

(ii) Determine the width of the different pMOS transistors in the PUN such that the driving capability of the PUN is equal to that of an inverter designed for the worst-case scenario. Assume that the $\left(\frac{W}{L}\right)$ ratio of the pMOS transistor for the inverter is $\left(\frac{3}{1}\right)$ and the length of all transistors is 28nm.

(10 Marks)

Note: Question No. 1 continues on page 3.

(c) Briefly discuss how the circuit delay and power dissipation could be affected by the variations of the process threshold voltage.

(3 Marks)

2. (a) Derive an expression for the closed-loop gain of a single-loop feedback amplifier. Show that the signal-to-noise ratio of a closed loop amplifier is lower than an open-loop amplifier.

(7 Marks)

(b) A negative feedback amplifier is depicted in Figure 2. Assume that R_s = 1kΩ, R_L = 3kΩ, R_{id} = 100kΩ, r_o = 1kΩ, R_1 = 200kΩ, R_2 = 200kΩ and R_3 = 1kΩ.

(i) Identify the feedback topology and determine the feedback factor, β. Determine the input and output impedances, $R_{\beta i}$ and $R_{\beta o}$, respectively, of the feedback network.

(ii) Determine the voltage gain, $\frac{V_o}{V_s}$, for two cases of the open-loop gain of the op-amp: $A = \infty$, and $A = 10^5$.

(iii) Determine the input and output impedances, R_{if} and R_{of}, respectively, of the feedback amplifier.

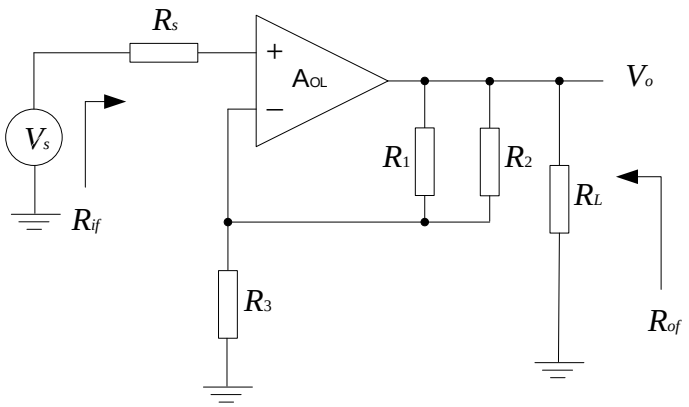

Figure 2

(15 Marks)

(c) Explain the -3 dB points in the lower and upper cut-off frequencies of an amplifier and their power gain relationship with the mid-band gain.

(3 Marks)

3. (a) Explain why a Bandgap voltage reference is preferred over a V_{BE}-based voltage reference.

(3 Marks)

(b) A Bandgap voltage reference is depicted in Figure 3. Derive the expression for V_{OUT} in terms of $V_{BE} + KV_T$ where K and V_T are a constant and the thermal voltage, respectively.

(16 Marks)

(c) Redesign the Bandgap voltage reference such that the current in the two transistors is not drawn from V_{CC}.

(4 Marks)

(d) The bipolar transistor Q1 and the bipolar op-amp A in the Bandgap voltage reference in Figure 3 are replaced by a PMOS transistor and a CMOS op-amp, respectively. Explain if these replacements are appropriate.

(2 Marks)

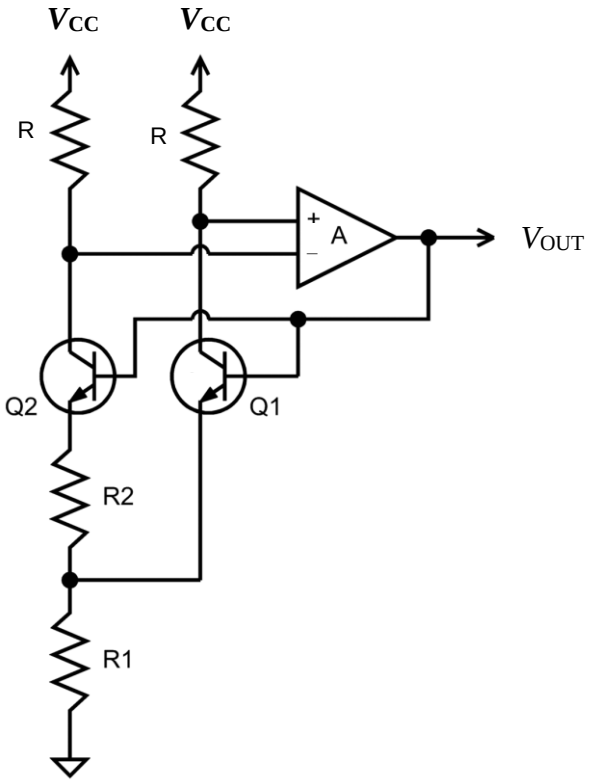

Figure 3

4. A multi-stage bipolar op-amp is depicted in Figure 4 on page 6. Assume the following parameters for the bipolar transistors:

$|V_{BE(on)}| = 0.7V$, $\beta \rightarrow \infty$, $V_T = 25mV$ and $|V_A| = 100$.

(a) Transistors Q_3 and Q_8 constitute a simple current mirror. State and explain two important attributes of the simple current mirror.

(5 Marks)

(b) Determine the following for transistor Q_5:
(i) DC bias current, and
(ii) DC voltage at the collector.

(8 Marks)

(c) Assuming that the output impedance of Q_3 and the input impedance of Q_4 and Q_5 are very large, determine the differential DC voltage gain of the first-stage of the op-amp.

(9 Marks)

(d) An engineer remarked that the op-amp in Figure 4 is not well designed. Explain if you agree or disagree with the engineer's remark, and suggest improvements, if any.

(3 Marks)

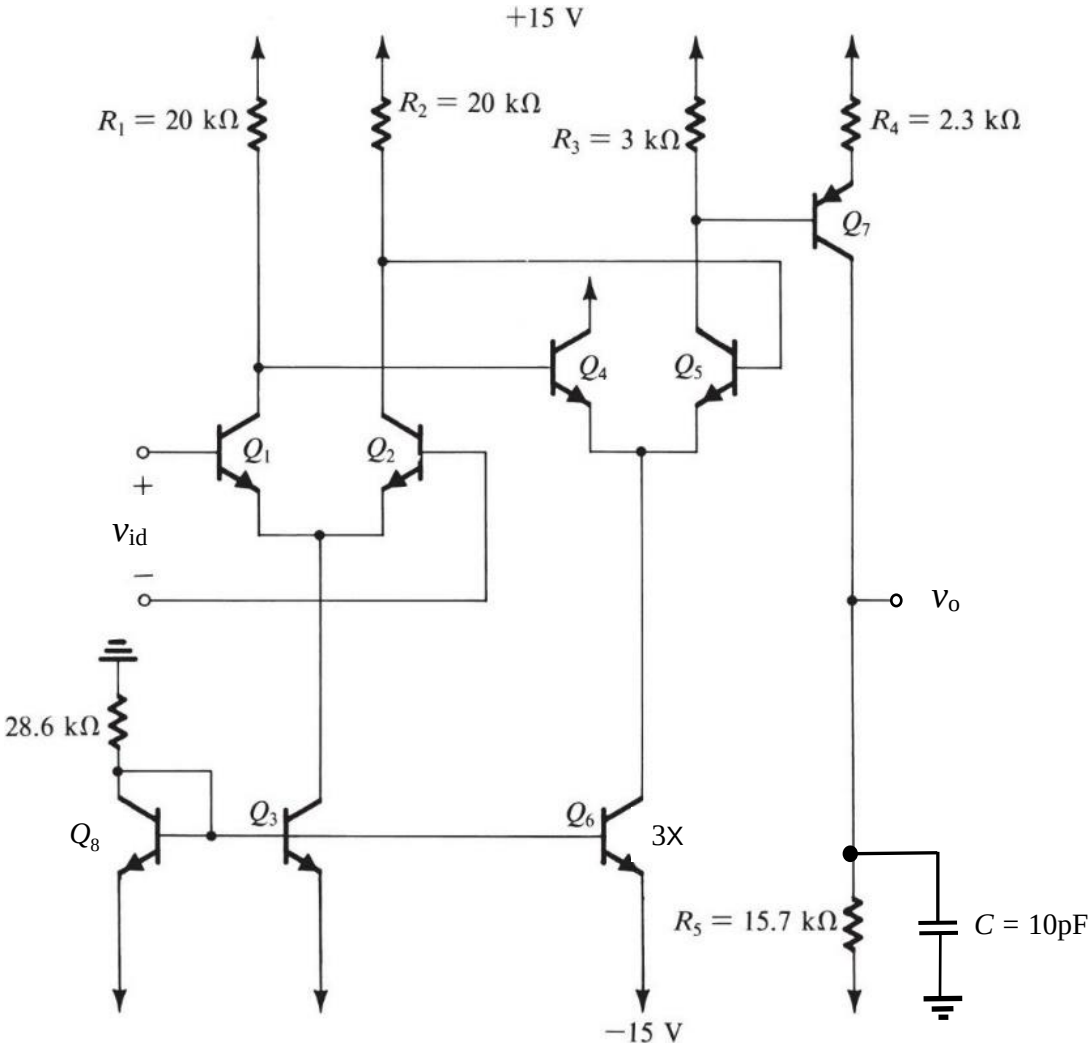

Figure 4

Appendix

List of Formulae

$$V = I\,Z \qquad P = I\,V$$

$$Z_L = j\omega L \qquad Z_C = \frac{1}{j\omega C}$$

$$\sum_{m=1}^{M} v_m = 0 \qquad \sum_{n=1}^{N} i_n = 0$$

$$v = L\frac{di}{dt} \qquad i = C\frac{dv}{dt}$$

$$S = V\,I^{*} \qquad i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

$$V_T = \frac{kT}{q} \qquad i_C \approx I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]$$

$$i_E = i_C + i_B \qquad \beta = \frac{i_C}{i_B}$$

$$\alpha = \frac{\beta}{1+\beta} \qquad A + B + C = \overline{\overline{A}\,\overline{B}\,\overline{C}}$$

$$ABC = \overline{\overline{A} + \overline{B} + \overline{C}} \qquad \tau_P = \frac{C_{load} \times \Delta V}{I_{avg}}$$

$$i_{Dn(LIN)} = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left((v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^{\,2}\right) \qquad A_f = \frac{A}{1 + A\beta}$$

$$i_{Dn(SAT)} = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad f = \frac{1}{2n\,\tau_p}$$

$$A(s) = A_m F_H(s) = \frac{A_m}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \qquad V_o = A_1A_2(V_i - \beta V_o) + A_1V_n$$

$$g_m = 2\frac{I_D}{(V_{GS} - V_t)} \qquad r_o = \frac{V_A}{I_D}$$

$$g_m = \frac{I_C}{V_T}$$

END OF PAPER