NANYANG TECHNOLOGICAL UNIVERSITY SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

ACADEMIC YEAR 2020-2021
SEMESTER 2
EE3019 INTEGRATED ELECTRONICS

TUTORIAL 4

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1. For the gate-level schematic of the level-triggered Clocked NOR based SR latch depicted in Figure **4.**1, realize the level-triggered Clock NOR based SR latch in transistor level with not more than 12 transistors. In integrated circuit design, two important design criteria are small IC area and low power dissipation. Try to implement the level-triggered Clocked NOR based SR latch using not more than 8 transistors.

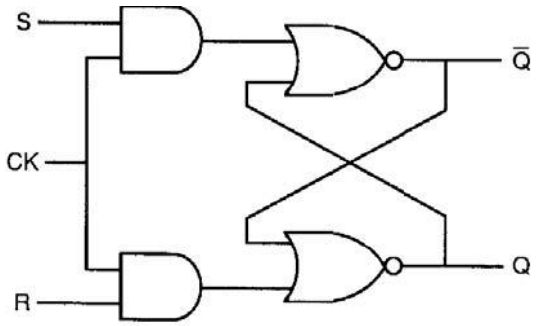

Figure **4.**1

2. The Clock SR latch depicted in Figure **4.**2 is fabricated in a process technology for which $\mu_n C_{ox}$ = 2.5$\mu_p C_{ox}$ = 50μA/V^2, V_{tn} = $|V_{tp}|$=1V and V_{DD}= 5V. Given that $(W/L)_1$ =$(W/L)_3$ = 6μm/2μm and $(W/L)_2$ =$(W/L)_4$ = 15μm/2μm, determine the W/L ratio of M_5, M_6, M_7 and M_8.

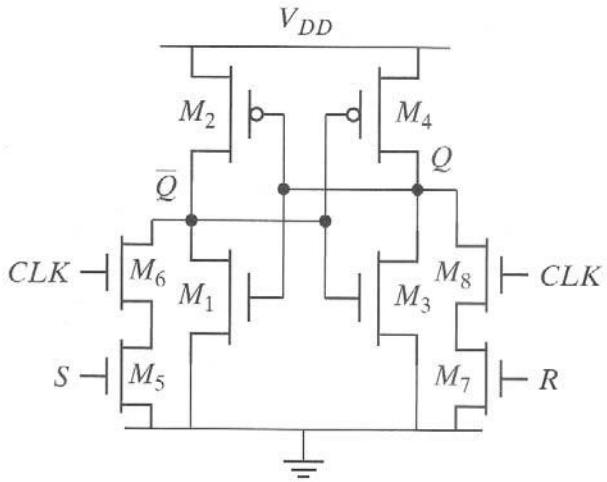

Figure **4.**2

[Ans: $(W/L)_5$ & $(W/L)_6 \geq 6$]

3. A 256K x 1 MOS DRAM is organised as a 512 row x 512 column matrix of memory cells. The cycle time comprising a read/write and refresh takes 200 ns. The refresh period is 2 ms.

   (a) Determine the time (in %) spent in the refresh activity.

   (b) A microprocessor is to be connected a number of 256K memory ICs. This microprocessor outputs a refresh cycle every 1 μs. Assuming that no additional DRAM refresh circuitry is used, determine the number of 256K memory ICs that can be connected to this microprocessor.

[Answer: *5.12%*, *3ICs*]