



Regions of Operation of BJT and MOSFET

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EE2002 Analog Electronics



Lesson Objectives

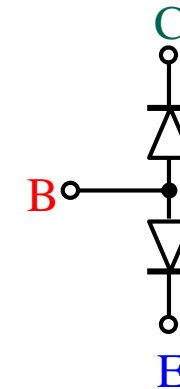
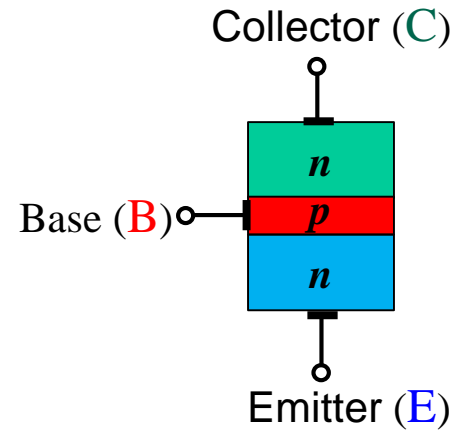
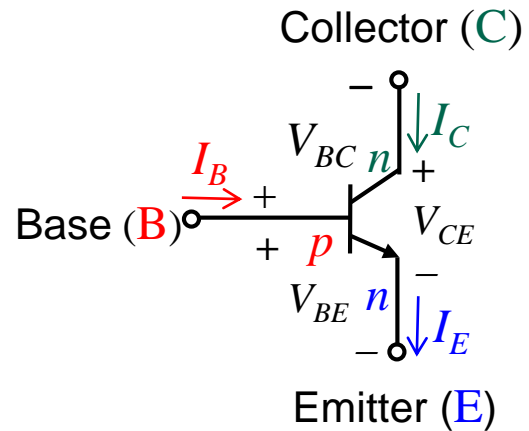
At the end of this lesson, you should be able to:

- Identify the symbols used to represent transistors in circuit schematics
- Identify the three different operation regions of BJT and MOSFET
- Describe the criteria for the different operation regions of BJT and MOSFET
- Discuss the i-v characteristics of MOSFET
- Analyse circuits used to bias BJT and MOSFET transistors into various regions of operation

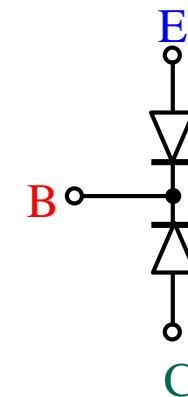
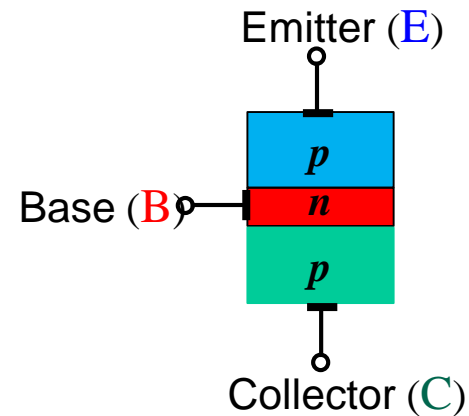
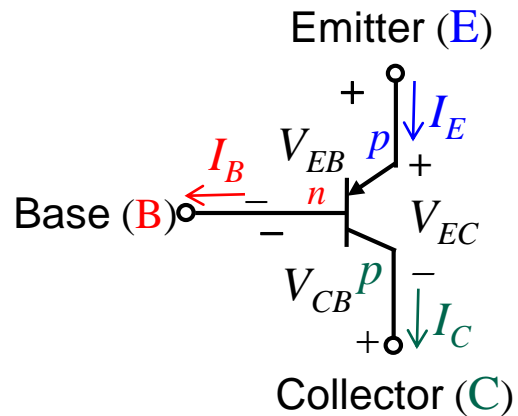
NPN and PNP BJTs

Don't get it

***n*pn**



***p*np**



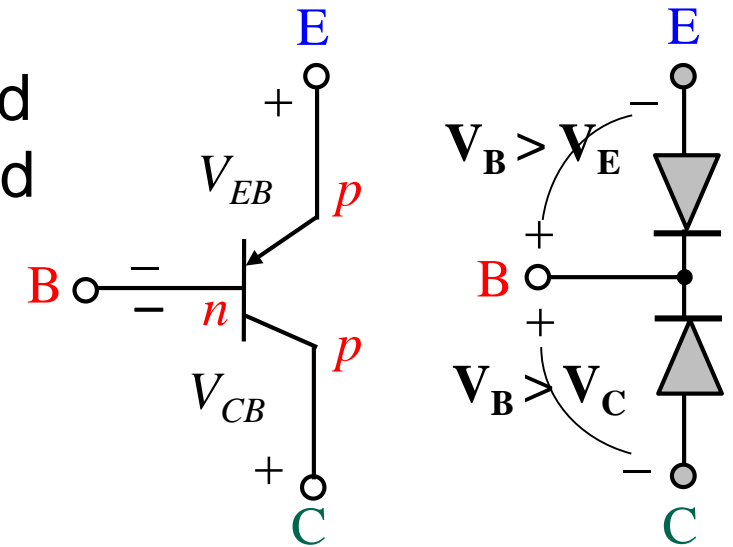
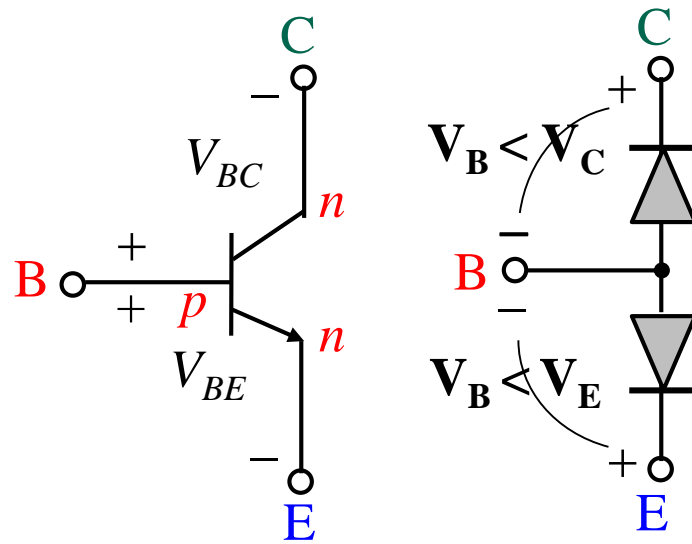
Operation Regions of BJT

Cutoff region

BEJ (npn) reverse biased
BCJ (npn) reverse biased

$$I_C = 0$$

⇒ **Open Switch**



Note: The junctions refer to EBJ and CBJ for pnp transistor.

Operation Regions of BJT

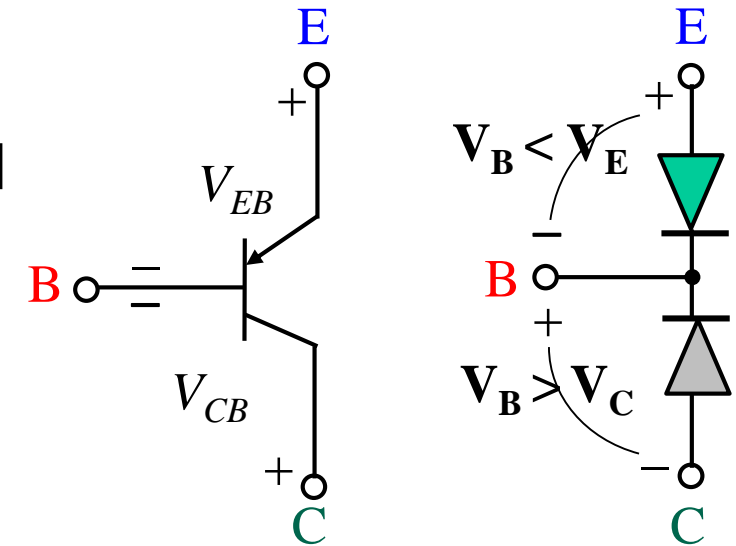
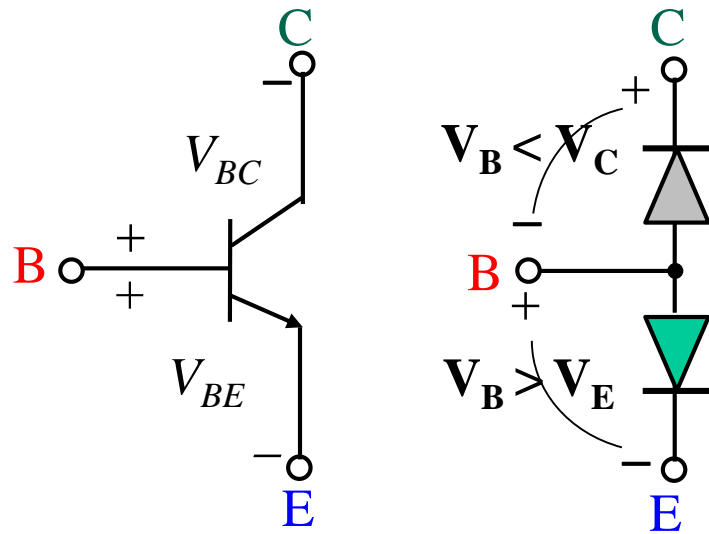
Forward-active region

BEJ (npn) forward biased
BCJ (npn) reversed biased

$$V_{BE} \approx 0.7 \text{ V}$$

$$I_C = \beta I_B = \alpha I_E$$

\Rightarrow **Good amplifier**
 $\alpha = \beta / (\beta + 1)$



Note: The junctions refer to EBJ and CBJ for pnp transistor.

Operation Regions of BJT

Saturation region

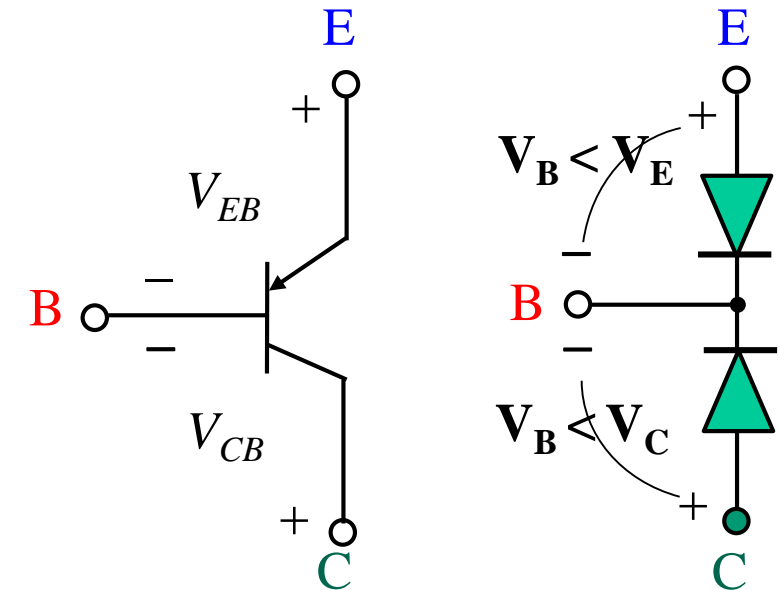
BEJ (npn) forward biased
BCJ (npn) forward biased

⇒ **Closed switch**

$$\Rightarrow V_{BE} \approx 0.7 \text{ V}$$

$$V_{BC} = 0.4 \sim 0.5 \text{ V}$$

$$\Rightarrow V_{CE(SAT)} = 0.2 \sim 0.3 \text{ V}$$



Note: The junctions refer to EBJ and CBJ for pnp transistor.

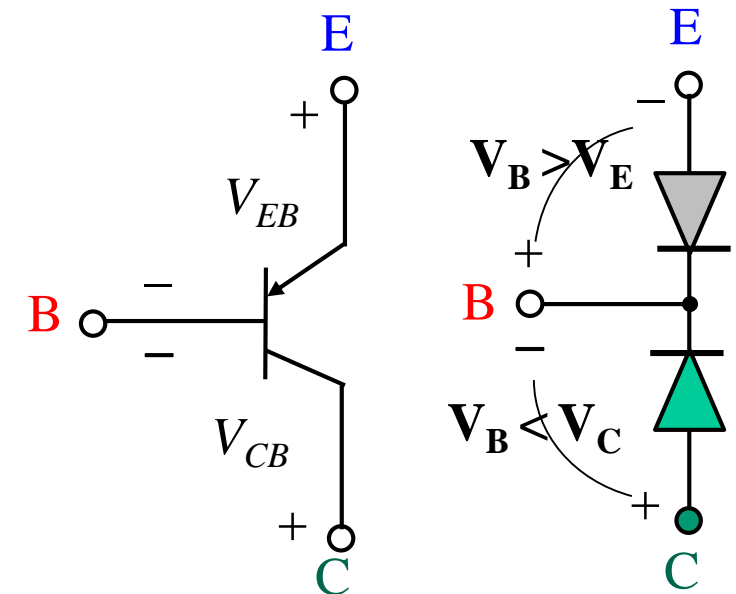
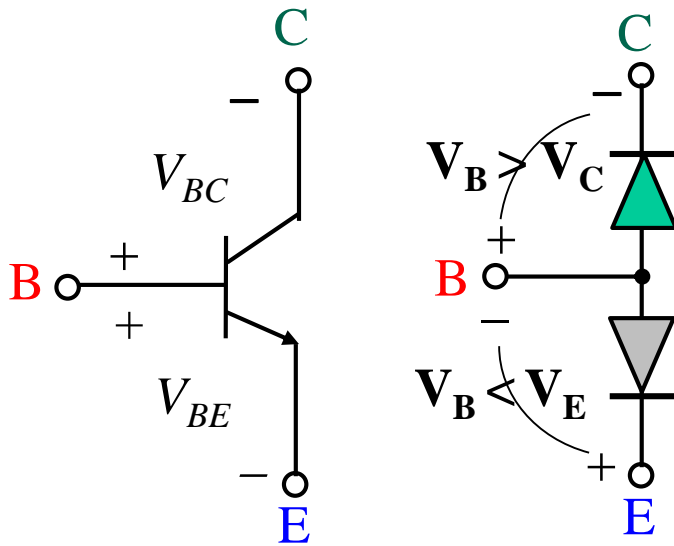
Operation Regions of BJT

Reverse-active region

BEJ (npn) reverse biased
BCJ (npn) forward biased

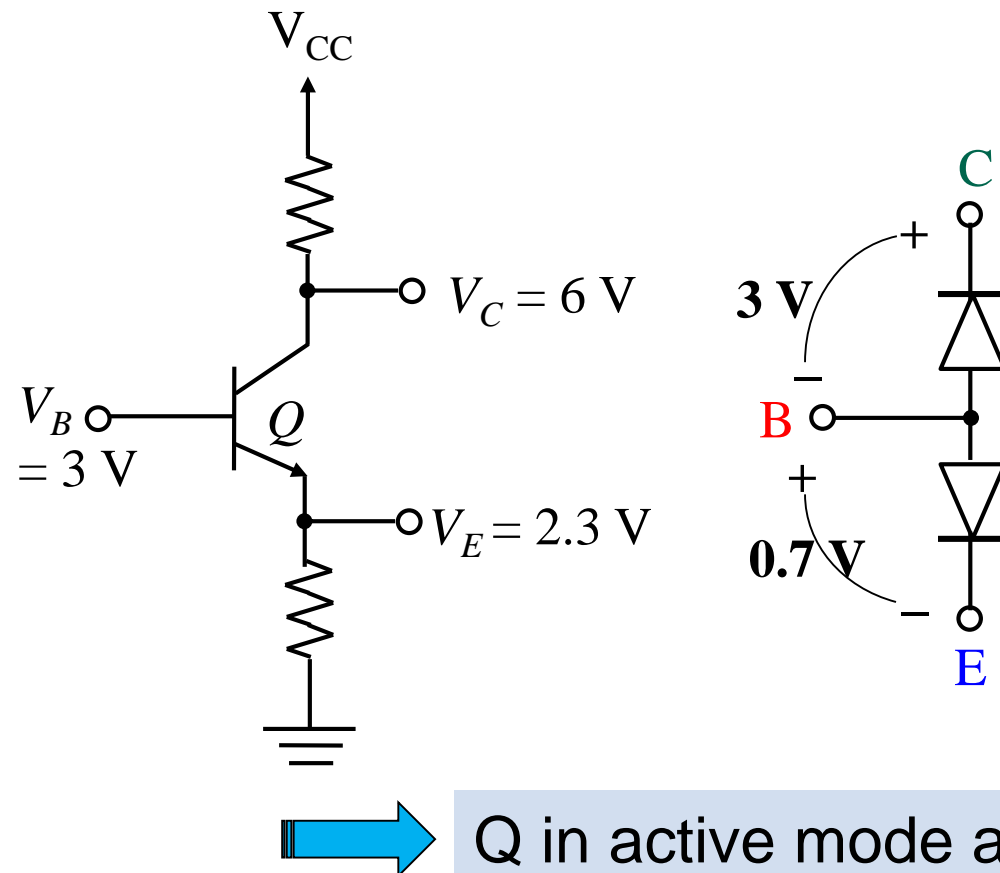
⇒ **Weak amplifier**

⇒ **Normally not use**



Note: The junctions refer to EBJ and CBJ for pnp transistor.

BJT Bias Analysis: Active Mode



$$\begin{aligned} V_{BE} &= V_B - V_E \\ &= 3 - 2.3 \\ &= 0.7\text{ V} \end{aligned}$$

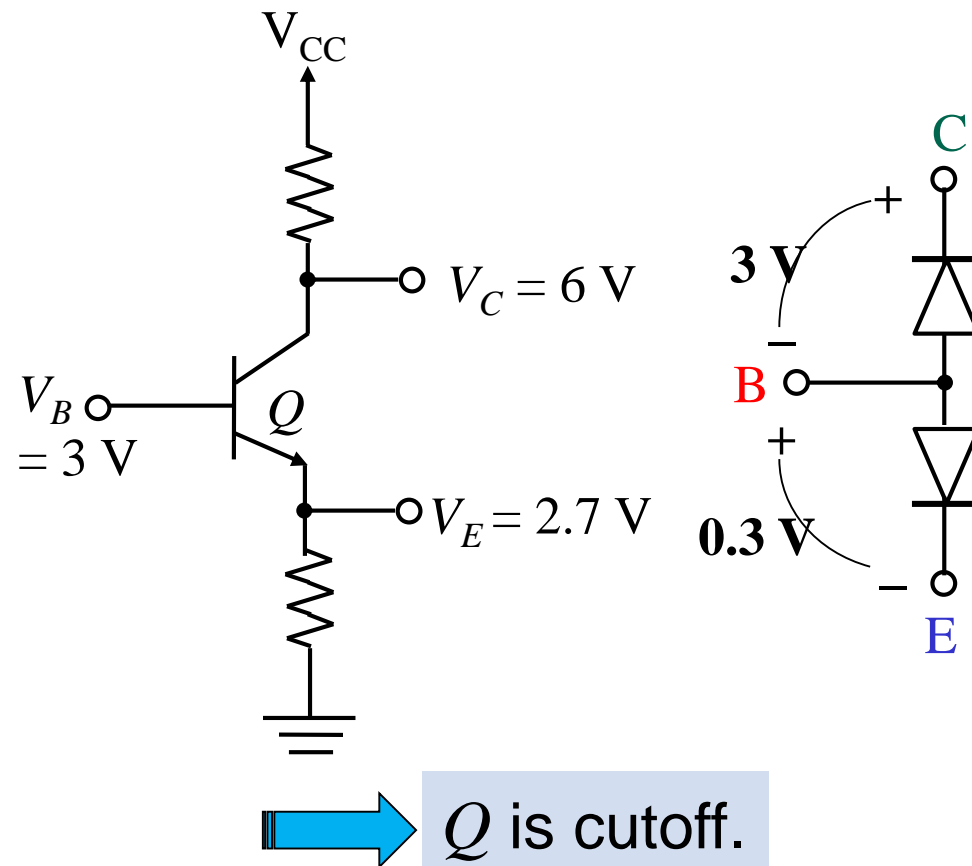
$$\begin{aligned} V_{BC} &= V_B - V_C \\ &= 3 - 6 \\ &= -3\text{ V} \end{aligned}$$

BCJ is reversed biased by 3 V

BEJ is forward biased by 0.7 V

Q in active mode and can be used as linear amplifier.

BJT Bias Analysis: Cutoff Mode



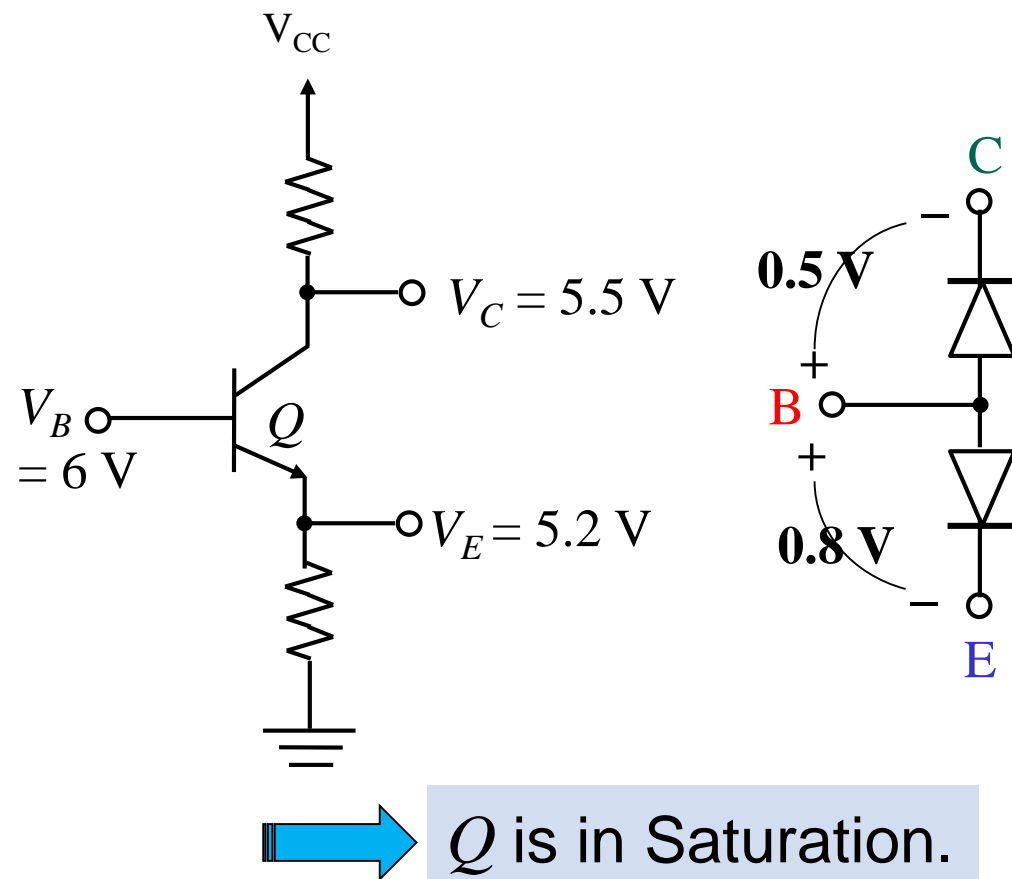
$$\begin{aligned} V_{BE} &= V_B - V_E \\ &= 3 - 2.7 \\ &= 0.3\text{ V} \end{aligned}$$

$$\begin{aligned} V_{BC} &= V_B - V_C \\ &= 3 - 6 \\ &= -3\text{ V} \end{aligned}$$

BCJ is reversed biased by 3 V

BEJ is forward biased by 0.3 V but inadequate to turn on BEJ

BJT Bias Analysis: Saturation Mode



$$\begin{aligned} V_{BE} &= V_B - V_E \\ &= 6 - 5.2 \\ &= 0.8 \text{ V} \end{aligned}$$

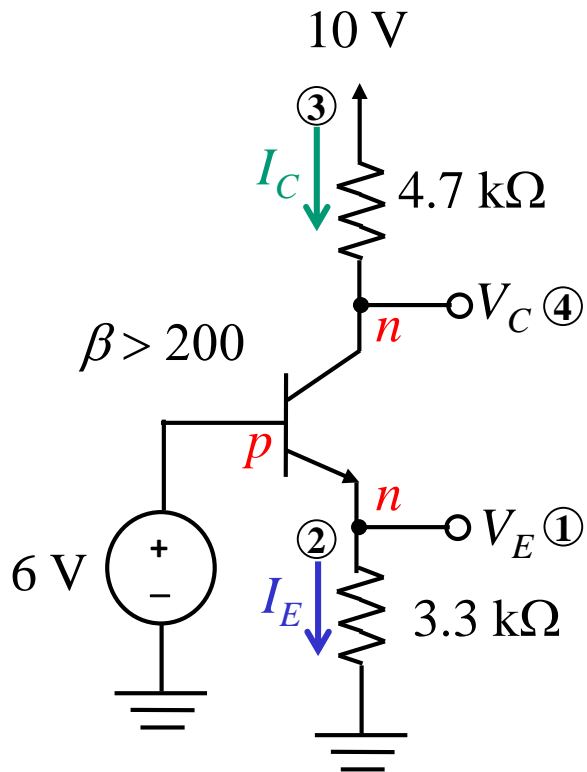
$$\begin{aligned} V_{BC} &= V_B - V_C \\ &= 6 - 5.5 \\ &= 0.5 \text{ V} \end{aligned}$$

BCJ is forward biased by 0.5 V

BEJ is forward biased by 0.8 V

$$\begin{aligned} V_{CE} &= V_{CB} + V_{BE} \\ &= -0.5 + 0.8 \\ &= 0.3 \text{ V} \end{aligned}$$

BJT Bias Analysis: Determine DC Node Voltages and Branch Currents



Assume active-mode operation,

$$\begin{aligned} V_E &= V_B - V_{BE} \\ &= 6 - 0.7 \\ &= 5.3 \text{ V} \end{aligned}$$

$$\begin{aligned} I_E &= \frac{5.3}{3.3} \\ &= 1.6 \text{ mA} \end{aligned}$$

Since β is very large,

$$\alpha \approx 1 \Rightarrow I_C \approx I_E = 1.6 \text{ mA}$$

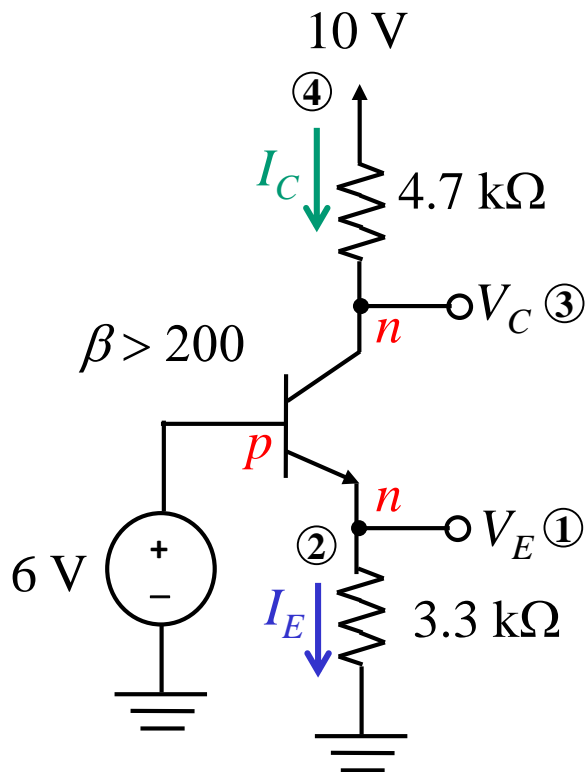
$$\begin{aligned} V_C &= 10 - 1.6 \times 4.7 \\ &= 2.48 \text{ V} \end{aligned}$$

$$\begin{aligned} V_{BC} &= V_B - V_C \\ &= 6 - 2.48 \\ &= 3.52 \text{ V} \end{aligned}$$

=> Wrong assumption! Q is in saturation mode.

BJT Bias Analysis: Determine DC Node Voltages and Branch Currents

(Cont.)



In saturation region,
 $V_{CE} \approx 0.2$ to 0.3 .

Assume $V_{CE(SAT)} = 0.2$ V,

$$V_E = 6 - 0.7 \quad \text{and} \quad I_E = \frac{5.3}{3.3} \\ = 5.3 \text{ V} \\ = 1.6 \text{ mA}$$

$$V_C = V_E + V_{CE(SAT)} \\ = 5.3 + 0.2 \\ = 5.5 \text{ V}$$

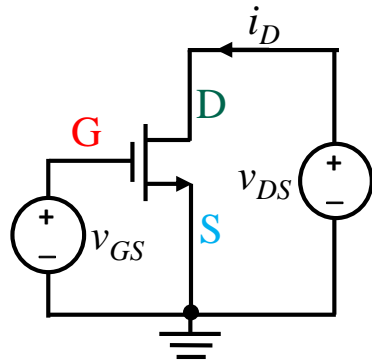
$$I_C = \frac{10 - 5.5}{4.7} \\ = 0.96 \text{ mA}$$

$$I_B = I_E - I_C = 1.6 - 0.96 = 0.64 \text{ mA}$$

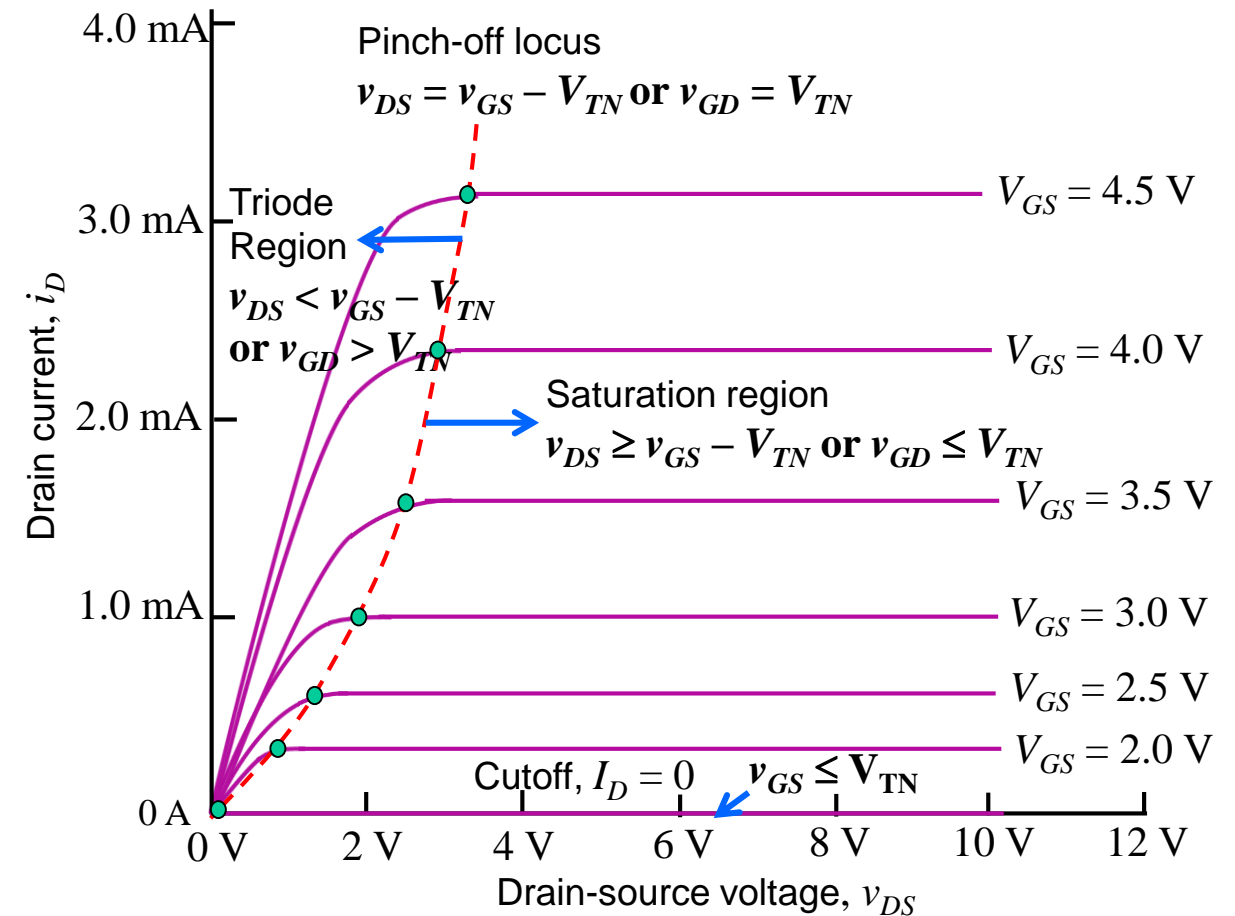
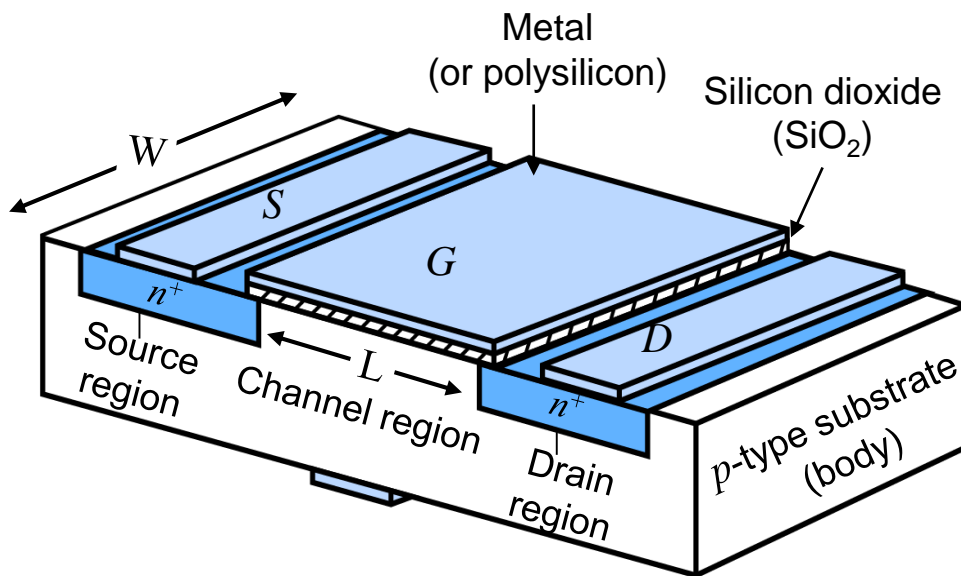
$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$

=> In saturation, $I_C \neq \beta I_B$.

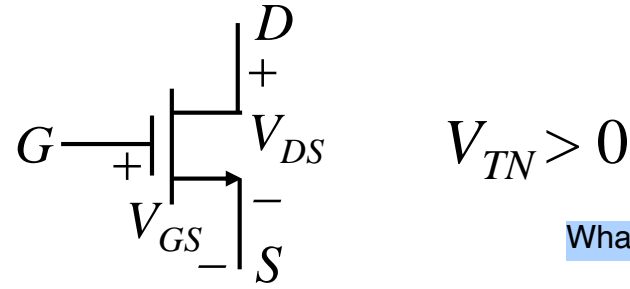
nMOS Transistor Structure and I-V Characteristics



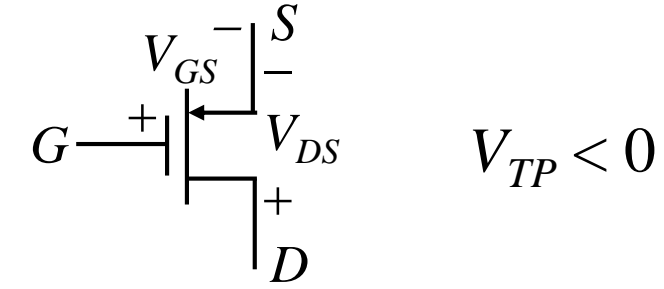
V_{TN} : Threshold Voltage of NMOS; $V_{TN} = 1$ V for this graph



MOSFET Biasing for Different Regions of Operation

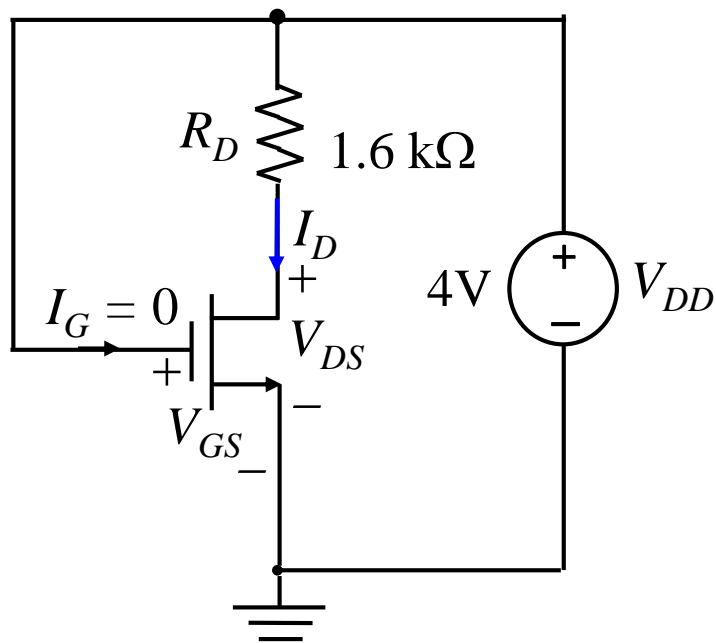


What is V_{TN} ?



Region	NMOS	PMOS
Cutoff	$V_{GS} < V_{TN}$ $I_D = 0$	$ V_{GS} < V_{TP} $ $I_D = 0$
Triode	$V_{GS} \geq V_{TN} \text{ and } V_{DS} < V_{GS} - V_{TN}$ $I_D = K_n \left(V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS}$	$ V_{GS} \geq V_{TP} \text{ and } V_{DS} < V_{GS} - V_{TP} $ $I_D = K_p \left(V_{GS} - V_{TP} - \frac{ V_{DS} }{2} \right) V_{DS} $
Saturation	$V_{GS} \geq V_{TN} \text{ and } V_{DS} \geq V_{GS} - V_{TN}$ $I_D = \frac{K_n}{2} (V_{GS} - V_{TN})^2$	$ V_{GS} \geq V_{TP} \text{ and } V_{DS} \geq V_{GS} - V_{TP} $ $I_D = \frac{K_p}{2} (V_{GS} - V_{TP})^2$

MOSFET Bias Analysis: Triode Region



$$K_n = 250 \mu\text{A}/\text{V}^2$$

$$V_{TN} = 1 \text{ V}$$

$$V_{GS} = V_{DD} = 4 \text{ V}.$$

Assume transistor is saturated,

$$I_D = \frac{K_n}{2} (V_{GS} - V_{TN})^2$$

$$= \frac{250 \mu}{2} (4 - 1)^2$$

$$= 1.13 \text{ mA}$$

$$V_{DS} = 4 - 1.6 \times 1.13$$

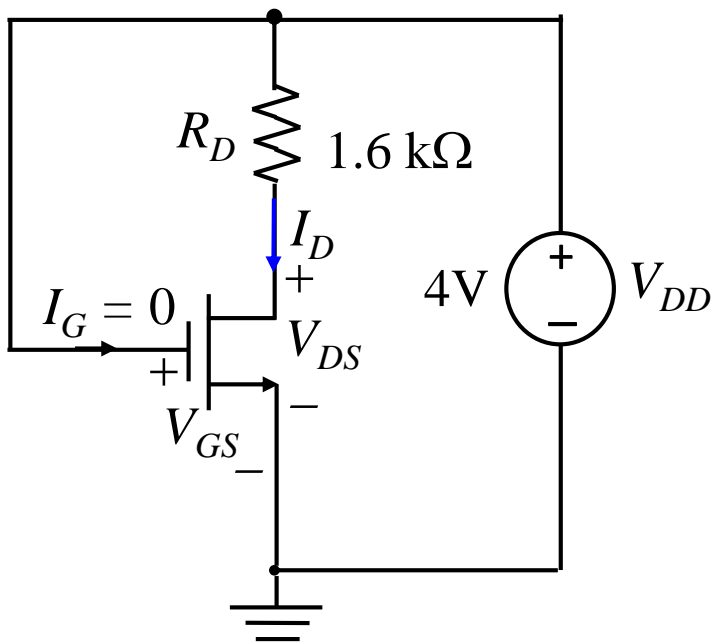
$$= 2.19 \text{ V}$$

$$\text{But } V_{DS} = 2.19 < V_{GS} - V_{TN} = 3$$

Saturation region
assumption is incorrect.

$$V_{DD} = I_D R_D + V_{DS}$$

MOSFET Bias Analysis: Triode Region



$$K_n = 250 \mu\text{A}/\text{V}^2$$
$$V_{TN} = 1 \text{ V}$$

(Cont...)

Using triode region equation,

$$I_D = K_n \left(V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS}$$

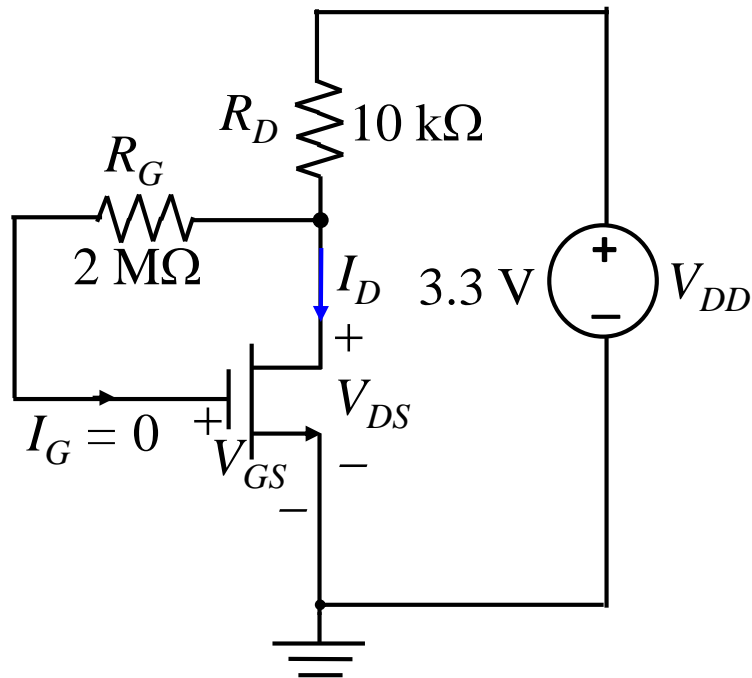
$$V_{DS} = 4 - 1600 \times 250 \mu \left(4 - 1 - \frac{V_{DS}}{2} \right) V_{DS}$$

$$0.2V_{DS}^2 - 2.2V_{DS} + 4 = 0$$

$$V_{DS} = 8.7 \text{ (infeasible) or } 2.3 \text{ V } (< V_{GS} - V_{TN} = 3)$$

Hence, $V_{DS} = 2.3 \text{ V}$ and $I_D = 1.06 \text{ mA}$

MOSFET Bias Analysis: nMOS Two-Resistor Biasing



$$K_n = 260 \mu\text{A/V}^2$$
$$V_{TN} = 1 \text{ V}$$

Since $I_G = 0$, $V_{DS} = V_{GS}$.

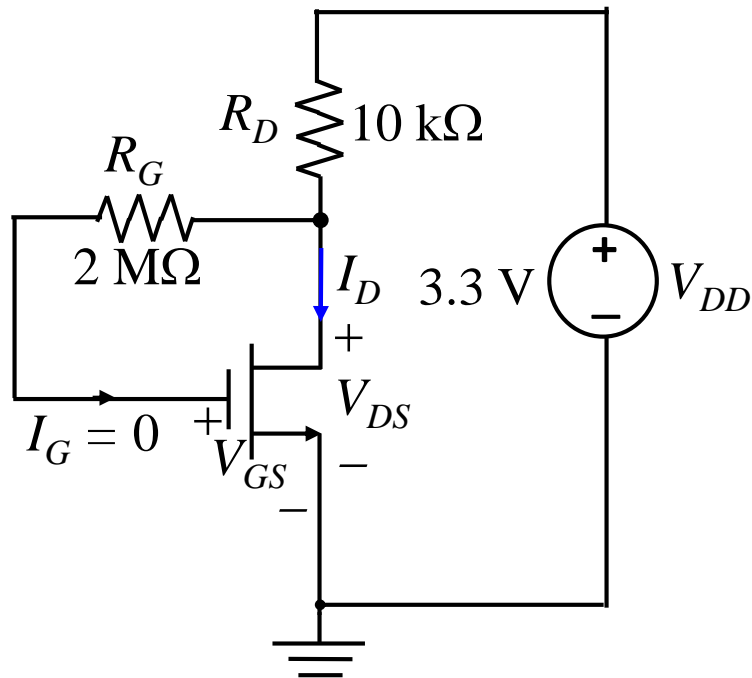
Transistor is saturated because $V_{DS} > V_{GS} - 1$

$$I_D = \frac{K_n}{2} (V_{GS} - V_{TN})^2$$
$$= \frac{260 \mu}{2} (V_{GS} - 1)^2$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{GS} = 3.3 - \frac{260 \mu}{2} (V_{GS} - 1)^2 \times 10000$$

MOSFET Bias Analysis: nMOS Two-Resistor Biasing



$$K_n = 260 \mu\text{A}/\text{V}^2$$
$$V_{TN} = 1 \text{ V}$$

(Cont.)

$$1.3V_{GS}^2 - 1.6V_{GS} - 2 = 0$$

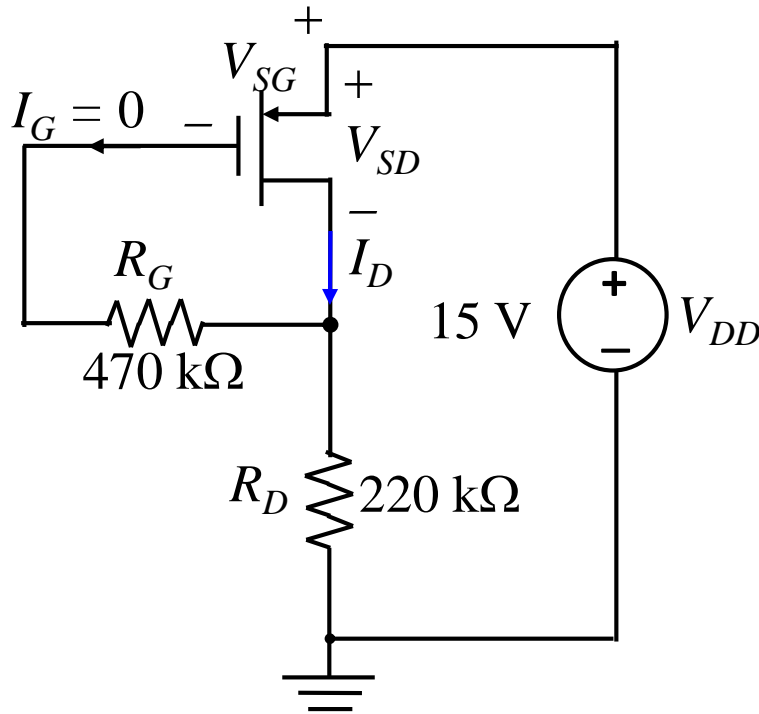
$$V_{GS} = \frac{1.6 \pm \sqrt{1.6^2 - 4 \times 1.3 \times (-2)}}{2 \times 1.3}$$
$$= -0.77 \text{ V or } 2 \text{ V}$$

$V_{GS} = -0.77 \text{ V}$ implies MOSFET is cutoff and contradicts the observation.

$$V_{GS} = 2 \text{ V and } V_{DS} = V_{GS} = 2 \text{ V.}$$

$$I_D = 130 \mu \times (2 - 1)^2 = 130 \mu\text{A}$$

MOSFET Bias Analysis: pMOS Two-Resistor Biasing



$$K_p = 50 \mu\text{A}/\text{V}^2$$
$$V_{TP} = -2 \text{ V}$$

Since $I_G = 0$, $V_{SG} = V_{SD}$.

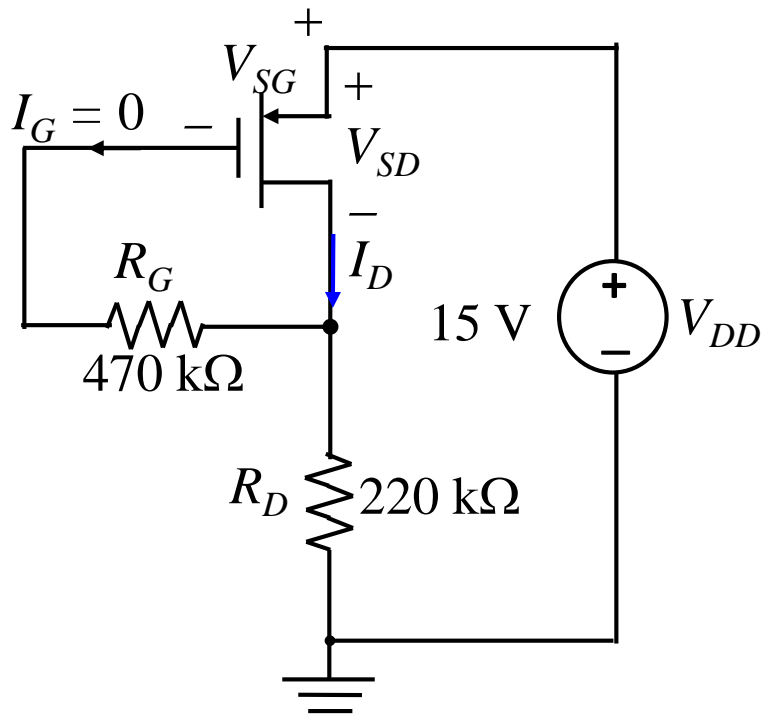
Transistor is saturated because $|V_{DS}| > |V_{GS}| - |-2|$

$$I_D = \frac{K_p}{2} (|V_{GS}| - |V_{TP}|)^2$$
$$= \frac{50 \mu}{2} (|V_{GS}| - 2)^2$$

$$|V_{DS}| = V_{DD} - I_D R_D$$

$$|V_{GS}| = 15 - 25 \times 10^{-6} (|V_{GS}| - 2)^2 \times 220 \times 10^3$$
$$= 15 - 5.5 (|V_{GS}| - 2)^2$$

MOSFET Bias Analysis: pMOS Two-Resistor Biasing



$$K_p = 50 \mu\text{A}/\text{V}^2$$
$$V_{TP} = -2 \text{ V}$$

(Cont.)

$$5.5|V_{GS}|^2 - 21|V_{GS}| + 7 = 0$$

$$|V_{GS}| = \frac{21 \pm \sqrt{21^2 - 4 \times 5.5 \times 7}}{2 \times 5.5}$$
$$= 0.37 \text{ V or } 3.45 \text{ V}$$

$$|V_{GS}| = 0.37 \text{ V} < |V_{TP}| = 2 \text{ V},$$

$$|V_{GS}| = 3.45 \text{ V or } V_{SG} = 3.45 \text{ V}.$$

$$V_{DS} = V_{GS} = -3.45 \text{ V}.$$

$$I_D = 25 \mu \times (3.45 - 2)^2 = 52.5 \mu\text{A}$$