NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2020-2021

EE2002 – ANALOG ELECTRONICS

November / December 2020 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 10 pages.
2. Answer all 4 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.
6. A list of formulae is provided in Appendix A on pages 7-10.

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1. (a) A non-ideal Op-Amp configured with resistors is shown in Figure 1(a) on page 2. The Op-Amp is powered by $\pm V_{CC}$ power supplies. It has 1 input source, v_{IN} and 3 non-ideal sources, I_+, I_- and V_{IO}.

Derive the expression for the output voltage v_{OUT}, in terms of all or some of the followings: v_{IN}, R_1, R_2, R_3, R_4, R_5, R_6, R_7, R_8, R_9, I_+, I_- and V_{IO}.

Note: *Parallel resistance of R_x and R_y can be written as $R_x // R_y$ without expanding it.*

(13 Marks)

Note: Question No. 1 continues on page 2.

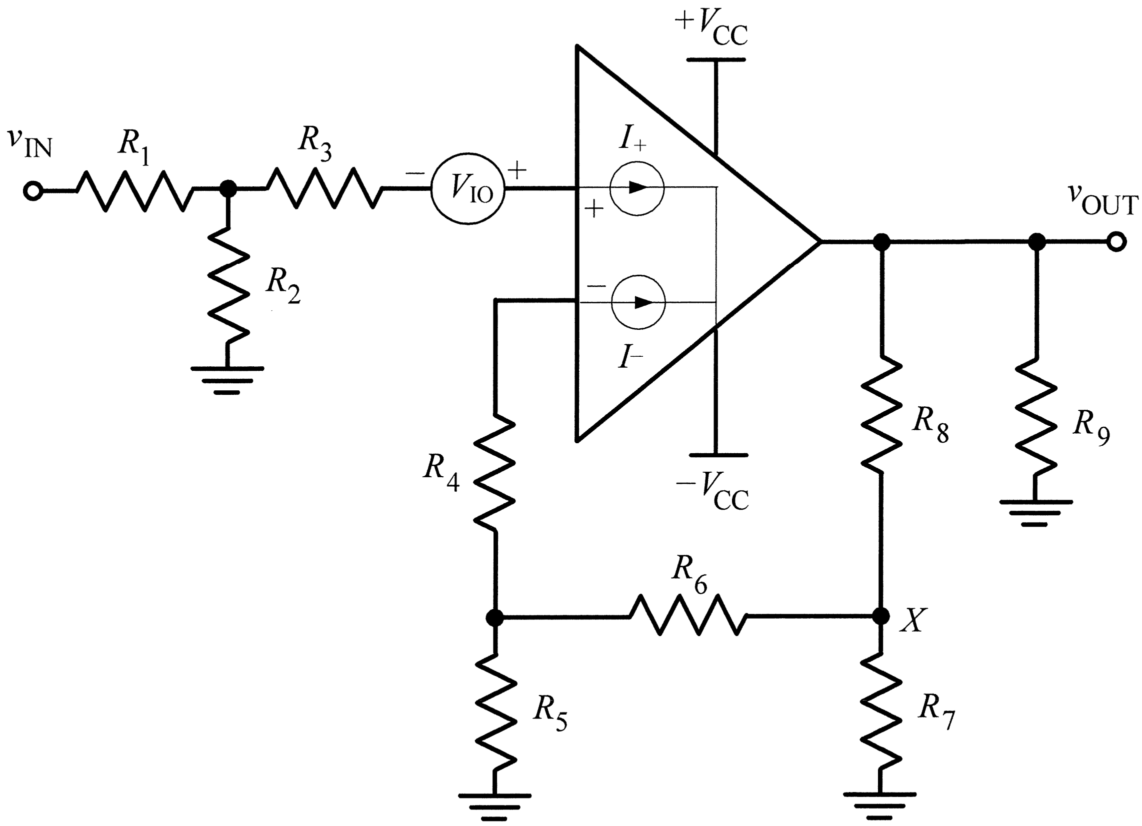


Figure 1(a)

(b) In Figure 1(b) on page 3, the empirical junction diode equation is:

$$V_D = nV_T \ln[I_D/I_S]$$

for the identical diodes D_1, D_2, D_3 and D_4, given that 2 points on the diode I-V characteristic curve are:

$$V_{Dx} = 0.650 \text{ V at } I_{Dx} = 400\ \mu\text{A and}$$

$$V_{Dy} = 0.740 \text{ V at } I_{Dy} = 4 \text{ mA.}$$

Also given that $V_1 = 9$ V and $V_2 = 12$ V, $R_1 = 3$ kΩ, $R_2 = 6$ kΩ, $R_3 = 4$ kΩ and $R_4 = 4$ kΩ, find the DC operating point or quiescent (Q) - point (I_D, V_D) for the diodes D_1, D_2, D_3 and D_4 (to 3 decimal places in mA and V, respectively).

Note: D_1, D_2, D_3 and D_4 have the same nV_T and I_S.

(12 Marks)

Note: Question No. 1 continues on page 3.

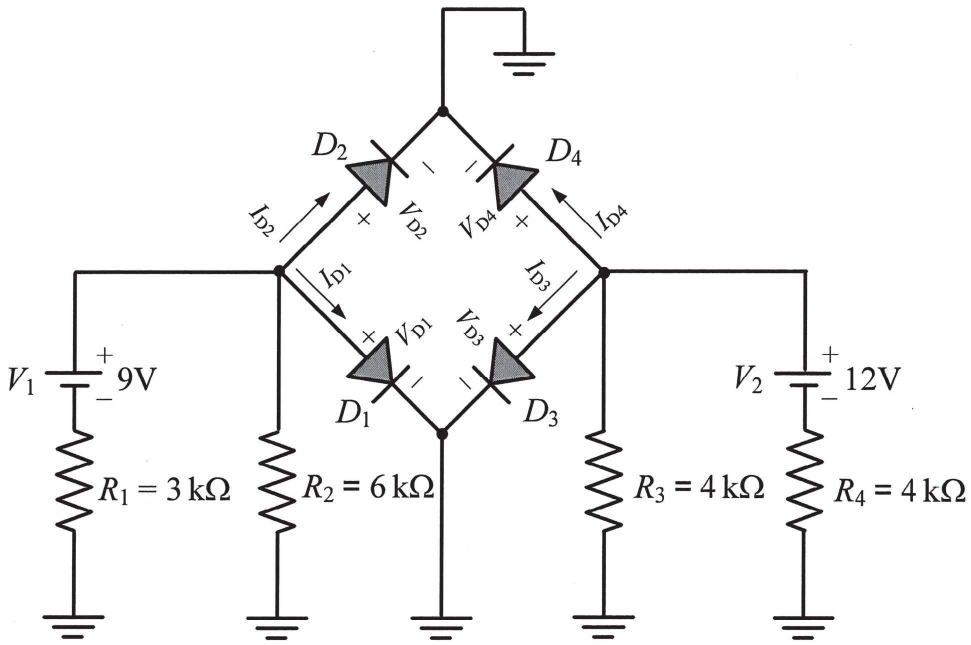


Figure 1(b)

2. For the single-stage amplifier shown in Figure 2 on page 4, the MOSFET has parameters of $K_n = 250\ \mu A/V^2$, $V_{TN} = 0.5$ V and $\lambda = 0.01V^{-1}$. All the capacitors C_i and C_o in the circuit are assumed to have infinite capacitance.

   (a) Find the DC operating point (I_D, V_{DS}) of the MOSFET.

   (6 Marks)

   (b) Draw the small signal equivalent circuit and derive the algebraic expressions for the input and output resistances (R_{in} and R_{out}), voltage and current gains ($A_v = v_o/v_i$ and $A_i = i_o/i_i$) of this circuit in terms of g_m, r_o and the resistors in the figure.

   (12 Marks)

   (c) Using the results of the DC analysis in part (a), find the values of the small signal parameters g_m, r_o and use them to find the numerical values of R_{in}, R_{out}, A_v and A_i determined in part (b).

   (7 Marks)

Note: Question No. 2 continues on page 4.

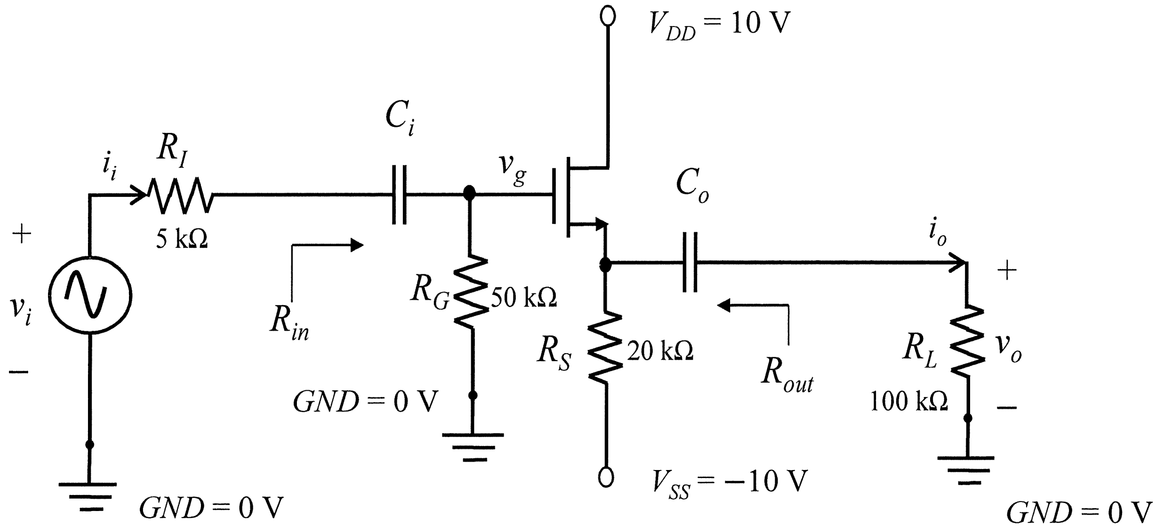


Figure 2

3. In Figure 3, the DC operating point for NPN BJT Q_1 are $I_C = 324$ µA and $V_{CE} = 2.5$ V, and the DC operating point for NMOS transistor M_2 are $I_D = 2.56$ mA and $V_{DS} = 2.32$ V. Q_1 has $\beta = 100$, $V_A = 75$ V, and $V_T = 25$ mV at room temperature, and M_2 has $K_n = 1.5$ mA/V^2, $V_{TN} = 1$ V and $\lambda = 0.01$ V^{-1}. Assume that $V_{CD} = 15$ V and all the capacitors have infinite values, and resistors have the values as indicated in Figure 3.

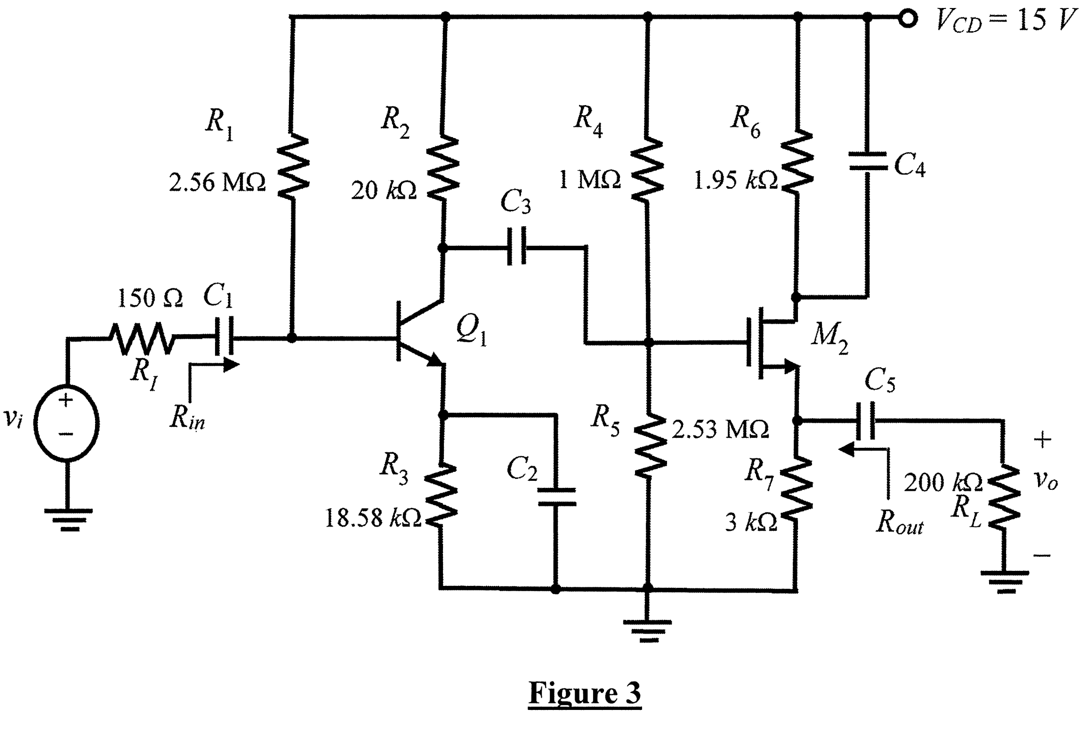


Figure 3

Note: Question No. 3 continues on page 5.

(a) Draw the small signal equivalent circuits.

(5 Marks)

(b) Determine the voltage gain $A_v = \frac{v_o}{v_i}$.

(7 Marks)

(c) Determine the input resistance R_{in} and output resistance R_{out} of the amplifier.

(8 Marks)

(d) Determine the input signal range for this amplifier for small signal operation.

(5 Marks)

4. The BJT current mirror shown in Figure 4 consists of an input transistor Q_1 and an output transistor Q_2, which are sized to have emitter areas A and $10A$ respectively. Both transistors have the same current gain β.

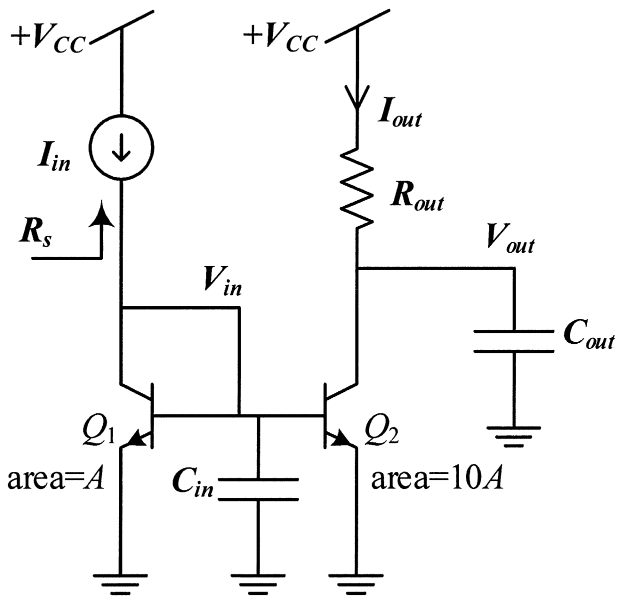


Figure 4

Note: Question No. 4 continues on page 6.

(a) Without considering the Early effect, find the DC mirror ratio I_{out} / I_{in}, in terms of the current gain β. You may ignore the AC effects produced by R_s, C_{in} and C_{out} for now.

(3 Marks)

(b) Now considering the Early effect, find a new expression for the mirror ratio I_{out} / I_{in}, which includes the terms V_{in}, V_{out} and Early voltage V_A.

(3 Marks)

(c) Calculate the value of I_{out} given that $I_{in} = 1\mu A$, $\beta = 100$, $V_{in} = 0.7V$, $V_{cc} = 5V$, $V_A = 50V$ and $R_{out} = 0.1\ M\Omega$. [Hint: express V_{out} in terms of I_{out} due to load resistor R_{out}, and substitute that into your answer for part (b)]

(8 Marks)

(d) Now consider the AC effects produced by R_s, C_{in} and C_{out} on the transfer function I_{out} / I_{in}. Draw the small-signal circuit for Figure 4, including these components.

(4 Marks)

(e) Explain whether C_{in} and C_{out} will contribute to the lower cut-off frequency ω_L, or the upper cut-off frequency ω_H. In your answer, use either the SCTC or OCTC method to calculate τ_{in} and τ_{out} under the DC condition found in part (c). Assume $R_s = 1M\Omega$, $C_{in} = C_{out} = 1pF$.

(4 Marks)

(f) Based on your answer in part (e), solve for the relevant cut-off frequency (either ω_L or ω_H). Is one of the time constants, τ_{in} or τ_{out}, a dominant term in your answer? If so, explain why.

(3 Marks)

Appendix A

List of Formulae (with the usual notations)

Op-Amps:

Closed-Loop Negative Feedback Inverting Gain, $A_{VCL} = \frac{v_o}{v_i} = -\frac{R_f}{R_i}$ Figure (a)

Closed-Loop Negative Feedback Non-Inverting Gain, $A_{VCL} = \frac{v_o}{v_i} = \left(1 + \frac{R_f}{R_i}\right)$ Figure (b)

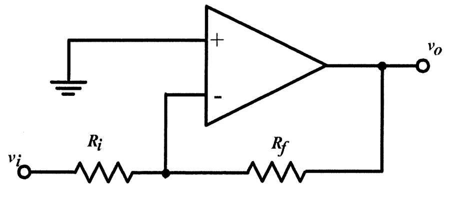


Figure (a)

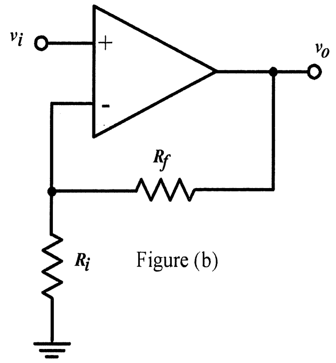


Figure (b)

Op-Amp's Slew Rate, $SR \geq \left|\frac{dv_o}{dt}\right|_{\max} = A_{VCL}\omega a_m = A_{VCL} a_m 2\pi f$,

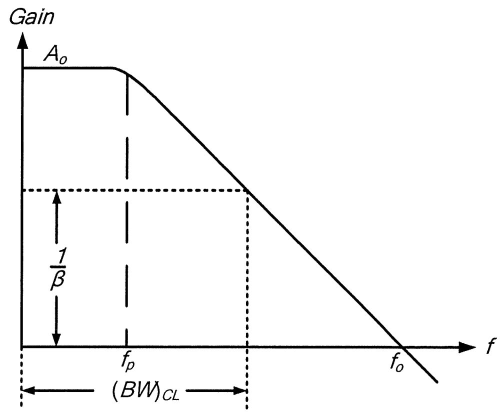
where $v_i = a_m \sin(\omega\, t)$, $v_o = A_{VCL} v_i$, $v_o = A_{VCL} a_m \sin(\omega t)$ and $\left|\frac{dv_o}{dt}\right| = A_{VCL}\omega\, a_m \cos(\omega t)$

Op-Amp's frequency response: $A_{VOL}(jf) = \frac{A_o}{\left(1 + \frac{jf}{f_p}\right)}$

Gain-Bandwidth Product: $A_o f_p = f_o = \frac{1}{\beta}(BW)_{CL}$

where $\frac{1}{\beta} = \frac{R_f + R_i}{R_i}$

$t_r = \frac{0.35}{(BW)_{CL}}$



Diodes:

$v_D \approx nV_T \ln\left(\frac{i_D}{I_S}\right)$ or $i_D \approx I_S e^{\left(\frac{v_D}{nV_T}\right)}$

where $e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \ldots\ldots\ldots$

Appendix A (Continued)

Diode conductance: $g_D = \dfrac{1}{r_D} = \dfrac{I_D}{nV_T}$

BJT in Forward Active Region:

Ignore early effect: $i_C = I_S \exp\left(\dfrac{|v_{BE}|}{V_T}\right)$

With early effect: $i_C = I_S \exp\left(\dfrac{|v_{BE}|}{V_T}\right)\left(1+\dfrac{|v_{CE}|}{V_A}\right)$

where I_s: Saturation current,
V_T: Thermal voltage, assume 25 mV at room temperature,
V_A: Early voltage.
For npn transistor, $|v_{BE}| = v_{BE}$ and $|v_{CE}| = v_{CE}$;
For pnp transistor, $|v_{BE}| = v_{EB}$ and $|v_{CE}| = v_{EC}$.

Small-signal model parameters of BJT:

$g_m = \dfrac{I_C}{V_T}$, $r_\pi = \dfrac{\beta}{g_m}$ and $r_o = \dfrac{V_A + |V_{CE}|}{I_C} \approx \dfrac{V_A}{I_C}$

where I_C : DC collector current at Q-point
V_{CE}: DC collector-emitter voltage at Q-point

Criterion for small-signal operation of BJT: $|v_{be}| \le 0.2V_T$

MOSFET in Saturation Region:

Criterion: $V_{DS} \ge V_{GS} - V_{TN}$ for NMOS;
$|V_{DS}| \ge |V_{GS}| - |V_{TP}|$ for PMOS

where V_{TN}, V_{TP}: Threshold voltage,
V_{DS}: DC drain-source voltage,
V_{GS}: DC gate-source voltage.

Ignore channel-length modulation effect: $i_D = \dfrac{K_n}{2}\left(v_{GS} - V_{TN}\right)^2$ for NMOS,

$i_D = \dfrac{K_p}{2}\left(|v_{GS}| - |V_{TP}|\right)^2$ for PMOS.

Appendix A (Continued)

With channel-length modulation effect: $i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2(1+\lambda v_{DS})$ for NMOS,

$i_D = \frac{K_p}{2}(|v_{GS}| - |V_{TP}|)^2(1+\lambda |v_{DS}|)$ for PMOS.

where λ: channel length modulation parameter,

For NMOS $K_n = K_n'\left(\frac{W}{L}\right)$ and $K_n' = \mu_n C_{ox}$; For PMOS $K_p = K_p'\left(\frac{W}{L}\right)$ and $K_p' = \mu_p C_{ox}$.

MOSFET in Triode Region:

Criterion: $V_{DS} < V_{GS} - V_{TN}$ for NMOS;
$|V_{DS}| < |V_{GS}| - |V_{TP}|$ for PMOS

Ignore channel-length modulation effect: $i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}$ for NMOS,

$i_D = K_p\left(|v_{GS}| - |V_{TP}| - \frac{|v_{DS}|}{2}\right)|v_{DS}|$ for PMOS.

With channel-length modulation effect: $i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}(1+\lambda v_{DS})$ for NMOS,

$i_D = K_p\left(|v_{GS}| - |V_{TP}| - \frac{|v_{DS}|}{2}\right)|v_{DS}|(1+\lambda |v_{DS}|)$ for PMOS.

Small-signal model parameters of MOSFET

For NMOS: $g_m = \sqrt{2K_n I_D(1+\lambda V_{DS})} \approx \sqrt{2K_n I_D}$ and $r_o = \frac{\frac{1}{\lambda} + V_{DS}}{I_D} \approx \frac{1}{\lambda I_D}$

For PMOS: $g_m = \sqrt{2K_p I_D(1+\lambda |V_{DS}|)} \approx \sqrt{2K_p I_D}$ and $r_o = \frac{\frac{1}{\lambda} + |V_{DS}|}{I_D} \approx \frac{1}{\lambda I_D}$

where I_D : DC drain current at Q-point
V_{DS}: DC drain-source voltage at Q-point

Criterion for small-signal operation:
For NMOS: $|v_{gs}| \leq 0.2(V_{GS} - V_{TN})$
For PMOS: $|v_{gs}| \leq 0.2(|V_{GS}| - |V_{TP}|)$
where V_{GS} : DC gate-source voltage at Q-point.

Appendix A (Continued)

Frequency Response: OCTC and SCTC

0) DISABLE DC sources…
voltage sources -> SHORT CIRCUIT, current sources -> OPEN CIRCUIT

1) Identify capacitors contributing (reducing V_o or causing trouble) to the frequency of interest (i.e. lower or higher cut-off).

2) DISABLE all independent AC sources...
voltage sources -> SHORT CIRCUIT, current sources -> OPEN CIRCUIT
DO NOT remove or "disable" dependent sources!

higher cut-off (OCTC)	lower cut-off (SCTC)
3) Idealize irrelevant capacitors by SHORT CIRCUIT (because at high f, cap → short) Next step to find time constant 4) For each contributing capacitor C_i, set all other capacitors (other than the one you are looking at) removed (i.e. OPEN CIRCUITS) and determine the resistance, R_i seen by C_i 5) Higher cut-off frequency is estimated as: $\omega_{H-3dB} \approx \dfrac{1}{\sum_i C_i R_i} = \dfrac{1}{C_1R_1 + C_2R_2 + \ldots}$	3) Idealize irrelevant capacitors by OPEN CIRCUIT (because at low f, cap → open) Next step to find time constant 4) For each contributing capacitor C_i, set all other capacitors (other than the one you are looking at) removed (i.e. SHORT CIRCUITS) and determine the resistance, R_i seen by C_i 5) Lower cut-off frequency is estimated as: $\omega_{L-3dB} \approx \sum_i \dfrac{1}{C_i R_i} = \dfrac{1}{C_1R_1} + \dfrac{1}{C_2R_2} + ..$

END OF PAPER

1. a) By superposition theorem

$V_{out} = V|_{IN} + V|_{I+} + V|_{I-} + V|_{VIO}$

Regardless of all other factors

for $V|_{IN}$

$V_+ = V_{IN} \cdot \frac{R_2}{R_1+R_2} = V_-$

$V_x = V_- \cdot \frac{R_5+R_6}{R_5}$

$V_{out1} = (V_-/R_5 + V_x/R_7) \cdot R_8 + V_x$

$= V_{IN}\left[\frac{R_2 \cdot R_8}{(R_1+R_2)\cdot R_5} + \frac{R_2\cdot(R_5+R_6)\cdot R_8}{R_5\cdot R_7\cdot(R_1+R_2)}\right] + V_{IN}\cdot\frac{R_2\cdot(R_5+R_6)}{R_5\cdot(R_1+R_2)}$

for $V|_{I+}$

$V_+ = -I_+ \cdot [R_3 + R_1 \| R_2] = V_-$

$V_x = V_- \cdot (R_5+R_6)/R_5$

$V_{out2} = (V_-/R_5 + V_x/R_7)\cdot R_8 + V_x$

$= -I_+\left[\frac{(R_3+R_1\|R_2)\cdot R_8}{R_5} + \frac{(R_3+R_1\|R_2)\cdot(R_5+R_6)\cdot R_8}{R_5\cdot R_7}\right]$

$+ -I_+ \cdot \frac{(R_3+R_1\|R_2)\cdot(R_5+R_6)}{R_5}$

for $V|_{I-}$

$V_+ = V_- = 0$

$\cancel{\left(\frac{R_4\cdot I_-}{R_5} + I_-\right)\times R_6 + I_-\cdot R_4 = V_x}$

$V_{out3} = \left(\frac{R_4\cdot I_-}{R_4\|R_5}\right)\times R_8 + (V_x/R_7)\times R_8 + V_x$

$= I_-\left[\left(\frac{R_4 R_8}{R_5} + R_8\right) + \left(\frac{R_4 R_6 R_8}{R_5\cdot R_7} + \frac{R_6 R_8}{R_7}\right) + \frac{R_4 R_8}{R_7}\right.$

$\left. + \frac{(R_4+R_5)\cdot R_6}{R_5} + R_4\right]$

for $V|_{VIO}$

$V_+ = V_- = V_{IO}$

$V_x = V_{IO} \times \frac{(R_5+R_6)}{R_5}$

$V_{out4} = V_{IO}\left[(R_8/R_5) + \frac{(R_5+R_6)\cdot R_8}{R_5\cdot R_7} + \frac{R_5+R_6}{R_5}\right]$

Combine them together

$V_{out} = V_{out1} + V_{out2} + V_{out3} + V_{out4}$

1 b) $V_{Dx} = nV_T \ln[I_{Dx}/I_s] \cdots ①$

$V_{Dy} = nV_T \ln[I_{Dy}/I_s] \cdots ②$

to find the value of nV_T & I_s

② − ①

$V_{Dy} - V_{Dx} = nV_T \ln[I_{Dy}/I_{Dx}]$

$\Rightarrow nV_T = 39.1\ mV$

$\Rightarrow I_s = 2.412 \times 10^{-11}\ A$

Based on Figure 1(b)

$V_{D1} = V_{D2}$; $V_{D3} = V_{D4}$

ie. $I_{D1} = I_{D2}$; $I_{D3} = I_{D4}$

left: $(I_{D1} + I_{D2} + \frac{V_{D1}}{R_2}) \cdot R_1 = V_1 - V_{D1}$

$\Rightarrow V_{D1} = 6 - 4k I_{D1}$

right: $(I_{D3} + I_{D4} + \frac{V_{D3}}{R_3}) \cdot R_4 = V_2 - V_{D3}$

$\Rightarrow V_{D3} = 6 - 4k I_{D3}$

$\therefore V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_D$; $I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_D$

$$\begin{cases} I_D = \frac{1}{4k} \cdot (6 - V_D) \\ V_D = 0.0391 \cdot \ln[I_D / 2.412\times10^{-11}] \end{cases}$$

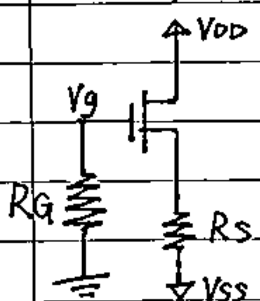
do iteration

V_D 0.700 V → 0.697 → 0.697 ✓

I_D 1.325 mA 1.326 ✓

$\therefore$ Q point $I_D = 1.326\ mA$ $V_D = 0.697\ V$

2. a) Draw DC diagram



Since $I_G = 0$ $\therefore V_g = 0$

$0 = V_{GS} + I_D \cdot R_S + V_{SS}$

$10V = V_{GS} + \frac{K_n}{2}(V_{GS} - V_{TN})^2 \times R_S$

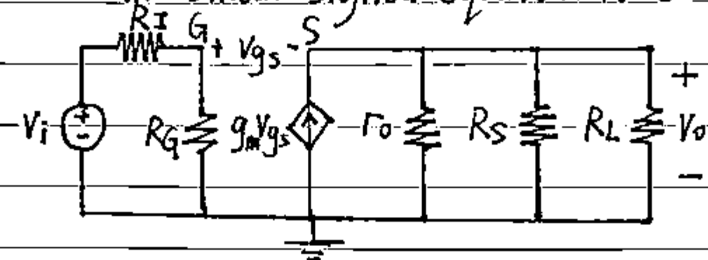
$10 = V_{GS} + \frac{250\mu}{2}(V_{GS} - 0.5)^2 \times 20k$

$2.5V_{GS}^2 - 1.5V_{GS} + \frac{5}{8} = 10$

$V_{GS} = 2.26\ V$

$\therefore I_D = 387.2\ \mu A$; $\because V_{DD} - V_{DS} - I_D R_S - V_{SS} = 0 \Rightarrow V_{DS} = 12.256\ V$

2.b) the small signal equivalent circuit :



$R_L' = r_o \| R_S \| R_L$

$A_{vt} = V_s / V_g = g_m V_{gs} R_L' / V_{gs} + g_m V_{gs} R_L' = \frac{g_m R_L'}{1 + g_m R_L'}$

$\therefore A_V = V_o / V_i = A_{vt} \times \frac{R_G}{R_G + R_I}$

$= \frac{g_m \cdot R_G \cdot (r_o \| R_S \| R_L)}{(R_G + R_I) \cdot [1 + g_m (r_o \| R_S \| R_L)]}$

$R_{in} = R_G$

$\because i_x = \frac{V_x}{R_S} + \frac{V_x}{r_o} - g_m V_{gs}$; $V_{gs} = -V_x$

$\therefore i_x = (\frac{1}{R_S} + \frac{1}{r_o} + g_m) V_x$

$R_{out} = V_x / i_x = R_S \| r_o \| \frac{1}{g_m}$

$A_i = i_o / i_i$

$= (V_o / R_{out}) / (V_i / R_{in}) = A_V \cdot \frac{R_{in}}{R_{out}} = A_V \cdot \frac{R_G}{R_S \| r_o \| \frac{1}{g_m}}$

c)

$g_m = \sqrt{2 K_n I_D (1 + \lambda V_{DS})} = 0.4662$ mS

$r_o = (\frac{1}{\lambda} + V_{DS}) / I_D = 289.92\ k\Omega$

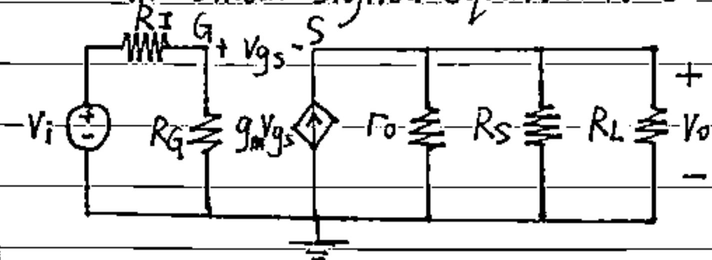
$R_{in} = 50 k\Omega$

$R_{out} = 1924.38\ \Omega$

$A_V = 0.8$

$A_i = 20.786$

2.b) the small signal equivalent circuit :



$R_L' = r_o \| R_S \| R_L$

$A_{vt} = V_S / V_g = g_m V_{gs} R_L' / V_{gs} + g_m V_{gs} R_L' = \dfrac{g_m R_L'}{1 + g_m R_L'}$

$\therefore A_V = V_o / V_i = A_{vt} \times \dfrac{R_G}{R_G + R_I}$

$$= \frac{g_m \cdot R_G \cdot (r_o \| R_S \| R_L)}{(R_G + R_I) \cdot [1 + g_m (r_o \| R_S \| R_L)]}$$

$R_{in} = R_G$

$\because i_x = \dfrac{V_x}{R_S} + \dfrac{V_x}{r_o} - g_m V_{gs}$; $V_{gs} = -V_x$

$\therefore i_x = (\frac{1}{R_S} + \frac{1}{r_o} + g_m) V_x$

$R_{out} = V_x / i_x = R_S \| r_o \| \frac{1}{g_m}$

$A_i = i_o / i_i$

$= (V_o / R_{out}) / (V_i / R_{in}) = A_V \cdot \dfrac{R_{in}}{R_{out}} = A_V \cdot \dfrac{R_G}{R_S \| r_o \| \frac{1}{g_m}}$

c)

$g_m = \sqrt{2 K_n I_D (1 + \lambda V_{DS})} = 0.4662 \ mS$

$r_o = (\frac{1}{\lambda} + V_{DS}) / I_D = 289.92 \ k\Omega$

$R_{in} = 50 k\Omega$

$R_{out} = 1924.38 \ \Omega$

$A_V = 0.8$

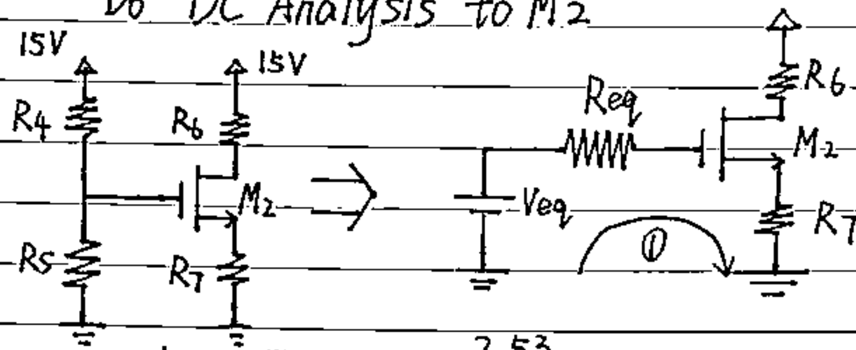
$A_i = 20.786$

Date No.

3 d) At V_{gs}, signal reach the maximum

$\because |V_{gs}| \le 0.2(V_{GS} - V_{TN})$

Do DC Analysis to M_2



where $V_{eq} = \frac{2.53}{1+2.53} \times 15 = 10.75\ V$

$R_{eq} = R_4 \parallel R_5 = 0.717\ M\Omega$

KVL 1 : $\because I_G = 0$, $V_{eq} = V_{GS} + I_D R_S$

$10.75 = V_{GS} + 0.5 \times 1.5m\ (V_{GS} - 1)^2 \times 3k$

$2.25 V_{GS}^2 - 3.5 V_{GS} - 8.5 = 0$

$V_{GS} = 2.87\ V$

$\therefore |V_{gs}| \le 0.374V$

$\therefore \left|V_i \times \frac{r_\pi \| R_1}{R_I + r_\pi \| R_1} \times A_{v t,1}\right| \le 0.374$

$V_i \le 1.635\ mV$

4 a) in DC Analysis without early effect

$I_{C1} = I_{S0} \cdot (A_{E1}/A) \cdot e^{V_{BE}/V_T}$

$I_{C2} = I_{S0} (10 A_{E1}/A) \cdot e^{V_{BE}/V_T}$

$I_{B1} = I_{C1}/\beta \qquad I_{B2} = I_{C2}/\beta$

$MR = \frac{I_{out}}{I_{REF}} = \frac{I_{C2}}{I_{C1} + I_{B1} + I_{B2}} = \frac{10}{1 + \frac{11}{\beta}}$

b) with early effect

$I_{C1} = I_{S0} \cdot (A_{E1}/A) \cdot e^{V_{BE}/V_T} \cdot (1 + \frac{V_{in}}{V_A})$

$I_{C2} = I_{S0} \cdot (10 A_{E1}/A) \cdot e^{V_{BE}/V_T} (1 + \frac{V_{out}}{V_A})$

$MR = \frac{10 \cdot (1 + V_{out}/V_A)}{1 + V_{in}/V_A + \frac{11}{\beta}}$

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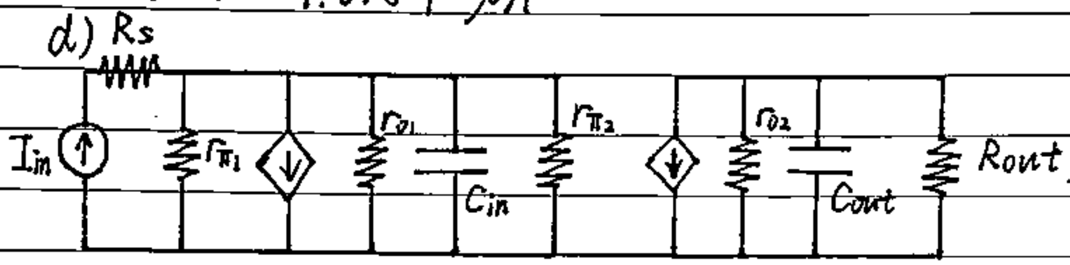
4 c) set I_{out} as x

$$V_{out} = V_{CC} - I_{out} \cdot R_{out}$$

$$MR = \frac{10 + 10 \cdot (5 - x \cdot 10^5)/50}{1 + \frac{0.7}{50} + \frac{11}{100}} = \frac{x}{1\mu}$$

$\Rightarrow x = 9.6154\ \mu A$

d)



e) & f) didn't have time to finish 🙁

Tips: 1. a) op-amp analysis
b) diodes circuit analysis (iteration method)
2. simple BJT / MOSFET circuit DC & AC analysis
3. Multi-Stage or Differential Amplifiers
⇓ Based on simple structure in Q2
⇓ Try to remember the result derived in ~~lect~~ slides
4. Current Mirror + Frequency Response

Most of us didn't have enough time to finish.
If you are out of time, just leave the derived equation there and skip calculation part. (Especially for Q3)
Try as many PYP papers as you can to be familiar with the types of questions.
Good luck
祝好
陈