NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2020-2021

EE3019 - INTEGRATED ELECTRONICS

November / December 2020 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer all 4 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.
6. A list of Formulae is provided in the Appendix A on page 7.

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1. (a) The pMOS pass-transistor circuit is depicted in Figure 1. Assume that $\mu_p C_{ox} = -50\ \mu A/V^2$, $\left(\frac{W}{L}\right)_p = \frac{56nm}{28nm}$, $V_{DD} = 1.2$ V, $V_{tp} = -0.47$ V, $C_L = 25$ fF and v_{out} changes from 0 V to 1.2 V.

   (i) Identify the regions of operation and determine the drain current, i_{DP}, of the pMOS transistor when $v_{out} = 0$ V and $v_{out} = 0.6$ V.

   (ii) Determine the propagation delay, t_{pLH}, of the circuit.

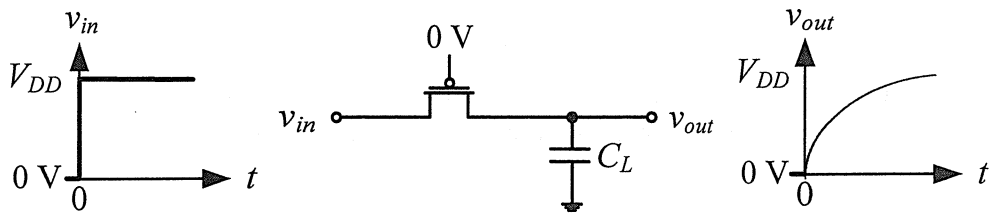

Figure 1

(11 Marks)

Note: Question No. 1 continues on page 2.

(b) The pull-up network of a CMOS logic circuit is depicted in Figure 2.

(i) Complete the CMOS logic circuit by designing the corresponding pull-down network. Derive the logic function of the circuit.

(ii) Assume that the $\left(\frac{W}{L}\right)$ ratio of the pMOS transistor of an inverter is $\left(\frac{2}{1}\right)$ and that the length of all transistors is 28 nm. Determine the $\left(\frac{W}{L}\right)$ ratio of the pMOS transistors in the pull-up network such that the driving capability of the pull-up network designed for the worst-case scenario is equal to that of the inverter. Note that all $\left(\frac{W}{L}\right)$ ratios should be in integer and in smallest possible sizes.

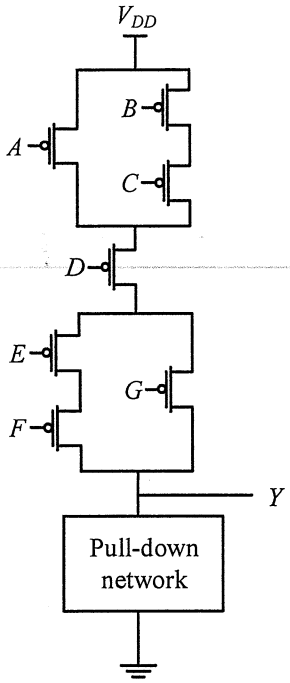

Figure 2

(11 Marks)

(c) Suggest a method to overcome the shortcoming(s) of the pass-transistor circuit without resorting to a transmission gate circuit.

(3 Marks)

2. (a) Draw a circuit schematic of a 2-nMOS transistor with 2-polysilicon resistor SRAM cell and a 4-transistor CMOS SRAM cell. Briefly compare their circuit area, power dissipation and operating speed.

(10 Marks)

(b) The equivalent circuit of a feedback amplifier is depicted in Figure 3. Assume that $R_i = 5\ \text{k}\Omega$, $R_o = 4\ \text{k}\Omega$, R_s is negligible, $v_{in} = 80\ \text{mV}$, $v_{fb} = 99\ \text{mV}$ and $v_{out} = 4\ \text{V}$.

(i) Identify the feedback configuration and determine the feedback factor, β.

(ii) Determine the open-loop gain and closed-loop gain of the amplifier.

(iii) Determine the input impedance, R_{if}, and the output impedance, R_{of}.

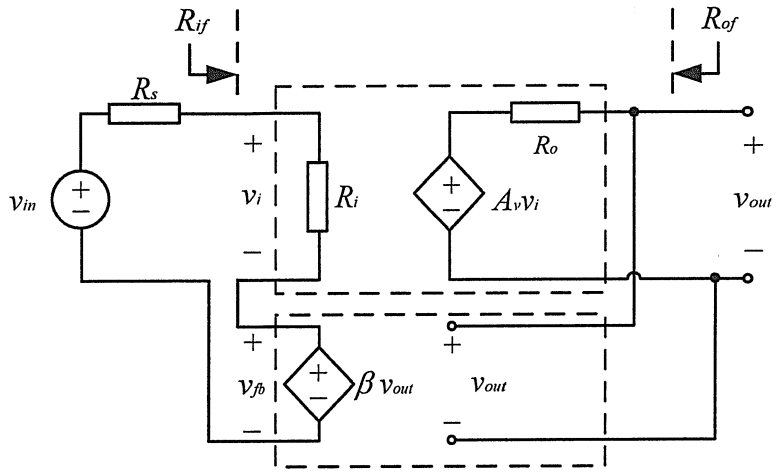

Figure 3

(12 Marks)

(c) Explain why the open-loop gain of the negative feedback amplifier should be large.

(3 Marks)

3. A simple bias circuit and an improved bias circuit are depicted in Figures 4(a) and 4(b), respectively, on page 5. Assume the following:

- all transistors are identical;
- thermal voltage, $V_T = kT/q = 26$ mV at room temperature, where k is Boltzmann's constant, T is temperature and q is charge; and
- $\frac{1}{\partial V_{BE}} \frac{\partial V_{BE}}{\partial T}$ = negative and $\frac{1}{\partial R} \frac{\partial R}{\partial T}$ = positive.

(a) State the mechanism of how a reference parameter is obtained in these bias circuits and two important attributes of a bias circuit.

(4 Marks)

(b) Derive an expression for I_{out} of the simple bias circuit in terms of I_{ref}/I_{S1} where I_{S1} is the saturation current of Q_1, and state any assumption(s). Explain why I_{out} is not independent of the supply voltage.

(7 Marks)

(c) From your expression in part (b) above and by analyzing the schematic of the improved bias circuit, plot a graph depicting the relationships between I_{C2} and I_{ref} for the improved bias circuit. Explain why the output of the improved bias circuit is independent of the supply voltage.

(6 Marks)

(d) Derive an expression for the Fractional Temperature Coefficient, $TC_F(I_{out})$, of the improved bias circuit in terms of $TC_F(V_{BE})$ and $TC_F(R)$. Comment if the $TC_F(I_{out})$ is sufficient for practical applications.

(6 Marks)

(e) Most commercial bias circuits are based on the Bandgap bias circuit. State and explain one important attribute of the op-amp employed in the Bandgap bias circuit.

(2 Marks)

Note: Question No. 3 continues on page 5.

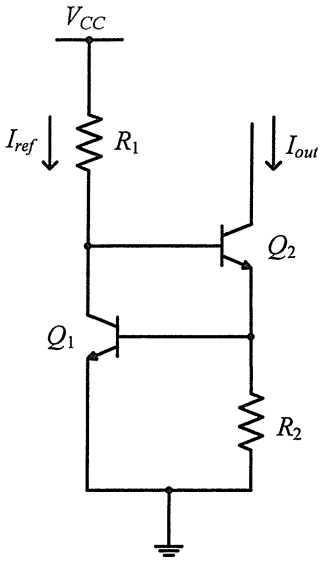

Figure 4(a)

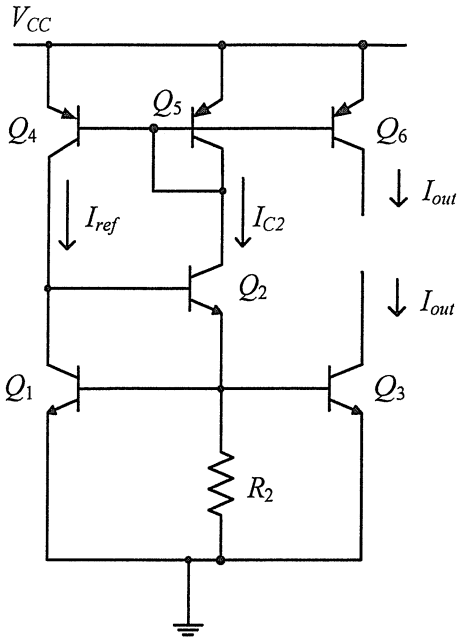

Figure 4(b)

4. A simple current mirror and a two-stage op-amp are depicted in Figures 5(a) and 5(b), respectively, on page 6.

   (a) State two important parameters of the simple current mirror.

   (3 Marks)

   (b) (i) Explain why it is inappropriate to design the differential input stage of the op-amp with load resistors, R_3 and R_4.

   (ii) Replace the load resistors, R_3 and R_4, with the simple current mirror. Draw the schematic of the redesigned input stage of the op-amp.

   (8 Marks)

   (c) Assume the following for the redesigned op-amp in part (b)(ii):

   - Three poles are located at 100 kHz, 10 MHz and 100 MHz;
   - DC open-loop voltage gain of the op amp is 10^4; and
   - The parameters of the transistors are:
     $|V_t| = 0.8$ V, $\mu_n C_{ox} = 30\ \mu A/V^2$, $\mu_p C_{ox} = 20\ \mu A/V^2$, and $|V_A| = 50$ V.

Note: Question No. 4 continues on page 6.

(i) Determine if the op-amp is stable.

(ii) Assuming that the aspect ratio of the transistors in the simple current mirror in the redesigned input stage of the op-amp is 40/8, determine the DC voltage gain of the input stage of the op-amp.

(12 Marks)

(d) Explain how you can improve the Power Supply Rejection Ratio of the op-amp and discuss the implications, if any.

(2 Marks)

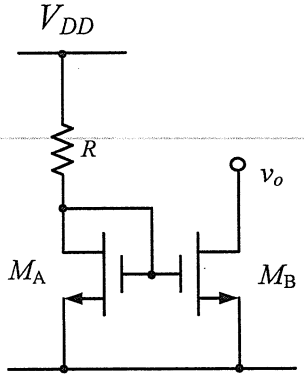

Figure 5(a)

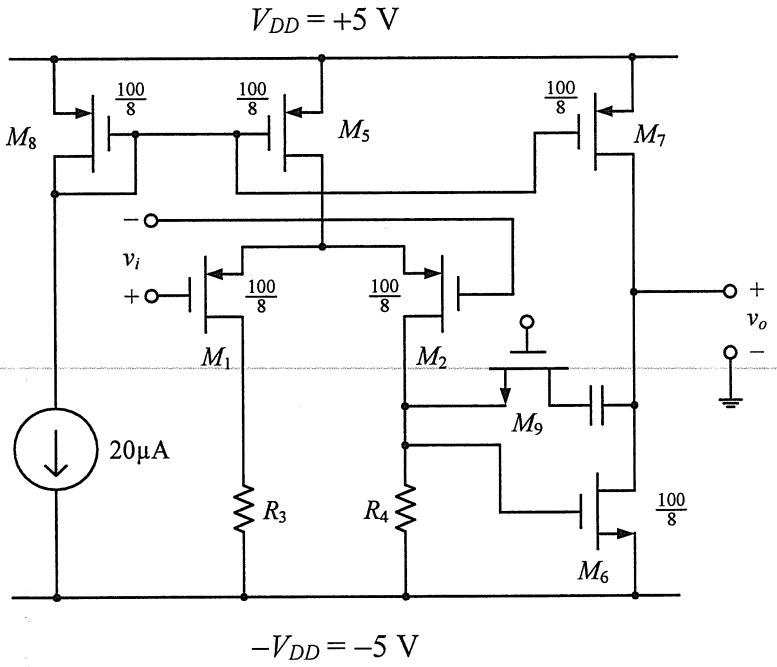

Figure 5(b)

Appendix A

List of Formulae

$$V = I\,Z \qquad P = I\,V$$

$$Z_L = j\omega L \qquad Z_C = \frac{1}{j\omega C}$$

$$\sum_{m=1}^{M} v_m = 0 \qquad \sum_{n=1}^{N} i_n = 0$$

$$v = L\frac{di}{dt} \qquad i = C\frac{dv}{dt}$$

$$S = V\,I^{*} \qquad i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

$$V_T = \frac{kT}{q} \qquad i_C \approx I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]$$

$$i_E = i_C + i_B \qquad \beta = \frac{i_C}{i_B}$$

$$\alpha = \frac{\beta}{1+\beta} \qquad A + B + C = \overline{\overline{A}\,\overline{B}\,\overline{C}}$$

$$ABC = \overline{\overline{A} + \overline{B} + \overline{C}} \qquad \tau_p = \frac{C_{load} \times \Delta V}{I_{avg}}$$

$$i_{Dn(LIN)} = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left((v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^{\,2}\right) \qquad A_f = \frac{A}{1+A\beta}$$

$$i_{Dn(SAT)} = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad f = \frac{1}{2n\,\tau_p}$$

$$A(s) = A_m F_H(s) = \frac{A_m}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \qquad V_o = A_1A_2(V_i - \beta V_o) + A_1V_n$$

$$g_m = 2\frac{I_D}{(V_{GS} - V_t)} \qquad r_o = \frac{V_A}{I_D}$$

END OF PAPER

EE3019 INTEGRATED ELECTRONICS

Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.