NANYANG TECHNOLOGICAL UNIVERSITY SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

ACADEMIC YEAR 2020-2021
SEMESTER 2

EE3019 INTEGRATED ELECTRONICS

TUTORIAL 3

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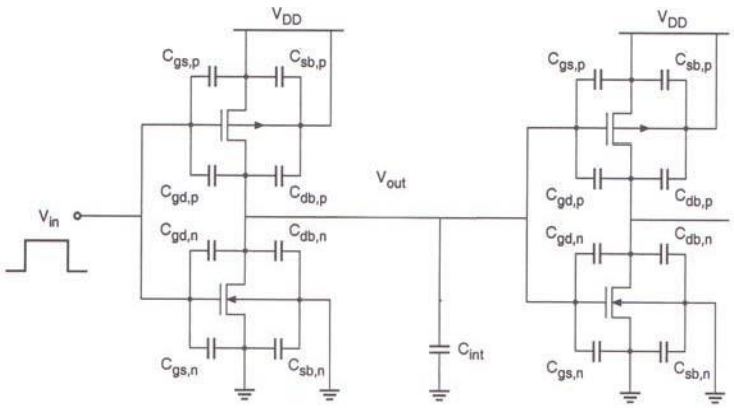
1. Consider a CMOS inverter fabricated in a 0.25μm process as depicted in Figure 3.1. Based on the parameters given below, calculate the dynamic power dissipation of inverter 1 when the inverter is clocked at 500MHz:

   nMOS: C_{gsn}= 0.7875 fF, C_{gdn}= 0.1125 fF, C_{sbn}= 1 fF, C_{dbn}= 1 fF,
   pMOS: C_{gsp}= 2.3625 fF, C_{gdp}= 0.3375 fF, C_{sbp}= 1 fF, C_{dbp}= 1 fF,
   Interconnect capacitance: C_{int}=0.2 fF, Supply Voltage, V_{DD}=2.5V



Inverter 1 **Inverter 2**

Figure 3.1 [Answer: 19.5 μW]

2. Consider the logic gate given in Figure 3.2.
   (a) What is the logic function implemented by this CMOS transistor network?
   (b) Label the sizes of nMOS and pMOS devices such that the gate has the same drive as the inverter with W_n = 0.25 μm and W_p = 0.5 μm.

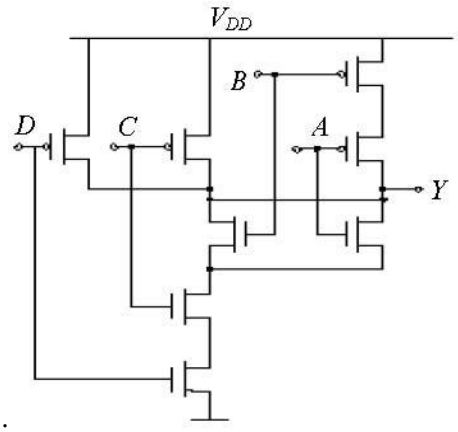


Figure 3.2

3. The transmission gate of Figure 3.2(a) and 3.2(b) is fabricated using a CMOS process technology for which $\mu_n C_{ox} = 50\mu A/V^2$ and $\mu_p C_{ox} = 20\mu A/V^2$. $V_{tn} = |V_{tp}|$, $V_{t0} = 1$ V, $\gamma = 0.5\ V^{1/2}$, $2\varphi_f = 0.6$ V, and $V_{DD} = 5$ V. Let Q_N and Q_P be the minimum size possible with this process, $(W/L)_n = (W/L)_p = 4\mu m/2\mu m$. The total capacitance at the output node is 70fF.

   (a) Find $i_{DN(0)}$, $i_{DP(0)}$, $i_{DN(tPLH)}$, $i_{DP(tPLH)}$, and t_{PLH} for Figure 3.3(a).

   (b) Find $i_{DN(0)}$, $i_{DP(0)}$, $i_{DN(tPHL)}$, $i_{DP(tPHL)}$, and t_{PHL} for Figure 3.3(b). At what value of v_o will Q_P turn off?

   (c) Find t_p.

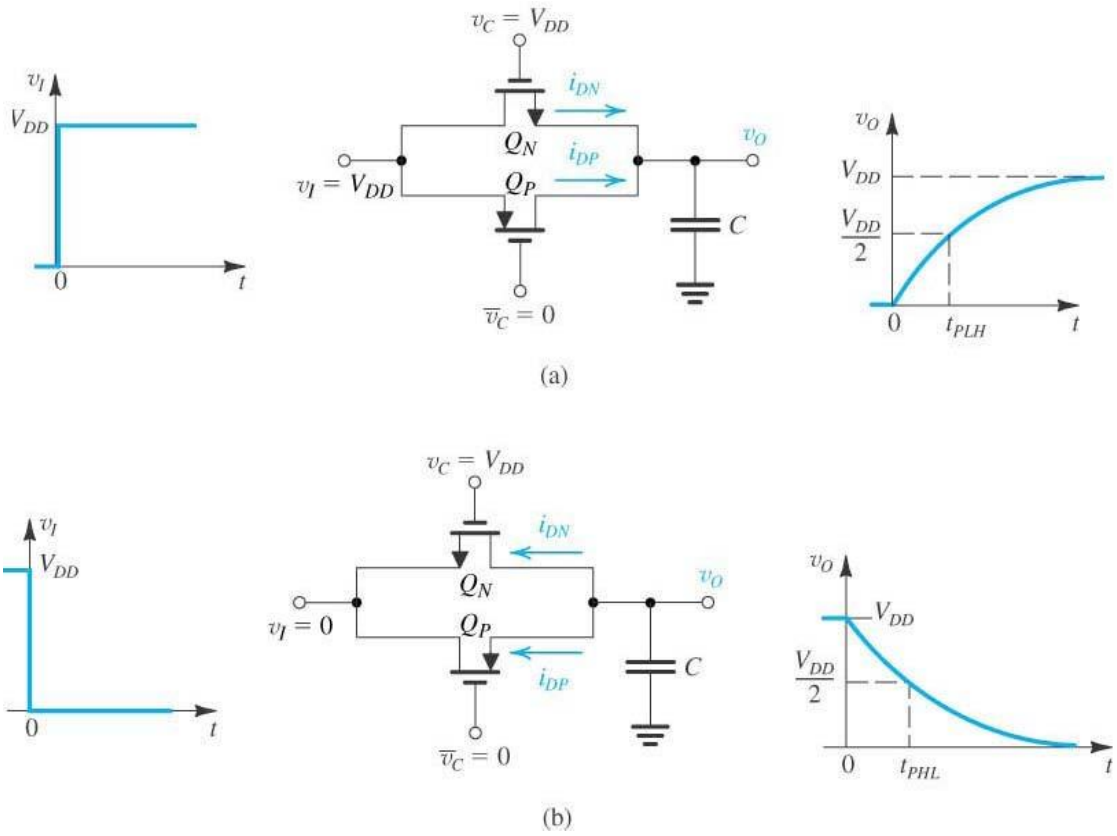


Figure 3.3

[Answer: 0.24ns, 0.19ns, 1.6V, 0.215ns]