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INTEGRATED ELECTRONICS

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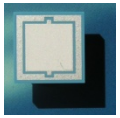
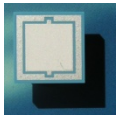


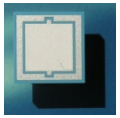
Topics

1. Power Supplies
2. Bias Circuits
3. **Operational Amplifiers**
4. Applications of Operational Amplifiers



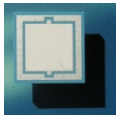
Reference Textbooks

1. Sedra and Smith, *Microelectronic Circuits*, 5th Edition, Oxford University Press, 2004.
2. Gray, Hurst, Lewis and Meyer, *Analysis and Design of Analogue Integrated Circuits*, 4th Edition, John Wiley & Sons, 2001.
3. Franco S, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd Edition, McGraw-Hill, 2002.



Operational Amplifiers

1. Introduction
2. Single-Stage Op Amp
3. Two-Stage Op Amp
4. Frequency Responses and Stability

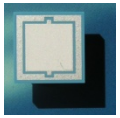


Introduction

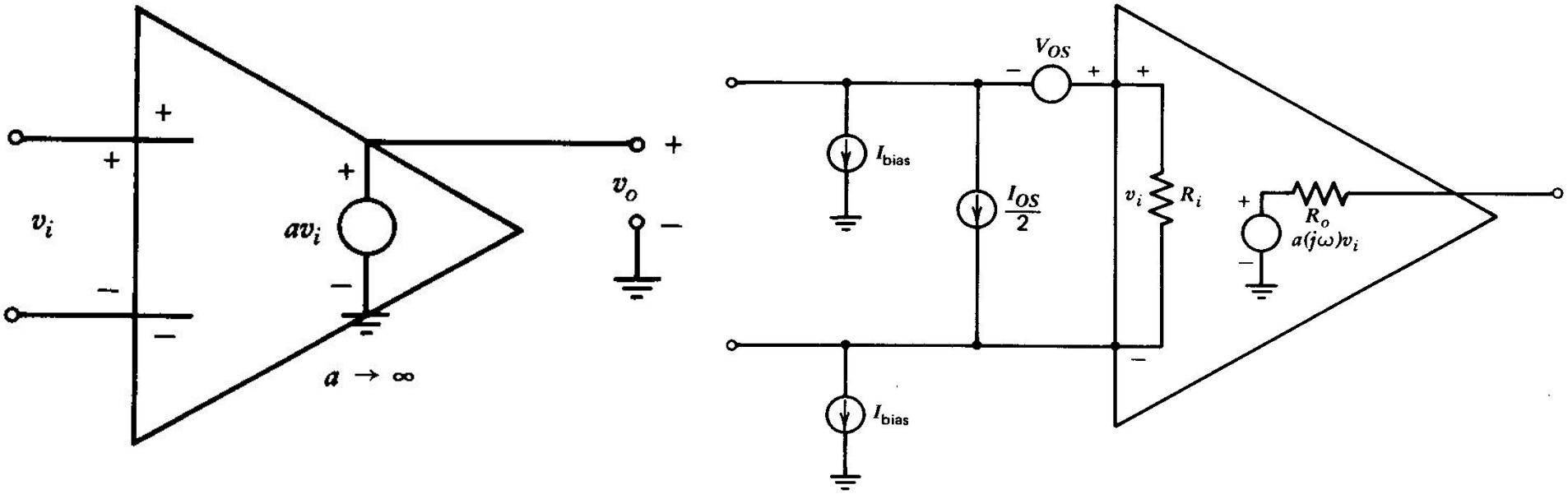
Op amp is a basic analogue building block.

An ideal op amp has the following properties: Infinite gain over infinite bandwidth, infinite input impedance, and zero output impedance.

A practical op amp typically have the following properties:Finite gain (typically 100dB at dc), finite bandwidth, non-zero input bias and offset currents (I_{bias} and I_{OS}), input offset voltage (V_{OS}), limited common-mode rejection ratio, finite input resistance, and non-zero output resistance

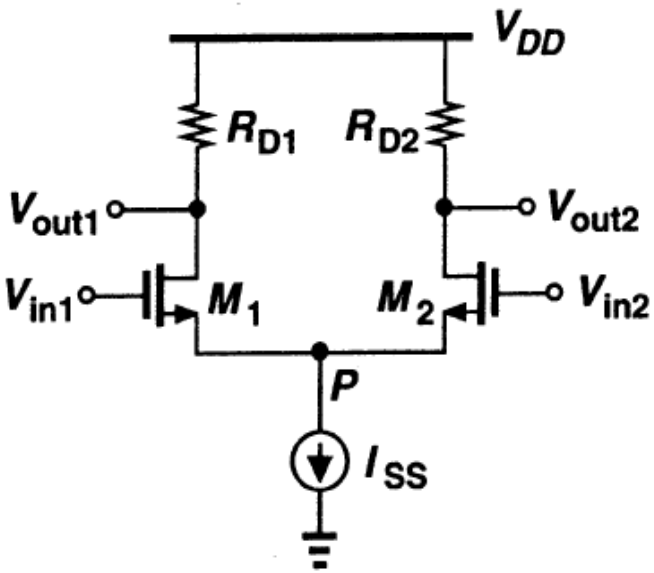


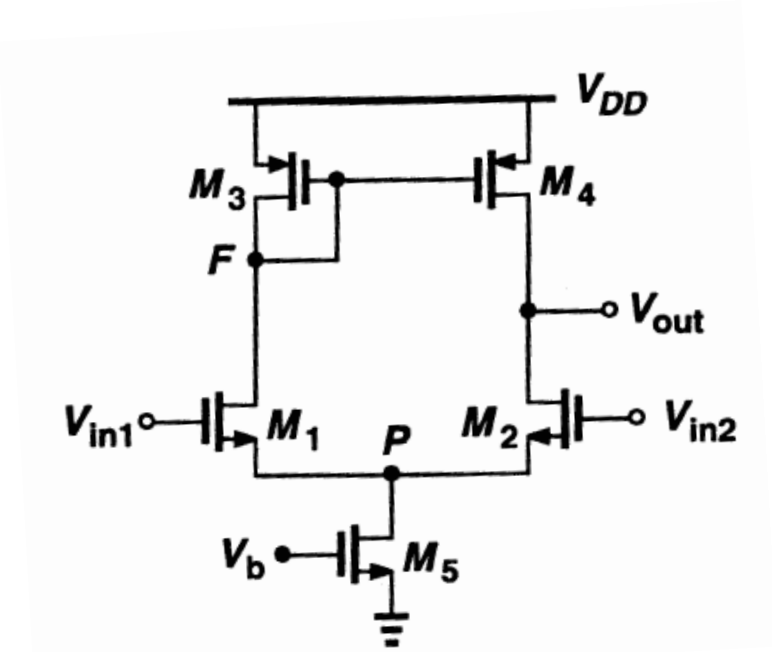
Introduction



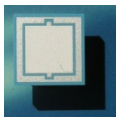
Models of an ideal and a practical op amps.

Single-Stage Op Amp





R_{D1} and R_{D2} are passive loads, while M_3 and M_4 are active loads.
Active load advantages: Minimizes number of passive elements needed, can produce very high gain in one stage, and inherent differential-to-single-ended conversion.
Active load disadvantages: No differential output available.



Single-Stage Op Amp

Assume that input to the gate of M_1 and M_2 are small inputs of $v_d/2$ and $-v_d/2$ respectively.

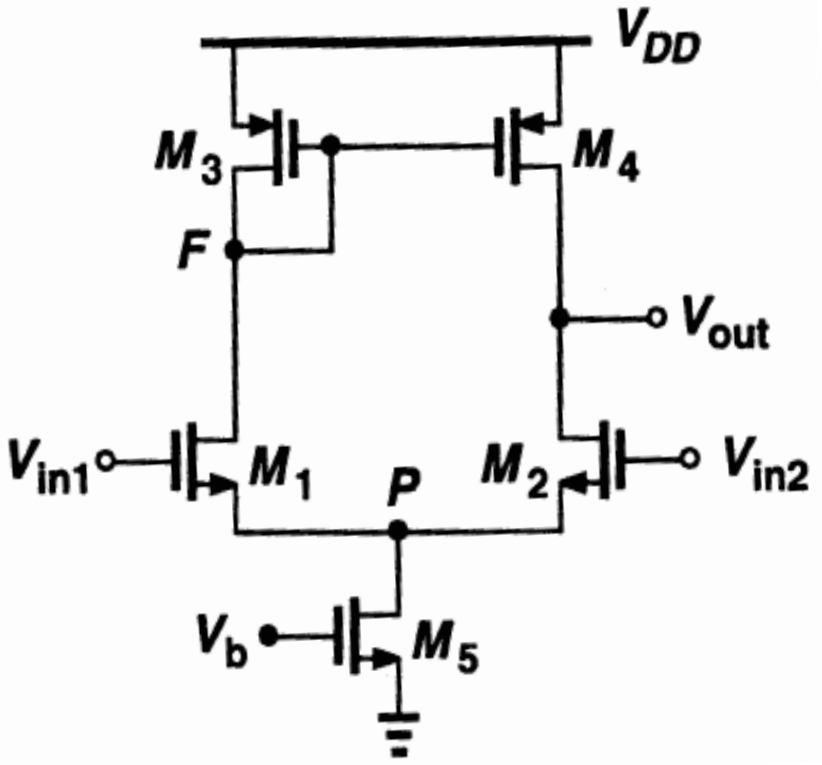
The small signal current in the drain of each transistor is $i_d=g_m v_d/2$.

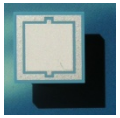
By inspection, due to the current mirror active load, the small signal output current is: $i_{out}=2i_d$.

The output voltage is: $v_{out}=2i_d(r_{o2}//r_{o4})$

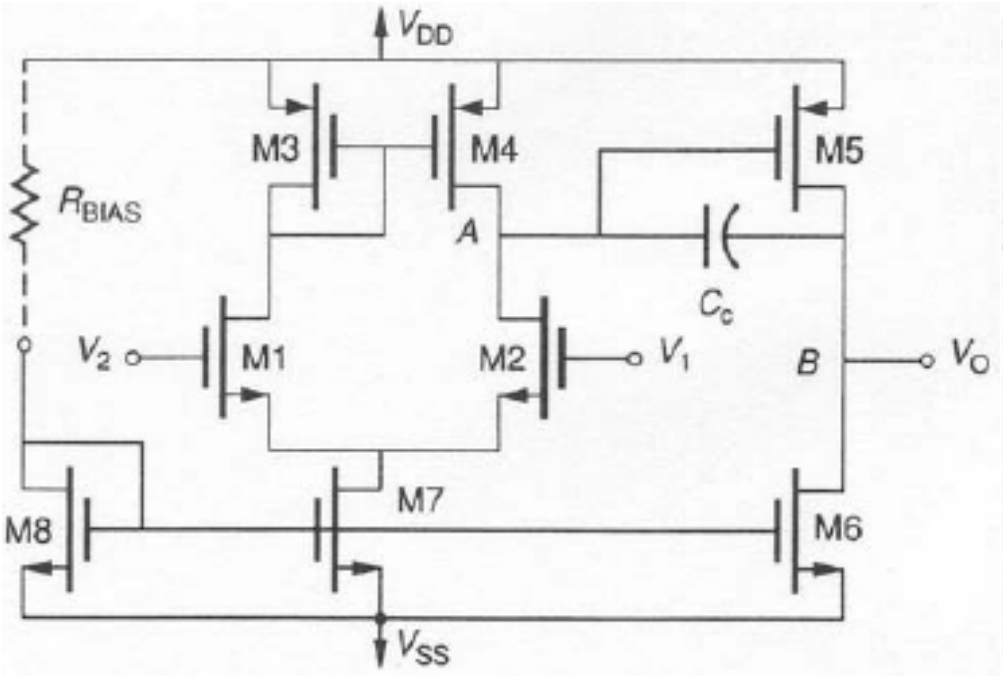
Hence the voltage gain is:

$A_V= v_{out}/v_d =g_{m2}(r_{o2}//r_{o4})$.

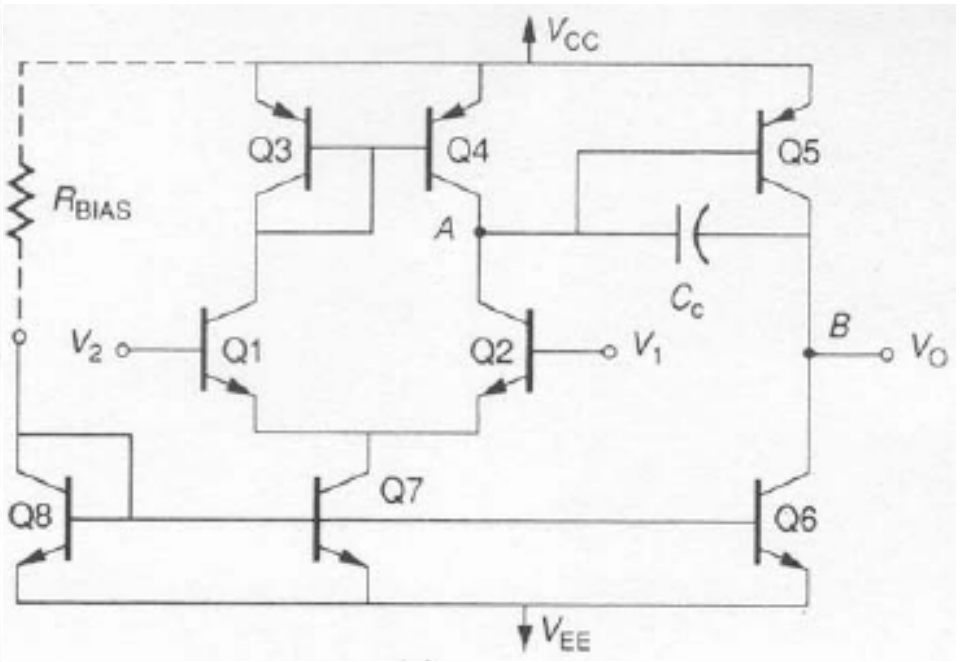




Two-Stage Op Amp



CMOS



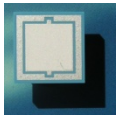
BJT

Two-Stage Op Amp

BJT op amps could be designed by replacing the CMOS transistors with BJT equivalents. The examples shown above do not have an output stage and are unable to drive large loads. They are designed as internal amplifiers in an IC where the load is usually fixed.

BJT op amp has higher gain. This is because for the same current, BJTs have a higher transconductance. CMOS op amp has a higher input resistance. This is because the gate of the CMOS transistors is a polysilicon isolated from substrate with an oxide layer.

It is often desirable (if feasible) to have FET (JFET more common than CMOS) inputs and BJTs used in the internal and output stages in an op amp design.



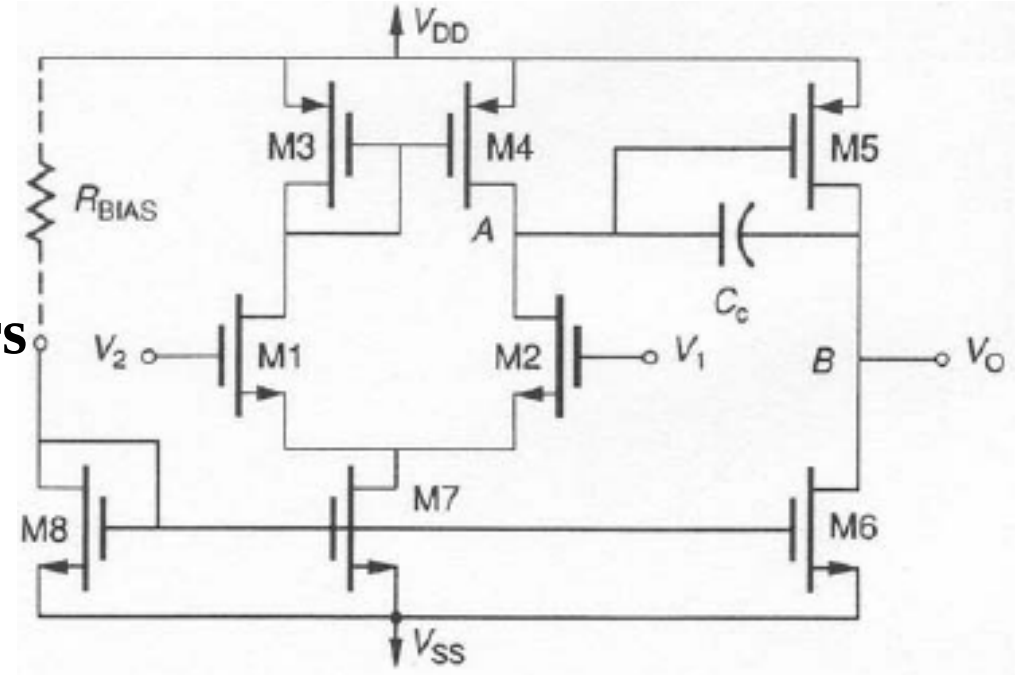
Two-Stage Op Amp

M_8 and R_{BIAS} form the bias circuit.

M_7 and M_8 form a current mirror where M_7 is the current source to the differential input stage.

M_1 and M_2 are the input transistors whose load comprises M_3 and M_4 which are a current mirror and active loads.

M_1-M_4 and M_7 form the first gain stage of the op amp.

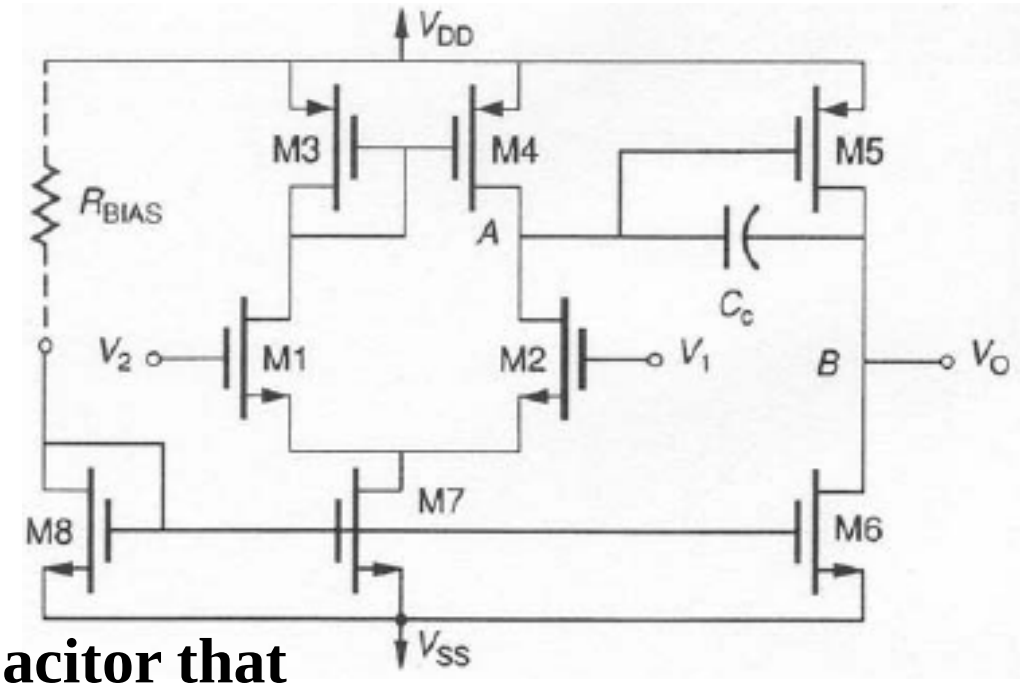


CMOS

Two-Stage Op Amp

M_6 and M_8 form a current mirror where M_6 is the active load for the common source amplifier formed by M_5.

M_5 and M_6 form the second gain stage of the op amp.



C_C is the Miller compensating capacitor that will cause the poles of the op amp to split. The pole at node A will dominate while the pole at B will move towards higher frequency.

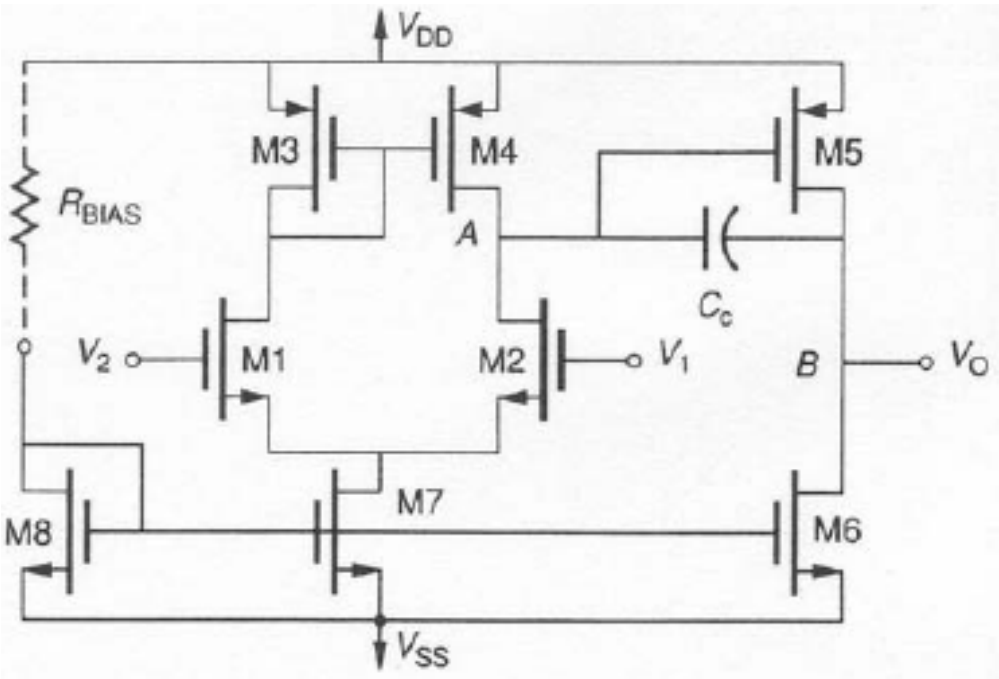
Two-Stage Op Amp

Input Common-Mode Range:

The input common-mode range can be determined by examining the input voltage range which ensures the associated MOSFETs are still operating in the saturation (active) region,

i.e. $V_{DS} \geq V_{GS}-V_{tn}$ **for NMOS**

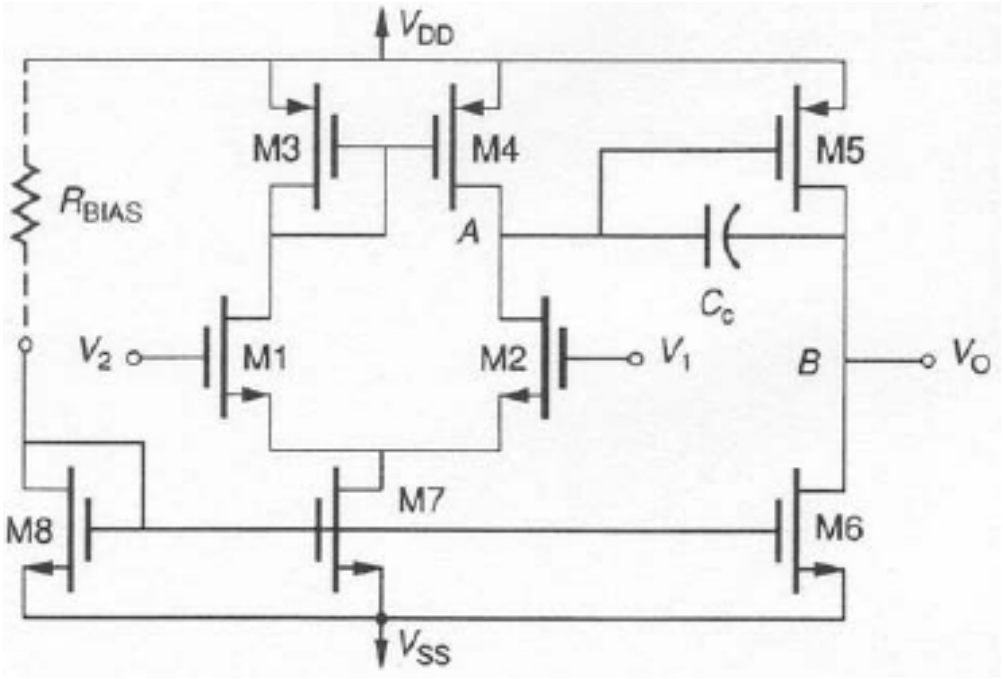
and $V_{SD} \geq V_{SG}-|V_{tp}|$ **for PMOS**



Two-Stage Op Amp

Output Voltage Range:

Similarly, the output voltage range can be determined by studying the range of output voltage which ensures the associated MOSFETs are still in the saturation region.



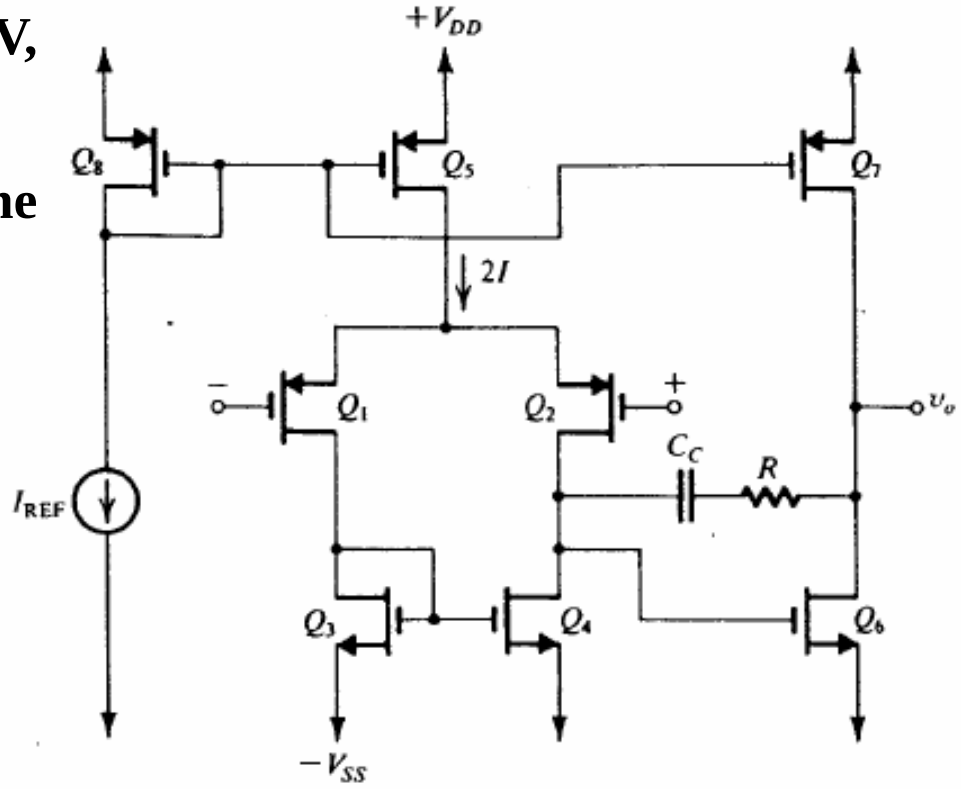
Two-Stage Op Amp

Example 1: Given that I_{REF} = 25μA, $|V_t|$ = 1V, $\mu_n C_{ox}$ = 20μA/V², $\mu_p C_{ox}$ = 10μA/V², V_{DD} = 5V, V_{SS} = 5V and $|V_A|$ = 25V.

The dimensions *W/L* in um/um of the transistors are:

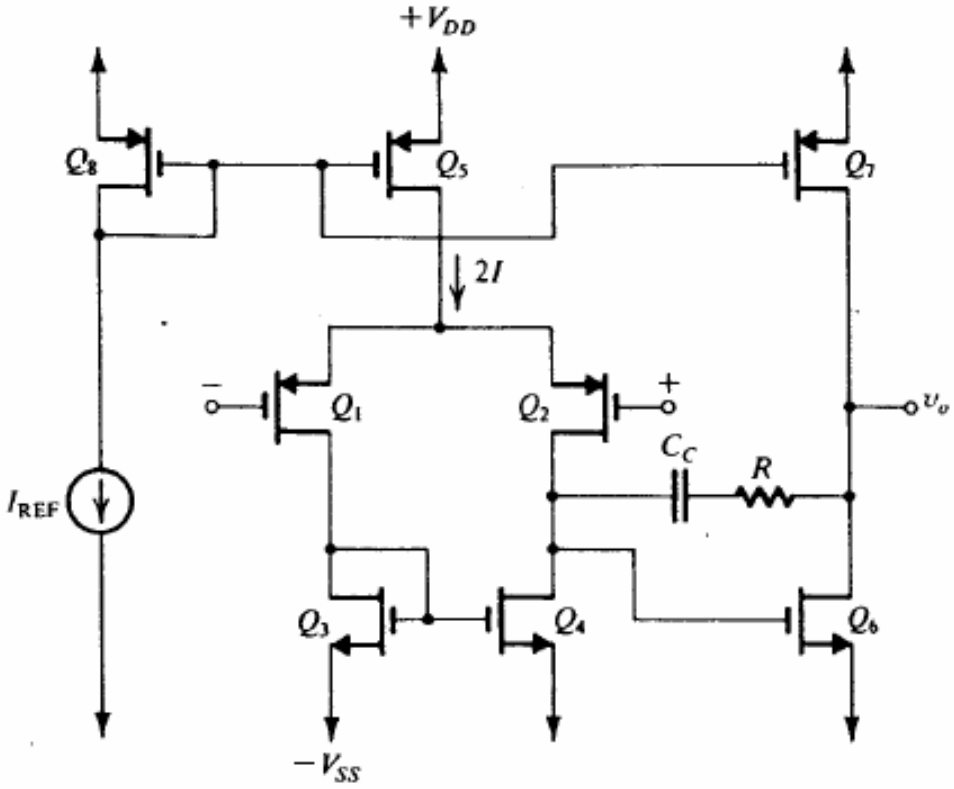
Q_1	Q_2	Q_3	Q_4
100/8	100/8	40/10	40/10
Q_5	Q_6	Q_7	Q_8
120/10	80/10	120/10	120/10

Determine the gain of the 2-stage amplifier and the input common-mode range and the output voltage range



Two-Stage Op Amp

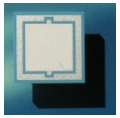
Bias Currents: Note that Q_8, Q_5 and Q_7 are current mirrors, we can determine their bias drain currents from the given transistor dimensions $I_{D5} = I_{D8} = I_{D7} = 25\mu A$. Since Q_6 and Q_7 are in series, $I_{D6} = I_{D7} = 25\mu A$. The bias current in Q_5 splits evenly between Q_1 and Q_2, therefore $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 12.5\mu A$.



Two-Stage Op Amp

Transconductance: Under normal operation, all the transistors operate in the saturation (linear) mode. Since I_D, W/L, and V_A are known, the transconductance g_m and output resistance r_o can be calculated respectively as: $g_m=2I_D/(V_{GS}-V_t)$ and $r_o=\lvert V_A\rvert/I_D$.

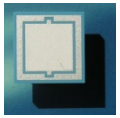
MOSFET	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
I_D (μA)	12.5	12.5	12.5	12.5	25	25	25	25
$\lvert V_{GS} \rvert$ (V)	1.4	1.4	1.6	1.6	1.6	1.6	1.6	1.6
g_m (μA/V)	62.5	62.5	42	42	83.3	83.3	83.3	83.3
r_o (MΩ)	2	2	2	2	1	1	1	1



Two-Stage Op Amp

By inspection gain for the first stage $A_{V1} = -g_{m2}(r_{o2}//r_{o4}) = -62.5$ V/V, gain for the second stage $A_{V2} = -g_{m6}(r_{o6}//r_{o7}) = -42$, and the overall gain $A_V = A_{V1} \times A_{V2} = 2625$ V/V.

To ensure proper operation of the differential amplifier, all the transistors must be in the active region. The input common-mode voltage $V_{IC} = V_{G1} = V_{G2}$ and the output voltage $V_O = V_{D7} = V_{D6}$ must be limited to ensure all the transistors are active.



Two-Stage Op Amp

The upper limit of V_{IC} is determined by examining the condition for Q_5 to be in the active region, i.e., $V_{SD5} \geq V_{SG5} - |V_t|$ or $-V_{D5} \geq -V_{G5} - |V_t|$

$\rightarrow \quad V_{D5} \leq V_{G5} + |V_t|$

$\rightarrow \quad (V_{IC} + V_{SG1}) \leq (V_{DD} - V_{SG5}) + |V_t|$

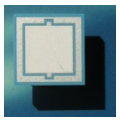
$\rightarrow \quad V_{IC} \leq (V_{DD} - V_{SG5}) + |V_t| - V_{SG1} = 5 - 1.6 + 1 - 1.4 = 3.0$ V.

The lower limit of V_{IC} is determined by examining the condition for Q_1 to be in the active region, i.e., $V_{SD1} \geq V_{SG1} - |V_t|$ or $V_{D1} \leq V_{G1} + |V_t|$

$\rightarrow \quad (-V_{SS} + V_{GS3}) \leq V_{IC} + |V_t|$

$\rightarrow \quad V_{IC} \geq (-V_{SS} + V_{GS3}) - |V_t| = (-5 + 1.6) - 1 = -4.4$ V

i.e. the max and min input common-mode voltages are +3.0 and - 4.4 V



Two-Stage Op Amp

To determine the output voltage range, we examine the condition for Q_6 and Q_7 to be in the active region.

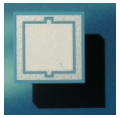
For Q_7, $V_{SD7} \geq V_{SG7} - |V_t|$ or $V_{D7} \leq V_{G7} + |V_t|$

$\rightarrow \quad V_O \leq (V_{DD} - V_{SG7}) + |V_t| = 5 - 1.6 + 1 = 4.4$ V

For Q_6, $V_{DS6} \geq V_{GS6} - V_t$ or $V_{D6} \geq V_{G6} - V_t$.

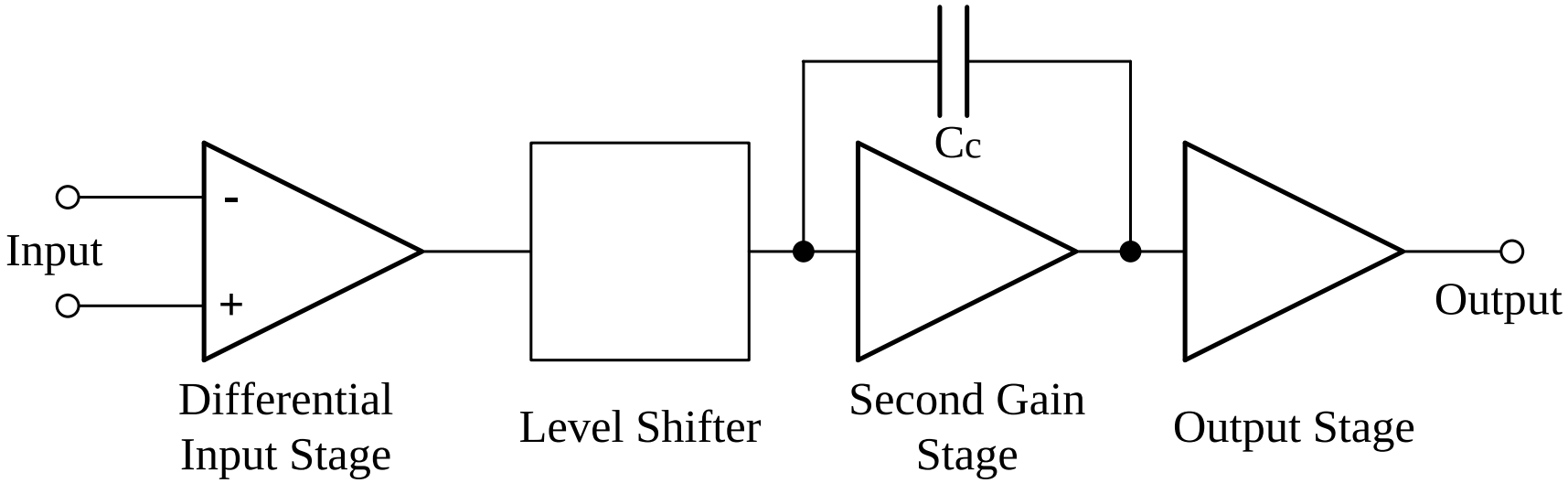
$\rightarrow \quad V_O \geq (-V_{SS} + V_{GS6}) - V_t = -5 + 1.6 - 1 = -4.4$ V.

i.e. the max and min output voltages are +4.4 and -4.4 V.



Frequency Response and Stability

The figure below shows a block diagram of a typical configuration of an op amp. Note an output stage is added to drive a large load. The op amp has very high gain, it may become unstable. Also, the behavior of the op amp depends upon the frequency of the input signal.



Frequency Response and Stability

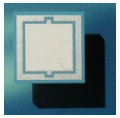
The gain of the uncompensated op amp can be expressed as:

$$a(j\omega) = \frac{a_0}{[1 + j(\omega/\omega_1)][1 + j(\omega/\omega_2)][1 + j(\omega/\omega_3)]}$$

where a_0 is the dc gain and ω_1, ω_2 and ω_3 are the poles. For practical purposes, only 3 poles are considered. The mathematical expressions for gain and phase are given by:

$$|a(\omega)| = \frac{a_0}{\sqrt{[1 + (\omega/\omega_1)^2][1 + (\omega/\omega_2)^2][1 + (\omega/\omega_3)^2]}}$$

$$\angle a(\omega) = -\left[\tan^{-1}(\omega/\omega_1) + \tan^{-1}(\omega/\omega_2) + \tan^{-1}(\omega/\omega_3)\right]$$



Frequency Response and Stability

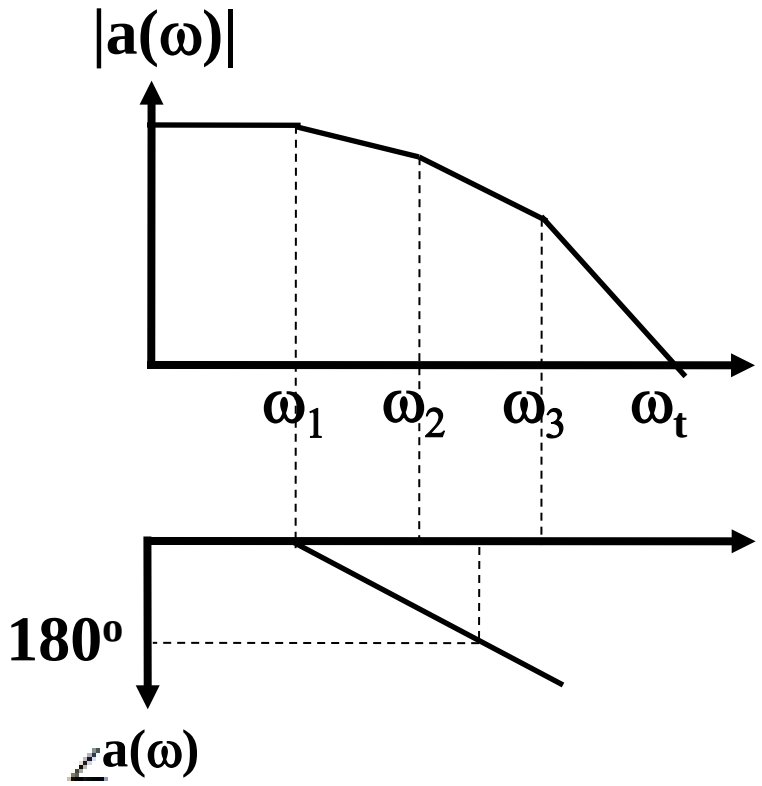
Between ω_1 and ω_2 the roll-off is -20dB/dec.

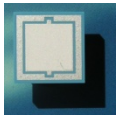
Between ω_2 and ω_3 the roll-off is -40dB/dec.

Beyond ω_3, the roll-off is -60dB/dec.

The phase lag of uncompensated op amp may be in excess of -180° => possibility of instability.

Frequency at -180° is between ω_2 and ω_3.





Frequency Response and Stability

Example 2: Determine $|a(\omega_{-180^\circ})|$ and ω_{-180° of the uA702 op amp with the frequency response:

$$|a(\omega)| = \frac{3600}{\sqrt{\left[1+(\omega/1\times10^6\times2\pi)^2\right]\left[1+(\omega/4\times10^6\times2\pi)^2\right]\left[1+(\omega/40\times10^6\times2\pi)^2\right]}}$$

By inspection, ω_{-180° is between ω_2 and ω_3, i.e. between 4MHz and 40MHz. By trial & error:

$$\angle a(20\times10^6\times2\pi) = -192.4^\circ;$$

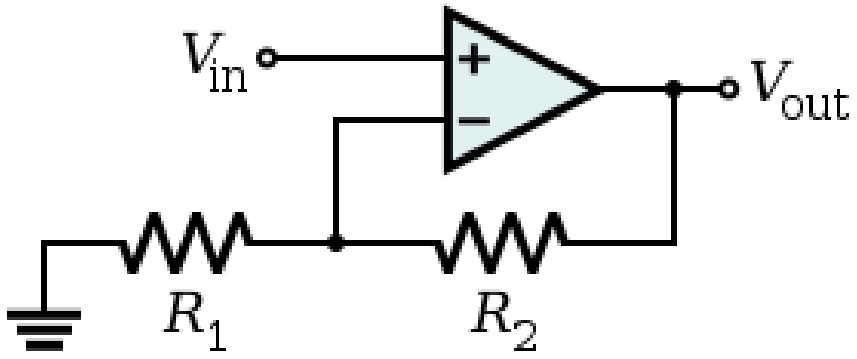
$$\angle a(14\times10^6\times2\pi) = -179.3^\circ;$$

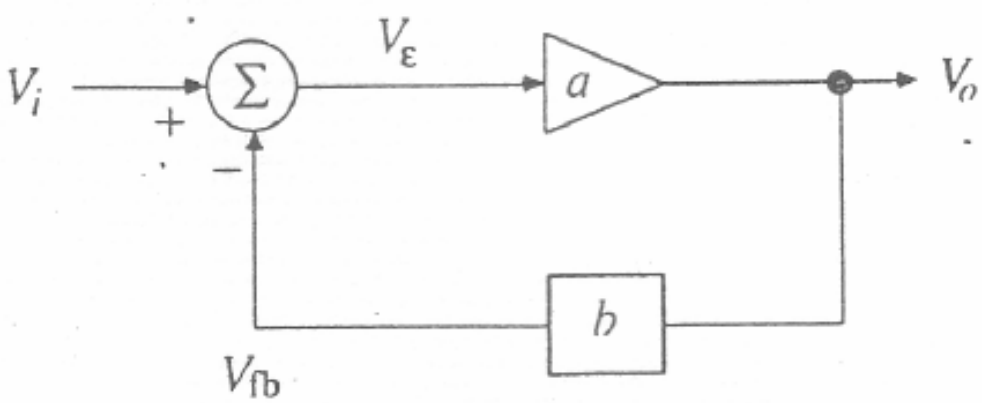
$$\angle a(14.3\times10^6\times2\pi) = -180^\circ$$

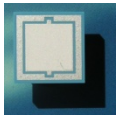
$$|a(14.3\times10^6\times2\pi)| = 63.7$$

Frequency Response and Stability

An op amp needs to work with external components in a closed-loop configuration. The left figure below is a non-inverting amplifier, which can be modeled by a feedback system shown in right figure.





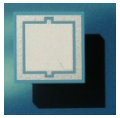


Frequency Response and Stability

For the feedback system, the closed-loop gain A_{cl} is expressed as:

$$A_{cl}(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{a(j\omega)}{1 + a(j\omega)b(j\omega)} = \frac{a(j\omega)}{1 + T(j\omega)}$$

where $a(j\omega)$ is the op amp gain, $b(j\omega)$ is the feedback factor, and $T(j\omega)$ is defined as the loop gain. For the non-inverting amplifier, we know that $b(j\omega) = R_1/(R_1+R_2)$ and at DC, that is, $\omega = 0$, the op amp has very high gain, the closed-loop gain is $A_{cl} = 1 + R_2/R_1$.



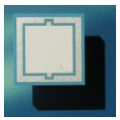
Frequency Response and Stability

For the feedback system, if the closed-loop gain A_{cl} goes to infinity, the system becomes unstable. Hence, the stability can be studied by solving the following equation: $1+T(j\omega) = 0$. This complex equation can be decomposed into two real equations:

$$|T(j\omega)|=1$$

$$\angle\, T(j\omega) = -180^{o}$$

When the combined phase shift experienced by the signal in propagating through the amplifier and the feedback network reaches -180°, the loop gain T becomes algebraically negative, the system changes from a negative to positive feedback.



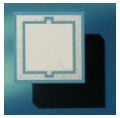
Frequency Response and Stability

There are 3 possibilities at $\omega = \omega_{-180^\circ}$:

If $|T(j\,\omega_{-180^\circ})| < 1$, with zero input, output will stabilize to zero.

If $|T(j\,\omega_{-180^\circ})| = 1$, circuit may produce a nonzero output for zero input. System is capable of providing as well as sustaining its own output. Once started, the circuit becomes unresponsive to external input.

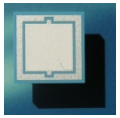
If $|T(j\,\omega_{-180^\circ})| > 1$, circuit will oscillate until non-linearity of the amplifier reduce the loop gain to exactly unity. The circuit will maintain sustained oscillation → an oscillator!!



Frequency Response and Stability

To test whether a closed-loop op amp is stable, a systematic procedure is to check either the Gain Margin or Phase Margin.

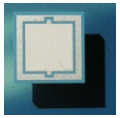
The procedures to check the Gain Margin is as follows:
Look for the frequency ω_{-180° where the loop gain (not gain!) yields an overall phase shift of -180°, i.e. $\angle T(j\omega_{-180^\circ}) = -180^\circ$
Determine $|T(j\omega_{-180^\circ})|$, If $|T(j\omega_{-180^\circ})| < 1$ => stable



Frequency Response and Stability

To test whether a closed-loop op amp is stable, a systematic procedure is to check either the Gain Margin or Phase Margin.

The procedure to check the Phase Margin is as follows:
Look for the frequency $\omega_{loop\ gain=1}$ where $|T(j\omega_{loop\ gain=1})| = 1$
Determine the phase at $\omega_{loop\ gain=1}$, i.e. $\angle T(j\omega_{loop\ gain=1})$.
If $\angle T(j\omega_{loop\ gain=1}) < -180°$ or has a phase lag > 180° => unstable
In other words, if $180° + \angle T(\omega_{lop\ gain=1}) > 0°$ => stable



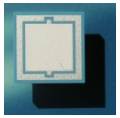
Frequency Response and Stability

A 'safety' margin in gain and phase is necessary to keep the system relatively stable against modest variations in circuit parameters such as thermal drift, ageing and etc.

A common rule-of-thumb (for practical systems) for minimum phase and gain margins is:

PM = 45° (some advocate 60°!!) and

GM = 10dB



Frequency Response and Stability

To make sure an op amp itself will not cause any stability problem, an internal compensation known as the dominant pole compensation technique is often used by adding a capacitor C_c as shown in the previous op amp. The 'trick' here is the deliberate creation of an additional pole for the open-loop response at a frequency low enough to ensure a constant roll-off of –20 dB/dec resulting in phase shift of –90° up to ω_t.