NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2020-2021

EE3019 – INTEGRATED ELECTRONICS

April / May 2021 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 4 pages.
2. Answer all 4 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.
6. A List of Formulae is provided in Appendix A on page 4.

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1. The parameters of the pMOS and nMOS transistors are given below:

pMOS $V_{tp} = -0.6$ V $\mu_p C_{ox} = 100\ \mu A/V^2$ $(W/L)_p = 5$

nMOS $V_{tn} = 0.6$ V $\mu_n C_{ox} = 250\ \mu A/V^2$ $(W/L)_n = 2$

$V_{DD} = 1.8$ V

Figure 1 is designed using the above device parameters.

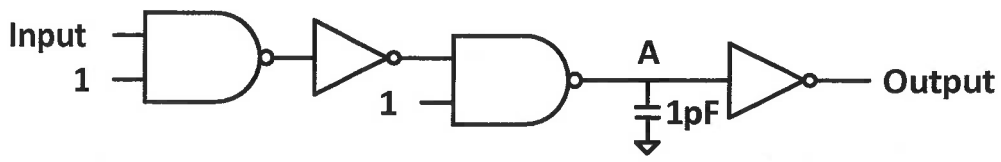

Figure 1

(a) Determine V_{IH}, V_{IL}, and V_{th} of the 2-input NAND gate and the inverter using the equivalent device sizes of the best case. Assume V_{out} for V_{IL} is 90% of V_{DD} and V_{out} for V_{IH} is 10% of V_{DD}.

(10 Marks)

Note: Question No. 1 continues on page 2.

(b) Calculate the noise margin of the 2-input NAND gate and the inverter.

(5 Marks)

(c) Determine the propagation delays (τ_{PHL} and τ_{PLH}) of the 2-input NAND gate driving node 'A' using the best case and briefly explain how to make the propagation delays identical.

(10 Marks)

2. (a) Figure 2 shows a schematic diagram of the 8-transistor clocked SR latch. The device parameters of the pMOS and nMOS transistors for M_1, M_2, M_3, and M_4 are given below:

pMOS $Vtp = -0.6$ V $\mu pCox = 40$ µA/V² $(W/L)p = 5$

nMOS $Vtn = 0.6$ V $\mu nCox = 100$ µA/V² $(W/L)n = 2$

$V_{DD} = 1.8$ V

Determine the minimum size of M5, M6, M7, and M8 for reliable set and reset operations. Assume that Q and QB need to be pulled down to $\frac{V_{DD}}{3}$.

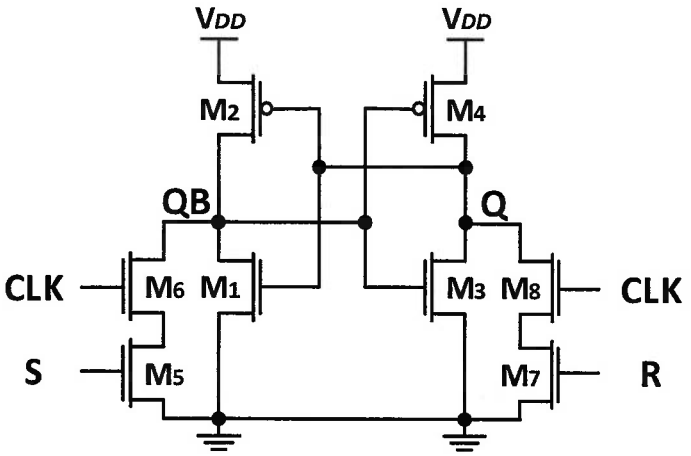

Figure 2

(10 Marks)

(b) Draw a schematic diagram of a 6-transistor SRAM cell and explain how to improve the reliability of read and write operations.

(10 Marks)

(c) Explain the characteristics of negative feedback in amplifiers.

(5 Marks)

3. (a) Draw schematic diagrams of basic and Wilson current mirrors using bipolar junction transistors and discuss their respective advantages.

(10 Marks)

(b) Consider the V_{BE}-based bias circuit illustrated in Figure 3 and derive its sensitivity of the output current to the power-supply voltage under the assumption of negligible base currents.

(10 Marks)

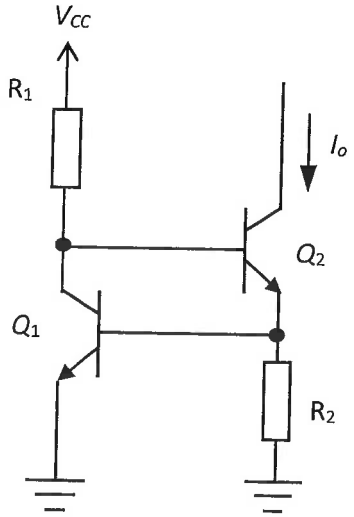

Figure 3

(c) Propose an idea to reduce the sensitivity of the output current to the power-supply voltage of the V_{BE}-based bias circuit.

(5 Marks)

4. The DC open loop gain of an op amp is 100 dB, and the dominant pole is 600 kHz. The op amp is used as an inverting amplifier.

(a) Draw a schematic diagram of the amplifier and find the external resistance values with an input resistance of 10 kΩ and gain of – 9.

(10 marks)

(b) Determine if the amplifier is stable.

(15 marks)

APPENDIX A

$$V_{IH} = \frac{V_{DD} + V_{tp} + k_R(2V_{out} + V_{tn})}{1 + k_R}$$

$$V_{IL} = \frac{2V_{out} + V_{tp} - V_{DD} + k_R V_{tn}}{1 + k_R}$$

$$V_{th} = \frac{V_{th} + \sqrt{\frac{1}{k_R}}(V_{DD} + V_{tp})}{1 + \sqrt{\frac{1}{k_R}}}$$

$$v_t = V_{to} + \gamma\left(\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f}\right)$$

END OF PAPER

EE3019 INTEGRATED ELECTRONICS

Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.