**NANYANG TECHNOLOGICAL UNIVERSITY**
**SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING**
**ACADEMIC YEAR 2022-2023**
**SEMESTER 1**

# EE3013 SEMINCONDUCTOR DEVICES AND PROCESSING

## MOS Devices

1.

(a) For an ideal metal-$SiO_2$-Si diode having $N_A = 10^{17}$ $cm^{-3}$ (p-type semiconductor), calculate the maximum width of the surface depletion region, corresponding to the onset of strong inversion. Assume $kT/q$ = 0.0259 V, and $n_i = 9.65 \times 10^9$ $cm^{-3}$ and permittivity of Si is 11.9x8.85x$10^{-14}$ F/cm.

(b) If the oxide thickness is 5 nm,

(i) determine the capacitance $C_o$ for the diode.

(ii) Also calculate the minimum capacitance for the MOS.

(iii) Determine the difference ($E_i - E_F$) for the semiconductor far away from the interface.

(iv) Estimate the threshold voltage $V_T$ for the MOS structure.

Assume that the relative dielectric constant for the oxide is 3.9.

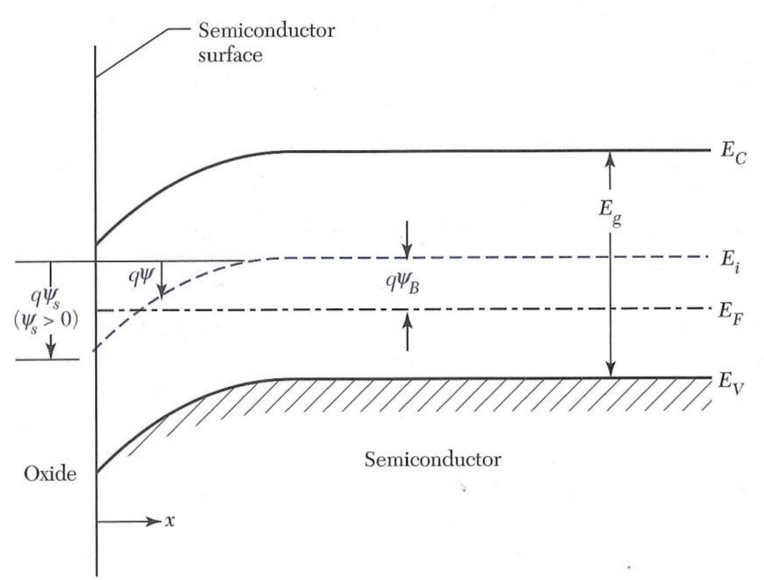
1 (a) For an ideal metal-$SiO_2$-Si diode having $N_A = 10^{17}$ cm$^{-3}$ (p-type semiconductor), **calculate the maximum width of the surface depletion region**, corresponding to the onset of strong inversion. Assume kT/q = 0.0259 V, and $n_i = 9.65 \times 10^9$ cm$^{-3}$ and permittivity of Si is $11.9 \times 8.85 \times 10^{-14}$ F/cm

At the onset of strong inversion

$$\psi_s = 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

The surface depletion layer reaches a maximum $W_m$ at this stage.

$$W_m^2 = \frac{2\varepsilon_s(2\psi_B)}{qN_A} = \frac{4\varepsilon_s kT}{q^2 N_A}\ln\left(\frac{N_A}{n_i}\right)$$



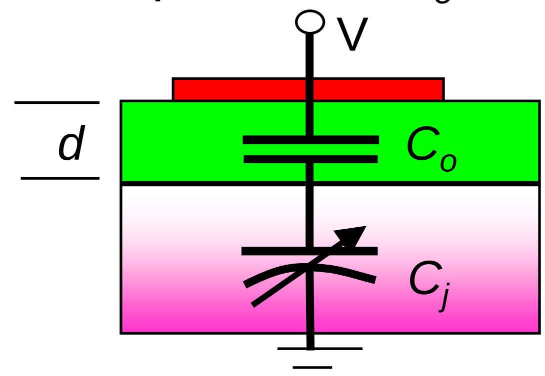

Accordingly,

$\varepsilon_s = 11.9 \times 8.85 \times 10^{-14}$ F/cm  $kT/q = 0.0259$ V

$q = 1.6 \times 10^{-19}$ coul. $N_A = 10^{17}$ cm$^{-3}$ $n_i = 9.65 \times 10^9$ cm$^{-3}$ ➔ $\boxed{W_m = 0.105\ \mu\text{m}}$

1 (b) If the oxide thickness is 5 nm, (i) **determine the capacitance $C_o$** for the diode. (ii) Also calculate the **minimum capacitance** for the MOS. (iii) **Determine the difference ($E_i$ – $E_F$)** for the semiconductor far away from the interface. (iv) **Estimate the threshold voltage $V_T$** for the MOS structure. Assume that the relative dielectric constant for the oxide is 3.9

(i) MOS capacitance $C$ is a series combination of oxide capacitance $C_o$ and depletion layer capacitance, $C_j$:

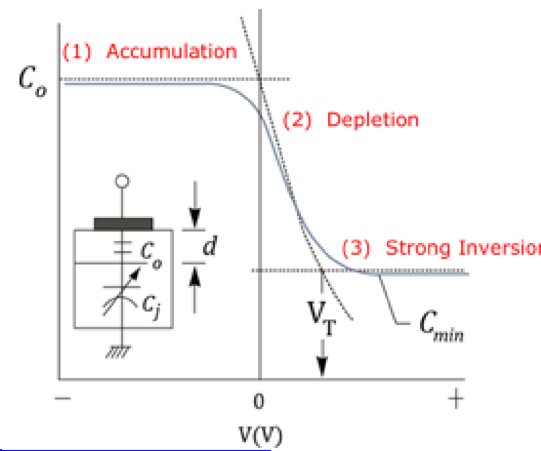



$$C = \frac{C_o C_j}{(C_o + C_j)} \quad \text{F.cm}^{-2}$$

where $C_j = \varepsilon_s/W$, and $C_o = \varepsilon_{ox}/d$

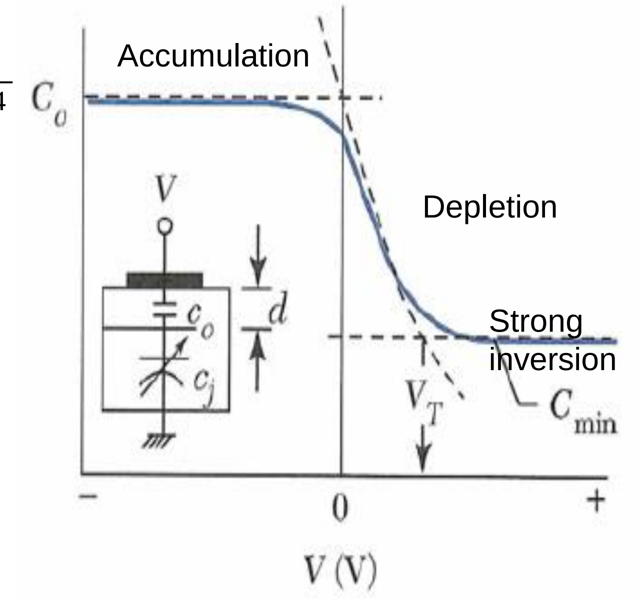
$$C_o = 3.9\times 8.85\times 10^{-14} / 5\times 10^{-7} = \boxed{6.90\times 10^{-7}\ \text{F/cm}^2}$$

Because $C_j$ acts in series with $C_o$, the total MOS capacitance is smaller than $C_o$.



(ii) Minimum capacitance $C_{min}$ occurs at the onset of strong inversion, when $W = W_m$ = 0.105 μm, so that

$$\frac{1}{C_{\min}} = \frac{1}{C_o} + \frac{1}{C_j} = \frac{1}{C_o} + \frac{W_m}{\varepsilon_s} = \frac{1}{6.9\times10^{-7}} + \frac{1.05\times10^{-5}}{11.9\times8.85\times10^{-14}}$$




$$\boxed{C_{min} = 8.76 \times 10^{-8} \text{ F/cm}^2}$$

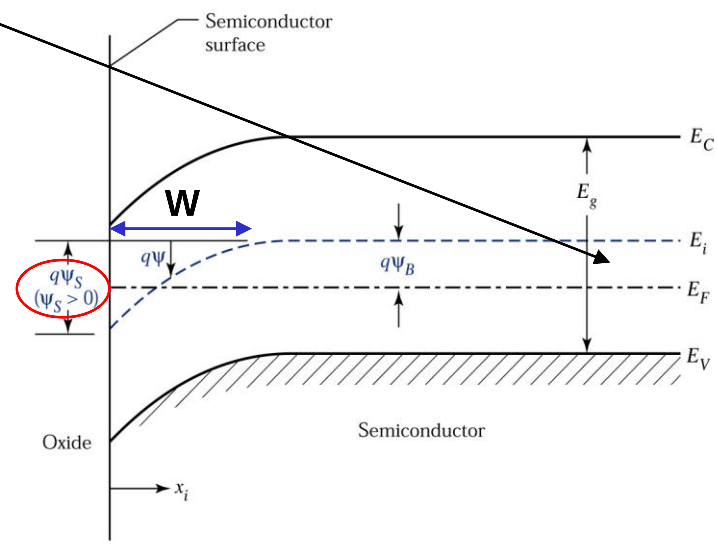
*(iii) Since* $E_i - E_F = q.\ \psi_B$ *far from the interface* and

$$\psi_s = 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

Substituting values,

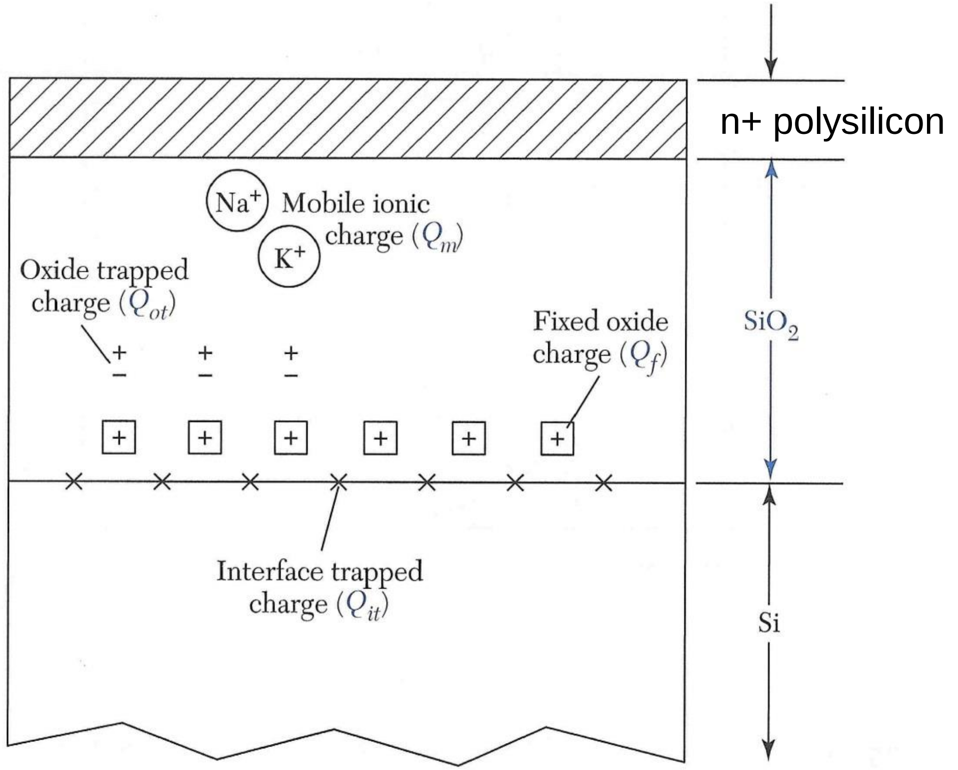
$$\psi_s = 2\psi_B = 2\times0.0259\ln\left(\frac{10^{17}}{9.65\times10^{9}}\right) = 0.84V$$

$\psi_B$ = 0.42 V; $E_i - E_F = q.\ \psi_B$ = 0.42 eV




(iv) $$V_T = \frac{qN_AW_m}{C_o} + 2\psi_B = \frac{1.602\times10^{-19}\times1.05\times10^{-5}}{6.9\times10^{-7}} + 0.84 = 1.08V$$

2. Calculate the flat band voltage for an $n^+$-polysilicon-$SiO_2$-Si diode having $N_A = 10^{17}$ cm$^{-3}$, oxide thickness d = 5 nm. Assume that $\phi_{ms} = -0.98$ V for the ($n^+$ polysilicon) – (p-Si) system, $Q_m$ and $Q_{ot}$ are negligible and $Q_f/q = 5\times10^{11}$cm$^{-2}$.




The flat band voltage is given by $$V_{FB} = \phi_{ms} - \frac{(Q_f + Q_m + Q_{ot})}{C_o}$$

Substituting $\phi_{ms}$ = -0.98 V , $Q_m$ = 0, $Q_{ot}$ = 0,

$$C_0 = \frac{\varepsilon_{ox}}{d}$$

$Q_f = 5 \times 10^{11} \times 1.6\times10^{-19}$ C/ cm$^2$, and $C_o = 6.9\times10^{-7}$ F/cm$^2$ ,

$\boxed{V_{FB} = -0.98 - 0.116 = -1.096 \text{ V.}}$

3. An enhancement type NMOS transistor with $V_T$ = 2 V has its source grounded and a 3 V supply connected to the gate. In what region does the device operate for (a) $v_D$ = 0.5 V? (b) $v_D$ = 1.0 V? (c) $v_D$ = 5.0 V? If the device parameters are $\mu_n C_{ox}$ = 20 μA/V$^2$, Z = 100 μm and L = 10 μm, **calculate the drain current** for each of the cases.

For enhancement NMOS transistor, $V_T$ is positive = 2 V

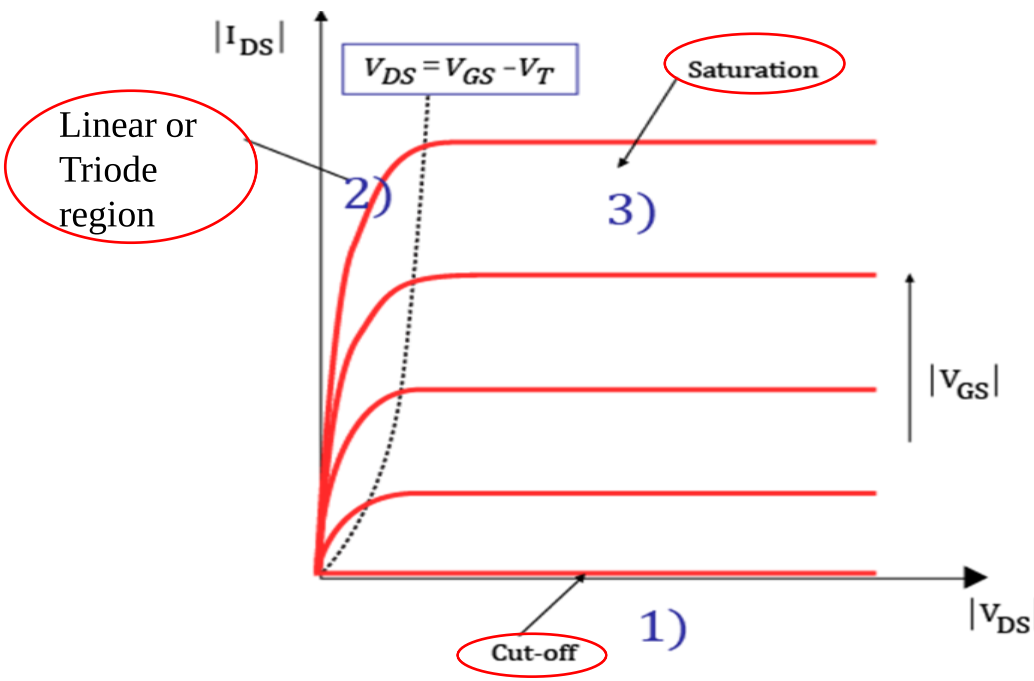
➔ If, $V_{GS} \geq 2$ V then transistor is ON.

* If $V_{DS} < (V_{GS} - 2)$ then the transistor is said to be in the triode region and equation (1) is valid:

$$I_D = K_n\left[(V_{GS} - V_T)V_{DS} - V_{DS}^2 / 2\right] \text{ ----- (1)}$$

* If $V_{DS} \geq (V_{GS} - 2)$ then the transistor is said to be in the saturation region and equation (2) is valid:

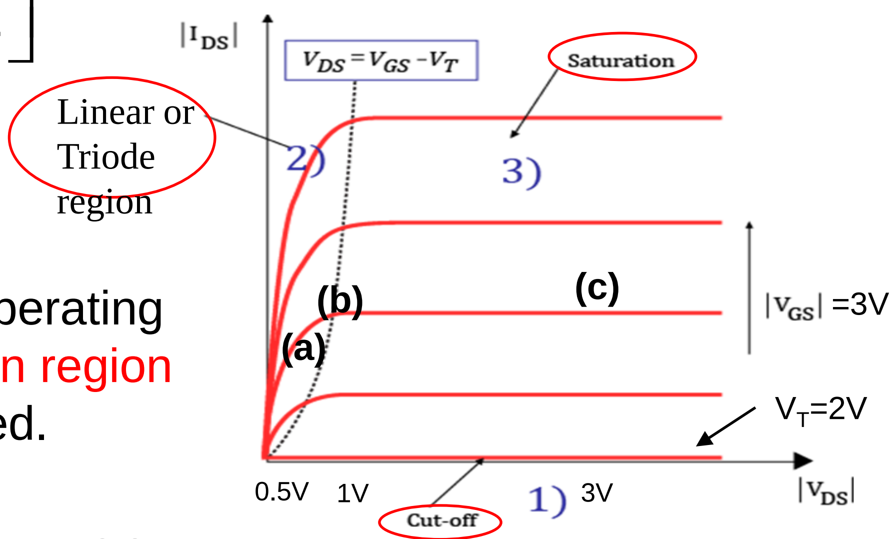
$$I_{DS} = \frac{K_n}{2}(V_{GS} - V_T)^2 \text{ ----- (2)}$$



$$K_n = \mu_n Cox\,(Z/L) = (200)(100/10) = 200$$

(a) With source common, $V_{DS}$ = 0.5 V; $V_{GS}$ = 3 V; $V_{GS} - V_T$ = 1 V. ( Triode region ) ➔ Equation (1) is valid.

$$I_D = K_n\left[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2\right]$$
$$= 200[(3-2)0.5-(0.5)^2/2]$$
$$= 75\mu A$$




*(b)* $V_{DS}$ = 1.0 V; $V_{GS}$ = 3 V; $V_{GS} - V_T$ = 1 V. Operating point is at the knee of triode and saturation region
➔ Equation (1) or Equation (2) can be used.

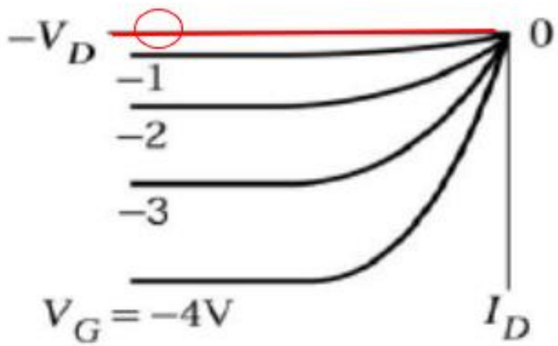
$$I_{DS} = \frac{K_n}{2}(V_{GS} - V_T)^2 = 100(3-2)^2 = 100\mu A$$

*(c)* $V_{DS}$ = 5.0 V; $V_{GS}$ = 3 V; $V_{GS} - V_T$ = 1 V. Operating point is in the saturation region
➔ Equation (2) should be used.

$$I_{DS} = \frac{K_n}{2}(V_{GS} - V_T)^2 = 100\ \mu A$$

4 An enhancement PMOS transistor has $K_p$ = 80 $\mu$A/$V^2$ and $V_T$ = -1.5 V. The gate is connected to -3.5 V and the source to ground. Find the drain current for (a) $V_D$ = -1 V, (b) $V_D$ = -2 V and (c) $V_D$ = -5 V.

For the enhancement mode PMOS transistor, a simple way to deal with PMOS is to use the same formulae but all the parameters involved use magnitude (ignore negative sign).




$V_T$ is negative = -1.5 V, $V_{GS}$ = -3.5 V ➔ $|V_{GS}|-|V_T|$ = 3.5-1.5=2V

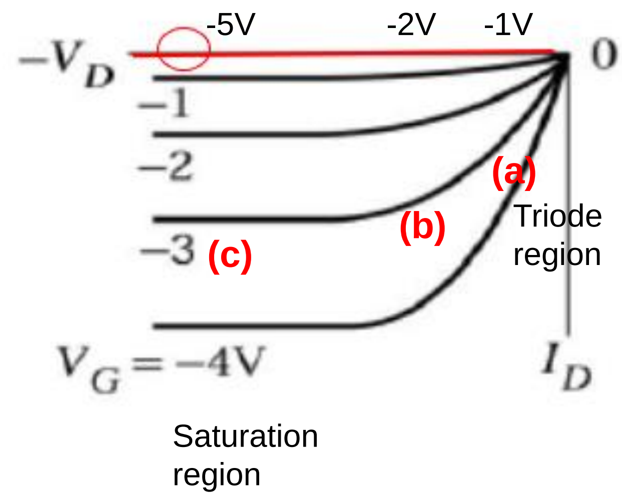
* If $|V_{DS}| < (|V_{GS}|-|V_T|)$, then the transistor is said to be in the triode region and equation (1) is valid.

$$I_D = K_n\left[(|V_{GS}|-|V_T|)|V_{DS}|-|V_{DS}|^2/2\right] \qquad \text{----- (1)}$$

* If $|V_{DS}| > (|V_{GS}|-|V_T|)$, then the transistor is said to be in the saturation region and equation (2) is valid.

$$I_{DS} = \frac{K_p}{2}(|V_{GS}|-|V_T|)^2 \qquad \text{----- (2)}$$

4 *(a)* $V_{DS}$ = -1 V




$|V_{DS}|$ (1V)<$|V_{GS}|$-$|V_T|$ (2V). Hence, the PMOS operates in triode region.

$$I_D = K_n\left[(|V_{GS}| - |V_T|)|V_{DS}| - |V_{DS}|^2/2\right]$$

$$= 80[(3.5 - 1.5)\times 1 - 1^2/2] = 120\mu A$$

*(b)* $V_{DS}$ = -2 V

$|V_{DS}|$ (2V)=$|V_{GS}|$-$|V_T|$ (2V).

Operating point is at the knee of triode and saturation regions. Equation (1) or Equation (2) can be used.

$$I_{DS} = \frac{K_p}{2}(|V_{GS}| - |V_T|)^2$$

$$= 40(3.5 - 1.5)^2 = 160\mu A$$

$$I_D = K_n\left[(|V_{GS}| - |V_T|)|V_{DS}| - |V_{DS}|^2/2\right]$$

$$= 80[(3.5 - 1.5)\times 2 - 2^2/2] = 160\mu A$$

(c) $V_{DS}$ = -5 V

$|V_{DS}|$ (5V)>$|V_{GS}|$-$|V_T|$ (2V). Operating point is in the saturation region. Equation (2) should be used.

$$I_{DS} = \frac{K_p}{2}(|V_{GS}| - |V_T|)^2$$

$$= 40(3.5 - 1.5)^2 = 160\mu A$$

**Q5**: For an ideal MOS diode fabricated on a n-Si substrate:

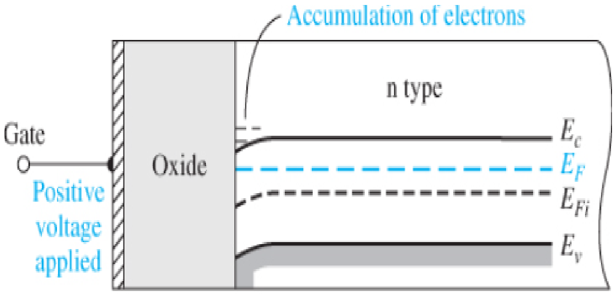
(i) Sketch the energy band diagrams when it is in (i) accumulation, (ii) depletion, and (iii) inversion. Indicate $E_c$, $E_v$, $E_i$ and $E_f$ in the diagrams.

(ii) Sketch the high-frequency capacitance versus voltage diagram and indicate the regions corresponding to (i) accumulation, (ii) depletion, and (iii) inversion.

## Solution:

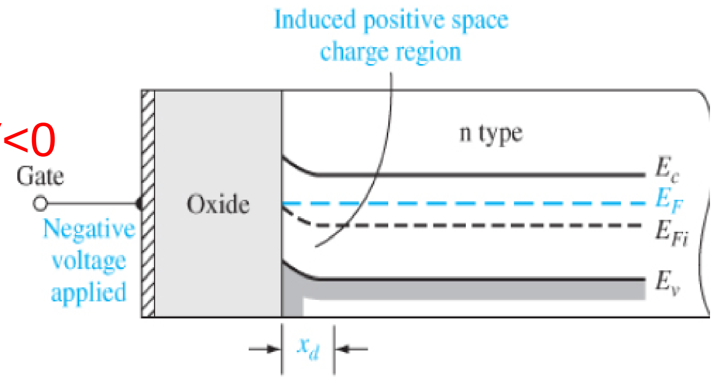
(i)

V>0



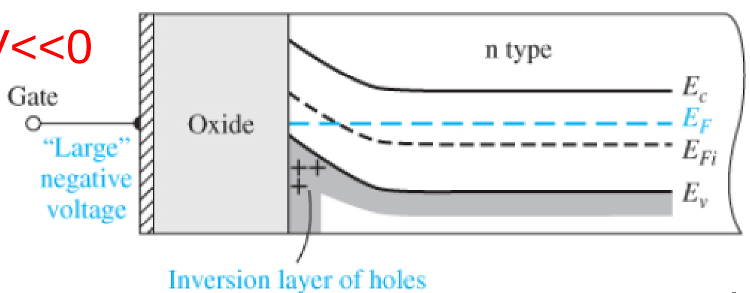

Accumulation

V<0




Depletion

V<<0




Inversion

(ii) High-frequency C-V Plot