NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2019-2020

EE3019 – INTEGRATED ELECTRONICS

November / December 2019 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 4 pages.
2. Answer all 4 questions.
3. All questions carry equal Marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.

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1. The parameters of the pMOS and nMOS transistors are given below:

pMOS $V_{tp} = -0.6$ V $\mu_p C_{ox} = 100$ μA/V² $(W/L)_p = 5$

nMOS $V_{tn} = 0.6$ V $\mu_n C_{ox} = 250$ μA/V² $(W/L)_n = 2$

(a) When a 2-input NAND (NAND2) is designed using the given device parameters, determine the switching threshold of the 2-input NAND gate. Use equivalent device sizes when calculating. Assume that the supply voltage is 1.5 V.

(5 Marks)

(b) Determine the propagation delays (τ_{PHL} and τ_{PLH}) when the 2-input NAND gate designed in part(a) drives 1pF. Assume that all the input signals switch at the same time with zero rise and fall times.

(10 Marks)

(c) Explain how to make τ_{PHL} and τ_{PLH} of the above 2-input NAND gate in part(b) identical.

(5 Marks)

Note: Question No. 1 continues on page 2.

(d) When a transmission gate is designed using the given device parameters, calculate the on-resistance of the transmission gate when the output is at 0 V and 1.5 V. Assume that the input signal is 1.5 V and the supply voltage is 1.5 V.

(5 Marks)

2. (a) A CMOS logic circuit is shown in Figure 1. Determine the equivalent width of the pull-down network using both best and worst case scenarios. Assume that the width of the nMOS transistors is W. Explain how to increase the switching threshold of the logic circuit.

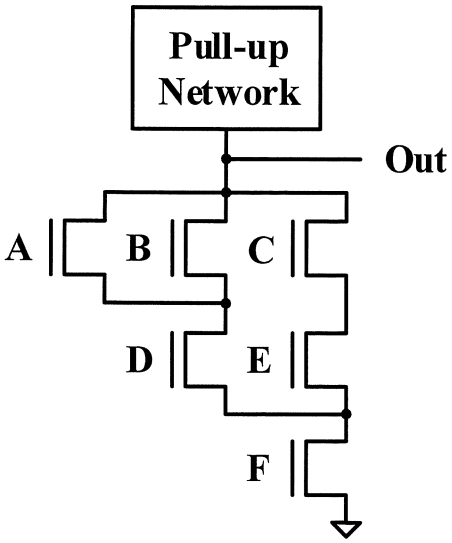

Figure 1

(5 Marks)

(b) A DRAM cell is shown in Figure 2. Calculate the voltage swing at the bit line when the voltage stored in the cell capacitor (30 fF) is 0 V and 5 V. Each DRAM cell has the parasitic capacitance of 10 fF on the bit line, and the number of DRAM cells on the bit line is 512. Assume that the bit line is pre-charged to 2.5 V.

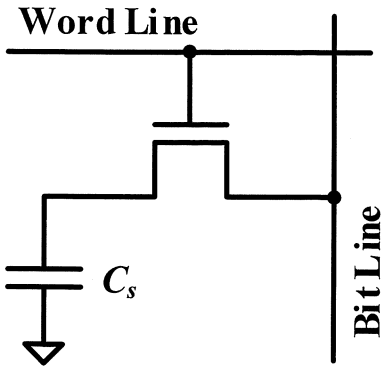

Figure 2

(5 Marks)

Note: Question No. 2 continues on page 3.

(c) A negative-feedback amplifier is shown in Figure 3. Assume that A = 1000, R_1 = 1 kΩ, R_2 = 2 kΩ, R_3 = 3 kΩ, and R_L = 4 kΩ.

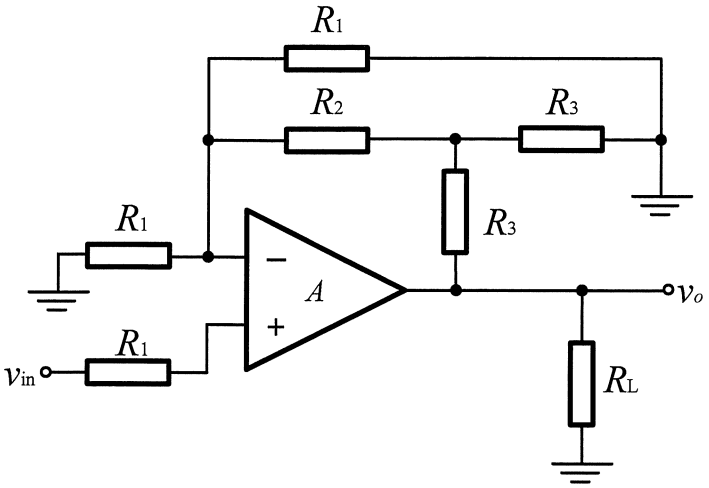

Figure 3

(i) Calculate the feedback factor β.

(5 Marks)

(ii) Derive the closed-loop gain (A_f) equation.

(5 Marks)

(iii) When A decreases by 30%, determine the corresponding decrease in A_f in percentage (%).

(5 Marks)

3. Figure 4 on page 4 shows the voltage-reference circuits. The dynamic small-signal resistance of each Zener diode r_z = 100 Ω.

(a) Find the DC output voltage of each circuit.

(8 Marks)

(b) Draw the small-signal equivalent circuit and derive an expression for the output impedance Z_o of each circuit.

(10 Marks)

(c) Comment on the advantages and disadvantages of the voltage-reference circuits.

(7 Marks)

Note: Question No. 3 continues on page 4.

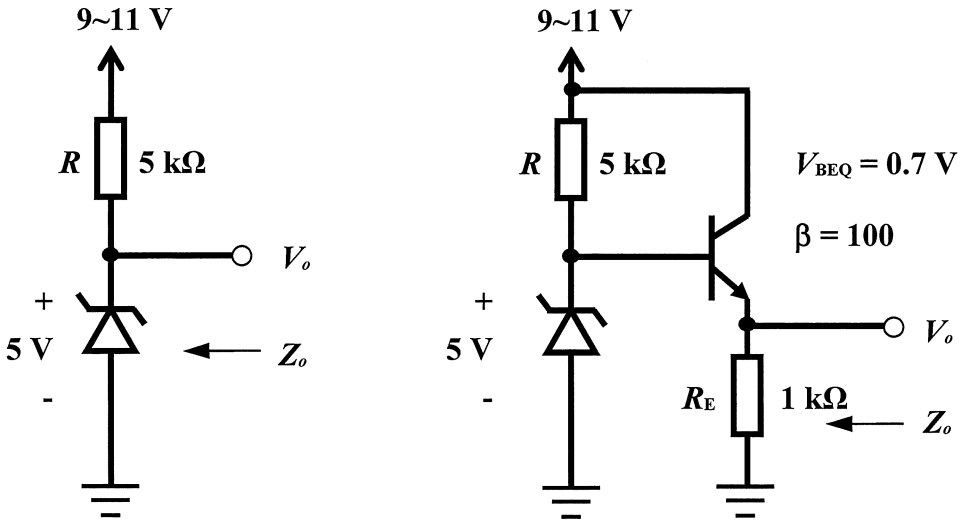

Figure 4

4. Given three MOSFETs with channel lengths of 10 μm, channel widths of 100 μm, threshold voltage of 1 V, early voltage of 100 V and $\mu_n C_{ox}$ = 20 μA/V², it is required to design the circuit for a Wilson MOSFET constant current source to obtain an output of 100 μA with a power supply V_{DD} = 10 V.

   (a) Draw the schematic of the Wilson MOSFET constant current source.

   (5 Marks)

   (b) What is the lowest possible value of the output voltage?

   (10 Marks)

   (c) Find the change in output current resulting from a 3-V change in the output voltage.

   (10 Marks)

END OF PAPER

EE3019 INTEGRATED ELECTRONICS

Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.