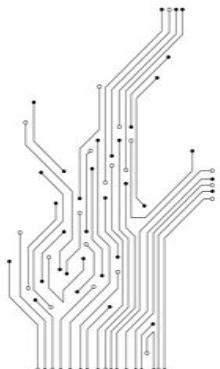


EE3019 – Integrated Electronics CMOS Logic Circuits

Learning Objectives

By the end of this lesson, you should be able to:

- Explain the Complimentary Metal Oxide Semiconductor (CMOS) process.
- Discuss the three different operating regions of Metal Oxide Semiconductor Field Effect Transistor (MOSFET).
- Describe the Voltage Transfer Characteristics (VTC) of a CMOS inverter.
- Explain the five different operating regions in the VTC of a CMOS inverter and noise margins.
- Describe circuit delay and dynamic power dissipation.
- Explain CMOS ring oscillator.
- Explain the effect of transistor sizing to ensure proper functioning.
- Explain the operation of CMOS Transmission Gate (TG) .



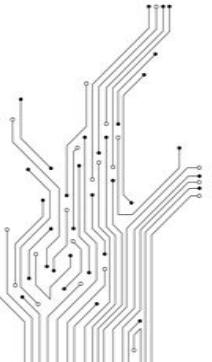
Integrated Circuit Components

An integrated circuit is a small piece of silicon (known as silicon chip) that contains millions of components.

In 1947 (23rd December) the first successful experiment was conducted.

Announcement - Invented in 1948

Components that are commonly used in Integrated Circuits are:



Analog IC

Transistors, resistors and capacitors



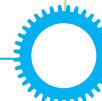
Radio Frequency (RF) IC

Transistors, resistors, capacitors and inductors

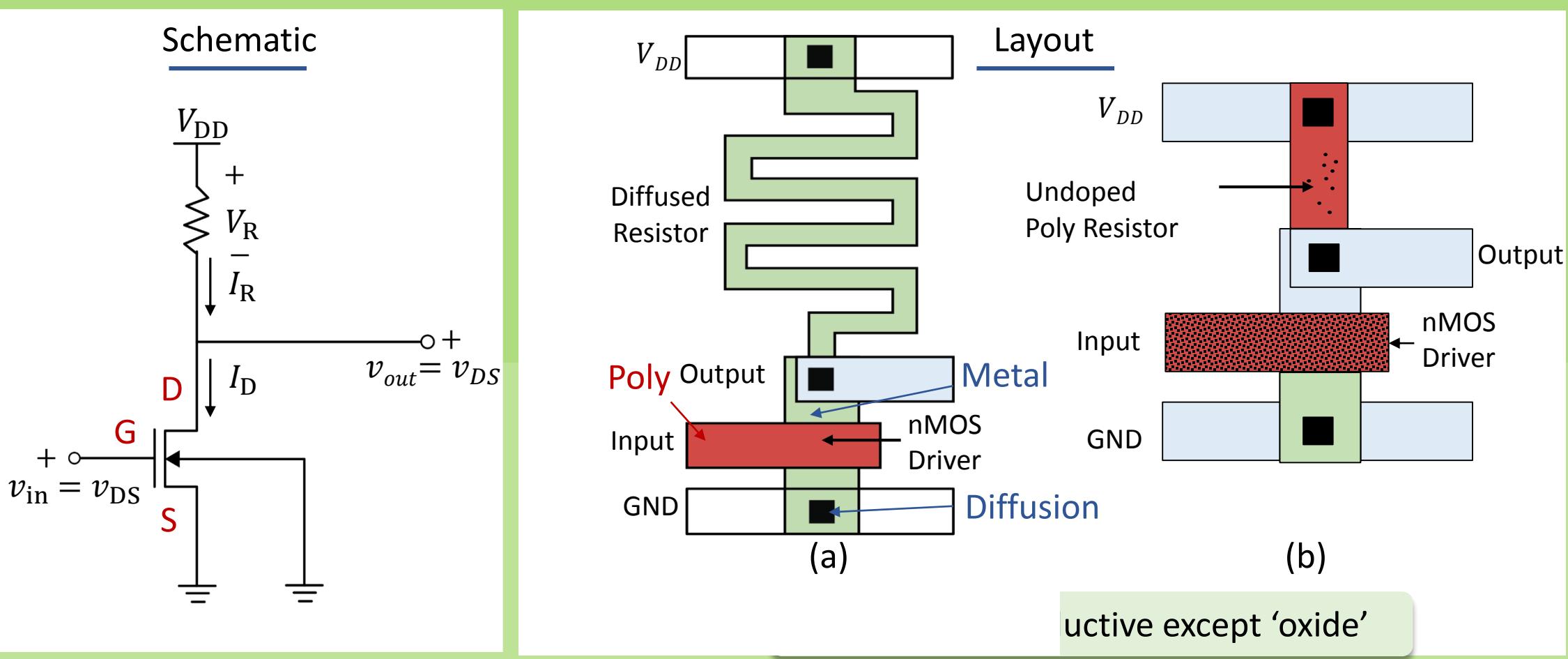
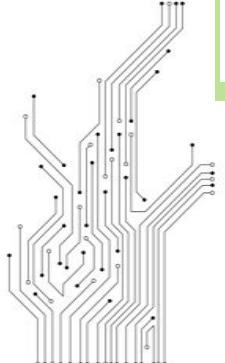


Digital IC

Mainly transistors

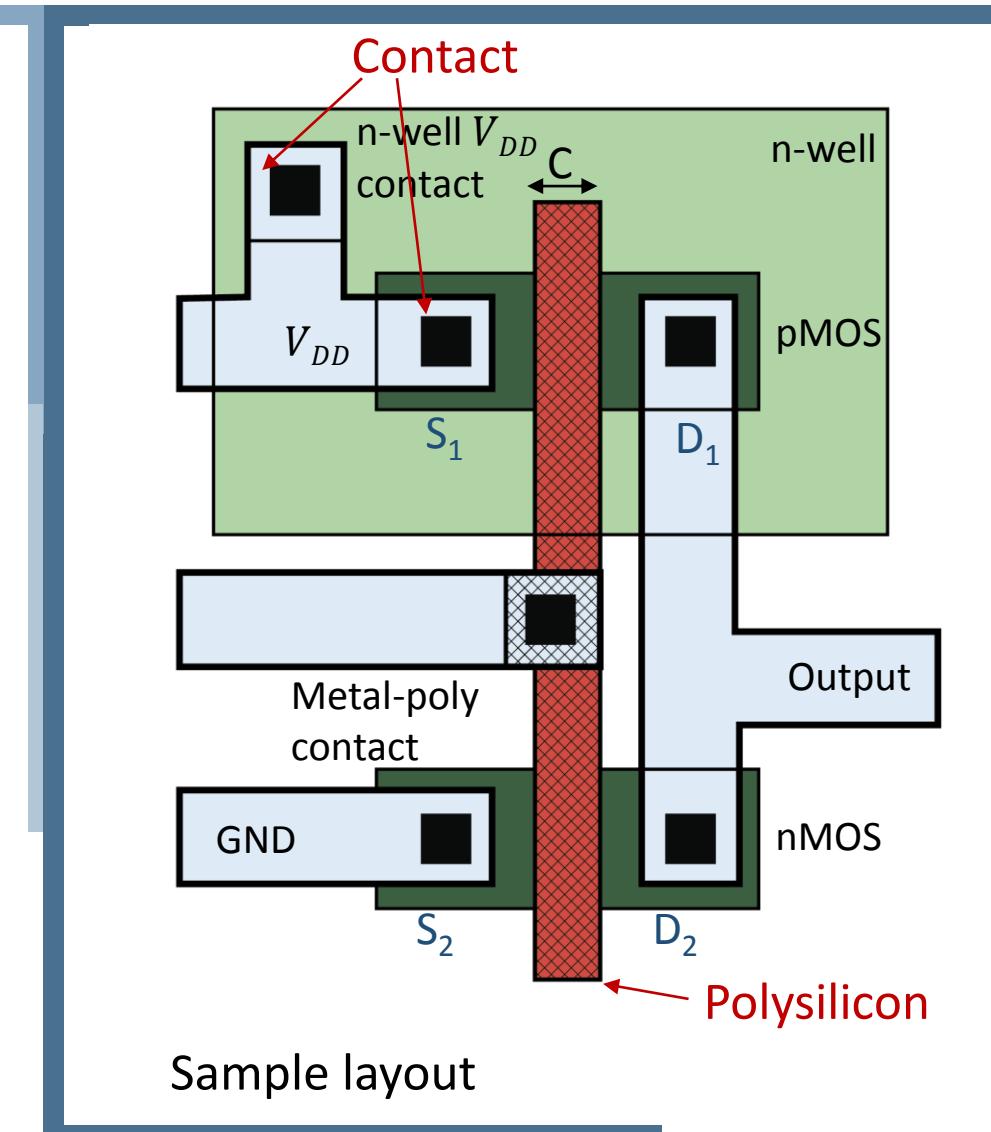
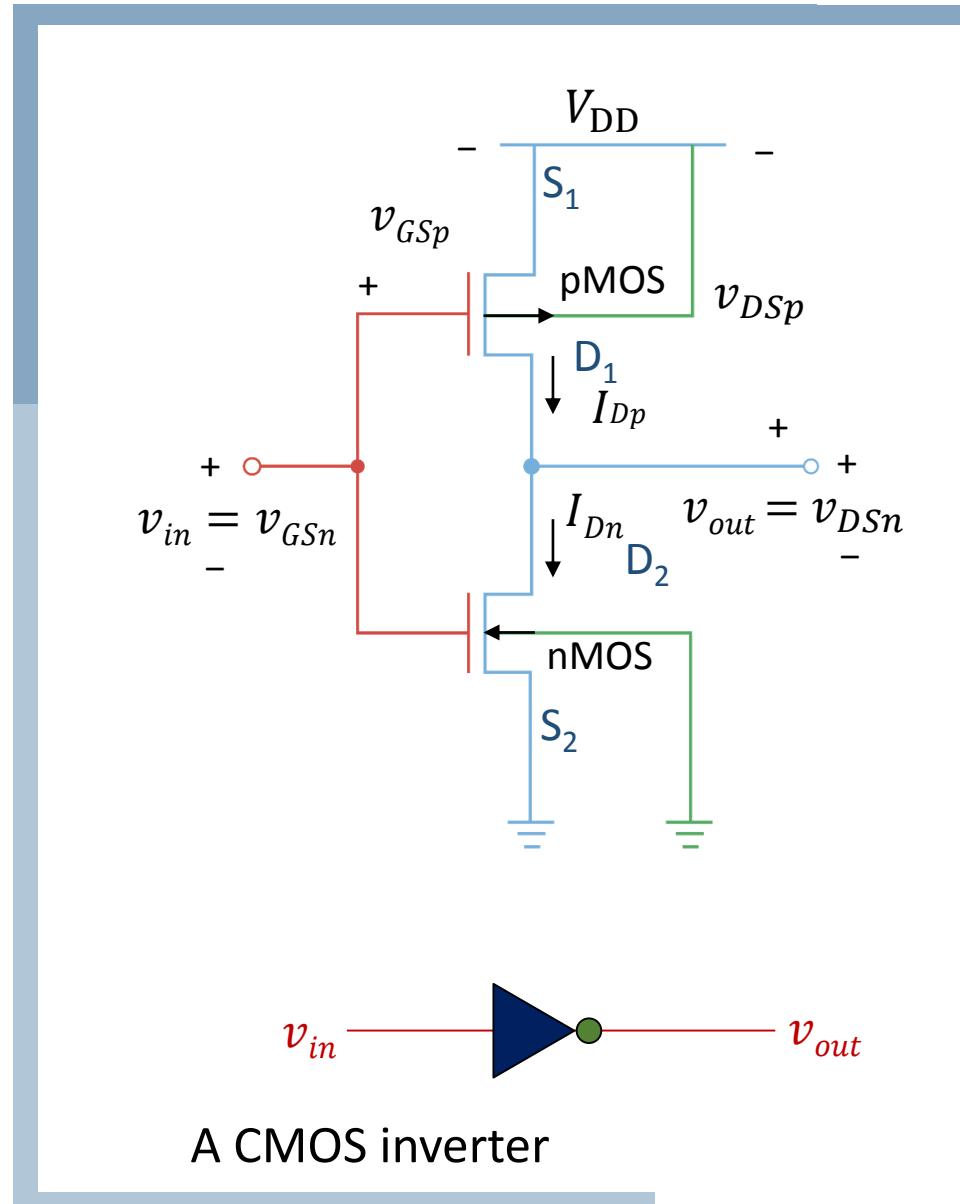
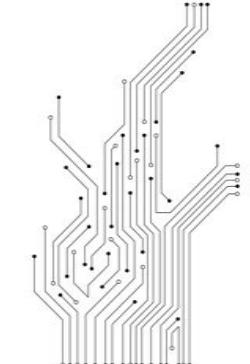


Integrated Circuit Components

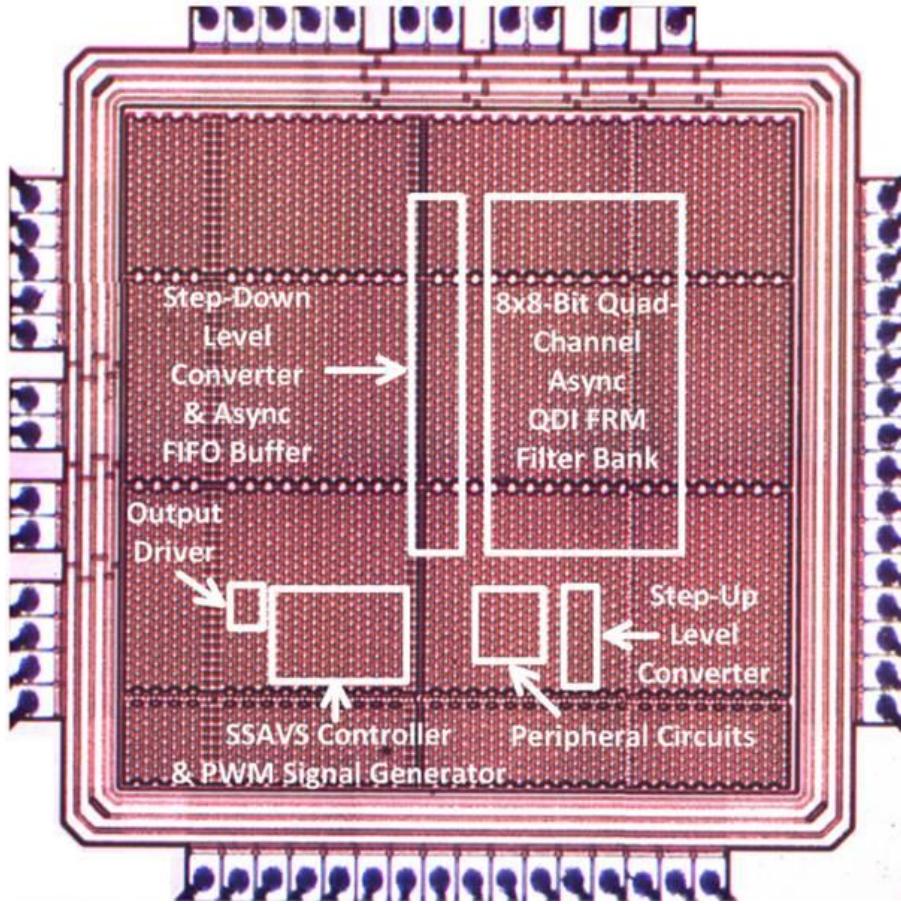


Sample layout of resistive-load inverter circuits with:
(a) diffused resistor and
(b) undoped polysilicon resistor.

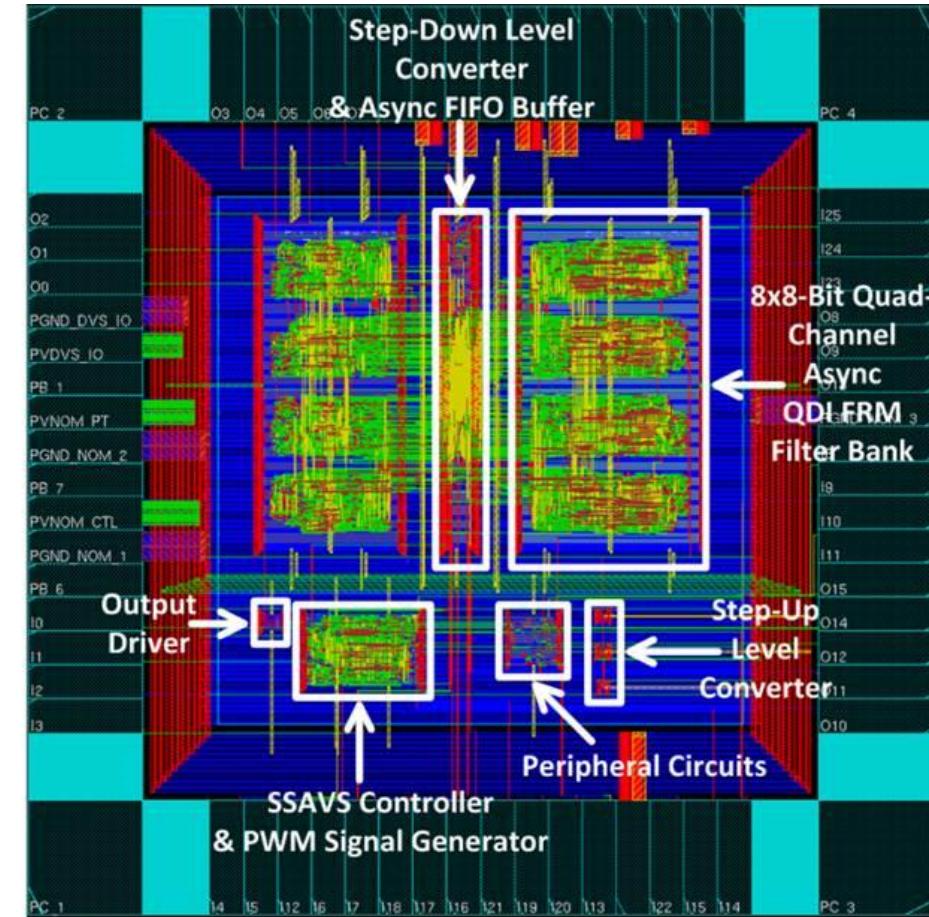
Integrated Circuit Components



Intel Pentium Microprocessor

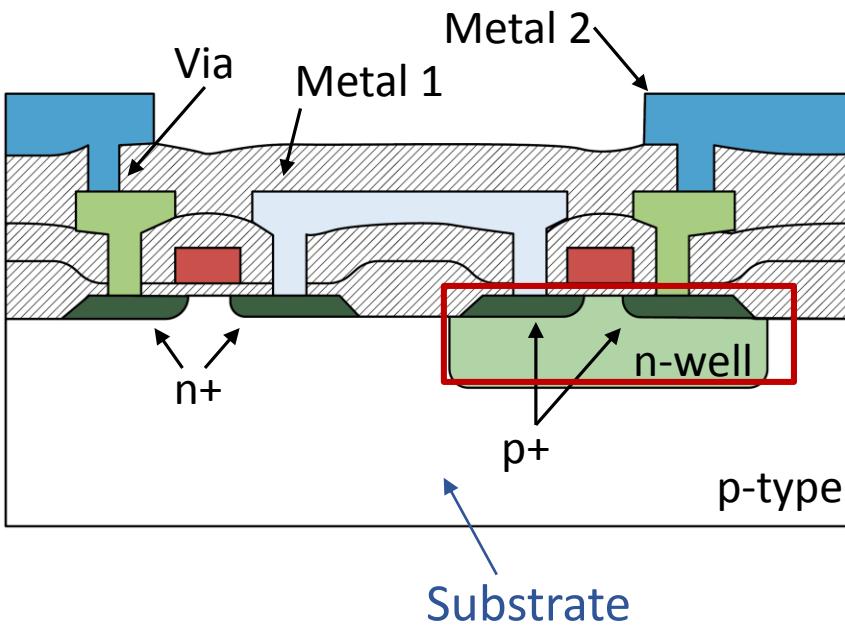


Async Adaptive V_{DD} System embodying Async Filter Bank



Area $\sim 0.18 \text{ mm}^2$

CMOS Process



CMOS Process – PMOS + NMOS (Low power as only 1 transistor is conducted at all time.)

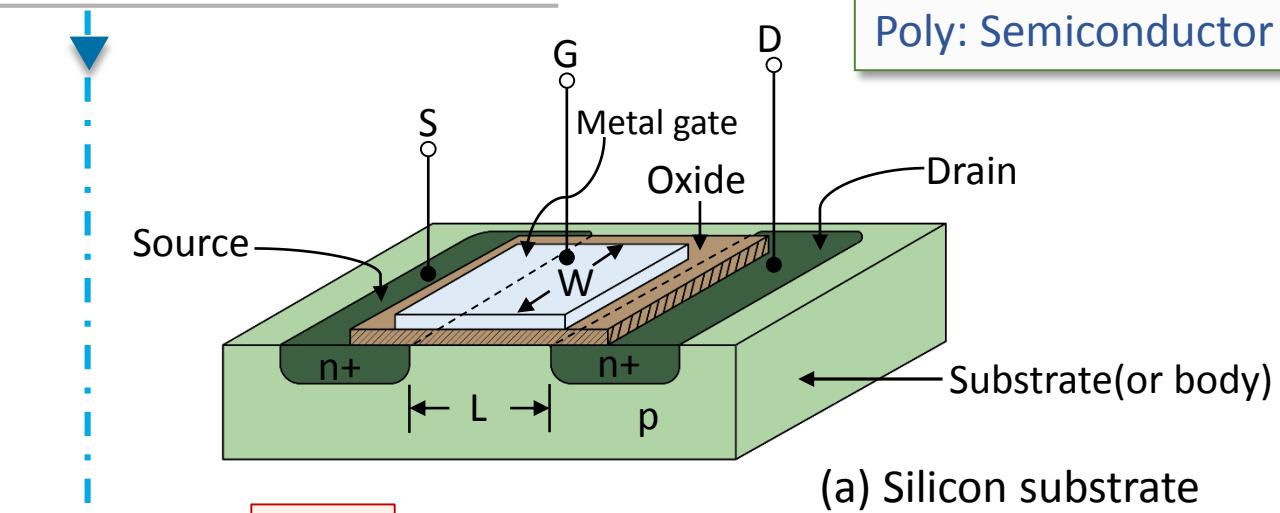
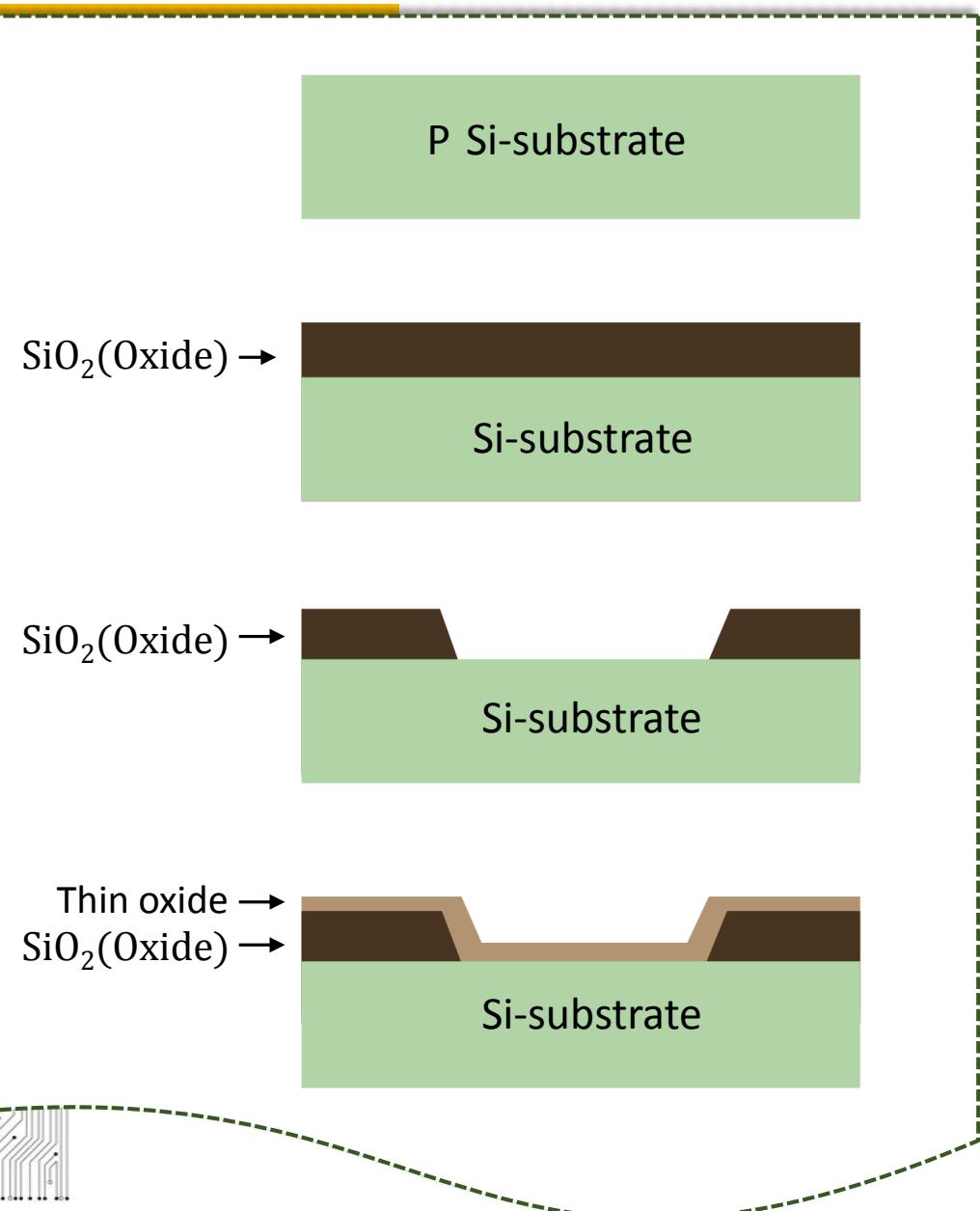
a

The CMOS process allows fabrication of nMOS and pMOS transistors side-by-side on the same Silicon substrate.

Contd.

Fabrication of an nMOS Transistor

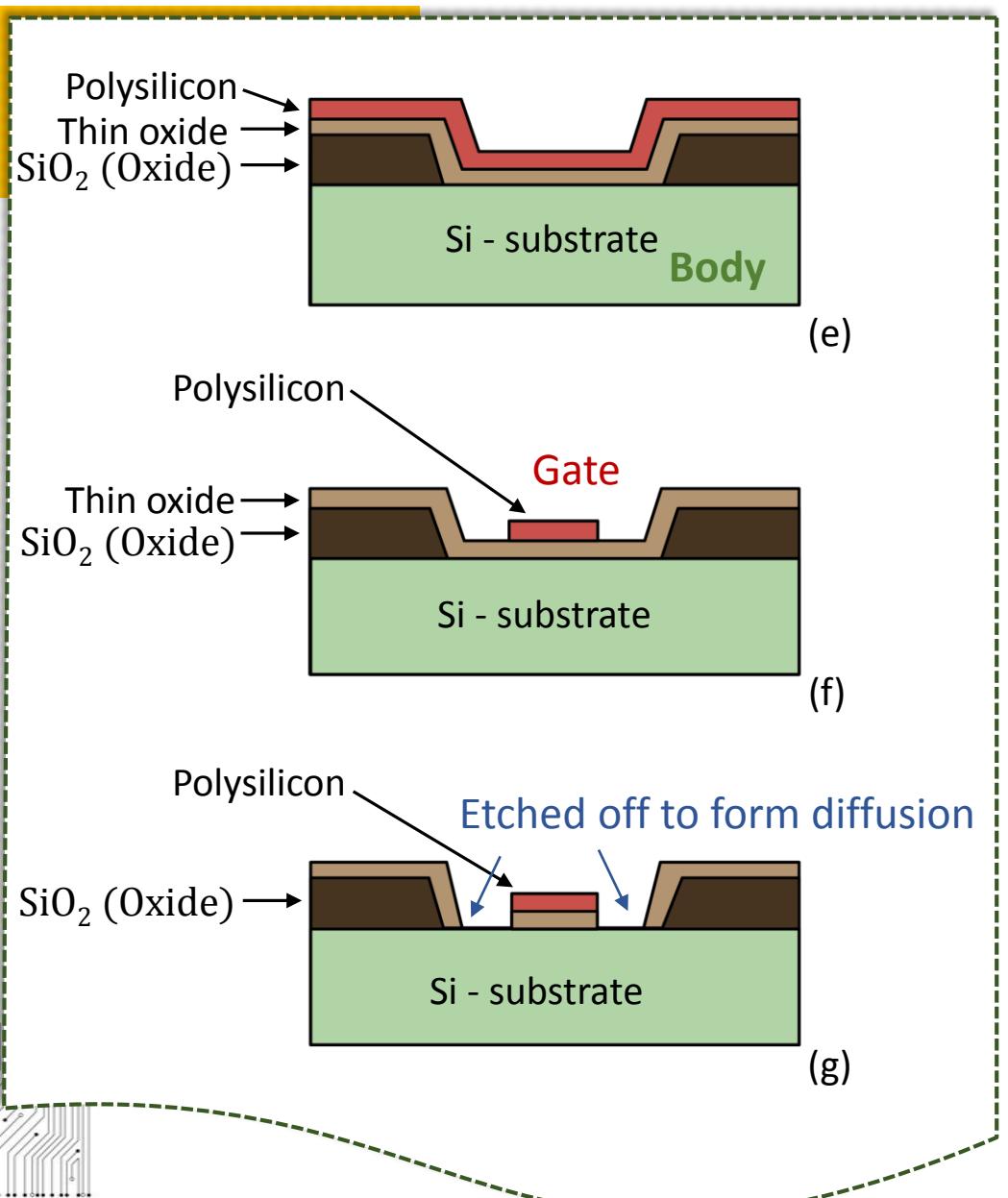
Oxide: Insulator
Metal: Conductor
Poly: Semiconductor



(a) Silicon substrate

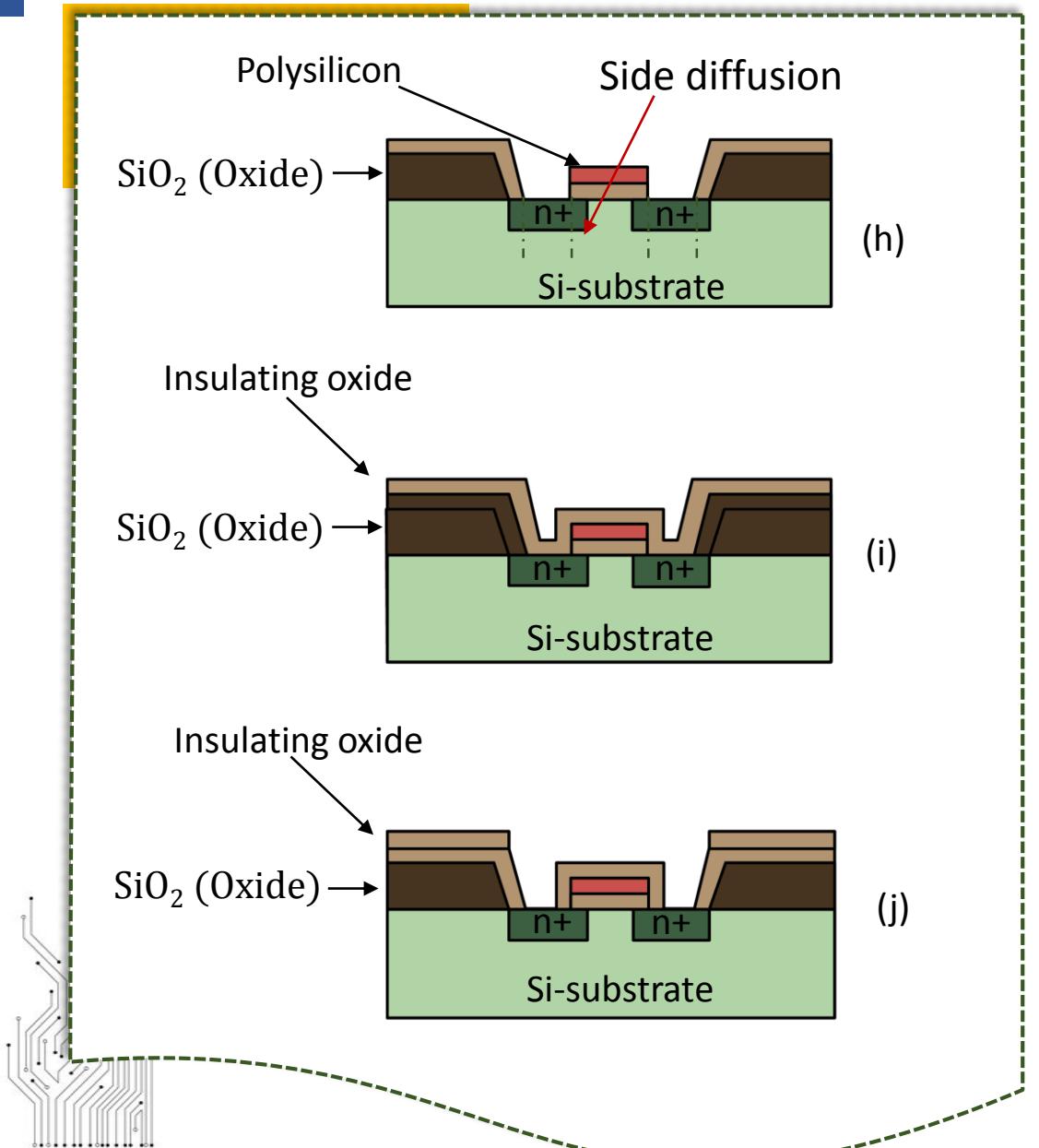
- b** Thick
Field oxide is created on surface of MOS transistor.
- c** Field oxide is etched to expose silicon surface on which the MOS transistor will be created.
- d** A thin, high quality oxide layer is formed. This is the gate oxide of the MOS transistor (the unit capacitance is C_{ox}).
- Contd.

Fabrication of an nMOS Transistor



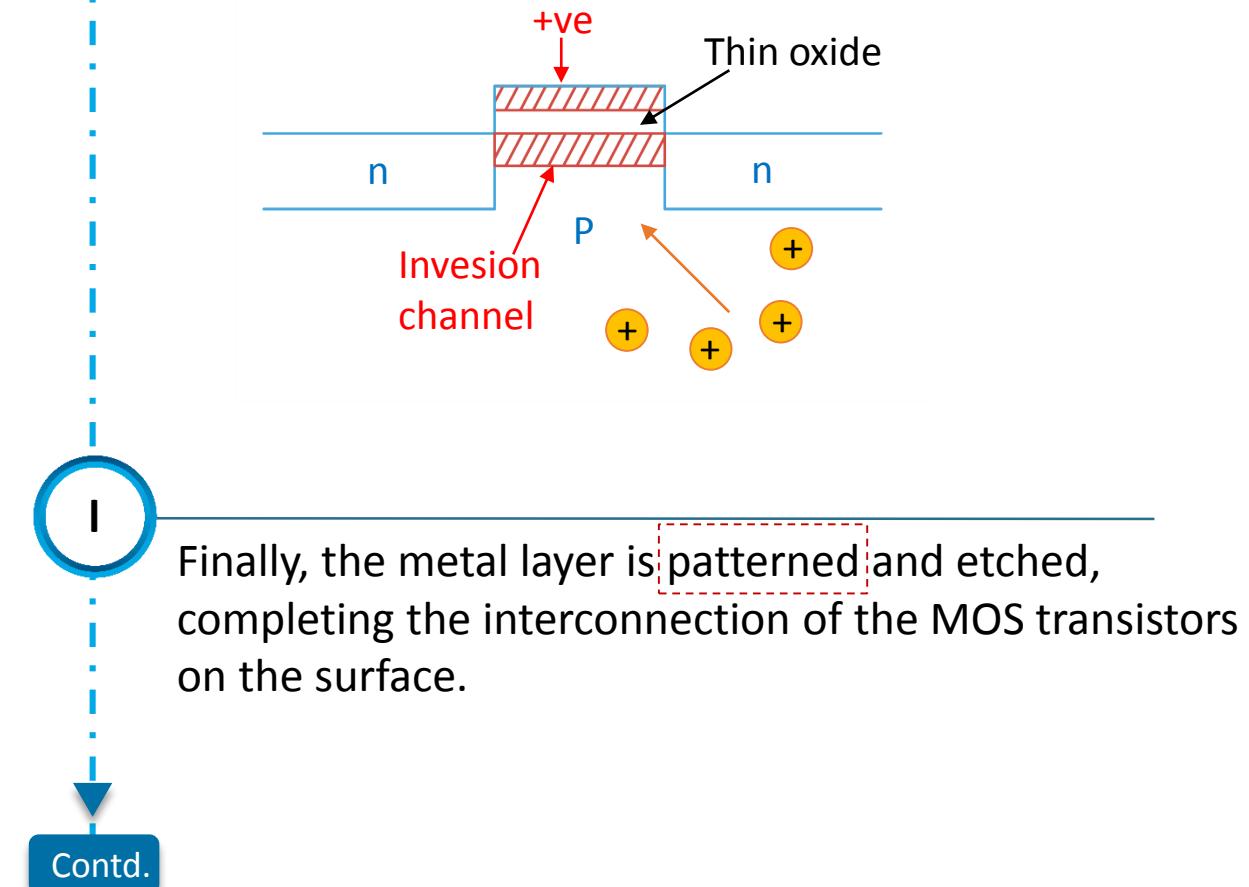
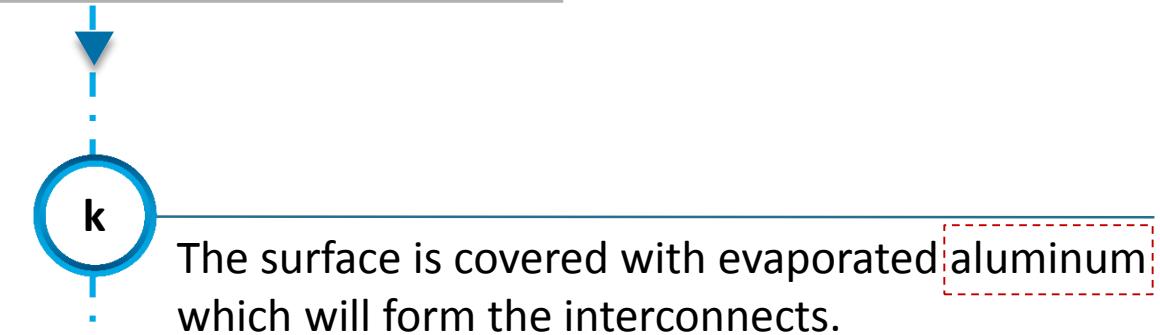
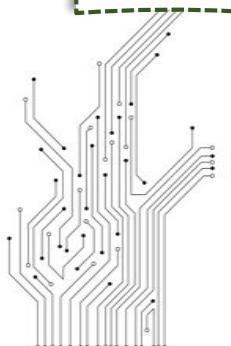
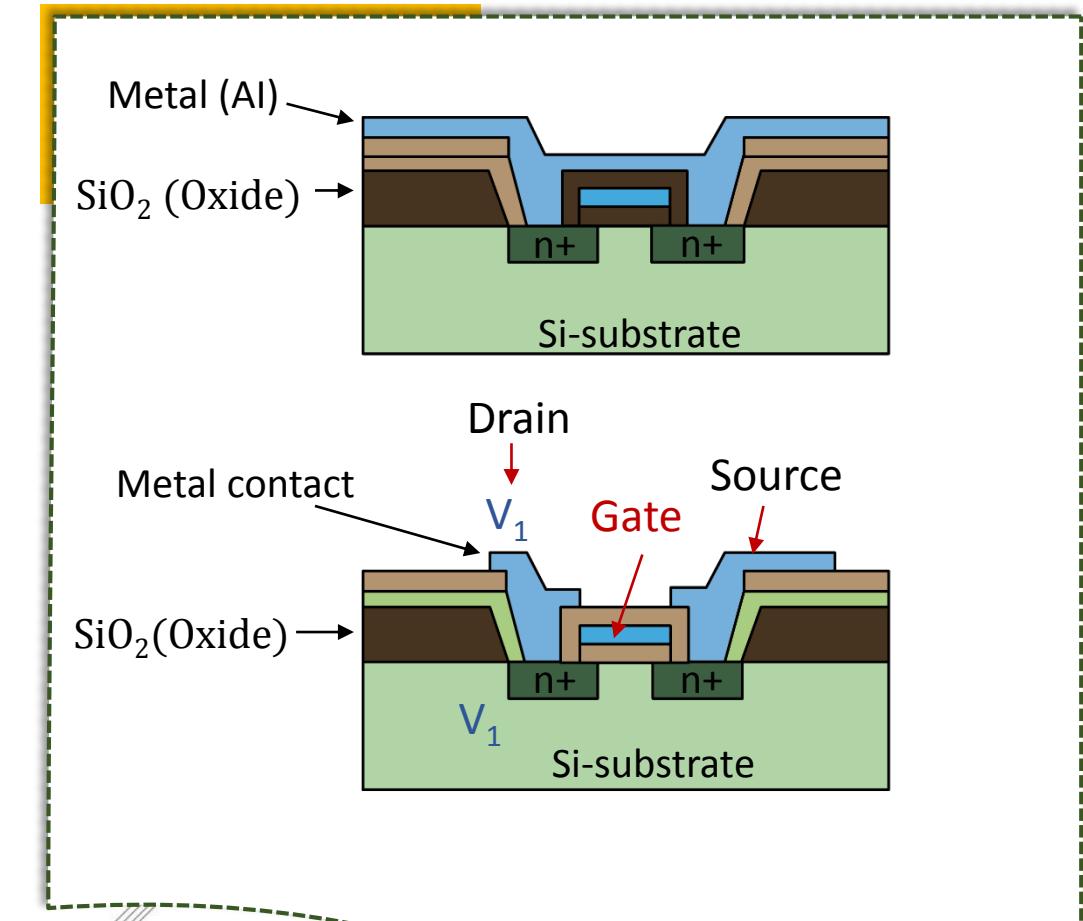
- e A layer of polysilicon is deposited. Polysilicon is used as the gate electrode material for MOS transistor and also as interconnect medium in IC.
- f After deposition, the polysilicon is patterned and etched to form the interconnects and the MOS transistor gates.
- g The thin gate oxide not covered by polysilicon is etched away, which exposes the bare silicon surface on which the source and drain junctions are to be formed.
- Contd.

Fabrication of an nMOS Transistor



- Parasitic
- h**: The entire silicon surface is then doped with a high concentration of impurities, either through diffusion or ion implantation. The two n-type regions (source and drain junctions) are created in the p-type substrate.
 - i**: The entire surface is again covered with an insulating layer of silicon dioxide.
 - j**: The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions.
- Contd.

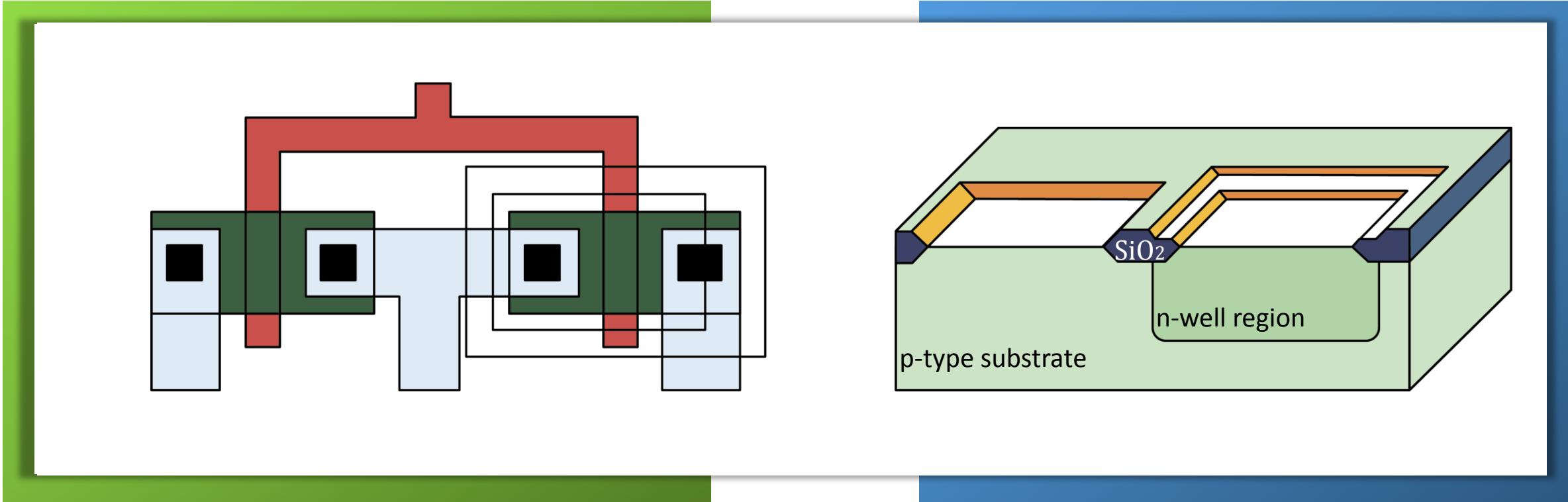
Fabrication of an nMOS Transistor



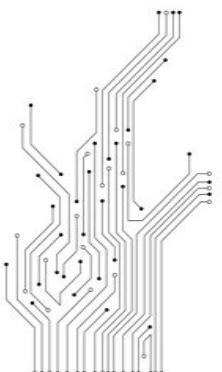
Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface.

Contd.

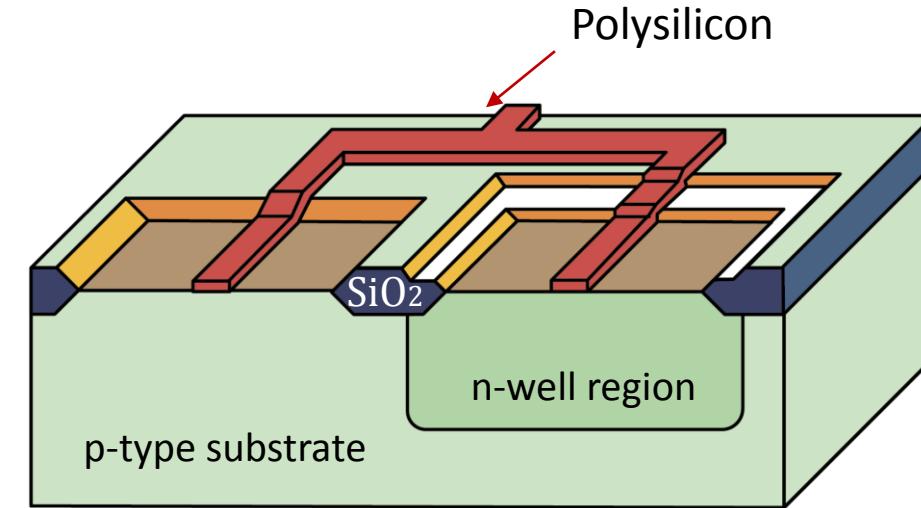
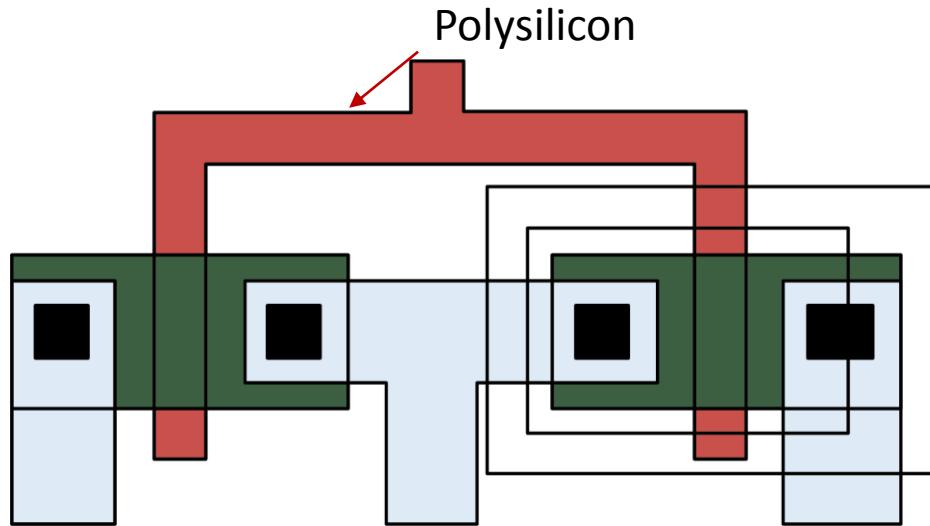
Fabrication of a CMOS Inverter



Following the creation of the n-well region, a thick field oxide is grown in the areas surrounding the transistor's active regions, and a thin gate oxide is grown on top of the active regions. The thickness and the quality if the gate oxide are two of the most critical fabrication parameters, since they strongly affect the operational characteristics of the MOS transistor, as well as its long-term reliability. (After Atlas of IC Technologies, by W. Maly.)

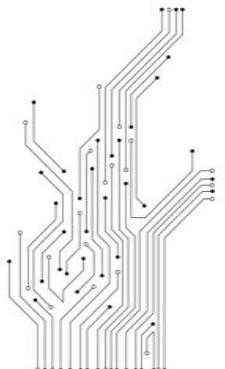


Fabrication of a CMOS Inverter

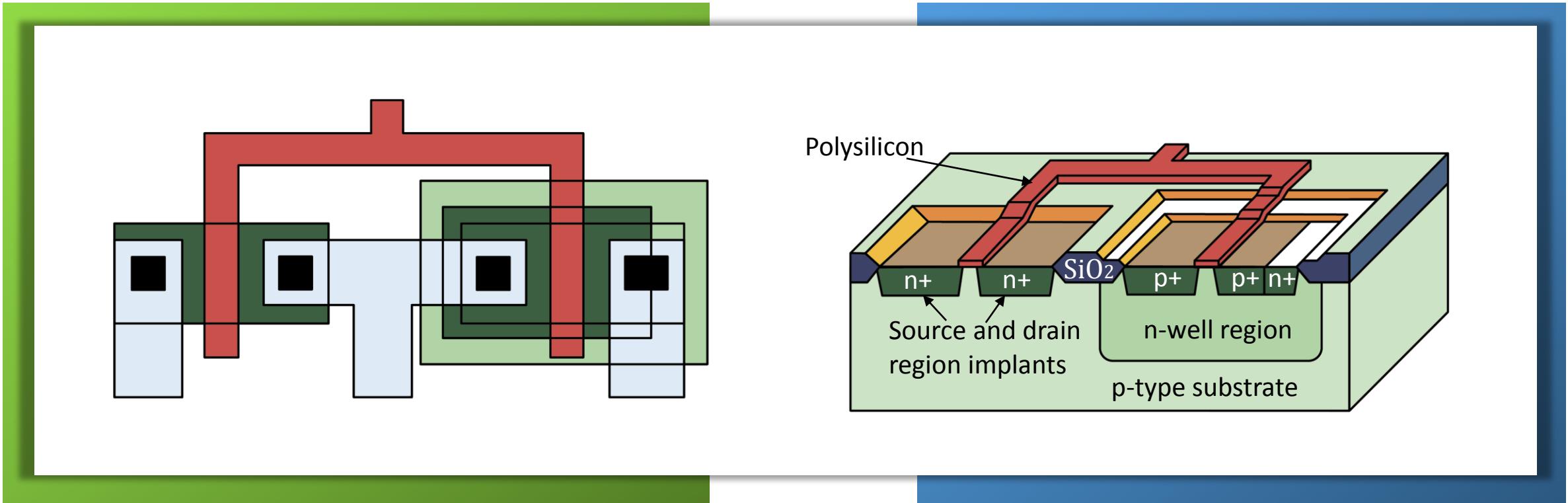


The polysilicon layer is deposited using chemical vapour deposition (CVD) and patterned by dry (plasma) etching. The created polysilicon lines will function as the gate electrodes of the nMOS and the pMOS transistors and their interconnects. Also, the polysilicon gates act as self-aligned masks for the source and drain implantations that follow this step.

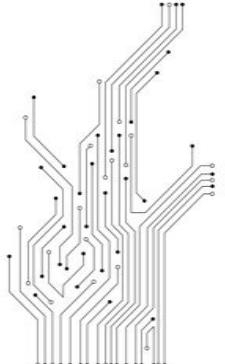
(After Atlas of IC Technologies, by W. Maly.)



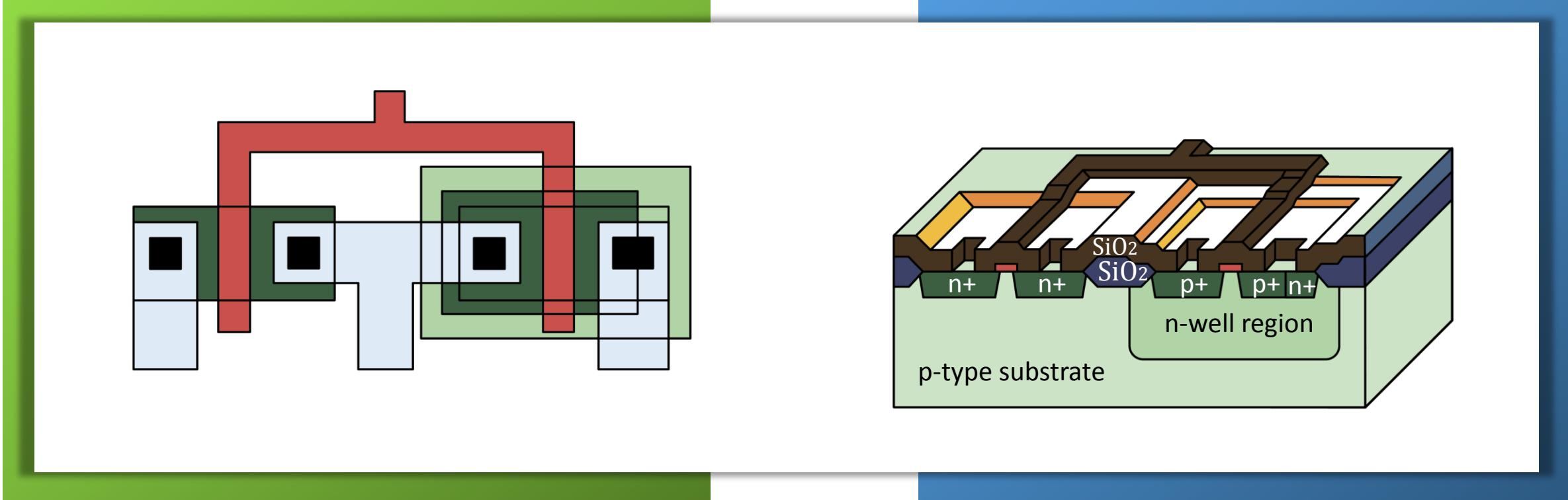
Fabrication of a CMOS Inverter (Contd.)



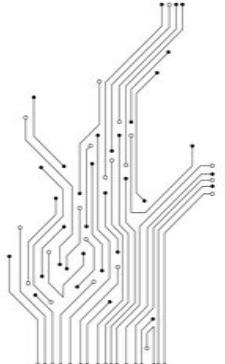
Using a set of two masks, the n+ and p+ regions are implanted into the substrate and into the n-well respectively. Also, the ohmic contacts to the substrate and to the n-well are implanted in this process step. (After Atlas of IC Technologies, by W. Maly.)



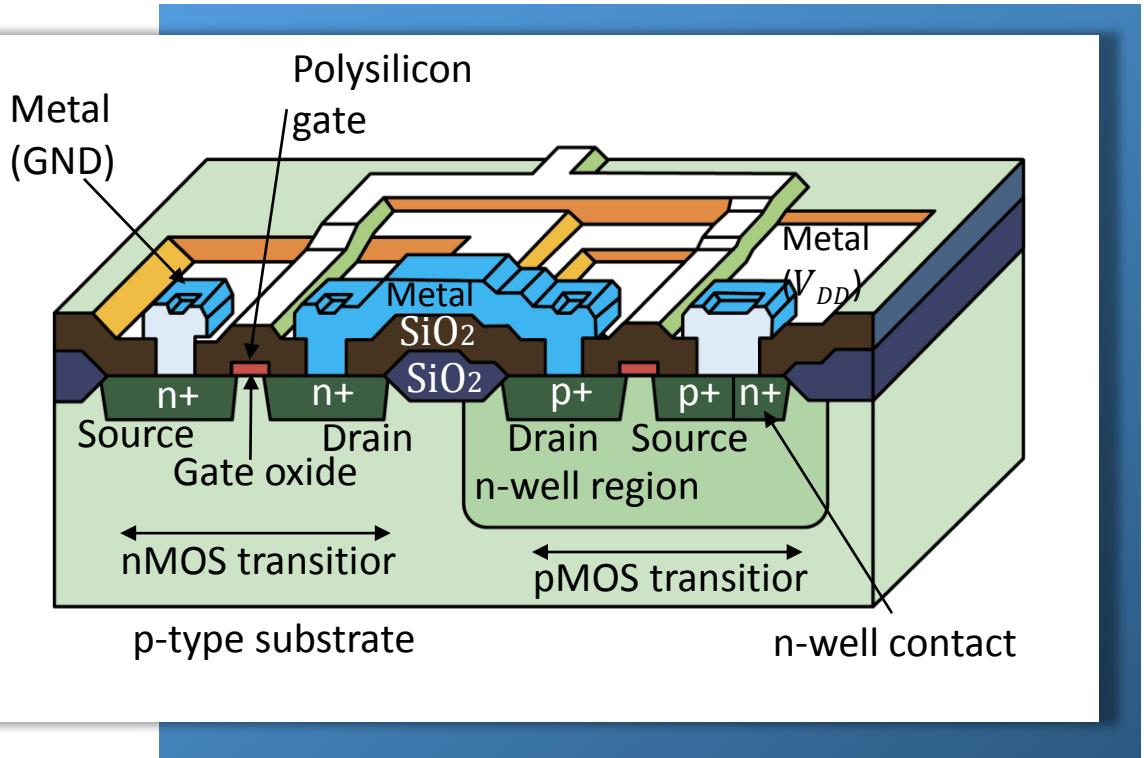
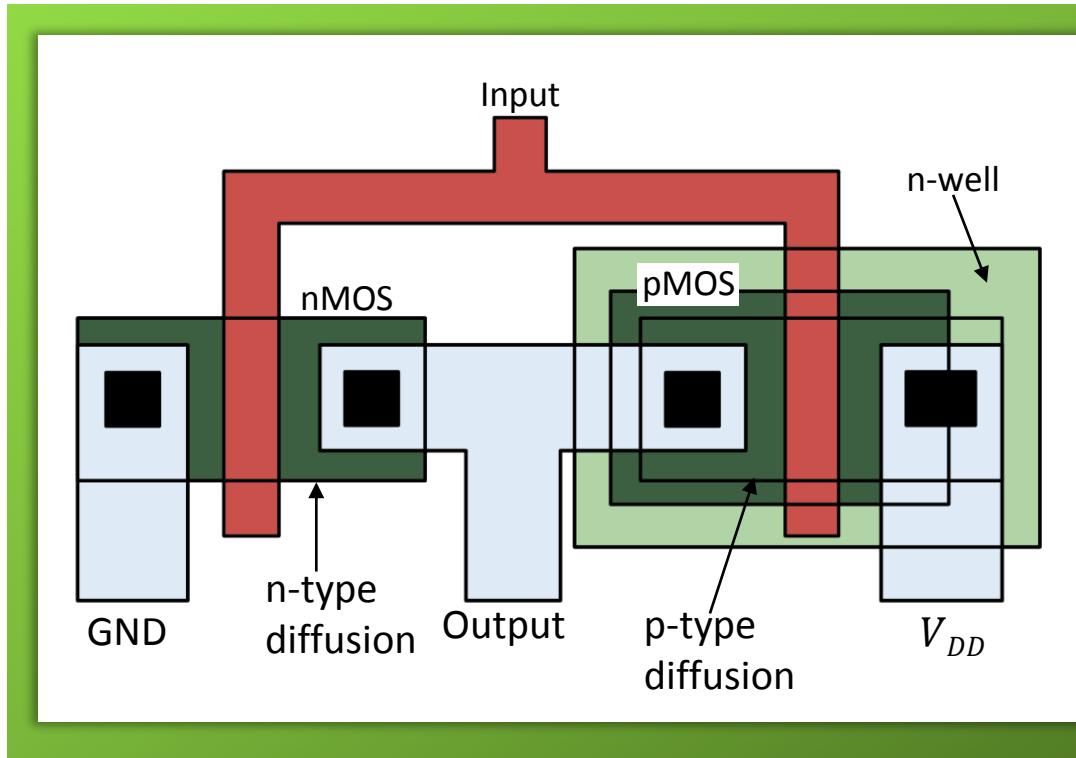
Fabrication of a CMOS Inverter (Contd.)



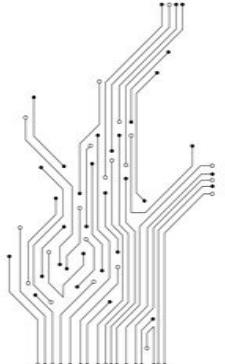
An insulating silicon dioxide layer is deposited over the entire wafer using CVD. Then, the contacts are defined and etched away to expose the silicon or polysilicon contact windows. These contact windows are necessary to complete the circuit interconnections using the metal layer, which is patterned in the next step. (After Atlas of IC Technologies, by W. Maly.)



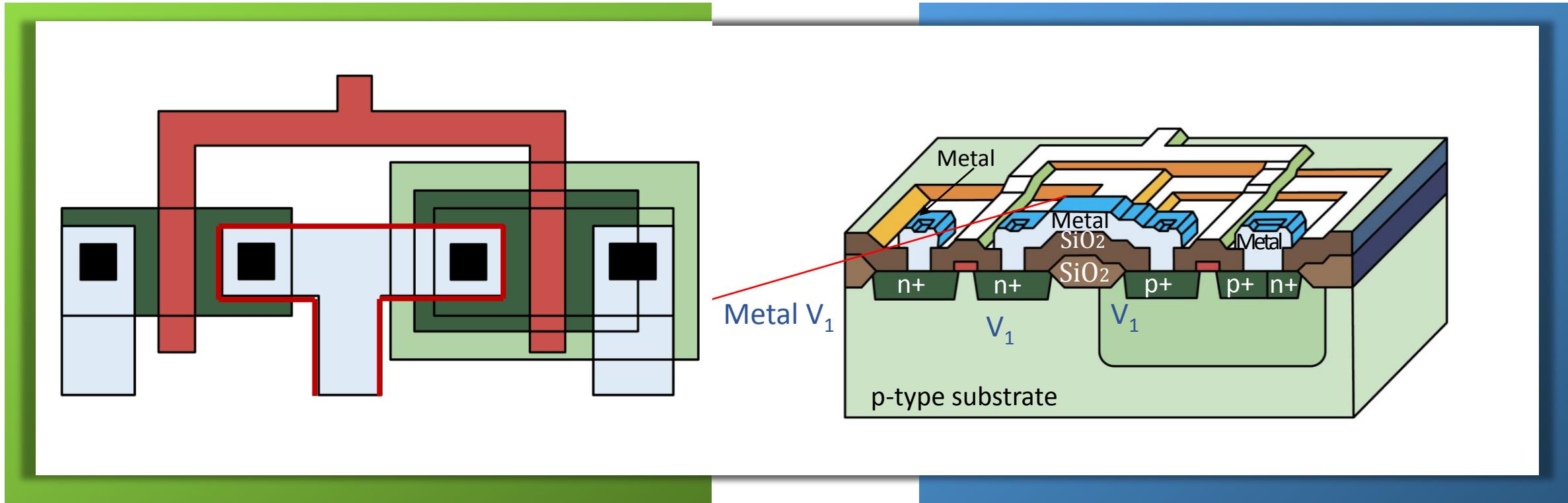
Fabrication of a CMOS Inverter (Contd.)



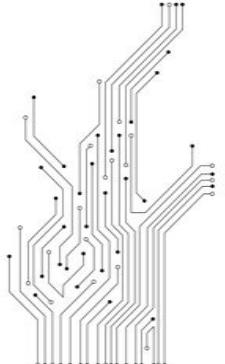
The composite layout and the resulting cross-sectional view of the chip showing one nMOS and one pMOS transistor (in the n-well), and the polysilicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except over wire-bonding pad areas. (After Atlas of IC Technologies, by W. Maly.)



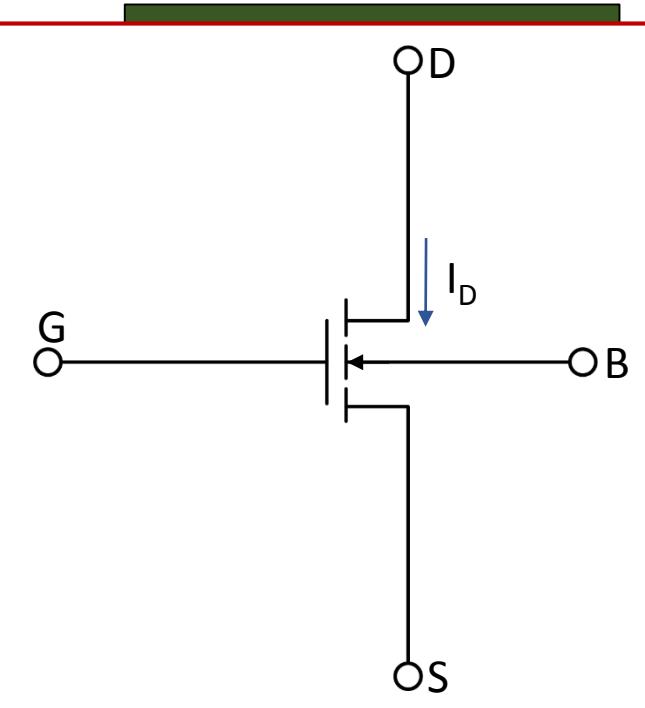
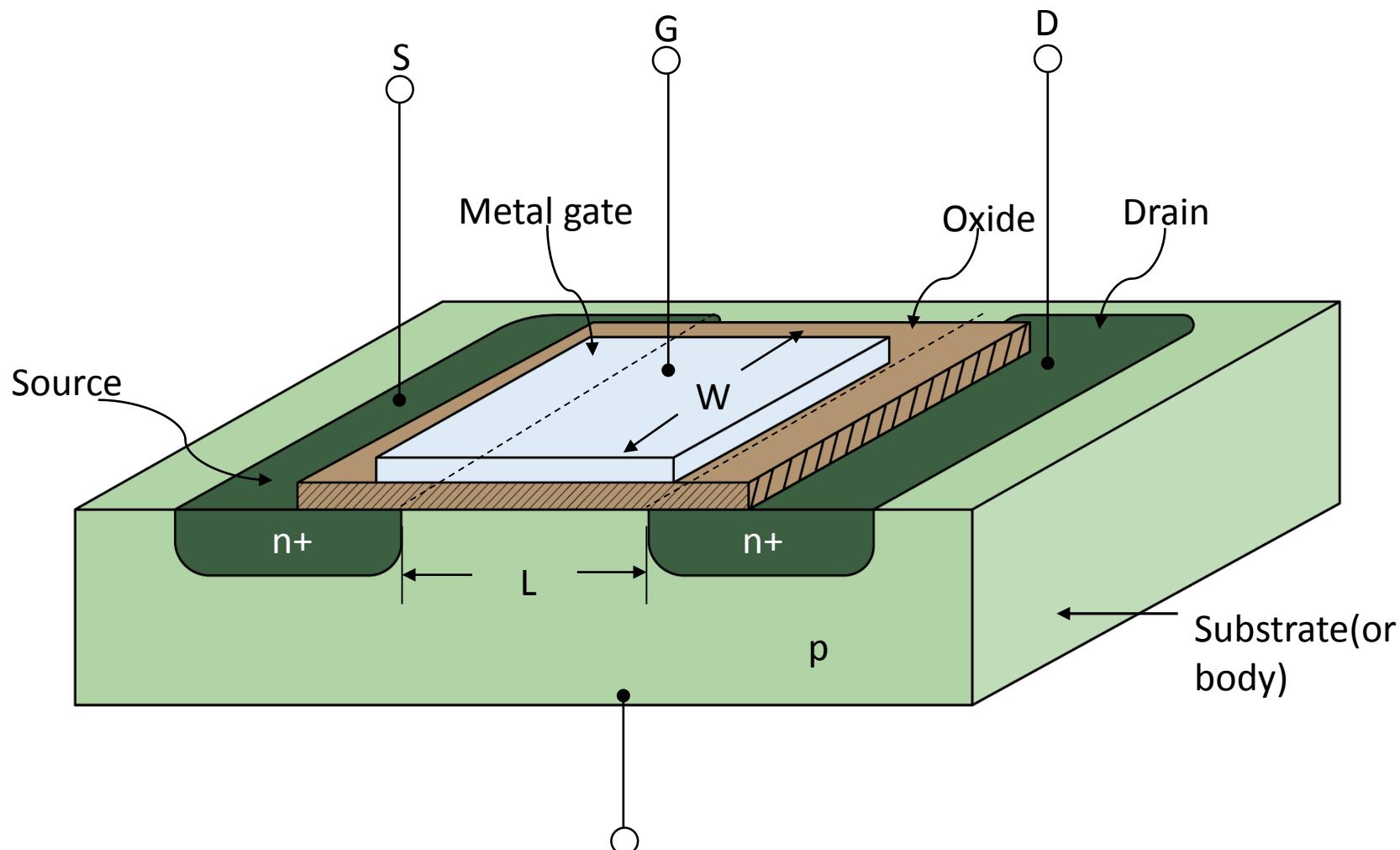
Fabrication of a CMOS Inverter (Contd.)



Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching. Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and ultimately essential for circuit reliability. (After Atlas of IC Technologies, by W. Maly.)



N-channel Enhancement-mode MOSFET

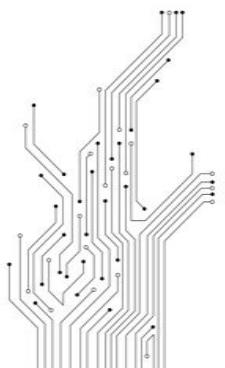


Summary

MOSFET is an acronym for Metal-Oxide Semiconductor Field Effect Transistor. The name “MOSFET” is derived from its physical structure. It is also commonly known as MOS.

In this course, we will only focus of the enhancement-mode MOSFET. As such, an N-channel enhancement-mode MOSFET shall be denoted as nMOS and a P-channel enhancement-mode MOSFET shall be denoted as pMOS.

A MOS consists of 4 terminals: the Gate terminal (G), the Source terminal (S), the Drain terminal (D) and the Body terminal (B).



Observations

The substrate (or Body) forms pn junction with the source (S) and drain (D) regions. In normal operation, the pn junctions are kept reverse bias at all times.

The substrate (or Body) has no effect on device operation, therefore, the MOSFET is usually treated as a three terminal device in most of the circuit analysis.

There are three regions of operations for a MOSFET:

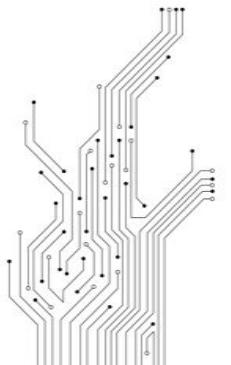
i. Cut-off region ($v_{GS} < V_{to}$)  

ii. Linear/Triode/Ohmic region

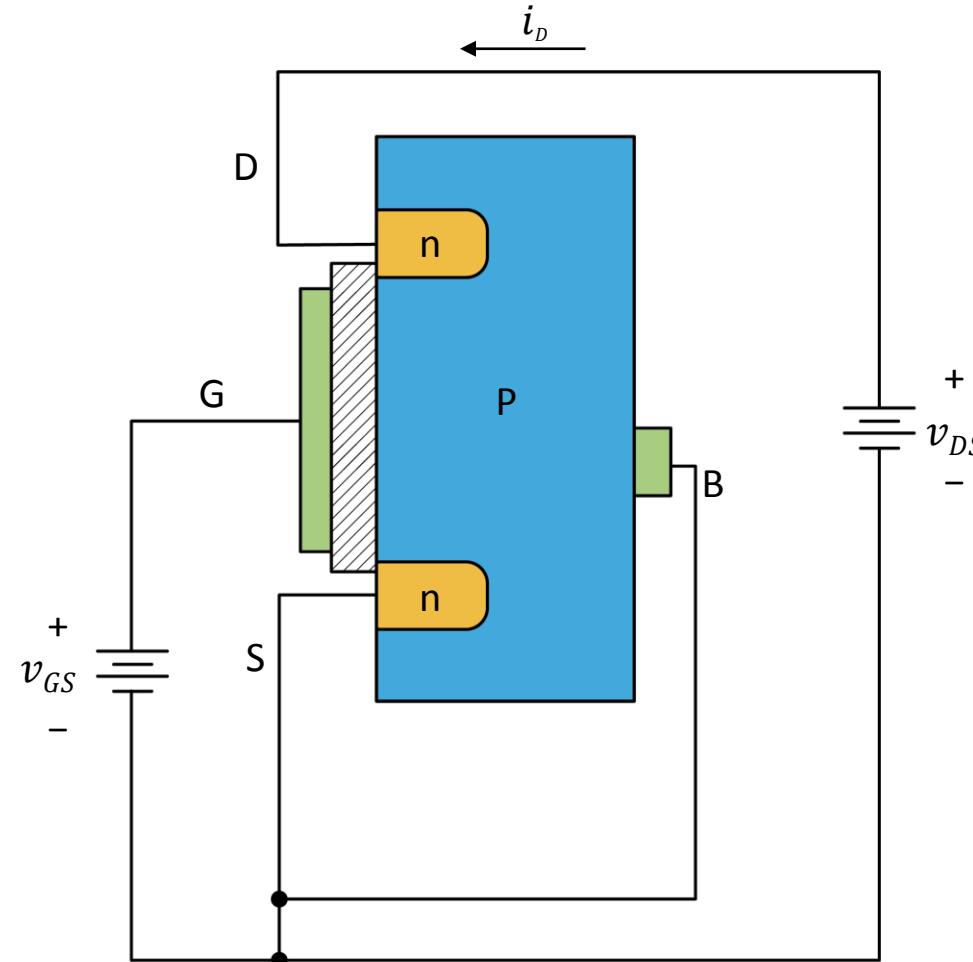
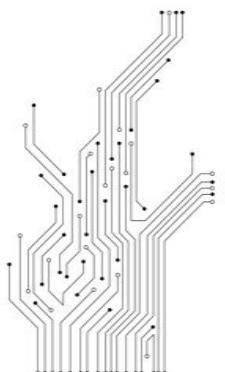
$$(v_{GS} \geq V_{to}, v_{DS} \leq v_{GS} - V_{to})$$

iii. Saturation region ($v_{GS} \geq V_{to}, v_{DS} \geq v_{GS} - V_{to}$)


On

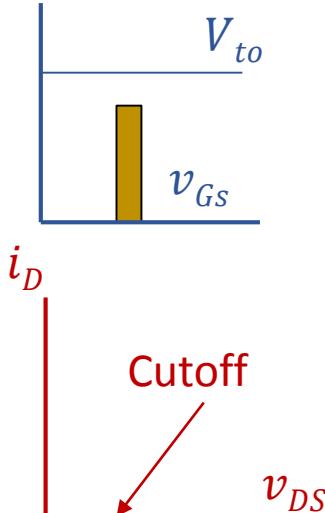
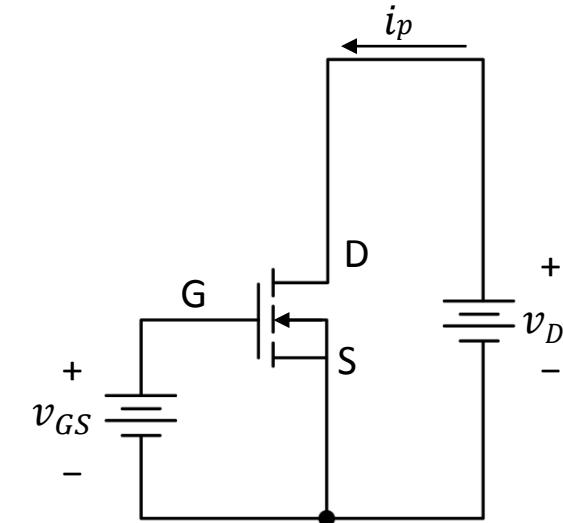


Region 1: Cut-off Region

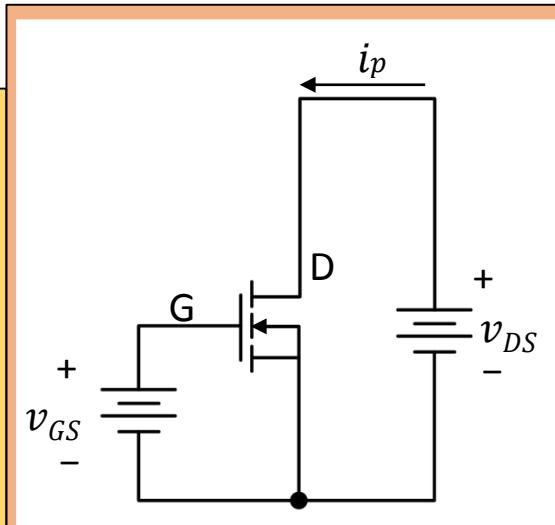
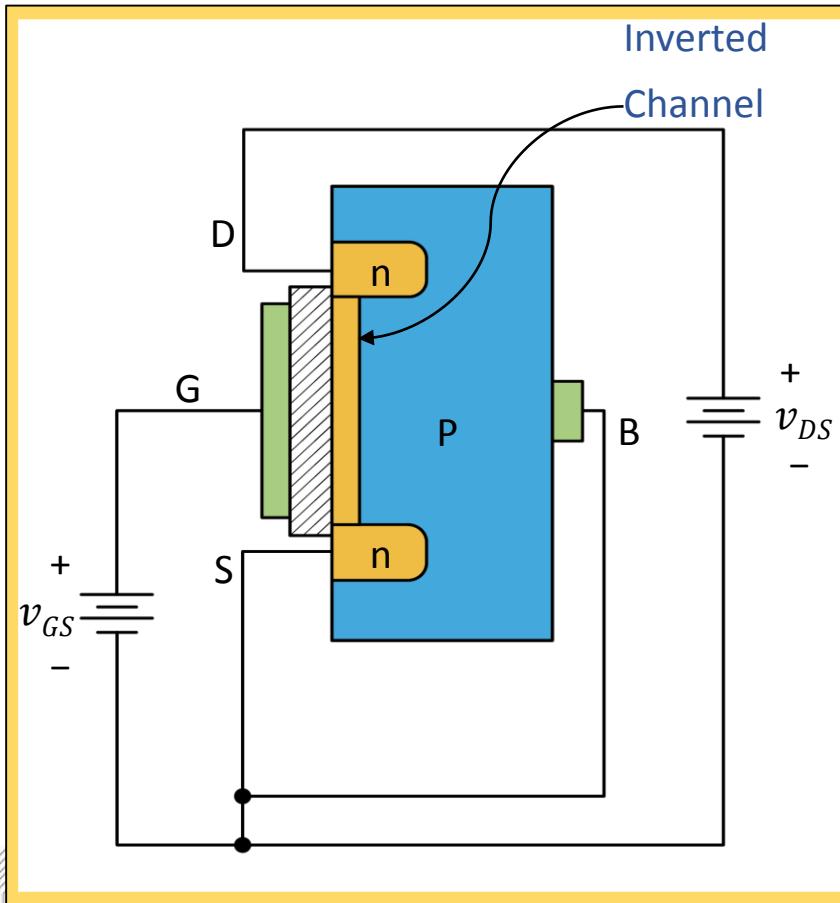


Analysis

- Body is connected to ground
- $v_{GS} < V_{to} \Rightarrow i_D = 0$



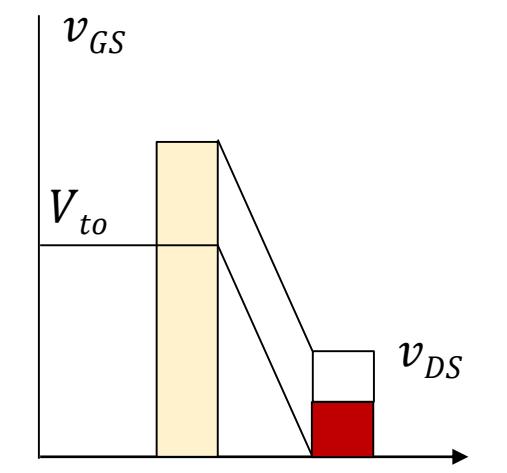
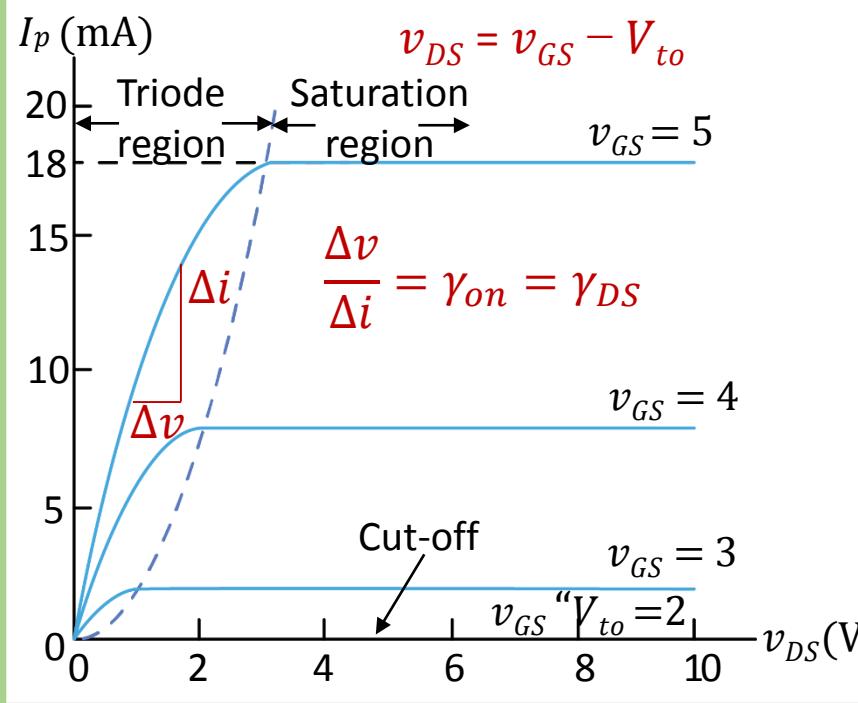
Region 2: Triode / Linear / Ohmic Region



Analysis

- $v_{GS} \geq V_{to}$
- $v_{DS} \leq v_{GS} - V_{to}$

V_{OD} , V_{eff} , v_{DS} (Sat)



Triode Region

Drain Characteristic: ($v_{GS} \geq v_{to}$ and $v_{GS} - v_{to} \geq v_{DS}$)

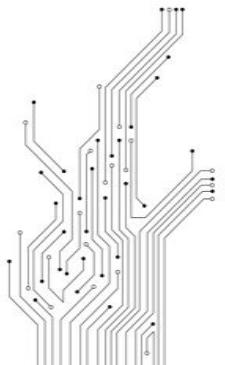
$$i_D = K \left((v_{GS} - v_{to}) v_{DS} - \frac{1}{2} v_{DS}^2 \right) \quad \text{--- (1)} \quad \frac{1}{2} v_{DS}^2$$

where $K = K' \left(\frac{W}{L} \right)$ and $K' = \mu_n C_{ox}$

What is the resistance of the NMOS transistor?

Assuming in equation (1) is negligible, the resistance r_{DS} is:

$$r_{DS} = r_{on} = \frac{v_{DS}}{i_D} = \frac{1}{K(v_{GS} - V_{to})}$$



Triode Region: (Contd.)

The drain current i_D at triode region is:

$$i_D = (\mu_n C_{ox}) \left(\frac{W}{L} \right) \left((v_{GS} - V_{to}) v_{DS} - \frac{1}{2} v_{DS}^2 \right) \frac{W}{L}$$

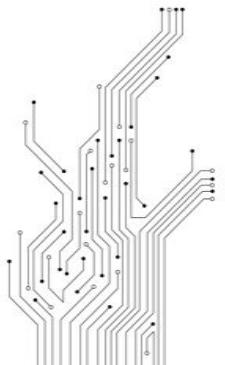
45 nm process →

Large $W \rightarrow$ High speed
Small $W \rightarrow$ Low power

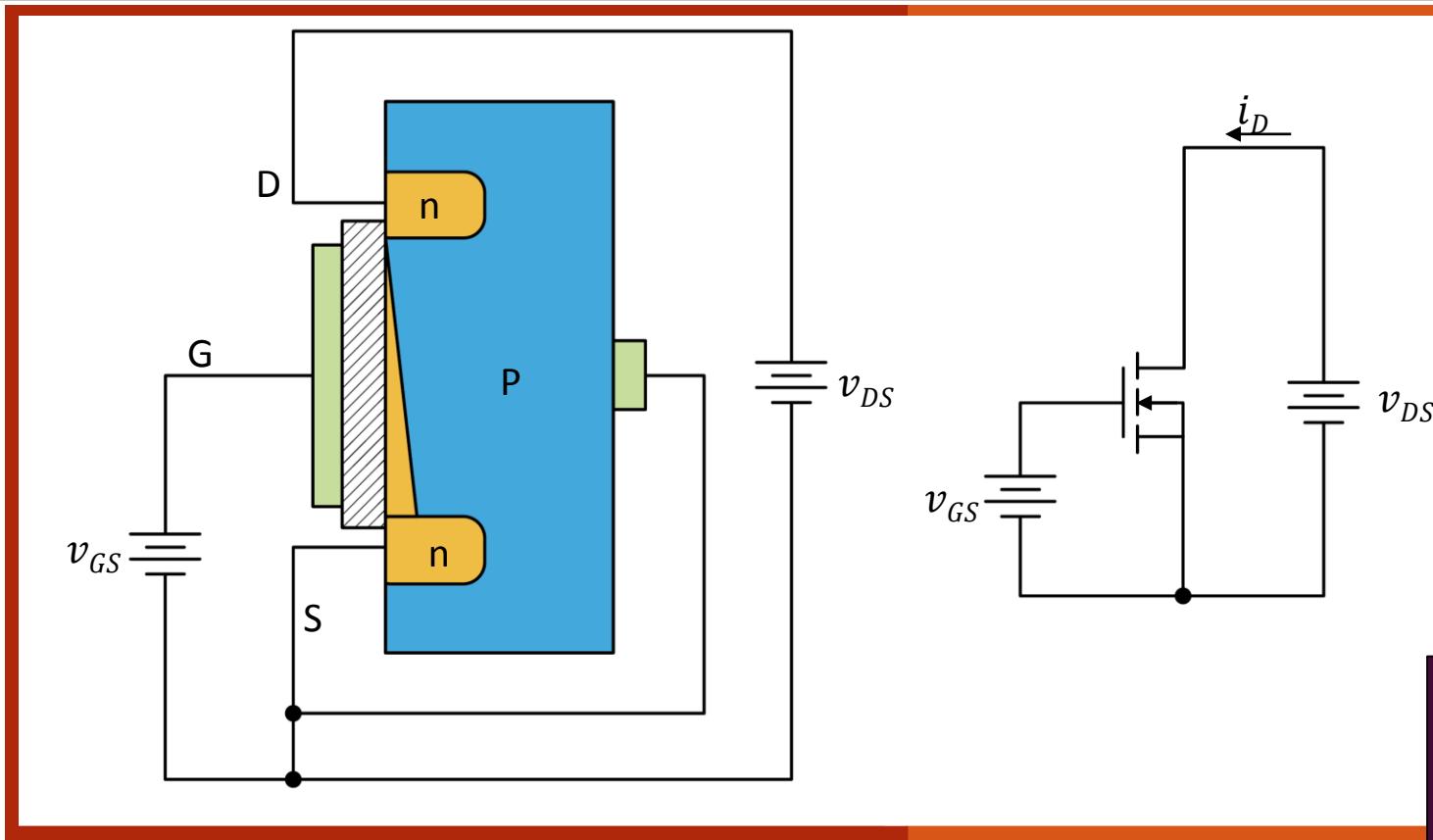
Analysis

$L \approx 45 \text{ nm}$

- $\mu_n C_{ox}$ depends on the physics and fabrication process.
- i_D can be controlled by the ratio of.
- MOSFET is operating like a linear resistor whose value is controlled by v_{GS} .



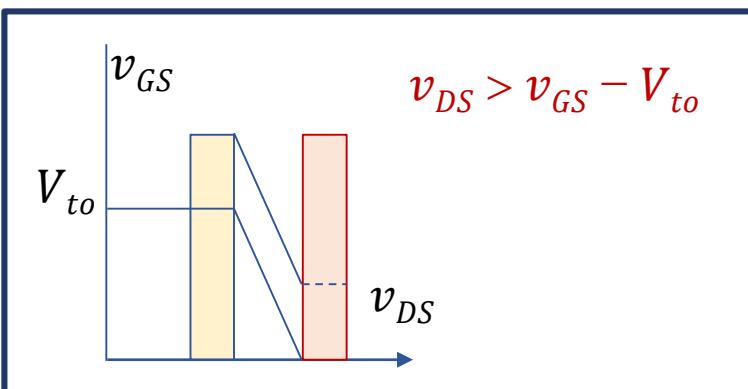
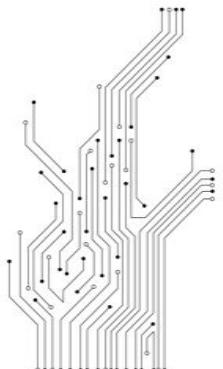
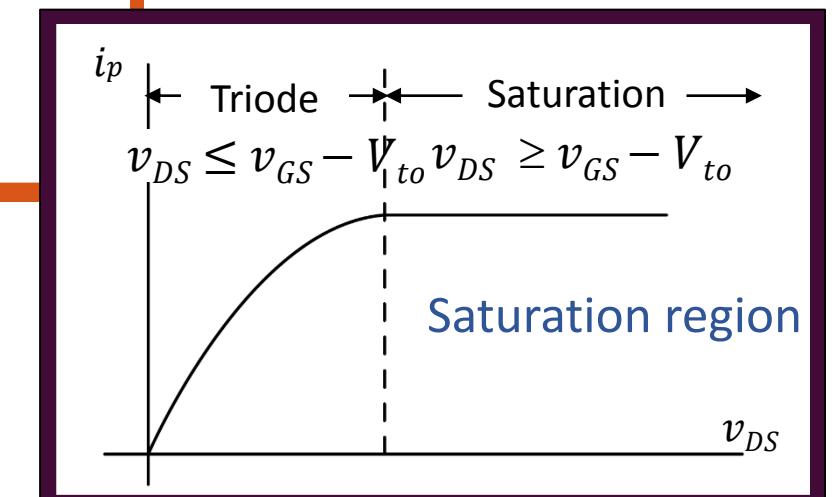
Region 3: Saturation Region



Analysis

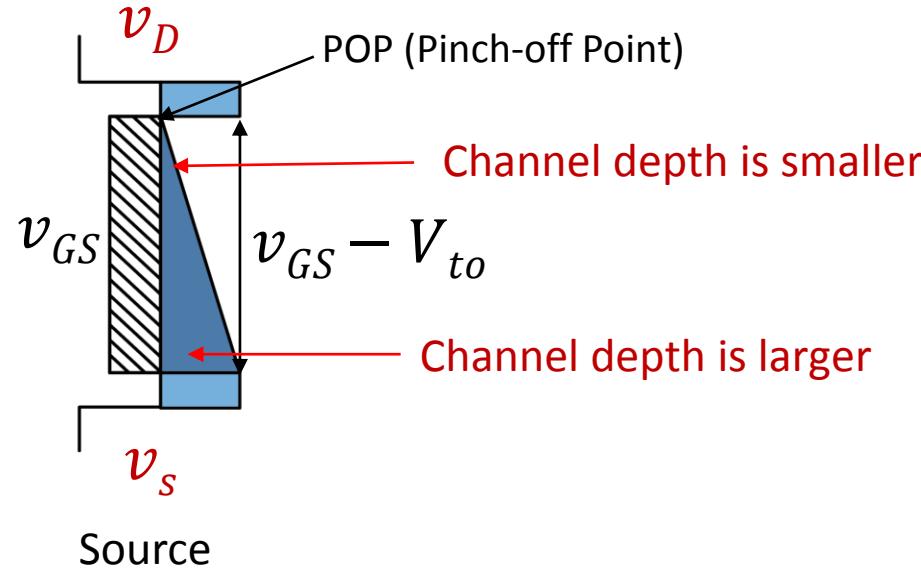
- $v_{GS} \geq V_{to}$, V_{OD} , V_{eff} , $V_{DS(SAT)}$
- $v_{DS} \geq v_{GS} - V_{to}$
- v_{GS} is held constant

i_p ← Triode → Saturation
 $v_{DS} \leq v_{GS} - V_{to}$ $v_{DS} \geq v_{GS} - V_{to}$

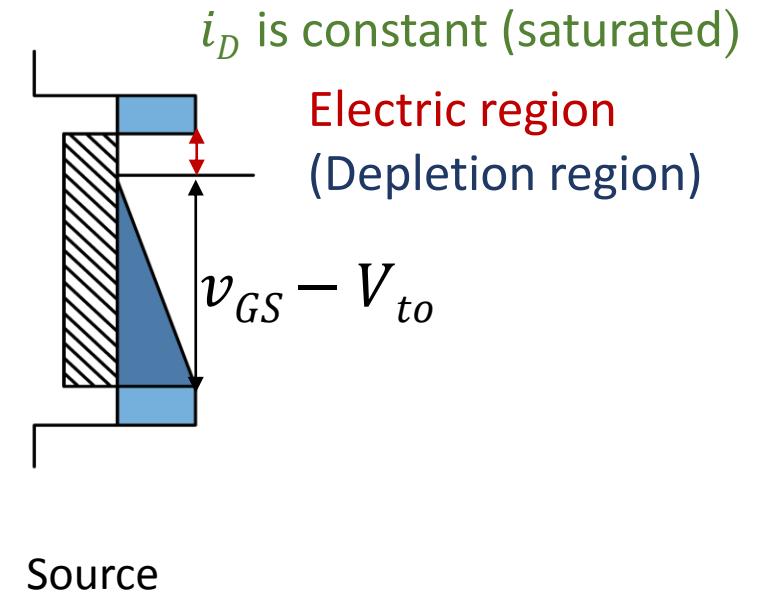


Pinch-Off Point

$$v_{pop} = v_{DS} = v_{GS} - V_{to}$$

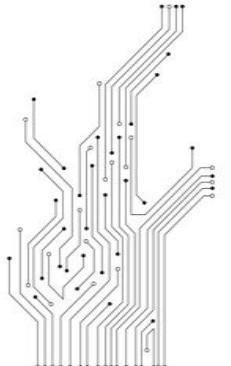


$$v_{DS} \geq v_{GS} - V_{to}$$



Analysis

- At pinch-off, $v_{DS} = v_{GS} - V_{to}$. (Try to locate this point in the IV characteristics curve).
- The inversion charge at the drain is zero.
- Pinch-off point is voltage across oxide layer at pinch-off point = V_{to} .



Saturation Region: (Contd.)

$V_{OD}, V_{eff}, V_{DS(SAT)}$

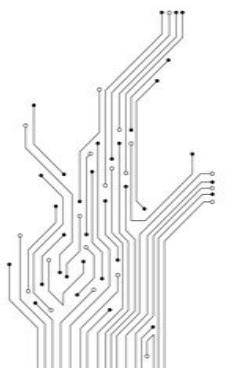
Drain Characteristics ($v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$)

In the saturation region, the drain current i_D is:

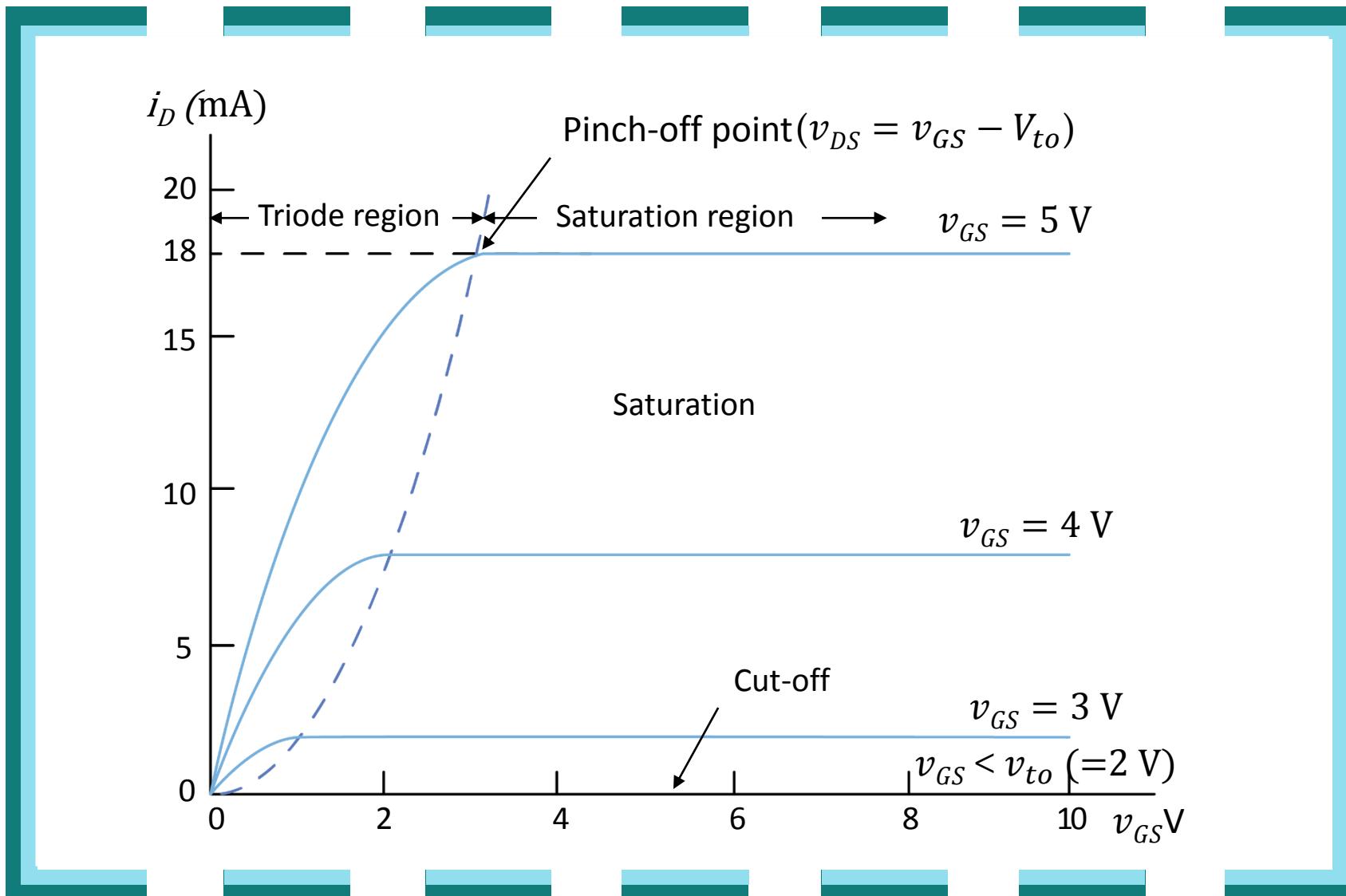
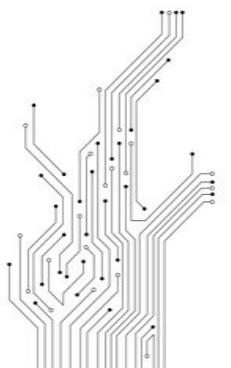
$$i_D = \frac{1}{2} K(v_{GS} - V_{to})^2$$

where $K = K' \left(\frac{W}{L} \right)$, $K' = \mu C_{ox}$ and K' is typically $50 \mu A/V^2$

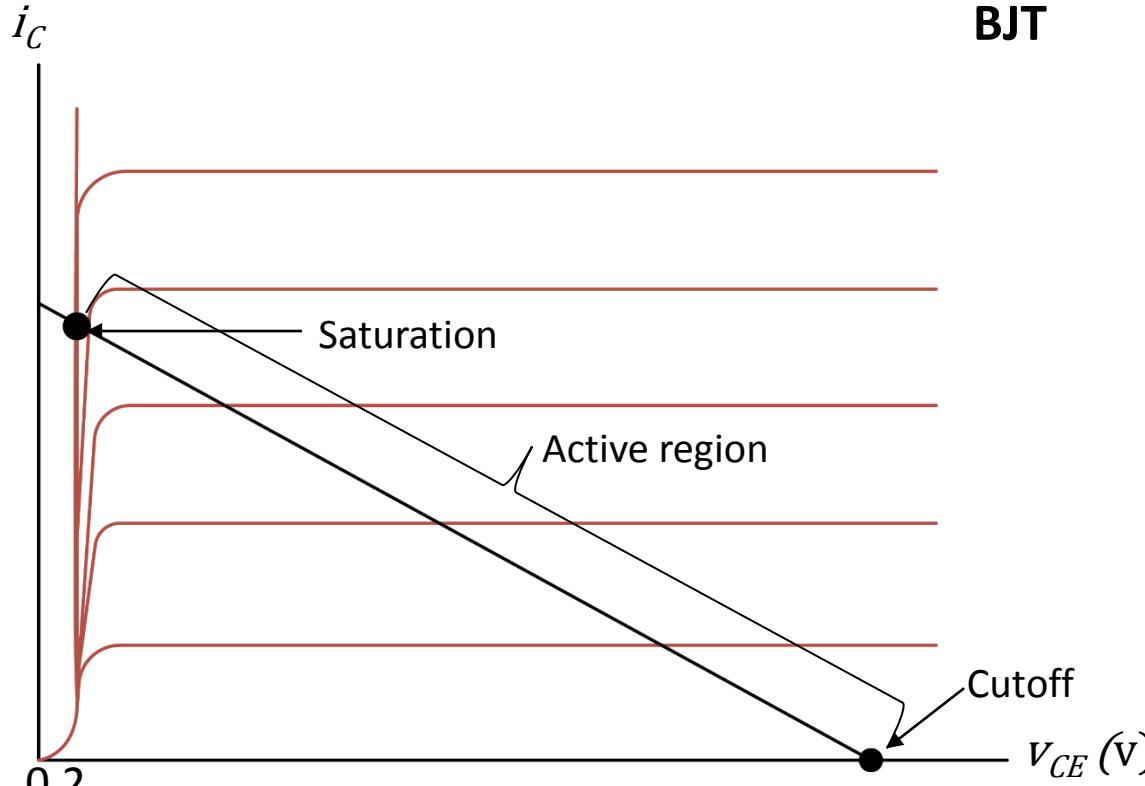
$$i_D = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_{to})^2$$



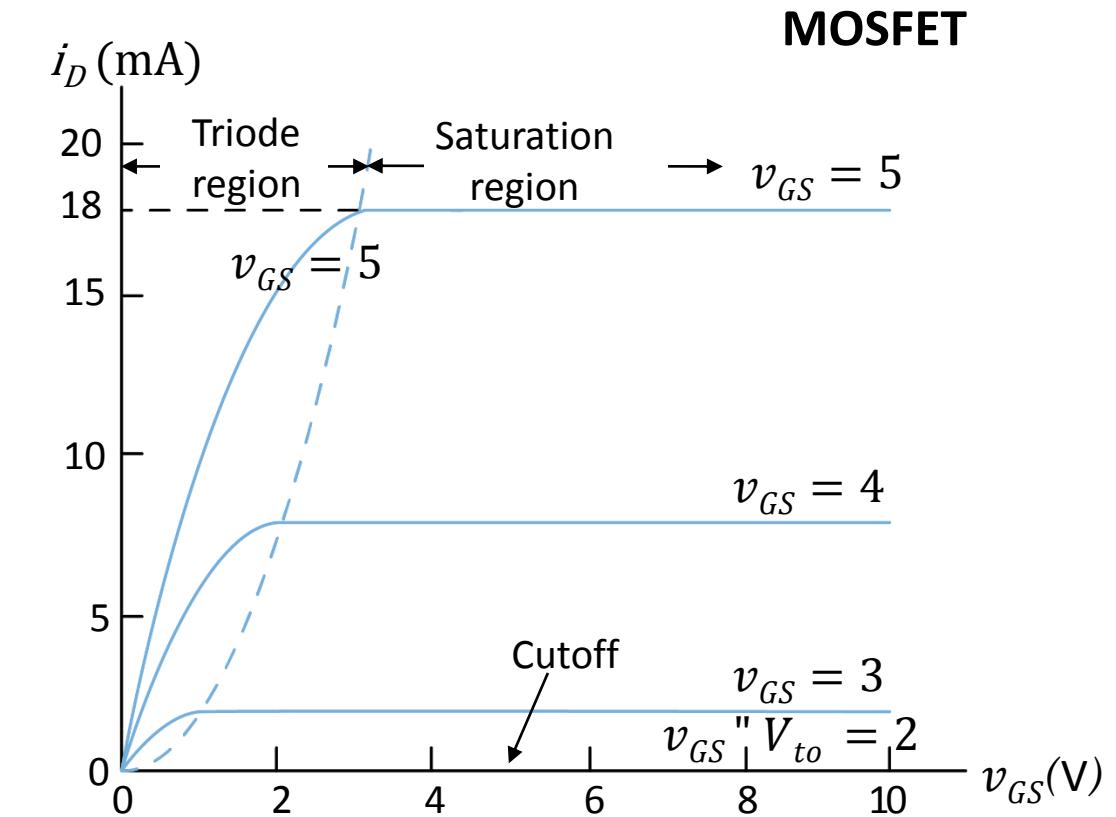
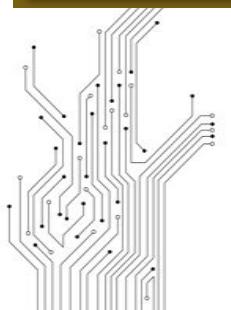
A Typical Drain I-V Characteristics



Saturation Region: Difference Between BJT and MOSFET



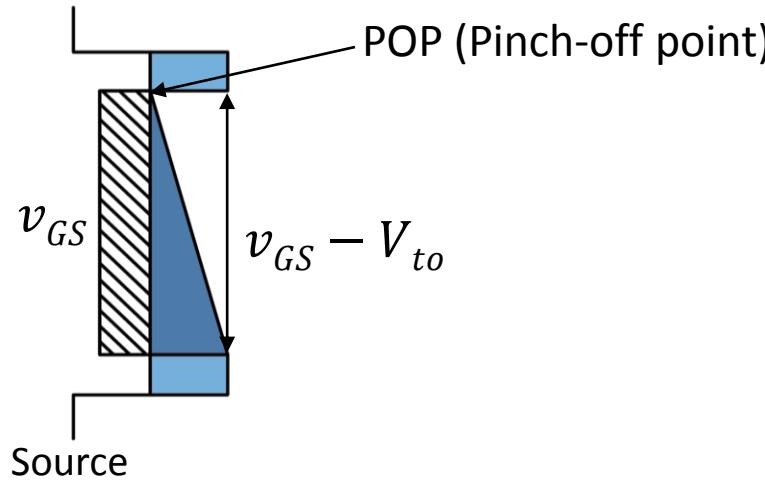
$V_{BE(sat)}$ is fixed, $V_{BE(sat)} \approx 0.2$ V



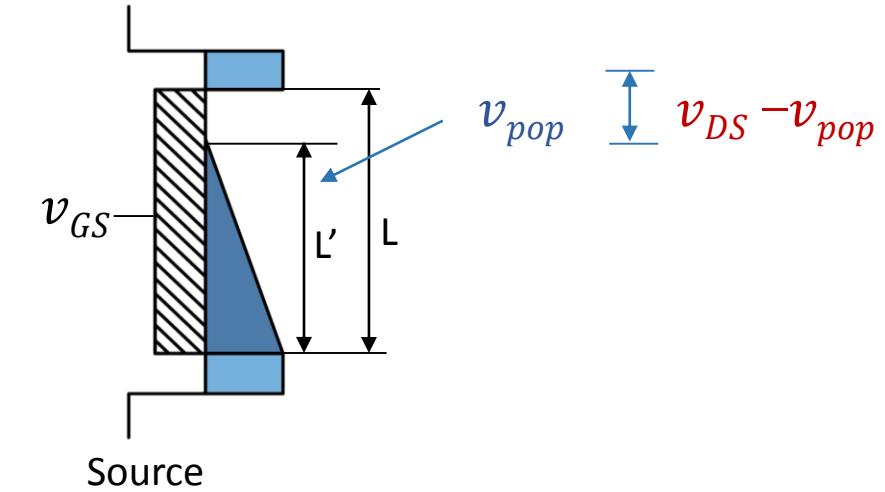
$v_{DS(sat)}$ varies, $v_{DS(sat)} = v_{GS} - V_{to}$

Short-Channel Length Effect

$$v_{pop} = v_{DS} = v_{GS} - V_{to}$$

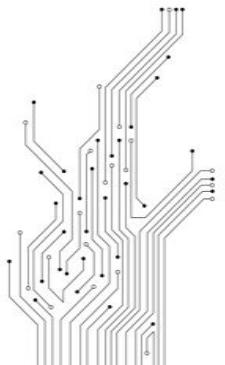


$$v_{DS} \geq v_{GS} - V_{to}$$

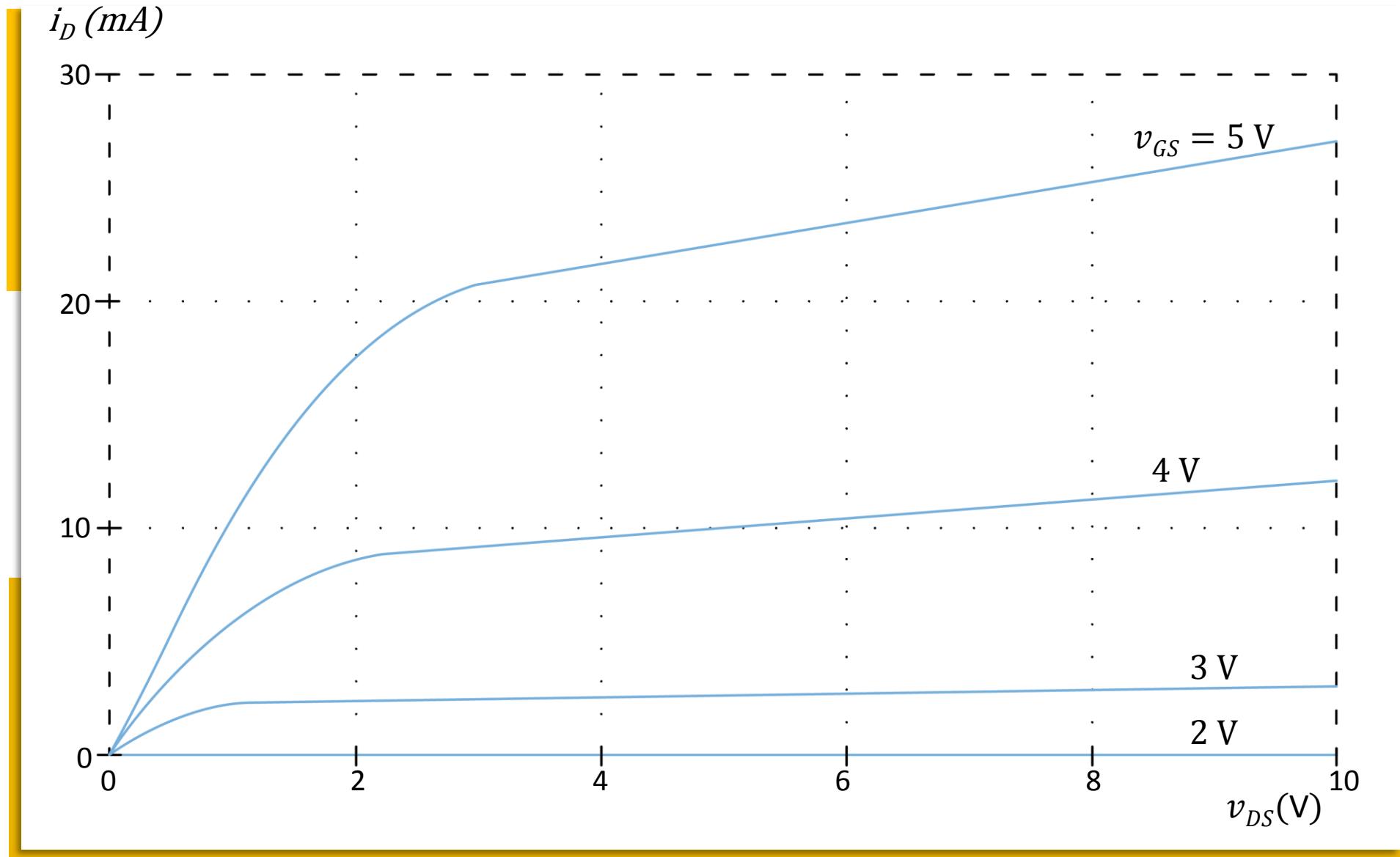
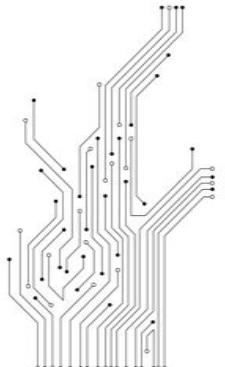


Analysis

- At pinch-off, $v_{DS} = v_{GS} - V_{to}$. When v_{DS} is increased further ($v_{DS} > v_{DS(sat)}$), an even larger portion of the channel become pinch-off.
- The effective channel length is reduced $L' = L - \Delta L$.



Short-Channel Length Effect on Drain Characteristic



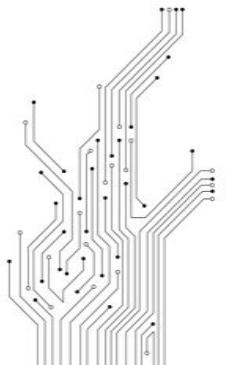
Channel-length Modulation Effect (Contd.)

In the Saturation Region: Due to channel effect

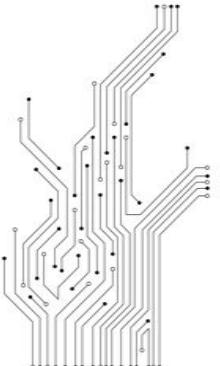
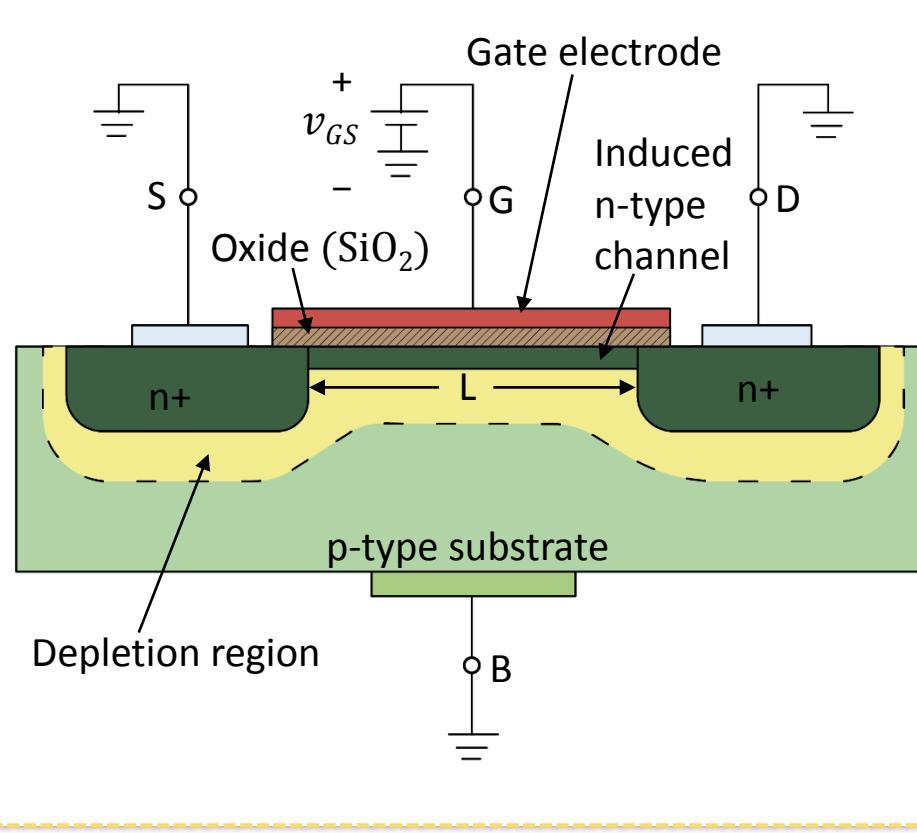
$$i_D = \frac{1}{2} K(v_{GS} - V_{to})^2 \underbrace{(1 + \lambda v_{DS})}_{\text{Due to channel effect}}$$

For longer L the channel-length modulation parameter λ will be 0.

(λ is assumed to be zero unless otherwise stated.)



The Body Effect



The threshold voltage of a MOS is:

$$v_t = V_{t0} + \gamma \left[\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f} \right]$$

Where:

V_{t0} = threshold voltage for $V_{SB} = 0$

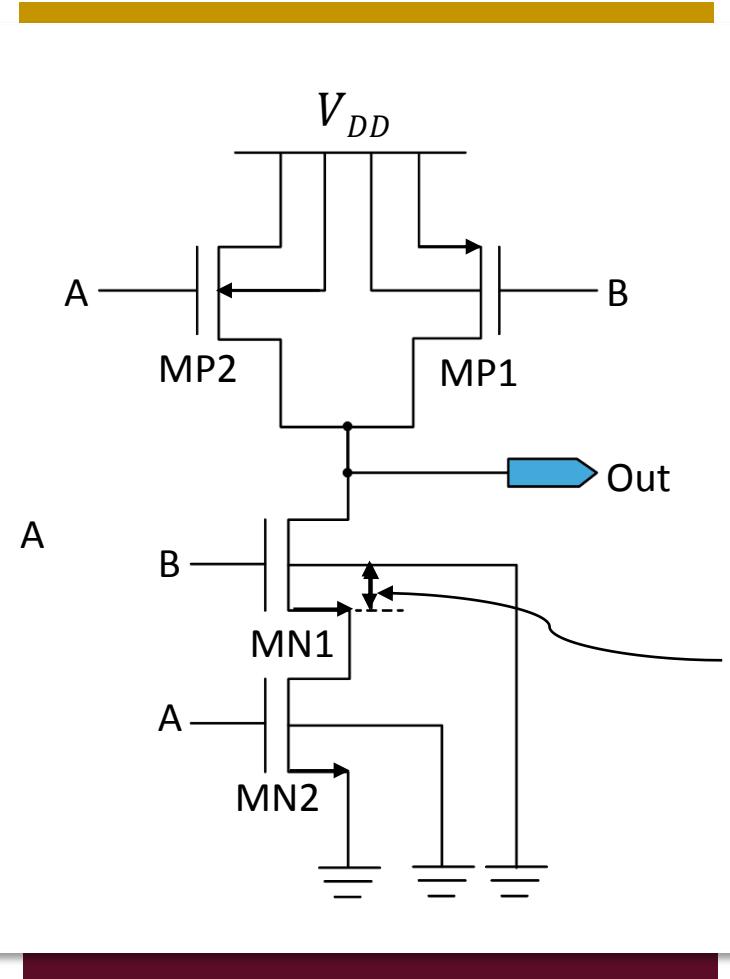
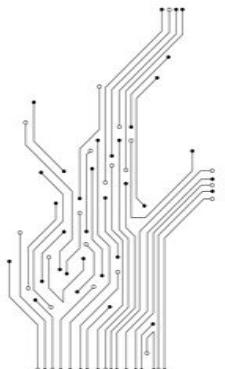
V_{SB} = reverse substrate bias voltage

γ = fabrication process parameter = $\frac{\sqrt{2qN_A\varepsilon_S}}{C_{ox}}$

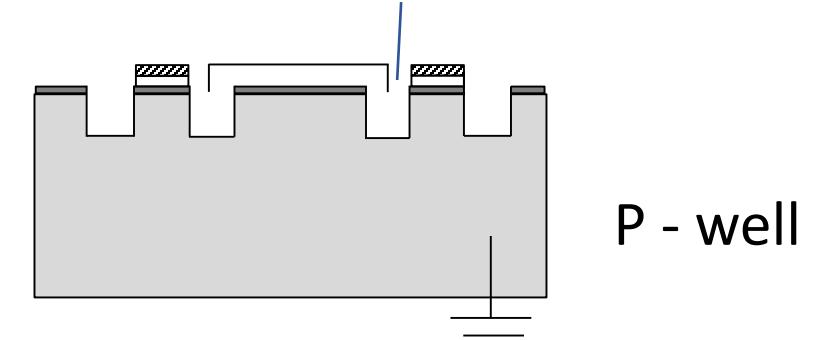
φ_f = physical parameter with $2\varphi_f$ typically = 0.6V

The Body Effect

When to include the body effect ?

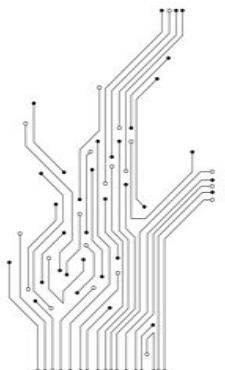
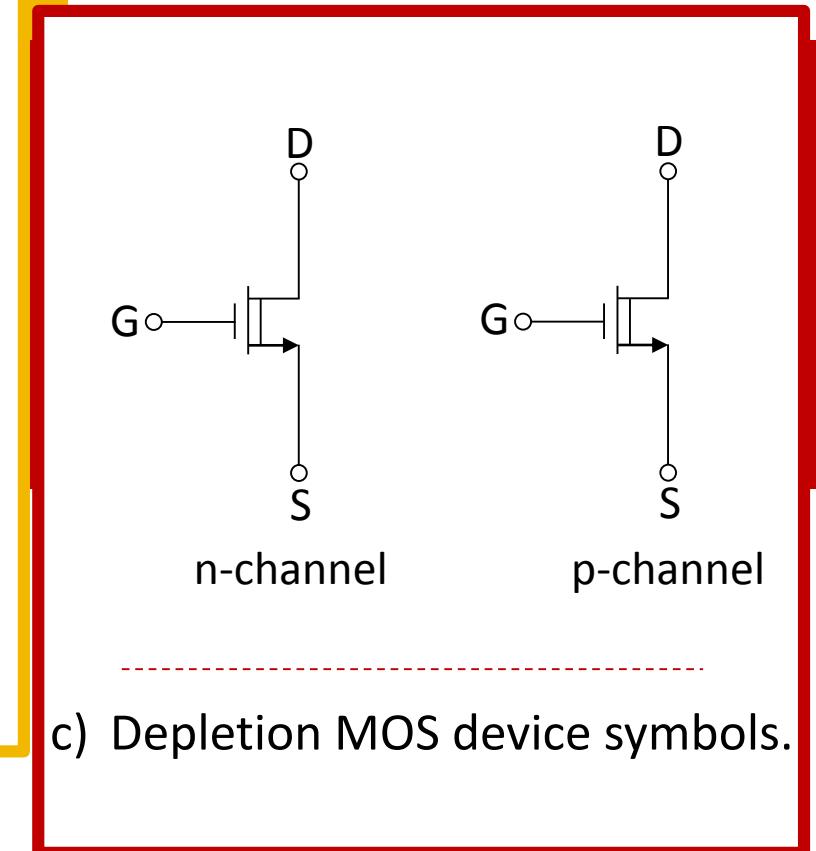
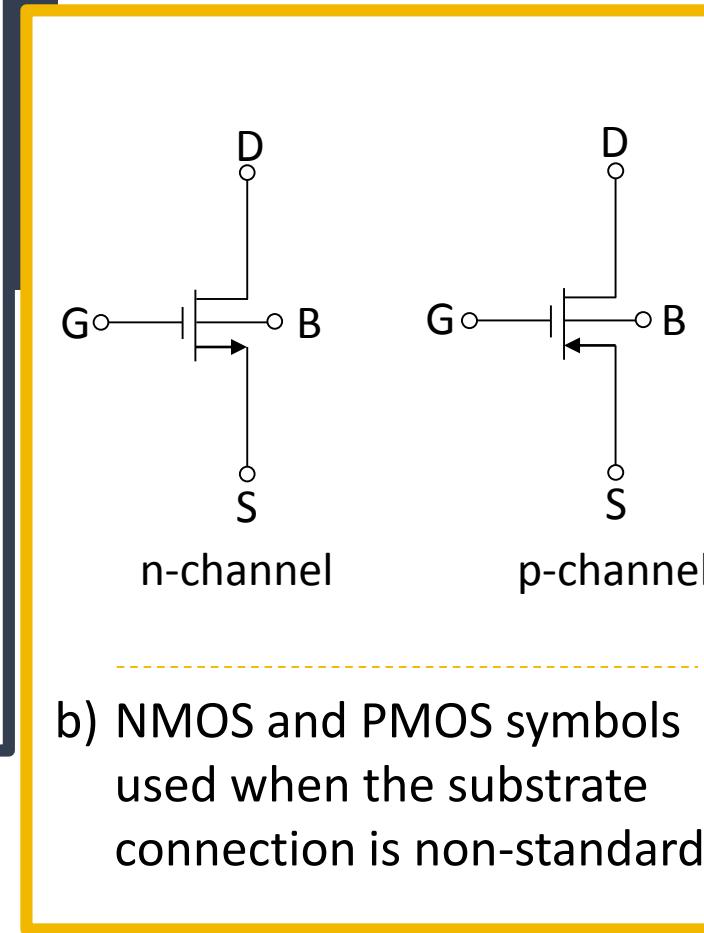
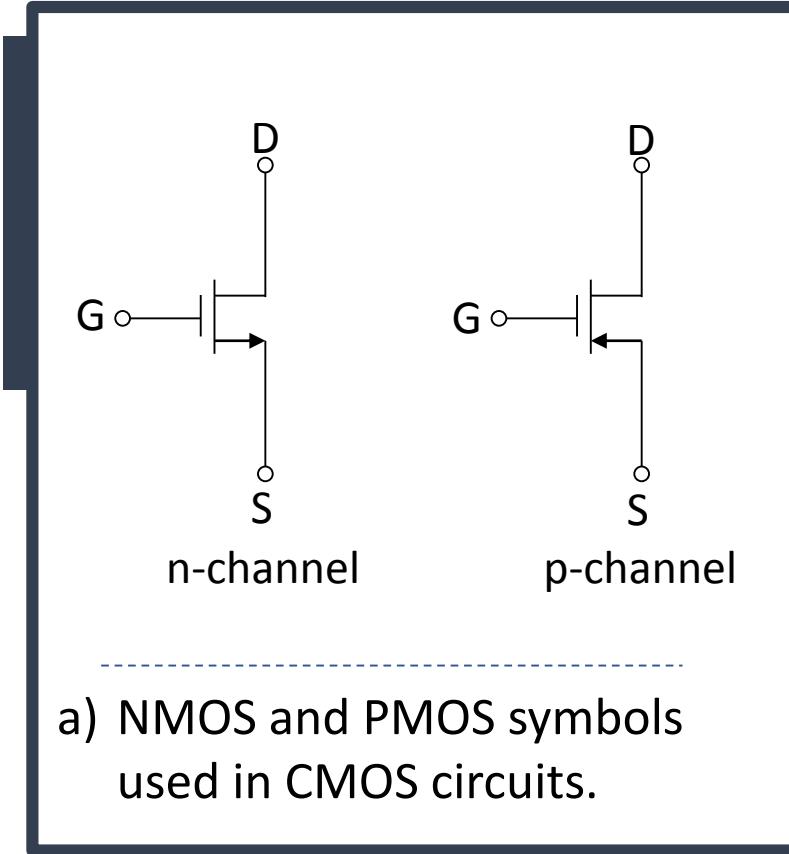


Reverse bias between the source and the body



Ans: When $V_{SB} \neq 0$

More Alternative Symbols of MOSFET



Summary of MOSFET

	nMOS	pMOS
MOSFET	N-enhancement	P-enhancement
V_{to}	Positive	Negative
v_{DS}	Positive	Negative
Cut-off	$v_{GS} < V_{to}$	$ v_{GS} < V_{to} $
Triode region	$v_{DS} \leq v_{GS} - V_{to}$ $I_{DS} = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$	$ v_{DS} \leq v_{GS} - V_{to} $ $I_{DS} = K[2(v_{GS} - V_{to}) v_{DS} - v_{DS}^2]$
Saturation region	$v_{DS} \geq v_{GS} - V_{to}$ $I_{DS} = K(v_{GS} - V_{to})^2$	$ v_{DS} \geq v_{GS} - V_{to} $ $I_{DS} = K(v_{GS} - V_{to})^2$
K	$K = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right)$	$K = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L} \right)$

$-v_{GS} > -V_{to}$

Summary of MOSFET

$V_T: 25mV/300k$

V_{to} : No bias between body and source (Nominal threshold process voltage or no body effect)

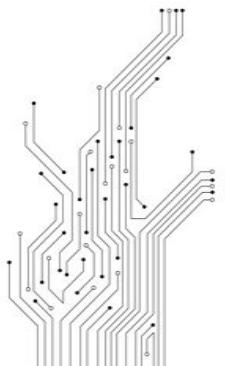
V_{tp} = pMOS threshold voltage

V_{tn} = nMOS threshold voltage

$$V_{th} = \frac{1}{2} V_{DD}$$

Threshold voltage for digital gate

1 logic gate (at least 2 CMOS transistors)



Three Applications of MOSFET

1. A voltage-controlled resistor in the **triode** or **ohmic** region, R_{DS} controlled by v_{GS} .

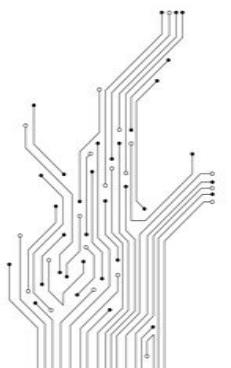
(Linear)

(Current ID remains constant)

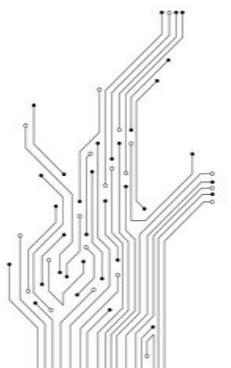
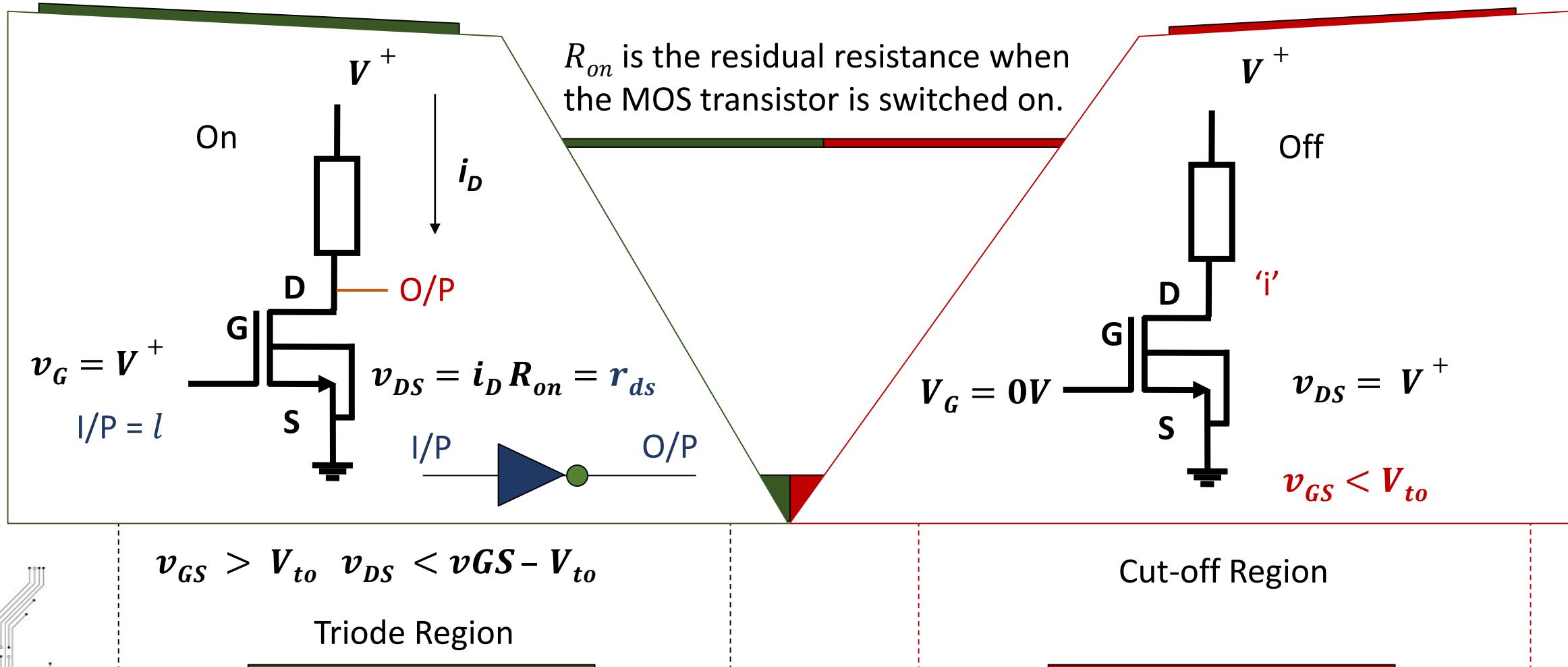
2. An amplifier when the FET operates in the **saturation** region.

(Saturation region)

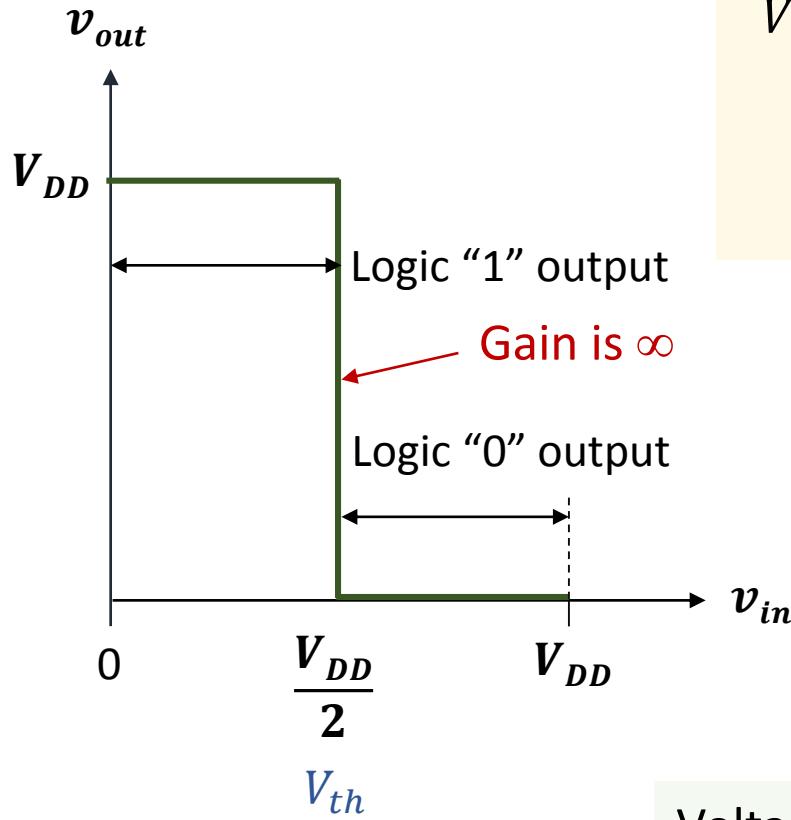
3. A switch, ON in the **triode** region, OFF in the **cutoff** region, transit through the saturation region.



nMOS as On-Off Switch

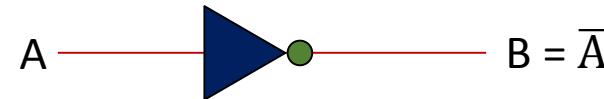


Ideal Inverter



V_{th} : Inverter threshold voltage

$$0 < v_{in} < V_{th} \rightarrow v_o = '1'$$
$$V_{th} < v_{in} < V_{DD} \rightarrow v_o = '0'$$



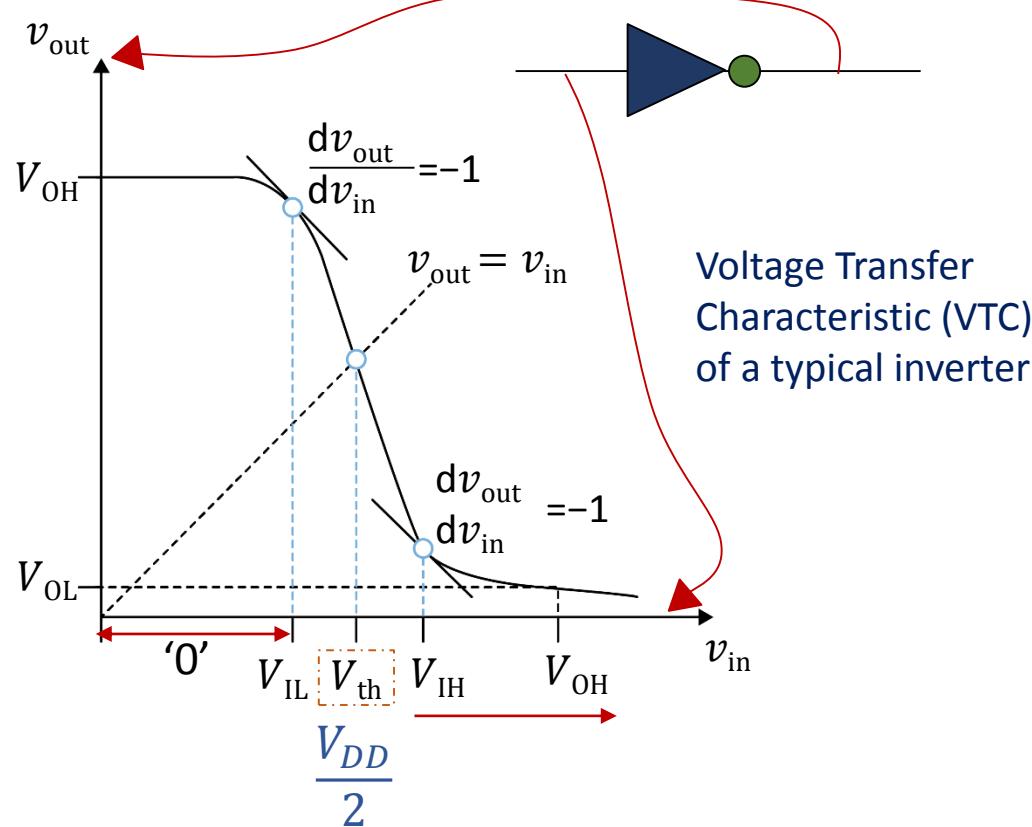
A	B
0	1
1	0

Truth table

Voltage Transfer Characteristics (VTC) of an ideal inverter



Voltage Transfer Characteristics (VTC)



V_t : Device threshold voltage

V_{th} : Digital gate threshold voltage
where $v_{out} = v_{in}$

Output

V_{OH} : Max v_o when O/P is '1'

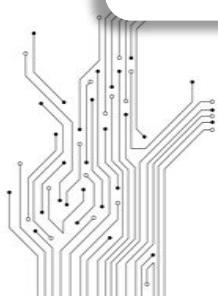
V_{OL} : Min v_o when O/P is '0'

Input

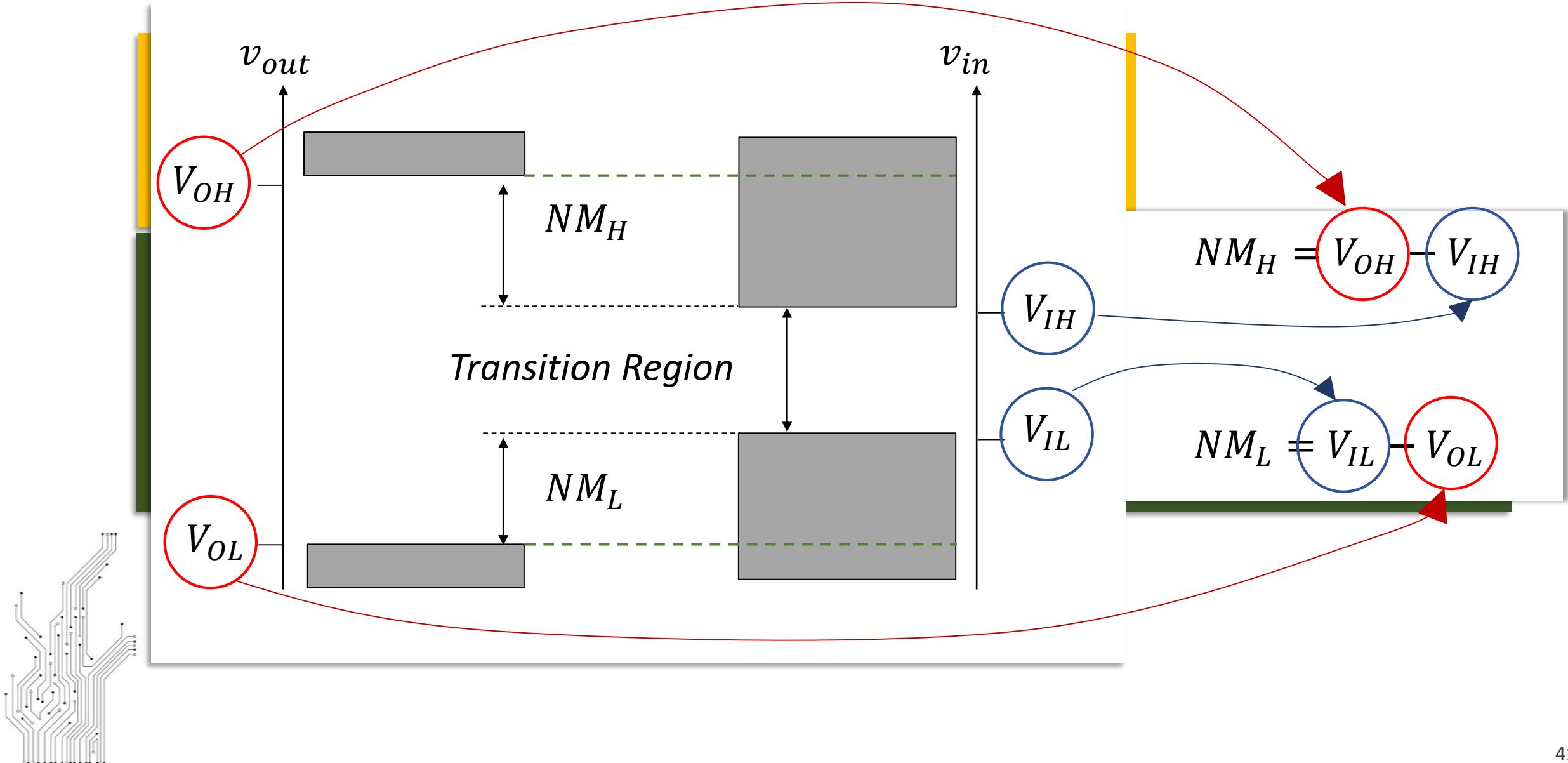
V_{IL} : Max v_{in} when I/P is '0'

V_{IH} : Min v_{in} when I/P is '1'

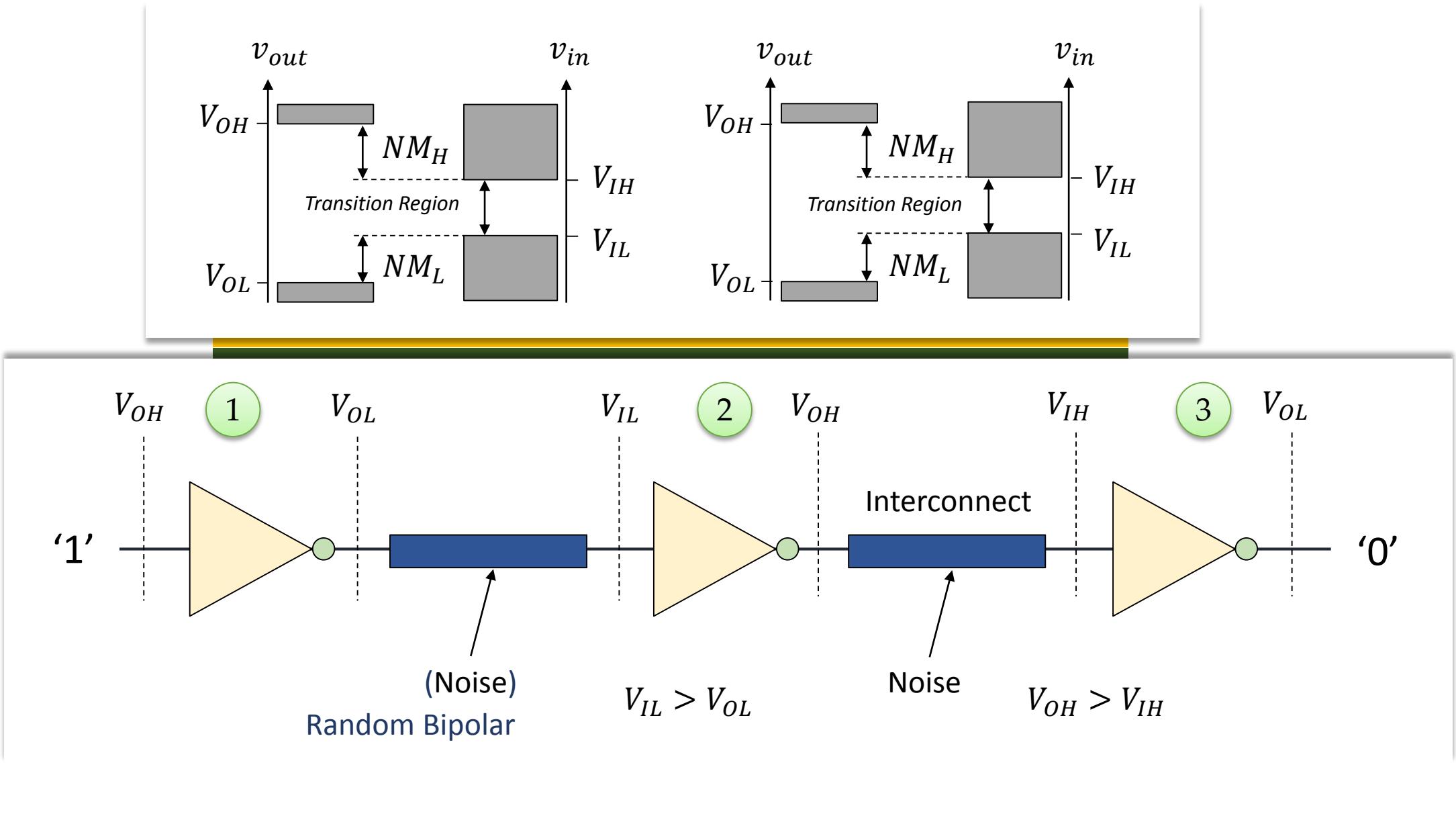
Symmetrical VTC = Matched inverter



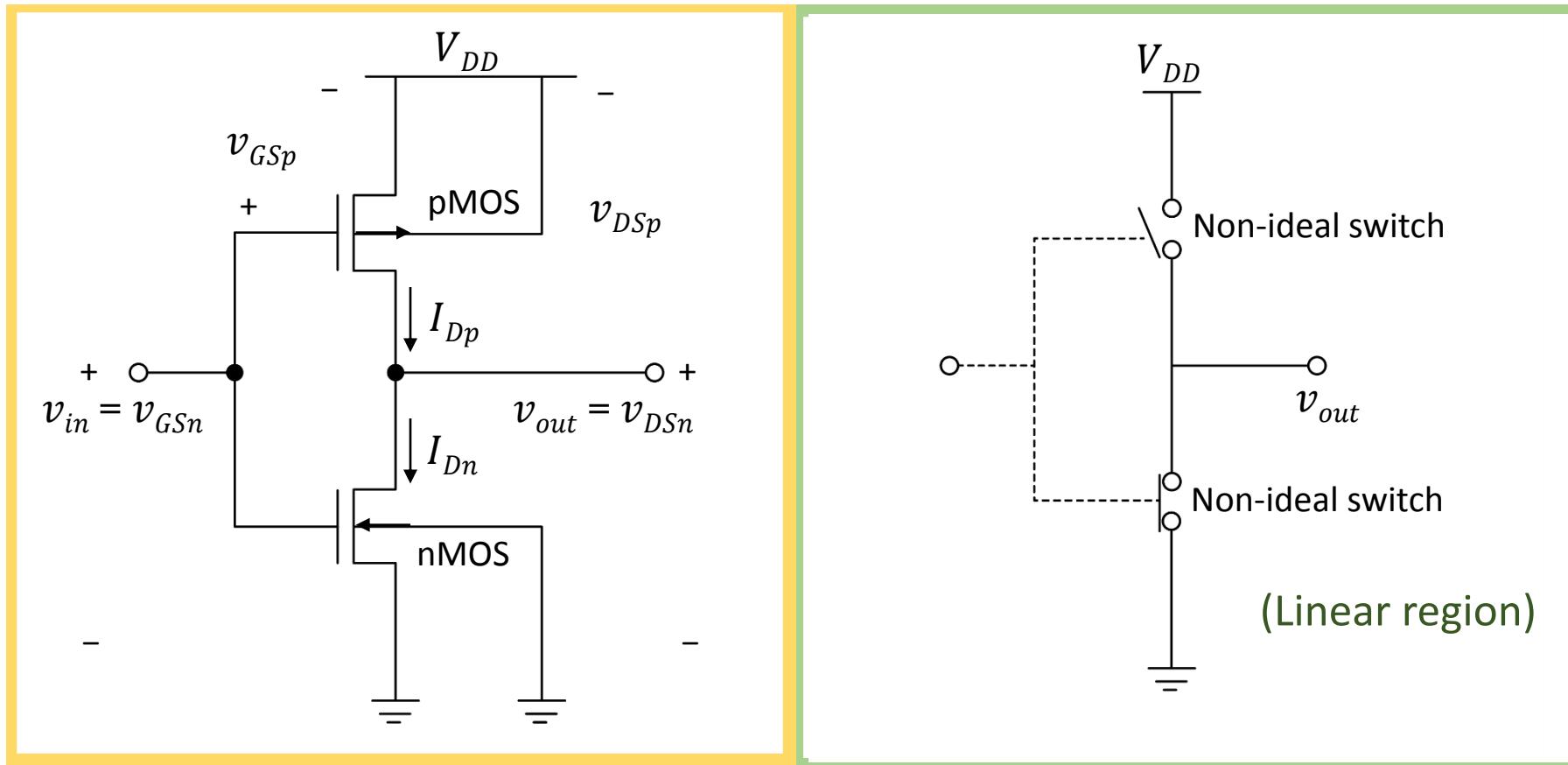
Noise Margins – Contd.



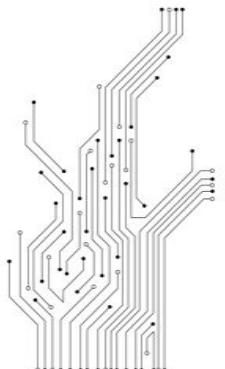
Noise Margins – Contd.



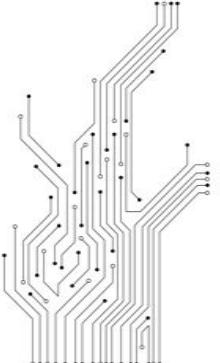
CMOS Inverter Circuit



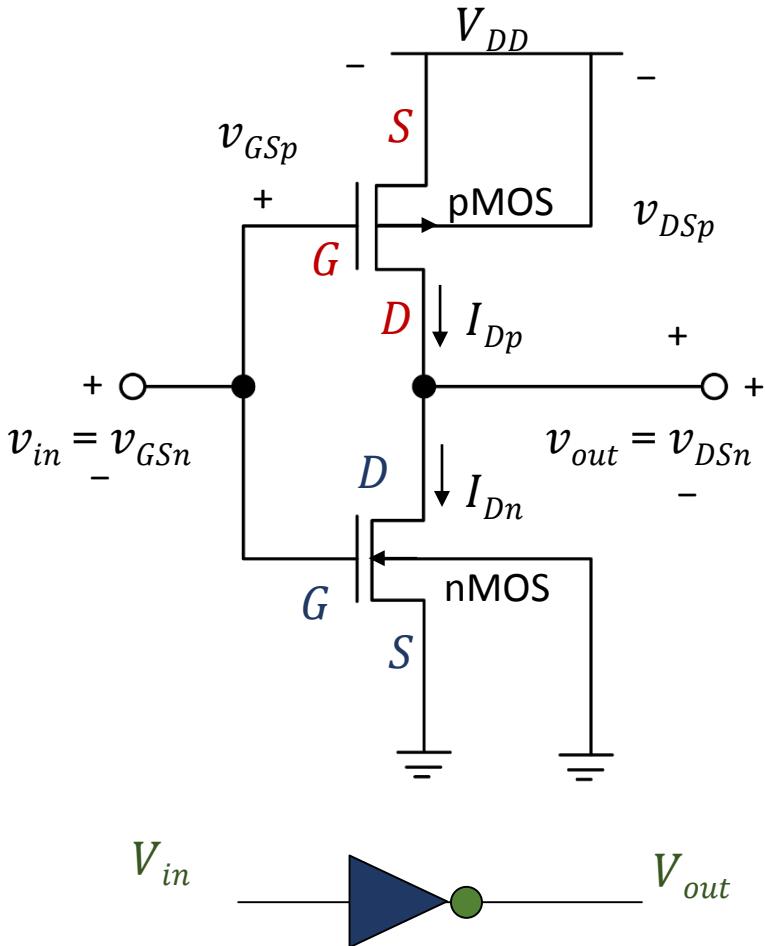
$P_{DC} = 0$ (ideal condition) and VTC resembles an ideal inverter.



CMOS Inverter Circuit



$$|v_{GS}| > |V_{to}|$$



$$|v_{DSp}| + v_{DSn} = V_{DD}$$

$$v_{GSn} = v_{in} \quad v_{GSp} = -(V_{DD} - v_{in})$$

$$v_{DSn} = v_{out} \quad v_{DSP} = -(V_{DD} - v_{out})$$

$$v_{in} < V_{tn} \quad I_{Dn} = I_{Dp} = 0$$

$$v_{out} = V_{OH} = V_{DD}$$

(nMOS – Cut-off, pMOS – Linear)

Logic 1

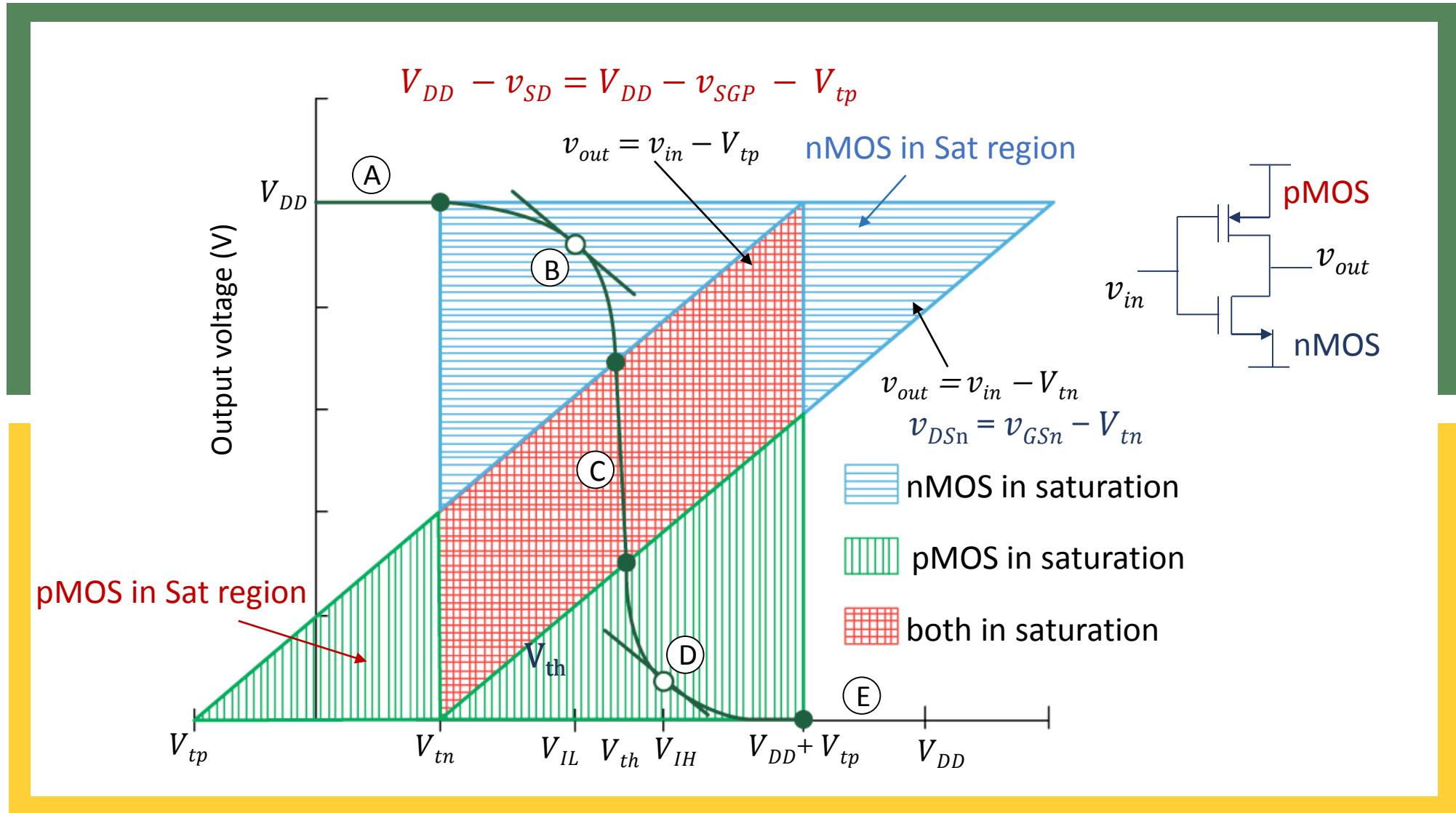
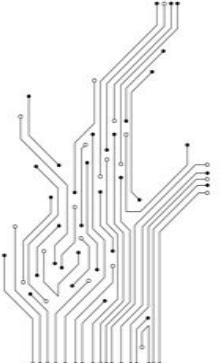
$$v_{out} = V_{OL} = 0$$

$$v_{in} > V_{DD} + V_{tp} \quad I_{Dn} = I_{Dp} = 0$$

(nMOS – Linear, pMOS – Cut-off)

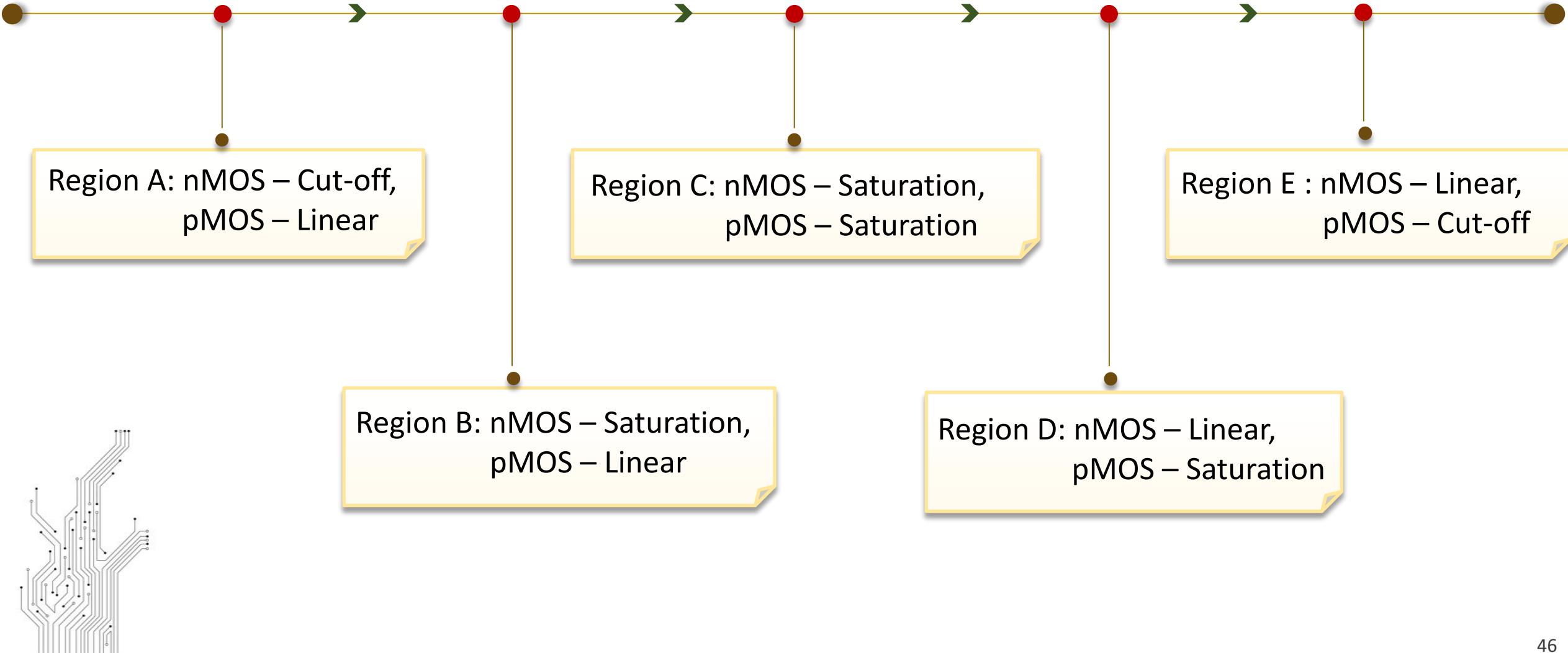
Logic 0

CMOS Inverter Circuit – VTC



CMOS Inverter Circuit – VTC

Five Operation Regions in Voltage Transfer Characteristic (VTC)



Derivation of V_{IL}

Region B: nMOS SAT & pMOS LIN

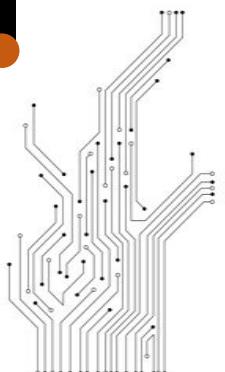
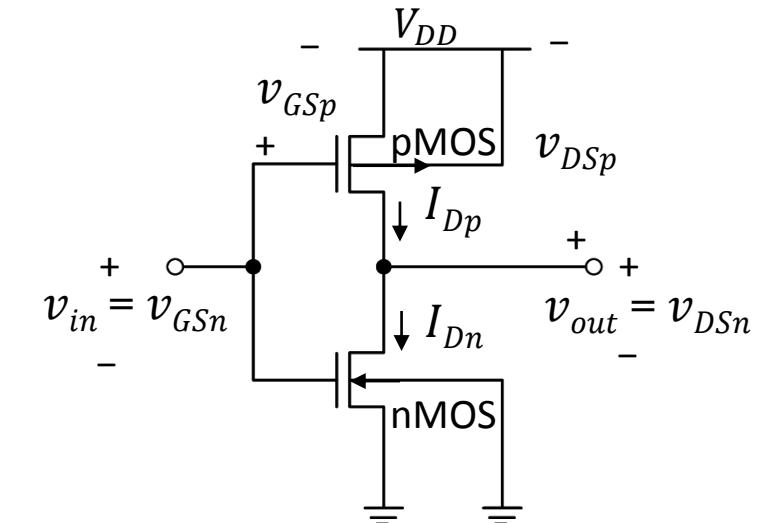
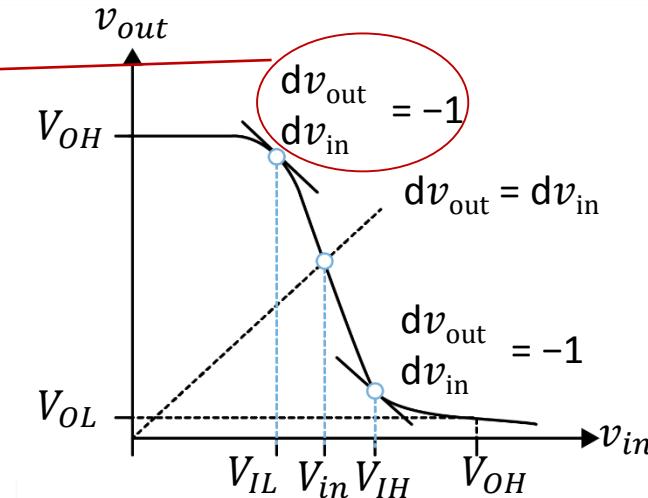
$$\frac{k_n}{2}(v_{GSn} - V_{tn})^2 = k_p \left[(v_{GSp} - V_{tp}) * v_{DSP} - \frac{1}{2}(v_{DSP})^2 \right]$$

v_{in} $-(V_{DD} - v_{in})$ $-(V_{DD} - v_{out})$

Differentiate w.r.t. v_{in} and equating $\frac{d v_{out}}{d v_{in}}$ to -1 :

$$v_{in} = V_{IL} = \frac{2v_{out} + V_{tp} - V_{DD} + k_R V_{tn}}{1 + k_R}$$

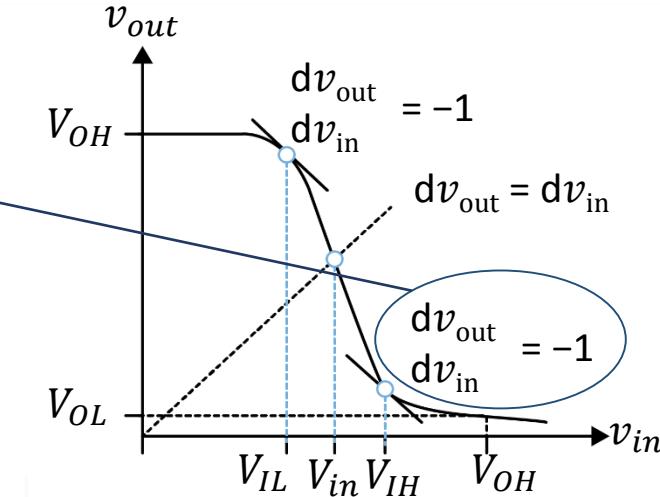
$$\text{where } k_R = \frac{k_n}{k_p}$$



Derivation of V_{IH}

Region D: nMOS LIN & pMOS SAT

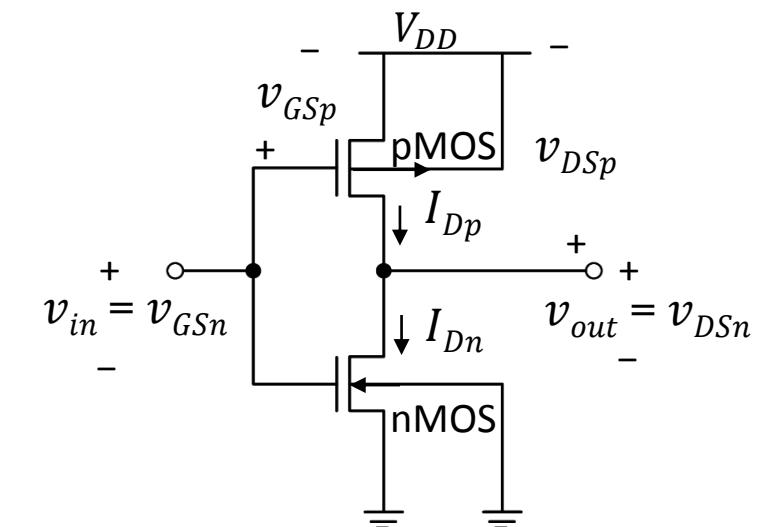
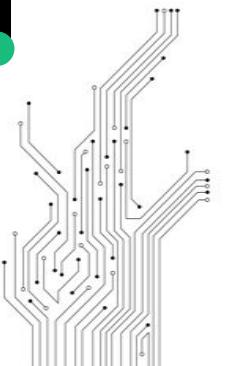
$$k_n \left[(v_{GSn} - V_{tn}) * v_{DSn} - \frac{1}{2} (v_{DSn})^2 \right] = \frac{k_p}{2} * (v_{GSp} - V_{tp})^2 - (V_{DD} - V_{in})$$



Differentiate w.r.t. v_{in} and equating $\frac{dv_{out}}{dv_{in}}$ to -1 :

$$v_{in} = V_{IH} = \frac{V_{DD} + V_{tp} + k_R(2v_{out} + V_{tn})}{1 + k_R}$$

$$\text{where } k_R = \frac{k_n}{k_p}$$



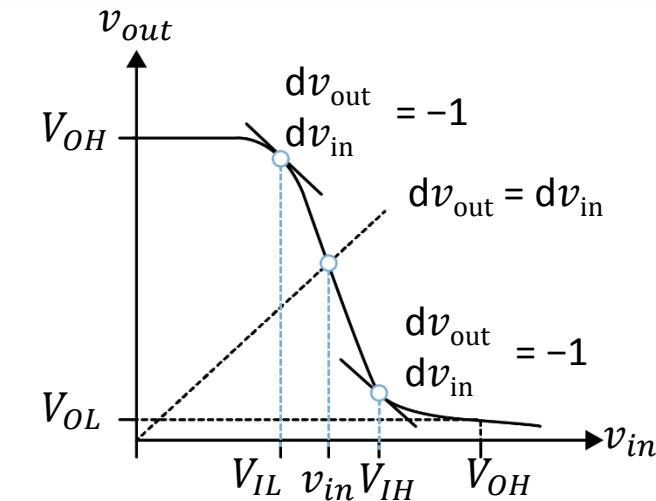
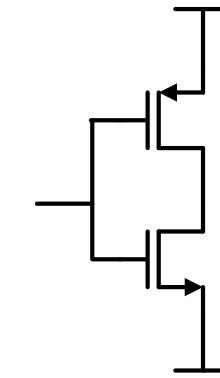
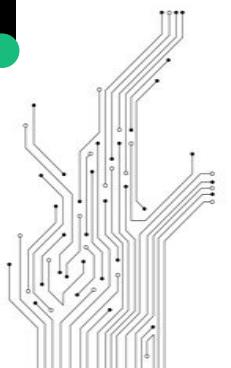
Derivation of V_{IH}

Region D: nMOS LINEAR & pMOS SATURATION

$$k_n \left[(v_{GSn} - V_{tn}) * v_{DSn} - \frac{1}{2} (v_{DSn})^2 \right] = \frac{k_p}{2} * (v_{GSp} - V_{tp})^2 - (V_{DD} - v_{in})$$

↑ v_{in} ↑ v_{out} ↑ $(V_{DD} - v_{in})$

or $V_{IH} = \frac{V_{DD} + V_{tp} + k_R(2v_{out} + v_{tn})}{1 + k_R}$ where $k_R = \frac{k_n}{k_p}$



Calculation of V_{th}

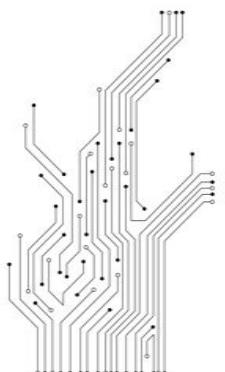
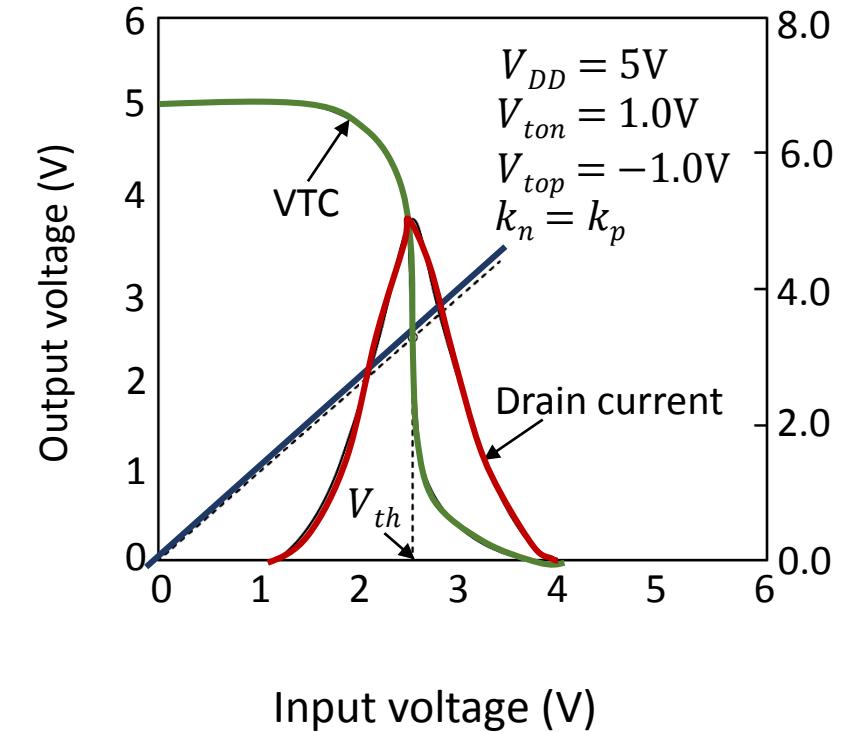
$$V_{th} = v_{in} = v_{out}$$

Region C: nMOS SAT & pMOS SAT

$$\frac{k_n}{2} (v_{GSn} - V_{tn})^2 = \frac{k_p}{2} (v_{GSp} - V_{tp})^2$$

$\uparrow I_{DN}$
 $\uparrow V_{in}$
 $\uparrow I_{DP}$
 $-(V_{DD} - V_{in})$

$$V_{in} = V_{th} = \frac{V_{tn} + \sqrt{\frac{1}{k_R}(V_{DD} + V_{tp})}}{1 + \sqrt{\frac{1}{k_R}}}$$



Design of CMOS Inverters

Aim: to achieve $V_{th} = \frac{V_{DD}}{2}$ ← **Normal condition**

From V_{th} equation, the required K_R is:

$$k_R = \frac{k_n}{k_p} = \left(\frac{V_{DD} + V_{tp} - V_{th}}{V_{th} - V_{tn}} \right)^2$$

If $V_{th} = \frac{V_{DD}}{2}$, $V_{tn} = |V_{tp}|$ and

C_{ox} are the same for nMOS and pMOS,

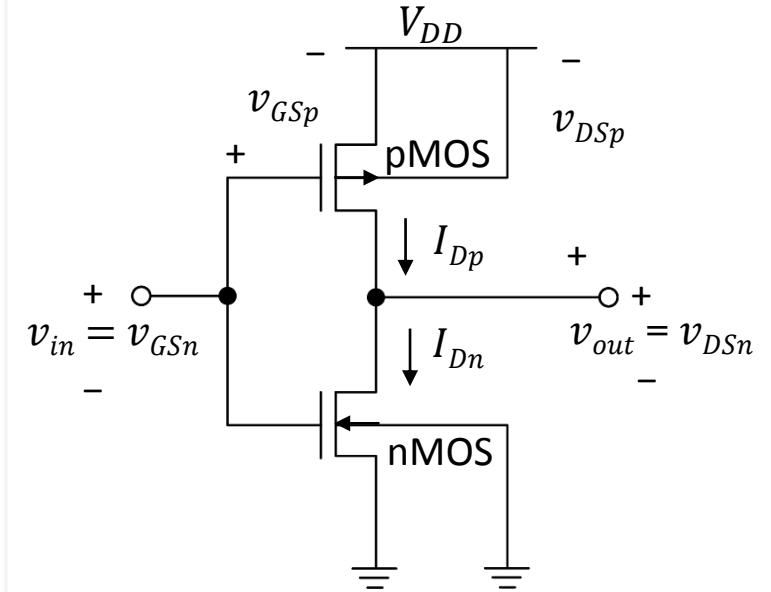
⇒ $k_n = k_p$ for symmetric inverter

$$\frac{k_n}{k_p} = \frac{\mu_n \left(\frac{W}{L}\right)_n}{\mu_p \left(\frac{W}{L}\right)_p} = 1$$

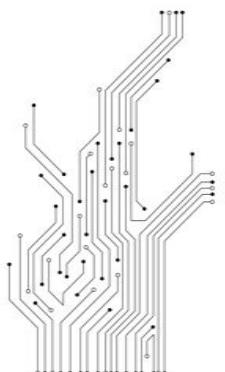
Mobility of electron

For typical process, $\mu_n = 2.5\mu_p$, hence, $\left(\frac{W}{L}\right)_p \approx 2.5 \left(\frac{W}{L}\right)_n$

Mobility of hole



Electrons travel 2.5 times faster than holes



Example

Calculate NM for the following CMOS inverter.

$$V_{DD} = 3.3V, k_n = 200\mu A/V^2, k_p = 80\mu A/V^2$$

$$V_{tn} = 0.6 V, V_{tp} = -0.7 V$$

$$V_{IL} = \frac{2V_{out} + V_{tp} - V_{DD} + k_R V_{tn}}{1 + k_R} = 0.57v_{out} - 0.71$$

$$\text{But } \frac{k_n}{2} * (v_{GSn} - V_{tn})^2 = k_p \left[(v_{GSp} - V_{tp}) \times v_{DSP} - \frac{1}{2}(v_{DSP})^2 \right]$$

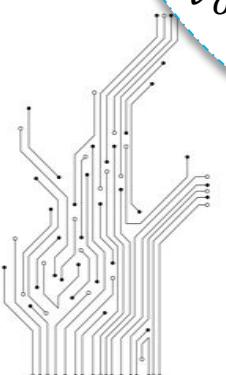
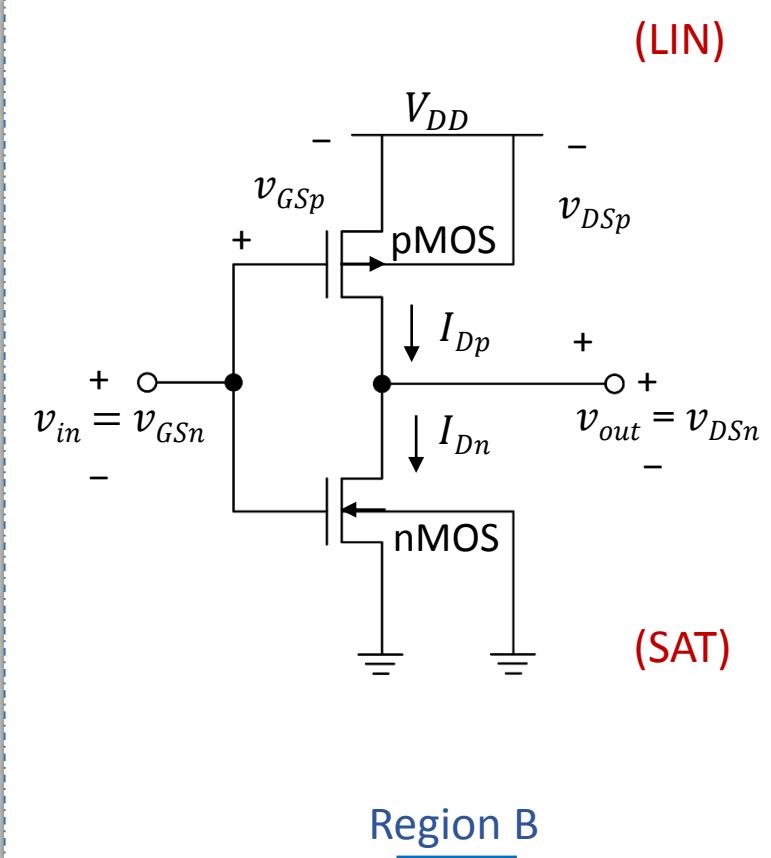
nMOS (SAT) pMOS (LIN)

$$\text{where } v_{GSn} = V_{IL}, v_{GSp} = V_{IL} - V_{DD}, v_{DSP} = v_{out} - V_{DD}$$

$$v_{out} = 3.14 V \text{ or } V_{IL} = 1.08 V$$

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$



Example (Contd.)

Similarly,

$$V_{IH} = \frac{V_{DD} + V_{tp} + k_R(2v_{out} + V_{tn})}{1 + k_R} = 1.43v_{out} + 1.17$$

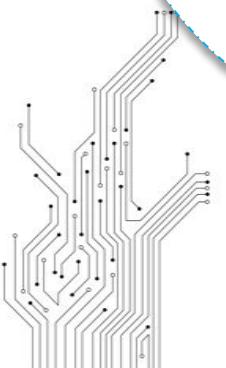
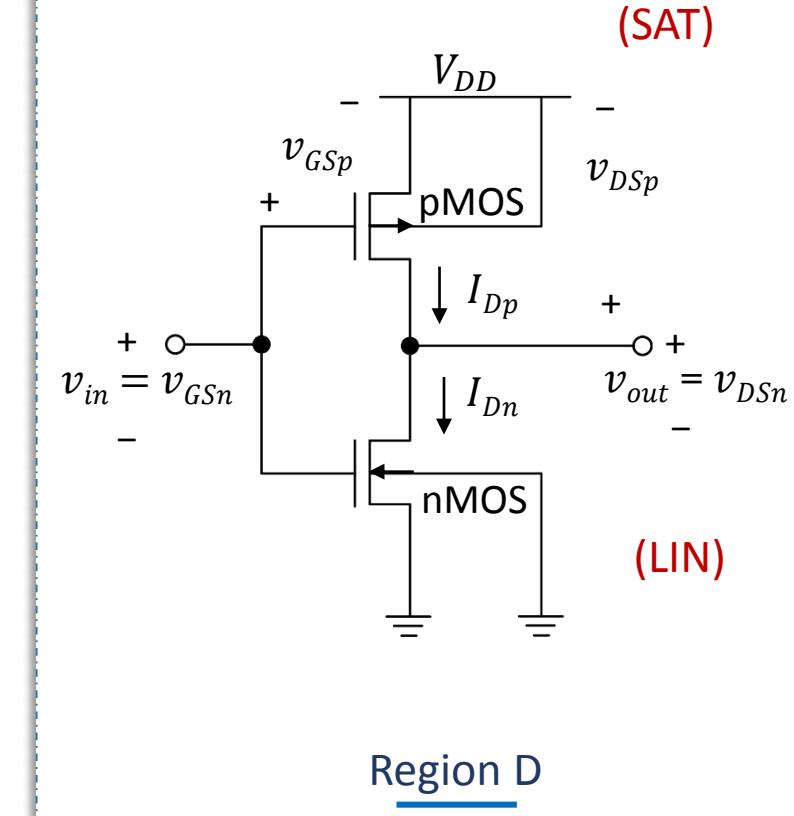
$$\text{and } k_n \left[(v_{GSn} - V_{tn}) * v_{DSn} - \frac{1}{2}(v_{DSn})^2 \right] = \frac{k_p}{2} * (v_{GSp} - V_{tp})^2$$

where $v_{GSn} = V_{IH}$, $v_{DSn} = v_{out}$, $v_{GSp} = V_{IH} - V_{DD}$

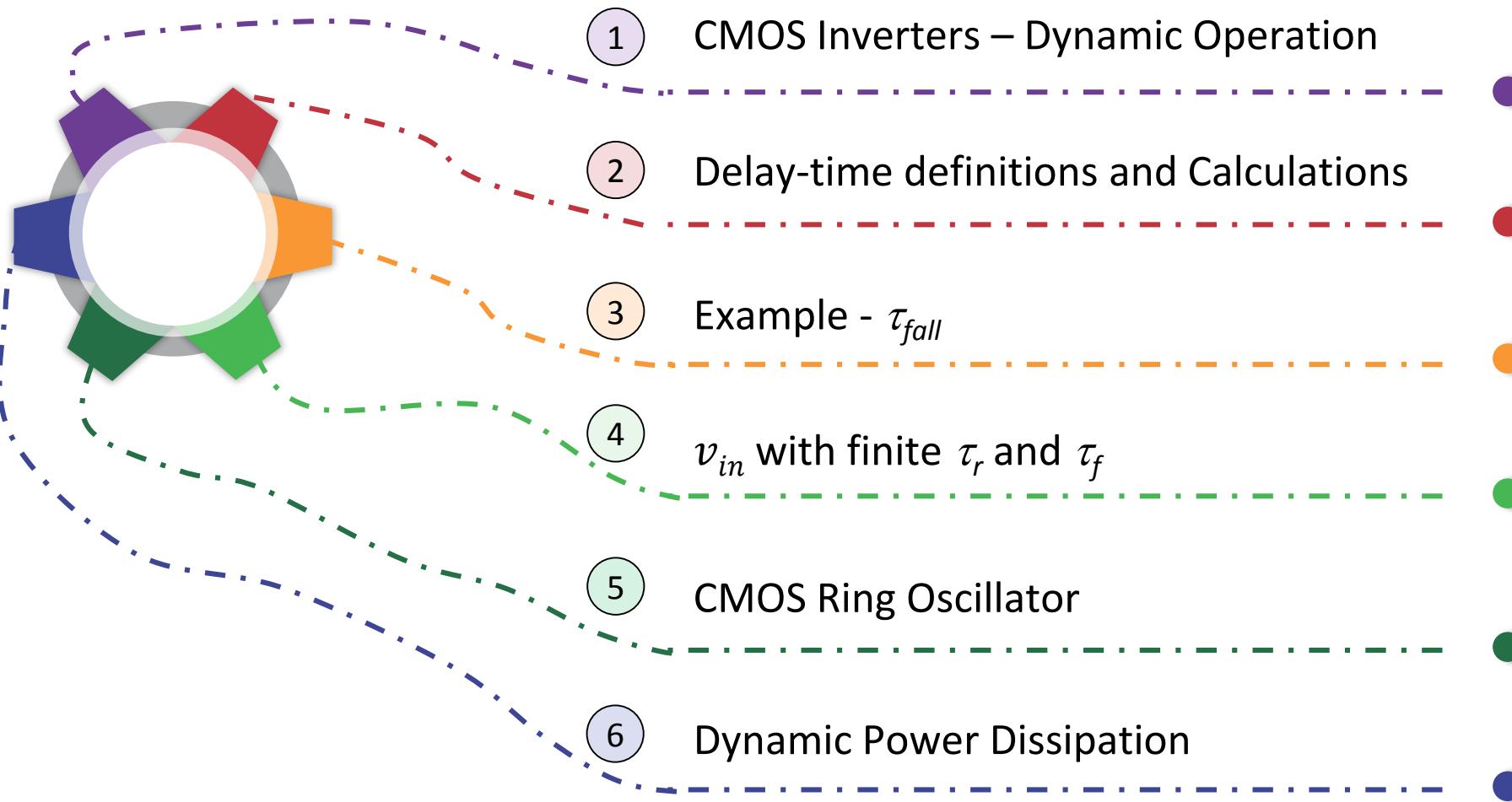
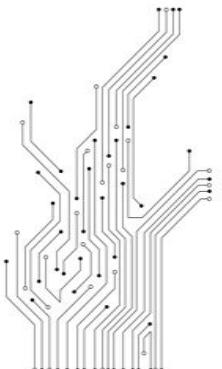
$$\Rightarrow v_{out} = 0.27 \text{ V or } V_{IH} = 1.55 \text{ V}$$

$$\left. \begin{array}{l} NM_L = V_{IL} - V_{OL} = 1.08 \text{ V} \\ NM_H = V_{OH} - V_{IH} = 1.75 \text{ V} \end{array} \right\} NM = 1.08 \text{ V}$$

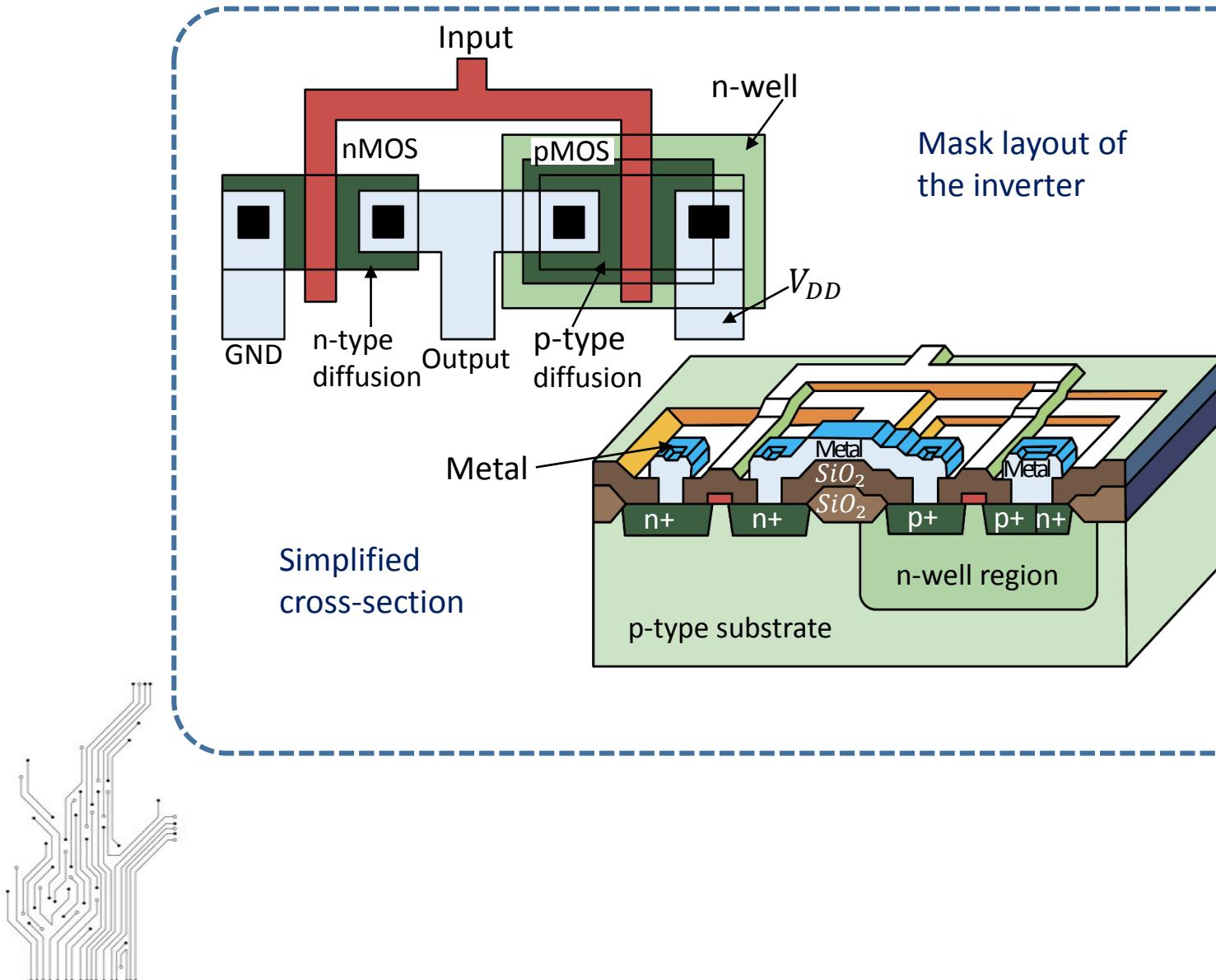
3.3V



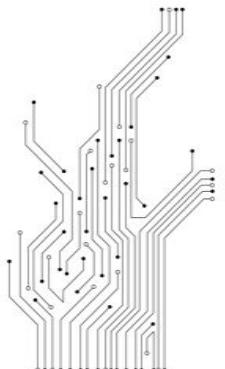
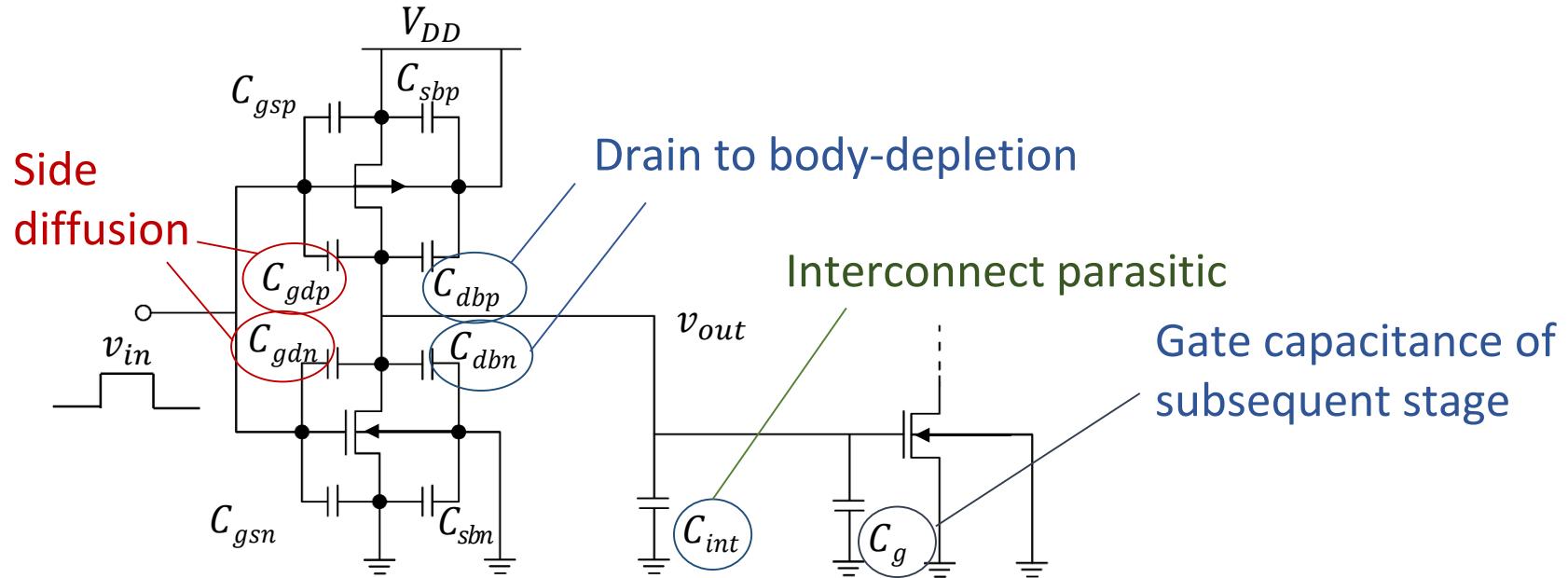
Switching Characteristics



CMOS Inverter Layout (Contd.)



CMOS Inverters – Dynamic Operation

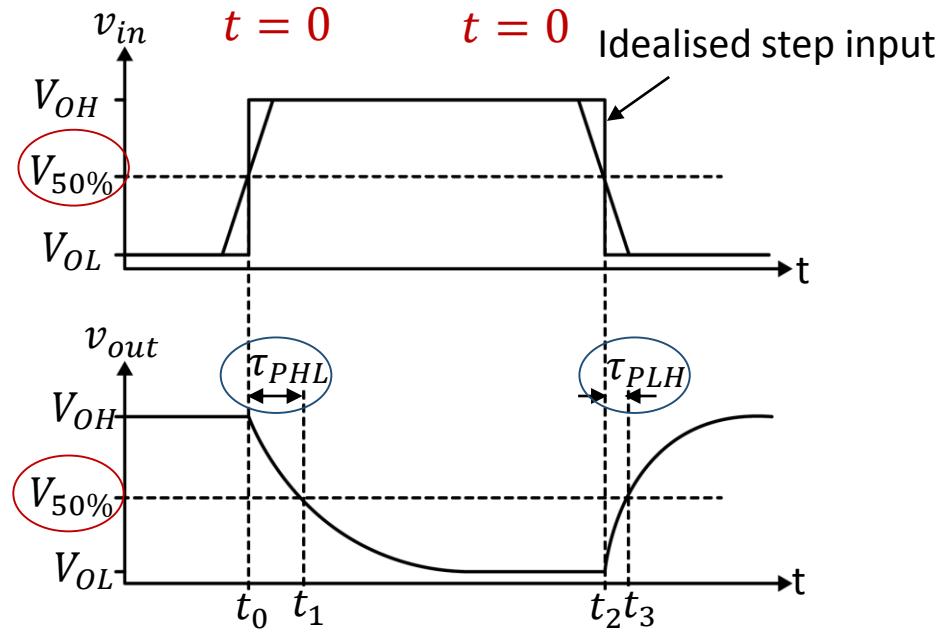


Parasitic Capacitance

$$C_{load} = C_{gdn} + C_{gdp} + C_{dbn} + C_{dbp} + C_{int} + C_g$$

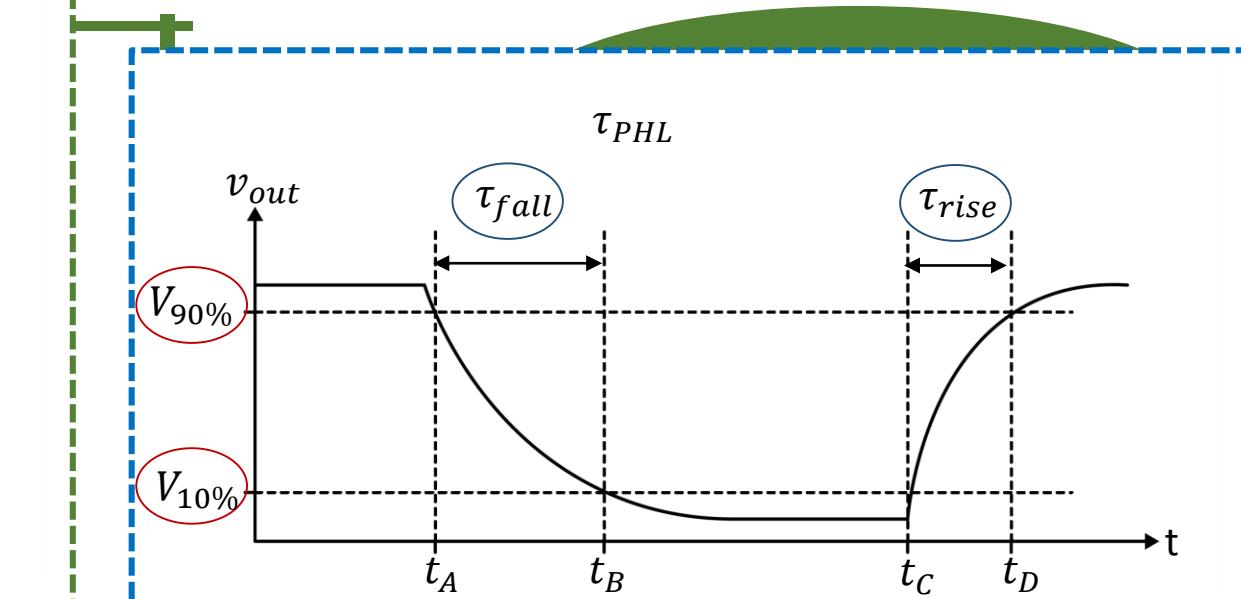
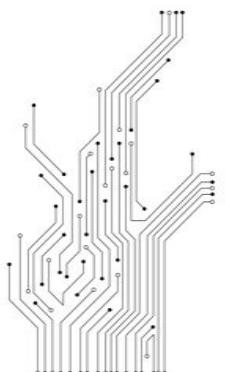
Delay-time Definitions

τ_P



$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH})$$

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$



$$V_{10\%} = V_{OL} + 0.1(V_{OH} - V_{OL})$$

$$V_{90\%} = V_{OL} + 0.9(V_{OH} - V_{OL})$$

Calculation of Delay Times – 1st Order

$$\tau_{PLH} = \frac{C_{load} \times \Delta V_{LH}}{I_{avg}|_{LH}} = \frac{C_{load} \times (V_{50\%} - V_{OL})}{I_{avg}|_{LH}}$$

$$\tau_{PHL} = \frac{C_{load} \times \Delta V_{HL}}{I_{avg}|_{HL}} = \frac{C_{load} \times (V_{OH} - V_{50\%})}{I_{avg}|_{HL}}$$

$$I_{avg}|_{HL} = \frac{1}{2} [I|_{V_{OH}} + I|_{V_{50\%}}]$$

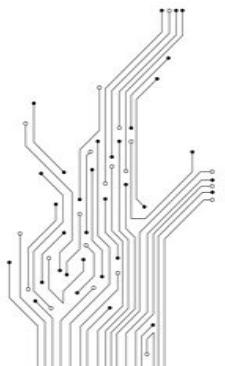
$$I_{avg}|_{LH} = \frac{1}{2} [I|_{V_{50\%}} + I|_{V_{OL}}]$$

$$\frac{dQ}{dt} \times t$$

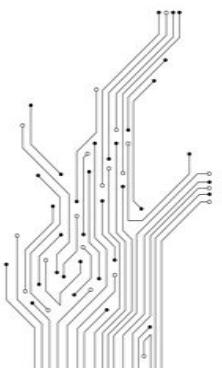
$$Q = C\Delta V = I * t$$

Therefore:

$$t = C\Delta V/I$$



Example - τ_{fall}

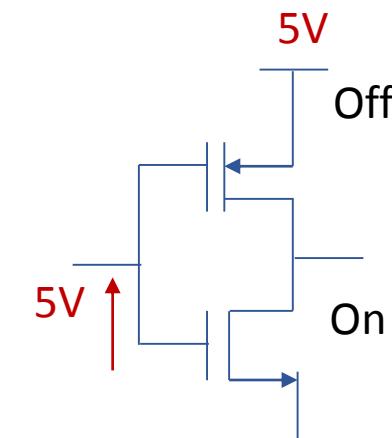


$$t = \frac{C \Delta V}{i}$$

Given: $V_{DD} = 5$ V, $V|_{90\%} = 4.5$ V, $V|_{10\%} = 0.5$ V, $C_{load} = 1$ pF, $\mu_n C_{ox} = 20 \mu \frac{A}{V}$, $(W/L)|_n = 10$ and $V_{tn} = 1$ V. Determine the τ_{fall} of the CMOS INVERTER.

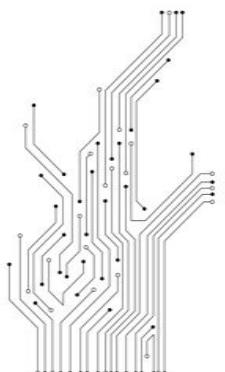
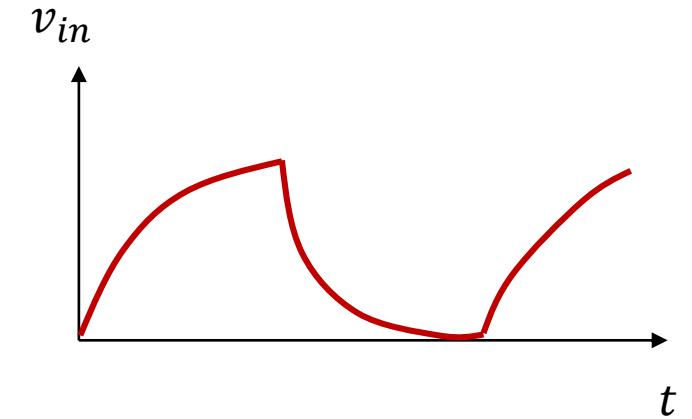
$$\begin{aligned} I_{avg} &= \frac{1}{2} (I|_{V_O=90\%}^{\text{pMOS OFF}} + I|_{V_O=10\%}^{\text{nMOS(SAT)}}) \\ &= \frac{1}{2} \left[\frac{1}{2} k_n (v_{in} - V_{tn})^2 + k_n \left((v_{in} - V_{tn}) v_{out} - \frac{1}{2} v_{out}^2 \right) \right] \\ &= 9.875 \times 10^{-4} \text{ A} \end{aligned}$$

$$\tau_{fall} = \frac{C_{load} * \Delta V}{I_{avg}} = 4.05 \text{ ns}$$

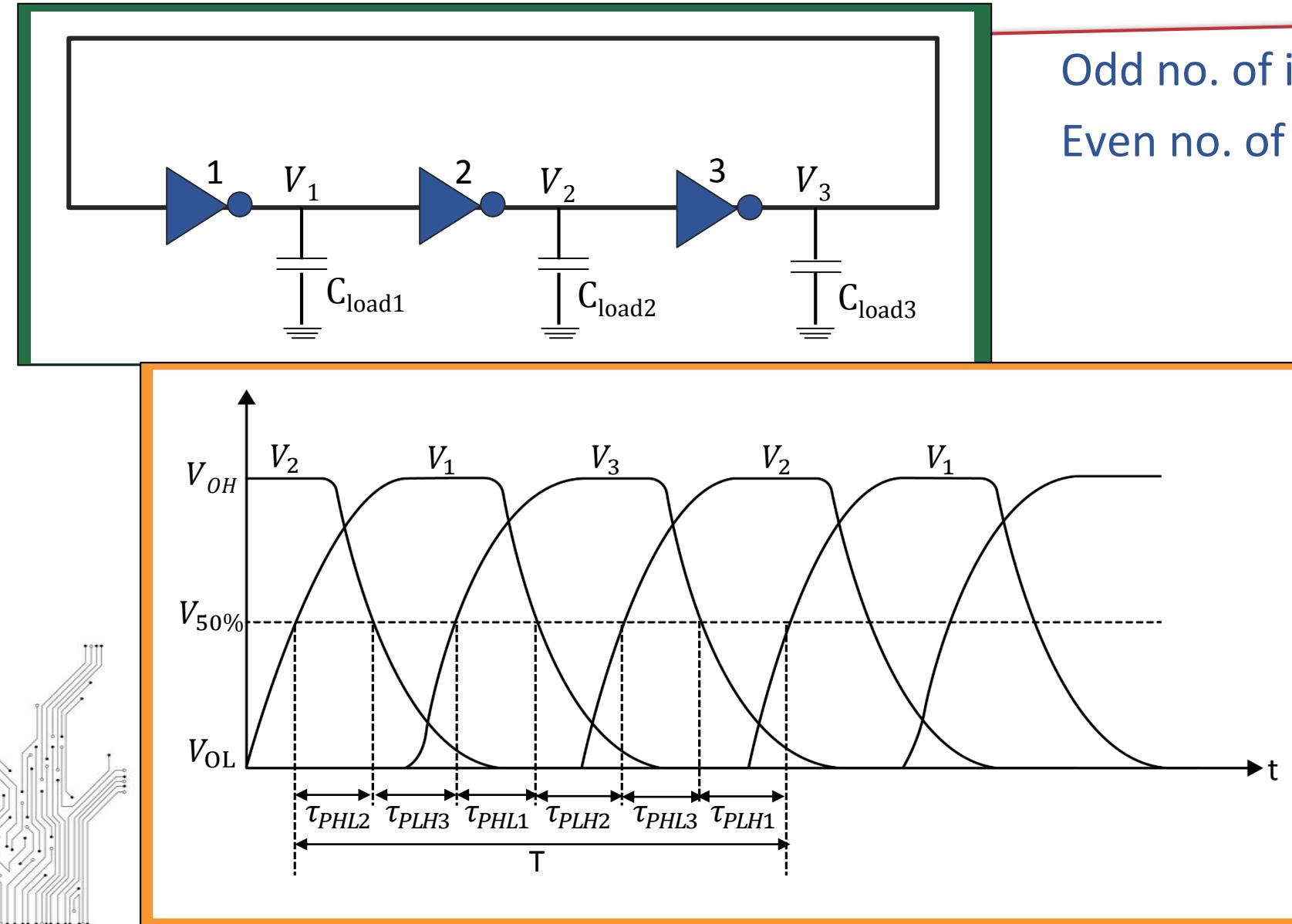


v_{in} with Finite τ_r and τ_f

$$\tau_{PHL(actual)} = \sqrt{\tau_{PHL}^2(\text{step input}) + \left(\frac{\tau_r}{2}\right)^2}$$
$$\tau_{PLH(actual)} = \sqrt{\tau_{PHL}^2(\text{step input}) + \left(\frac{\tau_f}{2}\right)^2}$$



CMOS Ring Oscillator



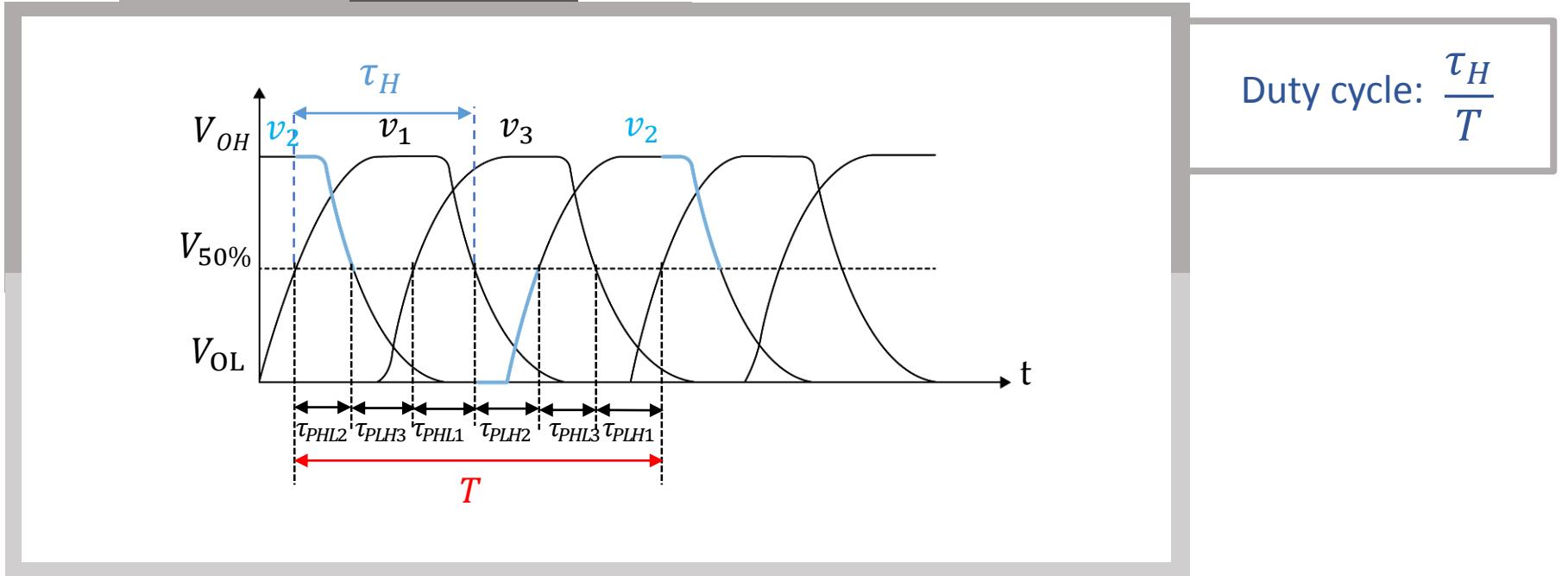
Odd no. of inverters: Oscillator
Even no. of inverters: Latch

V_{O1} : $V_{10L} \Rightarrow V_{10H}$
↓
 $V_{20H} \Rightarrow V_{20L}$
↓
 $V_{30L} \Rightarrow V_{30H}$
↓
 $V_{10H} \Rightarrow V_{10L}$
↓

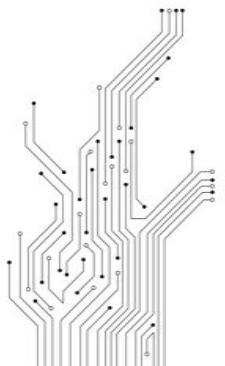
CMOS Ring Oscillator

Assuming identical INV and all C_{load} is the same:

$$T = \tau_{PHL1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH3} = 6\tau_p$$



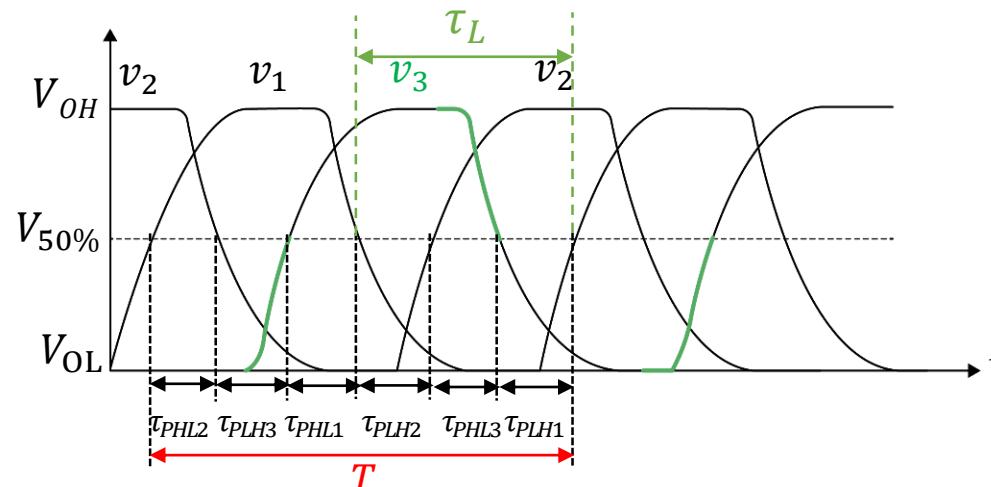
$$\text{or } f = \frac{1}{T} = \frac{1}{2 n \tau_p} \text{ where } n \text{ is the number of inverters}$$



CMOS Ring Oscillator

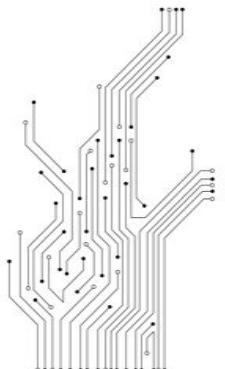
Assuming identical INV and all C_{load} is the same:

$$T = \tau_{PHL1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH3} = 6\tau_p$$



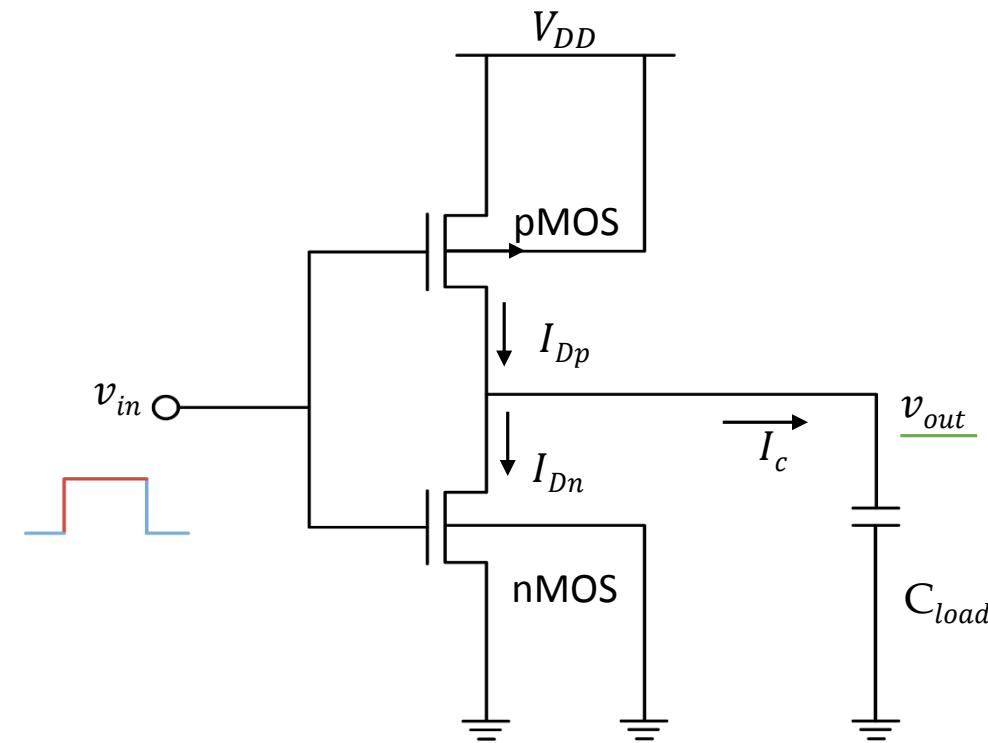
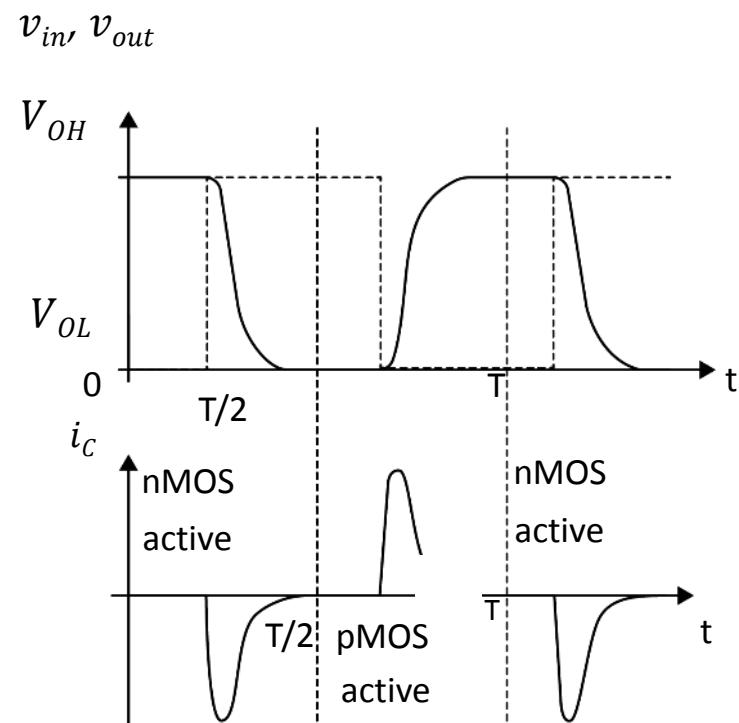
Duty cycle: $\frac{\tau_H}{T}$

or $f = \frac{1}{T} = \frac{1}{2 n \tau_p}$ where n is the number of inverters

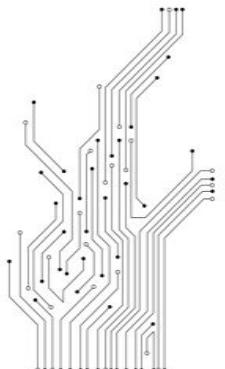


Dynamic Power Dissipation

0 \leftrightarrow 1

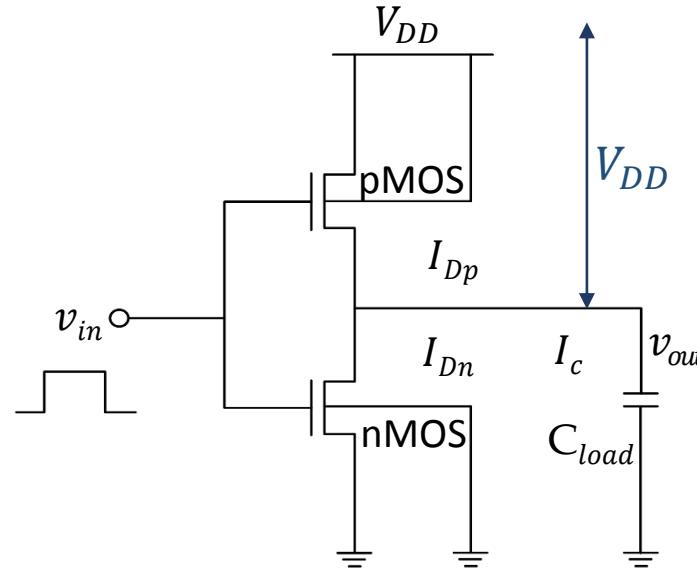
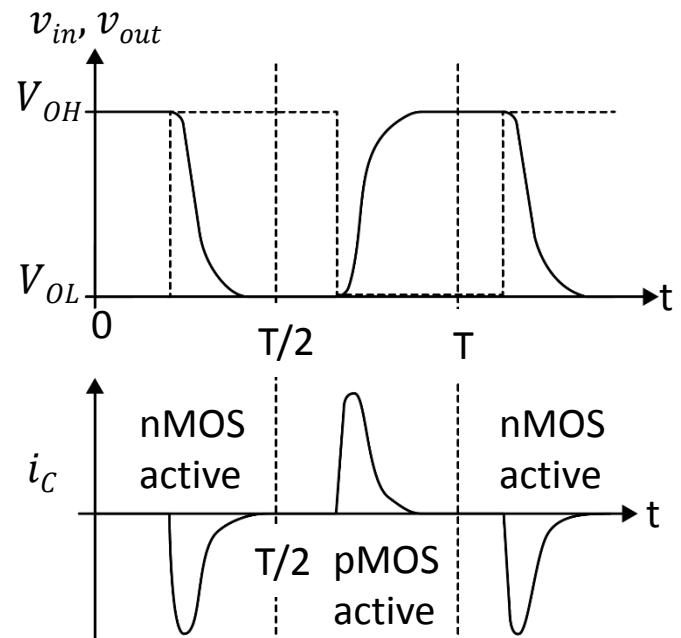


$$P_{avg} = \frac{1}{T} \int_0^T v(t) * i(t) dt$$



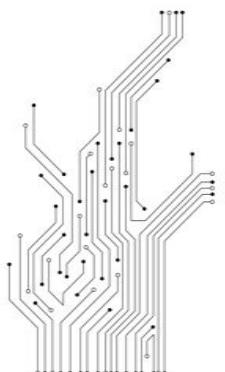
Dynamic Power Dissipation – Contd.

$$P = VI$$

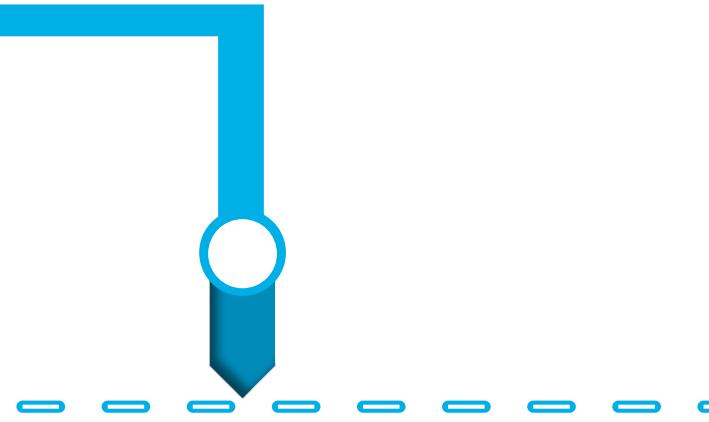
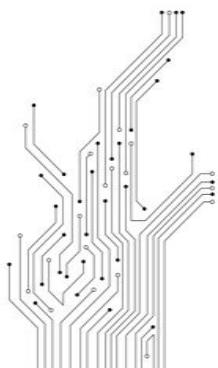


$$\begin{aligned} Q &= CV \\ &= It \\ I &= \frac{CdV}{dt} \end{aligned}$$

$$\begin{aligned} P_{avg} &= \frac{1}{T} \left[\int_0^{\frac{T}{2}} v_{out} \left(-C_{load} \frac{dv_{out}}{dt} \right) dt + \int_{\frac{T}{2}}^T (V_{DD} - v_{out}) \left(C_{load} \frac{dv_{out}}{dt} \right) dt \right] \\ &= \frac{1}{T} \left[\left(-C_{load} \frac{v_{out}^2}{2} \right) \Big|_0^{\frac{T}{2}} + \left(V_{DD} * v_{out} * C_{load} - \frac{1}{2} C_{load} v_{out}^2 \right) \Big|_{\frac{T}{2}}^T \right] \\ &= \frac{1}{T} * C_{load} * V_{DD}^2 \text{ or } C_{load} * V_{DD}^2 * f \text{ when } \frac{1}{T} = f \end{aligned}$$



Power and Area



Power

$$P = P_S + P_D$$

Static: Due to leakage Current of Source and Drain junction.

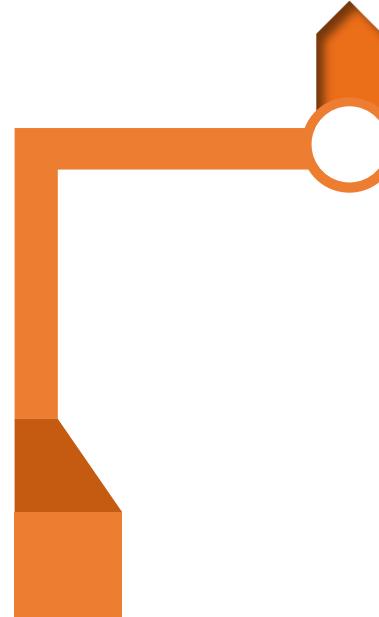
Dynamic: Significant amount of Current during switching event, i.e., during logic transition ' $0 \leftrightarrow 1$ ' and ' $1 \leftrightarrow 0$ '

Trade-off

Area consideration

$\left(\frac{W}{L}\right) I_{min} \Rightarrow \text{min area}$ but suffers from noise margins,

O/P Current Drive capability and dynamic switching speed. (**Fan-out**)



Logic Gates

01

Building blocks for digital circuits

02

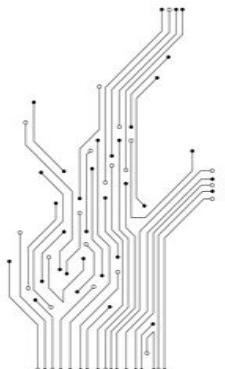
A logic gate comprises transistors

03

The transistors act as on-off switches

04

Logic gates perform logic or Boolean functions defined by **truth tables**
(Circuit design)



05

A logic or Boolean variable has only two values, 1 or 0

06

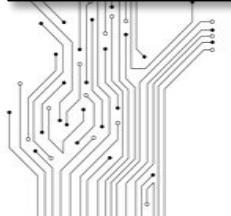
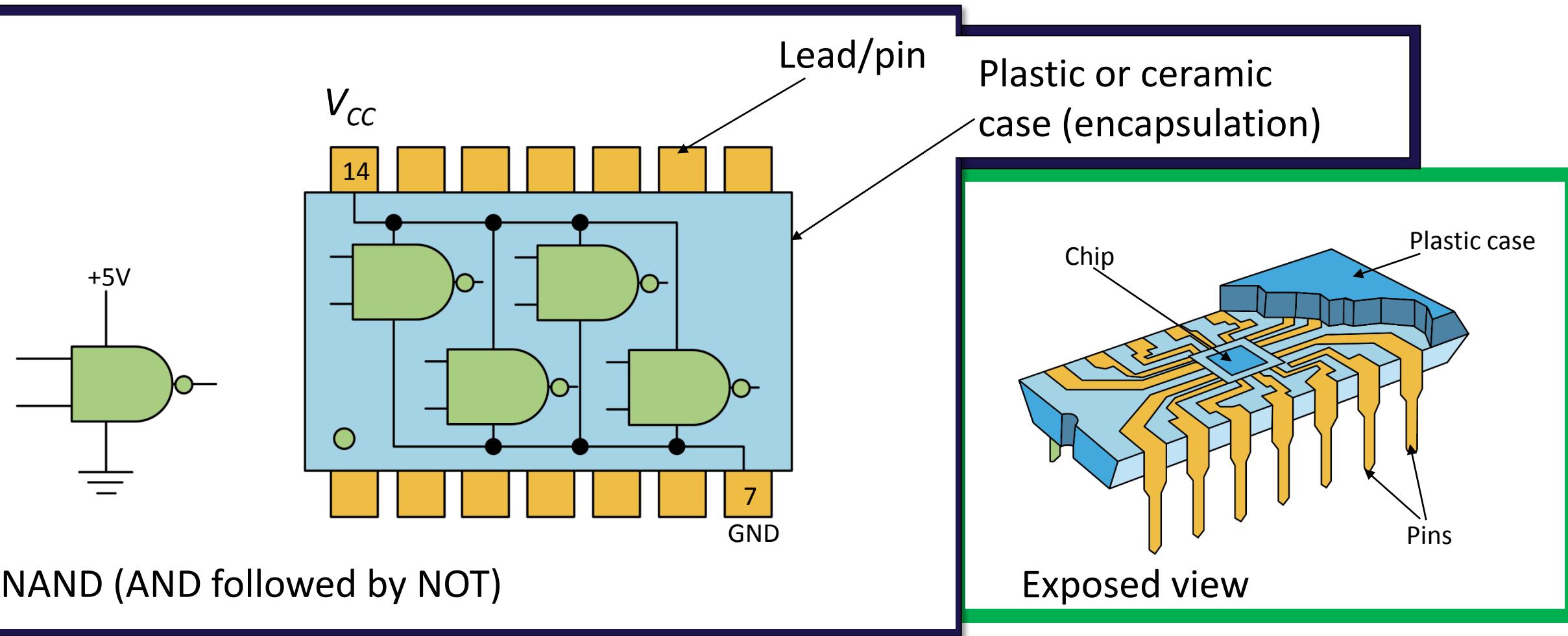
The 3 basic logic operators are **NOT**, **AND**, **OR**



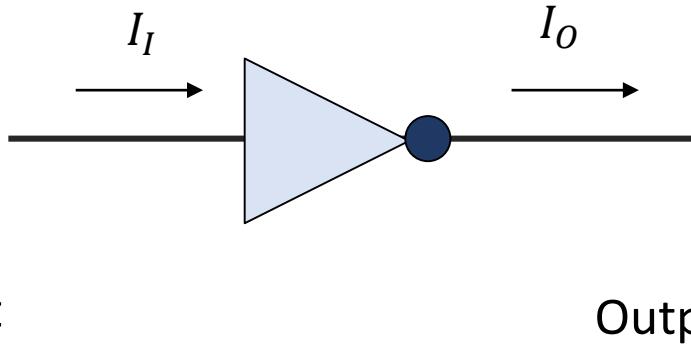
INV NAND NOR

Area: Equivalent number of NAND gates

Logic Gates in IC package



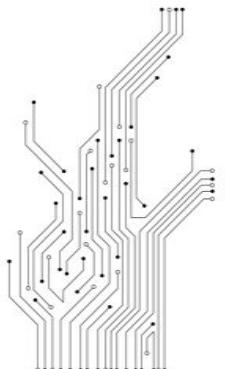
Defining Current Direction



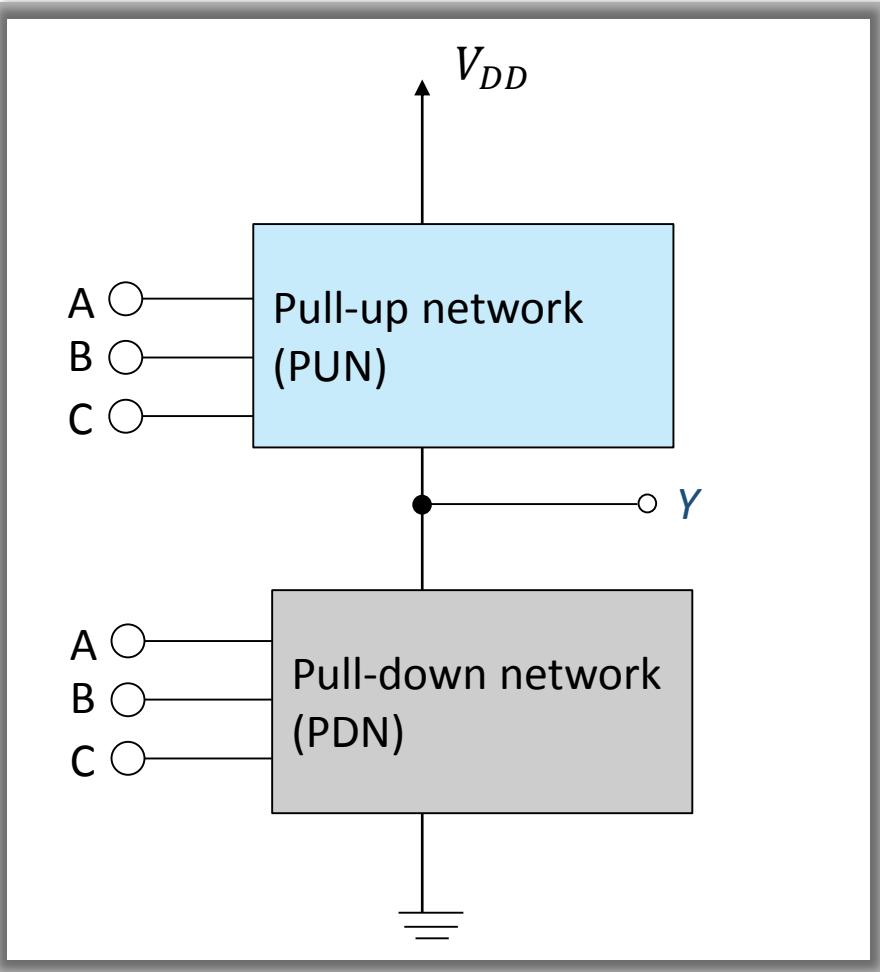
Current directions shown are defined as +ve (positive).

The gate **sinks** current if it flows into the i/p or o/p.

The gate **sources** current if it flows out of the i/p or o/p.

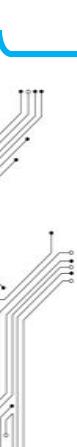
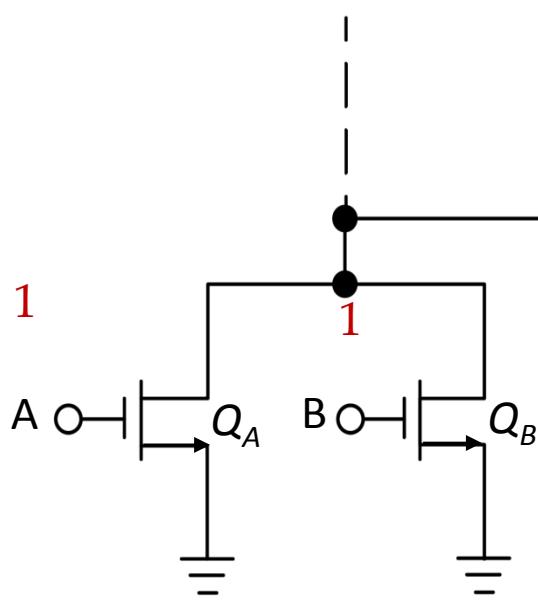


Combinational-logic Circuit



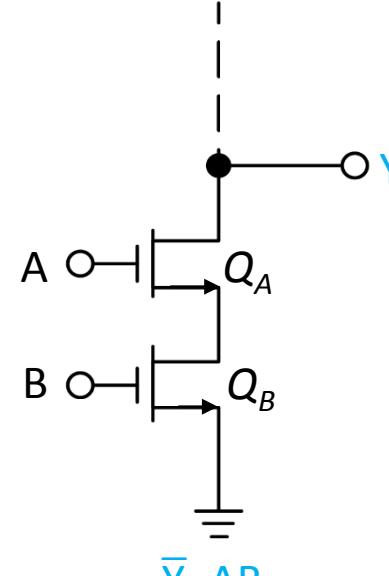
- CMOS Logic circuit is an extension of the CMOS inverter, it consists of 2 N/Ws.
- PDN are constructed of nMOS while PUN of pMOS.
- PDN will conduct for all I/P combinations that require a low O/P and will pull O/P to ground while PUN is OFF.

Examples: PDN and PUN

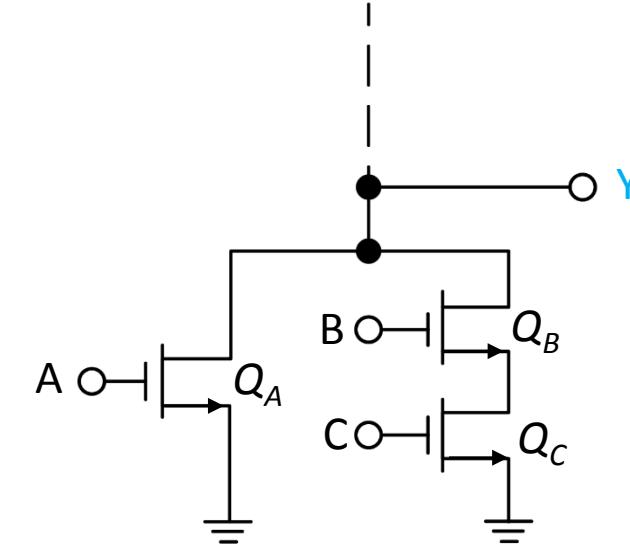


(a)

Parallel: OR
Series: AND

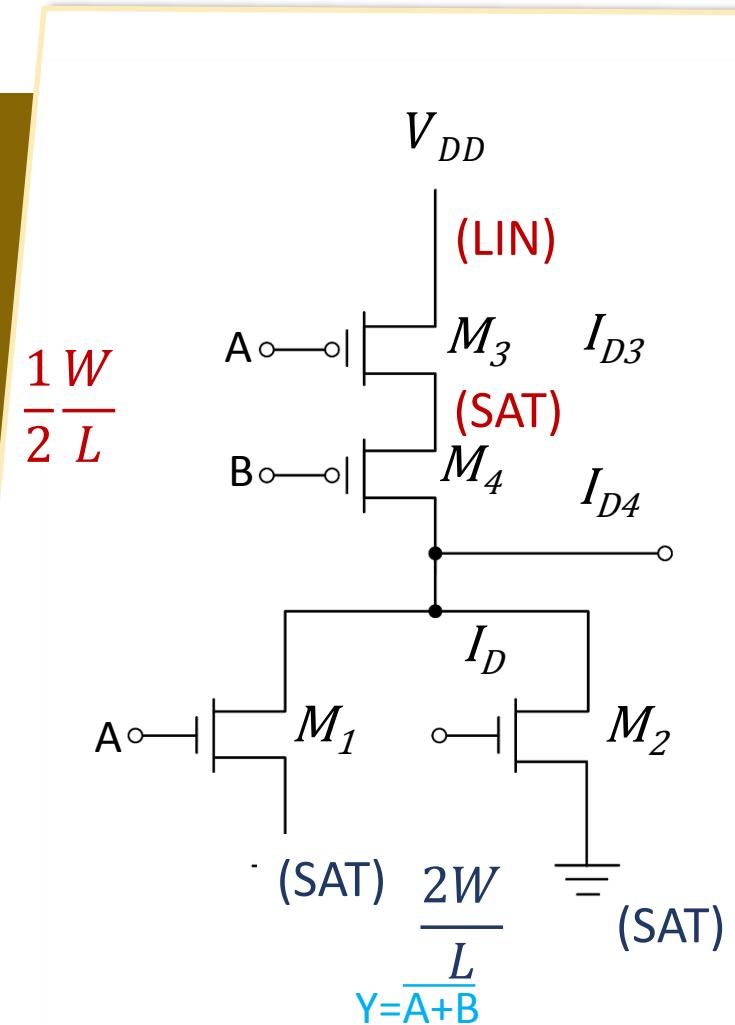
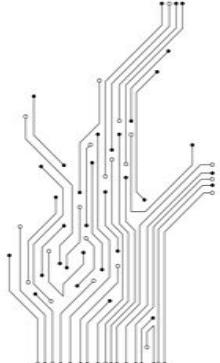


(b)



(c)

Circuit Design of NOR2



Assume: V_A, V_B switch simultaneously :

$$(W/L)_{M1} = (W/L)_{M2}; (W/L)_{M3} = (W/L)_{M4}$$

$$I_D = k_n(V_{th} - V_{tn})^2 \Rightarrow V_{th} = V_{tn} + \sqrt{\frac{I_D}{k_n}} \quad (\text{SAT}) - \text{nMOS}$$

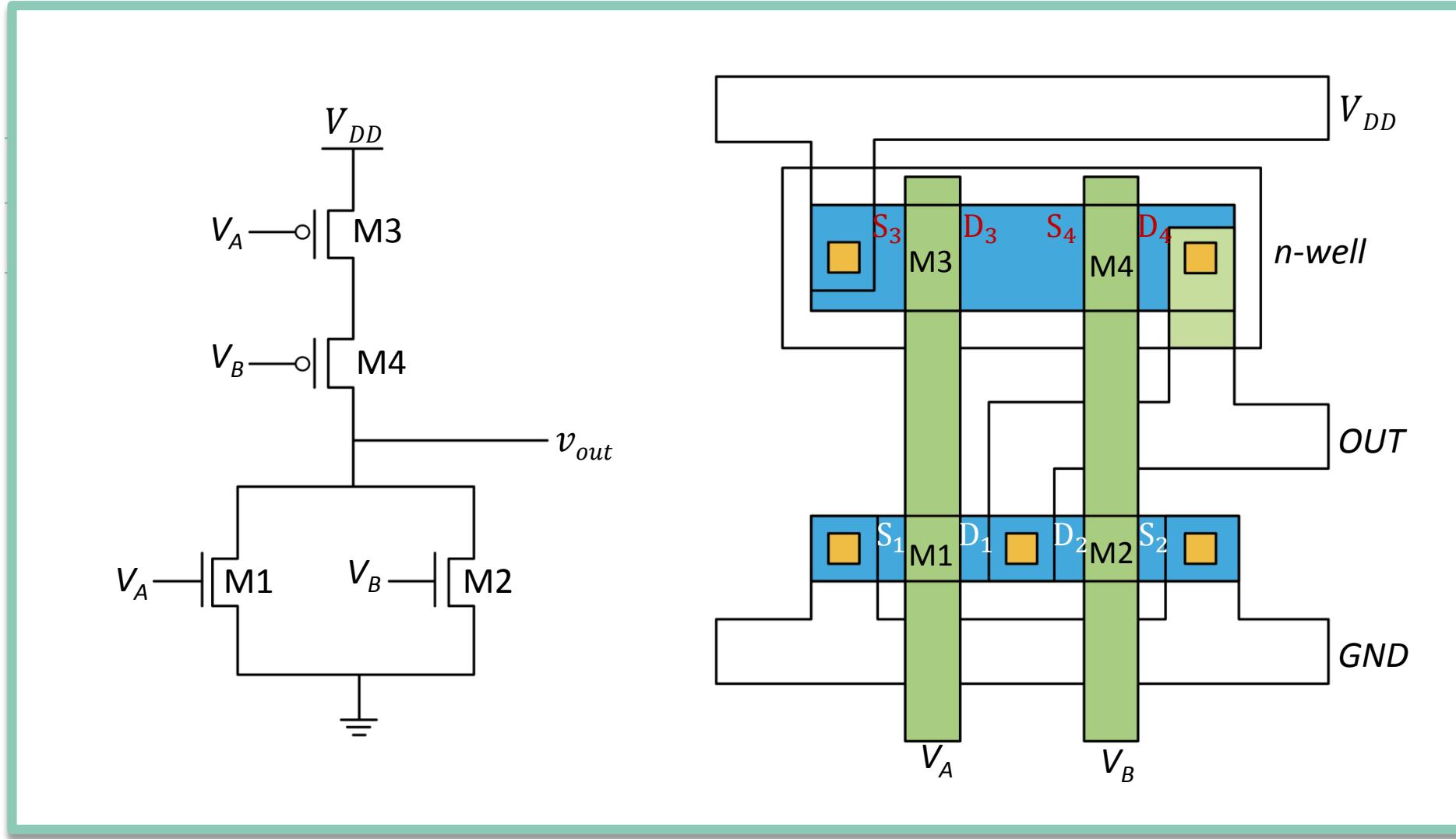
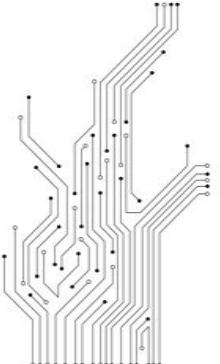
$$\begin{aligned} \text{But } I_D &= I_{D3} = \frac{k_p}{2} [2(V_{DD} - V_{th} - |V_{tp}|) * V_{SD3} - V_{SD3}^2] \quad (\text{LIN}) \\ &= I_{D4} = \frac{k_p}{2} (V_{DD} - V_{th} - |V_{tp}| - V_{SD3})^2 \end{aligned} \quad (\text{SAT}) \quad \left. \begin{array}{l} \text{PMOS} \\ \text{(SAT)} \end{array} \right\}$$

$$\text{Or } V_{DD} - V_{th} - |V_{tp}| = 2 \sqrt{\frac{I_D}{k_p}} \Rightarrow V_{th}$$

$$V_{tn} + \frac{1}{2} \sqrt{\frac{k_p}{k_n}} (V_{DD} - |V_{tp}|) = \frac{1}{1 + \frac{1}{2} \sqrt{\frac{k_p}{k_n}}} \sqrt{\frac{k_p}{k_n}} (V_{DD} - |V_{tp}|)$$

Compare with V_{th} of INV!

Layout of NOR2

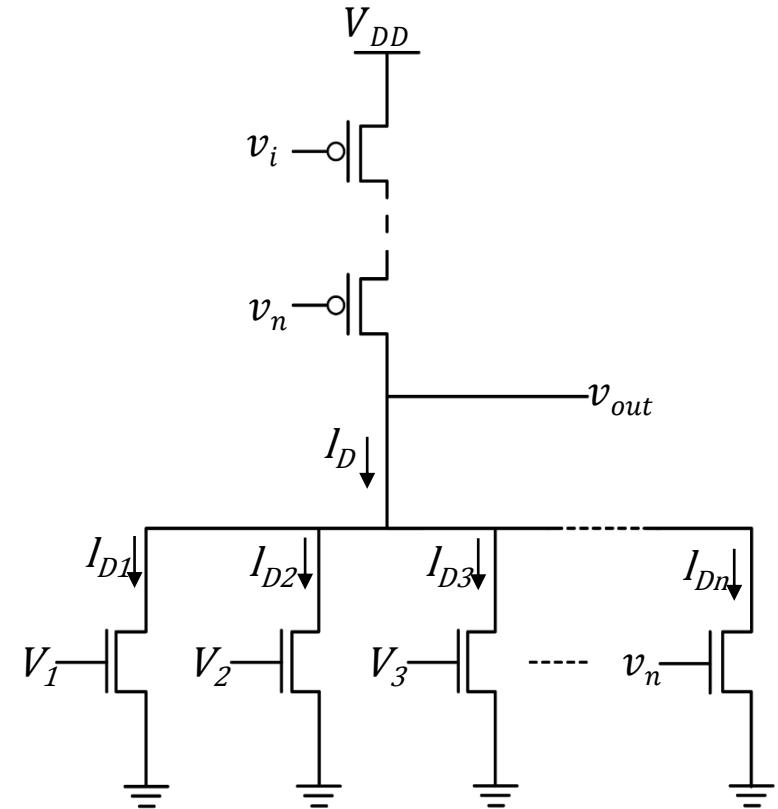


Equivalent $(W/L)_n$ of Parallel-connected Transistors

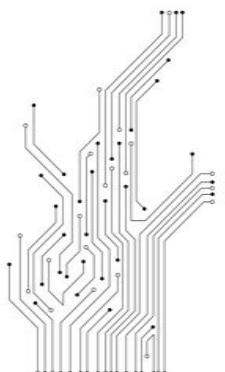
$$I_D = \sum_{k(on)} I_{D,k}$$

$$= \begin{cases} \sum_{k(on)} \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_k [2(v_{GSK} - V_{to})v_{out} - v_{out}^2] & \text{Linear} \\ \sum_{k(on)} \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_k (v_{GSK} - V_{to})^2 & \text{Saturation} \end{cases}$$

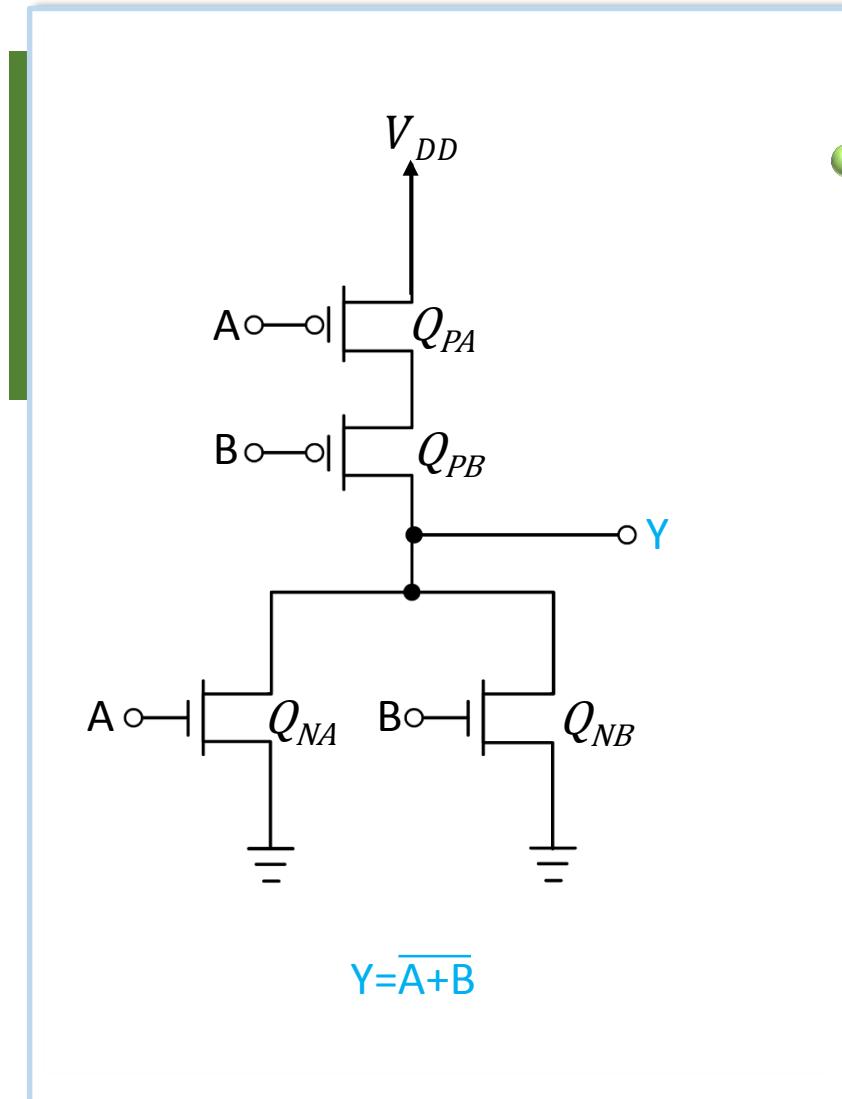
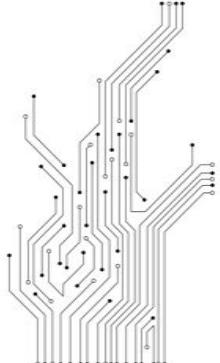
$$= \begin{cases} \frac{\mu_n C_{ox}}{2} \left(\sum_{k(on)} \left(\frac{W}{L}\right)_k \right) [2(v_{GSK} - V_{to})v_{out} - v_{out}^2] & \text{Linear} \\ \frac{\mu_n C_{ox}}{2} \left(\sum_{k(on)} \left(\frac{W}{L}\right)_k \right) (v_{GSK} - V_{to})^2 & \text{Saturation} \end{cases}$$



\therefore The equivalent aspect ratio, $\left(\frac{W}{L}\right)_{equ,driver}$ for the driver transistor is: $\sum_{k(on)} \left(\frac{W}{L}\right)_k$



Two I/P NOR Gate



Y to be low when A or B is high

∴ PDN consists of 2 parallel nMOS with A, B as I/P

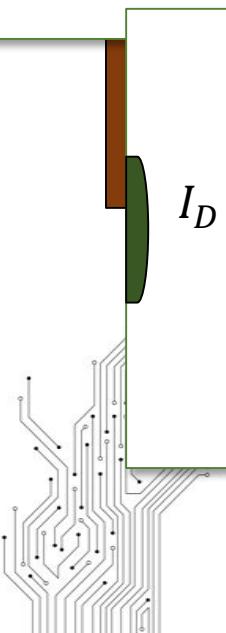
Y is high when A and B are both low

∴ PUN consists of 2 series pMOS with A, B as I/P

Equivalent $(W/L)_n$ of Series-connected Transistors

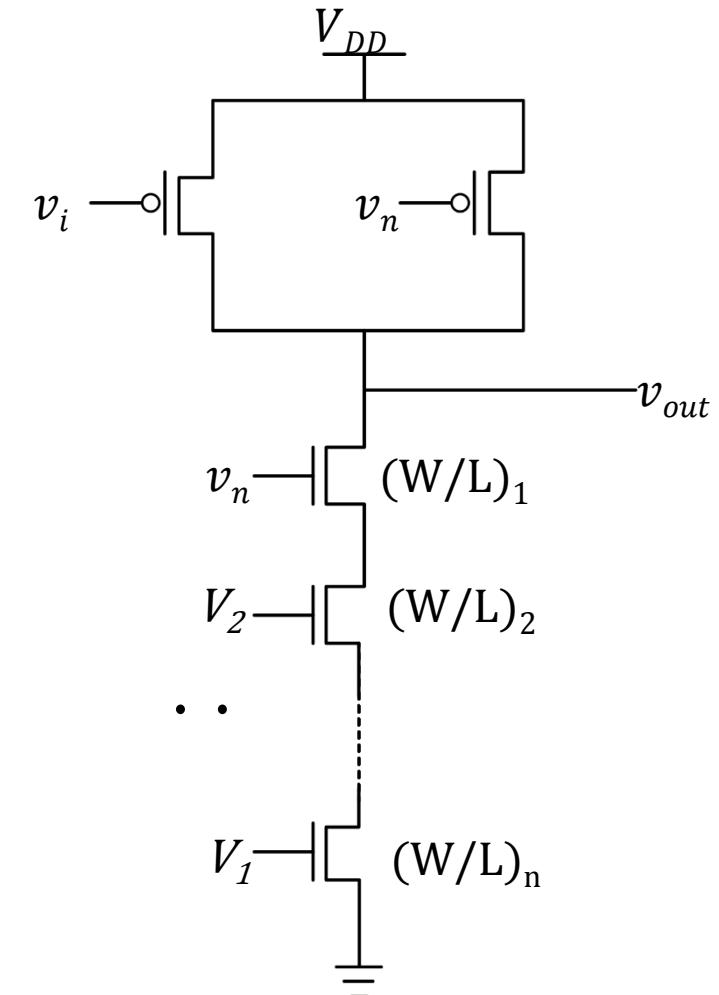
∴ The equivalent aspect ratio, $\left(\frac{W}{L}\right)_{equivalent}$ for the driver transistor is:

$$\sum_{k(on)} \frac{1}{\left(\frac{W}{L}\right)_k}, \text{ if } \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_n \text{ then } \left(\frac{W}{L}\right)_{equivalent} = \frac{1}{n} \left(\frac{W}{L}\right)$$



$I_D = \frac{\mu_n C_{ox}}{2} \left(\sum_{k(on)} \frac{1}{\left(\frac{W}{L}\right)_k} \right) \begin{cases} [2(v_{GSK} - V_{to})v_{out} - v_{out}^2] & \text{Linear} \\ (v_{GSK} - V_{to})^2 & \text{Saturation} \end{cases}$

$V_1 = V_2 = V_n$

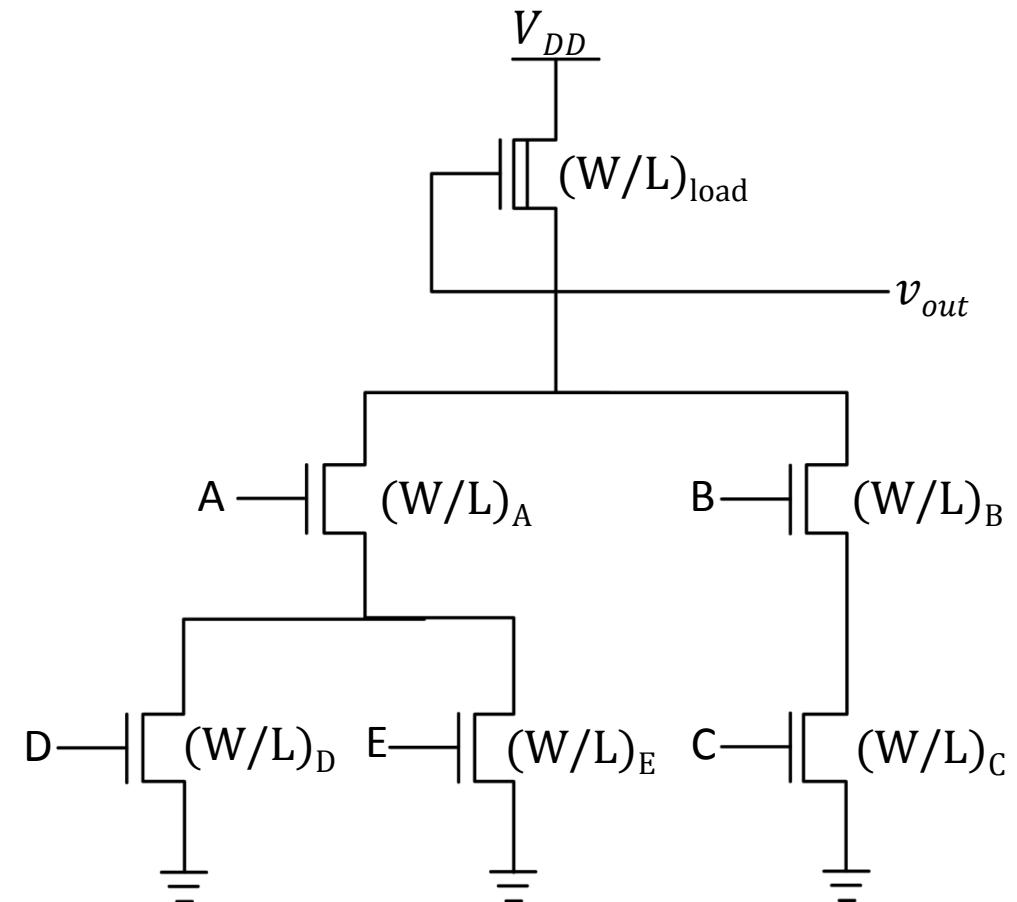
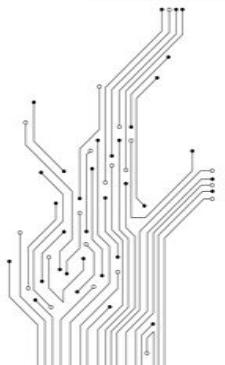


Complex Logic Gates

- For PDN:
 - OR: Parallel connected drivers
 - AND: Series connected drivers
 - Inversion is provided by the nature of MOS Circuit operation

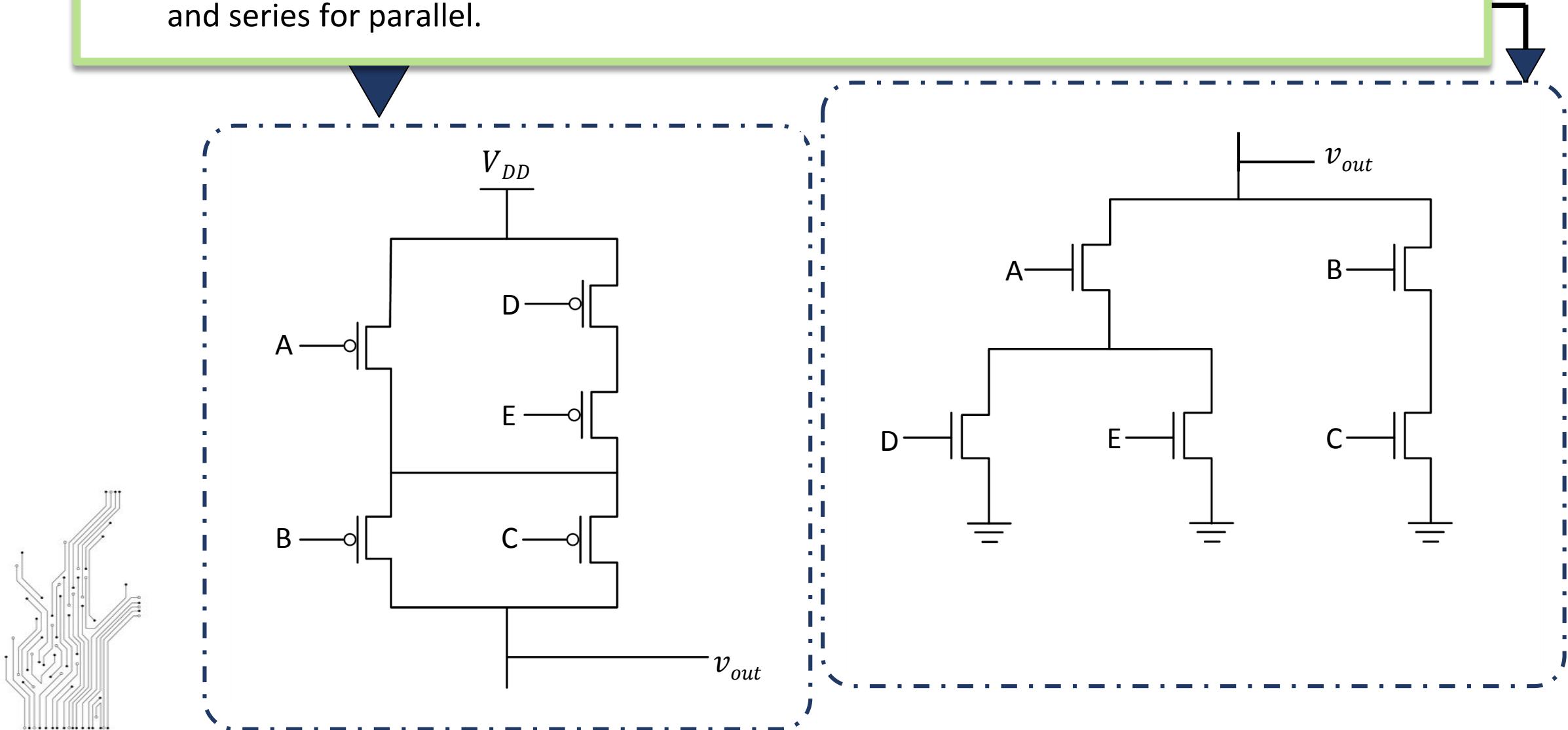
$$Z = \overline{A \cdot (D + E) + B \cdot C}$$

$$\left(\frac{W}{L}\right)_{equivalent} = \frac{1}{\left(\frac{W}{L}\right)_B + \left(\frac{W}{L}\right)_C} + \frac{1}{\left(\frac{W}{L}\right)_A + \left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E}$$

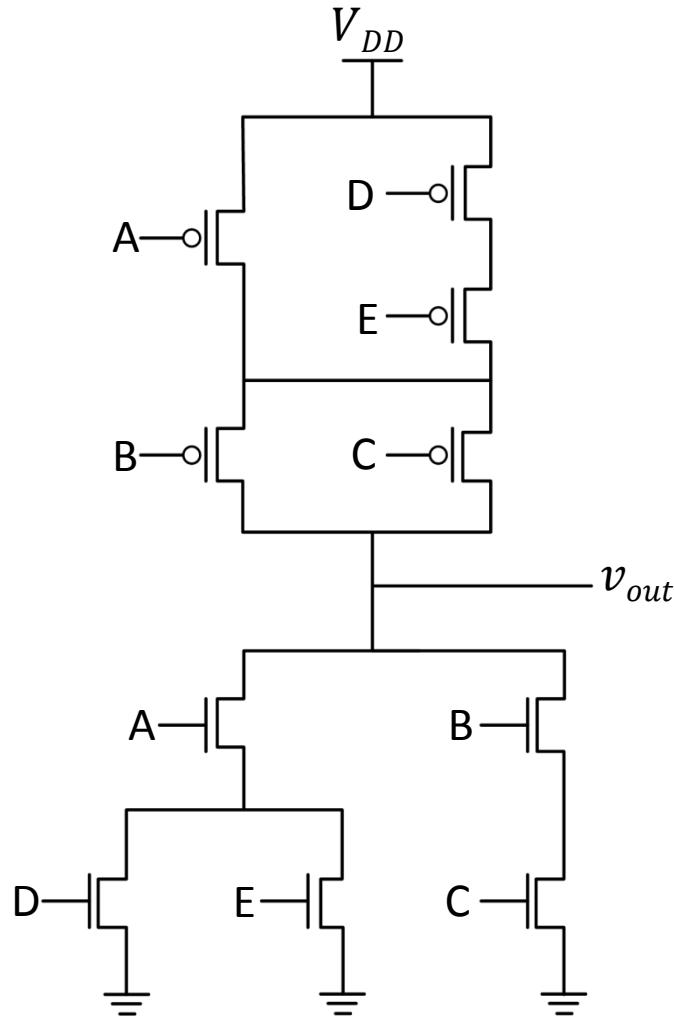


Completing the CMOS Design

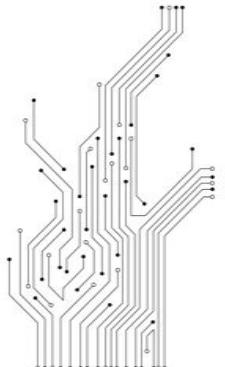
All parallel connections in nMOS will correspond to series connections in pMOS, and series for parallel.



Final Circuit Topology

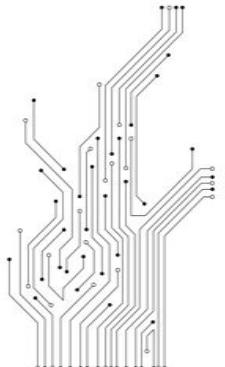
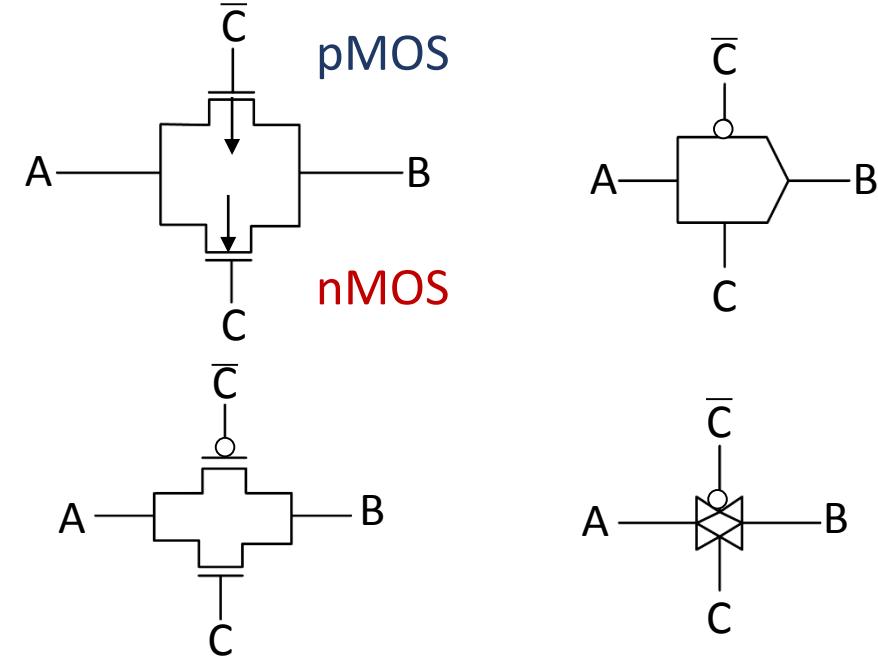


PUN + PDN
To ensure that no states
are undefined



CMOS Transmission Gate (TG)

- 1 x nMOS, 1 x pMOS in parallel
- Gate signals are complimentary
- Bidirectional switch that is controlled by the Gate voltage



DC Analysis of TG

$$v_{DSn} = V_{DD} - v_{out}$$

$$v_{GSn} = V_{DD} - v_{out}$$

nMOS: OFF $v_{out} > V_{DD} - V_{tn}$

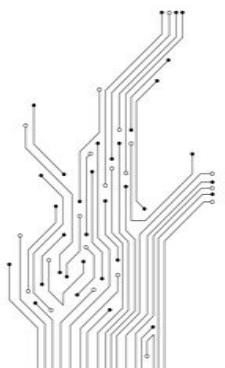
nMOS: SAT $v_{out} < V_{DD} - V_{tn}$

$$v_{DSP} = v_{out} - V_{DD}$$

$$v_{GSp} = -V_{DD}$$

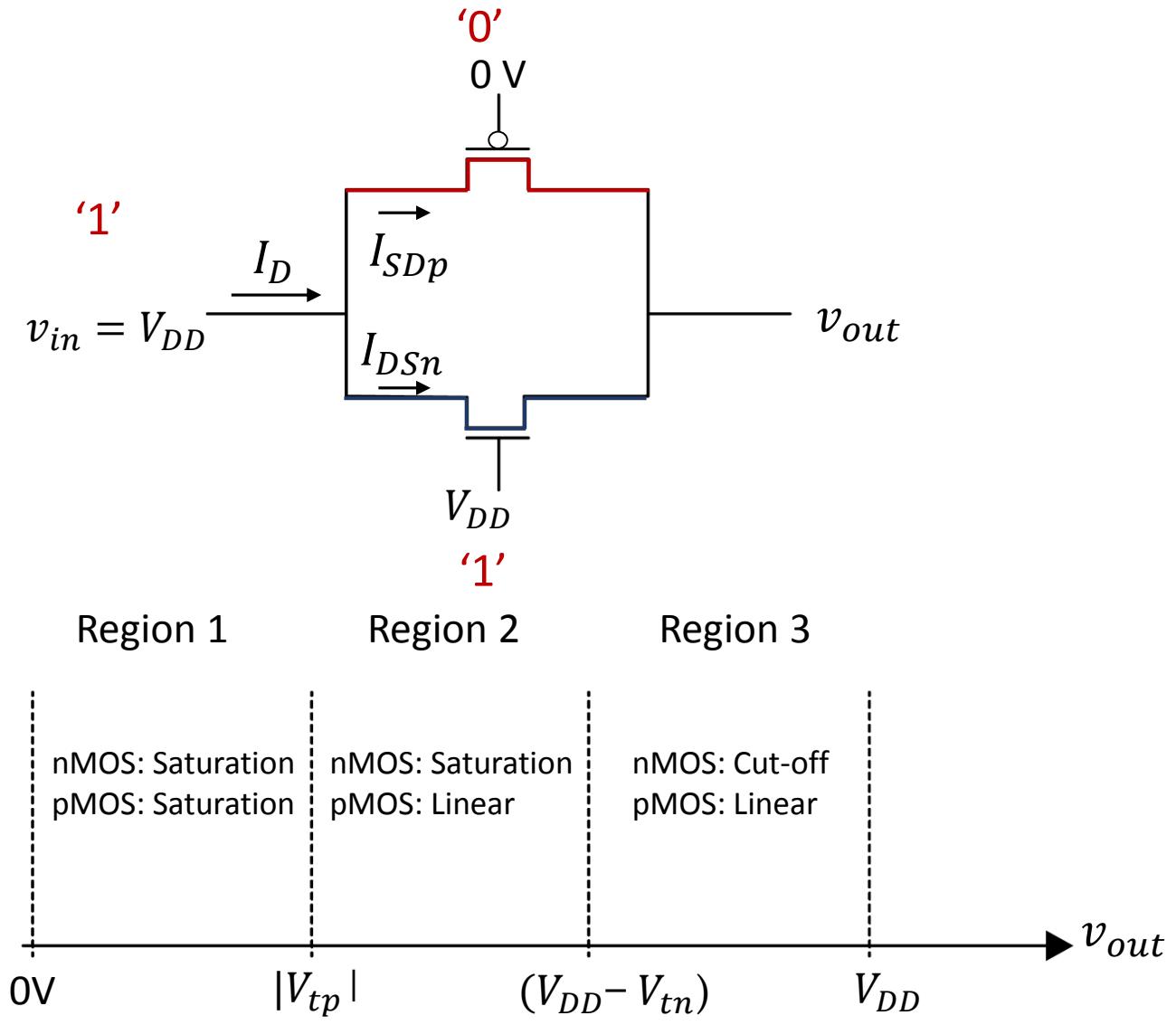
pMOS: LIN $v_{out} > |V_{tp}|$

pMOS: SAT $v_{out} < |V_{tp}|$



$$R_{EQn} = \frac{V_{DD} - v_{out}}{I_{DSn}}$$

$$R_{EQp} = \frac{V_{DD} - v_{out}}{I_{SDp}}$$



Problem of Pass Transistor Logic

$$v_{DSn} = V_{DD} - v_{out}$$

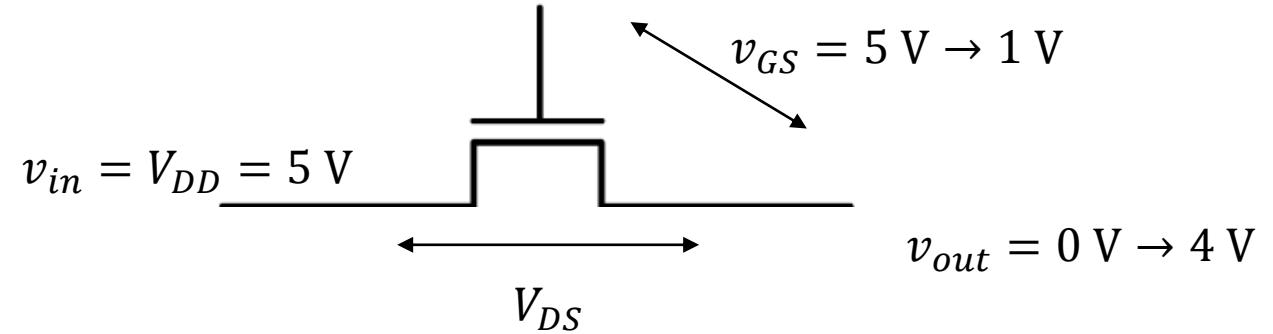
$$v_{GSn} = V_{DD} - v_{out}$$

nMOS: OFF $v_{out} > V_{DD} - V_{tn}$

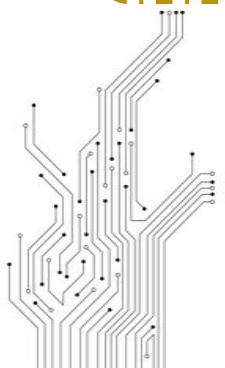
nMOS: SAT $v_{out} < V_{DD} - V_{tn}$

Assume $V_{DD} = 5 \text{ V}, V_{tn} = 1 \text{ V}^\circ$

$$V_{DD} = 5 \text{ V}$$



$v_{GS} - V_{tn} = 0 \text{ V}$ when v_{out} reaches 4 V.

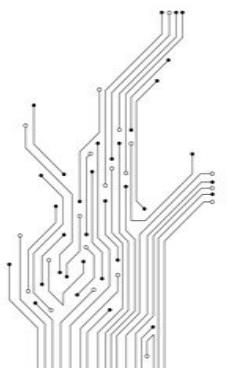


Region 1: $v_{out} < |V_{tp}|$

Both MOSs in SAT

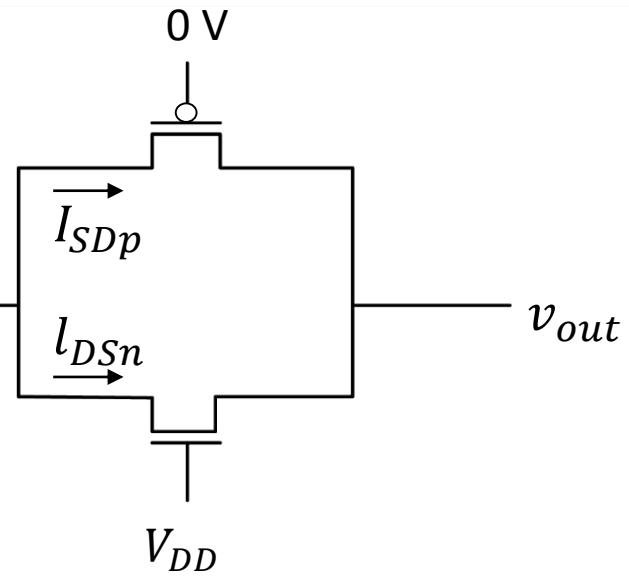
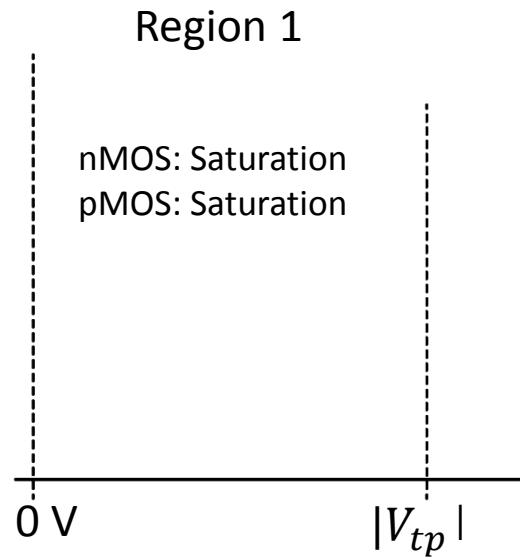
$$R_{Eqn} = \frac{2(V_{DD} - v_{out})}{k_n(V_{DD} - v_{out} - V_{tn})^2}$$

$$R_{Eqp} = \frac{2(V_{DD} - v_{out})}{k_p(V_{DD} - V_{tp})^2}$$



$$R = \frac{V}{I}$$

$$v_{in} = V_{DD} \xrightarrow{I_D} v_{out}$$



Region 2: $|V_{tp}| < v_{out} < V_{DD} - V_{tn}$

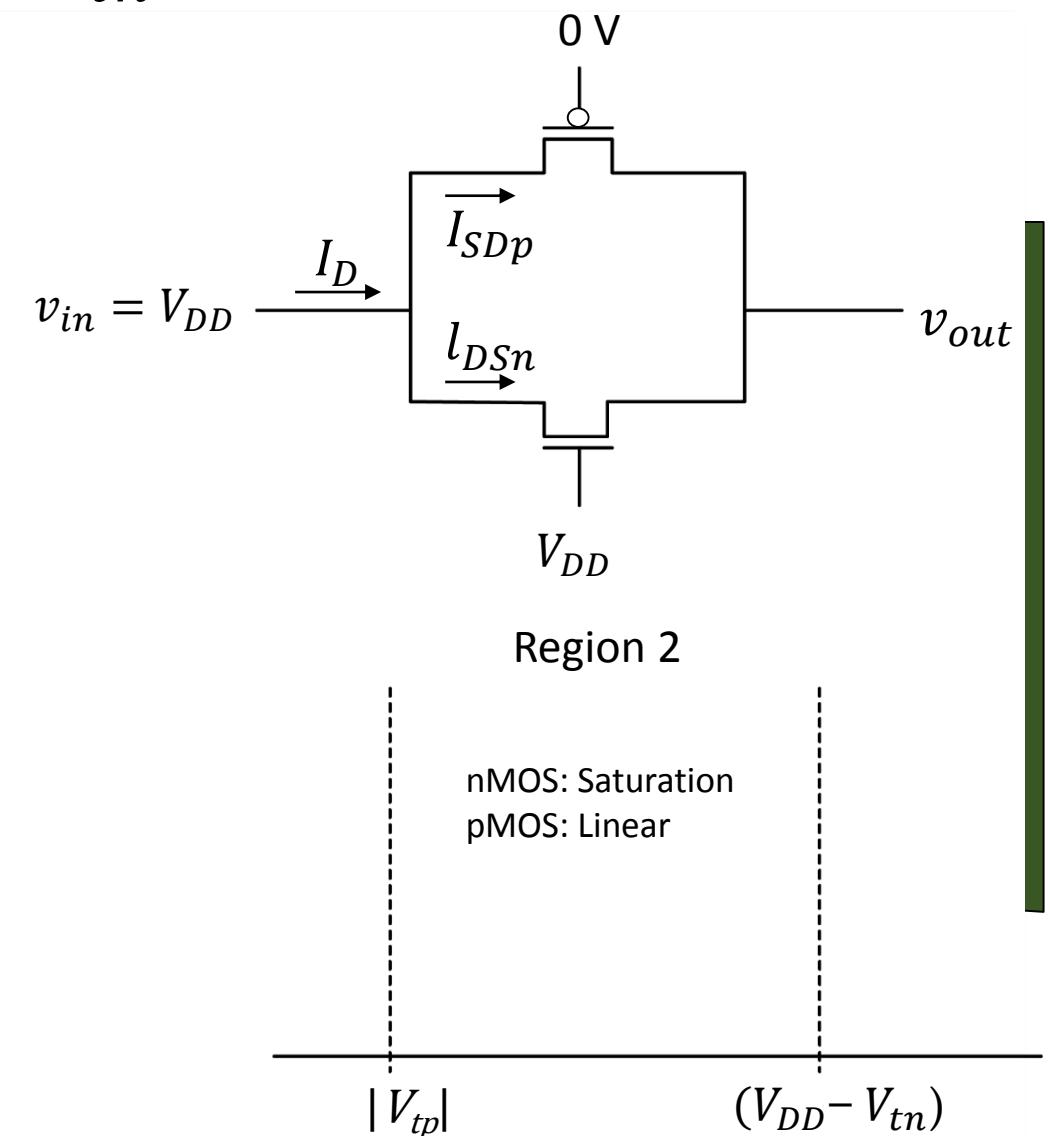
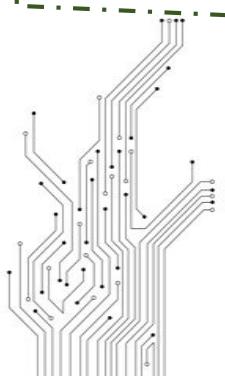
nMOS: SAT

pMOS: LIN

$$R_{Eqp} = \frac{2(V_{DD} - v_{out})}{k_p [2(V_{DD} - |V_{tp}|)(V_{DD} - v_{out}) - (V_{DD} - v_{out})^2]}$$

$$= \frac{2}{k_p [2(V_{DD} - |V_{tp}|) - (V_{DD} - v_{out})]}$$

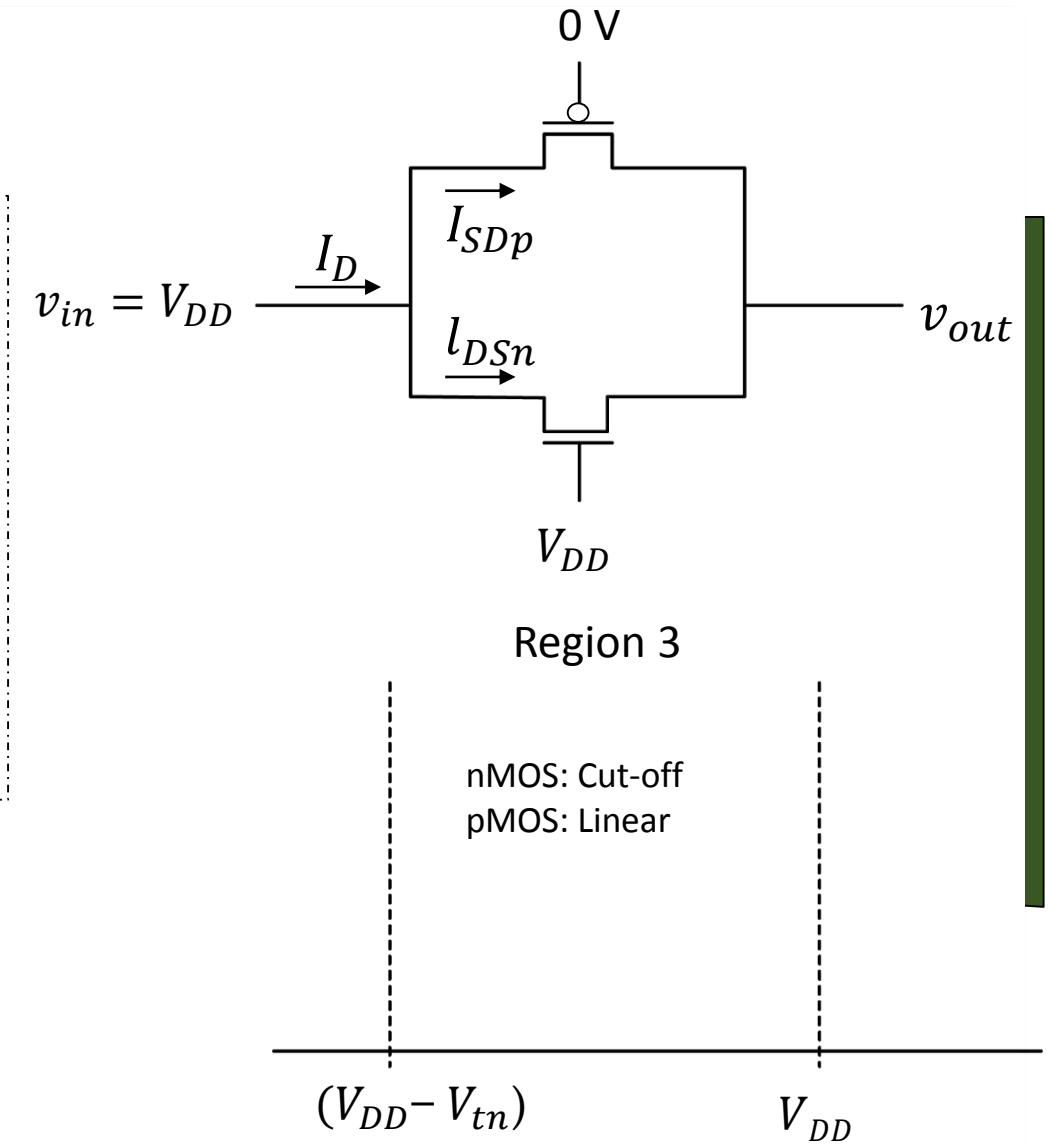
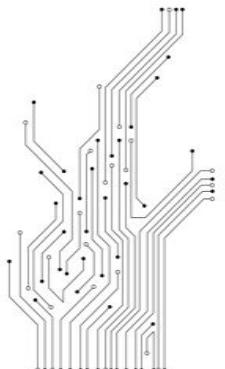
$$R_{Eqn} = \frac{2(V_{DD} - v_{out})}{k_n (V_{DD} - v_{out} - V_{tn})^2}$$



Region 3: $v_{out} > V_{DD} - V_{tn}$

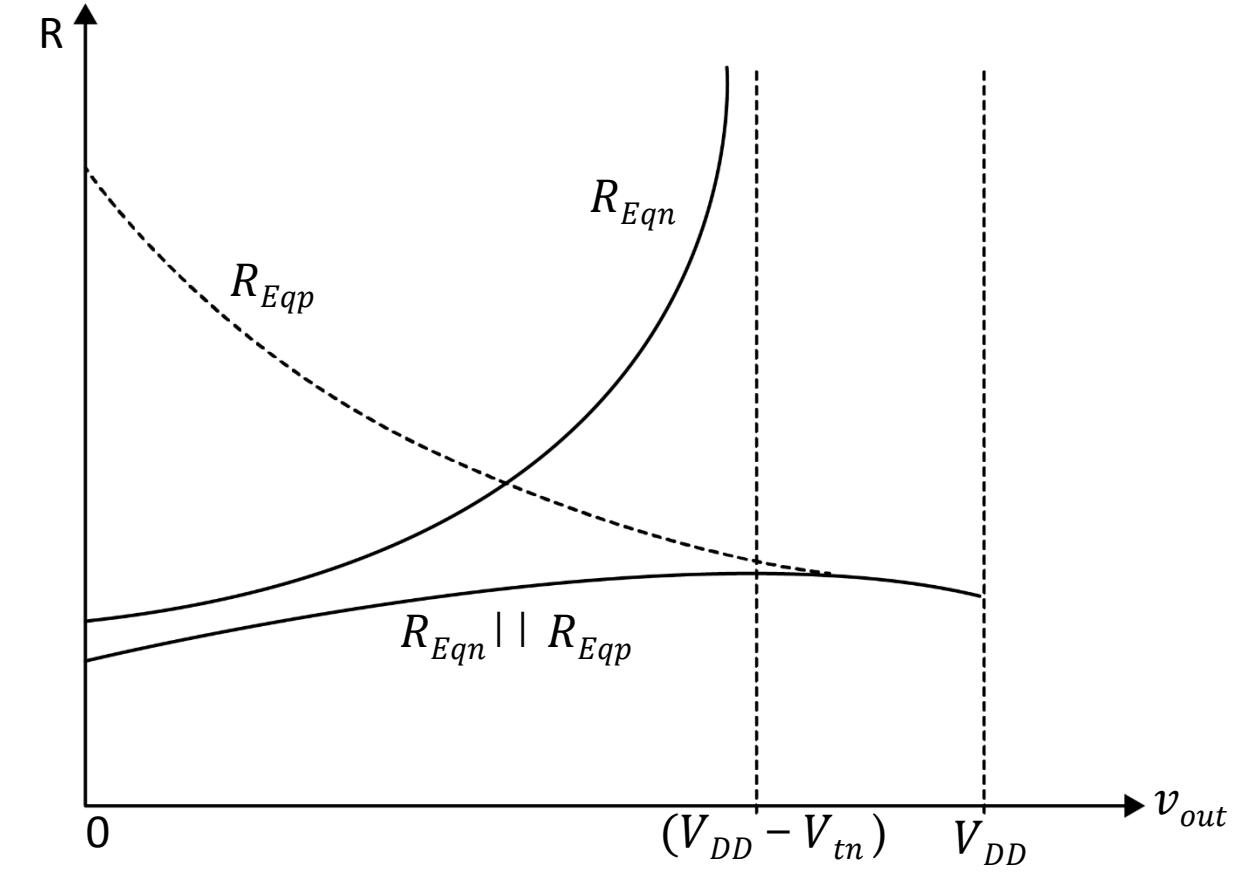
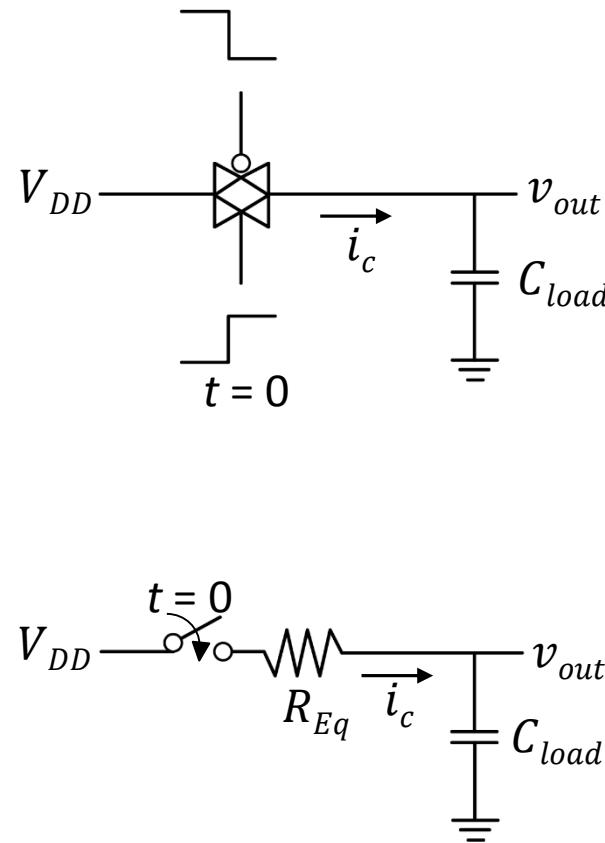
nMOS: OFF
pMOS: LIN

$$R_{Eqp} = \frac{2}{k_p [2(V_{DD} - |V_{tp}|) - (V_{DD} - v_{out})]}$$



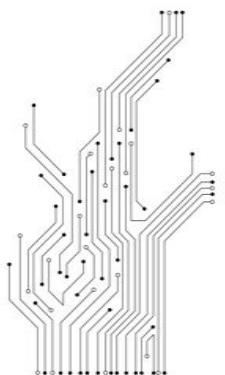
R_{EQ} of TG

- 1. Low R
- 2. Low variation of R ($\sim k\Omega$)

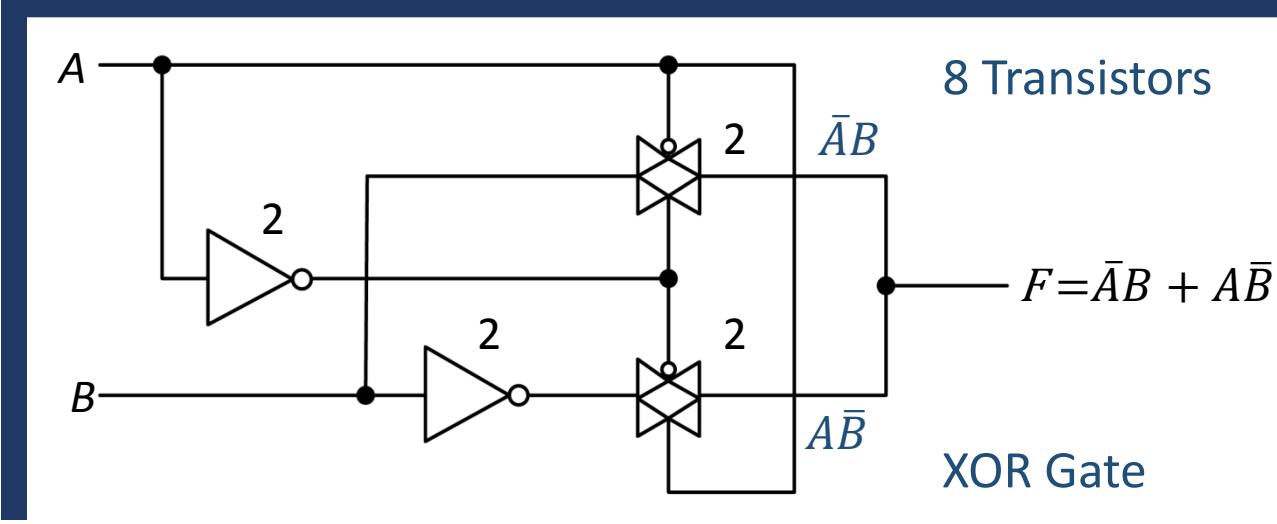


Observation

It can be seen that the total equivalent resistance of the TG remains relatively constant (i.e. it is independent of v_{out}).

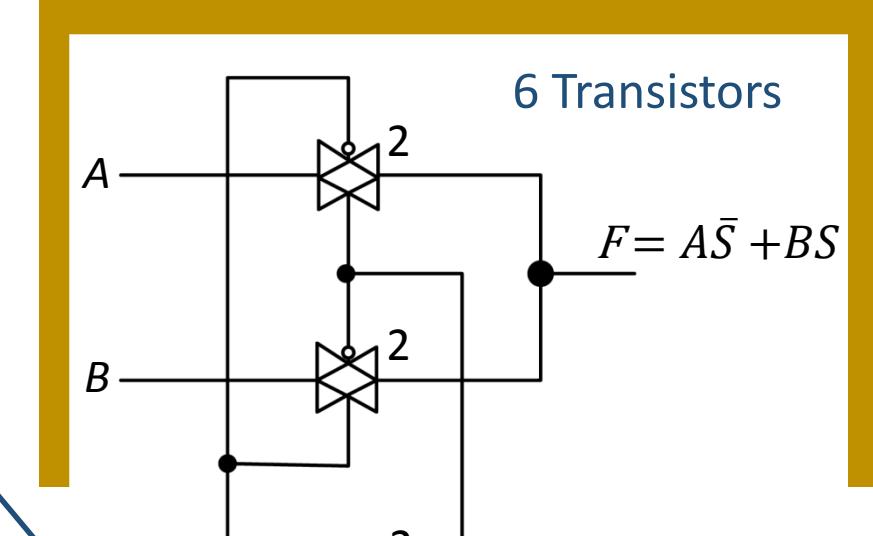


Example of TG Circuits



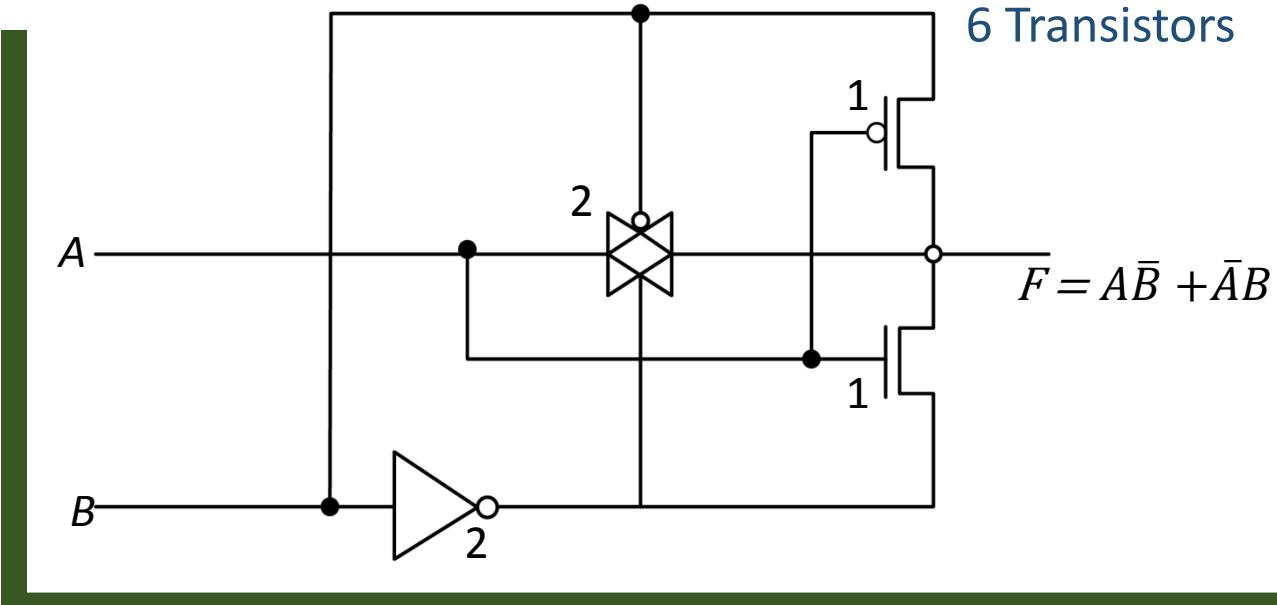
8 Transistors

XOR Gate



6 Transistors

Multiplexer



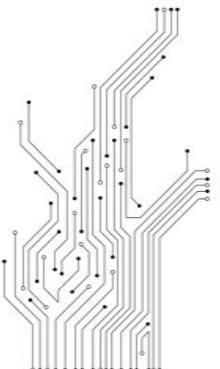
6 Transistors

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

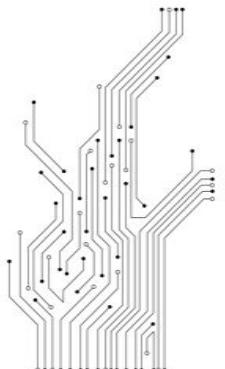
Summary

Here are the key takeaways from this lesson.

- ▶ The CMOS layout consists of Diffusion, Polysilicon, metal and Oxide.
- ▶ The CMOS process consists of nMOS and pMOS transistors.
- ▶ The three operating regions of nMOS and pMOS transistors are Cut-off, Linear and Saturation regions.
- ▶ The VTC of a CMOS inverter consists of these five elements; V_{IL} , V_{IH} , V_{th} , V_{OL} and V_{OH} .
- ▶ The five different operating regions in the VTC and the noise margins of a CMOS inverter.
 - ▶ There are three types of circuit delays; τ_p , τ_{rise} and τ_{fall} .
 - ▶ Dynamic power dissipation = $P_d = C_L \cdot V_{DD}^2 \cdot f$.
 - ▶ A CMOS ring oscillator has its application as a clock generator.
 - ▶ The effect of transistor sizing; W/L ratio.
 - ▶ A CMOS Transmission Gate holds application as a digital switching circuit .



Thank You



CMOS Logic Circuits