NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2018-2019

EE3019 – INTEGRATED ELECTRONICS

November / December 2018 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer ALL questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.
6. A list of Formulae is provided in Appendix A on page 6.

---

1. (a) Sketch the Voltage Transfer Characteristics of a symmetrical CMOS inverter. Identify the regions of operation of both the pMOS and nMOS transistors of the CMOS inverter when the input changes from 0 V to V_{DD}. Briefly discuss how the variations of V_{IL}, V_{IH}, V_{OL}, V_{OH} and V_{th} can affect the noise margin of the inverter.

(9 Marks)

(b) Consider a CMOS inverter in Figure 1 on page 2. Assume $V_{DD} = 1.2$ V, $V_{OH} = 1.1$ V, $V_{OL} = 0.1$ V, $C_o = 5$ fF and $C_g = 9$ fF. The falling time, τ_f, for V_{in} is 530 ps. The parameters of the pMOS and nMOS transistors are given below:

pMOS $V_{tp} = -0.45$ V, $\mu_p C_{ox} = 20\ \mu A/V^2$, $(W/L)_p = 4.5$

nMOS $V_{tn} = 0.46$ V, $\mu_n C_{ox} = 50\ \mu A/V^2$, $(W/L)_n = 2$

For parts (i) and (ii) below, state all your assumptions clearly.

Note: Question No. 1 continues on page 2.

9

(i) Identify the regions of operation of both the pMOS and nMOS transistors, and determine the drain current i_L when V_{out} is at 20% and 80% of its full value.

(ii) Determine the rising time, t_r, for V_{out} to rise from 20% to 80% of its full value.

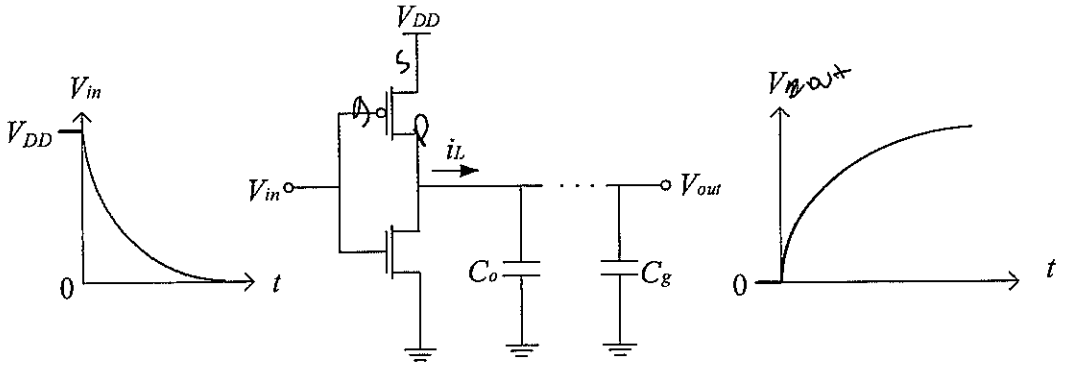


Figure 1

(13 Marks)

(c) Discuss how the noise margin and operating speed of a CMOS logic circuit could be affected by the transistor body effect.

(3 Marks)

2. (a) Consider the 1-T DRAM cell which is constructed using an nMOS transistor. Assume that V_{DD} = 1.2 V and the threshold voltage, V_{tn} = 0.46 V. The bit-line precharge voltage is 0.5 V_{DD}, bit-line capacitance is 0.52 pF and the storage capacitance per cell is 33 fF. Determine the voltage swing of the bit-line for a READ operation when accessing stored data values of '0' and '1'. Briefly discuss the purpose of the Sense Amplifier for the DRAM.

(8 Marks)

(b) A feedback amplifier is shown in Figure 2 on page 3. It is given that R_L = 10 kΩ, R_1 = 7 kΩ, R_2 = 53 kΩ , R_3 = 70 kΩ and R_4 = 60 kΩ,

(i) Identify the feedback topology, and determine the feedback factor, β.

(ii) Determine the closed-loop voltage gain, v_o/v_s, if the op-amp has an open-loop gain of $A = \infty$ and $A = 10^4$.

(iii) If the closed-loop gain changes by 0.5%, determine the corresponding change in the open-loop gain.

Note: Question No. 2 continues on page 3.

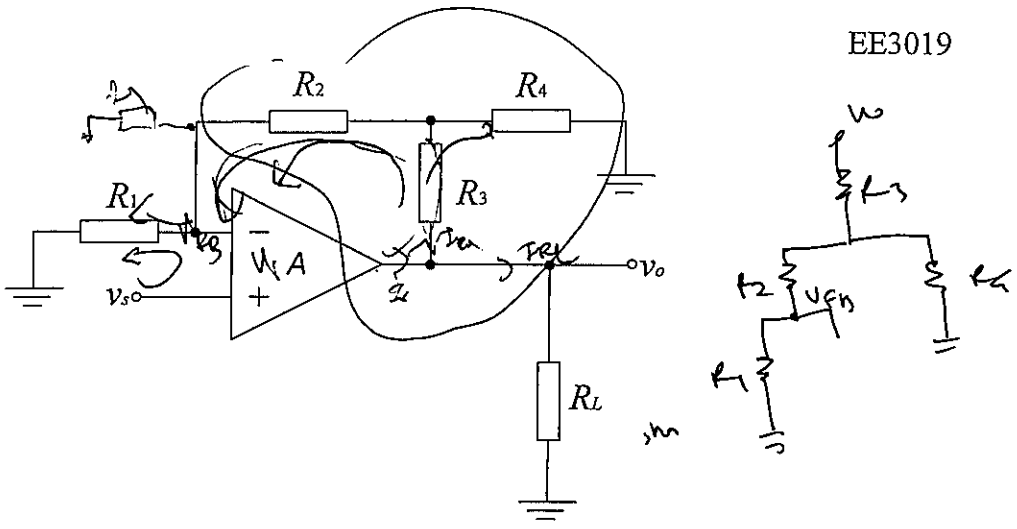


Figure 2

(14 Marks)

(c) Explain why the gain of the negative feedback amplifier decreases at high frequencies.

(3 Marks)

3. The circuit schematic of a Bandgap voltage reference with low Fractional Temperature Coefficient (TC_F) is depicted in Figure 3 on page 4. Resistor R_4 serves to improve the insensitivity to temperature and can be assumed to be a short circuit.

(a) Define the following two parameters:

(i) TC_F, and

(ii) $S_{V_{CC}}^{V_{REF}}$, the sensitivity of the output reference voltage with respect to the supply rail voltage, V_{cc}.

(4 Marks)

(b) Draw a conceptual block diagram of the Bandgap voltage reference and explain the phenomena that provide for low TC_F and low $S_{V_{CC}}^{V_{REF}}$.

(6 Marks)

(c) Derive the expression for the output voltage, V_{REF}, of the Bandgap voltage reference depicted in Figure 3.

(12 Marks)

(d) An engineer chose to employ the fully-bipolar LM741 op-amp in Figure 3. Explain and discuss if this op-amp choice is practically appropriate.

(3 Marks)

Note: Question No. 3 continues on page 4.

10

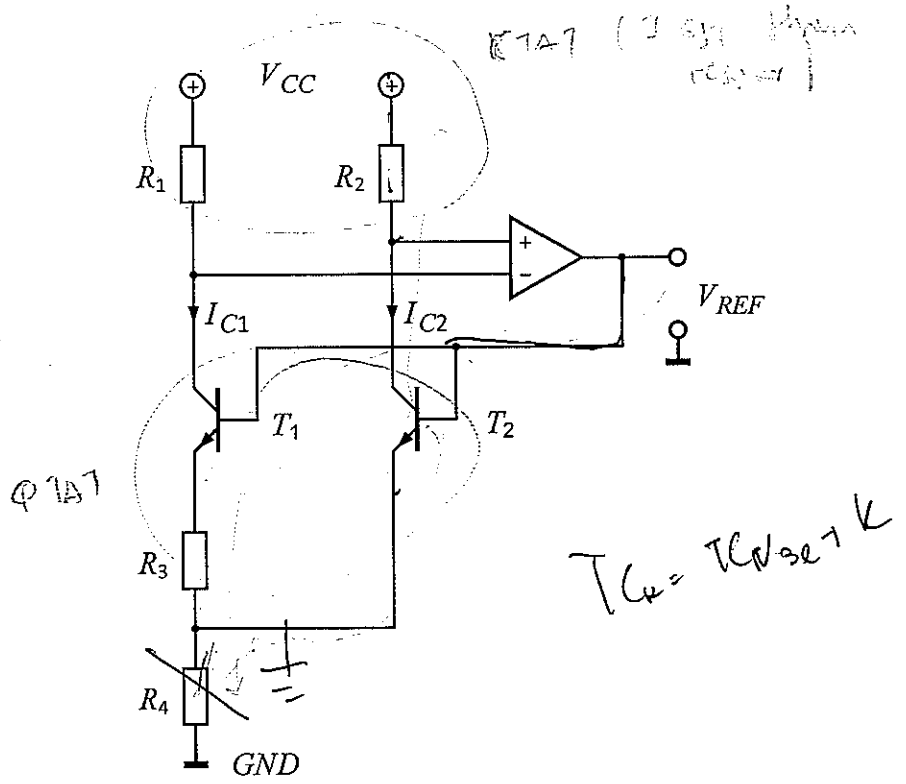


Figure 3

4. The hybrid BJT-CMOS op-amp depicted in Figure 4 on page 5 has three poles located at 10 kHz, 1 MHz and 100 MHz. Assume $R = 465\ \text{k}\Omega$ and the following parameters for the transistors in the op amp:

MOS transistors: $|V_t| = 0.8$ V, $\mu_n C_{ox} = 30\mu\text{A/V}^2$, $\mu_p C_{ox} = 15\mu\text{A/V}^2$, $|V_A| = 50$ V

BJT transistors: $V_{BE(on)} = 0.7$ V, $|V_A| = 50$ V

(a) Explain the function of transistors M_6 and T_9.

(4 Marks)

(b) Assume that the emitter area of the BJT transistors is equal. Determine the drain and collector bias currents in the MOS and BJT transistors, respectively. Complete the following table in your answer script.

Transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	T_9	T_{10}
Current										

(7 Marks)

Note: Question No. 4 continues on page 5.

(c) Determine the voltage gain of the first stage of the op-amp. Assuming that the voltage gain of the second stage of the op-amp is 500, determine if the op-amp is stable.

(12 Marks)

(d) In present-day electronic devices where the integrated circuits are very densely placed, the op-amp is required to feature very high power supply rejection ratio (PSRR). Explain how you would design the op-amp in Figure 4 to obtain high PSRR, and discuss the implication of your design.

(2 Marks)

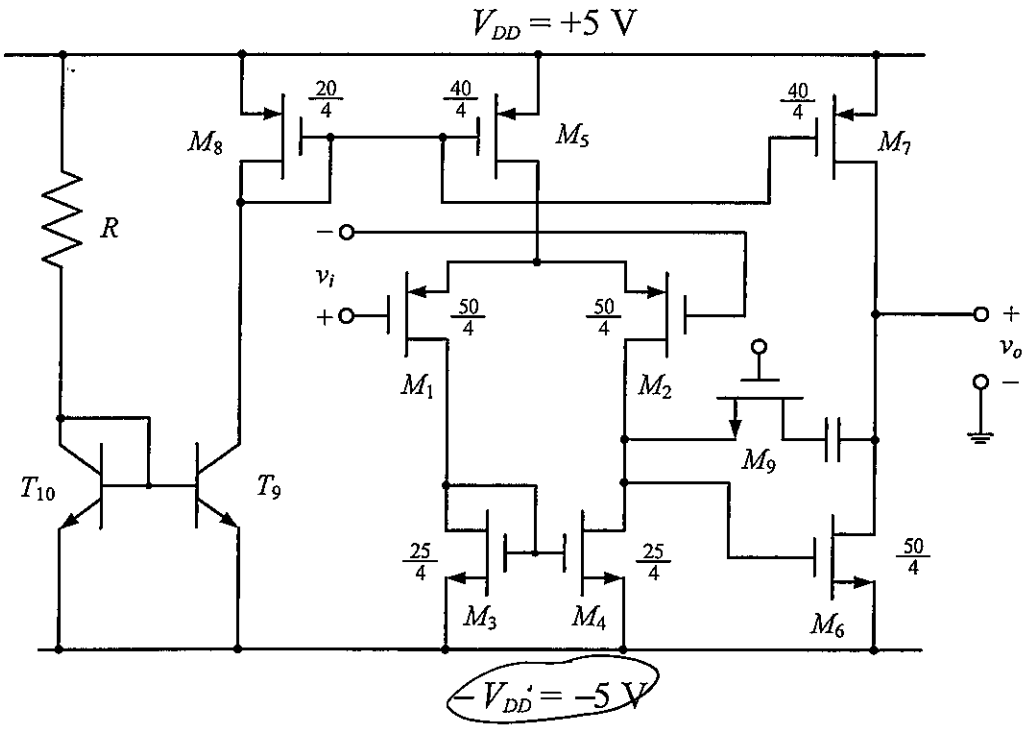


Figure 4

APPENDIX A: List of Formulae for EE3019

$$V = I\,Z \qquad P = I\,V$$

$$Z_L = j\omega L \qquad Z_C = \frac{1}{j\omega C}$$

$$\sum_{m=1}^{M} v_m = 0 \qquad \sum_{n=1}^{N} i_n = 0$$

$$v = L\frac{di}{dt} \qquad i = C\frac{dv}{dt}$$

$$\boldsymbol{S = V\,I^*} \qquad i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

$$V_T = \frac{kT}{q} \qquad i_C \approx I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]$$

$$\beta = \frac{i_C}{i_B}$$

$$i_E = i_C + i_B \qquad A + B + C = \overline{\overline{A}\,\overline{B}\,\overline{C}}$$

$$\alpha = \frac{\beta}{1+\beta} \qquad \tau_P = \frac{C_{load} \times \Delta V}{I_{avg}}$$

$$ABC = \overline{\overline{A} + \overline{B} + \overline{C}} \qquad A_f = \frac{A}{1 + A\beta}$$

$$i_{Dn(LIN)} = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left((v_{GS} - v_t)v_{DS} - \frac{1}{2}{v_{DS}}^2\right) \qquad f = \frac{1}{2n\,\tau_p}$$

$$i_{Dn(SAT)} = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - v_t)^2 \qquad V_1 = A_1 A_2\left(V_i - \beta V_o\right) + A_1 V_n$$

$$A(s) = A_m F_H(s) = \frac{A_m}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \qquad r_o = \frac{V_A}{I_D}$$

$$\tau_{PLH} = \sqrt{{\tau_{PLH}}^2(\text{Step Input}) + \left(\frac{\tau_f}{2}\right)^2} \qquad g_m = 2\frac{I_D}{(V_{GS} - V_t)}$$

$$\frac{dA_f}{A_f} = \frac{1}{1 + A\beta} \cdot \frac{dA}{A}$$

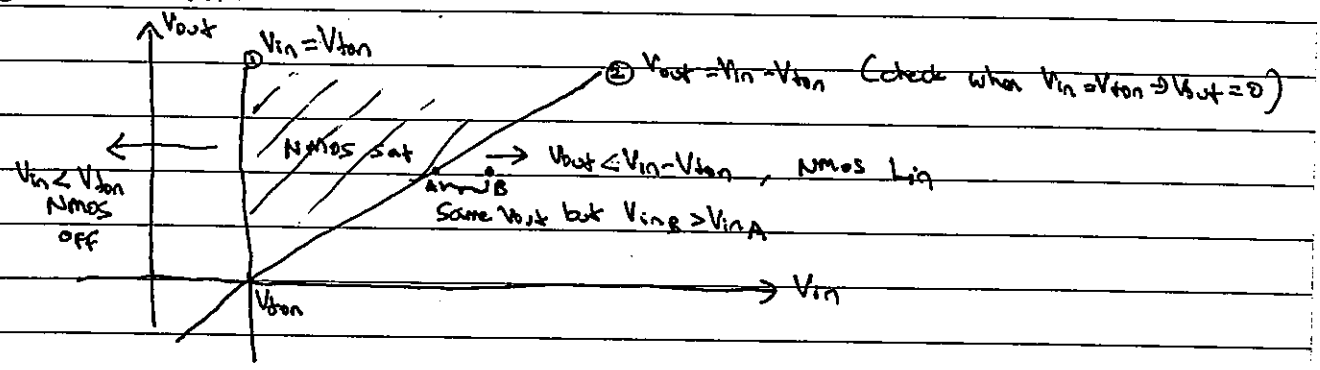
END OF PAPER

Note: please be reminded that this solution is for your reference only. It is not the official solution from examiners & thus might subject to error. Pls examine it carefully

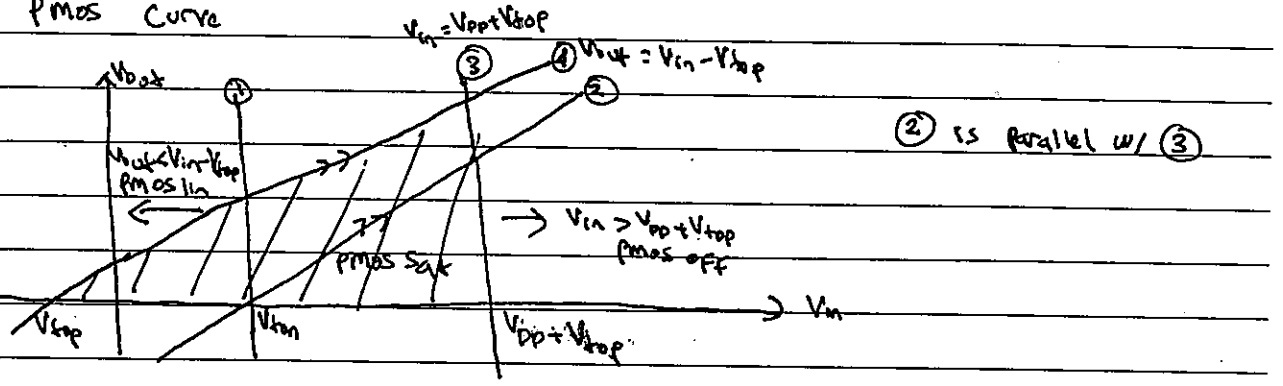
1. (a) * Sketch VTC

The answer is available in lecture notes. Here I will give you the step-by-step procedure on how to draw the curve to make it easier.

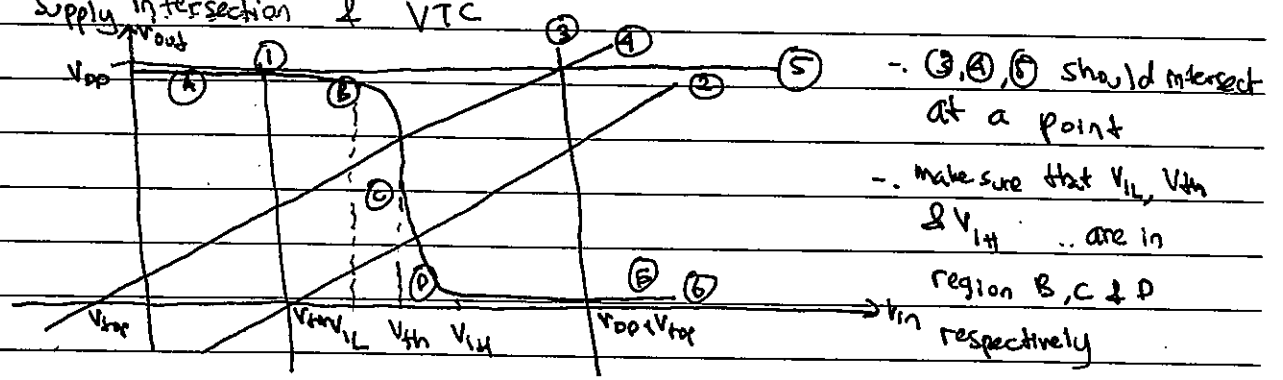
① Nmos Curve



② Pmos Curve



③ Supply intersection & VTC



- ③, ④, ⑤ should intersect at a point
- make sure that V_{IL}, V_{th} & V_{IH} .. are in region B, C & D respectively

Final answer:

* identify operation region

to identify, the student should realize from CMOS inverter schematic that $V_{GSn} = V_{in}$ $V_{GSp} = -(V_{DD} - V_{in})$

$V_{DSn} = V_{out}$ $V_{DSp} = -(V_{DD} - V_{out})$

① in each region (A, B, C, D, E), write the equation of Vout & Vin that contains Vton & Vtop, ② then change the Vout & Vin in terms of V_{GSn}, V_{DSn}, V_{GSp}, V_{DSp}.

③ Deduce from the eq the operating region

for your reference only

or else, you can memorize it

Final answer: region A = NMOS off, PMOS lin ↑ (reverse)

—"— B = —"— Sat, —"— lin

—"— C = —"— Sat, —"— Sat

—"— D = —"— lin, —"— Sat

—"— E = —"— lin ↓, —"— off

* The variations of $V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{th}$ might reduce NM in certain cases.

Recall that $NM_H = V_{OH} - V_{IH}$ $NM = \min(NM_L, NM_H)$

$NM_L = V_{IL} - V_{OL}$

For example, $NM_H < NM_L$ so that $NM = NM_H$. When V_{OH} or V_{IH} change such that $NM_H' < NM_H$, the new NM' will be less than NM of the original value.

(b) (i) assumption: Ignore T_F of V_{in} at the moment, i.e we are assuming that V_{in} is step function. Analyze when V_{in} is in its final state ($V_{in} = 0$ V)

② full value refer to V_{OH} instead of V_{DD}

$V_{GSn} = V_{in}$ $V_{SGp} = V_{DD} - V_{in}$

$V_{DSn} = V_{out}$ $V_{SDp} = V_{DD} - V_{out}$

* $V_{out} = 20\% V_{OH} = 0.2 \cdot 1.1 = 0.22$ V

NMOS: $V_{GSn} = V_{in} = 0$V $< V_{tn} = 0.46$V → off

PMOS: $V_{SGp} = V_{DD} - V_{in} = 1.2$ V

$V_{SDp} = V_{DD} - V_{out} = 1.2 - 0.22 = 0.98$ V

$0.98 > 1.2 - 0.45 \Leftrightarrow V_{SDp} > V_{SGp} - |V_{top}|$ → Sat

$i_{20\%} = i_{pmos\,sat} = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right)_p (V_{SGp} - |V_{tp}|)^2$

$= \frac{20\mu}{2} \cdot 4.5 (1.2 - 0.45)^2 = 25.3125\ \mu A$

* $V_{out} = 80\% V_{OH} = 0.8 \cdot 1.1 = 0.88$ V

NMOS : off

PMOS : $V_{SGp} = 1.2$V $V_{SDp} = 1.2 - 0.88 = 0.32$ V

$0.32 < 1.2 - 0.45 \Leftrightarrow V_{SDp} < V_{SGp} - |V_{top}|$ → lin

$i_{80\%} = i_{pmos\,lin} = \mu_p C_{ox} \left(\frac{W}{L}\right)_p ((V_{SGp} - |V_{tp}|) V_{SDp} - 0.5 V_{SDp}^2)$

$= 20\mu \cdot 4.5 ((1.2 - 0.45) \cdot 0.32 - 0.5 \cdot 0.32^2)$

$= 16.992\ \mu A$

1. (b) (ii) Firstly, find t_r when V_{in} is a step function

I_{avg}: $\frac{i_{20\%} + i_{80\%}}{2} = \frac{25.3125 + 16.992}{2} = 21.15225\ \mu A$

$C = C_o + C_g = 5 + 9 = 14fF$

ΔV: $V_{80\%} - V_{20\%} = 0.88 - 0.22 = 0.66\ V$

$\tau_{r\,step}$: $\frac{C \cdot \Delta V}{I_{avg}} = \frac{14f \cdot 0.66}{21.15225\mu} = 0.4368\ nS$

Then use the formula

$\tau_{r\,actual} = \sqrt{\tau_{r\,step}^2 + \left(\frac{\tau_{fin}}{2}\right)^2}$

$= \sqrt{0.4368^2 + \left(\frac{0.53}{2}\right)^2} = 0.5109\ nS$

assumption:

1.) approximating the value with formula given by $\tau_{ractual}$ is accurate enough to give the answer to the question

2.) C at output node is only contributed by C_o & C_g

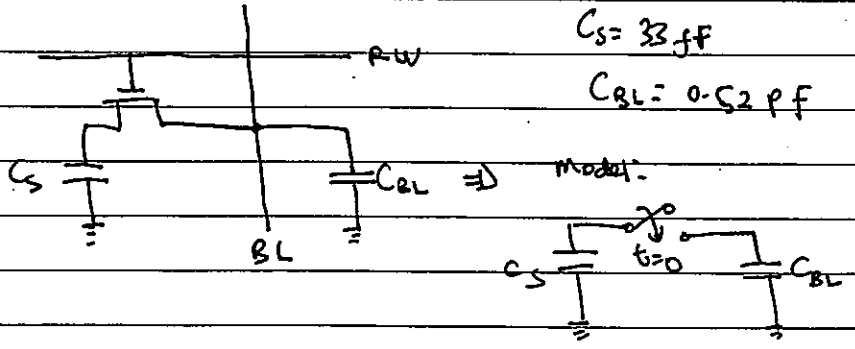
3.) ignore 2nd order effect s.a λ, V_t', etc

(c) when there is body effect, the threshold voltage will be increased. This might result in:

1.) NM ↓ because when V_{th} changes, the VTC curve will change & thus affect V_{IH}, V_{OH}, V_{IL} & V_{OL} accordingly, resulting in change in NM

2.) Speed ↓ because to switch from 0→1 will take longer time due to V_{th} being increased

2. (a) 1-T DRAM



$C_S = 33fF$

$C_{BL} = 0.52\ pF$

For your reference only

* Read 0

When reading 0, RW will be charged to V_{DD} to turn on NMOS & BL will be pre-charged to $\frac{V_{DD}}{2}$. C_S is storing Logic 0 &

thus $V_{CS} = 0V$. When NMOS is on, I will flow from C_{BL} to C_S & will decrease V_{BL}. Sense amplifier will detect this small decrease of V_{BL} & amplify it through positive fB to read the 0 value

initial voltage → $V_{CS} = 0V$ $V_{CBL} = 0.5V_{DD} = 0.6V$

final voltage → $V_{CS}' = V_{CBL}' = \frac{V_{CS} \cdot C_S + V_{CBL} C_{BL}}{C_S + C_{BL}}$

$= \frac{0.33 + 0.6 \cdot 520}{33 + 520} \approx 0.5642V$

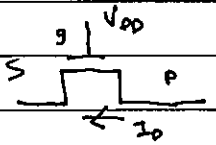
BL voltage swing: $V_{CBL} \rightarrow V_{CBL}' \Leftrightarrow 0.6V \rightarrow 0.5642$

* Read 1

When reading 1, C_S is storing logic 1 & thus $V_{CS} = V_{DD} - V_{tn} = 0.74V$

The mechanism is the same except that now it is discharging through NMOS to charge C_{BL}

∴ Note that C_S is charged to $V_{DD} - V_{tn}$ instead of V_{DD} when storing logic 1 because we are using NMOS instead of TG. NMOS will be off when $V_{out} \geq V_{DD} - V_{tn}$



when writing logic 1, I_D will flow from C_{BL} to C_S to charge the latter.

once V_S reached a value of $V_{DD} - V_{tn}$, NMOS will be off bcs $V_{gsn} = V_g - V_s = V_{DD} - (V_{DD} - V_{tn}) = V_{tn}$

$V_S > V_{DD} - V_{tn} \Rightarrow V_{gsn} < V_{tn}$

thus, we can see that max value of C_S is $V_{DD} - V_{tn}$

Initial voltage → $V_{CS} = 0.74V$ $V_{CBL} = 0.6V$

final voltage → $V_{CS}' = V_{CBL}' = \frac{0.74 \cdot 33 + 0.6 \cdot 520}{33 + 520} \approx 0.6084V$

BL voltage swing: $0.6V \rightarrow 0.6084V$

* Sense amplifier is used to detect the small voltage changes of ΔV when reading operation is performed in 1-T DRAM. It is through the positive feedback effect.

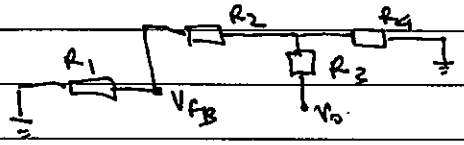
2 (b) (i) * FB Topology

ip: voltage mixing (series mixing) } series-shunt

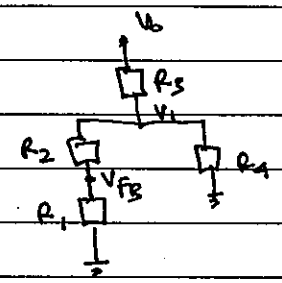
op: voltage sampling (shunt sampling)

* β

FB network :



re-draw



$\beta = \frac{V_{FB}}{V_o}$

$\frac{V_{FB}}{V_1} = \frac{R_1}{R_1+R_2}$

$\frac{V_1}{V_o} = \frac{R_p}{R_p+R_3}$ $\quad R_p = (R_1+R_2) \,//\, R_4$

$= \frac{(R_1+R_2) \,//\, R_4}{(R_1+R_2) \,//\, R_4 + R_3}$

$\beta = \frac{V_{FB}}{V_o} = \frac{V_{FB}}{V_1} \cdot \frac{V_1}{V_o} = \frac{R_1}{R_1+R_2} \cdot \frac{(R_1+R_2) \,//\, R_4}{(R_1+R_2) \,//\, R_4 + R_3}$

key in the value → $R_p = (7+53) \,//\, 60 = 60 \,//\, 60 = 30\,k\Omega$

$\beta = \frac{7}{60} \cdot \frac{30}{30+70} = 0.035$ V/V

(ii) $A_v = \frac{A}{1+A\beta}$

$A = \infty \rightarrow A_v \simeq \frac{1}{\beta} = \frac{1}{0.035} = 28.57$ V/V

$A = 10^4 \rightarrow A_v = \frac{10^4}{1+10^4 \cdot 0.035} = 28.49$ V/V

(iii) Gain desensitivity formula:

$\frac{dA_v}{A_v} = \frac{1}{1+A\beta} \cdot \frac{dA}{A}$

$\%A_v = \frac{1}{1+A\beta} \%A$ (G) $\quad \%A = (1+A\beta) \cdot \%A_v$

$= (1+10^4 \cdot 0.035) \cdot 0.5\% = 175.5\%$

for your reference only

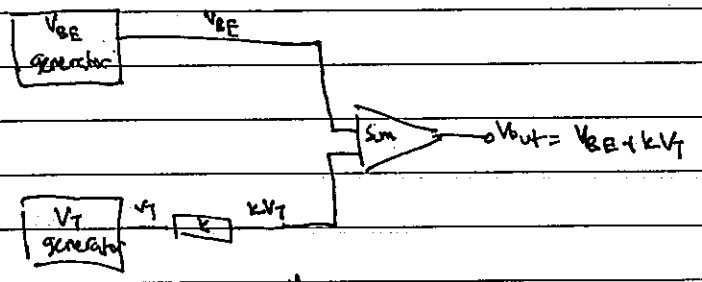
(c) The physical mechanism might vary on different type of amplifier However, the general cause of the ↓ in A_F of (-) FB @ f_{high}:

1. C_{out} can't be regarded as OC anymore & thus it will decrease ... the output impedance, thereby reducing the amplifier gain ($A = g_m R_o$)
2. gain of active components inside the amplifier decrease as f ↑, thus reducing OL gain & will reduce CL gain accordingly
3. other parasitic losses inside the internal structure of amplifier

3. (a) (i) $TC_F(V_{ref}) = \frac{1}{V_{ref}} \frac{\partial V_{ref}}{\partial T}$

(ii) $S_{V_{CC}}^{V_{ref}} = \frac{V_{CC}}{V_{ref}} \frac{\partial V_{ref}}{\partial V_{CC}}$

(b) • block diagram



→ how TC_F & $S_{V_{CC}}^{V_{ref}}$

$TC_F(V_{BE})$: (-)

$TC_F(V_T)$: (+)

when combined with proper weightings, TC_F of both around reference will tend to cancel off, decreasing TC_F value

• On the other hand, the key point that enables V_{ref} to be less dependent on V_{CC} is the fact that it is using (-) FB op-amp which will force $V_+ = V_-$ irrespective of supply. I_{R_1} & I_{R_2} will adjust their value to achieve this.

3 (c) $V_+ = V_-$

$$V_{CC} - I_{R_2} \cdot R_2 = V_{CC} - I_{R_1} R_1$$

$$\frac{I_{R_1}}{I_{R_2}} = \frac{R_2}{R_1}$$

neglect I_B & I_{offset} → $I_{R_3} = I_{R_1}$, $I_{T_1} = I_{R_1}$, $I_{T_2} = I_{R_2}$

KVL → $V_{BE_2} = V_{BE_1} + V_{R_3}$

$$V_T \ln\left(\frac{I_{T_2}}{I_{S_2}}\right) = V_T \ln\left(\frac{I_{T_1}}{I_{S_1}}\right) + I_{R_3} \cdot R_3$$

$$V_T \ln\left(\frac{I_{T_2}}{I_{T_1}} \cdot \frac{I_{S_1}}{I_{S_2}}\right) = I_{R_3} \cdot R_3$$

$$V_T \ln\left(\frac{I_{R_2}}{I_{R_1}} \cdot \frac{I_{S_1}}{I_{S_2}}\right) = I_{R_1} \cdot R_3$$

$$I_{R_1} = \frac{V_T}{R_3} \ln\left(\frac{R_1}{R_2} \cdot \frac{I_{S_1}}{I_{S_2}}\right)$$

$$I_{R_2} = \frac{R_1}{R_2} I_{R_1} = \frac{R_1}{R_2} \frac{V_T}{R_3} \ln\left(\frac{R_1}{R_2} \cdot \frac{I_{S_1}}{I_{S_2}}\right)$$

KVL → $V_{ref} = V_{BE_1} + I_{R_1} \cdot R_3$

$$= V_{BE_1} + \ln\left(\frac{R_1}{R_2} \cdot \frac{I_{S_1}}{I_{S_2}}\right) V_T$$

(d) In my opinion, it is not practically appropriate since BJT will have base current & thus increase the offset current of op-amp. I would suggest to use MOSFET as the input stage of op-amp to reduce the offset (note that the V_{ref} equation is enabled by the assumption that $I_{offset} = 0$. The higher the offset will make our output equation deviates from the desired one).

The amplifier can be changed to those of hybrid-type of MOSFET & BJT (expensive, but high gain) or full MOSFET (cheap, but relatively low gain)

for your reference only

4. (a) M_6 → input transistor for the 2nd gain stage

I_g → Current mirror to give current to the biasing transistor, also act as active load for M_8

(b) $A_{E_g} = A_{E_{10}} \Rightarrow I_{S_{T_g}} = I_{S_{T_0}}$

KVL → $V_{DD} - (-V_{DD}) = I \cdot R + V_{BE_{on}}$

$10 = I \cdot 465k + 0.7$

$I = 0.02\ mA$

$I_{T_{10}} = I = 0.02mA$

$V_{BE_g} = V_{BE_{10}} \rightarrow I_{T_g} = I_{T_{10}} = 0.02mA$

$I_{m_8} = I_{T_g} = 0.02\ mA$

$I_{m_5} = \frac{(\frac{W}{L})_5}{(\frac{W}{L})_8} \cdot I_{m_8} = 2 \cdot I_{m_8} = 0.04mA$

$I_{m_1} = I_{m_2} = \frac{I_{m_5}}{2} = 0.02mA$

$I_{m_4} = I_{m_3} = I_{m_1} = 0.02mA$

$I_{m_7} = I_{m_5} = 0.04mA$

$I_{m_6} = I_{m_7} = 0.04mA$

Summary:

Transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	T_g	T_{10}
Current (mA)	0.02	0.02	0.02	0.02	0.04	0.04	0.04	0.02	0.02	0.02

(c) * gain calculation

$A_{v_1} = -g_{m_2} \cdot (r_{o_2} // r_{o_4})$

$g_{m_2} = \frac{2 \cdot |I_D|}{|V_{GS} - V_t|} = \frac{2 I_D}{\sqrt{\frac{2 I_D}{\mu_p C_{ox} (\frac{W}{L})}}} = \sqrt{2 I_{m_2} \mu_p C_{ox} (\frac{W}{L})_2}$

$g_{m_2} = \sqrt{2 \cdot 20\mu \cdot 15\mu \cdot \frac{50}{4}} = 86.6\mu S$

$r_{o_2} = \frac{V_A}{I_{m_2}} = \frac{50}{0.02m} = 2.5M\Omega$

$r_{o_3} = \frac{V_A}{I_{m_3}} = 2.5M\Omega$ $\quad A_{v_1} = -108.25\ V/V$

ALL THE BEST FOR YOUR EXAMINATION!

for your reference only

* stability analysis

$a_0 = A_V = A_{V1} \cdot A_{V2} = -108.25 \times 500 = -54,125$

$$a(jw) = \frac{a_0}{\left(1+j\frac{w}{w_1}\right)\left(1+j\frac{w}{w_2}\right)\left(1+j\frac{w}{w_3}\right)}$$

$w_1 = 10\ kHz = 0.01\ MHz$

$w_2 = 1\ MHz$

$w_3 = 100\ MHz$

$$a(jw) = \frac{54,125}{\left(1+j\frac{w}{0.01}\right)\left(1+j\frac{w}{1}\right)\left(1+j\frac{w}{100}\right)} \quad (w \text{ in } MHz)$$

phase margin:

1. $\therefore |a(jw)| = 1$

$$\frac{54,125}{\sqrt{\left(1+\left(\frac{w}{0.01}\right)^2\right)\left(1+\left(\frac{w}{1}\right)^2\right)\left(1+\left(\frac{w}{100}\right)^2\right)}} = 1$$

rough approx → ignore +1

$$54,125^2 = \left(\frac{w}{0.01}\right)^2 \cdot (w)^2 \left(\frac{w}{100}\right)^2 \Leftrightarrow w = 37.83\ MHz$$

iteration

w (MHz)	Square root right	$\lvert a(jw)\rvert$
37.83	153,062	0.3536
30	94,015	0.5757
25	64,475	0.8395
23	54,332	0.9962

$w \simeq 23\ MHz$. (approximation only)

2. $\angle T(jw) = -\left(\tan^{-1}\left(\frac{w}{w_1}\right) + \tan^{-1}\left(\frac{w}{w_2}\right) + \tan^{-1}\left(\frac{w}{w_3}\right)\right)$

$$= -\left(\tan^{-1}\left(\frac{23}{0.01}\right) + \tan^{-1}(23) + \tan^{-1}\left(\frac{23}{100}\right)\right)$$

$$= -190.44^\circ$$

3. Reduce: $w = -190.44^\circ < -180^\circ \rightarrow$ unstable

(d) High PSRR → supply independent

To make it supply independent, I will change the biasing circuit to bootstrap bias circuit configuration. However, the drawback of this proposed design is that it will occupy larger area since it requires startup circuit & more transistors are used. It will also be more expensive.