NANYANG TECHNOLOGICAL UNIVERSITY

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

ACADEMIC YEAR 2022-2023

SEMESTER 1

EE3013 SEMINCONDUCTOR DEVICES AND PROCESSING

Week 7

Thermal Oxidation

1. A silicon dioxide layer was grown at 1000°C under steam oxidation on (111) Si for 120-min. Given that A =0.226 µm and B = 0.287 µm^2/hr. Assume that the wafer initially had 100nm of oxide layer, calculate the thickness of the oxide. [Ans. 0.67µm]

2. A silicon wafer has a 2000Å oxide on its surface. The wafer is put back in the furnace in wet oxygen at 1000°C. How long will it take to grow an additional 3000Å of oxide? [Ans. 0.968 hrs].

4.1 Dry oxidation coefficients for silicon

	Dry		Wet (640 torr)	
Temp (°C)	***A*** **(µm)**	***B*** **(µm^2/hr)**	***A*** **(µm)**	***B*** **(µm^2/hr)**
800	0.370	0.0011	—	—
920	0.235	0.0049	0.50	0.203
1000	0.165	0.0117	0.226	0.287
1100	0.090	0.027	0.11	0.510
1200	0.040	0.045	0.05	0.720

3. In an oxidation process the growth rate was monitored during the oxide-growth. When the oxide-thickness was 0.5µm and 1µm the growth rate was determined to be 0.135µm/hr and 0.081µm/hr, respectively. Determine the linear rate constant (B/A) and the parabolic rate constant (B).
[Ans. B = 0.2025 µm^2/hr. (B/A) = 0.405 µm/hr]

4. A p-type <100> Si wafer is placed in a wet oxidation system to grow a field oxide of 5000 A at 1000^{o}C. Determine the time required. After this step, a window is opened in the oxide layer to grow a gate oxide at 1200^{o}C for 12 min. by dry oxidation. Find the thickness of the gate oxide and the total field oxide. Oxide growth rates can be obtained from the charts given in *Lecture Notes*
   [Ans. t =1.3 hr; gate oxide=0.08 μm and total thickness=0.5086 μm]

5. A silicon wafer with the profile as shown in below is placed in a dry oxidation system at 1100^{o}C. Determine the time required to grow an oxide layer of 0.2 μm thickness on the exposed <100> silicon surface. What is the thickness of the additional oxide grown on the existing SiO_2 layer for the same period of time? Draw the resultant profile after the oxidation.
   [Ans. 2.15 hr; 0.1 μm]

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Week 8

Diffusion

1. (a) If arsenic is diffused into a thick slice of silicon doped with $1x10^{15}$ boron atoms/ cm^3 at a temperature of 1100˚C for 3 hr, what is junction depth if the surface concentration is held constant at $4x10^{18}$ atoms/cm^{-3} ? $D_{As}=3x10^{-14}cm^2/s$ at 1100˚C. You may use Error Function table in *Lecture Notes*

   (b) If the diffusion temperature is lowered to 900˚C, what is the junction depth? $D_{As}=1x10^{-16}cm^2/s$ at 900°C.
   [Ans. (a) x_j =0.93 µm (b) 0.054 µm]

2. A pn junction with a junction depth of 2µm is formed by diffusing pre-deposited boron atoms into the n-type silicon substrate at 1150°C for 1 hr. The dose for the pre-deposited boron atoms is 3×10^{13} boron atoms/cm^2. Assuming that the diffusion is Gaussian, find the doping of the n-type silicon substrate. Given that $D_B=9.2\times10^{-13}cm^2/s$ at 1150°C.

3. In a diffusion step $2.25x10^{13}$ boron atoms/cm^2 were deposited on the surface of a silicon slice. The slice was subsequently placed in a diffusion furnace tube at 1145°C for 2 hr. The n-type substrate had an impurity concentration of $1x10^{16}cm^{-3}$. Assuming that the diffusion is Gaussian, find the depth of the p-n junction in micrometers. $D_B=9.2x10^{-13}cm^2/s$ at 1145°C.
   [Ans. x_j =2.7 µm]

4. An emitter-base junction is formed by diffusing n-type phosphorous atoms into p-type silicon for 1 hr at 1000°C. The phosphorous concentration at the silicon surface is maintained at the limit of solid solubility. Assuming that the base has a uniform p-type background concentration of $1x10^{17}$ atoms/cm^{-3}, locate the emitter-base junction. If the emitter diffusion is performed at 900°C, determine the diffusion time for obtaining the same junction depth. Solid solubility of P in Si is suitably assumed. $D_P=1x10^{-15}cm^2/s$ at 900°C and $3x10^{-14}cm^2/s$ at 1000°C.
   [Ans. x_j = 0.575 µm. t=33.2 hours]

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Week 9

Ion-Implantation

1. Boron is implanted with an energy of 60 keV through a 0.25μm layer of silicon dioxide. The implanted dose is $1x10^{14}$ cm^{-2}. Find the boron concentration at the silicon-silicon dioxide interface if the straggle range ΔR_p is 0.09μm and the projected range R_p is 0.19μm.

   [Ans. $3.5x10^{18}$ cm^{-3}]

2. A 200 mm-silicon wafer is implanted with P^+ ions at 100 KeV for 5 seconds. If the average current measured is 10 μA, find
   (a) the dose
   (b) the maximum dopant concentration, and
   (c) the depth at which the maximum dopant concentration occurs
   (d) If a p-n junction is located at 0.3 μm, what is the background dopant concentration of the wafer? Sketch the dopant profile, and verify if there is one more p-n junction!

   Use the charts (*Lecture Notes)* to determine the approximate values of R_p and $\Delta R_{p.}$

   [Ans: (a) ≈ $1x10^{12}cm^{-2}$, (b) $8.9x10^{16}cm^{-3}$, (c) 0.14μm, d) $1.6x10^{14}cm^{-3}$]

3. We wish to implant double-ionized boron into 0.25 μm oxide-covered n-type <100> silicon wafer with a background concentration of $1x10^{15}$ atoms/cm^3. The dose is $2x10^{13}cm^{-2}$, and the acceleration voltage used is 150 KV. Sketch the doping profile, and locate the p-n junctions, if any. Determine the amount of boron atoms that ended up inside the silicon wafer. You may assume that, for boron: R_p in Si = R_p in SiO_2, and ΔR_p in Si = ΔR_p in SiO_2. Values of R_p and ΔR_p can be taken from the graphs provided in the *Lecture Notes*.

   [Ans: x_{j1}=0.334 μm, x_{j2}=1.066μm, ≈$2.0x10^{13}cm^{-2}$]

4. Boron was implanted into an n-type oxide-covered silicon wafer with a background concentration of $1x10^{15}cm^{-3}$. The oxide thickness was 0.6 µm and the ion dose used was $2x10^{13}$ atoms/cm^2. After implantation the wafer was annealed at 1050°C for 30 minutes to activate the implanted ions. Assume that the values of projected range and straggle are same for B in Si and the oxide. Given R_p=700nm and ΔR_p=100nm, Diff. Coeff. of B =$5x10^{-14}cm^2/s$ at 1050°C

   (i) Calculate the peak concentration of the implanted profile and the junction depths from the wafer surface. Draw the schematic of the dopant profile

   (ii) Calculate the peak concentration and the projected straggle after annealing. Does the peak location change after annealing?

   (iii) Find the required thickness of the oxide before and after annealing if the maximum concentration of B in Si is at most 10% of the background concentration.

   [Ans: $7.97x10^{17}cm^{-3}$, x_{j1} = 0.334 µm, x_{j2} = 1.066 µm, $4.77x10^{17}cm^{-3}$, 0.167 µm, 1.12 and 1.38 µm]

5. An arsenic dose of $1x10^{12}$ cm^{-3} is implanted through a 50 nm layer of silicon dioxide with the peak of the distribution at the Si-SiO_2 interface. The straggle range ΔR_p is 0.017µm. A silicon nitride film on top of the silicon oxide is to be used as a barrier material in the regions where arsenic is not desired. How thick should the nitride layer be if the background concentration is $1x10^{15}$ cm^{-3}? Assume silicon oxide is only 85% effective in stopping ions as compared to silicon nitride.

   [Ans. $1.44x10^{16}$ cm^{-3}]

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Week 11

Recap of PN Junctions

1. An abrupt junction silicon p-n diode has a p-layer acceptor doping density of 10^{18} cm^{-3} and n-side donor doping density of 10^{15} cm^{-3}. Assume that the dopants are fully ionized. For this junction in equilibrium at 300 K:
   (a) Computer the position of the Fermi level (with respect to the conduction band edge) on both sides of the junction.
   (b) Sketch the band diagram (with the energy axis drawn to scale) and estimate the built-in potential.
   (c) Computer V_{bi} directly from the doping densities and the intrinsic concentration, and compare the result with that from part (b).
   (d) Calculate the widths of the depletion regions on either side of the junction.
   (e) Calculate the maximum electric field in the depletion region.
   (Ans. (a) -0.265 eV and -0.085 eV; (c) 0.776 eV; (d) 9.99 x 10^{-4} μm and 0.999 μm; (e) -1.52 x 10^{4} V/cm)

2. Consider a uniformly doped abrupt pn junction at 300 K. At thermal equilibrium, it is designed such that 10 % of the total depletion width region lies in the p region. You are given that the built in potential is 0.8 V. Determine the doping concentration N_a and N_d of the p and n region, respectively, and the total depletion width.
   (Hint: Consider charge neutrality and x_{n0} + x_{p0} = W to relate N_a and N_d. You can relate N_a and N_d via the expression for V_{bi}. Then, solve the two equations.)
   [Ans: 2.59×10^{16} cm^{-3}; 2.33×10^{17} cm^{-3}; 0.212 μm]

3. Assume that the p-n abrupt junction has $N_A = 10^{17}$ cm^{-3} and $N_D = 10^{15}$ cm^{-3}, (a) Find the V_{bi} at 250 and 500 K. *T.* (b) Comment on your result in terms of energy band diagram. (c) Find the depletion layer width and maximum field at zero bias for T = 500 K.
   Assume that the intrinsic carrier concentrations at 250 and 500 K are 1.5 x 10^{8} cm^{-3} and 2.2 x 10^{14} cm^{-3} respectively.
   (Ans. (a) 0.777 V and 0.329. (c) 0.658 μm and 10^{4} V/cm)

4. A one-sided p-n junction at 300 K is doped with $N_A = 10^{19}$ cm^{-3}, Design the junction so that Cj = 8.5 nF at a reverse voltage of 4 V.
   (Ans. $N_D = 3.43 \times 10^{15}$ cm^{-3}.)

5. Design the Si p-n diode such that J_n = 25 A/cm^{-2} and J_p = 7 A/cm^{-2} at V_a = 0.7 V. Other parameters are as follows: $n_i = 9.65 \times 10^9$ cm^{-3}, D_n = 21 cm^2/s, D_p = 10 cm^2/s and $\tau_n = \tau_p = 5 \times 10^{-7}$ s. Assume that J_p and J_n are given by expressions of the form $(qD_p p_{no}/L_p).(e^{qV/kT} - 1)$ and $(qD_n n_{po}/L_n).(e^{qV/kT} - 1)$ respectively
   (Ans. $N_D = 5.2 \times 10^{15}$ cm^{-3} and $N_A = 2.111 \times 10^{15}$ cm^{-3}.)

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Week 12

Bipolar Junction Transistors (BJTs)

1. Draw the energy band diagram for an n^+pn transistor for the following cases: (a) thermal equilibrium, (b) active mode, (c) cut off mode, (d) saturation mode.

2. A *pnp* transistor has a base transport factor α_T of 0.998, and emitter efficiency of 0.997, and an I_{Cn} of 10 nA. (a) Calculate α_0 and β_0 for the device. (b) If I_E = 1 mA, what is the total collector current?
[Ans: 0.995, 199, 0.99501 mA]

3. A silicon *pnp* transistor has impurity concentrations of 5 x 10^{18}, 2 x 10^{17}, and 10^{16} cm^{-3} in the emitter, base, and collector, respectively. The base width is 1.0μm, and the device cross-sectional area is 0.2 mm^2. When the emitter-base junction is forward biased to 0.5 V and the base-collector junction is reverse biased to 5 V, calculate
(a) the neutral base width
(b) the minority carrier concentration at the emitter-base junction.
(c) if the diffusion constants of minority carriers in the emitter, base, and collector are 52, 40, and 115cm^2/s, respectively; and the corresponding lifetimes are 10^{-8}, 10^{-7}, 10^{-6} s. find the current components I_{Ep}, I_{Cp}, I_{En}, I_{Cn}, and I_{BB} .
(d) Hence find the terminal currents I_E, I_C, and I_B of the transistor and calculate emitter efficiency, base transport factor, common-base current gain, and common-emitter current gain;
(e) comment on how the emitter efficiency and base transport factor can be improved.
[Ans: (a) 0.904 μm (b) 2.543x10^{11} cm^{-3} (c) I_{Cp} = I_{Ep} = 1.596x10^{-5} A, I_{En} = 1.041x10^{-7}A, I_{Cn} = 3.196x10^{-14} A (d) I_E = 1.606x10^{-5}A, I_C = 1.596x10^{-5}A, I_B = 1.041x10^{-7} A, 0.9938, 1, 0.9938, 160.3]

4. A Si *pnp* bipolar transistor has impurity concentrations of 3x10^{18}, 2x10^{16} and 5x10^{15} cm^{-3} in the emitter, base and collector regions. The mobilities of electrons and holes are assumed to be expressed by
$\mu_n = 88 + \frac{1252}{\left(1 + 0.698x10^{-17} N\right)}$ cm^2/V.s and $\mu_p = 54.3 + \frac{407}{\left(1 + 0.374x10^{-17} N\right)}$ cm^2/V.s

   Assuming T = 300K, determine the Diffusion coefficients of minority carriers in the three regions respectively. [Ans. 3.755 cm^2 /s, 11.21 cm^2 /s, 33.6 cm^2 /s]

5. In a Si *npn* transistor at 300 K, the impurity concentrations are 10^{18}, 3×10^{16} and 5×10^{15} cm^{-3} in the emitter, base, and collector, respectively. Assume $D_B = 20$ cm^2/s and $\tau_{BO} = 5\times10^{-7}$ s and let $V_{BE} = 0.7$ V. Assume $V_{CB} = 5$ V and 10 V as two data points.
   (a) Find collector current density as a function of neutral base (ignore J_{Cp}).
   (b) Find neutral base at 5 V and 10 V, respectively.
   (c) Estimate the early voltage for metallurgical base width of 1 μm.

   [Ans: $J_C = 5.44 \times 10^{-3}/W$, 0.812 μm (5V), 0.743 μm (10V)]

6. (a) A Si transistor has D_p of 10 cm^2 and W of 0.5 μm. Find the cut-off frequencies for the transistor with a common base current gain of 0.998. Neglect the emitter and collector delays.
   (b) To design a bipolar transistor with 5 GHz cut-off frequency. What the neutral base width *W* will be?

   [Ans: (a) $f_T = 1.27$ GHz and $f_\beta = 2.55$ MHz; (b) 0.252 μm]

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Week 13

MOS Devices

1. (a) For an ideal metal-SiO_2-Si diode having $N_A = 10^{17}$ cm^{-3} (p-type semiconductor), calculate the maximum width of the surface depletion region, corresponding to the onset of strong inversion. Assume $kT/q = 0.0259$ V, and $n_i = 9.65 \times 10^9$ cm^{-3} and permittivity of Si is $11.9 \times 8.85 \times 10^{-14}$ F/cm. [Ans. 0.105 μm]

   (b) If the oxide thickness is 5 nm, determine the capacitance C_o for the diode. Also calculate the minimum capacitance for the MOS. Determine the difference ($E_i - E_F$) for the semiconductor far away from the interface. Estimate the threshold voltage V_T for the MOS structure. Assume that the relative dielectric constant for the oxide is 3.9.

   [Ans. W_m = 0.105 μm; = 6.90×10^{-7} F/cm^2, $C_{min} = 8.76 \times 10^{-8}$ F/cm^2, $E_i - E_F = q.\ \psi_B = 0.42$ eV, V_T=1.08 V]

2. Calculate the flat band voltage for an n^+-polysilicon-SiO_2-Si diode having $N_A = 10^{17}$ cm^{-3}, oxide thickness d = 5 nm. Assume that $\phi_{ms} = -0.98$ V for the (n^+ polysilicon) – (p-Si) system, Q_m and Q_{ot} are negligible and $Q_f/q = 5 \times 10^{11}$ cm^{-2}. [Ans. V_{FB} = -1.096 V]

3 An enhancement type NMOS transistor with V_{TH} = 2 V has its source grounded and a 3 V supply connected to the gate. In what region does the device operate for (a) V_D = 0.5 V? (b) V_D = 1.0 V? (c) V_D = 5.0 V? If the device parameters are $\mu_n C_{ox}$ = 20 μA/V^2, Z = 100 μm and L = 10 μm, calculate the drain current for each of the cases.

   [Ans. (a) linear region I_D = 75 μA; (b) pinch-off point I_D = 100 μA; (c) Saturation region I_D = 100 μA]

4. An enhancement PMOS transistor has K_p = 80 μA/V^2 and V_T = -1.5 V. The gate is connected to -5 V and the source to ground. Find the drain current for (a) V_D = -1 V, (b) V_D = -2 V and (c) V_D = -5 V. [Ans. 120 μA, 160 μA and 160 μA]

5. For an ideal MOS diode fabricated on a n-Si substrate:

   (i) Sketch the energy band diagrams when it is in (i) accumulation, (ii) depletion, and (iii) inversion. Indicate E_c, E_v, E_i and E_f in the diagrams.

   (ii) Sketch the high-frequency capacitance versus voltage diagram and indicate the regions corresponding to (i) accumulation, (ii) depletion, and (iii) inversion.