## EE2073 week 6 Lab Report

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Lab: EJ26

For this experiment, with the various values we input for Vin and Vc, we will be able to obtain the Vout from the oscilloscope. Following this, we will measure the gain.

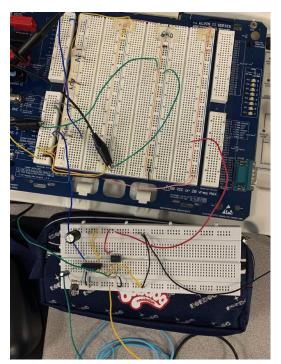


Fig 1: Circuit board

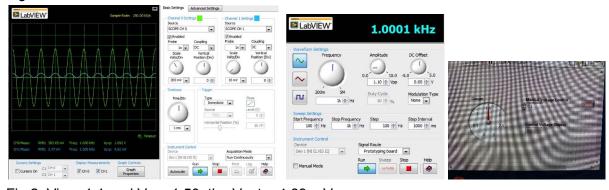


Fig 2. Vin = 1.1 and Vc = 1.50, the Vout = 4.89 mV.



Fig 3.

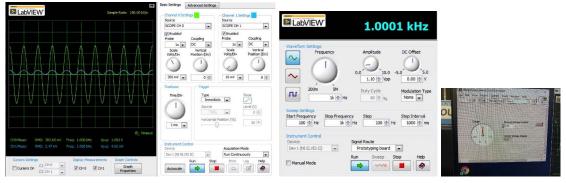


Fig 4.



Fig 5.



Fig 6



Fig 7



Fig 8.

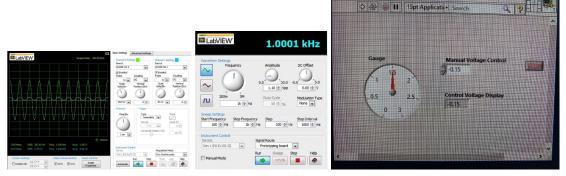


Fig 9.

Vin(Vpp)	Vc(V)	Vout(Vpp)	Measured Gain = (Vout / Vin)	Measured Gain (dB)	Theoretical Gain (dB)
1.2	0.5	0.00226	0.0188	-54.501	-82.03
0.5	0.35	0.00225	0.00451	-46.9	-59.016
0.52	0.18	0.018	0.0346	-29.215	-29.508
0.31	0.06	0.101	0.319	-9.931	-9.836
0.31	0	0.397	1.018	0.1545	0
0.16	-0.06	0.524	3.0823	9.777	9.836
0.17	-0.12	1.512	10.08	20.069	19.672
0.12	-0.15	2.003	16.691	24.45	24.59

Fig 10. Gain measured

The measurements are tabulated accordingly to Vin with reference to my matriculation number.

From the table above, it shows that as Vc decreases, Vout (Vpp) increases. Therefore from the table above, I can conclude that the gain increases inversely proportional to Vc. The measured gain can be further clarified by comparing it with the theoretical gain in dB. Both measured gain and theoretical gain are very similar; therefore the circuit is working as required. The tabulated results are then plotted accordingly as seen below.

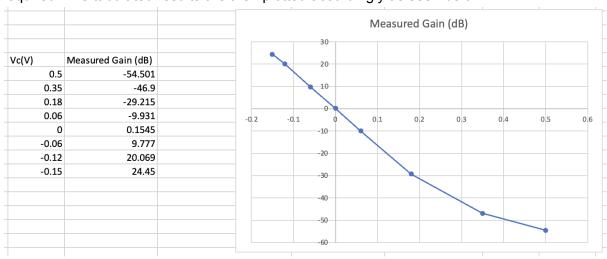


Fig 11. Graph of Measured Gain against Vc

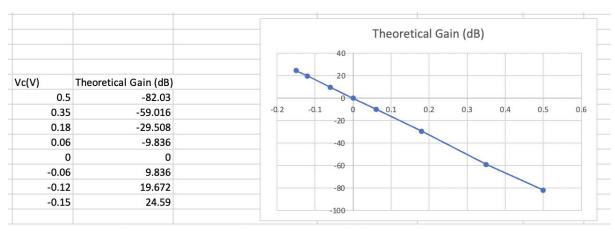


Fig 12. graph of Theoretical Gain against Vc

## **Open Ended Question**

## Please describe how the choice of input resistor will affect the distortion. Will there be a difference if the input resistor is replaced by a $1k\Omega$ one?

The choice of resistance will affect the amplifier distortion as output signal will get clipped if the bias level is too low or too high. Amplification may not be taking place over the whole signal cycle due to frequency distortion. The output signal will be smaller.