NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2013-2014

EE3019 – INTEGRATED ELECTRONICS

April / May 2014 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer ALL questions.
3. All questions carry equal marks.
4. This is a closed-book examination.
5. Unless specifically stated, all symbols have their usual meanings.

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1. (a) Draw the CMOS transistor-level circuit for the following Boolean function:

$$Y = \overline{(A + B) \cdot (C \cdot D + E)}$$

$\bar{Y} = (A+B)\,[CD+E]$

It is given that the $\left(\frac{W}{L}\right)$ ratios of the nMOS and pMOS transistors of a matched inverter are $\left(\frac{W}{L}\right)_n = \frac{90\text{nm}}{45\text{nm}}$ and $\left(\frac{W}{L}\right)_p = \frac{225\text{nm}}{45\text{nm}}$, respectively. Determine the $\left(\frac{W}{L}\right)$ ratio of each transistor such that the worst-case propagation delays, t_{pLH} and t_{pHL}, of the CMOS circuit are approximately equal to those of the matched inverter.

(12 Marks)

Note: Question No. 1 continues on page 2

(b) The nMOS transistor circuit shown in Figure 1 is fabricated using a process technology for which $\mu_n C_{ox}$ = 50 μA/V² and $\left(\frac{W}{L}\right)_n = \frac{90\text{nm}}{45\text{nm}}$. The V_{DD} is 5 V, V_{tn} = 1 V and C_L = 50 fF.

(i) V_{out} is at 5 V initially and V_{in} is changing from V_{DD} to 0 V at $t = 0$. Identify the regions of operation for the nMOS transistor when V_{out} is at 5 V and at 2.5 V, respectively.

(ii) Determine the propagation delay, t_{pHL}, of this circuit.

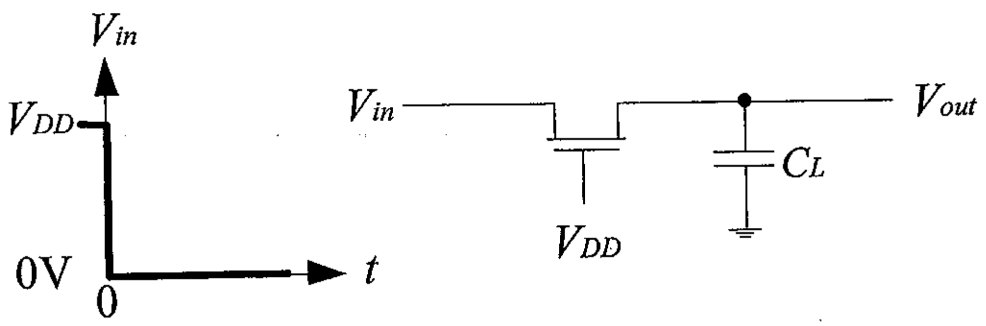

Figure 1

(10 Marks)

(c) What is the name of the nMOS circuit shown in Figure 1? List the advantage(s) and disadvantage(s) of this circuit over a CMOS transmission gate.

low static power dissipation

(3 Marks)

↳ only one on at a time

threshold.

2. (a) Draw the transistor-level schematic diagrams of a 3-T DRAM cell and a 6-T SRAM cell~~, and~~ clearly indicate their select and data lines. List an advantage and a disadvantage of DRAM and SRAM.

(10 Marks)

(b) Consider a 1-T DRAM cell of $V_{DD} = 5$ V. The bit-line pre-charge voltage is 0.5 V_{DD} and the bit-line capacitance is 0.3 pF. The voltages of the storage cell are V_{DD} for logic '1' and 0 V for logic '0', respectively. The positive voltage swing of the bit-line for a READ operation when an accessing stored data value of '1' is 0.34 V. Determine the storage capacitance of this DRAM cell.

(6 Marks)

(c) Derive the gain equation of a negative feedback amplifier and show that if the open-loop gain, A, is very large, the overall closed-loop gain can be computed as $A_f \approx \frac{1}{\beta}$, where β is the feedback gain. List the advantages of a negative feedback amplifier.

(7 Marks)

(d) Discuss the key requirements of the Op-amp for a practical negative feedback amplifier.

(2 Marks)

3. For the following CMOS Op-amp shown in Figure 2 on page 5, assume that:

- *All* the transistors are identical with ALL the design parameters being the same (including $\left(\frac{W}{L}\right)$, $|V_t|$, $|V_{GS}|$, I_B, and λ), and
- The Op-amp has a *single dominant pole.*

a) Write down the design equations for the following:

(i) Bias resistor R_B as a function of I_B, $\left(\frac{W}{L}\right)$, and V_t.

(ii) Low-frequency gain $\left(\frac{v_o}{v_i}\right)$. A

(iii) -3 dB frequency. $\omega_1 = \frac{1}{RC}$

(iv) Unity-gain frequency. $\omega_0 = A\omega_1$

(10 Marks)

b) Assume that the parameters for the transistors are $\mu_p C_{ox} = \mu_n C_{ox} = 100\ \mu A/V^2$, $V_{tp} = -0.8$ V, $V_{tn} = 0.8$ V and $\lambda_p = \lambda_n = 0.1\ V^{-1}$. In addition, $V_{DD} = 3$ V and $C_C = 10$ pF. Design the circuit parameters R_B, I_B, R_E, and $\left(\frac{W}{L}\right)$, to *SIMULTANEOUSLY* achieve the following specifications:

DC Gain	$\geq$ 300 V/V
Unity-Gain Frequency	$\geq$ 100 MHz
$V_{GS} - V_t$	$\geq$ 0.2 V
Drain Bias Voltage V_{D1} of M_1	2.6 V > V_{D1} > 2.0 V
Power Consumption	< 7 mW
C_C	10 pF

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)^2;\ g_m = \frac{2I_D}{V_{GS} - V_t}$$

(15 Marks)

Note: Question No. 3 continues on page 5

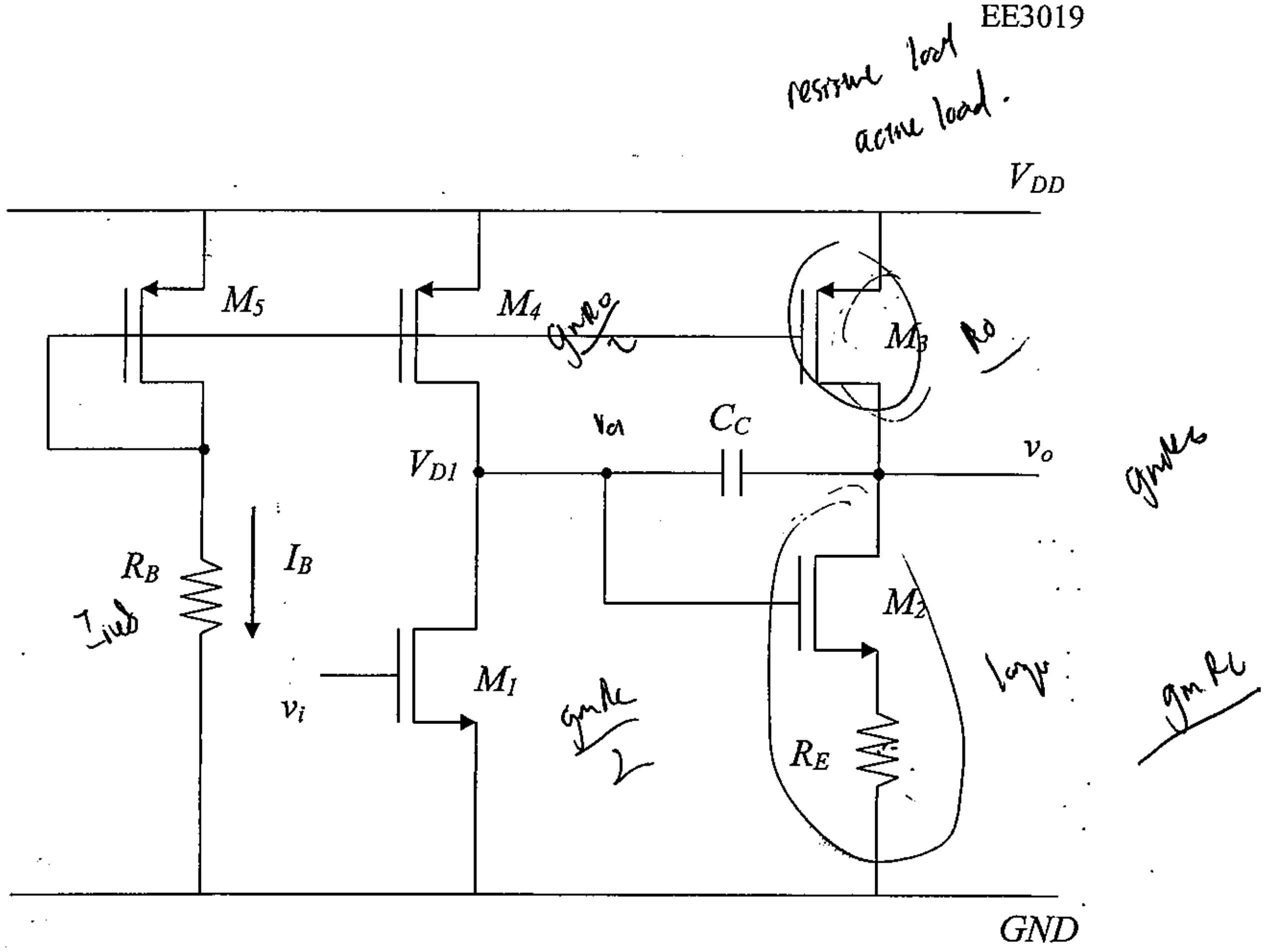
resistive load
active load.
V_{DD}
M_5
M_4
M_3
V_{D1}
C_C
v_o
R_B
I_B
M_2
v_i
M_1
R_E
GND

Figure 2

3

4. Bode plots of the open-loop gain $A(j\omega)$ of an Op-amp are shown in Figure 3 on page 7. Consider applying the amplifier in a feedback configuration with a *feedback gain* β.

$\rightarrow 40dB$

a) For a feedback gain $\beta = 0.01$, what are the phase margin (PM) and the gain margin (GM)?

(5 Marks)

b) What *would* be the feedback gain β for the system to achieve a phase margin of 90°?

(5 Marks)

c) For a feedback gain $\beta = 1$ with a *narrowbanding* compensation, where should the *new dominant pole be addded* to achieve a PM of 45°?

(5 Marks)

d) For a feedback gain $\beta = 1$ with an *improved* compensation, where should the *original first pole be moved* to achieve a PM of 45°?

(5 Marks)

e) For a feedback gain $\beta = 1$ with an *improved* compensation, if the *original* first pole is moved to 0.5 Hz, what would be the PM?

(5 Marks)

Note: Question No. 4 continues on page 7

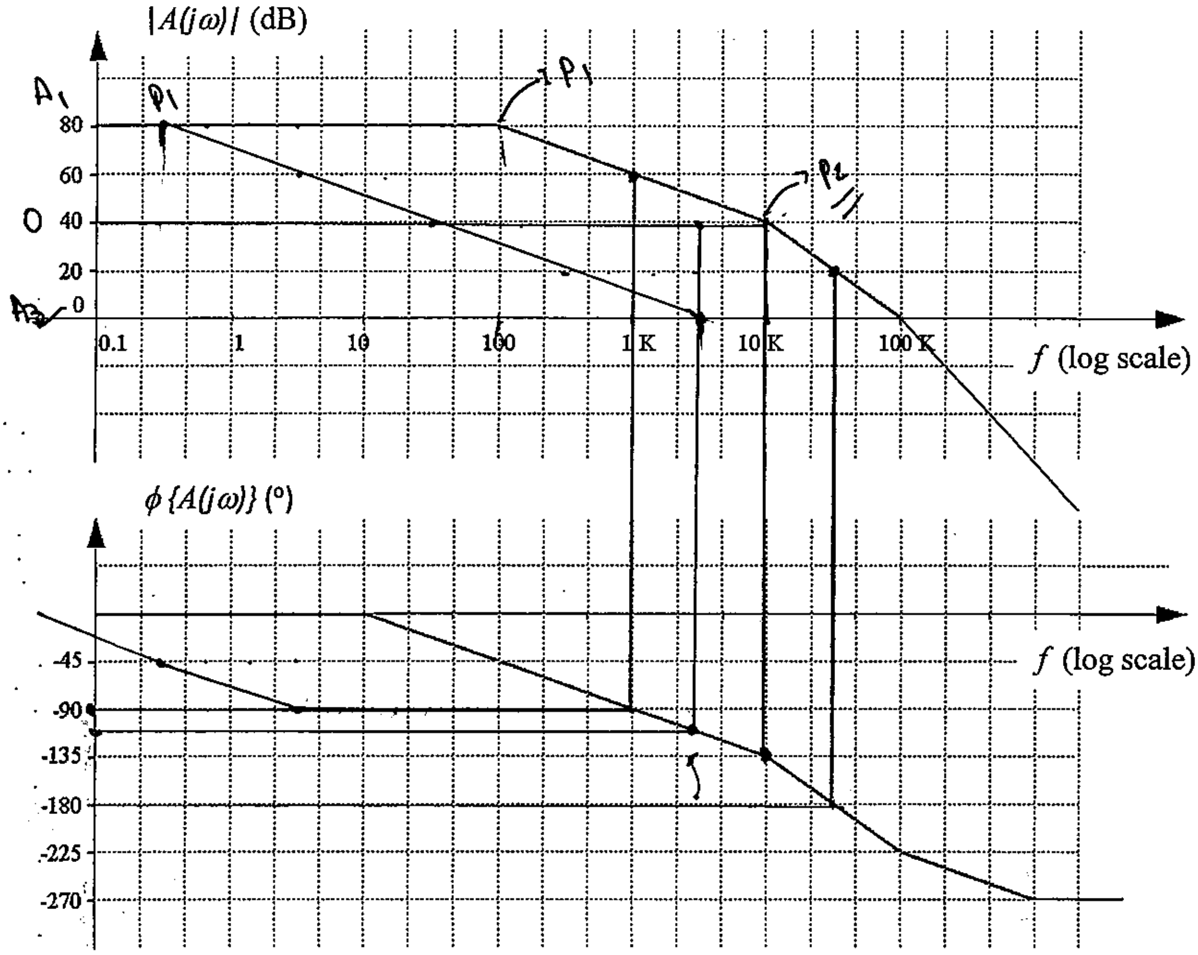

Figure 3

END OF PAPER

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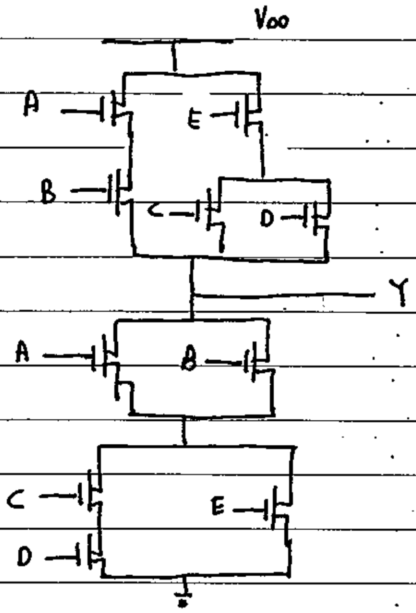
① (a) $Y = \overline{(A+B).(C.D+E)}$

$= [\bar{A}.\bar{B}] + [\bar{C}+\bar{D}.\bar{E}] \approx$ PMOS ~ PUN

$\bar{Y} = [A+B].[C.D+E] \approx$ NMOS ~ PDN

CMOS transistor-level circuit



Worse case, only one path, t_{PLH} ~ PMOS

$$\left[\frac{W}{L}\right]_{eq} = \frac{1}{\frac{1}{[\frac{W}{L}]_A} + \frac{1}{[\frac{W}{L}]_B}} = \frac{1}{\frac{1}{[\frac{W}{L}]_E} + \frac{1}{[\frac{W}{L}]_C}} = \frac{1}{\frac{1}{[\frac{W}{L}]_E} + \frac{1}{[\frac{W}{L}]_D}}$$

$$\therefore \left[\frac{W}{L}\right]_A = \left[\frac{W}{L}\right]_B = \left[\frac{W}{L}\right]_C = \left[\frac{W}{L}\right]_D = \left[\frac{W}{L}\right]_E = 2\left[\frac{W}{L}\right]_P$$

$$= 2\left[\frac{225nm}{45nm}\right] = \frac{450nm}{45nm}$$

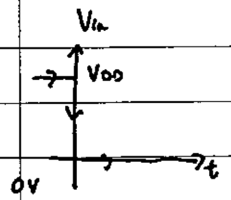
Worse case, only one path, t_{PHL}, ~ NMOS

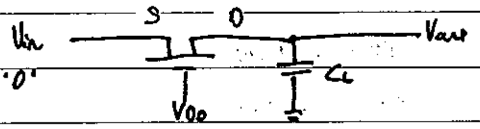
$$\left[\frac{W}{L}\right]_{eq} = \frac{1}{\frac{1}{[\frac{W}{L}]_A} + \frac{1}{[\frac{W}{L}]_C} + \frac{1}{[\frac{W}{L}]_D}} = \frac{1}{\frac{1}{[\frac{W}{L}]_A} + \frac{1}{[\frac{W}{L}]_E}} = \frac{1}{\frac{1}{[\frac{W}{L}]_B} + \frac{1}{[\frac{W}{L}]_C} + \frac{1}{[\frac{W}{L}]_D}} = \frac{1}{\frac{1}{[\frac{W}{L}]_B} + \frac{1}{[\frac{W}{L}]_E}}$$

$$\left[\frac{W}{L}\right]_A = \left[\frac{W}{L}\right]_B = \left[\frac{W}{L}\right]_E = 2\left[\frac{90nm}{45nm}\right] = \frac{180nm}{45nm}$$

$$\left[\frac{W}{L}\right]_C = \left[\frac{W}{L}\right]_D = \frac{360nm}{45nm}$$

① (b) $V_{DD} = 5V$ $V_{tn} = 1V$ $C_L = 50fF$ $[\frac{W}{L}]_n = \frac{90nm}{45nm}$





(i) Initially, $V_{out} = 5V$

when $V_{out} = 5V$,

$V_{GS} = V_{DD}$ $V_{DS} = V_{DD}$ [SAT]

when $V_{out} = 2.5V$

$V_{GS} = V_{DD}$, $V_{DS} = \frac{V_{DD}}{2}$

$V_{DS} \leq V_{GS} - V_{tn}$ [LIN].

(ii) $i_{D(5V)} = \frac{k_n}{2}[V_{GS} - V_{tn}]^2$

$= \frac{50\times10^{-6}}{2}\left[\frac{90}{45}\right][5-1]^2 = 800\mu A$

$i_{Dn(50\%)} = k_n[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}(V_{DS})^2]$

$= 50\times10^{-6}\left[\frac{90}{45}\right][(5-1)2.5 - \frac{1}{2}(2.5)^2]$

$= 687.5\mu A$

$i_{Dn(avg)} = \frac{800 + 687.5}{2} = 743.75\mu A$

$t_{PHL} = \frac{C \times \Delta V}{i_{avg}} = \frac{50\times10^{-15}\times 2.5}{743.75\times10^{-6}} = 16.8ns$

(c) 1-T DRAM cell.

↳ refresh more frequency
↳ More leakage
} Disadvantages

↳ smaller circuit area
↳ low static power dissipation
} Advantages

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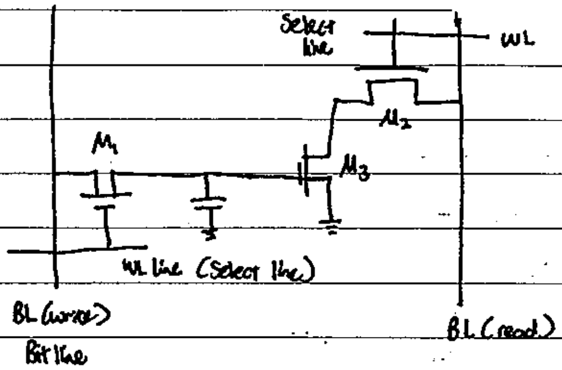
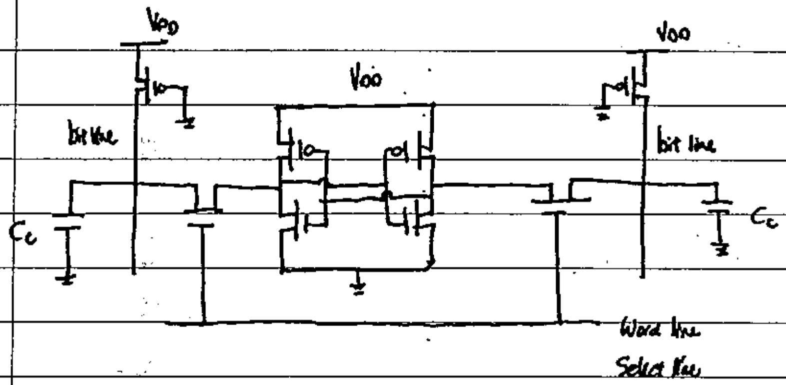
Date No.

(2) (a) 3-T DRAM



6-T SRAM



DRAM => Advantage => Smaller circuit area.

Disadvantage => More leakage ~ charge leak out faster

SRAM => Advantage => fastest memory, low static power dissipation.

Disadvantage => volatile memory ~ needs continuous power.

(b) 1-T DRAM $V_{DD} = 5V$ $C_d = 0.3pF$

$V + \Delta V = V_{cd} = V_{cs}$

$\Delta V = 0.34V$

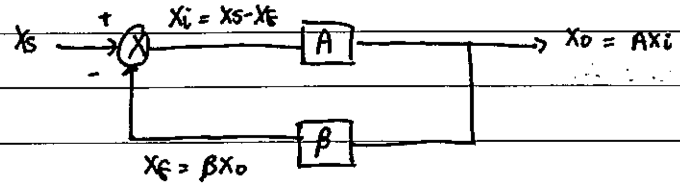
$V_{cd} = V_{cs} = 2.5 + 0.34 = 2.84V$

$$V_{cd} = V_{cs} = \frac{2.5 \times 0.3pF + 5 \times C_s}{0.3pF + C_s}$$

$0.852pF + 2.84 C_s = 0.75pF + 5C_s$

$C_s = 0.0472 pF$

(c)



$$\left.\begin{aligned} X_i &= X_s - X_f \\ X_o &= AX_i \\ X_f &= \beta X_o \end{aligned}\right\}$$

$$X_o = A(X_s - \beta X_o)$$
$$= AX_s - A\beta X_o$$
$$X_o(1 + A\beta) = AX_s$$
$$A_f = \frac{X_o}{X_s} = \frac{A}{1+A\beta}$$

when $A = \infty$

$$A_f \approx \frac{1}{\beta}$$

Advantages of a negative feedback amplifier

- Gain Desensitivity
- Reduced Frequency Distortion
- Noise Reduction
- Reduced Non-Linear Distortion.

(d) Self-stabilizing system.

③ (a) (i) R_B as a function of I_B, $(\frac{W}{L})$ and V_t.

$$R_B = \frac{1}{\lambda I_D} \qquad I_D = \frac{k}{2}\left[\frac{W}{L}\right]\left[V_{GS}-V_t\right]^2$$

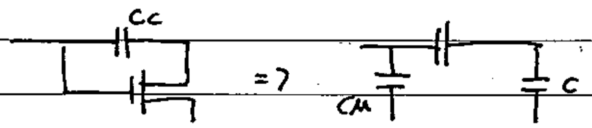
$$= \frac{1}{\lambda\left[\frac{k}{2}\left(\frac{W}{L}\right)\left(V_{GS}-V_t\right)^2\right]} = \frac{2}{\lambda\left[k\left[\frac{W}{L}\right]\left(V_{GS}-V_t\right)^2\right]}$$

(ii) $$A = \frac{V_o}{V_i} = \frac{V_{o1}}{V_{in}} \times \frac{V_o}{V_{o1}}$$

$$\frac{V_{o1}}{V_{in}} = \frac{g_m R_L}{2} \qquad \frac{V_o}{V_{o1}} = g_m R_L$$

$$A = \left[\frac{g_m R_L}{2}\right]\left[g_m R_L\right] = \frac{(g_m R_L)^2}{2}$$

(iii) $$\omega_1 = \frac{1}{RC}$$



$$R = \frac{R_L}{2}$$

$$C = C_c\left[1+g_m R_L\right]$$

$$\omega_1 = \frac{1}{\frac{R_L}{2} C_c\left[1+g_m R_L\right]}$$

$$= \frac{2}{R_L C_c\left[1+g_m R_L\right]}$$

(iv) $$\omega_0 = A\omega_1$$

$$= \left[\frac{(g_m R_L)^2}{2}\right]\left[\frac{2}{R_L C_c\left[g_m R_L\right]}\right]$$

$$= \frac{g_m}{C_c}$$

(b) $C_c = 10pF$ $V_{DD} = 3V$

$P = 3 I_B V_{DD}$

$6.5m = 3 I_B (3)$

$I_B = 0.722\,mA$ ~ let $I_B = 0.75mA$ ~ $P = 6.75mW$. [Checked]

$$g_m = \frac{2I_D}{V_{GS}-V_t} = \frac{0.722\times10^{-3}\times2}{0.2} = 7.22\,mA/V \qquad V_{GS}-V_t = 0.2V \text{ [Checked]}$$

$$\omega_0 = \frac{7.22\times10^{-3}}{10\times10^{-12}} = 722\,Mrad/s$$

$$f_0 = \frac{722\times10^6}{2\pi} = 115\,MHz \text{ ~ [Checked]}$$

$A = 300V/V$.

$$A = \frac{[g_m R_L]^2}{2}$$

$$R_L = \frac{\sqrt{2A}}{g_m} = \frac{\sqrt{2 \times 300}}{7.22 \times 10^{-3}}$$

$$= 3392.65\ \Omega$$

$$g_m = \mu C_{ox} \left[\frac{W}{L}\right][V_{GS} - V_t]$$

$$7.22 \times 10^{-3} = 100 \times 10^{-6} \left[\frac{W}{L}\right][0.2]$$

$$\left[\frac{W}{L}\right] = 361$$

$$I_B = 0.722\,mA$$

$$R_E = \frac{V_{o1}}{I_B} = \frac{2.3}{0.722 \times 10^{-3}}$$

$$= 3185.6\ \Omega$$

$$R_B = \frac{2}{\lambda [k (\frac{W}{L})(V_{GS} - V_t)^2]} \qquad \lambda_n = \lambda_p = 0.1\,V^{-1}$$

$$= \frac{2}{0.1 [100 \times 10^{-6} (361)(0.2)^2]}$$

$$= 13.85\ k\Omega$$

* Take note, this is a design question. there is no exact solutions / answers. Have to meet all the specifications

4 (a) $\beta = 0.01$

$\cancel{20 \log \frac{1}{\beta} = 40dB}$

From the graph, $GM = -20dB$ $GM < 1$

$PM = -135° + 180°$

$= 45°$ $PM > 0$

Hence, system is stable.

(b) $PM = 90°$

$20 \log \frac{1}{\beta} = 60dB$

$\beta = 0.001$

(c) $\beta = 1$, Narrow banding compensation.

$P_0' = P_2' \frac{A_3}{A_1} = P_1 \frac{A_3}{A_1}$

$\cancel{PM = 45°}$

$\omega_0 = \omega_z = 100Hz$ $A_3 = 1$

$\omega_0 = A\omega_p$ $A_1 = 80dB$

$= 0.0001$

$A = \frac{A_3}{A_1} = \frac{1}{0.0001} = 10000$

$\omega_p = \frac{\omega_0}{A} = \frac{100}{10000} = 0.01 Hz$

(d) $\beta = 1$ $P_0'' = P_2'' \frac{A_3}{A_1} = P_2 \frac{A_3}{A_1}$ Improved Compensation.

$\omega_0 = \omega_z = 10kHz$

$\omega_p = \frac{10k}{10000} = 1Hz$

(e) $\beta = 1$, Improved compensation.

$\omega_0 = A\omega_p$ $\omega_p = 0.5Hz$

$= 10000 [0.5Hz]$

$= 5kHz$

$PM = -112.5° + 180°$

$= 67.5°$