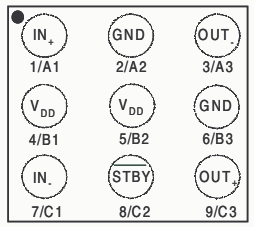
TS4962M

3W Filter-free Class D Audio Power Amplifier

PRELIMINARY DATA

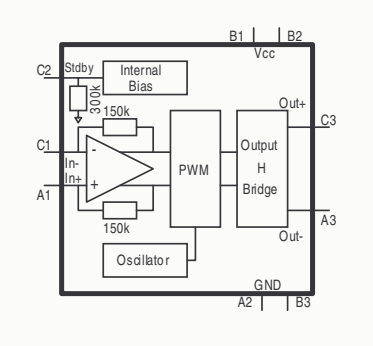
- Operating from Vcc=2.4V to 5.5V
- Standby mode active low
- Output power: 3W into 4Ω and 1.75W into 8Ω with 10% THD+N max and 5V power supply.
- Output power: 2.3W @5V or 0.75W @ 3.0V into 4Ω with 1% THD+N max.
- Output power: 1.4W @5V or 0.45W @ 3.0V into 8Ω with 1% THD+N max.
- Adjustable gain via external resistors
- Low current consumption 2mA @ 3V
- Efficiency: 88% typ.
- Signal to noise ratio: 85dB typ.
- PSRR: 63dB typ. @217Hz with 6dB gain
- PWM base frequency: 250kHz
- Low pop & click noise
- Thermal shutdown protection
- Available in flip-chip 9 x 300µm (Pb-free)

TS4962MEIJT - Flip Chip



IN+: positive differential input
IN-: negative differential input
VDD: analog power supply
GND: power supply ground
STBY: standby pin (active low)
OUT+: positive differential output
OUT-: negative differential output

Block diagram



Description

The TS4962M is a differential class-D B.T.L. power amplifier. It is able to drive up to 2.3W into a 4Ω load and 1.4W into a 8Ω load at 5V. It achieves outstanding efficiency (88%typ.) compared to classical AB-class audio amps.

The gain of the device can be controlled via two external gain-setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows the reduction of current consumption to 10nA typ.

Applications

- Cellular Phone
- PDA
- Notebook PC

Order Codes

Part Number	Temperature Range	Package	Packing	Marking
TS4962MEIJT	-40, +85°C	Lead-Free Flip-Chip	Tape & Reel	62
TS4962MEIKJT		Lead-Free + Back Coating		62

1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1), (2)	6	V
V_i	Input Voltage (3)	G_{ND} to V_{cc}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient (4)	200	°C/W
Pd	Power Dissipation	Internally Limited(5)	
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
Latch-up	Latch-up Immunity	200	mA
V_{STB}	Standby pin voltage maximum voltage (6)	G_{ND} to V_{cc}	V
	Lead Temperature (soldering, 10sec)	260	°C

1. Caution: This device is not protected in the event of abnormal operating conditions, such as for example, short-circuiting between any one output pin and ground, between any one output pin and Vcc, and between individual output pins.
2. All voltages values are measured with respect to the ground pin
3. The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
4. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
5. Exceeding the power derating curves during a long period, involves abnormal operating condition.
6. The magnitude of standby signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage(1)	2.4 to 5.5	V
V_{IC}	Common Mode Input Voltage Range(2)	0.5 to V_{CC}-0.8	V
V_{STB}	Standby Voltage Input: (3) Device ON Device OFF	 $1.4 \leq V_{STB} \leq V_{CC}$ $G_{ND} \leq V_{STB} \leq 0.4$ (4)	V
RL	Load Resistor	≥ 4	Ω
R_{thja}	Thermal Resistance Junction to Ambient (5)	90	°C/W

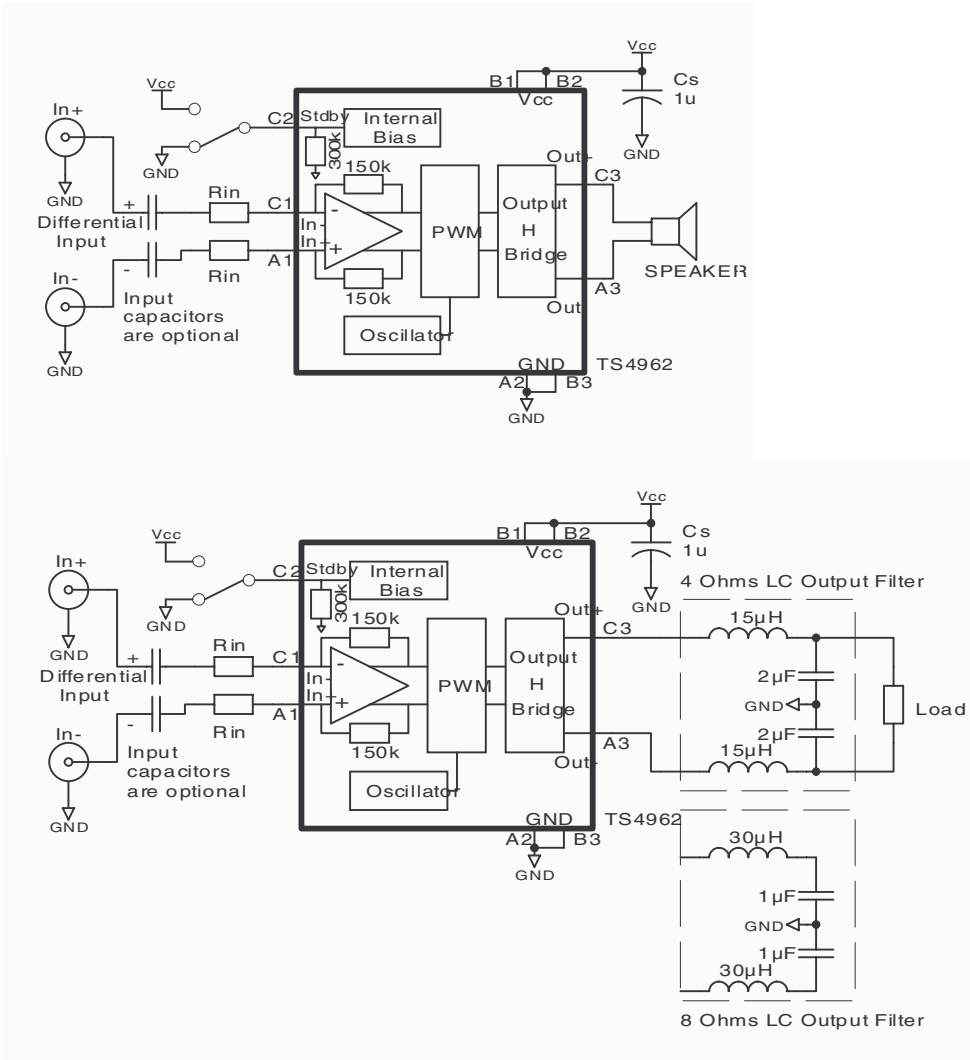
1. For V_{CC} from 2.4V to 2.5V, the operating temperature range is reduced to 0°C≤ Tamb ≤70°C
2. For V_{CC} from 2.4V to 2.5V, the common mode input range must be set at V_{CC}/2
3. Without any signal on V_{STB}, the device will be in standby
4. Minimum current consumption shall be obtained when V_{STB} = GND
5. With heat sink surface = 125mm^2

2 Application Component Information

Table 3. Component information .

Component	Functional Description
Cs	Bypass supply capacitor. To install as close as possible to the TS4962M to minimize high-frequency ripple. A 100nF ceramic capacitor should be added to enhance the power supply filtering at high frequency.
Rin	Input resistor to program the TS4962M differential gain (Gain = 300kΩ/Rin with Rin in kΩ).
Input Capacitor	Thanks to common mode feedback, these input capacitors are optional. However, they can be added to form with Rin a 1st order high pass filter with -3dB cut-off frequency = 1/(2*π*Rin*Cin).

Figure 1. Typical application schematics



3 Electrical Characteristics

Table 4. Vcc = +5V, GND = 0V, Vicm = 2.5V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		2.3	3.3	mA
$I_{STANDBY}$	Standby Current (1) No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, R_L = 8Ω		3	25	mV
Po	Output Power, G=6dB THD = 1% Max, f = 1kHz, R_L = 4Ω THD = 10% Max, f = 1kHz, R_L = 4Ω THD = 1% Max, f = 1kHz, R_L = 8Ω THD = 10% Max, f = 1kHz, R_L = 8Ω		 2.3 3 1.4 1.75		W
THD + N	Total Harmonic Distortion + Noise Po = 900 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, R_L = 8Ω + 15µH, BW < 30kHz Po = 1W_{RMS}, G = 6dB, f = 1kHz, R_L = 8Ω + 15µH, BW < 30kHz		 1 0.4		%
Efficiency	Efficiency Po = 2 W_{RMS}, R_L = 4Ω + ≥ 15µH Po =1.2 W_{RMS}, R_L = 8Ω+ ≥ 15µH		 78 88		%
PSRR	Power Supply Rejection Ratio with inputs grounded (2) f = 217Hz, R_L = 8Ω, G=6dB, Vripple = 200mV_{pp}		63		dB
CMRR	Common Mode Rejection Ratio, f = 217Hz, R_L = 8Ω, G = 6dB, ΔVic = 200mV_{pp}		57		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	273	300	327	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency	180	250	320	kHz
SNR	Signal to Noise ratio (A Weighting), Po = 1.2W, R_L = 8Ω		85		dB
T_{WU}	Wake-up time		5	10	ms
T_{STB}	Standby time		5	10	ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted R_L = 4Ω A weighted R_L = 4Ω Unweighted R_L = 8Ω A weighted R_L = 8Ω Unweighted R_L = 4Ω + 15µH A weighted R_L = 4Ω + 15µH Unweighted R_L = 4Ω + 30µH A weighted R_L = 4Ω + 30µH Unweighted R_L = 8Ω + 30µH A weighted R_L = 8Ω + 30µH Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter		 85 60 86 62 83 60 88 64 78 57 87 65 82 59 90 66		μV_{RMS}

1. Standby mode is active when Vstdby is tied to GND.
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the superimposed sinusoidal signal to V_{cc} @ f = 217Hz.

Table 5. Vcc = +4.2V, GND = 0V, Vicm = 2.1V, Tamb = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		2.1	3	mA
$I_{STANDBY}$	Standby Current (2) No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, $R_L = 8\Omega$		3	25	mV
Po	Output Power, G=6dB THD = 1% Max, f = 1kHz, $R_L = 4\Omega$ THD = 10% Max, f = 1kHz, $R_L = 4\Omega$ THD = 1% Max, f = 1kHz, $R_L = 8\Omega$ THD = 10% Max, f = 1kHz, $R_L = 8\Omega$		 1.6 2 0.95 1.2		W
THD + N	Total Harmonic Distortion + Noise Po = 600 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, $R_L = 8\Omega$ + 15µH, BW < 30kHz Po = 700mW_{RMS}, G = 6dB, f = 1kHz, $R_L = 8\Omega$ + 15µH, BW < 30kHz		 1 0.35		%
Efficiency	Efficiency Po = 1.45 W_{RMS}, $R_L = 4\Omega + \geq 15\mu H$ Po = 0.9 W_{RMS}, $R_L = 8\Omega + \geq 15\mu H$		 78 88		%
PSRR	Power Supply Rejection Ratio with inputs grounded (3) f = 217Hz, $R_L = 8\Omega$, G=6dB, Vripple = 200mV_{pp}		 63		dB
CMRR	Common Mode Rejection Ratio f = 217Hz, $R_L = 8\Omega$, G = 6dB, ΔVic = 200mV_{pp}		57		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	273	300	327	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency	180	250	320	kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.9W, $R_L = 8\Omega$		85		dB
T_{WU}	Wake-up time		5	10	ms
T_{STB}	Standby time		5	10	ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted $R_L = 4\Omega$ A weighted $R_L = 4\Omega$ Unweighted $R_L = 8\Omega$ A weighted $R_L = 8\Omega$ Unweighted $R_L = 4\Omega$ + 15µH A weighted $R_L = 4\Omega$ + 15µH Unweighted $R_L = 4\Omega$ + 30µH A weighted $R_L = 4\Omega$ + 30µH Unweighted $R_L = 8\Omega$ + 30µH A weighted $R_L = 8\Omega$ + 30µH Unweighted $R_L = 4\Omega$ + Filter A weighted $R_L = 4\Omega$ + Filter Unweighted $R_L = 4\Omega$ + Filter A weighted $R_L = 4\Omega$ + Filter		 85 60 86 62 83 60 88 64 78 57 87 65 82 59 90 66		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.5V and 5V.
2. Standby mode is active when Vstdby is tied to GND.
3. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the superimposed sinusoidal signal to Vcc @ f = 217Hz.

Table 6. Vcc = +3.6V, GND = 0V, Vicm = 1.8V, Tamb = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		2	2.8	mA
$I_{STANDBY}$	Standby Current (2) No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, $R_L = 8\Omega$		3	25	mV
Po	Output Power, G=6dB THD = 1% Max, f = 1kHz, $R_L = 4\Omega$ THD = 10% Max, f = 1kHz, $R_L = 4\Omega$ THD = 1% Max, f = 1kHz, $R_L = 8\Omega$ THD = 10% Max, f = 1kHz, $R_L = 8\Omega$		 1.15 1.51 0.7 0.9		W
THD + N	Total Harmonic Distortion + Noise Po = 500 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, $R_L = 8\Omega$ + 15µH, BW < 30kHz Po = 500mW_{RMS}, G = 6dB, f = 1kHz, $R_L = 8\Omega$ + 15µH, BW < 30kHz		 1 0.27		%
Efficiency	Efficiency Po = 1 W_{RMS}, $R_L = 4\Omega + \geq 15\mu H$ Po = 0.65 W_{RMS}, $R_L = 8\Omega + \geq 15\mu H$		 78 88		%
PSRR	Power Supply Rejection Ratio with inputs grounded (3) f = 217Hz, $R_L = 8\Omega$, G=6dB, Vripple = 200mV_{pp}		62		dB
CMRR	Common Mode Rejection Ratio f = 217Hz, $R_L = 8\Omega$, G = 6dB, ΔVic = 200mV_{pp}		56		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	273	300	327	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency	180	250	320	kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.6W, $R_L = 8\Omega$		83		dB
T_{WU}	Wake-up time		5	10	ms
T_{STB}	Standby time		5	10	ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted $R_L = 4\Omega$ A weighted $R_L = 4\Omega$ Unweighted $R_L = 8\Omega$ A weighted $R_L = 8\Omega$ Unweighted $R_L = 4\Omega$ + 15µH A weighted $R_L = 4\Omega$ + 15µH Unweighted $R_L = 4\Omega$ + 30µH A weighted $R_L = 4\Omega$ + 30µH Unweighted $R_L = 8\Omega$ + 30µH A weighted $R_L = 8\Omega$ + 30µH Unweighted $R_L = 4\Omega$ + Filter A weighted $R_L = 4\Omega$ + Filter Unweighted $R_L = 4\Omega$ + Filter A weighted $R_L = 4\Omega$ + Filter		 83 57 83 61 81 58 87 62 77 56 85 63 80 57 85 61		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.5V and 5V.
2. Standby mode is actived when Vstdby is tied to GND.
3. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the superimposed sinusoidal signal to Vcc @ f = 217Hz.

Table 7. Vcc = +3.0V, GND = 0V, Vicm = 1.5V, Tamb = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.9	2.7	mA
$I_{STANDBY}$	Standby Current (2) No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, $R_L = 8\Omega$		3	25	mV
Po	Output Power, G=6dB THD = 1% Max, f = 1kHz, $R_L = 4\Omega$ THD = 10% Max, f = 1kHz, $R_L = 4\Omega$ THD = 1% Max, f = 1kHz, $R_L = 8\Omega$ THD = 10% Max, f = 1kHz, $R_L = 8\Omega$		 0.75 1 0.5 0.6		W
THD + N	Total Harmonic Distortion + Noise Po = 350 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, $R_L = 8\Omega$ + 15µH, BW < 30kHz Po = 350mW_{RMS}, G = 6dB, f = 1kHz, $R_L = 8\Omega$ + 15µH, BW < 30kHz		 1 0.21		%
Efficiency	Efficiency Po = 0.7 W_{RMS}, $R_L = 4\Omega + \geq 15\mu H$ Po = 0.45 W_{RMS}, $R_L = 8\Omega + \geq 15\mu H$		 78 88		%
PSRR	Power Supply Rejection Ratio with inputs grounded (3) f = 217Hz, $R_L = 8\Omega$, G=6dB, Vripple = 200mV_{pp}		 60		dB
CMRR	Common Mode Rejection Ratio, f = 217Hz, $R_L = 8\Omega$, G = 6dB, ΔVic = 200mV_{pp}		54		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	273	300	327	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency	180	250	320	kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.4W, $R_L = 8\Omega$		82		dB
T_{WU}	Wake-up time		5	10	ms
T_{STB}	Standby time		5	10	ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted $R_L = 4\Omega$ A weighted $R_L = 4\Omega$ Unweighted $R_L = 8\Omega$ A weighted $R_L = 8\Omega$ Unweighted $R_L = 4\Omega$ + 15µH A weighted $R_L = 4\Omega$ + 15µH Unweighted $R_L = 4\Omega$ + 30µH A weighted $R_L = 4\Omega$ + 30µH Unweighted $R_L = 8\Omega$ + 30µH A weighted $R_L = 8\Omega$ + 30µH Unweighted $R_L = 4\Omega$ + Filter A weighted $R_L = 4\Omega$ + Filter Unweighted $R_L = 4\Omega$ + Filter A weighted $R_L = 4\Omega$ + Filter		 83 57 83 61 81 58 87 62 77 56 85 63 80 57 85 61		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.5V and 5V.
2. Standby mode is active when Vstdby is tied to GND.
3. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the superimposed sinusoidal signal to Vcc @ f = 217Hz.

Table 8. Vcc = +2.5V, GND = 0V, Vicm = 1.25V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.7	2.4	mA
$I_{STANDBY}$	Standby Current (1) No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, R_L = 8Ω		3	25	mV
Po	Output Power, G=6dB THD = 1% Max, f = 1kHz, R_L = 4Ω THD = 10% Max, f = 1kHz, R_L = 4Ω THD = 1% Max, f = 1kHz, R_L = 8Ω THD = 10% Max, f = 1kHz, R_L = 8Ω		 0.52 0.71 0.33 0.42		W
THD + N	Total Harmonic Distortion + Noise Po = 200 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, R_L = 8Ω + 15µH, BW < 30kHz Po = 200mW_{RMS}, G = 6dB, f = 1kHz, R_L = 8Ω + 15µH, BW < 30kHz		 1 0.19		%
Efficiency	Efficiency Po = 0.47 W_{RMS}, R_L = 4Ω + ≥ 15µH Po = 0.3 W_{RMS}, R_L = 8Ω+ ≥ 15µH		 78 88		%
PSRR	Power Supply Rejection Ratio with inputs grounded (2) f = 217Hz, R_L = 8Ω, G=6dB, Vripple = 200mV_{pp}		60		dB
CMRR	Common Mode Rejection Ratio f = 217Hz, R_L = 8Ω, G = 6dB, ΔVic = 200mV_{pp}		54		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	273	300	327	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency	180	250	320	kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.4W, R_L = 8Ω		80		dB
T_{WU}	Wake-up time		5	10	ms
T_{STB}	Standby time		5	10	ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted R_L = 4Ω A weighted R_L = 4Ω Unweighted R_L = 8Ω A weighted R_L = 8Ω Unweighted R_L = 4Ω + 15µH A weighted R_L = 4Ω + 15µH Unweighted R_L = 4Ω + 30µH A weighted R_L = 4Ω + 30µH Unweighted R_L = 8Ω + 30µH A weighted R_L = 8Ω + 30µH Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter		 85 60 86 62 76 56 82 60 67 53 78 57 74 54 78 59		μV_{RMS}

1. Standby mode is active when Vstdby is tied to GND.
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the superimposed sinusoidal signal to Vcc @ f = 217Hz.

Table 9. Vcc +2.4V$_1$, GND = 0V, Vicm = 1.2V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.7		mA
$I_{STANDBY}$	Standby Current (1) No input signal, V_{STBY} = GND		10		nA
Voo	Output Offset Voltage No input signal, R_L = 8Ω		3		mV
Po	Output Power, G=6dB THD = 1% Max, f = 1kHz, R_L = 4Ω THD = 10% Max, f = 1kHz, R_L = 4Ω THD = 1% Max, f = 1kHz, R_L = 8Ω THD = 10% Max, f = 1kHz, R_L = 8Ω		 0.48 0.65 0.3 0.38		W
THD + N	Total Harmonic Distortion + Noise Po = 200 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, R_L = 8Ω + 15µH, BW < 30kHz		1		%
Efficiency	Efficiency Po = 0.38 W_{RMS}, R_L = 4Ω + ≥ 15µH Po = 0.25 W_{RMS}, R_L = 8Ω+ ≥ 15µH		 77 86		%
CMRR	Common Mode Rejection Ratio f = 217Hz, R_L = 8Ω, G = 6dB, ΔVic = 200mV_{pp}		54		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	273	300	327	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency		250		kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.25W, R_L = 8Ω		80		dB
T_{WU}	Wake-up time		5		ms
T_{STB}	Standby time		5		ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted R_L = 4Ω A weighted R_L = 4Ω Unweighted R_L = 8Ω A weighted R_L = 8Ω Unweighted R_L = 4Ω + 15µH A weighted R_L = 4Ω + 15µH Unweighted R_L = 4Ω + 30µH A weighted R_L = 4Ω + 30µH Unweighted R_L = 8Ω + 30µH A weighted R_L = 8Ω + 30µH Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter		 85 60 86 62 76 56 82 60 67 53 78 57 74 54 78 59		μV_{RMS}

1. Standby mode is active when Vstdby is tied to GND.

4 Electrical characteristic curves

In the graphs that follow, the following abbreviations are used:

- RL + 15µH or 30µH = pure resistor+ very low series resistance inductor
- Filter = LC output filter (1µF+30µH for 4Ω and 0.5µF+60µH for 8Ω)
- All measurements done with Cs1=1µF and Cs2=100nF except for PSRR where Cs1 is removed.

Figure 2. Test diagram for measurements

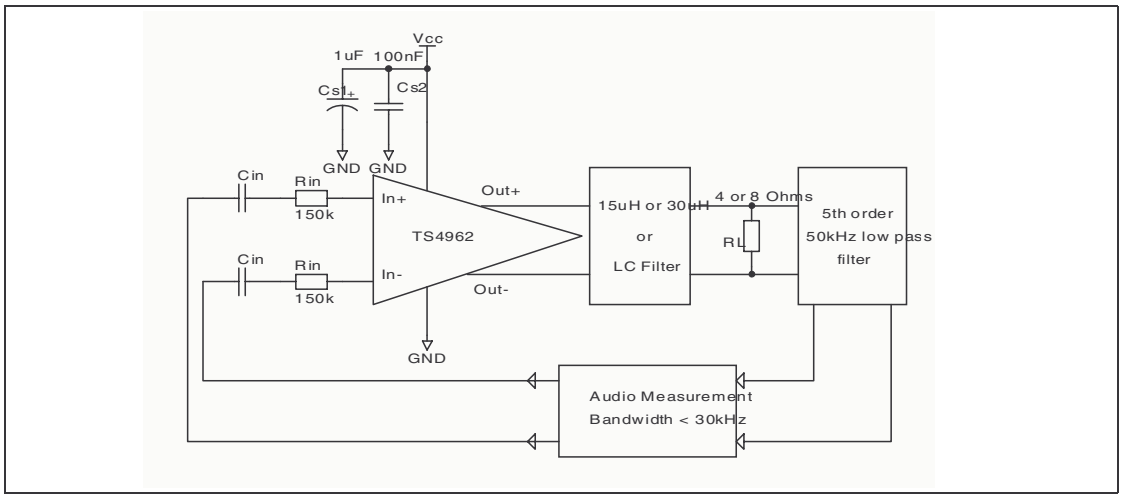


Figure 3. Test diagram for PSRR measurements

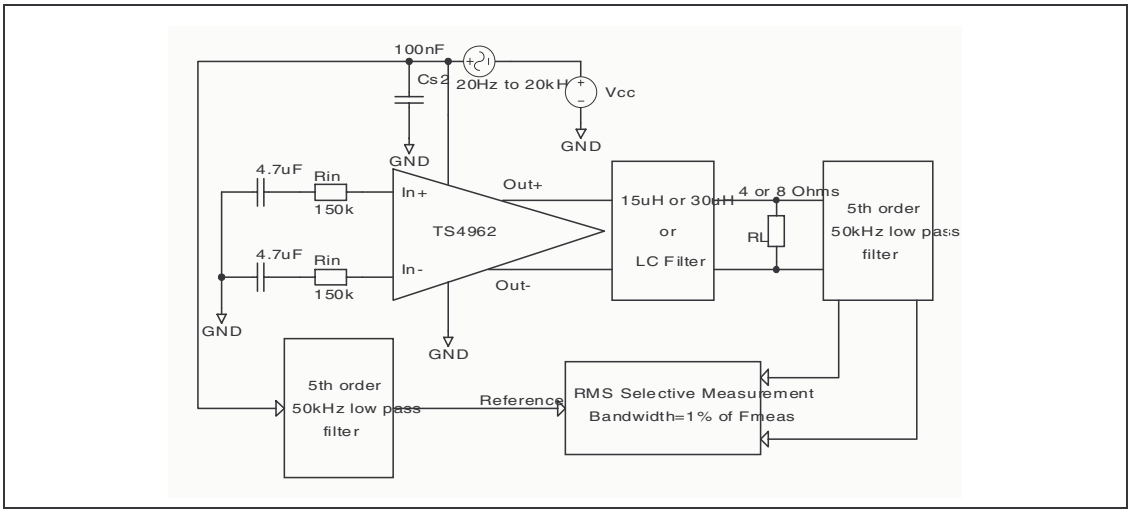


Figure 4. Current consumption vs. power supply voltage

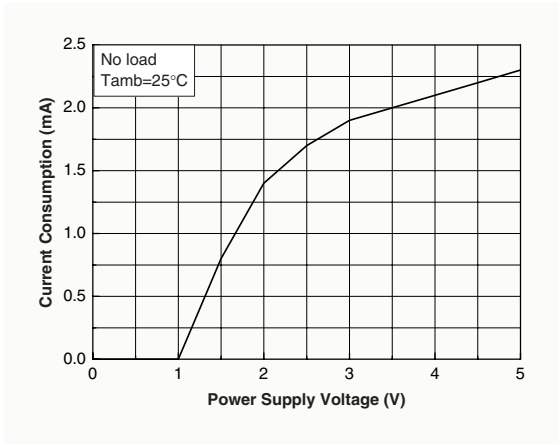


Figure 5. Current consumption vs. standby voltage

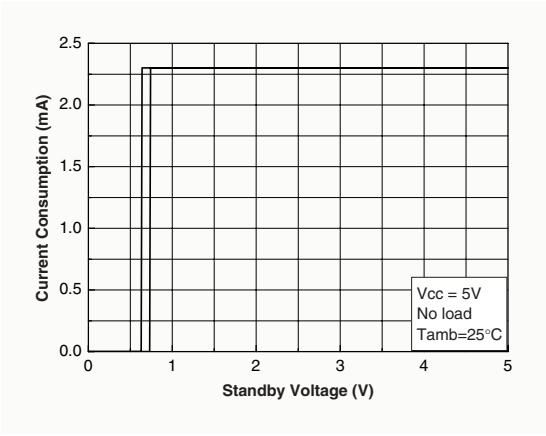


Figure 6. Current consumption vs. standby voltage

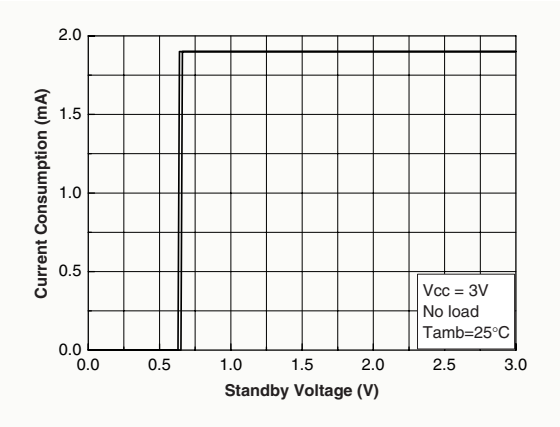


Figure 7. Output offset voltage vs. common mode input voltage

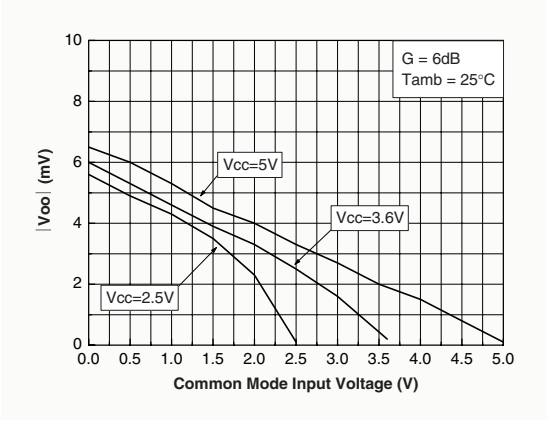


Figure 8. Efficiency vs. output power

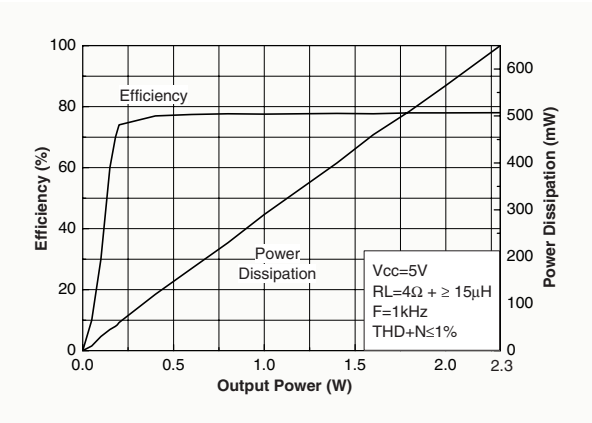


Figure 9. Efficiency vs. output power

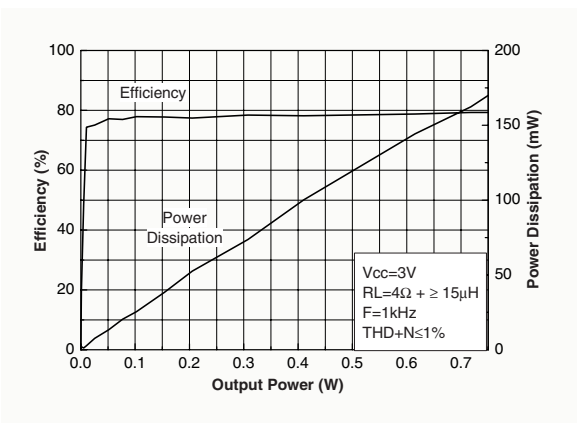


Figure 10. Efficiency vs. output power

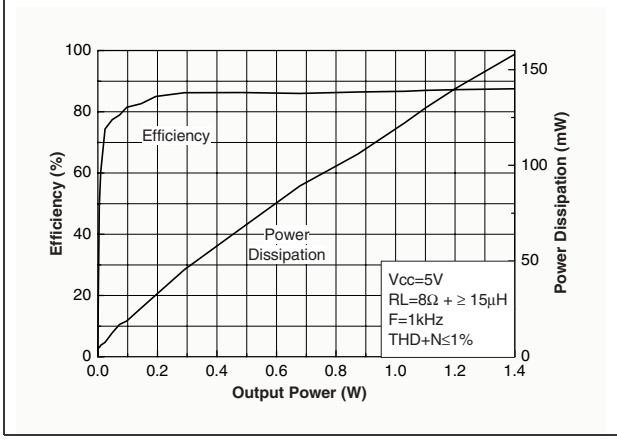


Figure 11. Efficiency vs. output power

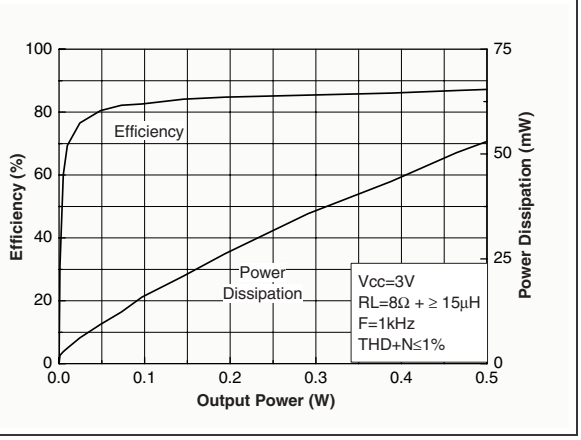


Figure 12. Output power vs. power supply voltage

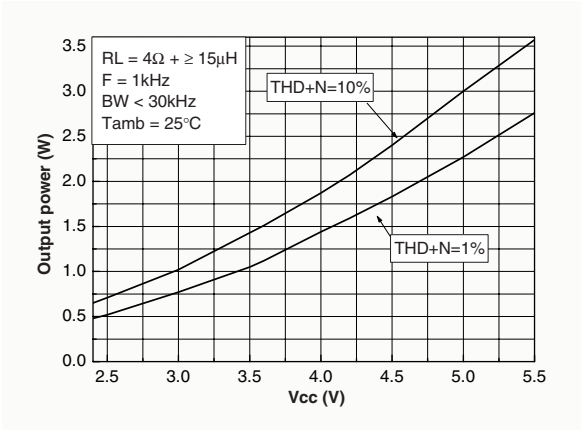


Figure 13. Output power vs. power supply voltage

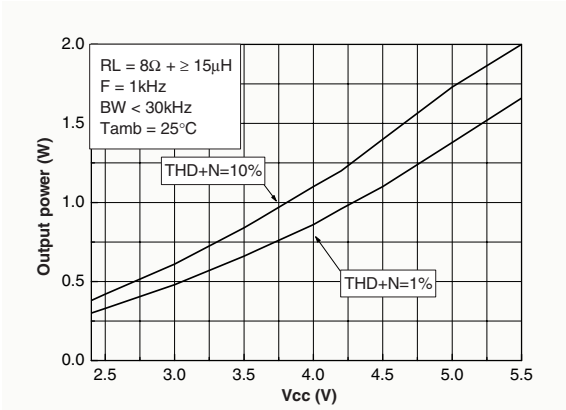


Figure 14. PSSR vs. frequency

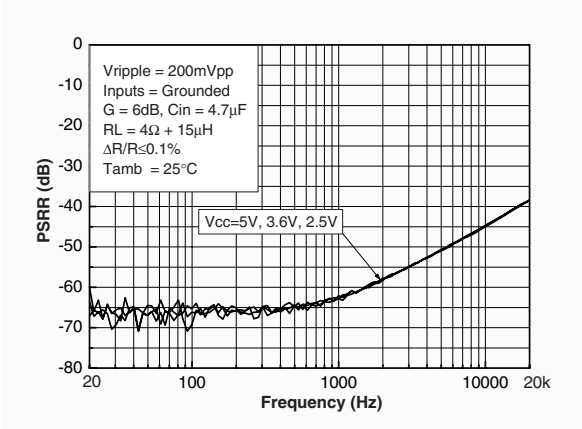


Figure 15. PSSR vs. frequency

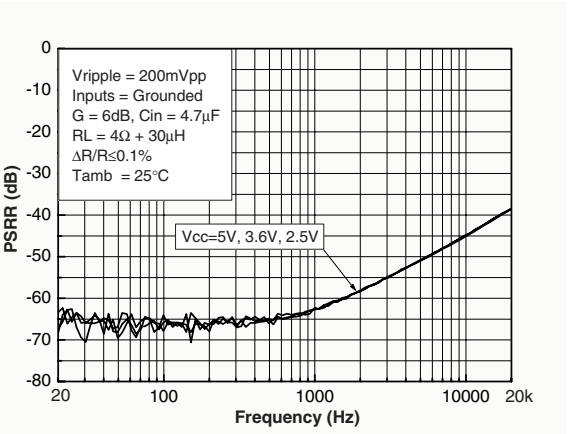


Figure 16. PSSR vs. frequency

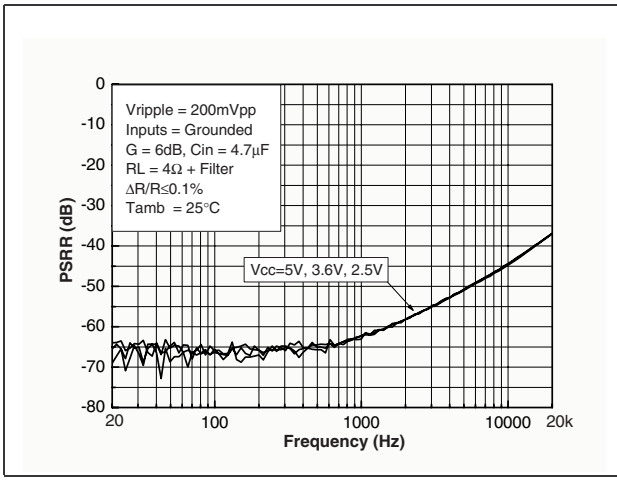


Figure 17. PSSR vs. frequency

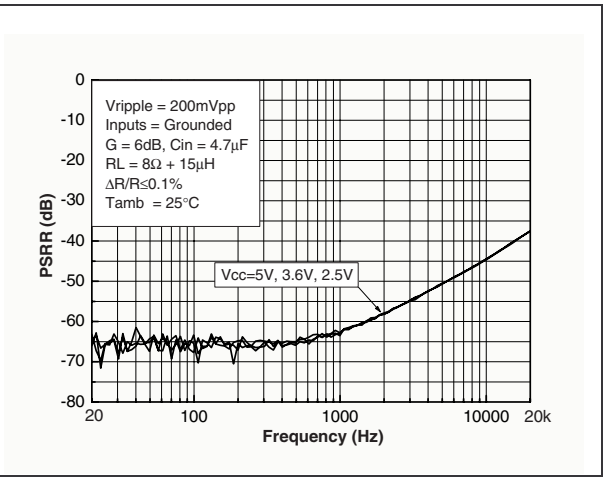


Figure 18. PSSR vs. frequency

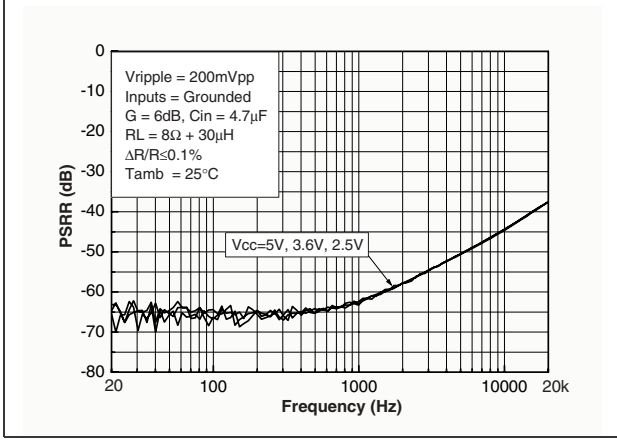


Figure 19. PSSR vs. frequency

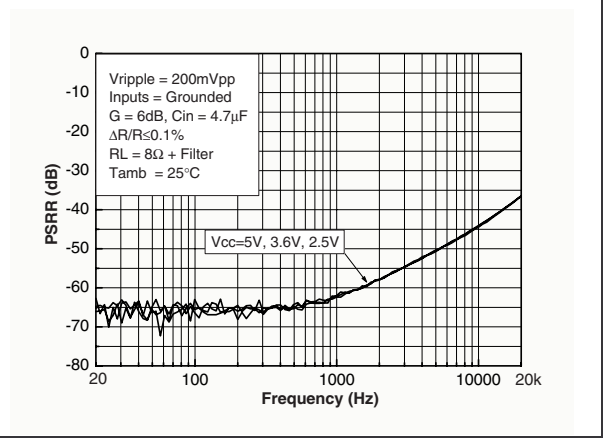


Figure 20. PSRR vs. common mode input voltage

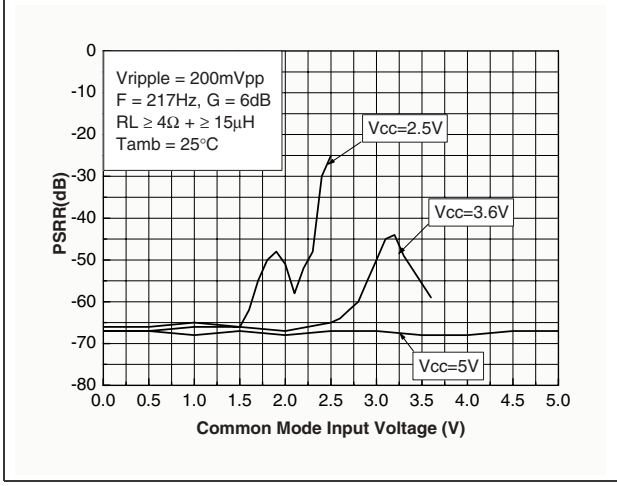


Figure 21. CMR vs. frequency

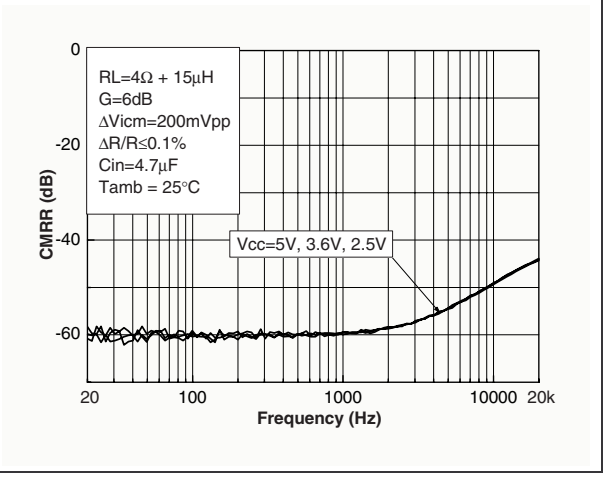


Figure 22. CMRR vs. frequency

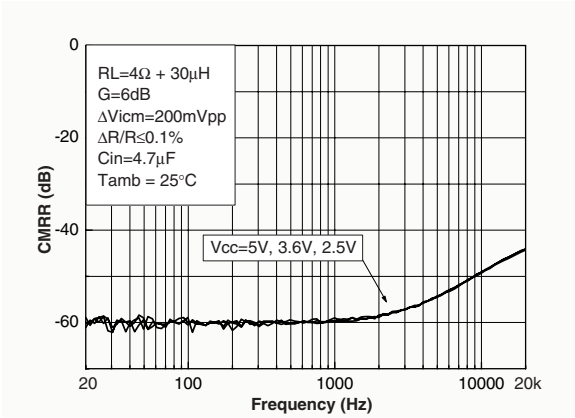


Figure 23. CMRR vs. frequency

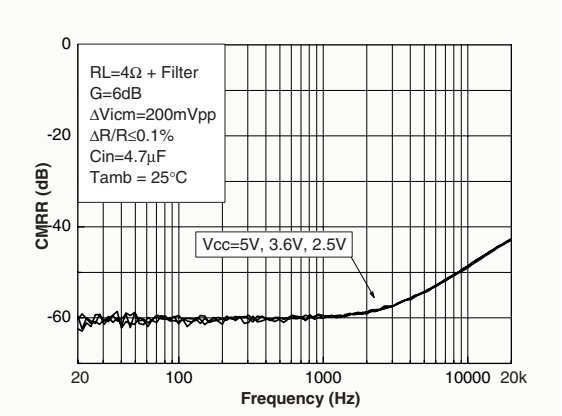


Figure 24. CMRR vs. frequency

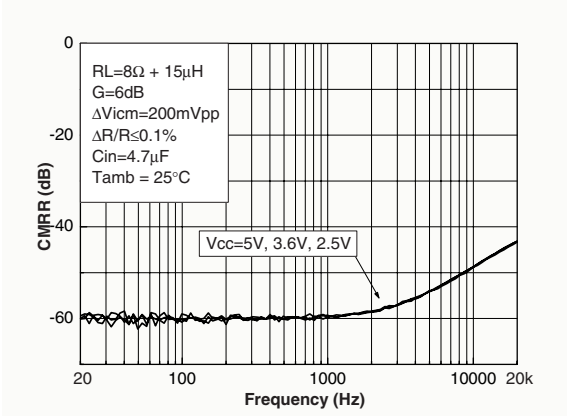


Figure 25. CMRR vs. frequency

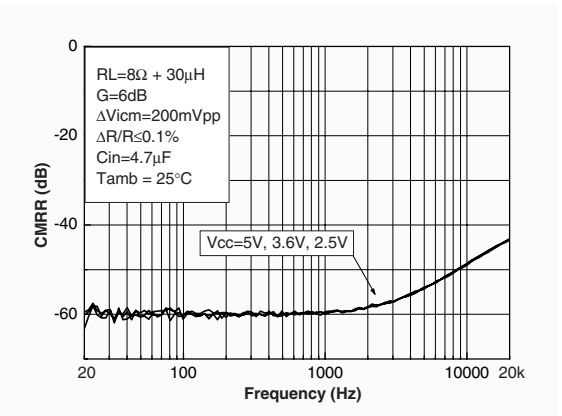


Figure 26. CMRR vs. frequency

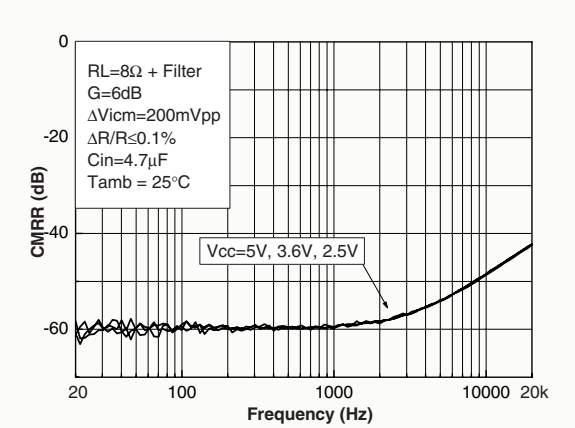


Figure 27. CMRR vs. common mode input voltage

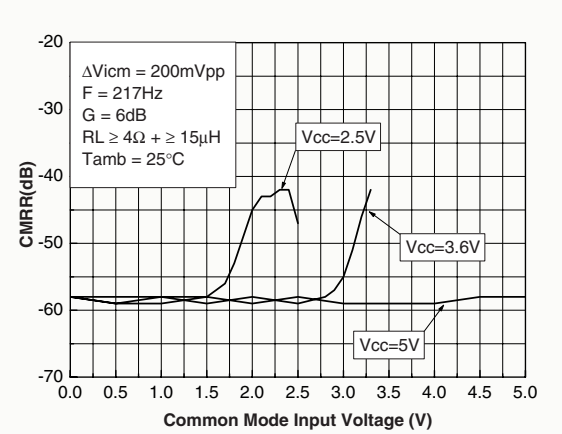


Figure 28. THD+N vs. output power

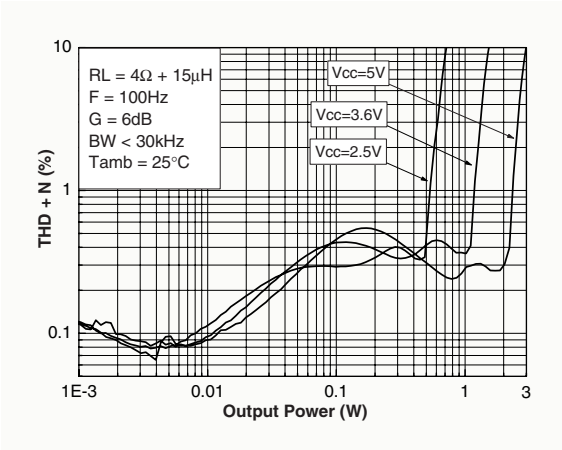


Figure 29. THD+N vs. output power

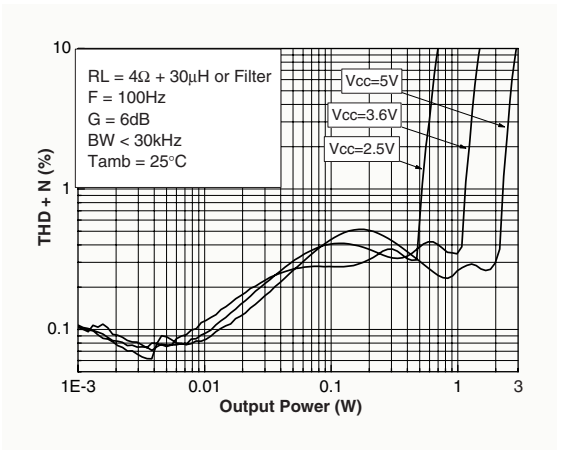


Figure 30. THD+N vs. output power

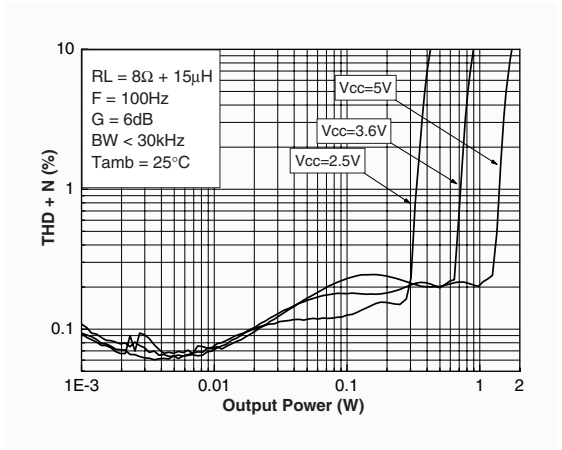


Figure 31. THD+N vs. output power

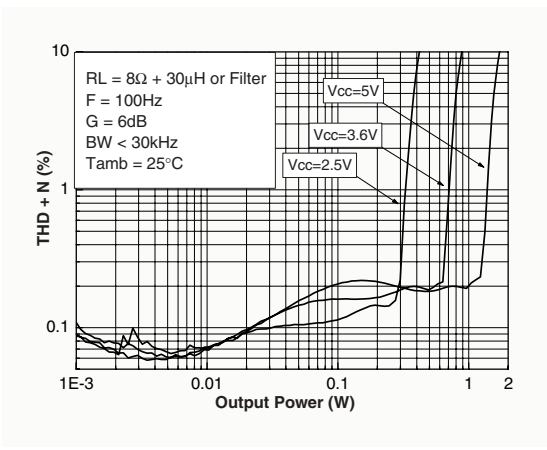


Figure 32. THD+N vs. output power

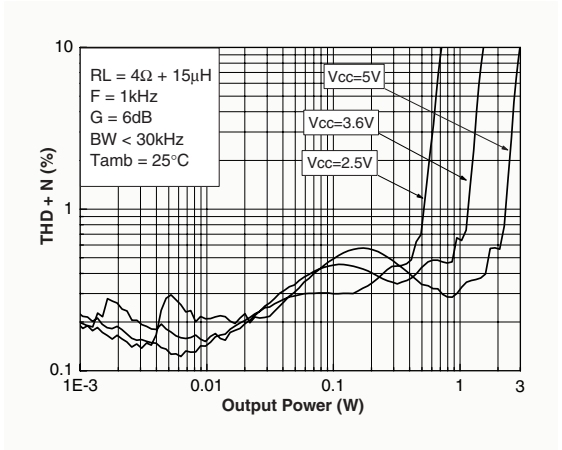


Figure 33. THD+N vs. output power

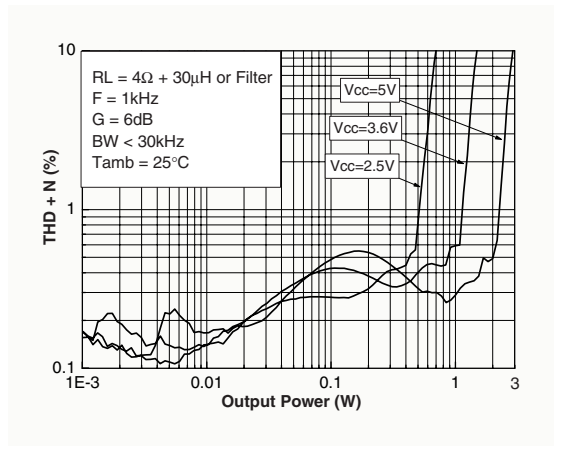


Figure 34. THD+N vs. output power

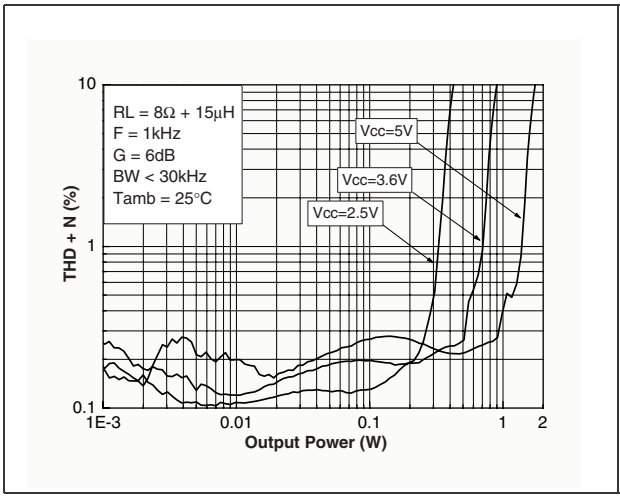


Figure 35. THD+N vs. output power

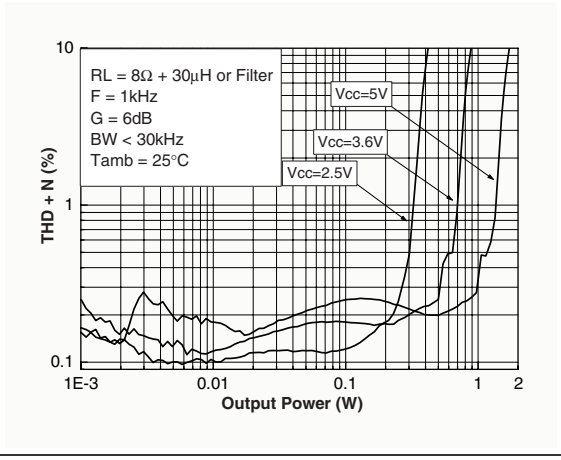


Figure 36. THD+N vs. frequency

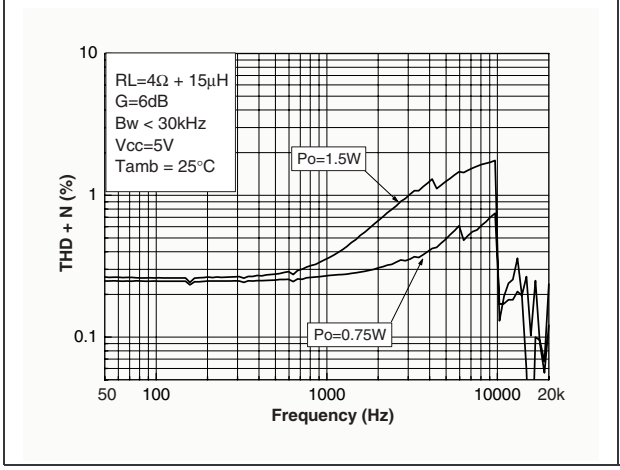


Figure 37. THD+N vs. frequency

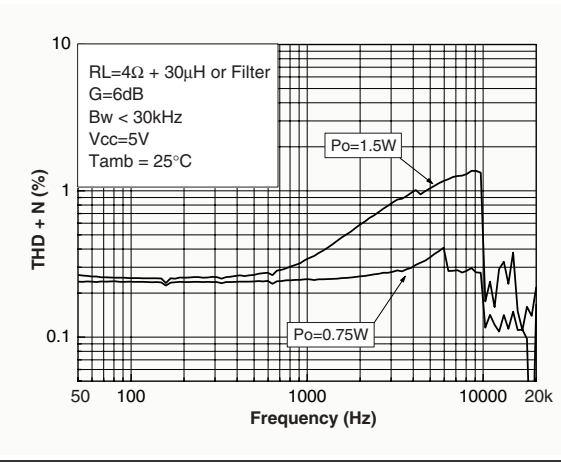


Figure 38. THD+N vs. frequency

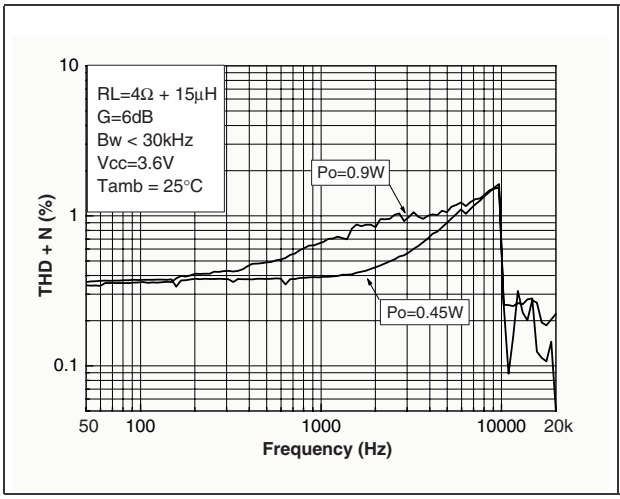


Figure 39. THD+N vs. frequency

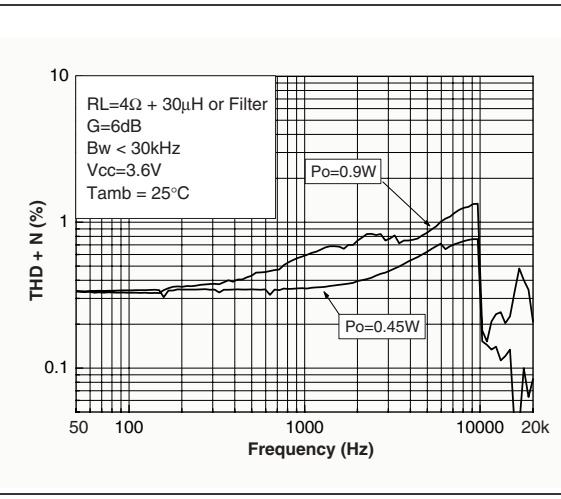


Figure 40. THD+N vs. frequency

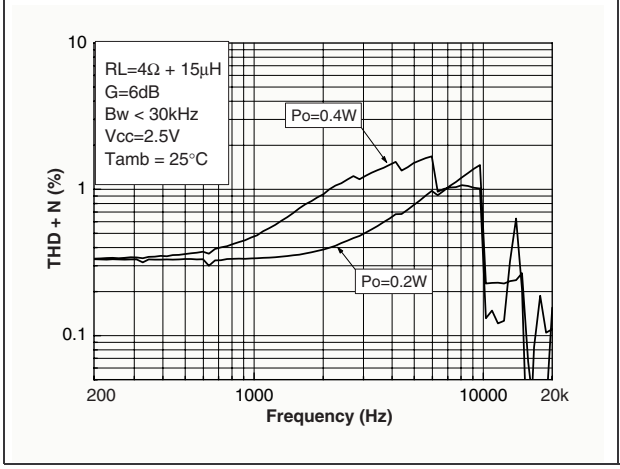


Figure 41. THD+N vs. frequency

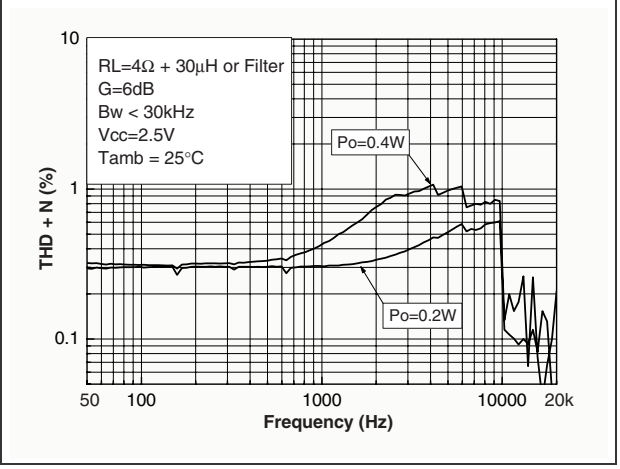


Figure 42. THD+N vs. frequency

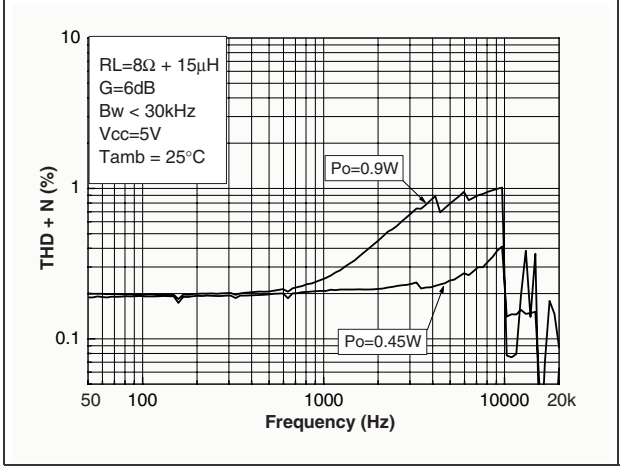


Figure 43. THD+N vs. frequency

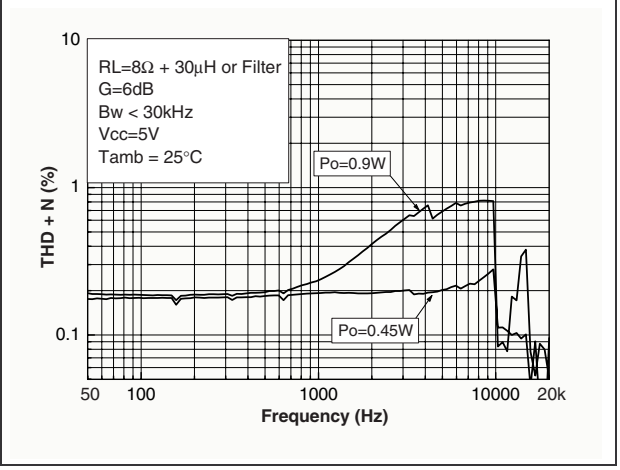


Figure 44. THD+N vs. frequency

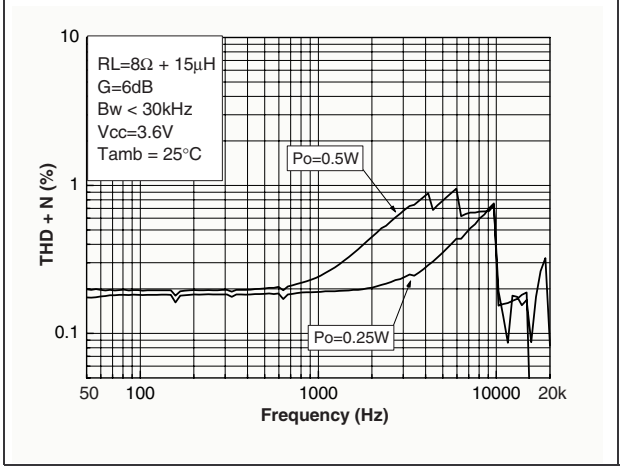


Figure 45. THD+N vs. frequency

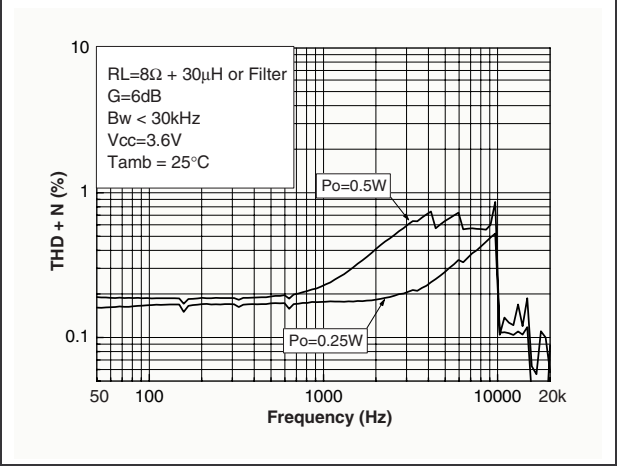


Figure 46. THD+N vs. frequency

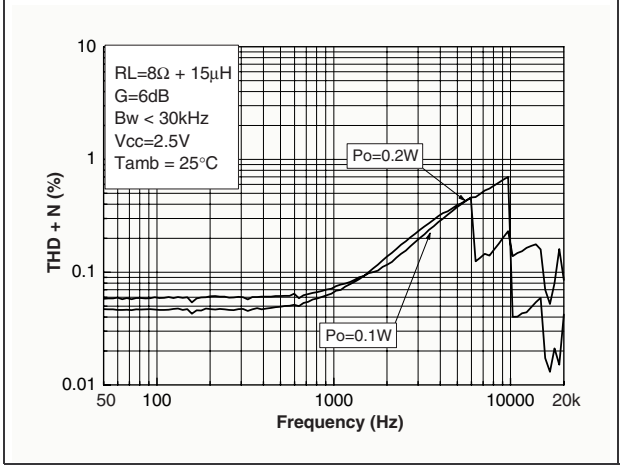


Figure 47. THD+N vs. frequency

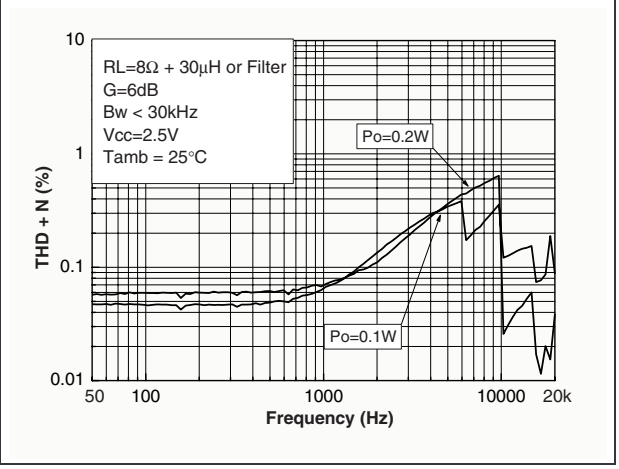


Figure 48. Gain vs. frequency

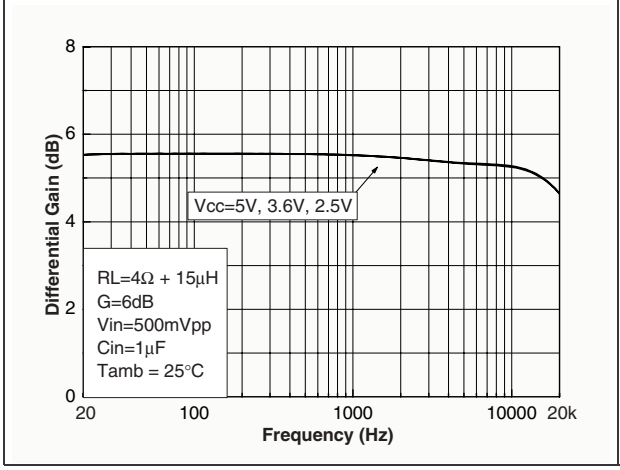


Figure 49. Gain vs. frequency

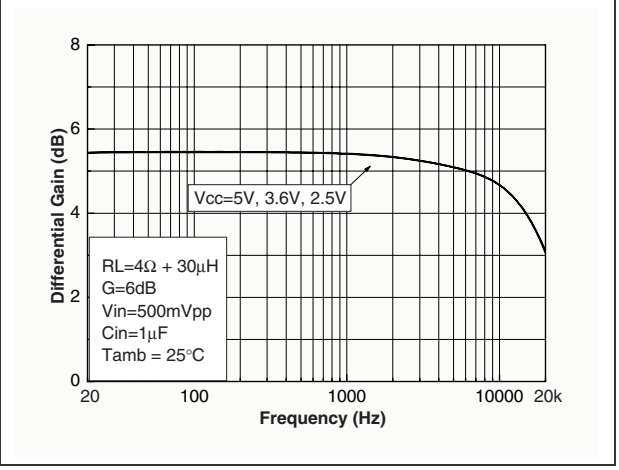


Figure 50. Gain vs. frequency

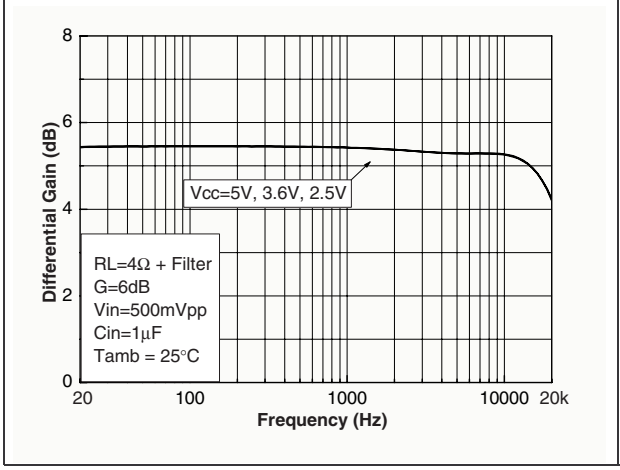


Figure 51. Gain vs. frequency

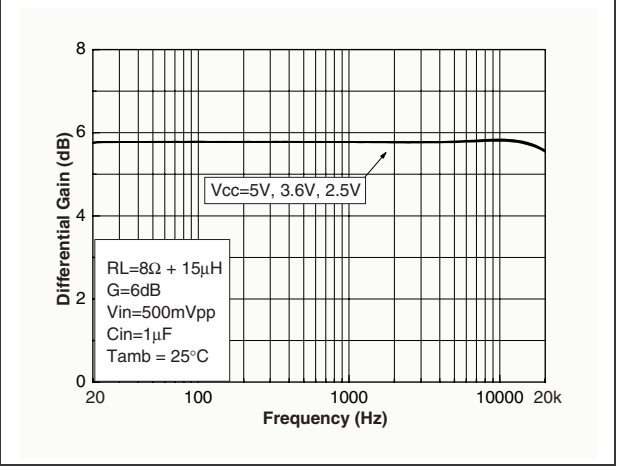


Figure 52. Gain vs. frequency

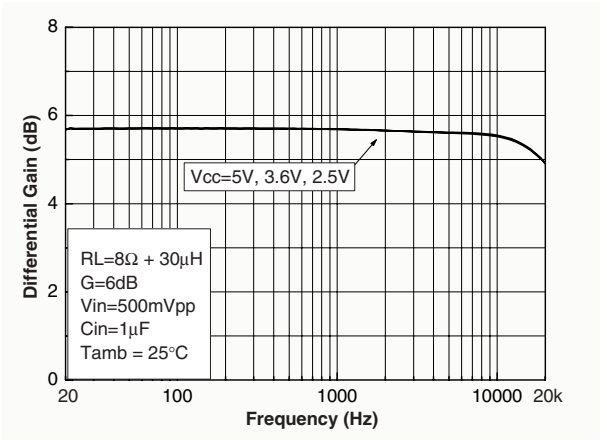


Figure 53. Gain vs. frequency

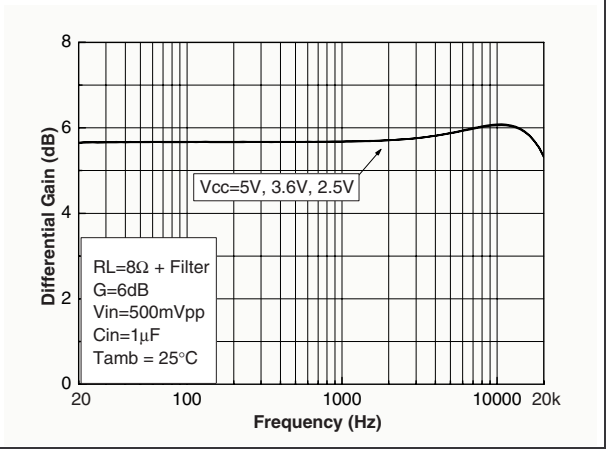


Figure 54. Gain vs. frequency

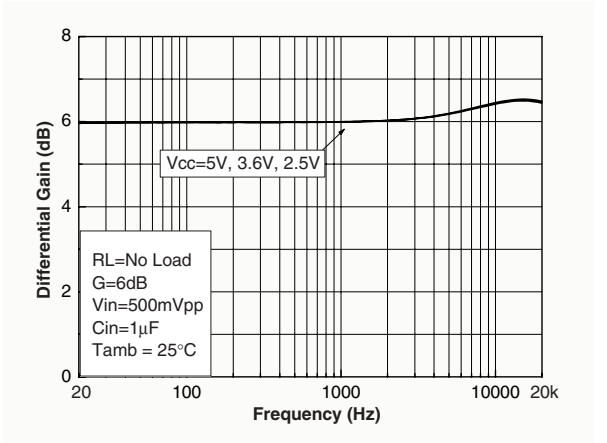


Figure 55. Startup & shutdown time Vcc=5V, G=6dB, CIN=1µF (5ms/div)

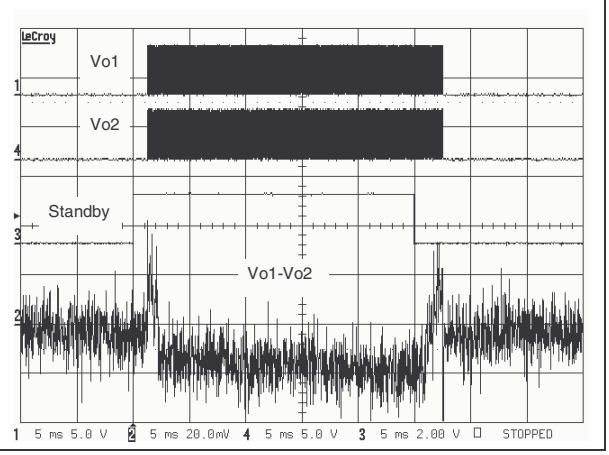


Figure 56. Startup & shutdown time Vcc=3V, G=6dB, CIN=1µF (5ms/div)

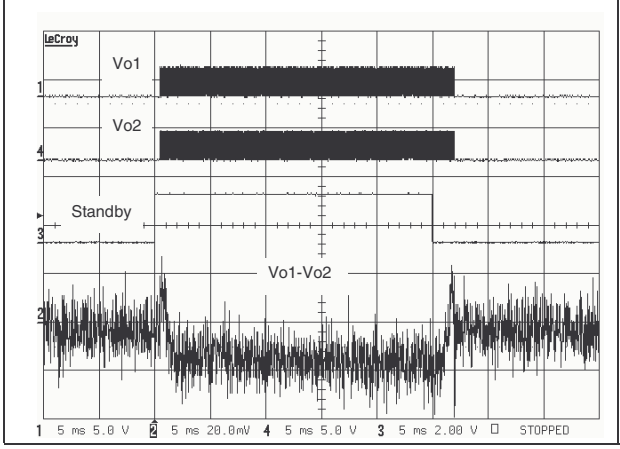


Figure 57. Startup & shutdown time Vcc=5V, G=6dB, CIN=100nF (5ms/div)

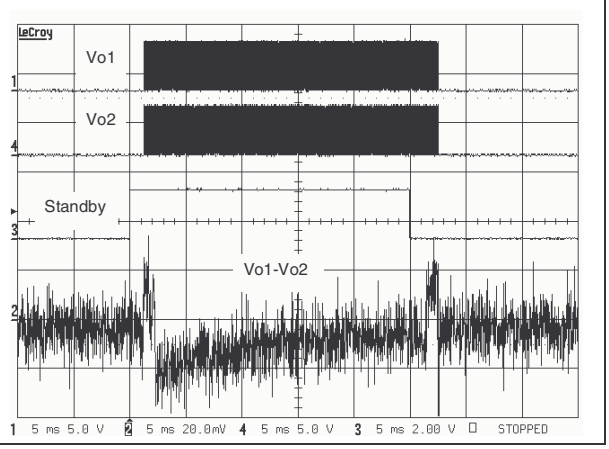


Figure 58. Startup & shutdown time Vcc=3V, G=6dB, CIN=100nF (5ms/div)

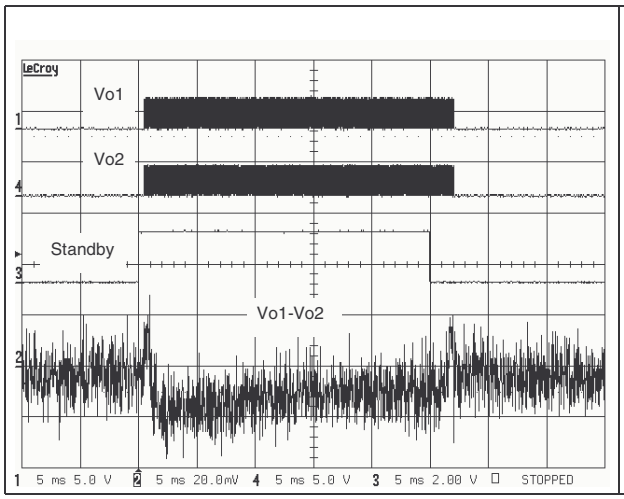


Figure 59. Startup & shutdown time Vcc=5V, G=6dB, NoCIN (5ms/div)

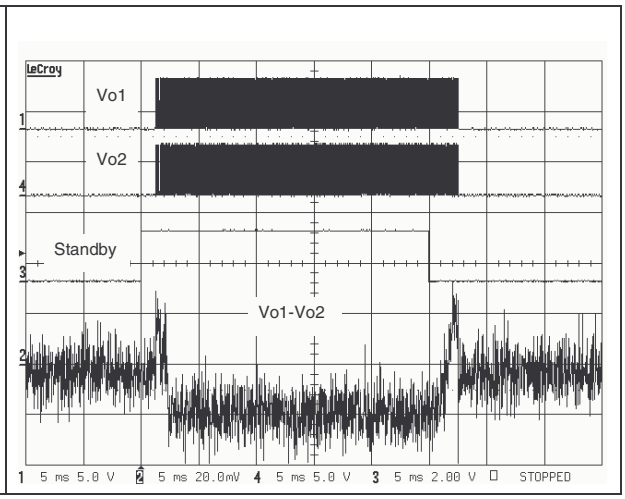
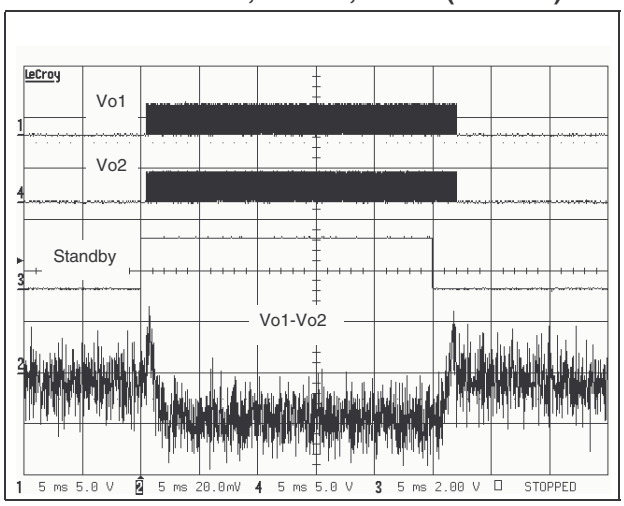


Figure 60. Startup & shutdown time Vcc=3V, G=6dB, NoCIN (5ms/div)



5 Application Information

5.1 Differential configuration principle

The TS4962M is a monolithic fully-differential input/output class D power amplifier. The TS4962M also includes a common-mode feedback loop that controls the output bias value to average it at Vcc/2 for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The advantages of a full-differential amplifier are:

- High PSRR (Power Supply Rejection Ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving an faster start-up time compared to conventional single-ended input amplifiers.
- Easier interfacing with differential output audio DAC.
- No input coupling capacitors required thanks to common mode feedback loop.

The main disadvantage is:

- As the differential function is directly linked to external resistor mismatching, paying particular attention to this mismatching is mandatory in order to obtain the best performance from the amplifier.

5.2 Gain in typical application schematic

Typical differential applications are shown in *Figure 1 on page 3*.

In the flat region of the frequency-response curve (no input coupling capacitor effect), the differential gain is expressed by the relation:

$$Av_{diff} = \frac{Out+ - Out-}{In+ - In-} = \frac{300}{R_{in}}$$

with Rin expressed in kΩ. For the remainder of this chapter, Avdiff will be referred to as Av for simplicity's sake.

Due to the tolerance of the internal 150kΩ feedback resistor, the differential gain will be in the range (no tolerance on Rin):

$$\frac{273}{R_{in}} \leq Av_{diff} \leq \frac{327}{R_{in}}$$

5.3 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at Vcc/2 for any DC common mode bias input voltage.

However, due to VICM limitation in the input stage (see *Table 2: Operating conditions on page 2*), the common mode feedback loop can ensure its role only within a defined range. This range depends upon the values of Vcc and Rin (Av). To have a good estimation of the VICM value, we can apply this formula (no tolerance on Rin):

$$V_{ICM} = \frac{Vcc \times R_{in} + 2 \times V_{IC} \times 150k\Omega}{2 \times (R_{in} + 150k\Omega)} \quad (V)$$

with

$$V_{IC} = \frac{In+ + In-}{2} \quad (V)$$

and the result of the calculation must be in the range:

$$0.5V \leq V_{ICM} \leq Vcc - 0.8V$$

Due to the +/-9% tolerance on the 150kΩ resistor, it's also important to check V_{ICM} in these conditions:

$$\frac{Vcc \times R_{in} + 2 \times V_{IC} \times 136.5k\Omega}{2 \times (R_{in} + 136.5k\Omega)} \leq V_{ICM} \leq \frac{Vcc \times R_{in} + 2 \times V_{IC} \times 163.5k\Omega}{2 \times (R_{in} + 163.5k\Omega)}$$

If the result of VICM calculation is not in the previous range, input coupling capacitors must be used (with Vcc from 2.4V to 2.5V, input coupling capacitors are mandatory).

For example:

With Vcc=3V, Rin=150k and VIC=2.5V, we found VICM=2V typically and this is lower than 3V-0.8V=2.2V. With 136.5kΩ we found 1.97V and with 163.5kΩ we have 2.02V. So, no input coupling capacitors are required.

5.4 Low frequency response

If a low frequency bandwidth limitation is requested, it's possible to use input coupling capacitors.

In the low frequency region, Cin (input coupling capacitor) starts to have an effect. Cin forms, with Rin, a first order high-pass filter with a -3dB cut-off frequency:

$$F_{CL} = \frac{1}{2 \times \pi \times R_{in} \times C_{in}} \quad (Hz)$$

So, for a desired cut-off frequency we can calculate Cin:

$$C_{in} = \frac{1}{2 \times \pi \times R_{in} \times F_{CL}} \quad (F)$$

With R_{in} in W and F_{CL} in Hz.

5.5 Decoupling of the circuit

A power supply capacitor is needed to correctly bypass the TS4962M, referred to as C_S.

The TS4962M has a typical switching frequency at 250kHz and output fall and rise time about 5ns. Due to these very fast transients, careful decoupling is mandatory.

A 1µF ceramic capacitor is enough, but it must be located very close to the TS4962M in order to avoid any extra parasitic inductance created an overly long track wire. These parasitic inductances introduce, in relation with dI/dt, overvoltage that decreases the global efficiency and may cause, if this parasitic inductance is too high, a TS4962M breakdown.

In addition, even if a ceramic capacitor has an adequate high frequency ESR value, its current capability is also important. A 0603 size is a good compromise, particularly when 4Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1µF/6.3V capacitor used at 5V, lose about 50% of its value. In fact at 5V power supply voltage, we have a decoupling value about 0.5µF instead of 1µF. As C_S has particular influence on the THD+N in the medium, high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoot that can be problematic if they reach the power supply AMR value (6V).

5.6 Wake-up Time: TWU

When the standby is released to set the device ON, there is a wait of about 5ms. The TS4962M has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

5.7 Shutdown time

When the standby command is set, the time required to put the two output stages into high impedance and to put the internal circuitry in shutdown mode, is about 5ms. This time is used to decrease the gain and avoid any pop noise during shutdown.

5.8 Consumption in shutdown mode

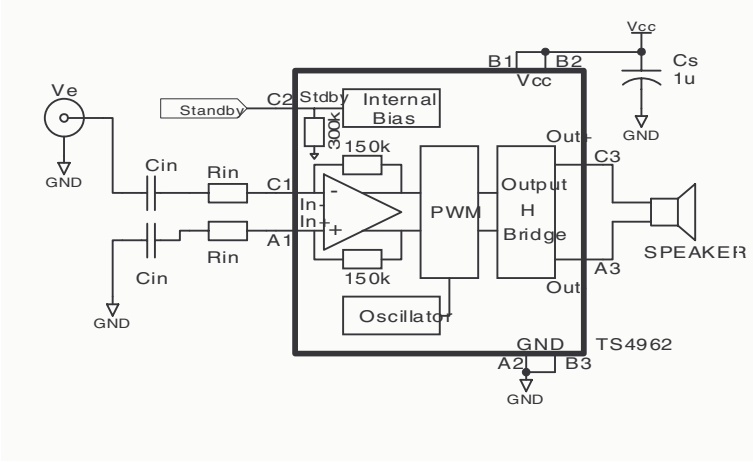
Between the shutdown pin and GND there is an internal 300kΩ resistor. This resistor force the TS4962M to be in shutdown when the shutdown input is leaved floating.

However, this resistor also introduces additional shutdown power consumption if the shutdown pin voltage is not 0V.

Referring to *Table 2: Operating conditions on page 2*, with 0.4V shutdown voltage pin for example, we have 0.4V/300k=1.3µA in typical (0.4V/273k=1.46µA in maximum) to add to the shutdown current specified in the tables in *Table 4 on page 4*.

5.9 Single ended input configuration

It's possible to use the TS4962M in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The following schematic shows a single ended input typical application.



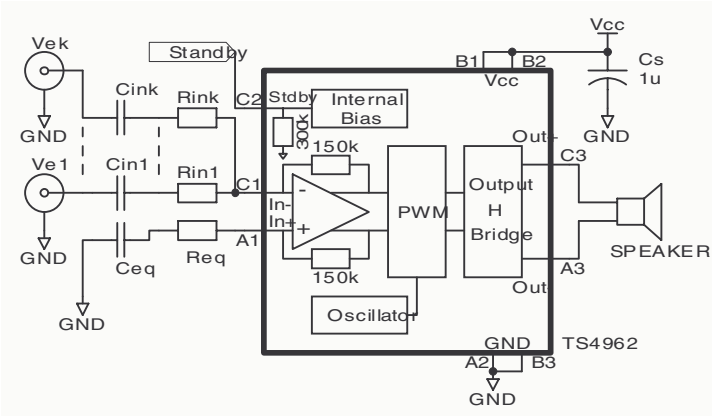
All formulas are identical except for the gain with Rin in kΩ:

$$Av_{single} = \frac{Ve}{Out+ - Out-} = \frac{300}{R_{in}}$$

And, due to the internal resistor tolerance we have:

$$\frac{273}{R_{in}} \leq Av_{single} \leq \frac{327}{R_{in}}$$

In the event that multiple single-ended inputs are summed, it is important that the impedance on both TS4962M inputs (In- and In+) are equal.



We have following equations:

$$Out + - Out - = V_{e1} \times \frac{300}{R_{in1}} + ... + V_{ek} \times \frac{300}{R_{ink}} \quad (V)$$

$$C_{eq} = \sum_{j=1}^{k} C_{inj}$$

$$C_{inj} = \frac{1}{2 \times \pi \times R_{inj} \times F_{CLj}} \quad (F)$$

$$R_{eq} = \frac{1}{\sum_{j=1}^{k} 1 \frac{1}{R_{inj}}}$$

In general, for mixed situations (single-ended and differential inputs) we must use the same rule: equalize impedance on both TS4962M inputs.

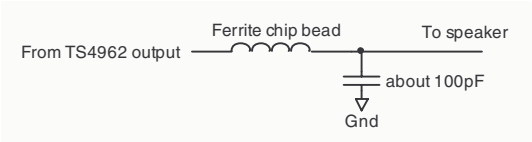
5.10 Output filter considerations

The TS4962M is designed to operate without an output filter. However, due to very sharp transients on TS4962M output, EMI radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS4962M outputs and loudspeaker terminal are long (typically more than 50mm, or 100mm in both directions, to the speaker terminals). As each PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow:

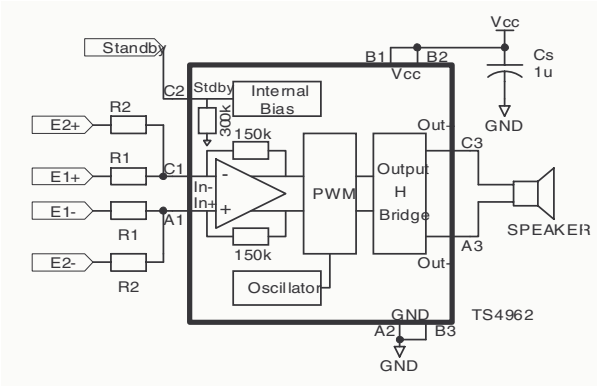
- Reduce, as much as possible, the distance between the TS4962M output pins and the speaker terminals.
- Uses ground plane for “shielding” sensitive wire.
- Place, as close as possible to the TS4962M and in series with each output, a ferrite bead with a rated current at minimum 2A and impedance greater than 50Ω at frequencies >30MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit. Murata BLM18EG221SN1 or BLM18EG121SN1 are possible examples.
- Allow a footprint to place, if necessary, a capacitor to short perturbations to ground (see following schematic).



In the case where distance between TS4962M's output and speaker terminals is high, it's possible to have low frequency EMI issues due to the fact that the typical operating frequency is 250kHz.
In this configuration, utilization of the output filter represented in page 3 and close of the TS4962M is necessary.

5.11 Different examples with summed inputs

Example 1: Dual differential inputs



With (Ri in kΩ)

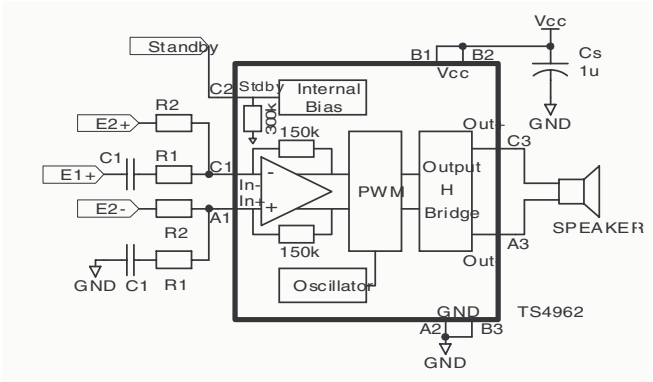
$$Av1 = \frac{Out+ - Out-}{E1+ - E1-} = \frac{300}{R1}$$

$$Av2 = \frac{Out+ - Out-}{E2+ - E2-} = \frac{300}{R2}$$

$$0.5V \le \frac{Vcc \times R1 \times R2 + 300 \times (V_{IC1} \times R2 + V_{IC2} \times R1)}{300 \times (R1 + R2) + 2 \times R1 \times R2} \le Vcc - 0.8V$$

$$V_{IC1} = \frac{E1+ + E1-}{2} \quad \text{and} \quad V_{IC2} = \frac{E2+ + E2-}{2}$$

Example 2: One differential input plus one single ended input



With (Ri in kΩ)

$$Av1 = \frac{Out+ - Out-}{E1+} = \frac{300}{R1}$$

$$Av2 = \frac{Out+ - Out-}{E2+ - E2-} = \frac{300}{R2}$$

$$C1 = \frac{1}{2 \times \pi \times R1 \times F_{CL}} \quad (F)$$

6 Demoboard

A demoboard for the TS4962M is available with a the flip-chip adapter flip-chip to DIP.

For more information about this demoboard, please refer to **Application Note AN2134.**

Figure 61. Schematic diagram of mono class D demoboard for TS4962M

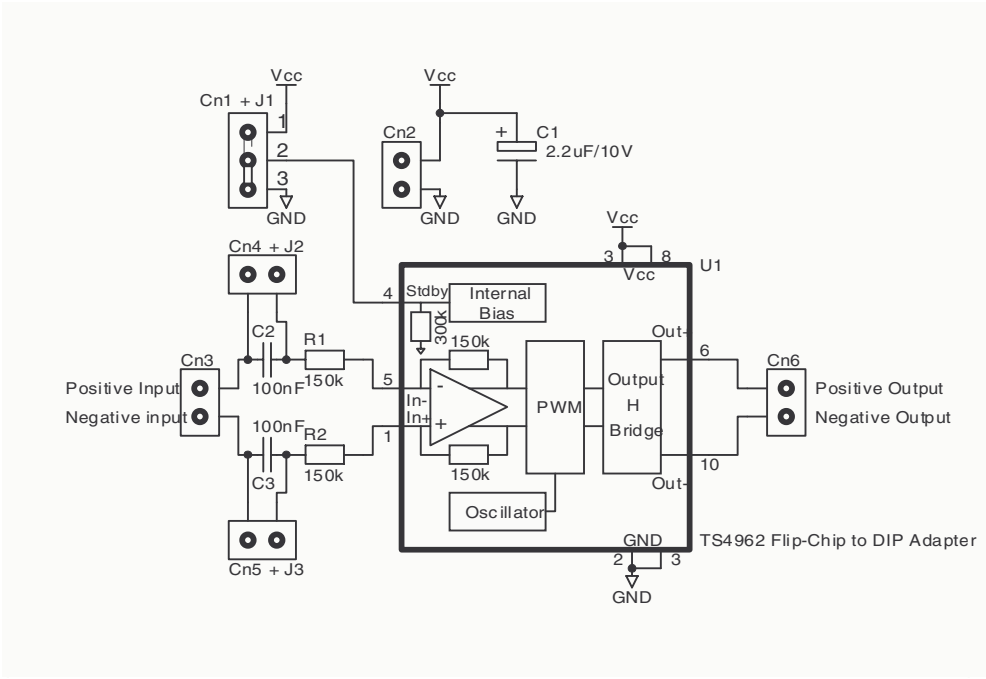


Figure 62. Diagram for flip-chip-to-DIP adapter

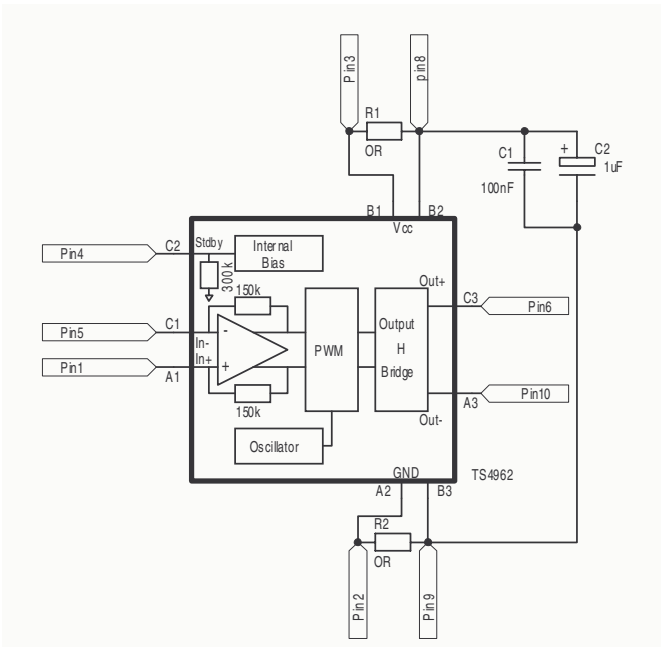


Figure 63. Top view

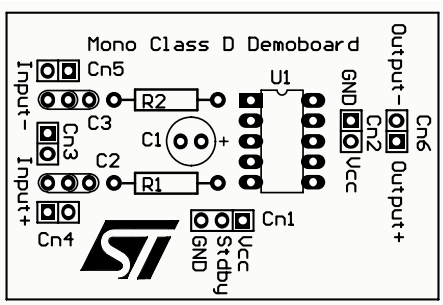


Figure 64. Bottom layer

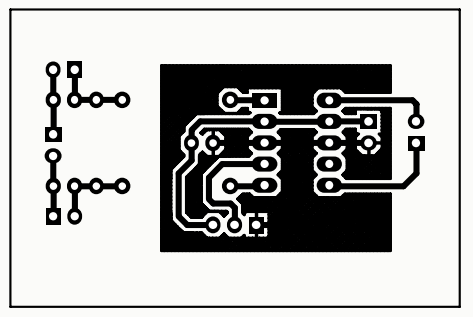
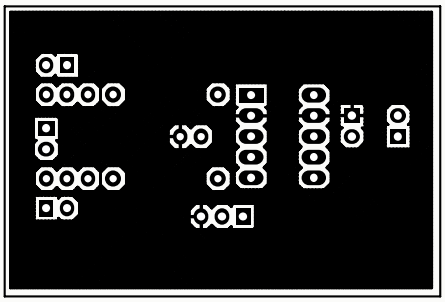
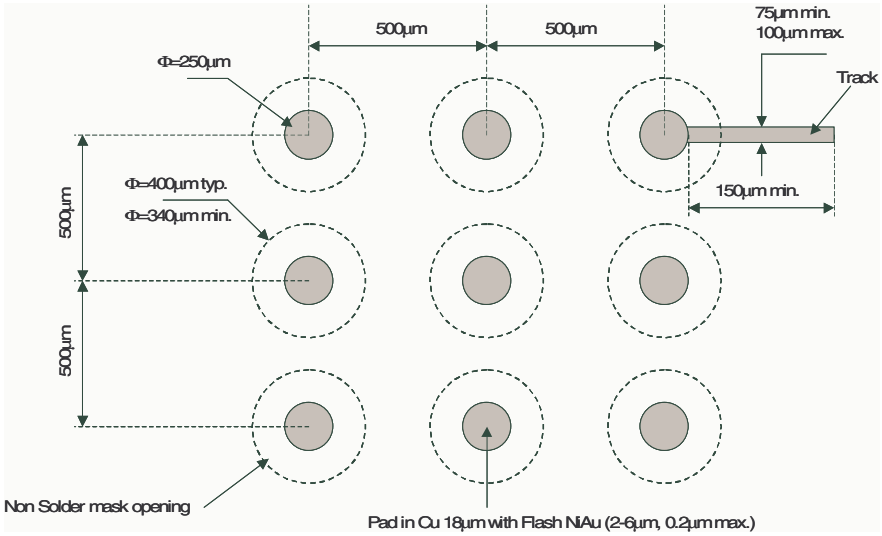


Figure 65. Top layer



7 Footprint recommendations

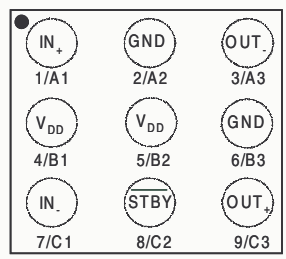
Figure 66. Footprint recommendations



8 Package Mechanical Data

9-bump flip-chip

Figure 67. Pin-out for 9-bump flip-chip (top view)

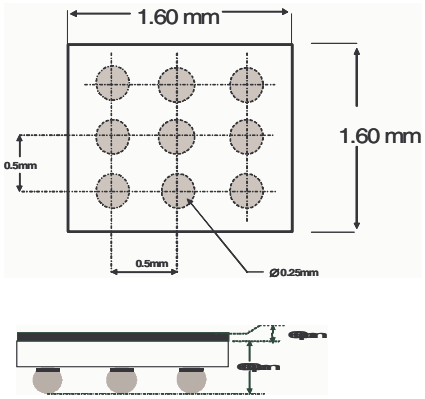


- Bumps are underneath
- Bump diameter = 300µm

Figure 68. Marking for 9-bump flip-chip (top view)

- ST Logo
- Symbol for lead-free: E
- Two first XX Product code: 62
- third X: Assembly Code
- Three digits Datecode: Y for Year - WW for week.
- The dot is for marking pin A1

Figure 69. Mechanical data for 9-bump flip-chip



- Die size: **1.6mm x 1.6mm** ±30µm
- Die height (including bumps): **600µm**
- Bump diameter: **315µm** ±**50µm**
- Bump diameter before Reflow: **300µm** ±**10µm**
- Bump height: **250µm** ±40**µm**
- Die Height: **350µm** ±20**µm**
- Pitch: **500µm** ±**50µm**
- *Back Coating layer Height: **60µm** ±**10µm**
- Coplanarity: **50µm max**

*** Optional**

9 Revision History

Date	Revision	Changes
Oct. 2005	1	First Release corresponding to the product preview version.