National Semiconductor

February 2006

LM4961 Boomer® Audio Power Amplifier Series
Ceramic Speaker Driver

General Description

The LM4961 is an audio power amplifier primarily designed for driving Ceramic Speaker for applications in Cell Phone and PDAs. It integrates a boost converter, with variable output voltage, with an audio power amplifier. It is capable of driving $15V_{p-p}$ in BTL mode to 2uF+ 30 ohms load, continuous average power, with less than 1% distortion (THD+N) from a $3.2V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal number of external components. The LM4961 does not require bootstrap capacitors, or snubber circuits therefore it is ideally suited for portable applications requiring high voltage output to drive capacitive loads like Ceramic Speakers. The LM4961 features a low-power consumption shutdown mode. Additionally, the LM4961 features an internal thermal shutdown protection mechanism.

The LM4961 contains advanced pop & click circuitry that eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4961 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- Quiescent Power Supply Current 7mA (typ)
- Voltage Swing in BTL at 1% THD 15Vp-p (typ)
- Shutdown current 0.1µA (typ)

Features

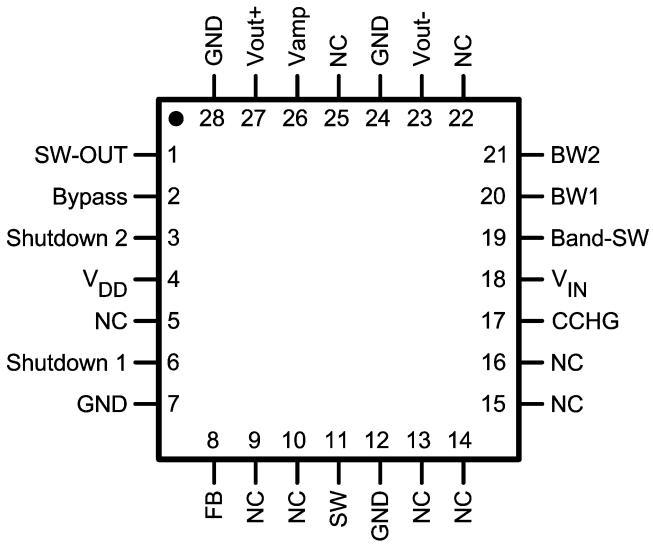
- Pop & click circuitry eliminates noise during turn-on and turn-off transitions
- Low current shutdown mode
- Low quiescent current
- Mono 15Vp-p BTL output, R_L = 2µF+30Ω, f = 1kHz
- Thermal shutdown protection
- Unity-gain stable
- External gain configuration capability
- Including Band exchange SW
- Including Leakage cut SW

Applications

- Cellphone
- PDA

Connection Diagram

LM4961LQ (5x5)



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Top View
Order Number LM4XXX
See NS Package Number

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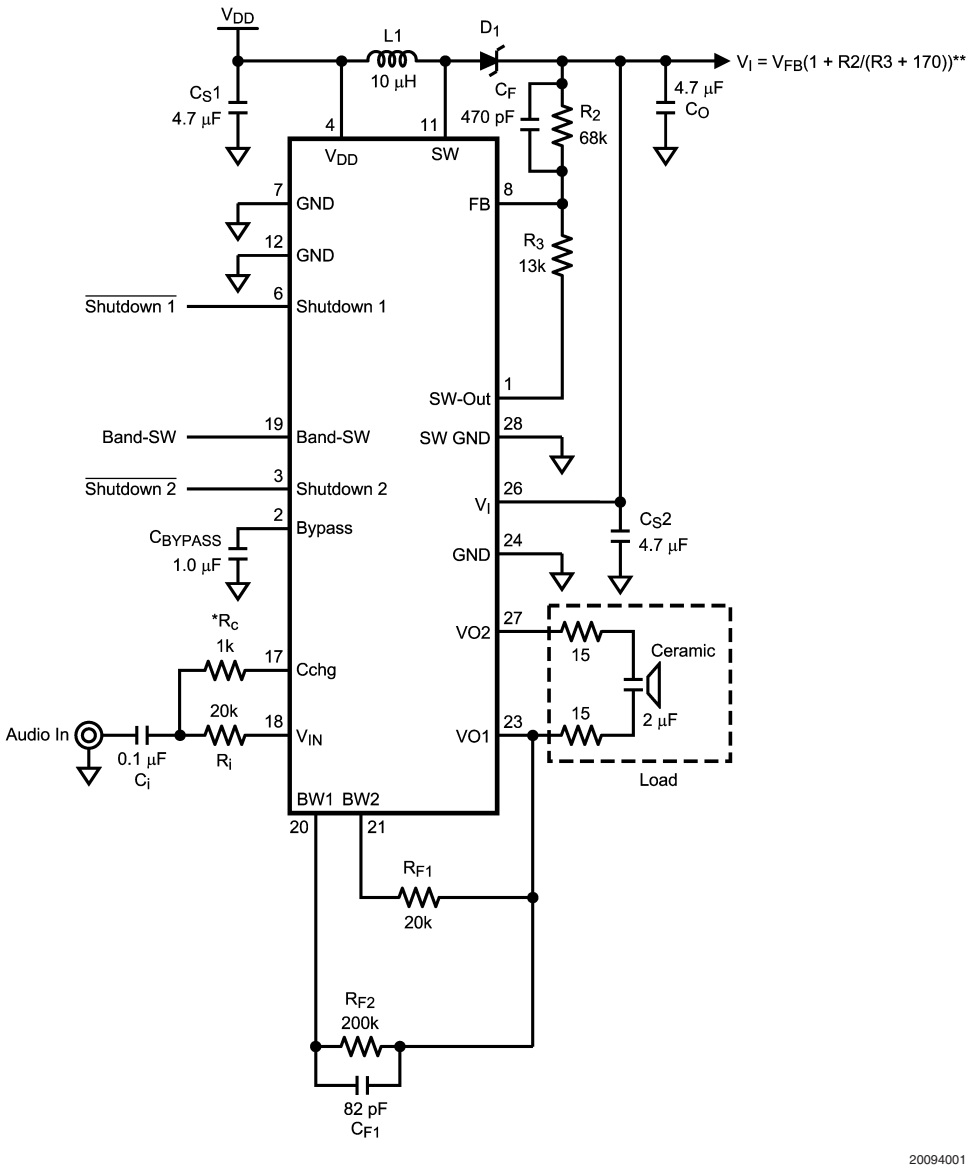
Typical Application



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* R_C is needed for over/under voltage protection. If inputs are less than V_{DD} +0.3V and greater than −0.3V, and if inputs are disabled when in shutdown mode, then R_C can be shorted.

** V_{FB} = 1.23V

FIGURE 1. Typical Audio Amplifier Application Circuit

	Shutdown 1	**Shutdown 2**	**Band-SW**
Receiver Mode (BW2)	—	high	low
Ringer Mode (BW1)	high	high	high
Shutdown	low	low	low

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{dd})	6.0V
Amplifier Supply Voltage (V_1)	9.5V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JA} (LLP)	66˚C/W

See AN-1187 'Leadless Leadframe Packaging (LLP).'

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40˚C \le T_A \le +85˚C$
Supply Voltage (V_{DD})	$3.0V < V_{DD} < 5.0V$
Amplifier Supply Voltage (V_1)	$2.7V < V_1 < 9.0V$

Electrical Characteristics V_{DD} = 4.2V

The following specifications apply for V_{DD} = 4.2V, $A_{V\text{-}BTL}$ = 26dB, R_L = 2µF+30Ω, Cb = 1.0µF, Band-SW = V_{DD} unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4961		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, No Load Band-SW = V_{DD}	7	14	mA (max)
Iddrcv	Iq in receiver mode	V_{IN} = 0V, No Load Band-SW = GND	2	4	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN1}$ = $V_{SHUTDOWN2}$ = GND Band-SW = GND (Note 9)	0.1	2.0	µA (max)
V_{LH}	Logic High Threshold Voltage	For Shutdown 1, Shutdown 2, and Band-SW		1.5	V (min)
V_{LL}	Logic Low Threshold Voltage	For Shutdown 1, Shutdown 2, and Band-SW		0.4	V (max)
$R_{PULLDOWN}$	Pulldown Resistor	For Shutdown 2 and Band-SW	70k	50k	Ω (min)
TSD	Thermal Shutdown Temperature			125	˚C (min)
V_{out}	Output Voltage Swing	THD = 1%, f = 1kHz R_L = 2µF+30Ω Mono BTL	15	14	Vp-p (min)
THD+N	Total Harmomic Distortion + Noise	V_{out} = 14Vp-p, f = 1kHz	0.05	1.0	% (max)
ϵ_{OS}	Output Noise	A-Weighted Filter, V_{IN} = 0V (Note 10)	115		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200m$V_{p\text{-}p}$, f = 100Hz	80	65	dB (min)
Ron-sw-out	On Resistance on SW-Out	Band SW "High" Isink = 100µA (Between pin 1 and pin 28)	170	220	Ω (max)

Electrical Characteristics V_{DD} = 3.2V

The following specifications apply for V_{DD} = 3.2V, $A_{V\text{-}BTL}$ = 26dB, R_L = 2µF+30Ω, Cb = 1.0µF, Band-SW = V_{DD} unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4961		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, No Load Band-SW = V_{DD}	9	15	mA (max)
Iddrcv	Iq in receiver mode	V_{IN} = 0V, No Load Band-SW = GND	2	4	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN1}$ = $V_{SHUTDOWN2}$ = GND Band-SW = GND (Note 9)	0.1	2.0	µA (max)

Electrical Characteristics V_{DD} = 3.2V (Continued)

The following specifications apply for V_{DD} = 3.2V, $A_{V\text{-}BTL}$ = 26dB, R_L = 2µF+30Ω, Cb = 1.0µF, Band-SW = V_{DD} unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4961		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
V_{LH}	Logic High Threshold Voltage	For Shutdown 1, Shutdown 2, and Band-SW		1.5	V (min)
V_{LL}	Logic Low Threshold Voltage	For Shutdown 1, Shutdown 2, and Band-SW		0.4	V (max)
$R_{PULLDOWN}$	Pulldown Resistor	For Shutdown 2 and Band-SW	70k	50k	Ω (min)
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V_{out}	Output Voltage Swing	THD = 1%, f = 1kHz R_L = 2µF+30Ω Mono BTL	15	14	Vp-p (min)
THD+N	Total Harmomic Distortion + Noise	V_{out} = 14Vp-p, f = 1kHz	0.1	1.0	% (max)
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Ron-sw-out	On Resistance on SW-Out	Band SW “High” Isink = 100µA (Between pin 1 and pin 28)	170	220	Ω (max)

Note 1: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the given in Absolute Maximum Ratings, whichever is lower. For the LM4961 typical application (shown in *Figure 1*) with V_{DD} = 4.2V, R_L = 2µF+30Ω mono BTL operation the maximum power dissipation is 232mW. θ_{JA} = 66˚C/W.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

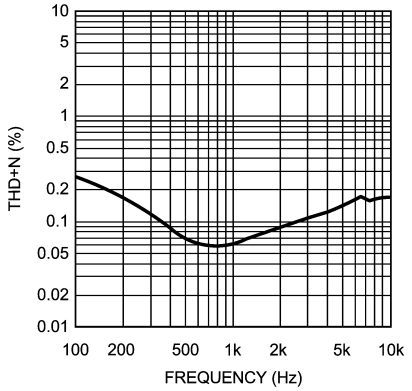
Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: Shutdown current is measured in a normal room environment. The Shutdown pin should be driven as close as possible to GND for minimum shutdown current.

Note 10: Noise measurements are dependent on the absolute values of closed loop gain setting resistors (input and feedback resistors).

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 4.2V, V_O = 14V_{P-P}, R_L = 2µF+30Ω



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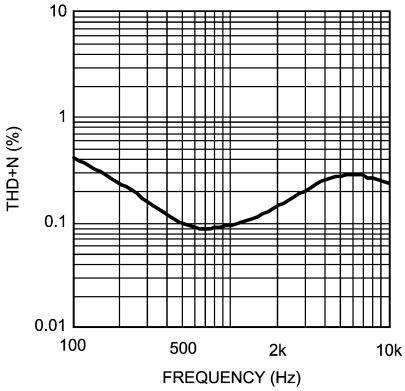
THD+N vs Frequency
V_{DD} = 3.2V, V_O = 14V_{P-P}, R_L = 2µF+30Ω



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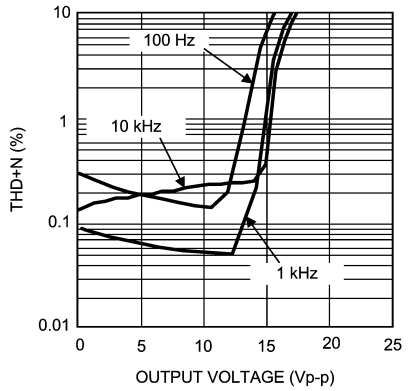
THD+N vs Output Voltage
V_{DD} = 4.2V, R_L = 2µF + 30Ω



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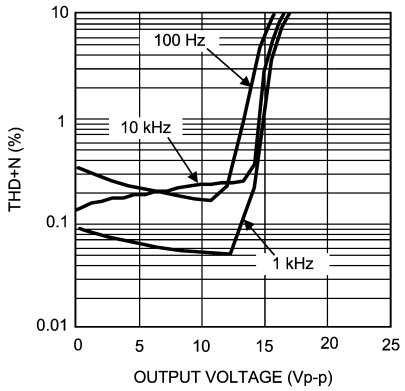
THD+N vs Output Voltage
V_{DD} = 3.2V, R_L = 2µF + 30Ω



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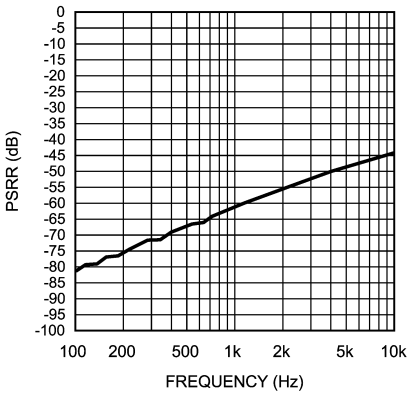
PSRR vs Frequency
V_{DD} = 4.2V, R_L = 8Ω, V_{RIPPLE} = 200mV_{P-P}



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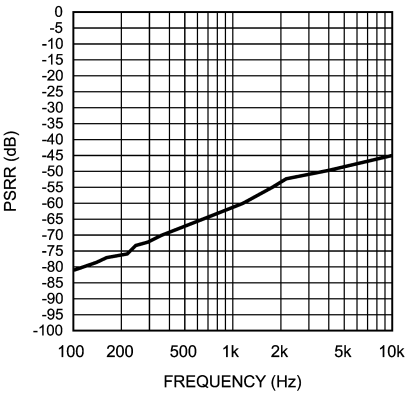
PSRR vs Frequency
V_{DD} = 3.2V, R_L = 8Ω, V_{RIPPLE} = 20mV_{P-P}



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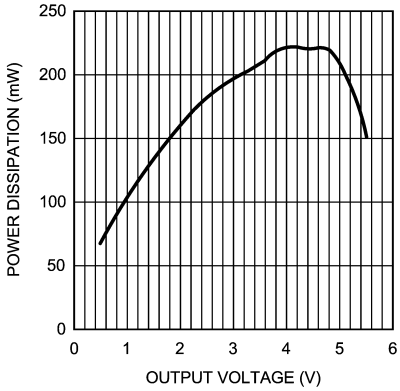
Typical Performance Characteristics (Continued)

Power Dissipation vs Output Power
V_{DD} = 4.2V, R_L = 2µF + 30Ω, f = 1kHz



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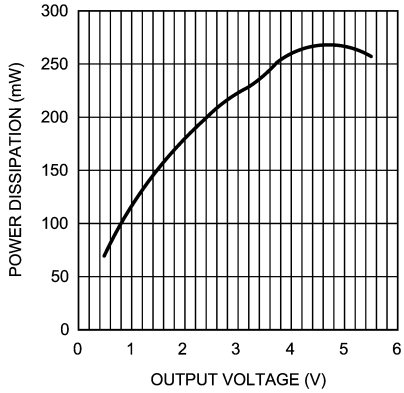
Power Dissipation vs Output Power
V_{DD} = 3.2V, R_L = 2µF + 30Ω, f = 1kHz



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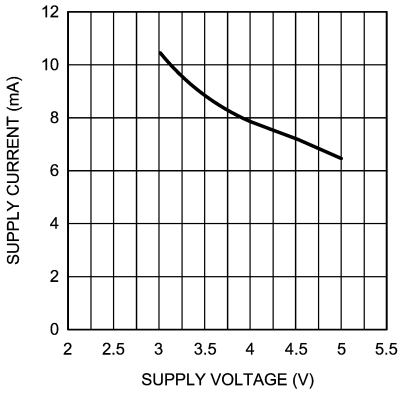
Supply Current vs Supply Voltage
R_L = 2µF + 30Ω, V_{IN} = 0V, R_{SOURCE} = 50Ω



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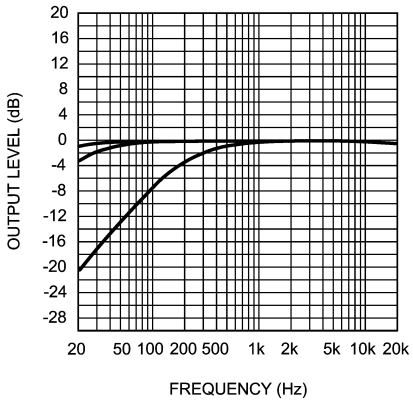
Frequency Response vs Input Capacitor Size
R_L = 8Ω
from top to bottom:
C_i = 1.0µF, C_i = 0.39µF, C_i = 0.039µF



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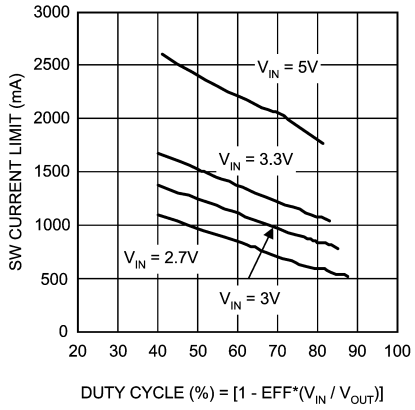
Switch Current Limit vs Duty Cycle



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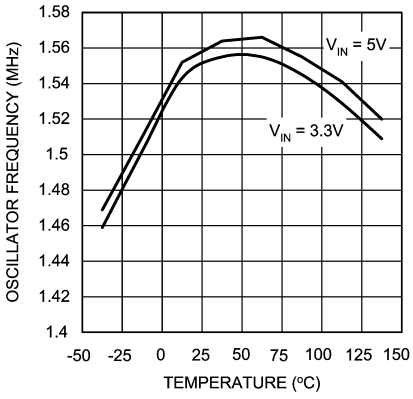
Oscillator Frequency vs Temperature



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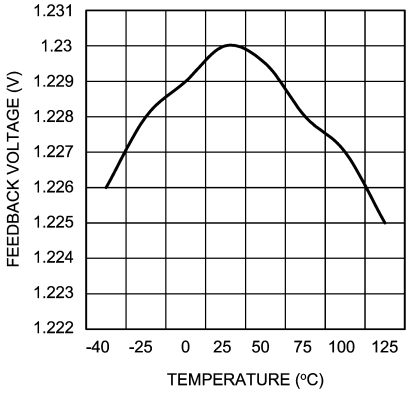
Typical Performance Characteristics (Continued)

Feedback Voltage vs Temperature



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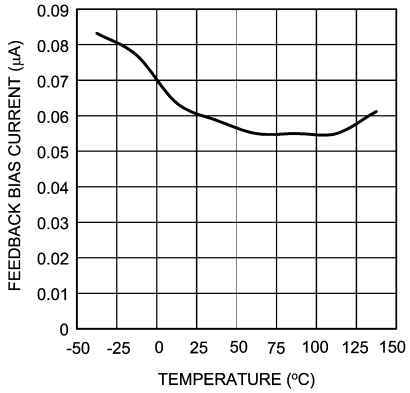
Feedback Bias Current vs Temperature



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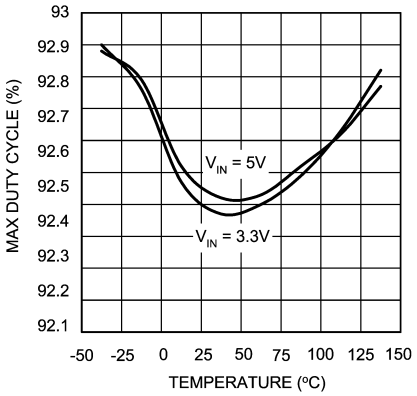
Max. Duty Cycle vs Temperature - "X"



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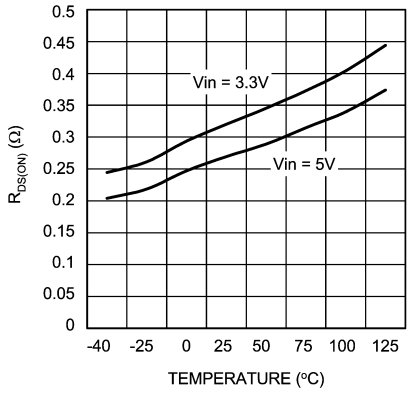
R_{DS} (ON) vs Temperature



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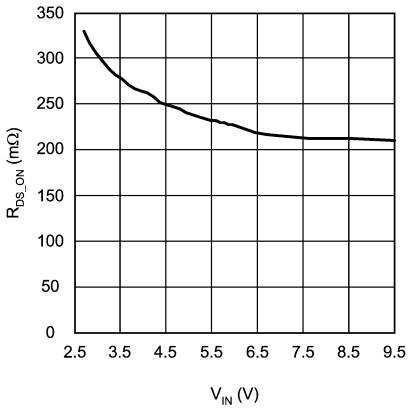
R_{DS} (ON) vs V_{DD}



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Application Information

BRIDGE CONFIGURATION EXPLANATION

The Audio Amplifier portion of the LM4961 has two internal amplifiers allowing different amplifier configurations. The first amplifier's gain is externally configurable, whereas the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of Rf to Ri while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two. This results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the Audio Amplifier is

$$A_{VD} = 2 * (Rf/Ri)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classic single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration. It provides differential drive to the load, thus doubling the output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions.

The bridge configuration also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

BOOST CONVERTER POWER DISSIPATION

At higher duty cycles, the increased ON-time of the switch FET means the maximum output current will be determined by power dissipation within the LM4961 FET switch. The switch power dissipation from ON-time conduction is calculated by Equation 2.

$$P_{D(SWITCH)} = DC \times I_{IND}(AVE)^2 \times R_{DS}(ON) \quad (1)$$

where DC is the duty cycle.

There will be some switching losses as well, so some derating needs to be applied when calculating IC power dissipation.

MAXIMUM AMPLIFIER POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the amplifier portion of the LM4961 has two operational amplifiers, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given BTL application can be derived from Equation 1.

$$P_{DMAX(AMP)} = (2V_{DD}^2) / (\pi^2 R_L) \quad (2)$$

where

$$R_L = R_o1 + R_o2$$

MAXIMUM TOTAL POWER DISSIPATION

The total power dissipation for the LM4961 can be calculated by adding Equation 1 and Equation 2 together to establish Equation 3:

$$P_{DMAX(TOTAL)} = (2V_{DD}^2) / (\pi^2 EFF^2 R_L) \quad (3)$$

where

EFF = Efficiency of boost converter

$R_L = R_o1 + R_o2$

The result from Equation 3 must not be greater than the power dissipation that results from Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta JA \quad (4)$$

For the LQA28A, θ_{JA} = 66˚C/W. T_{JMAX} = 125˚C for the LM4961. Depending on the ambient temperature, T_A, of the system surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than that of Equation 4, then either the supply voltage must be increased, the load impedance increased or T_A reduced. For the typical application of a 4.2V power supply, with a 2uF+30Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 109˚C provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output levels.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4961's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. The low thermal resistance allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air. The LD package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LD (LLP) package is found in National Semiconductor's Package Engineering Group under application note AN1187.

SHUTDOWN FUNCTION

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch connected between V_{DD} and Shutdown pins.

Application Information (Continued)

BAND SWITCH FUNCTION

The LM4961 features a Band Switch function which allows the user to use one amplifier for both receiver (earpiece) mode and ringer/loudspeaker mode. When a logic high (V_{DD}) is applied to the Band-SW pin (pin 19) the amplifier is in ringer mode. This enables the boost converter and sets the externally configurable closed loop gain selection to BW1. If the Band-SW pin has a logic low (GND) applied to its terminal then the device is in receiver mode. In this mode the boost converter is disabled and the gain selection is switched to BW2. This allows the amplifier to be powered directly from the battery minus the voltage drop across the Schottky diode.

REDUCING TRANSIENT CURRENT SPIKE

Due to the quick turn-on time of the Boost Converter, a transient supply current spike is observed on shutdown release. To reduce the rise time of the output voltage (V_1), thus reducing the value of the supply current spike, please refer to application circuit in Figure 2. Using this configuration will allow the user to reduce the transient supply current spike without the Boost Converter experiencing any stability issues.

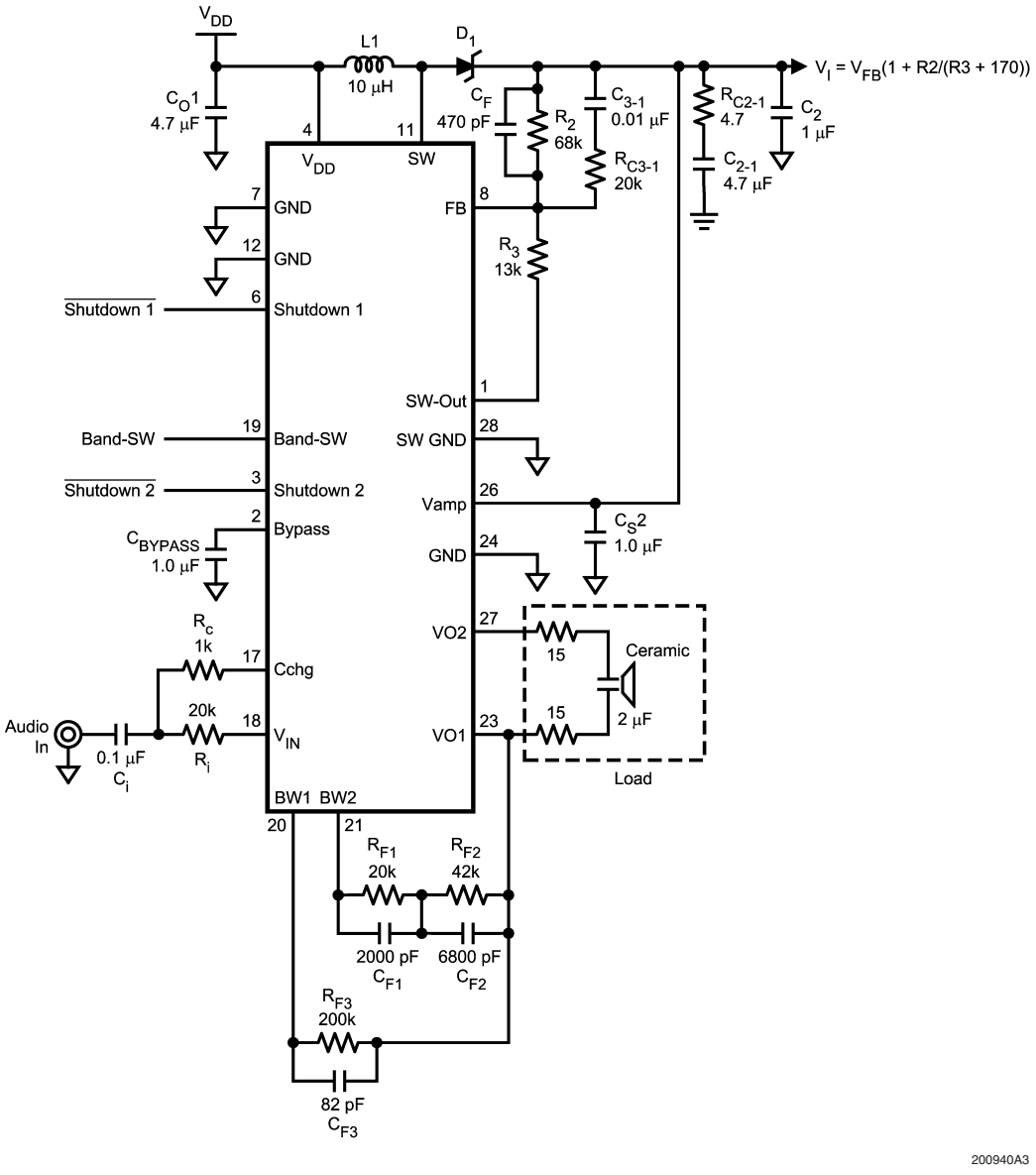

FIGURE 2. Transient Current Spike Reduction Configuration

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers, and switching DC-DC converters, is critical for optimizing device and system performance. Consideration to component values must be used to maximize overall system quality.

Application Information (Continued)

The best capacitors for use with the switching converter portion of the LM4961 are multi-layer ceramic capacitors. They have the lowest ESR (equivalent series resistance) and highest resonance frequency, which makes them optimum for high frequency switching converters.

When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer's data curves before selecting a capacitor. High-quality ceramic capacitors can be obtained from Taiyo-Yuden.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both V1 and V_{DD} pins should be as close to the device as possible.

SELECTING INPUT CAPACITOR FOR AUDIO AMPLIFIER

One of the major considerations is the closedloop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

High value input capacitors are both expensive and space hungry in portable designs. Clearly, a certain value capacitor is needed to couple in low frequencies without severe attenuation. But ceramic speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a high value input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is affected by the value of the input coupling capacitor, C_i. A high value input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor value based on desired low frequency response, turn-on pops can be minimized.

SELECTING BYPASS CAPACITOR FOR AUDIO AMPLIFIER

Besides minimizing the input capacitor value, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the amplifer turns on. The slower the amplifier's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.039µF to 0.39µF), should produce a virtually clickless and popless shutdown function. Although the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0µF is recommended in all but the most cost sensitive designs.

SELECTING FEEDBACK CAPACITOR FOR AUDIO AMPLIFIER

The LM4961 is unity-gain stable which gives the designer maximum system flexability. However, to drive ceramic speakers, a typical application requires a closed-loop differential gain of 10. In this case a feedback capacitor (C_f2) will be needed as shown in Figure 1 to bandwidth limit the amplifier.

This feedback capacitor creates a low pass filter that eliminates possible high frequency noise. Care should be taken when calculating the -3dB frequency because an incorrect combination of R_f and C_f2 will cause rolloff before the desired frequency

SELECTING OUTPUT CAPACITOR (C_O) FOR BOOST CONVERTER

A single 4.7µF to 10µF ceramic capacitor will provide sufficient output capacitance for most applications. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used. Aluminum electrolytics with ultra low ESR such as Sanyo Oscon can be used, but are usually prohibitively expensive. Typical Al electrolytic capacitors are not suitable for switching frequencies above 500 kHz because of significant ringing and temperature rise due to self-heating from ripple current. An output capacitor with excessive ESR can also reduce phase margin and cause instability.

In general, if electrolytics are used, we recommended that they be paralleled with ceramic capacitors to reduce ringing, switching losses, and output voltage ripple.

SELECTING INPUT CAPACITOR (Cs1) FOR BOOST CONVERTER

An input capacitor is required to serve as an energy reservoir for the current which must flow into the coil each time the switch turns ON. This capacitor must have extremely low ESR, so ceramic is the best choice. We recommend a nominal value of 4.7µF, but larger values can be used. Since this capacitor reduces the amount of voltage ripple seen at the input pin, it also reduces the amount of EMI passed back along that line to other circuitry.

SETTING THE OUTPUT VOLTAGE (V_1) OF BOOST CONVERTER

The output voltage is set using the external resistors R_2 and R_3 (see Figure 1). A value of approximately 13.3kΩ is recommended for R_3 to establish a divider current of approximately 92µA. R_2 is calculated using the formula:

$$V_1 = V_{FB} [1 + R_2(R_3 + 170)] \quad (5)$$

FEED-FORWARD COMPENSATION FOR BOOST CONVERTER

Although the LM4961's internal Boost converter is internally compensated, the external feed-forward capacitor C_f is required for stability (see Figure 1). Adding this capacitor puts a zero in the loop response of the converter. The recommended frequency for the zero fz should be approximately 6kHz. C_f1 can be calculated using the formula:

$$C_f1 = 1 / (2\pi \times R_1 \times fz) \quad (6)$$

Application Information (Continued)

SELECTING DIODES

The external diode used in Figure 1 should be a Schottky diode. A 20V diode such as the MBR0520 from Fairchild Semiconductor is recommended.

The MBR05XX series of diodes are designed to handle a maximum average current of 0.5A. For applications exceeding 0.5A average but less than 1A, a Microsemi UPS5817 can be used.

DUTY CYCLE

The maximum duty cycle of the boost converter determines the maximum boost ratio of output-to-input voltage that the converter can attain in continuous mode of operation. The duty cycle for a given boost application is defined as:

$$\text{Duty Cycle} = V_{OUT} + V_{DIODE} - V_{IN} \,/\, V_{OUT} + V_{DIODE} - V_{SW}$$

This applies for continuous mode operation.

INDUCTANCE VALUE

The first question we are usually asked is: "How small can I make the inductor." (because they are the largest sized component and usually the most costly). The answer is not simple and involves trade-offs in performance. Larger inductors mean less inductor ripple current, which typically means less output voltage ripple (for a given size of output capacitor). Larger inductors also mean more load power can be delivered because the energy stored during each switching cycle is:

$$E = L/2 \times (Ip)2$$

Where "Ip" is the peak inductor current. An important point to observe is that the LM4961 will limit its switch current based on peak current. This means that since Ip(max) is fixed, increasing L will increase the maximum amount of power available to the load. Conversely, using too little inductance may limit the amount of load current which can be drawn from the output.

Best performance is usually obtained when the converter is operated in "continuous" mode at the load current range of interest, typically giving better load regulation and less output ripple. Continuous operation is defined as not allowing the inductor current to drop to zero during the cycle. It should be noted that all boost converters shift over to discontinuous operation as the output load is reduced far enough, but a larger inductor stays "continuous" over a wider load current range.

To better understand these trade-offs, a typical application circuit (5V to 12V boost with a 10µH inductor) will be analyzed. We will assume:

$$V_{IN} = 5V,\ V_{OUT} = 12V,\ V_{DIODE} = 0.5V,\ V_{SW} = 0.5V$$

Since the frequency is 1.6MHz (nominal), the period is approximately 0.625µs. The duty cycle will be 62.5%, which means the ON-time of the switch is 0.390µs. It should be noted that when the switch is ON, the voltage across the inductor is approximately 4.5V. Using the equation:

$$V = L\ (di/dt)$$

We can then calculate the di/dt rate of the inductor which is found to be 0.45 A/µs during the ON-time. Using these facts, we can then show what the inductor current will look like during operation:

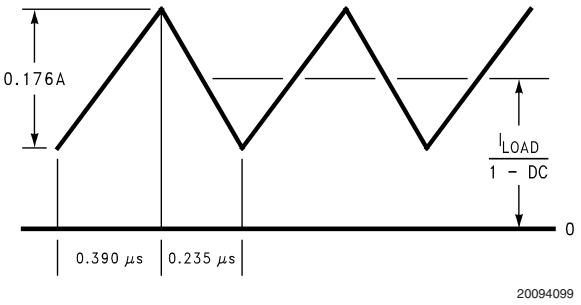

FIGURE 3. 10µH Inductor Current 5V - 12V Boost (LM4961X)

During the 0.390µs ON-time, the inductor current ramps up 0.176A and ramps down an equal amount during the OFF-time. This is defined as the inductor "ripple current". It can also be seen that if the load current drops to about 33mA, the inductor current will begin touching the zero axis which means it will be in discontinuous mode. A similar analysis can be performed on any boost converter, to make sure the ripple current is reasonable and continuous operation will be maintained at the typical load current values. Taiyo-Yudens NR4012 inductor series is recommended.

MAXIMUM SWITCH CURRENT

The maximum FET switch current available before the current limiter cuts in is dependent on duty cycle of the application. This is illustrated in a graph in the typical performance characterization section which shows typical values of switch current as a function of effective (actual) duty cycle.

CALCULATING OUTPUT CURRENT OF BOOST CONVERTER (I_{AMP})

As shown in Figure 2 which depicts inductor current, the load current is related to the average inductor current by the relation:

$$I_{LOAD} = I_{IND}(AVG) \times (1 - DC) \quad (7)$$

Where "DC" is the duty cycle of the application. The switch current can be found by:

$$I_{SW} = I_{IND}(AVG) + 1/2\ (I^{RIPPLE}) \quad (8)$$

Inductor ripple current is dependent on inductance, duty cycle, input voltage and frequency:

$$I_{RIPPLE} = DC \times (V_{IN}\text{-}V_{SW}) \,/\, (f \times L) \quad (9)$$

combining all terms, we can develop an expression which allows the maximum available load current to be calculated:

$$I_{LOAD}(max) = (1-DC)x(I_{SW}(max)-DC(V_{IN}\text{-}V_{SW}))/2FL \quad (10)$$

Application Information (Continued)

The equation shown to calculate maximum load current takes into account the losses in the inductor or turn-OFF switching losses of the FET and diode.

DESIGN PARAMETERS V_{SW} AND I_{SW}

The value of the FET "ON" voltage (referred to as V_{SW} in equations 7 thru 10) is dependent on load current. A good approximation can be obtained by multiplying the "ON Resistance" of the FET times the average inductor current.

FET on resistance increases at V_{IN} values below 5V, since the internal N-FET has less gate voltage in this input voltage range (see Typical Performance Characteristics curves). Above V_{IN} = 5V, the FET gate voltage is internally clamped to 5V.

The maximum peak switch current the device can deliver is dependent on duty cycle. For higher duty cycles, see Typical Performance Characteristics curves.

INDUCTOR SUPPLIERS

The recommended inductors for the LM4961 is the Taiyo-Yuden NR4012. When selecting an inductor, make certain that the continuous current rating is high enough to avoid saturation at peak currents. A suitable core type must be used to minimize core (switching) losses, and wire power losses must be considered when selecting the current rating.

PCB LAYOUT GUIDELINES

High frequency boost converters require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LM4961 device. It is recommended that a 4-layer PCB be used so that internal ground planes are available. See Figures 4–7 for demo board reference schematic and layout.

Some additional guidelines to be observed:

1. Keep the path between L1, D1, and Co extremely short. Parasitic trace inductance in series with D1 and Co will increase noise and ringing.

2. The feedback components R1, R2 and C_f 1 must be kept close to the FB pin of U1 to prevent noise injection on the FB pin trace.

3. If internal ground planes are available (recommended) use vias to connect directly to ground at pin 2 of U1, as well as the negative sides of capacitors C_s1 and Co.

GENERAL MIXED-SIGNAL LAYOUT RECOMMENDATION

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will take require a greater amount of design time but will not increase the final price of the board. The only extra parts required may be some jumpers.

Single-Point Power / Ground Connection

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to place digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and crosstalk.

Schematic Board Layout

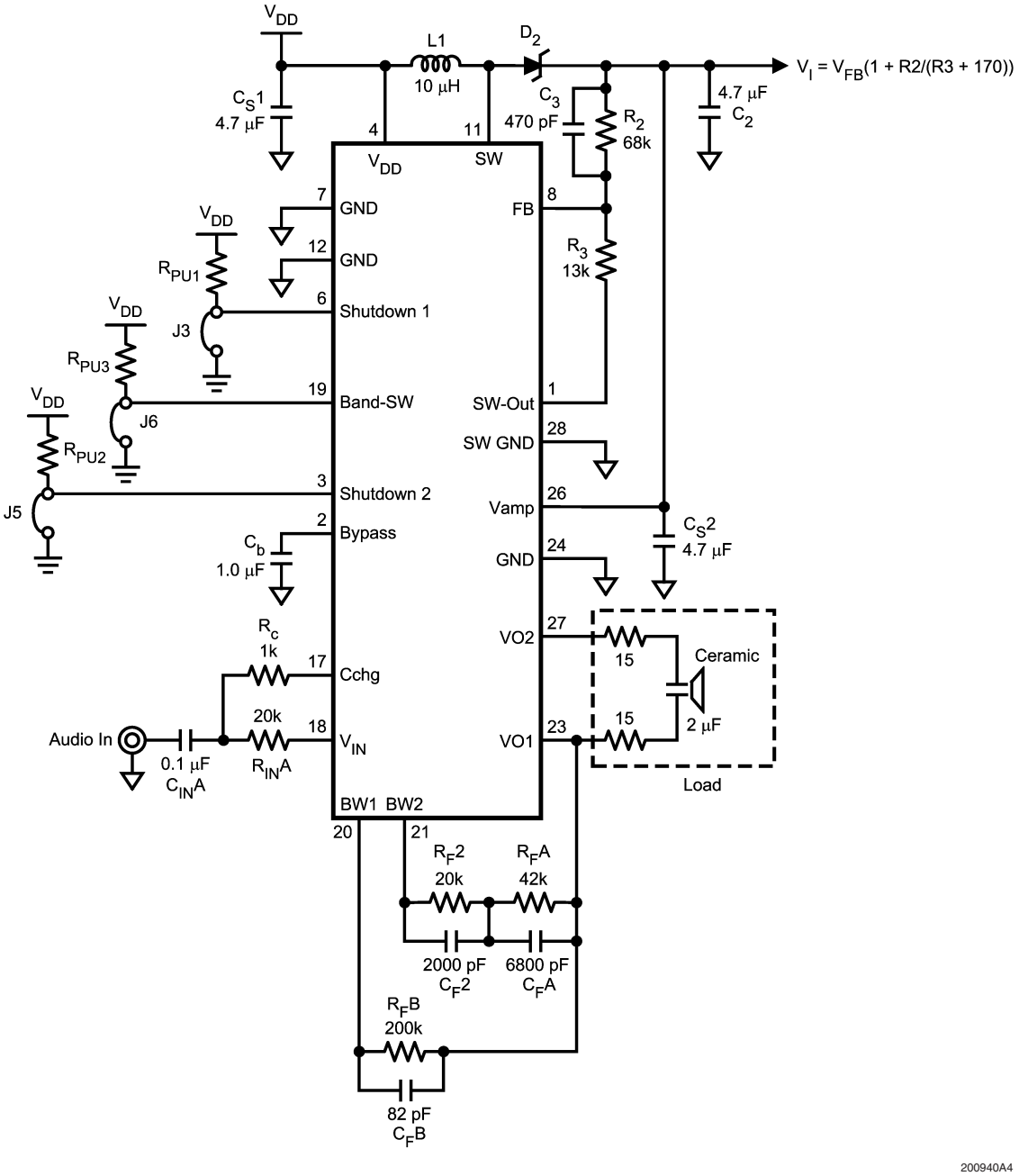

FIGURE 4. Demo Board Schematic

Demonstration Board Layout

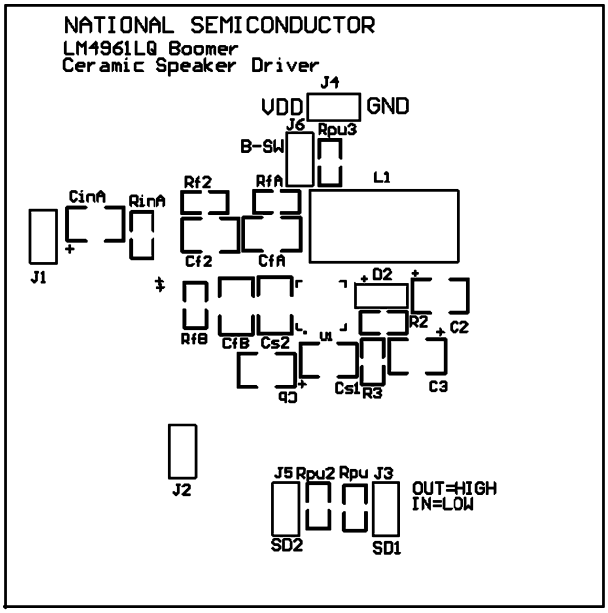

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FIGURE 5. Recommended TS SE PCB Layout: Top Silkscreen

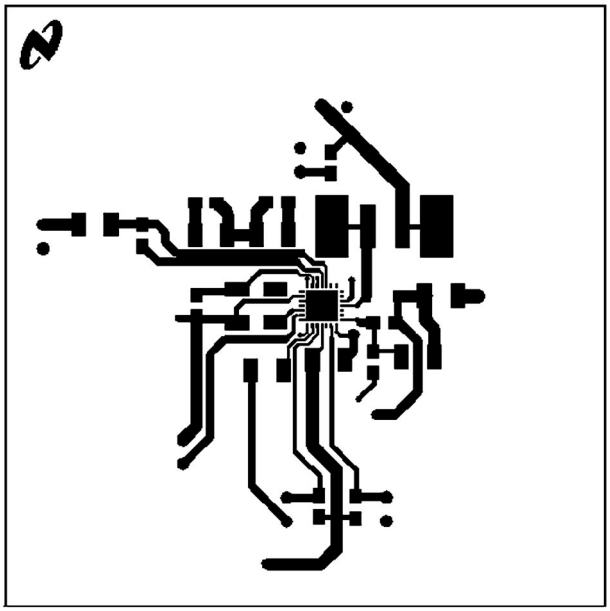

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FIGURE 6. Recommended TS SE PCB Layout: Top Layer

Demonstration Board Layout (Continued)

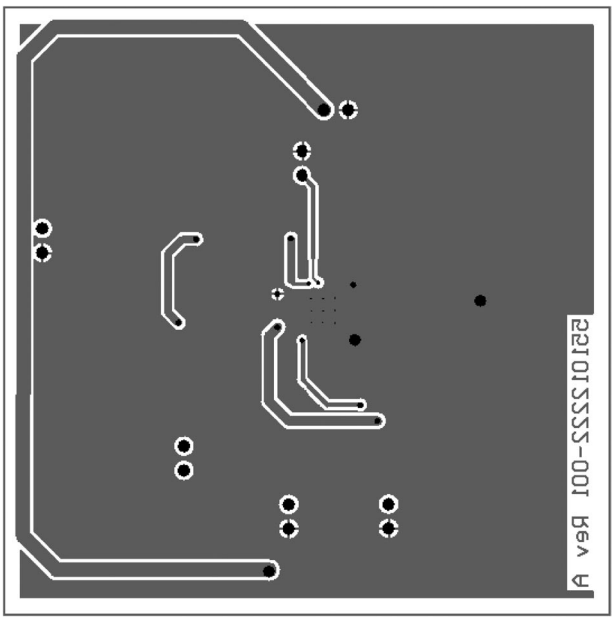

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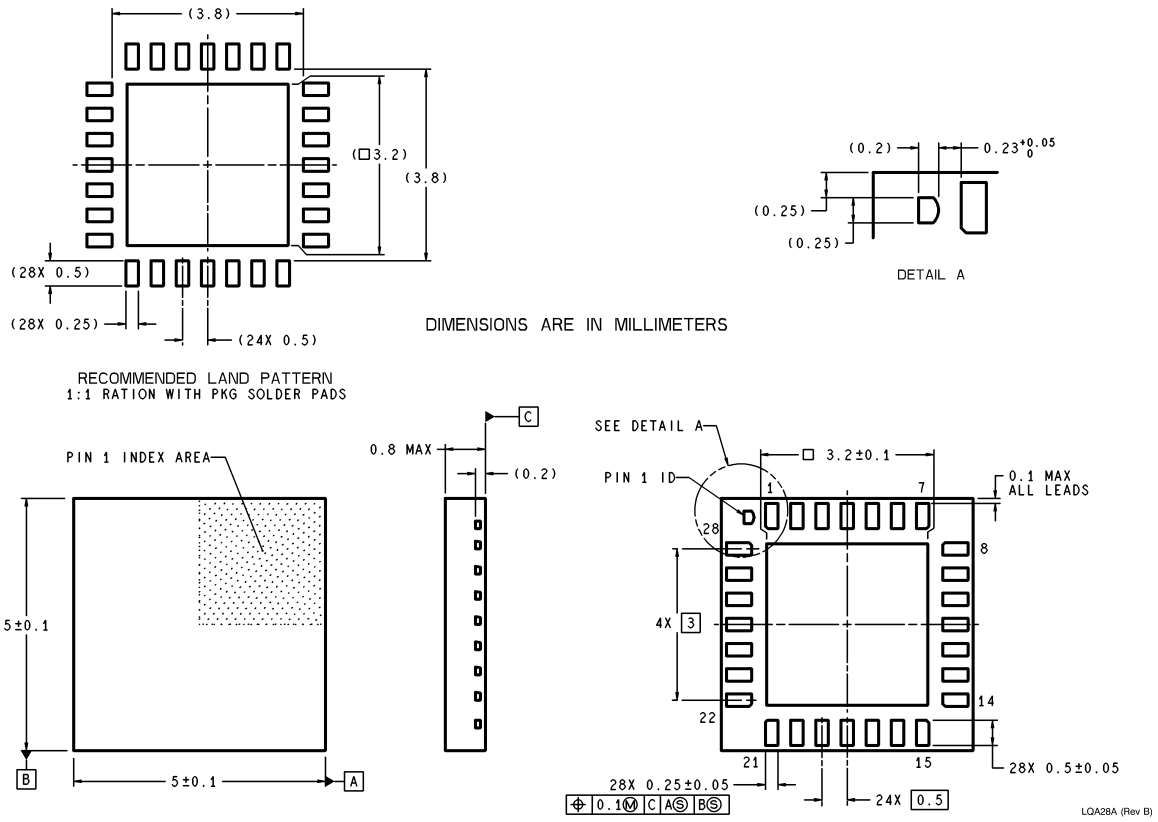
FIGURE 7. Recommended TS SE PCB Layout: Bottom Layer

Revision History

Rev	Date	Description
1.0	11/14/05	Edited 83, C4, and C5 (replaced with 01, 02, and 03), then re-WEB per Nisha.
1.1	2/02/06	Some text edits, then re-WEBd.

Physical Dimensions inches (millimeters) unless otherwise noted



LQ Package
Order Number LM4961LQ
NS Package Number LQA28A

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