YAMAHA

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YMU765

APPLICATION MANUAL

MA-5 Mobile Audio 5

YAMAHA CORPORATION

YMU765 Application Manual
CATALOG No.:LSI-6MU765A2
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Content

Introduction

This document describes the functions, usages, and electrical characteristics of YMU765.
The compositions of this book are as follows.

About the descriptions of this document

Descriptions of marks used in the document

: Indicates the restrictions or notes for use.

: Indicates the supplementary information or tips.

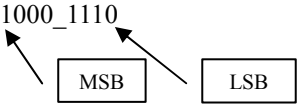
Numerical description used in this specification

Basic notation is "Number of bits (decimal) + radix + constant".
Binary one bit is treated exceptionally.
[Example] When describing decimal numeral of "15",

- Binary: 8'b 0000_1111
- Decimal: 15 (described as it is)
- Hexadecimal: 8'h0f

Weighting of signals

- For signals consisting of multiple bits, the leftmost bit is MSB, and the rightmost bit is LSB.
  [Example] 8'b 1000_1110



- For registers consisting of multiple bits, they are converted to decimal numerals in accordance with the following example.
  $(2^n \times Dn) + \cdots (2^1 \times D1) + (2^0 \times D0)$
  [Example] Correspondence between the setting values of the following register and numeric values

D7	D6	D5	D4	D3	D2	D1	D0
IRQ	VALID_R	B_ADR					

When "6'b 01_0101" is set in D5 to D0, the set value of "B_ADR" is described as "21" ($21 = 2^4 + 2^2 + 2^0$)

Description of register numbers

- Decimal notation is used. Numerals are prefixed with "#". ([Example] #0, #1 ...)
- The following prefixes are attached before the registers to distinguish three registers.
  - Interface register : A_Address ([Example] A_Address #0)
  - Intermediate register : B_Address ([Example] B_Address #0)
  - Control register : C_Address ([Example] C_Address #0)

Description of memory address

- Address of ROM / SRAM is prefixed with "M_Address".
- Hexadecimal notation is used for numerals of address numbers.
- Numbers are prefixed with "#".

The notation system of Levels

- Pins are "L" or "H".
- Internal signals are "0" and "1".

L1 Outline

This chapter describes the organizations of YMU765.
The explanations are constituted as follows.

L1.1 WHAT IS YMU765?

L1.2 BLOCK DIAGRAM

L1.3 HYBRID SYNTHESIZER

L1.4 FM SYNTHESIZER

L1.5 WT (WAVE TABLE) SYNTHESIZER

L1.6 HV (HUMANOID VOICE) SYNTHESIZER

(*) HV synthesizer function only responds to Japanese and Korean language at present.

L1.7 AL (ANALOG LITE) SYNTHESIZER

L1.1 What is YMU765?

YMU765 is a synthesizer LSI for mobile phones that realize advanced game sounds of Java application program etc. This LSI has a built-in speaker amplifier, and thus, is an ideal device for outputting sounds that are used by mobile phones in addition to game sounds and ringing melodies that are replayed by a synthesizer.

The synthesizer section adopts the "Stereophonic Hybrid Synthesizer System" which is given advantages of both FM synthesizers and Wave Table synthesizers to allow simultaneous generation of up to 32 FM voices and 32 Wave Table voices. Furthermore, the stream playback function, the voice synthesis function by HV (Humanoid Voice) synthesizer (*), and the time-variant low pass filter function by AL (Analog Lite) synthesizer have also on board.

Since FM synthesizer is able to present countless voices by specifying parameters with only several tens of bytes, memory capacity and communication band can be saved, and thus, the device exhibits the features in operating environment of mobile phones such as allowing distribution of arbitrary melodies with voices.
On the other hand, Wave Table synthesizer can pronounce the voice built in ROM and arbitrary ADPCM/PCM voices from sequencer by the download of the melody with voices etc..

YMU765 has a built-in hardware sequencer that helps to realize a complex play without heavily loading the host CPU. In addition, it is possible to create more highly efficient applications by the voice synthesis function (*) and the function of time-variant low pass filter. Moreover, the device also has a built-in circuit for controlling vibrators and LEDs synchronizing with play of music.

(*) HV synthesizer function only responds to Japanese and Korean language at present.

- Built-in the hybrid synthesizer, and possible to generate 64 tones simultaneously as maximum.
- FM synthesizer : The maximum of the simultaneously sound generation is 16 tones by 4OP voices, 32 tones by 2OP voice.
- WT (Wave Table) Synthesizer : The maximum of the simultaneously sound generation is 32 tones
- Stream playback section : The maximum simultaneously sound generation is 2 tones.
- HV (Humanoid Voice Synthesizer) : The maximum simultaneously sound generation is 1 tone.
- AL (Analog Lite) Synthesizer : The maximum simultaneously sound generation is 1 tone.
- Voice synthesis voice function by HV synthesizer is on board.
  (*) HV synthesizer function only responds to Japanese and Korean language at present.
- The time fluctuation low pass filter function by AL synthesizer is on board.
- Compiles with the software processing load abatement.
- Compiles with the function and pin location of MA-3.
- Compiles with the TCXO (Temperature Compensated Crystal Oscillator).
- Has power down mode.
- Power supply for core 2.65V ~ 3.30V
- Power supply for I/O 1.65V ~ VDD
- Power supply for speaker amplifier VDD ~ 4.50V
- 32-pin QFN plastic package

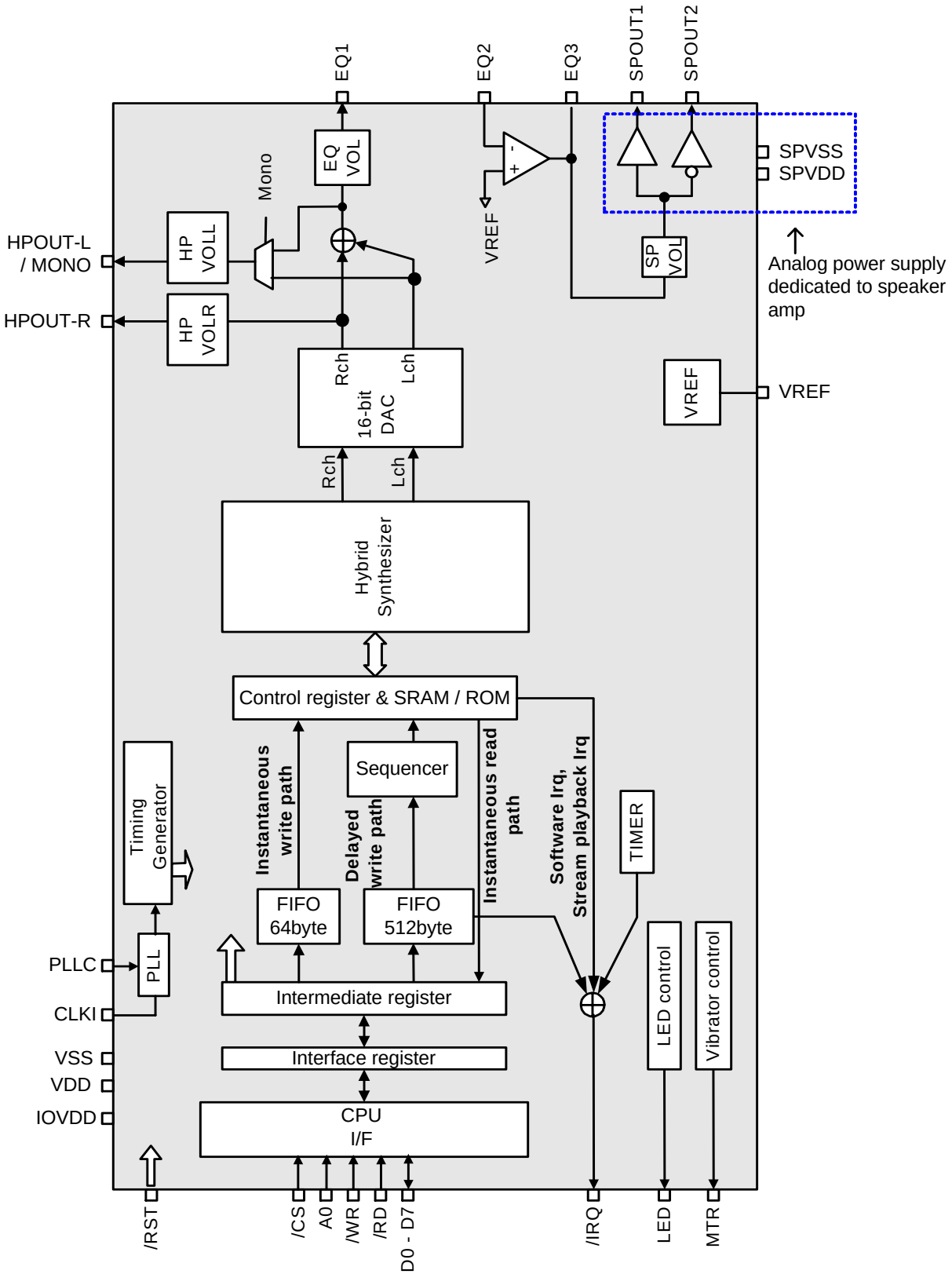
The number of simultaneous sound generation has restrictions.

There is a place which is sharing the hardware resource between each synthesizer sources.
For example, since the stream playback section shares the resource with WT synthesizer, the number of simultaneous sound generations is reduced by generating the stream playback.
For more details, refer to the "L3.4 Hybrid Synthesizer (Synthesizer Mode Selection)" in this document.

For the details about the "HV synthesizer" and "AL synthesizer", please refer to "L1.6" and "L1.7".

L1.2 Block Diagram

The functions of the internal devices and the stream of the each signal are described in this section



CPU Interface

CPU interface is an 8-bit parallel type.
It assumes that a total of 13 pins of 4 control signals (/WR, /RD, /CS, A0 pin), 8 data bus (D0 to D7), and 1 Interrupt pin (/IRQ) are connected to the external CPU.
This block controls the writing and reading of data by the input polarity of control signal.

Interface Register

This register is able to access directly from the external CPU. There are 2 bytes spaces.
The latter Intermediate register can be accessed through the Interface register.

Intermediate Register

This register is accessed through the Interface register.
The “Control register” and ROM/SRAM, which describes below, can be accessed through this register.
This register is called the “Intermediate register” since this exists in the middle of the Interface register and the Control register.
In the Intermediate register, there are some registers to control various functions.

Control Register, ROM/SRAM

The Control register and ROM/SRAM are accessed from “Instantaneous write register”, “Delayed write register”, and “Instantaneous read register” in the Intermediate register.
In the Control register, there is a register to control the following synthesizer mainly.
The voice parameter for FM (GM 128 voices + DRUM 40 voices) and Wave data for WT are stored in ROM.
SRAM is used at the download of arbitrary FM voice parameter and Wave data for WT.
Moreover, it is used as storing buffer at the stream playback of PCM/ADPCM.

FIFO

This is an abbreviation of “First In First Out” means the memory which data is read in order of written.
There are 2 paths to write into FIFO in the Intermediate register.
The “Instantaneous write path” is for accessing the Control register and ROM/SRAM immediately, also “Delayed write path” is for accessing the Control register after managing time through the sequencer.
FIFO size of Instantaneous path is 64-byte, and its size of Delayed path is 512-byte.

Sequencer

This is for interpreting the contents of data which was written into the Delayed write path.
Generally, “Music data” is written into the Delayed write path. It interprets the contents of music data and controls the synthesizer after sequencer, and then plays the music.

Hybrid Synthesizer

This device contains a built-in Polyphonic synthesizer that adopts a stereophonic hybrid system that generates up to 64 tones.
FM synthesizer, WT (Wave Table) synthesizer, Stream playback, HV (Humanoid Voice) synthesizer (*), and AL (Analog Lite) synthesizer are available.

(*) HV synthesizer function only responds to Japanese and Korean language at present.

LED, Vibrator Control

It is possible to synchronize an LED and vibrator with a play, and to control. A synchronous control to a play is also possible.

Clock Generating Block

This device supports a clock input ranging from 1.5 MHz to 20 MHz. (Stop = 0 Hz is possible at power down.)
It is a block to generate a clock which is needed inside of LSI in the PLL.

DAC (Digital-to-Audio Converter) Section

It converts digital signals from a synthesizer and a digital audio section into analog signals. The length of a data is 16bits.

Headphone Amplifier Section

This is an amplifier of Stereophonic output for Headphone. The monaural output is also possible.

EQ Amplifier Section

The change of Filter characteristic and gain is possible by adjusting the resistors and external parts.

Speaker Amplifier Section

A speaker amplifier, which has maximum output power of 580 mW at SPVDD=3.6V, is integrated this device. There is a volume to adjust output level in the first part of amplifier.

L1.3 Hybrid Synthesizer

A hybrid synthesizer is equipped in it, and the maximum simultaneous sound generation of 64 tones is possible. The hybrid synthesizer means the synthesizer which has several kinds of playback functions in one synthesizer core.

It has the following five synthesizer functions.

- FM synthesizer
- WT synthesizer
- Stream playback
- HV synthesizer

  (*)HV synthesizer function only responds to Japanese and Korean language at present.
- AL synthesizer

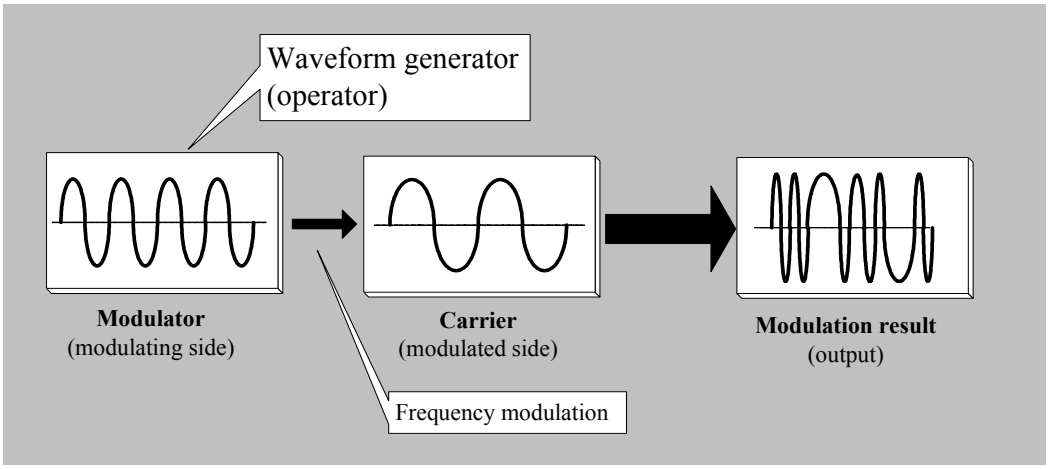
L1.4 FM Synthesizer

What is FM?

"FM" is an abbreviation of "Frequency Modulation", and it is a synthesizer which generates tones, such as a piano and a guitar, using the structure of frequency modulation. Although the word of "FM" will generally remind many people of radio, both of them are using frequency modulation, so that a basic principle is the same. (Radio uses the frequency modulation for a radio wave, and the FM synthesizer uses it for a sound).
Fist of all, Dr. Chowning of the Stanford University discovered the principle of a FM synthesizer, and YAMAHA, a musical instrument maker, put it to practical use.
"FM synthesizer" is widely utilized from the synthesizer card for personal computers to professional musical instruments, and then it has been used as a synthesizer for mobile phones since the beginning of the 2000.

The Fundamental Principle of FM Synthesizer

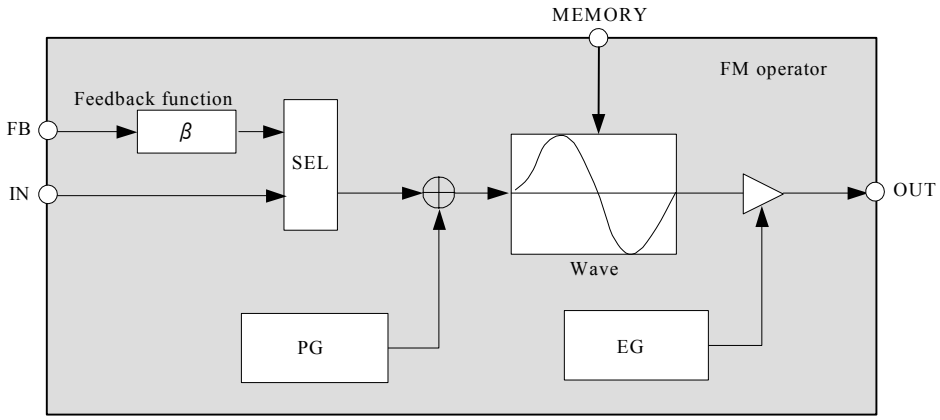
The fundamental principle of FM is shown as follows.
Waveform generator is called an "operator".
A basic configuration of FM generates a tone by using two operators. The operator that modulates a signal is called "a modulator", the operator that is modulated is called "a carrier".
A complicated output waveform is generated by a way of applying modulation to a career waveform by a modulator waveform.



In addition, an operation called "Feedback FM" can be selected; the way is that operators are connected, so that output waveform is fed back again to use the signal as an input signal.

Fundamental Composition of each Operator

Secondly, the fundamental configuration of each operator is described in this section.
There are four different functions, PG, EG, Wave, and Feedback in the internal of operator.



PG

PG is an abbreviation of the "Phase Generator", and it is a block to controls the frequency of waveform signal outputted from the operator.

EG

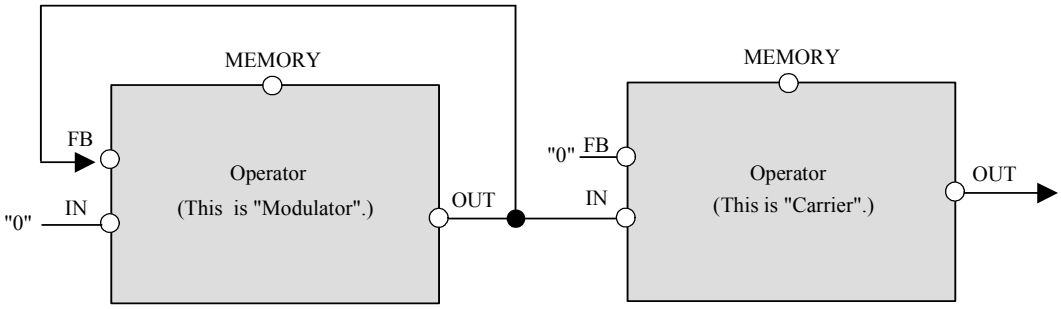
EG is an abbreviation of the "Envelope Generator", and it is a block to controls the time change of volume outputted from the operator on time scale.
By applying EG to the modulator side, the "Time Change of Voice" is obtained as an effect, and it is obtained on the carrier side.

Wave

Wave is a block to read a waveform data registered in RAM/SRAM and to generate a waveform, in accordance with a result of an addition between PG and Feedback path.

Feedback

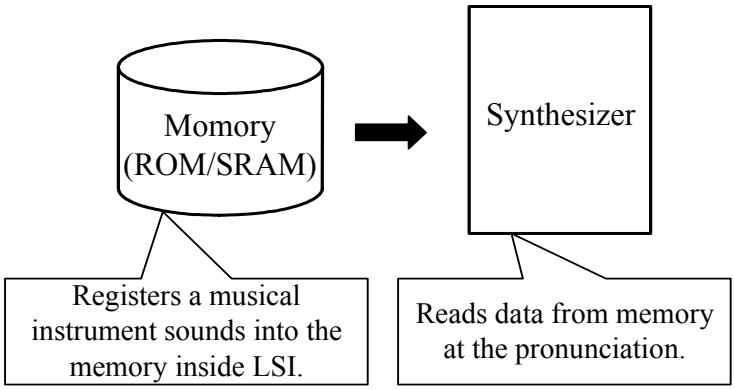
When a feedback setup is carried out, OUT and FB are connected, and FB input is chosen in the SEL. β is a block to adjust the amount of feedbacks.
For example, when two operators are connected by using feedback is as follows.



L1.5 WT (Wave Table) Synthesizer

Fundamental Principle of WT (Wave Table) Synthesizer

WT synthesizer is a system that stores a recorded voice data of actual musical instruments, such as pianos and drums into the memory beforehand, and reads the data from the memory to output it in case of generation of voices. Therefore, WT synthesizer is able to generate realistic voices that resemble an actual musical instrument better than FM synthesizer.
However, WT synthesizer has a shortcoming of which a memory to store various musical instrument data is needed, and consequently it costs higher than FM synthesizer.



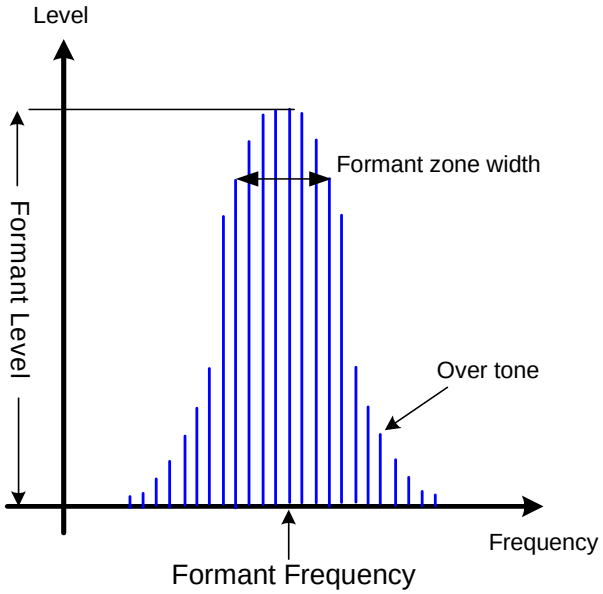
In a FM synthesizer, sounds are produced by synthesizing waves made artificially by using formula, in a word, FM synthesizer produces voices.
As for WT synthesizer, voices are not things to make but it is a thing to reproduce the voice data which are registered beforehand.

L1.6 HV (Humanoid Voice) Synthesizer

HV is an abbreviation of the “Humanoid Voice”, and it is a voice synthesis function simulating a human voice.
HV generates formant frequencies from a sign-wave etc., and it executes a voice synthesis operations.
(*) HV synthesizer function only responds to Japanese and Korean language at present.

Structure of how People Pronounce Languages?

The vibration of vocal cords becomes the origin of human voices. In addition, even if the language to pronounce is different, a number of vibrations hardly changes. Then, why various languages can be spoken, the reason is that the resonance produced according to how to open a mouth and how to form a throat, etc., fricative and explosive which accompanies it, are added to vibration of vocal cords.
In our voice, there are many portions in which the spectrum is concentrating at the specific frequency band and making mountains.
The mountain of the spectrum is called “Formant” and has become one of the important elements that allow human voice to be heard as language.

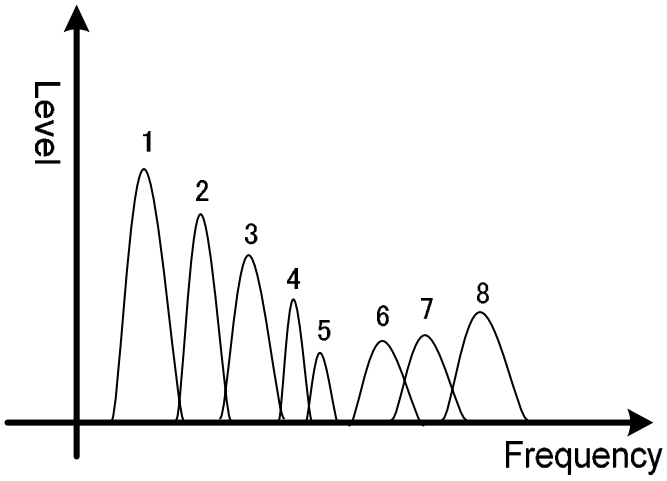


Center value or the maximum amplitude frequency of a “Formant” is called “Formant frequency”.

Voiced Sound and an Un-voiced Sound

The number of the formant contained in voice, frequency and amplitude of each formant, bandwidth, and etc. are elements to determine characteristics for the voice, and it differs considerably depending upon the sex, physique, and age of the person who utters voice.
In fact, in the human voice the combination of a characteristic formant is determined depending upon kinds of language to pronounce. Therefore, various languages can be recognized even if vocal quality is different.

If the kinds of formant is divided roughly, there is a voiced formant that has pitch information to synthesize voiced sound (*), and an unvoiced formant that has no pitch information to synthesize unvoiced sound (*).
HV synthesizer section realizes a structure which makes the formant frequency of eight pieces and pronounces language.



*Voiced Sound

In case it pronounces, the voice to which vocal cords vibrate is called “Voiced Sound”. When you touch your throat with your finger and pronounce some word, a sound that vibrates the throat is a voiced sound.

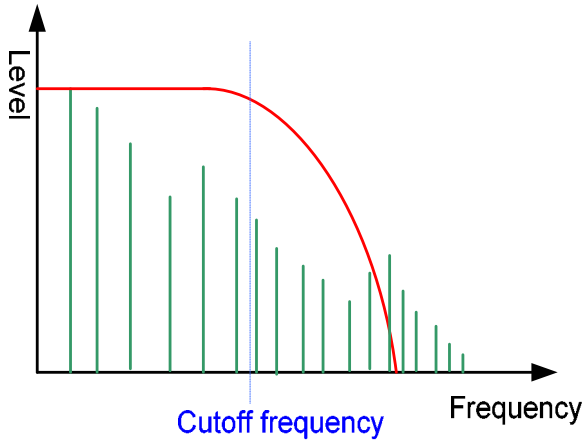
*Un-voiced Sound

In case it pronounces, the voice to which vocal cords do not vibrate is called “Un-voiced Sound”. When you touch your throat with your finger and pronounce some word, a sound that does not vibrate the throat is an unvoiced sound.

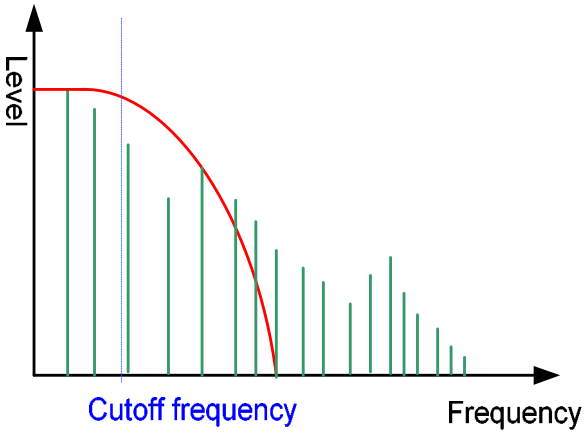
L1.7 AL (Analog Lite) Synthesizer

AL synthesizer is an abbreviation of “Analog Lite”.
This section describes the time-variant low pass filter and resonance of AL synthesizer.

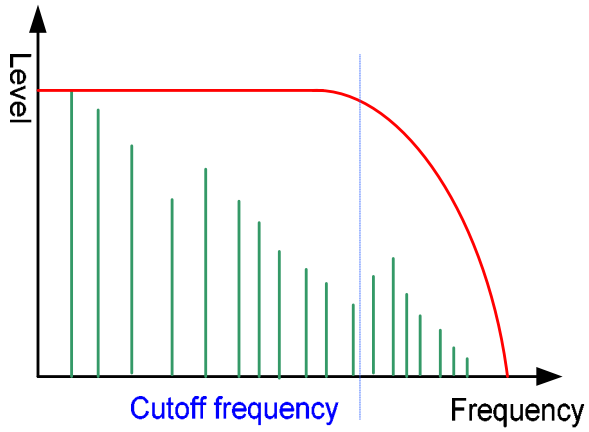
What is the Time-Fluctuation Low Pass Filter?



The role of the low pass filter is removing the specific frequency contained in the voices to change the voices.
The frequency to be removed varies according to the cutoff frequency.
For the low pass filter, harmonic of frequency that is higher than the cutoff frequency is removed.
Therefore, for instance, lowering the cutoff frequency removes many harmonic including relatively low frequency, and the voices become darker consequently.



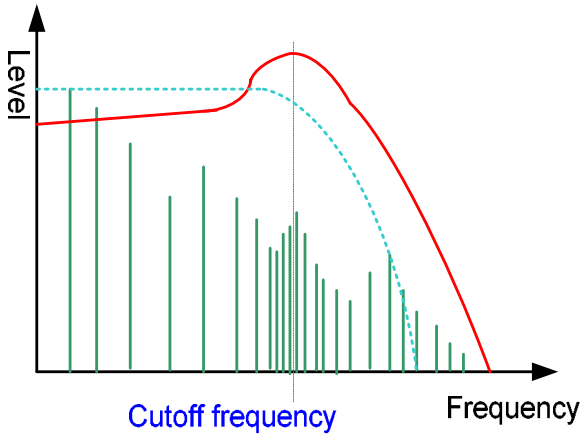
If the numeric of a cutoff frequency is raised, the harmonic to be removed will be decreased. As a result of it, the voices become lighter. However, the voices are made lighter relatively, it merely means the original voices are restored.
(This is pretty important matter, when you understand a filter.)



The “Time-variant low pass filter” is a low pass which can change a cutoff frequency with time (real time).

Resonance Function

The low pass filter is also given a function called “Resonance”.
The resonance has a function that changes voices by accentuating the sound near the cutoff frequency, and it allows to accentuate specific harmonic and to add new harmonic to original ones.



The effects of the resonance cannot be described flatly because it varies depending on the setting of the cutoff frequency. Generally, applying the resonance makes voices peculiar and sharp.
When the setup of the cutoff frequency are changed during resonance, the harmonic frequency to be accentuated moves; so that the peculiar effect such as “mew” which are often used for analog base can be reproduced.
Applying the resonance raises the voice level near the cutoff frequency, in contrast, the frequency lower than cutoff frequency reduces the level. Therefore, note that excessive application of the resonance eliminates low frequency voices.

L2 Direction of each Operation

In this chapter, the usage of each register is described.

L2.1 Register Structure

L2.2 The Access Method of the Interface Register

L2.3 Wait Time at the Time of Access

L2.4 How to Access to the Intermediate Register?

L2.5 How to Access into the Control Registers and SRAM?

L2.5.1 Instantaneous Write Register
L2.5.2 Delayed Write Register
L2.5.3 Instantaneous Read Register
L2.5.4 Read Buffer Register

L2.6 Initialization Procedure

L2.6.1 Power Management Setup

L2.7 Power-down Procedure

L2.7.1 Sequence for Transition to Power-down (Synthesizer Section)
L2.7.2 Sequence for Power-down Cancellation
L2.7.3 A Setup According to Configuration to Use Form
L2.7.4 Division of the Power Management Control

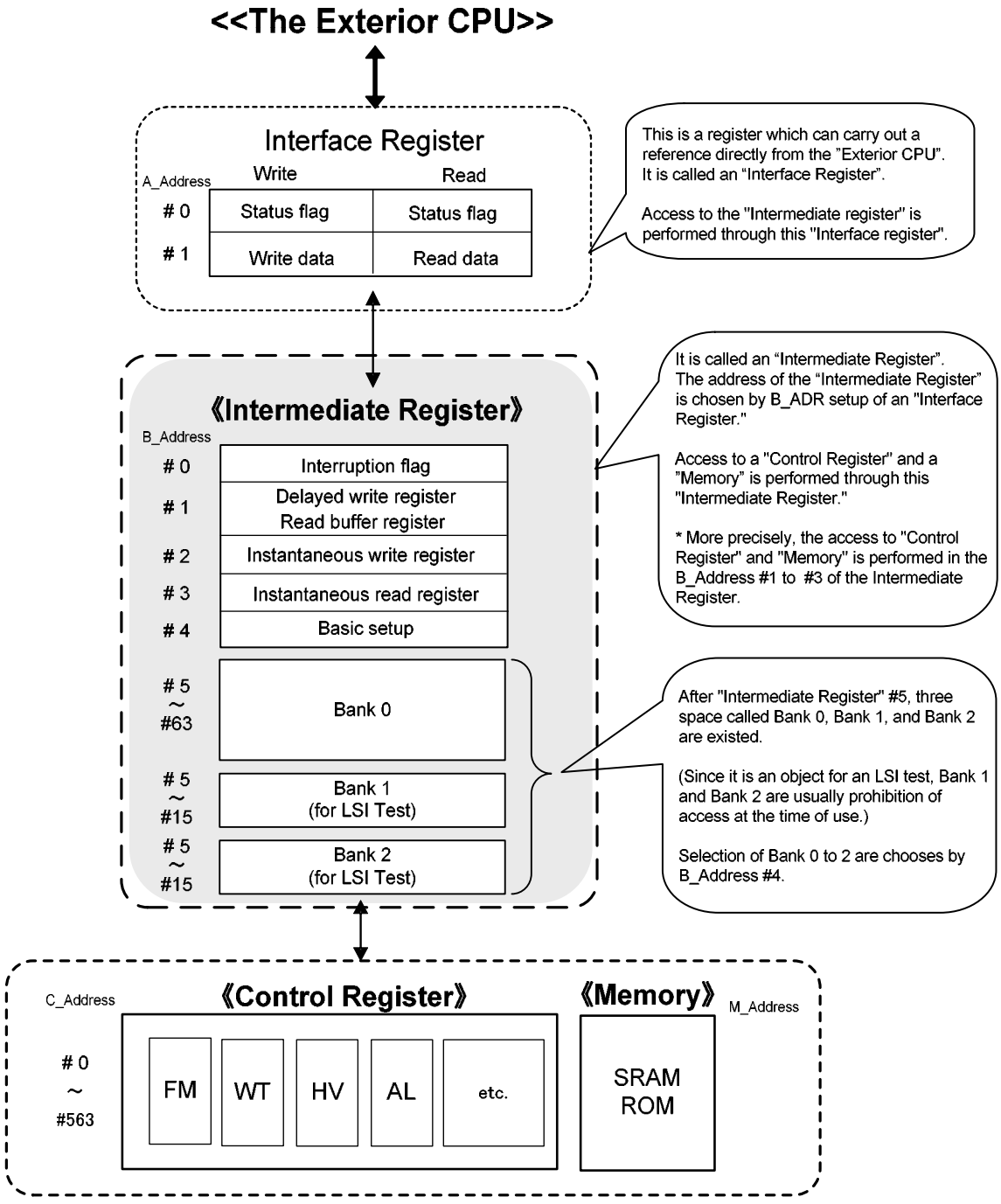
L2.8 Setup Procedure to Sound Generation

L2.1 Register Structure

There are three kinds of registers in YMU765.

- “Interface Register”
- “Intermediate Register”
- “Control Register”

The “Interface Register” is a register directly controlled from the external CPU.
The three steps of registers are composed to access “Intermediate Register” through “Interface Register” and to access “Control Register” and “Memory” through “Intermediate Register”.
***Access from “Interface register” → “Intermediate register” → “Control register” & “Memory”.**



L2.2 The Access Method of the Interface Register

The registers which are directly accessible from the external CPU is called the “Interface Register”.
There are four registers in the “Interface Register”.

- Status flag register (WRITE)
- Status flag register (READ)
- Write data register
- Read data register

In order to access these four registers (/CS, A0, /WR, /RD), set the input pins of CPU interface to the level as shown in the following table.
During the period /RST=“L” (during a hardware reset), it is always “No response”

Pins				Operation mode
/CS	A0	/WR	/RD	
H	*	*	*	No response
L	L	L	H	Status flag register (WRITE)
L	H	L	H	Write data register
L	L	H	L	Status flag register (READ)
L	H	H	L	Read data register

Please don’t input logic “L” into /CS, /WR, and /RD at the same time.

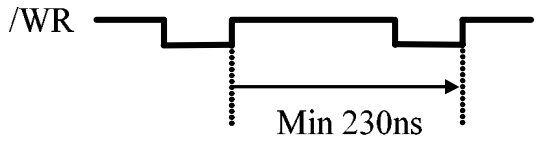
Although D0 to D7 pins will be in output state, write-operation also becomes valid simultaneously, so that the output data may be written into the register.

L2.3 Wait Time at the Time of Access

In case the “Interface Register” is accessed, the following four wait-times become necessary.
Please be sure to keep the regulation of the wait time and use.
For more details about the timing of WRITE / READ, refer to the “L4.4.5.2 CPU interface timing“.

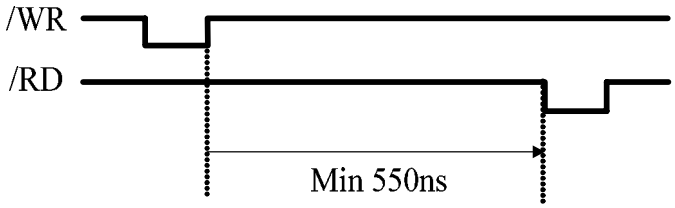
Wait Time at WRITE to WRITE

The wait time from rising edge of /WR to rising edge of the next /WR is necessary at least 230 ns (*).
(*) To be accurate, it is 17000 / Fp (ns). Fp is oscillation frequency of PLL.
For instance, when the oscillation frequency of PLL is 73.7MHz, substitute “73.7” for Fp of the above formula.
For more details about Fp, refer to the “L3.13.3 Error (Synthesizer Section)“.



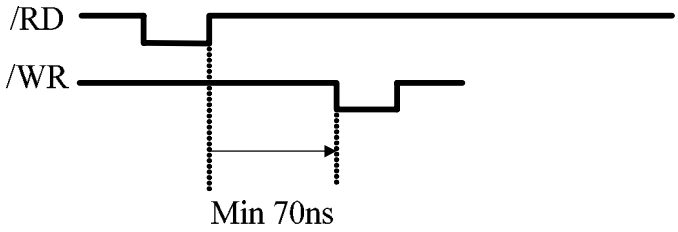
Wait Time at WRITE to READ

The waiting time from rising edge of /WR to falling edge of /RD is necessary at least 550 ns (*).
(*) To be accurate, it is 41000 / Fp (ns). Fp is oscillation frequency of PLL.
For instance, when the oscillation frequency of PLL is 73.7MHz, substitute “73.7” for Fp of the above formula.
For more derails about Fp, refer to the “L3.13.3 Error (Synthesizer Section)“.



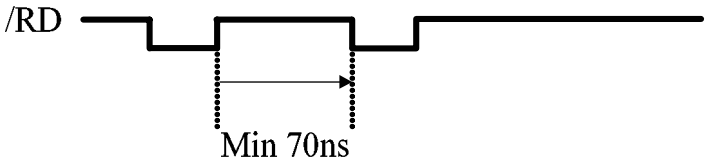
Wait time at READ to WRITE

The waiting time from rising edge of /RD to the falling edge of /WR is necessary at least 70 ns.



Wait Time at READ to READ

The waiting time from rising edge of /RD to the falling edge of /RD is necessary at least 70 ns.



L2.4 How to Access to the Intermediate Register?

How to WRITE into the Intermediate Register?

The status flag register (WRITE) and the Bank bit register

Status flag register (WRITE)

A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	W	IRQ	VALID_R	B_ADR					

<< Fundamental setting >>

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#4	W/R	SFTRST	R_FIFO#1	R_FIFO#0	R_SEQ#1	R_SEQ#0	“0”	BANK	

The procedures to write into a register in the Bank 0

1. Write an address number of the Intermediate Register into the B_ADR bit of the “Status flag register (WRITE)”.
2. Set up a data to write into the “Write data register”.

The procedures to write into a register (for LSI test) other than bank 0

In addition to the above-mentioned procedures, selection of a bank number is needed.

1. Write 6’h04 into B_ADR bit of the “Status flag register (WRITE)”.
2. Write a bank number into BANK bit of the “Intermediate register #4”.
3. Write a Bank number of the Intermediate Register to be accessed into B_ADR bit of the “Status flag register (WRITE)”.
4. Set up a data to write into the “Write data register”.

Bank 1 to Bank 3 are prohibited to access.

Usually, set up 2'b00 into the BANK bit and use.

There is no Bank 3, and it is from Bank 0 to Bank 2.

Banks 1 and Bank 2 are for LSI test, so access to the banks is prohibited.

How to READ from the Intermediate Registers?

The read data register

Read data register

A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#1	R	Read data register							

The procedures to read a data from a register in the Bank 0

1. Write an address number of the intermediate Register into the B_ADR bit of a status flag register (WRITE).
2. Read the “Read data register”.
3. Data from the register are read at D0 to D7 pins.

The procedures to read a data from a register (for LSI test) other than bank 0

In addition to the above-mentioned procedure, selection of a bank number is needed.

1. Write “6’h04” into B_ADR bit of the “Status flag register (WRITE)”.
2. Write a bank number into BANK bit of the “Intermediate Register #4”.
3. Write an address number of the Intermediate Register to be read into B_ADR bit of the “Status flag register (WRITE)”.
4. Read the “Readout data register”.
5. Data from the register are read at D0 to D7 pins.

Intermediate registers #2 and #3 cannot be read.
Bank 1 to Bank 3 are prohibited to access.

L2.5 How to Access into the Control Registers and SRAM?

How to WRITE into the Control Registers and SRAM?

There are the following two methods to write into the Control registers and SRAM.

- Way to write through the “Delayed write register” in the Intermediate register #1.

Delayed write register is described in the “L2.5.2 Delayed Write Register“.

- Way to write through the “Instantaneous write register” in the Intermediate register #2

Instantaneous write register is described in the “L2.5.1 Instantaneous Write Register”.

The Differences between “Delayed Write Register” and “Instantaneous Write Register”

Data written through the Delayed write register are written into the Control Register or SRAM after they are time-managed at the sequencer section. Data written from the Instantaneous write register are written into the Control Register or SRAM immediately. Select appropriate registers according to the application. (Normally, “Music Data” are written into the Delayed write register.)

How to Read from the Control Registers and SRAM?

In order to read a data from the Control Register, the “Instant read register #3” in the Intermediate Register is used. The procedure of “READ” is as follows.

- Set up a register address to be read at the “Instantaneous read register”.
- Read data from the “Read buffer register (#1)” in the Intermediate Register.

For more details about the “Instantaneous read register”, refer to the “L2.5.3 Instantaneous Read Register“.

L2.5.1 Instantaneous Write Register

The Instantaneous write register #2 is in the Intermediate register. It is “WRITE” only registers.

A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2	W	Instantaneous write register							

By setting up the “Packet for the Instantaneous write” to the Instantaneous write register, the data can be written into the Control Register or SRAM.

For the details about the “Packet for the Instantaneous write”, please refer to the “L2.5.1.2 The Packet for the Instantaneous Write“.

L2.5.1.1 The Status Flag of FIFO for Instantaneous Write

The data written into the “Instantaneous write register” is stored in the 64-byte FIFO at first.
When the 64-byte FIFO is full, additional data written into the FIFO is thrown away.
Therefore, be sure to confirm the status of FIFO when you want to write data into the “Instantaneous write register”.

The status of the FIFO for “Instantaneous write” is located in D2 bit (FULL_W) and D0 bit (EMP_W) of the “Interface register status flag (Read)”.

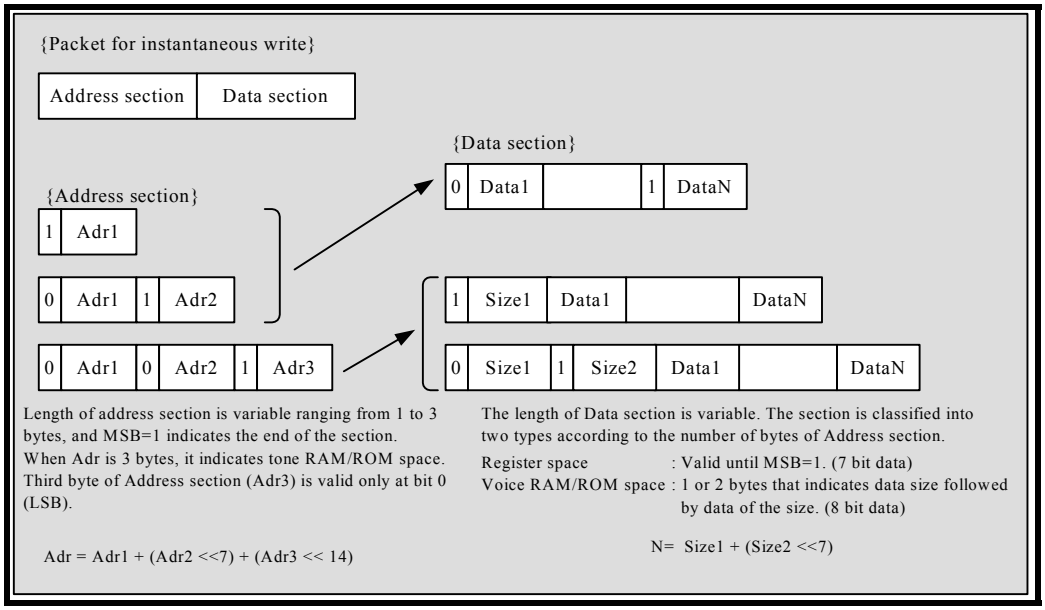
Default 8’h03

A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	R	BUSY	VALID_R	“0”	“0”	FULL_DW	FULL_W	EMP_DW	EMP_W

- EMP_W: Logic “1” indicates that the FIFO (64 byte) for “Instantaneous write “is empty.
- FULL_W: Logic “1” indicates that the FIFO for “Instantaneous write” is full.

L2.5.1.2 The Packet for the Instantaneous Write

The [Address of Control Register + WRITE data] is called the “Packet for the Instantaneous write”.
The “Packet for the Instantaneous write” is written in the “Instantaneous write register”.
The contents of the “Packet of the Instantaneous write” are as follows.



When an Address section is 3 bytes length, it indicates a ROM/SRAM spaces, and they are allocated as follows.

ROM space.....15’h0000 to 15’h3FFF
SRAM space.....15’h4000 to 15’h5FFF

As for the size of Data section, the Size = 0 is prohibited.

Example of a setup: When you want to write 8’h01 into C_Address#0 of the “Control Register”.

1. Write 6’h02 into B_ADR bit of the “Status flag register (WRITE)”.
   → Instantaneous write register is selected.
2. Write 8’h80 and 8’h81 successively into the “Write data register”.
   → Now, data are written into the Control register
   .

L2.5.1.3 Burst Write Function

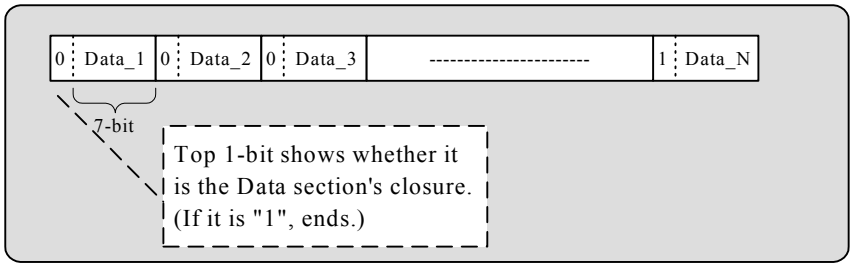
When it is required to write a data into registers successively such as C_Address #0, #1, #2....., the “Burst write function” is selectable in order to reduce the number of data to access.
In the “Packet for Instantaneous write”, the “Burst write” is selected by arranging the multiple Data sections after the Address sections.

- **Write data explanation at “Burst write”**

Arrange the multiple data sections after the Address sections.

– Data_1 into Address
– Data_2 into Address+1
– Data_3 into Address+2
– Data_N into Address+N-1 are written.

The hardware takes it as the write operations into consecutive address, until MSB of DATA section becomes “1”.



[Example] When you want to write 1, 2, 3, 4, 5, 6 and 7 into the Control Register C_Address #0 to #6.

1. Write “6’h02” into B_ADR bit of the “Status flag register (WRITE)”.
2. Write “8’h80, 8’h01, 8’h02, 8’h03, 8’h04, 8’h05, 8’h06, and 8’h87” into the “Write data register” continuously.

– The first 8’h80 is the Address section. MSB “1” indicates that is a last Address section.
– The last 8’h87 indicates the is an end of Data section.
– As far as not making MSB to “1”, it takes as a successive write operation into a register.

[Example] Voice generation setup method with “Burst write”

When the 9 bytes of DATA1 to DATA9 are set up into M_Address# 15’h4000 of ROM/SRAM space

1. Write “6’h02” into B_ADR bit of the “Status flag register (WRITE)”.
   → Instantaneous write register is selected.
2. Write 8’h00, 8’h00, 8’h81, 8’h89, DATA1, DATA2, DATA3, DATA4, DATA5, DATA6, DATA7, DATA8, DATA9 into the “Write data register”.

The meaning of the packet is as follows.

- Access into h4000 → 8’h00 8’h00 8’h81
- Size Setup : 9 bytes → 8’h89
- Data Setup: DATA1 to DATA9 (9 bytes)

L2.5.2 Delayed Write Register

It is in the Intermediate Register #1 and a WRITE only registers.

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
# 1	W	Delayed write register							

By setting the “Packet for delayed write” to the “Delayed write register”, the data can be written into the “Control Register” or SRAM.
For the explanations about the “Packet for the delayed write”, refer to the “L2.5.2.2 The Packet for the “Delayed Write””.

L2.5.2.1 The Status Flag of FIFO for the Delayed Write

The data written through the “Delayed write register” is stored in the 512 bytes FIFO at first, and then it is time-managed in a sequencer section and written into the “Control Register” and SRAM.
When the 512-byte FIFO is full, an additional data written into the FIFO is thrown away. Therefore, be sure to confirm the status of FIFO when you want to write a data into the Delayed write register.
The status of the FIFO for the “Delayed write” is located in D3 bit (FULL_DW) and D1 bit (EMP_DW) of the status flag of the “Interface Register”.

Default 8’h03

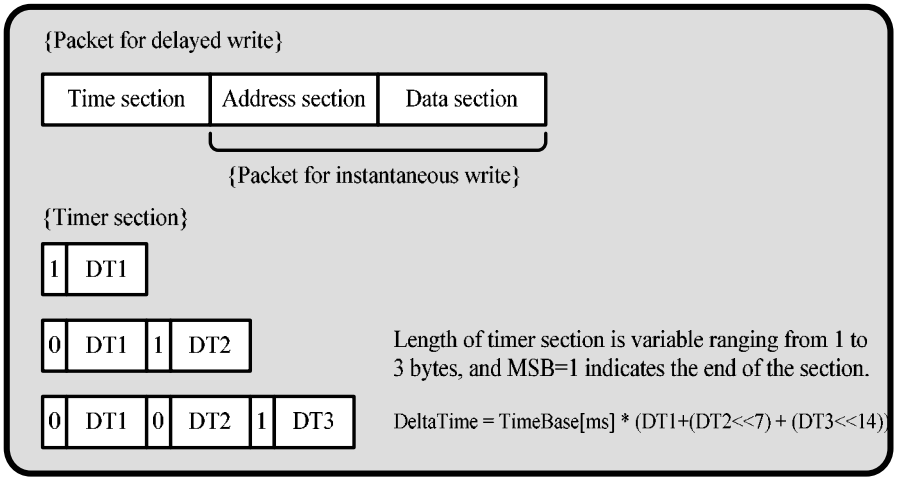
A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	R	BUSY	VALID_R	“0”	“0”	FULL_DW	FULL_W	EMP_DW	EMP_W

- EMP_DW： “1” indicates that the “Delay write for FIFO (512 bytes) “ is empty.
- FULL_DW： “1” indicates that the “Delay write for FIFO” is full.

For the details about the data write method of 512-byte FIFO by the use of an interrupt, refer to the “L3.3 Interrupt”.

L2.5.2.2 The Packet for the “Delayed Write”

The packet for the “Delayed write” is a packet of which time information (Timer section) is added to the “Instantaneous write packet (“L2.5.1 Instantaneous Write Register” explanation) as a leading data.
It supports the “Burst write” as well as the “Instantaneous write register”.
The contents of the “Packet of the delay write” are as follows.



When you want to write 8’h01 into C_Address #0 of the “Control register” with Time section = 5.

1. Write “6’h01” is written into B_ADR bit of the “Status flag register (WRITE)”.
2. Write 8’h85, 8’h80, and 8’h81 consecutively into the “Write data register”.

→ The write process is completed here.

L2.5.3 Instantaneous Read Register

This register is used to read a register data from the “Control Register” and “SRAM”.
The “Instantaneous read register #3” is in the “Intermediate register”, and it is a WRITE only register.

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#3	W	Instantaneous readout register							

L2.5.3.1 VALID_R, BUSY

The status flag register（WRITE） Default 8’h00

A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	W	IRQ	VALID_R	B_ADR					

VALID_R: A flag is cleared by writing “1”.

The status flag register（READ） Default 8’h03

A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	R	BUSY	VALID_R	“0”	“0”	FULL_DW	FULL_W	EMP_DW	EMP_W

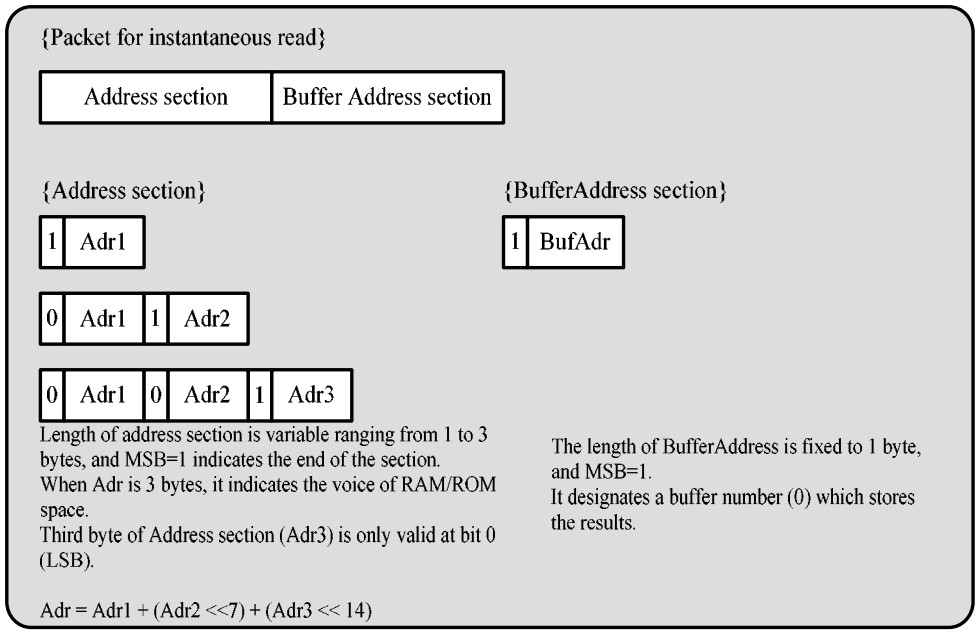
VALID_R: “1” indicates the “Read buffer register” has a valid data.
“0” indicates the “Read buffer register” has invalid data.

BUSY: It is the flag to indicate a write access.
“1” indicates BUSY state (write access is impossible).
Conditions of which BUSY flag is set to “1” are the following three cases.

- During the hardware reset
- During the software reset
- During 23μs after software reset is released.

L2.5.3.2 Packet for the Instantaneous Read

The packet of "Register address + Return buffer address (=0)" is set to the "Instantaneous read register". After the setup, the read data is input to the specified position of a returned buffer.
When the data is stored into the "Read buffer register (refer to the "L2.5.4 Read Buffer Register"), The VALID_R bit of the status flag is set up. The data read from the "Instantaneous readout register" is preserved until the next read data is set up.



[Access method]

1. Write "6'h03" into the B_ADR of the Status flag register (Write).
2. Write the "Packet for instantaneous read" into the Write data register (The packet includes multiple bytes). "0" (That is 8'h80) is entered into the Buffer Address section in the packet.
3. Read the Status flag register (Read) to confirm VALID_R.

   VALID_R bit is in D6 bit of Status flag register (Read).

   "1" is set to VALID_R when the read data are entered in the "Read buffer register" (#1) of the Intermediate register.
4. Write "6'h01" into the B_ADR of the Status flag register (Write).
5. Read the data register to obtain the expected data.

L2.5.4 Read Buffer Register

It is assigned as the "Intermediate Register #1". Data value, which was designated to read from control registers by the "Instantaneous read register" are read from this register.

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#1	R	Read buffer register							

L2.6 Initialization Procedure

In case of the Power-on (hardware rest), be sure to follow the following procedure.
When initialization is not executed as following procedure exactly, the internal hardware may not be initialized correctly.

L2.6.1 Power Management Setup

It is the register for power management setup of digital sections.
It is in the "Intermediate register #5".

Default 8'h0F

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#5	W/R	"0"	"0"	"0"	"0"	DP3	DP2	DP1	DP0

"1" makes it power-down; common to every bits. Logic "0" makes the power-down cancel.

DP3 : A bit for the current control of a built-in memory in a synthesizer section.

DP2, DP1 : Bits for the operation control of internal clock in a synthesizer section..

DP0 : A bit for clock input control of CLKI pins.

This is a register for the power management setup of analog section.
It is in the Intermediate Register #6.

Default 8'hBF

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#6	W/R	PLLPD	"0"	AP4R	AP4L	AP3	AP2	AP1	AP0

"1" makes it power-down; common to every bits. "0" makes the power-down cancel.

PLLPD : A bit for an operation control of the built-in PLL.
AP0 : A bit for an operation control of VREF circuit.
AP1 : A bit for an operation control for a speaker amplifier for SPOUT1 output, a volume circuit of SP amplifier sections, a volume circuit, and EQ amplifier in the EQ sections.
AP2 : A bit for an operation control for SPOUT2 output in the speaker output section.
AP3 : A bit for an operation control of DAC and "Stereo → Mono conversion section".
AP4L : A bit for an operation control of a headphone volume circuit of the Lch side.
AP4R : A bit for an operation control of a headphone volume circuit of the Rch side.

Initialization Procedure

1. Set /RST to logic “L” at the same time as the power-on of VDD.
   - 100μs or over as the width of /RST=“L” is needed.
   - During /RST=L, clock input is arbitrary. (It does not care about the clock)
   - However, do not input an intermediate level that does not meet V_{IH} or V_{IL} into CLKI pin.
2. Write 8’h00 into the address #7 to #15 and #63 in the “Intermediate Register Bank 0”.
   →It is an insurance setup on the assumption that hardware-reset does not work normally because of disturbance.
3. Set up the PLL. (Intermediate Register #30, #31)
   When using in the TCXO mode, set the CKSEL bit to “1” at this time.
4. Set the DP0 to “0”.
5. After the input from CLKI has been stable at the actual operating state (frequency and level), wait for at least 2ms, and then set the PLLPD and AP0 to “0” respectively.
6. After waiting for more than [10ms×(the capacity value connected to VREF pin/ 0.1uF)], set the DP1 to “0”.
7. Set the DP2 to “0”.
8. Set the SFTRST (Intermediate Register #4) to “1”.
9. Return the SFTRST to “0”.
10. Make an interval more than 2fs (= 41.7 μs)
11. Confirm whether software-reset has become valid.
    For example, when the Control Register (such as #192 to #207 and #208 to #223) for which only software reset is valid is read and the contents is the default value, it proves that the software reset is working normally, then proceed to step 12. On the contrary, if the register has not default value, determine that the software reset has failed, and then repeat the step 8 through 11.
    (On the assumption that the software reset does not work normally even if executing it many times, timeout process etc. is needed.)
12. Set the DP3 to “0”.
13. Set AP1, AP3, AP4L, and AP4R to “0”.
14. After the elapse of 10μs or more, set AP2 to “0”.
15. Regular operation.

Please perform a setup of AP* as necessary.

Although it is necessary to execute a setup of both DP* and PLLPD bit surely during the initialization procedure, be sure to perform a setup of AP* bit as necessary.
For more details, refer to the “L2.7.3 A Setup According to Configuration to Use Form”.

Note for a setup procedure

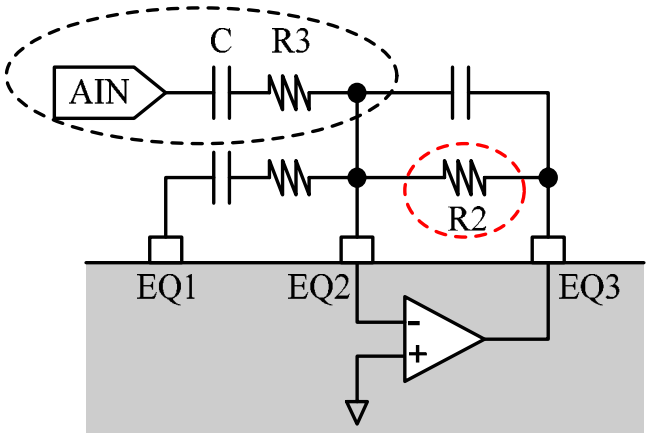
- Be sure to apply another write cycle to each step when the number of setup procedure differs.
- There is a register which cannot be accessed unless all of DP0 to DP3, and PLLPD are canceled (=“0”).

  → for the details, refer to the “L3.1 Register map“.
- A headphone output (HPOUT-L/MONO pin, HPOUT-R pin) is changed from unfixed potential to VREF potential immediately after AP3, AP4L, and AP4R are set to “0”. Therefore, please perform MUTE processing in the external of device.
- As shown in the following figure, when there is an analog mix from the outside in EQ amplifier section, it is necessary to reserve a time until the time at which MUTE of SPVOL is cancelled from the setup of AP2= “0”.
- When sufficient time is not reserved, the offset noise occurs from a speaker output.

  The period is determined by a time constant given by C and (R2+R3) that are attached to the analog input path.

  When the settling condition is 99%, the time “t” is given by the following formula.

  $$1 - \exp\left(-t / (R2+R3)\, C \right) = 0.99$$



L2.7 Power-down Procedure

Be sure to perform the power down transition or release according to the following procedure.

L2.7.1 Sequence for Transition to Power-down (Synthesizer Section)

1. In the state of which the sound generation is completely terminated, the volume (the Intermediate Register #7 to #10) of an analog section is setup to MUTE.
2. Set the DP3 to “1”.
3. Set the DP2 to “1”.
4. Set the DP1 to “1”.
5. Set the PLLPD, AP0 to AP4L, and AP4R to “1”.
6. Set the DP0 to “1”.

Here, the transition to the power-down is completed.

L2.7.2 Sequence for Power-down Cancellation

1. Set the DP0 to “0”.
2. After the input from CLKI has been stable at the actual operating state (frequency, level), take at least 2ms, and then set the PLLPD and AP0 to “0”.
3. After waiting for [10ms×(the capacity value connected to VREF pin / 0.1uF)], set the DP1 to “0”.
4. Set the DP2 and DP3 to “0”.
5. Set the AP1, AP3, AP4L, and AP4R to “0”.
6. After waiting 10μs or more, AP2 is set as “0.”
7. Normal operation. Cancel the MUTE operation to the Analog Volume to be used.

   Here, cancellation of the power-down is completed.

Perform a setup of AP* as necessary.

Although it is necessary to execute a setup of DP* and a PLLPD bit surely during the initialization procedure, be sure to perform a setup of AP* bit as necessary.
For the details, refer to the “L2.7.3 A Setup According to Configuration to Use Form”.

Notes for the transition to power down & the cancellation setup procedure

Note for the same contents as the “Notes for setting procedure” of the “L2.6 Initialization Procedure”.

L2.7.3 A Setup According to Configuration to Use Form

In the case of using only a headphone output and not using a speaker output

Use AP1 and AP2 by fixation.
Be sure to set SPVOL (the Intermediate Register #10) to MUTE.

In the case of using only a speaker amplifier output and not using a digital section and a headphone output

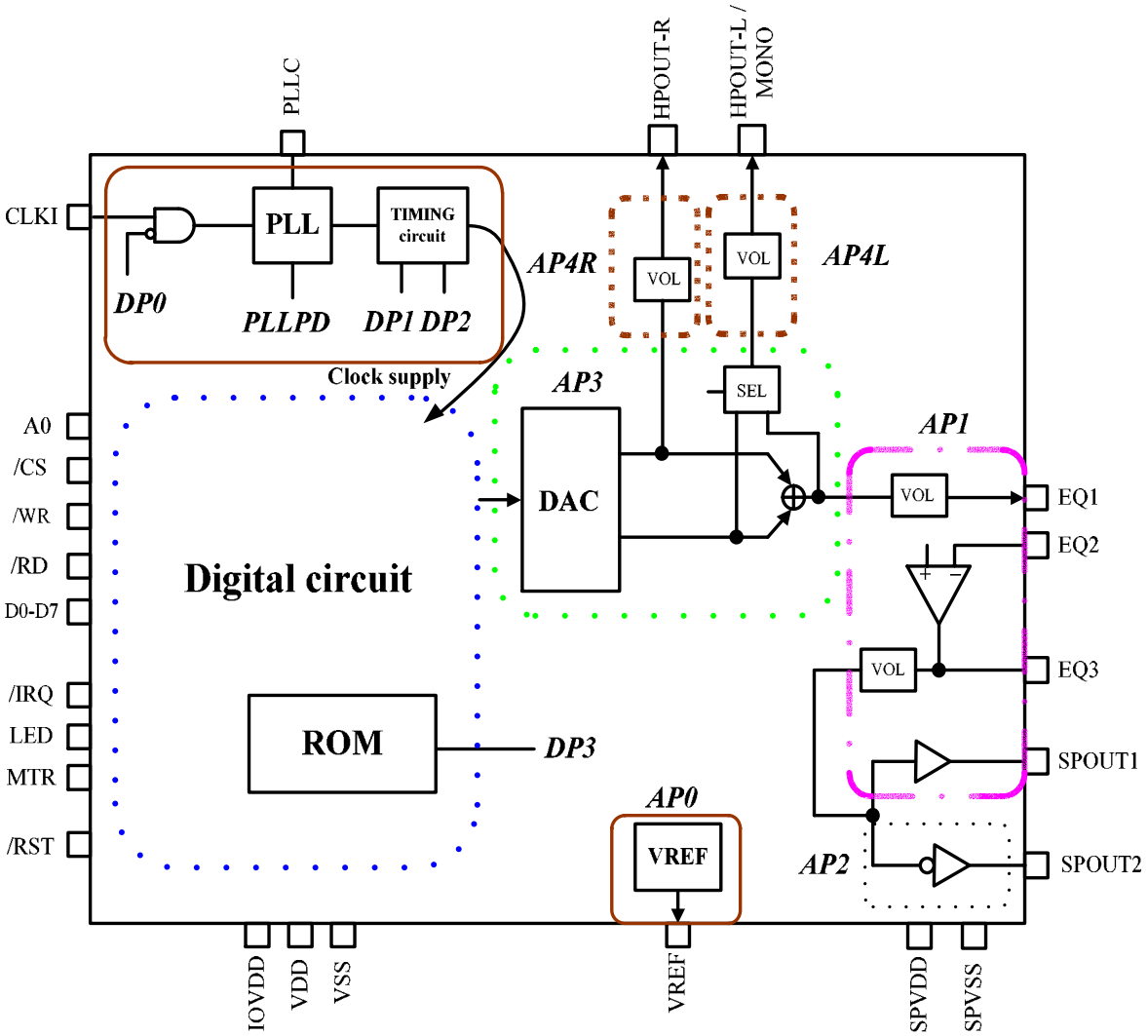
Use DP0 to DP3, PLLPD, AP3, AP4L, and AP4R by “1” fixation.
However, be sure to perform a control of DP0 to DP3 and PLLPD at the time of an Initialization sequence.
Be sure to set HPVOLL, HPVOLR, and EQVOL (the Intermediate Register #7 to 9) to MUTE.

In the case of using only a speaker amplifier output and not using a headphone output. (A digital part uses it)

Use AP4L and AP4R by “1” fixation.
Be sure to set HPVOLL and HPVOLR (the Intermediate Register #7 to #9) to MUTE.

L2.7.4 Division of the Power Management Control

The division of the control is made as follow.



L2.8 Setup Procedure to Sound Generation

In the Case of Performing the HV Playback

It explains from the place where the initialization sequence is completed.

1. Set the Intermediate Register #56 HVMODE bit to “1”.
   The resources of WT #16 to #24 are assigned for HV.
2. MUTE of HVVOL in the Intermediate Register #44 is released and set to the arbitrary value.
3. Set the each volume to the arbitrary value.
4. Set the Control Register #500 to #536 in order.
5. When the Control Register #536 KeyOn is changed to “1”, the sound is pronounced.

L3 Function Detail

This section describes the details of each function.

L3.1 Register map

L3.1.1 Interface Register map

The map of the Interface Register is as follows.

A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	W	IRQ	VALID_R	B_ADR					
#0	R	BUSY	VALID_R	“0”	“0”	FULL_DW	FULL_W	EMP_DW	EMP_W
#1	W	Write Data Register							
#1	R	Read Data Register							

L3.1.1.1 List of default values, reset valid range, and power down accessibility

A_Address	W/R	Content of register	Default value	Reset valid range	Power down accessibility
# 0	W	Status flag register (WRITE)	8’h00	H&S is valid only for VALID_R (*2) Only H is valid for IRQ and B_ADR	accessible
# 0	R	Status flag register (READ)	8’h03 (*1)	H&S is valid for other than BUSY.	accessible
# 1	W	Write data register	–	–	accessible
#1	R	Readout data register	–	–	accessible

Supplementary information

(*1) It may become 83h depending on the status of BUSY.

(*2) “H&S is valid” means that “It is initialized by either the hardware reset or the software reset”.

“Only H is valid” means that “It is initialized only by the hardware reset”.

(It is not initialized by the software reset.)

“The occasion for Power-down” is the state that any one of DP0 to DP3 and PLLPD is “1”.

L3.1.2 Intermediate Register Map

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	W/R	FIFO	TM#2	TM#1	TM#0	SIRQ#1	SIRQ#0	STM#1	STM#0
#1	W	Delayed WRITE register							
#1	R	READ buffer register							
#2	W	Instantaneous WRITE register							
#3	W	Instantaneous READ register							
#4	W/R	SFTRST	R_FIFO#1	R_FIFO#0	R_SEQ#1	R_SEQ#0	“0”	BANK	

BANK 0

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#5	W/R	“0”	“0”	“0”	“0”	DP3	DP2	DP1	DP0
#6	W/R	PLLPD	“0”	AP4R	AP4L	AP3	AP2	AP1	AP0
#7	W/R	“0”	“0”	“0”	EQVOL				
#8	W/R	MONO	“0”	“0”	HPVOLL				
#9	W/R	“0”	“0”	“0”	HPVOLR				
#10	W/R	VSEL2	VSEL1	“0”	SPVOL				
#11	W/R	“0”	“0”	“0”	“0”	“0”	“0”	“0”	MIDLED
#12	W/R	“0”	LED FREQ			“0”	LED MODE		
#13	W/R	“0”	“0”	“0”	“0”	“0”	“0”	“0”	MIDMTR
#14	W/R	“0”	MTR FREQ			“0”	MTR MODE		
#15	-	Reserved							
#16	W/R	“0”	“0”	SIRQ#5	SIRQ#4	SIRQ#3	SIRQ#2	“0”	“0”
#17	W/R	EFIFO	ETM#2	ETM#1	ETM#0	ESIRQ#1	ESIRQ#0	ESTM#1	ESTM#0
#18	W/R	“0”	“0”	ESIRQ#5	ESIRQ#4	ESIRQ#3	ESIRQ#2	“0”	“0”
#19	R	“0”	RAM#0						
#20	R	“0”	RAM#1						
#21	R	“0”	RAM#2						
#22	R	“0”	RAM#3						
#23	R	“0”	RAM#4						
#24	R	“0”	RAM#5						
#25	R	“0”	“0”	STREAM PG#0					
#26	R	“0”	“0”	STREAM PG#1					
#27	R	“0”	TIMER#0 COUNT						
#28	R	“0”	TIMER#1 COUNT						
#29	R	“0”	TIMER#2 COUNT						
#30	W/R	CKSEL	“0”	“0”	ADJUST 1				
#31	W/R	“0”	ADJUST 2						
#32	R	“0”	“0”	“0”	SEQUENCE COUNT (H)				
#33	R	SEQUENCE COUNT (M)							
#34	R	SEQUENCE COUNT (L)							
#35	W/R	MS_S(H)							
#36	W/R	MS_S(L)						“0”	“0”
#37	W/R	“0”	“0”	“0”	“0”	“0”	IRQ POINT		
#38	W/R	“0”	“0”	“0”	“0”	“0”	“0”	CNTRST	START
#39	W/R	MASTER VOLL					“0”	MASTER L SHIFT	
#40	W/R	MASTER VOLR					“0”	MASTER R SHIFT	
#41	W/R	FMVOL					“0”	FMSHIFT	
#42	W/R	WTVOL					“0”	WTSHIFT	
#43	W/R	STMVOL					“0”	STMSHIFT	
#44	W/R	HVVOL					“0”	HVSHIFT	
#45	-	Reserved							
#46	W/R	“0”	MS_T						
#47	W/R	“0”	TIMER #0						
#48	W/R	“0”	“0”	“0”	“0”	“0”	TS #0	ONE #0	TMST #0
#49	W/R	“0”	TIMER #1						
#50	W/R	“0”	“0”	“0”	“0”	“0”	TS #1	ONE #1	TMST #1
#51	W/R	“0”	TIMER #2						
#52	W/R	“0”	“0”	“0”	“0”	“0”	TS #2	ONE #2	“0”
#53	W/R	“0”	“0”	“0”	“0”	“0”	“0”	“0”	TMST#2A
#54	W/R	“0”	“0”	“0”	“0”	“0”	“0”	“0”	TMST#2B
#55	W/R	SV_MUTE		SV_CHV	SV_PAN	MVSEL	NOP2E	FINT	DADJT
#56	W/R	“0”	“0”	“0”	“0”	“0”	HVMODE	STMMODE	FMMODE
#57	W/R	“0”	“0”	BUF SIZE		“0”	“0”	STM IRQPOINT	
#58	W/R	“0”	“0”	“0”	STEREO	“0”	“0”	RSTM#1	RSTM#0
#59~#63	W/R	Reserved							
B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0

L3.1.2.1 Default values, Reset valid range, and Power-down accessibility list

B_Address	<<Write side>>	<<Read side>>	Default value	Reset valid range	Power down accessibility
# 0	Interrupt flag (1)		8'h00	H & S is valid.	accessible
# 1	Delayed write register	Read buffer register #0	8'h00	H & S is valid.	not accessible
# 2	Instantaneous write register		8'h00	H & S is valid.	not accessible
# 3	Instantaneous read register		8'h00	H & S is valid.	not accessible
# 4	Fundamental setup		8'h00	Only H is valid.	accessible

B_Address	Register content	Default value	Reset valid range	Power down accessibility
# 5	Power management setup (Digital)	8'h0F	Only H is valid.	accessible only DP3 cannot be rewritten.
# 6	Power management setup (Analog)	8'h9F	Only H is valid.	accessible
# 7	Analog setup (EQVOL)	8'h00	Only H is valid.	accessible
# 8, 9	Analog setup (HPVOLL, HPVOLR, MONO)	8'h00	Only H is valid.	accessible
# 10	Analog setup (SPVOL)	8'h00	Only H is valid.	accessible
# 11, 12	LED setup	8'h00	Only H is valid.	accessible
# 13, 14	Vibrator setup	8'h00	Only H is valid.	accessible
#15	Reserved (Access is prohibited)	–	–	–
# 16	Interrupt flag (2)	8'h00	H & S is valid.	accessible only for read
# 17, 18	Interrupt enable / disable setup	8'h00	H & S is valid.	not accessible
# 19 ~ 24	Software interrupt read	8'h00	H & S is valid.	not accessible
# 25, 26	Stream playback position read-out	8'h00	H & S is valid.	not accessible
#27 ~ 29	Timer count read-out	8'h7F	H & S is valid.	not accessible
# 30, 31	PLL setup	#30=8'h0A #31= 8'h37	Only H is valid.	accessible
# 32 ~ 38	Sequencer control	8'h00	H & S is valid.	not accessible
# 39 ~ 40	Master volume setup	8'h00	H & S is valid.	not accessible
#41 ~ 45	Volume setup for individual synthesizers	8'h00	H & S is valid.	not accessible
# 46 ~ 54	Timer setting	8'h00	H & S is valid.	not accessible
# 55	Extension function setting	8'h00	H & S is valid.	not accessible
# 56	Synthesizer mode setting	8'h00	H & S is valid.	not accessible
# 57, 58	Stream playback interrupt setting	#57=8'h10 #58=8'h00	H & S is valid.	not accessible
# 59 ~ 63	Reserved (Access is prohibited.)	–	–	–

Access prohibited domain

Be sure to set 2'b00 to the BANK bit in the Intermediate Register #4.
Bank 1 to Bank 3 are reserved area (for LSI test or other purposes). Access is prohibited.

L3.1.3 Control Register Map

FM Voice #0 ~ #15

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0	
# 0	W/R	Voice Adr [14:8]							FM Voice #0
# 1	W/R	Voice Adr [7:1]							
# 2	W/R	VOVOL					MTRON	LEDON	
# 3	W/R	EXCH	BLOCK			FNUM (H)			
# 4	W/R	FNUM (L)							
# 5	W/R	KeyOn	MUTE	RST	#CH				

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# 90	W/R	Voice Adr [14:8]							FM Voice #15
# 91	W/R	Voice Adr [7:1]							
# 92	W/R	VOVOL					MTRON	LEDON	
# 93	W/R	EXCH	BLOCK			FNUM (H)			
# 94	W/R	FNUM (L)							
# 95	W/R	KeyOn	MUTE	RST	#CH				

WT Voice #0 ~ #15

# 96	W/R	Voice Adr [14:8]							WT Voice#0
# 97	W/R	Voice Adr [7:1]							
# 98	W/R	VOVOL					MTRON	LEDON	
# 99	W/R	EXCH	BLOCK			FNUM (H)			
# 100	W/R	FNUM (L)							
# 101	W/R	KeyOn	MUTE	RST	#CH				

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# 186	W/R	Voice Adr [14:8]							WT Voice#15
# 187	W/R	Voice Adr [7:1]							
# 188	W/R	VOVOL					MTRON	LEDON	
# 189	W/R	EXCH	BLOCK			FNUM (H)			
# 190	W/R	FNUM (L)							
# 191	W/R	KeyOn	MUTE	RST	#CH				

Channel Parameter

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0	CHVOL
#192 ~ #207	W/R	CHVOL #0 ~ CHVOL#15					“0”	DRCT	

＊#192 is CHVOL#0, #193 is CHVOL#1..... #207 is CHVOL#15

#208 ~ #223	W/R	CHPAN#0 ~ CHPAN#15				“0”	DRCT	CHPANPOT

#224 ~ #239	W/R	EVIB#0 ~ EVIB#15	“0”	ESUS#0 ~ ESUS#15	“0”	XVB#0 ~ XVB #15		EVIB / ESUS / XVB

#240	W/R	“0”	“0”	INT #0	FRAC(H) #0		BEND #0
#241	W/R	FRAC (L) #0				“0”	

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#270	W/R	“0”	“0”	INT #15	FRAC(H) #15		BEND #15
#271	W/R	FRAC (L) #15				“0”	

FM Sound Generator #16 ~ #31

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0	
# 272	W/R	Voice Adr [14:8]							FMVoice#16
# 273	W/R	Voice Adr [7:1]							
# 274	W/R	VOVOL					MTRON	LEDON	
# 275	W/R	EXCH	BLOCK			FNUM (H)			
# 276	W/R	FNUM (L)							
# 277	W/R	KeyOn	MUTE	RST	#CH				

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# 362	W/R	Voice Adr [14:8]							FMVoice#31
# 363	W/R	Voice Adr [7:1]							
# 364	W/R	VOVOL					MTRON	LEDON	
# 365	W/R	EXCH	BLOCK			FNUM (H)			
# 366	W/R	FNUM (L)							
# 367	W/R	KeyOn	MUTE	RST	#CH				

WT Sound Generator #16 ~ #31

# 368	W/R	Voice Adr [14:8]							WTVoice#16
# 369	W/R	Voice Adr [7:1]							
# 370	W/R	VOVOL					MTRON	LEDON	
# 371	W/R	EXCH	BLOCK			FNUM (H)			
# 372	W/R	FNUM (L)							
# 373	W/R	KeyOn	MUTE	RST	#CH				

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# 458	W/R	Voice Adr [14:8]							WTVoice#31
# 459	W/R	Voice Adr [7:1]							
# 460	W/R	VOVOL					MTRON	LEDON	
# 461	W/R	EXCH	BLOCK			FNUM (H)			
# 462	W/R	FNUM (L)							
# 463	W/R	KeyOn	MUTE	RST	#CH				

FM Extended Waveform, Software Interrupt, and etc.

# 464	W/R	FM WAVE#15 [14:8]	FM extension waveform
# 465	W/R	FM WAVE#15 [7:1]	
# 466	W/R	FM WAVE#23 [14:8]	
# 467	W/R	FM WAVE#23 [7:1]	
# 468	W/R	FM WAVE#31 [14:8]	
# 469	W/R	FM WAVE#31 [7:1]	

# 470	W/R	RAM #0	Software interrupt setting
# 471	W/R	RAM #1	
# 472	W/R	RAM #2	
# 473	W/R	RAM #3	
# 474	W/R	RAM #4	
# 475	W/R	RAM #5	

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0	
# 476	W/R	“0”	“0”	“0”	“0”	“0”	“0”	LED	LED control
# 477	W/R	“0”	“0”	“0”	“0”	“0”	“0”	MTR	MTR control
# 478	W	“0”	“0”	“0”	“0”	“0”	“0”	“0”	NOP_2
# 479	W	“0”	“0”	“0”	“0”	“0”	“0”	“0”	NOP
# 480	W/R	“0”	“0”	“0”	“0”	“0”	“0”	SEQSTOP	Sequencer stop
# 481	–	Reserved							Reserved
# 482	R	“0”	“1”	“0”	“0”	“0”	“0”	“1”	ID register

Extension Channel Parameter

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0	
# 483	W/R	EXCHVOL					"0"	DRCT	Extension channel
# 484	W/R	EXPANPOT					"0"	"0"	
# 485	W/R	"0"	"0"	EXESUS	"0"	EXXVB			
# 486	W/R	"0"	"0"	EXINT		EXFRAC(H)			
# 487	W/R	EXFRAC(L)						"0"	

HV Sound Generator setup

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0	
# 500	W/R	"0"	PAI_0	WS_0					Waveform selection at the time of a voiced sound
# 501	W/R	"0"	PAI_1	WS_1					
# 502	W/R	"0"	PAI_2	WS_2					
# 503	W/R	"0"	PAI_3	WS_3					
# 504	W/R	"0"	PAI_4	WS_4					
# 505	W/R	"0"	PAI_5	WS_5					
# 506	W/R	"0"	PAI_6	WS_6					
# 507	W/R	"0"	PAI_7	WS_7					
# 508	W/R	FMT Level 0							Formant 0
# 509	W/R	"0"	BLOCK_F 0			FNUM_F 0(H)			
# 510	W/R	FNUM_F 0(L)							
# 511	W/R	FMT Level 1							Formant 1
# 512	W/R	"0"	BLOCK_F 1			FNUM_F 1(H)			
# 513	W/R	FNUM_F 1(L)							
# 514	W/R	FMT Level 2							Formant 2
# 515	W/R	"0"	BLOCK_F 2			FNUM_F 2(H)			
# 516	W/R	FNUM_F 2(L)							
# 517	W/R	FMT Level 3							Formant 3
# 518	W/R	"0"	BLOCK_F 3			FNUM_F 3(H)			
# 519	W/R	FNUM_F 3(L)							
# 520	W/R	FMT Level 4							Formant 4
# 521	W/R	"0"	BLOCK_F 4			FNUM_F 4(H)			
# 522	W/R	FNUM_F 4(L)							
# 523	W/R	FMT Level 5							Formant 5
# 524	W/R	"0"	BLOCK_F 5			FNUM_F 5(H)			
# 525	W/R	FNUM_F 5(L)							
# 526	W/R	FMT Level 6							Formant 6
# 527	W/R	"0"	BLOCK_F 6			FNUM_F 6(H)			
# 528	W/R	FNUM_F 6(L)							
# 529	W/R	FMT Level 7							Formant 7
# 530	W/R	"0"	BLOCK_F 7			FNUM_F 7(H)			
# 531	W/R	FNUM_F 7(L)							
# 532	W/R	"0"	"0"	"0"	"0"	"0"	MTRON	LEDON	LED,MTR Synchronous control
# 533	W/R	EXCH	BLOCK_P			FNUM_P(H)			Pitch
# 534	W/R	FNUM_P(L)							
# 535	W/R	"0"	"0"	"0"	"0"	U/V	PANOFF	DIREC	PANOFF, DIREC, U/V
# 536	W/R	KeyOn	MUTE	RST	# CH				KeyOn etc.

AL synthesizer setting

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0	
# 537	W/R	LPFCLR	"0"	SYNTH		"0"	NOISE	"0"	LPF control
# 538	W/R	"0"	"0"	Q					Resonance
# 539	W/R		Fc0(H)						Cut off frequency setting
# 540	W/R	Fc0(L)							
# 541	W/R		Fc1(H)						
# 542	W/R	Fc1(L)							
# 543	W/R		Fc2(H)						
# 544	W/R	Fc2(L)							
# 545	W/R		Fc3(H)						
# 546	W/R	Fc3(L)							
# 547	W/R		Fc4(H)						
# 548	W/R	Fc4(L)							
# 549	W/R	"0"	"0"	FAR					Change rate setting
# 550	W/R	"0"	"0"	FDR					
# 551	W/R	"0"	"0"	FSR					
# 552	W/R	"0"	"0"	FRR					
# 553	W/R	LFO DEPTH			LFO MODE	LFO FREQ			LFO setting
# 554	W/R	FIX0E	FIX_BLOCK0			FIX_FNUM0 (H)			FIX
# 555	W/R	FIX_FNUM0 (L)							
# 556	W/R	FIX1E	FIX_BLOCK1			FIX_FNUM1 (H)			
# 557	W/R	FIX_FNUM1 (L)							
# 558	W/R	FIX2E	FIX_BLOCK2			FIX_FNUM2 (H)			
# 559	W/R	FIX_FNUM2 (L)							
# 560	W/R	FIX3E	FIX_BLOCK3			FIX_FNUM3 (H)			
# 561	W/R	FIX_FNUM3 (L)							
# 562	W/R	LFORST	FcOFFSET(H)						Cut off frequency Offset setting
# 563	W/R	FcOFFSET(L)							

Notes about the Control Register

- All control registers can be accessed only during the time of power-down released. (Power-down release is a state in which DP0, DP1, DP2, DP3, and PLLPD bit are all "0")
- Access after the control register #563 is prohibited.
- Be sure to write "0" into the bit in which "0" is written.
- If it is rewritten less than 1fs (=20.83µs), there are some registers which are not reflected to operation as a setup. The following are such registers.

  Control register #0 to #463 (Except Voice Adr)
  Control register #464 to #469
  Control register # 483 to #487
  Control register #500 to #536
  Control register #537 to #563

  When you change a register setup a value less than 1 fs in the case of use, reserve the time using NOP_2 of the Control register #478. For the details, refer to "L3.2.5.2 NOP_2".
  Probably, as for KeyOn, MUTE, and a RST bit, register setup value may actually be changed in time of less than 1 fs.
  About these bits, even if it does not use NOP_2, there is the method to reserve a time automatically. For the details, refer to "L3.2.5.3 NOP2E".

L3.1.3.1 Default values, Reset valid range, and Power down accessibility list

All registers are not accessible during power-down.

C_Address	Register content	Default value	Reset valid range
# 0 ~ 95	FM voice setup (#0 to #15)	7'h00	Only S is valid
# 96 ~ 191	WT voice setup (#0 to #15)	7'h00	Only S is valid
#192~ 207	Channel volume	7'h60	Only S is valid
#208~ 223	Channel panpot	7'h3C	Only S is valid
#224~ 239	Channel vibrato designation, and channel sustain designation	7'h00	Only S is valid
#240~ 271	Channel pitch bend	Odd #=7'h00 Even #=7'h08	Only S is valid
#272~ 367	FM voice setup (#16 to #31)	7'h00	Only S is valid
#368~ 463	WT voice setup (#16 to #31)	7'h00	Only S is valid
#464~ 469	FM expanded waveform setup	7'h00	Only S is valid
#470~ 475	Software interrupt setup	7'h00	H&S is valid
#476	LED control	7'h00	H&S is valid
#477	MTR control	7'h00	H&S is valid
#478, 479	NOP, NOP_2 setup	7'h00	–
#480	Sequencer stop	7'h00	H&S is valid
#481	Reserved	–	–
#482	ID register	7'h21	–
#483	Expanded channel volume	7'h60	H&S is valid
#484	Expanded channel panpot	7'h3C	H&S is valid
#485	Expanded channel vibrato designation channel sustain designation	7'h00	H&S is valid
#486, 487	Expanded channel pitch bend	#486=7'h08 #487=7'h00	H&S is valid
#500~507	HV synthesizer waveform selection at the time of voiced sound	7'h00	H&S is valid
#508~531	HV synthesizer Formant setup 0 to 7	7'h00	H&S is valid
#532	HV synthesizer LED, MTR synchronous control	7'h00	H&S is valid
#533、534	HV synthesizer pitch setup	7'h00	H&S is valid
#535	HV synthesizer voiced sound / non-voiced sound change, panpot off setup, etc.	7'h00	H&S is valid
#536	HV synthesizer voice control	7'h00	H&S is valid
#537	AL synthesizer noise setup, LPF input resource select, LPF clear	7'h00	H&S is valid
#538	AL synthesizer resonance	7'h00	H&S is valid
#539~ 548	AL synthesizer cutoff frequency setup	7'h00	H&S is valid
#549~ 552	AL synthesizer change rate setup	7'h00	H&S is valid
#553	AL synthesizer LFO setup	7'h00	H&S is valid
#554~ 561	AL synthesizer FIX setup	7'h00	H&S is valid
#562, 563	AL synthesizer cutoff frequency offsetting setup	7'h00	H&S is valid

L3.1.3.2 ID register

Default 7'h21

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
#482	R	"0"	"1"	"0"	"0"	"0"	"0"	"1"

This Control register #482 is a register to read the device ID and Version ID.
This is a Read only register. 7'h21 is read.

- D6 to D4 bits: Device ID
- D3 to D0 bits: Version ID

L3.1.4 SRAM

SRAM and ROM are embedded.
The size of SRAM is 8k bytes.
SRAM is used for the Stream playback and the voice registration of FM and WT.

FM Voice Parameter

The map of FM voice parameter is as follows.

	D7	D6	D5	D4	D3	D2	D1	D0	
#0	PANPOT					“0”	BO		
#1	LFO		PE	PAN OFF	“0”	ALG			
#2	SR				XOF	“0”	SUS	KSR	OP1
#3	RR				DR				
#4	AR				SL				
#5	TL						KSL		
#6	“0”	DAM		EAM	“0”	DVB		EVB	
#7	MULTI				“0”	DT			
#8	WS					FB			
#9	SR				XOF	“0”	SUS	KSR	OP2
#10	RR				DR				
#11	AR				SL				
#12	TL						KSL		
#13	“0”	DAM		EAM	“0”	DVB		EVB	
#14	MULTI				“0”	DT			
#15	WS					“0”			
#16	SR				XOF	“0”	SUS	KSR	OP3
#17	RR				DR				
#18	AR				SL				
#19	TL						KSL		
#20	“0”	DAM		EAM	“0”	DVB		EVB	
#21	MULTI				“0”	DT			
#22	WS					FB			
#23	SR				XOF	“0”	SUS	KSR	OP4
#24	RR				DR				
#25	AR				SL				
#26	TL						KSL		
#27	“0”	DAM		EAM	“0”	DVB		EVB	
#28	MULTI				“0”	DT			
#29	WS					“0”			

WT Voice & Parameter for a Stream Playback

	D7	D6	D5	D4	D3	D2	D1	D0
# 0	PANPOT					“0”	STM	PE
# 1	LFO		“0”	“0”	“0”	PAN OFF	MODE	
# 2	SR				XOF	“0”	SUS	“0”
# 3	RR				DR			
# 4	AR				SL			
# 5	TL						“0”	“0”
# 6	“0”	DAM		EAM	“0”	DVB		EVB
# 7	START ADDRESS (H)							
# 8	START ADDRESS(L)							
# 9	LOOP POINT(H)							
# 10	LOOP POINT(L)							
# 11	END POINT (H)							
# 12	END POINT (L)							

L3.1.5 ROM Voice Map

●Normal

Pch#	Instrument		M_Address
0	GrandPno	FM param	0800
1	BritePno	FM param	0810
2	E.GrandP	FM param	0820
3	HnkyTonk	FM param	0830
4	E.Piano1	FM param	0840
5	E.Piano2	FM param	0850
6	Harpsi	FM param	0860
7	Clavi	FM param	0870
8	Celesta	FM param	0880
9	Glocken	FM param	0890
10	MusicBox	FM param	08A0
11	Vibes	FM param	08B0
12	Marimba	FM param	08C0
13	Xylophon	FM param	08D0
14	TubulBel	FM param	08E0
15	Dulcimar	FM param	08F0
16	DrawOrgn	FM param	0900
17	PercOrgn	FM param	0910
18	RockOrgn	FM param	0920
19	ChrchOrg	FM param	0930
20	ReedOrgn	FM param	0940
21	Acordion	FM param	0950
22	Harmnica	FM param	0960
23	TangoAcd	FM param	0970
24	NylonGtr	FM param	0980
25	SteelGtr	FM param	0990
26	JazzGtr	FM param	09A0
27	CleanGtr	FM param	09B0
28	Mute.G.tr	FM param	09C0
29	Ovrdrive	FM param	09D0
30	Dist.Gtr	FM param	09E0
31	GtrHarmo	FM param	09F0
32	AcoBass	FM param	0A00
33	FngrBass	FM param	0A10
34	PickBass	FM param	0A20
35	Fretless	FM param	0A30
36	SlapBas1	FM param	0A40
37	SlapBas2	FM param	0A50
38	SynBass1	FM param	0A60
39	SynBass2	FM param	0A70
40	Violin	FM param	0A80
41	Viola	FM param	0A90
42	Cello	FM param	0AA0
43	Contrabs	FM param	0AB0
44	TremStr	FM param	0AC0
45	PizzStr	FM param	0AD0
46	Harp	FM param	0AE0
47	Timpani	FM param	0AF0
48	Strings1	FM param	0B00
49	Strings2	FM param	0B10
50	Syn.Str1	FM param	0B20
51	Syn.Str2	FM param	0B30
52	ChoirAah	FM param	0B40
53	VoiceOoh	FM param	0B50
54	SynVoice	FM param	0B60
55	Orch.Hit	FM param	0B70
56	Trumpet	FM param	0B80
57	Trombone	FM param	0B90
58	Tuba	FM param	0BA0
59	Mute.Trp	FM param	0BB0
60	Fr.Horn	FM param	0BC0
61	BrasSect	FM param	0BD0
62	SynBras1	FM param	0BE0
63	SynBras2	FM param	0BF0

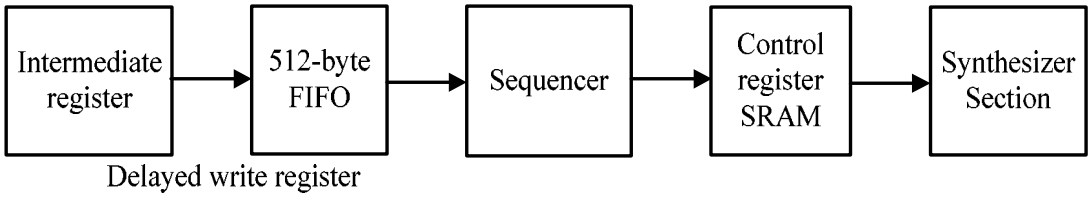
Pch#	Instrument		Address
64	SprnoSax	FM param	0C00
65	AltoSax	FM param	0C10
66	TenorSax	FM param	0C20
67	Bari.Sax	FM param	0C30
68	Oboe	FM param	0C40
69	Eng.Horn	FM param	0C50
70	Bassoon	FM param	0C60
71	Clarinet	FM param	0C70
72	Piccolo	FM param	0C80
73	Flute	FM param	0C90
74	Recorder	FM param	0CA0
75	PanFlute	FM param	0CB0
76	Bottle	FM param	0CC0
77	Shakhchi	FM param	0CD0
78	Whistle	FM param	0CE0
79	Ocarina	FM param	0CF0
80	SquareLd	FM param	0D00
81	SawLead	FM param	0D10
82	CaliopLd	FM param	0D20
83	ChiffLd	FM param	0D30
84	CharanLd	FM param	0D40
85	VoiceLd	FM param	0D50
86	FifthLd	FM param	0D60
87	Bass&Ld	FM param	0D70
88	NewAgePd	FM param	0D80
89	WarmPad	FM param	0D90
90	PolySyPd	FM param	0DA0
91	ChoirPad	FM param	0DB0
92	BowedPad	FM param	0DC0
93	MetalPad	FM param	0DD0
94	HaloPad	FM param	0DE0
95	SweepPad	FM param	0DF0
96	Rain	FM param	0E00
97	SoundTrk	FM param	0E10
98	Crystal	FM param	0E20
99	Atmosphr	FM param	0E30
100	Bright	FM param	0E40
101	Goblins	FM param	0E50
102	Echoes	FM param	0E60
103	Sci-Fi	FM param	0E70
104	Sitar	FM param	0E80
105	Banjo	FM param	0E90
106	Shamisen	FM param	0EA0
107	Koto	FM param	0EB0
108	Kalimba	FM param	0EC0
109	Bagpipe	FM param	0ED0
110	Fiddle	FM param	0EE0
111	Shanai	FM param	0EF0
112	TnklBell	FM param	0F00
113	Agogo	FM param	0F10
114	SteelDrm	FM param	0F20
115	WoodBlk	FM param	0F30
116	TaikoDrm	FM param	0F40
117	MelodTom	FM param	0F50
118	Syn.Drum	FM param	0F60
119	RevCymbl	FM param	0F70
120	FretNoiz	FM param	0F80
121	BrthNoiz	FM param	0F90
122	SeaShore	FM param	0FA0
123	Tweet	FM param	0FB0
124	Telphone	FM param	0FC0
125	Helicptr	FM param	0FD0
126	Applause	FM param	0FE0
127	Gunshot	FM param	0FF0

● Drum

Note#	Instrument		Address
24	SeqClick H	FM param	1000
25	Brush Tap	FM param	1010
26	Brush Swirl L	FM param	1020
27	Brush Slap	FM param	1030
28	Brush Swirl H	FM param	1040
29	Snare Roll	FM param	1050
30	Castanet	FM param	1060
31	Snare L	PCM param	1070
32	Sticks	FM param	1080
33	Bass Drum L	PCM param	1090
34	Open Rim Shot	FM param	10A0
35	Bass Drum M	PCM param	10B0
36	Bass Drum H	PCM param	10C0
37	Closed Rim Shot	FM param	10D0
38	Snare M	PCM param	10E0
39	Hand Clap	FM param	10F0
40	Snare H	PCM param	1100
41	Floor Tom L	PCM param	1110
42	Hi-Hat Closed	PCM param	1120
43	Floor Tom H	PCM param	1130
44	Hi-Hat Pedal	PCM param	1140
45	Low Tom	PCM param	1150
46	Hi-Hat Open	PCM param	1160
47	Mid Tom L	PCM param	1170
48	Mid Tom H	PCM param	1180
49	Crash Cymbal 1	PCM param	1190
50	High Tom	PCM param	11A0
51	Ride Cymbal 1	PCM param	11B0
52	Chinese Cymbal	PCM param	11C0
53	RideCymbal Cup	FM param	11D0
54	Tamboulin	FM param	11E0
55	Splash Cymbal	PCM param	11F0
56	Cowbell	FM param	1200
57	Crash Cymbal 2	PCM param	1210
58	Vibraslap	FM param	1220
59	Ride Cymbal 2	PCM param	1230
60	Bongo H	FM param	1240
61	Bongo L	FM param	1250
62	Conga H Mute	FM param	1260
63	Conga H Open	FM param	1270
64	Conga L	FM param	1280
65	Timbale H	FM param	1290
66	Timbale L	FM param	12A0
67	Agogo H	FM param	12B0
68	Agogo L	FM param	12C0
69	Cabasa	FM param	12D0
70	Maracas	FM param	12E0
71	Samba Whistle H	FM param	12F0
72	Samba Whistle L	FM param	1300
73	Guiro Short	FM param	1310
74	Guiro Long	FM param	1320
75	Claves	FM param	1330
76	Wood Block H	FM param	1340
77	Wood Block L	FM param	1350
78	Cuica Mute	FM param	1360
79	Cuica Open	FM param	1370
80	Triangle Mute	FM param	1380
81	Triangle Open	FM param	1390
82	Shaker	FM param	13A0
83	Jingle Bell	FM param	13B0
84	Belltree	FM param	13C0

L3.2 Sequencer

The role of a sequencer section is to manage data written into the Delayed write register in the Intermediate Register #1, and to control a latter synthesizer section. The circuits located before and after the sequencer are explained in this section.



The 512-byte FIFO is located in the previous stage of the sequencer, the sequencer processes the data written into the Delayed write register in the Intermediate Register #1.
The format of data written into the Delayed write register is “Time information data＋Register setup value”. (For the details, refer to the “L2.5.2 Delayed Write Register“)

For the data which has been written into the FIFO, the sequencer is operated by the following steps.

1. Reads data from the FIFO
2. Counts the time in accordance with the time information designated with data
3. Writes data into the Control Register and SRAM located in the subsequent stage after the time is elapsed.
4. Reads subsequent data from the FIFO and repeats above steps from #2.

The data written into the Delayed write register are normally music data.
Setup for the sequencer sections are performed in the Intermediate Registers #32 to #38.

L3.2.1 Sequencer Setup

This section describes the registers to control the sequencer.

#32 ~ #34=Read Only , #35 ~ #38=Write / Read possible Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#32	R	"0"	"0"	"0"	SEQUENCE COUNT (H)				
#33	R	SEQUENCE COUNT (M)							
#34	R	SEQUENCE CONT (L)							
#35	W/R	MS_S(H)							
#36	W/R	MS_S(L)						"0"	"0"
#37	W/R	"0"	"0"	"0"	"0"	"0"	IRQ POINT		
#38	W/R	"0"	"0"	"0"	"0"	"0"	"0"	CNTRST	START

L3.2.1.1 SEQUENCE COUNT

The MS_S count value after a sequencer start can be read.
This is a read-only register.
A count value is latched at the timing specified the Intermediate Register #32.
The conditions in which count value is reset are the following three.

- At the time of hardware reset
- At the time of software reset
- When CNTRST bit of the Intermediate Register #38 is set to "1".

L3.2.1.2 MS_S

This is a register to set up the minimum unit time of a sequencer.
Time unit [sec] = (setting value of MS_S) / (192fs / 10) fs [Hz]: sampling frequency
When fs is 48.0 kHz, the resolution is 1.085µs.
By writing to MS_S (L), the setup value of MS_S (H) and MS_S (L) becomes effective.

L3.2.1.3 IRQ POINT

This is a register to designate the interrupt occurrence position of 512-byte FIFO.
For more detail, refer to the "L3.3 Interrupt ".

L3.2.1.4 START

This is a register to designate the operations of the sequencer. "0" : stopping "1" : starting

L3.2.1.5 CNTRST

This is a bit to clear the sequencer count values of #32 to #34.
"1" clears the values (all "0"). When the count value has been cleared, this bit automatically returns to "0". Therefore, it is not necessary to rewrite "0" after setting to "1".

When START bit and CNTRST bit are set to "1" at the same time;

The counts value of the sequencer is cleared, and the sequencer starts its operation.

The time of resolution of this device is a little different from MA-3.

Minimum resolution of MA-5 series = 1 / (192fs / 10) (=1.085µs)
Minimum resolution of MA-3 series = 1 /18fs (=1.157µs)

L3.2.2 Sequencer Stop Setup

The sequencer can be stopped by the Control Register.
A register to stop the sequencer is assigned to D0 bit of the Control Register #480.

Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 480	W/R	"0"	"0"	"0"	"0"	"0"	"0"	SEQSTOP

SEQSTOP: When "1" is set, START bit of the Intermediate Register #38 is reset.

Not only the transition from "0" to "1", but also the setting of "1" has the START bit of the Intermediate Register #38 reset. (The START bit is reset also by overwriting "1" to "1" of SEQSTOP).

L3.2.3 Clear-bits of Sequencer & FIFO

The bit for clearing a sequencer and FIFO are assigned in the Intermediate Register #4.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#4	W/R	SFTRST	R_FIFO#1	R_FIFO#0	R_SEQ#1	R_SEQ#0	"0"	BANK	

L3.2.3.1 R_FIFO#

- R_FIFO#1: This is a bit to clear the FIFO for instantaneous writing. "1" clears the FIFO.
  - Data to write into the Instantaneous write register after the clear, should be begun with the address of the packet for instantaneous writing or for instantaneous reading.
  - The instantaneous writing/reading cannot be made when R_FIFO#1= "1".

- R_FIFO#0: This is a bit to clear the FIFO for delayed writing. Logic "1" clears the FIFO.
  - Data to write into the Delayed write register after the clear, should be begun with the address of the packet for delayed writing.
  - Both R_FIFO#1 and #0 should be returned to "0" after it is set to "1". Set "1" at least 300ns, and then return to "0".
  - Writing into the Delayed write register cannot be made when R_FIFO#0="1".

L3.2.3.2 R_SEQ#

- R_SEQ#1: This is a bit to clear the sequencer circuit for instantaneous writing. "1" has it clear.
  - The instantaneous writing/reading cannot be made when R_SEQ#1="1".
- R_SEQ#0: This is a bit to clear the sequencer circuit for delayed writing. "1" has it clear.
  - Both R_SEQ#1 and #0 should be returned to "0" after it is set to "1".
  - Like R_FIFO, Set "1" to R_SEQ for at least 300ns and then return to "0".
  - It is prohibited to start the sequencer when R_SEQ#0="1".

L3.2.4 Delay Recovery Function

When the sequence data FIFO becomes empty, the sequencer terminates the process, and then restarts the process at the moment of a subsequent data comes into the FIFO. The termination causes a time difference from absolute time. To compensate the difference from absolute time, the sequencer section is equipped with the "Delay recovery function".
The Delay recovery function always compares the "Absolute time" with "Sequence data processing time", and a delay from the absolute time occurs, the function recovers the delay.

The Intermediate register #55 has a bit to turn on and off the Delay recovery functions.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#55	W/R	SV_MUTE		SV_CHV	SV_PAN	MVSEL	NOP2E	FINT	DADJT

DADJT : This is a bit to select the Delay recovery function ON/OFF for the sequence FIFO.
"0" : Turns on the Delay recovery function (= valid).
"1" : Turn off the Delay recovery function (= invalid).

L3.2.5 NOP, NOP_2 setting

"NOP" and "NOP_2" are an abbreviation of "No Operation", the meaning is "do nothing".
Both register can not read

[#479=NOP] , [#478=NOP_2]

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 478	W	"0"	"0"	"0"	"0"	"0"	"0"	"0"
# 479	W	"0"	"0"	"0"	"0"	"0"	"0"	"0"

L3.2.5.1 NOP

The time that NOP is processed is approximately 1 / 96fs (= 217ns)

L3.2.5.2 NOP_2

NOP_2 is used for the time reservation of 2fs to 3fs.
The time that NOP_2 is processed is 2fs to 3fs (= 41.7µs to 62.5µs)

The operations of the device when FIFO becomes empty

The hardware stops the process of the sequencer.

- Reading from the delay FIFO is terminated. (The same as MA-3)
- Process of the absolute time counter and timer value down counter are terminated. (The process is stopped under this condition that is added to the conditions for count up/down.)

Stop sequencer time.

- Reading from the delay FIFO is stopped. (The same as MA-3)
- Sequencer time count up is stopped. (Resolution and time unit counters continue their operations.)
- Sequencer synchronizing timer is also stopped.

L3.2.5.3 NOP2E

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#55	W/R	SV_MUTE		SV_CHV	SV_PAN	MVSEL	NOP2E	FINT	DADJT

NOP2E: This is a bit for selecting valid / invalid of automatic NOP_2 issue and for selecting operation of RST bit.

"0": Automatic NOP_2 issue is disabled
RST bit should be made a level operation, and thus, should be returned to "0" after writing "1" to it.

"1": Automatic NOP_2 issue is enabled.
When a byte which includes a KeyOn bit is accessed, the hardware automatically secures the NOP_2 time. RST bit should be made an edge operation, and thus, it is not necessary to return the bit to "0".

The timing when NOP_2 automatic issue is inserted

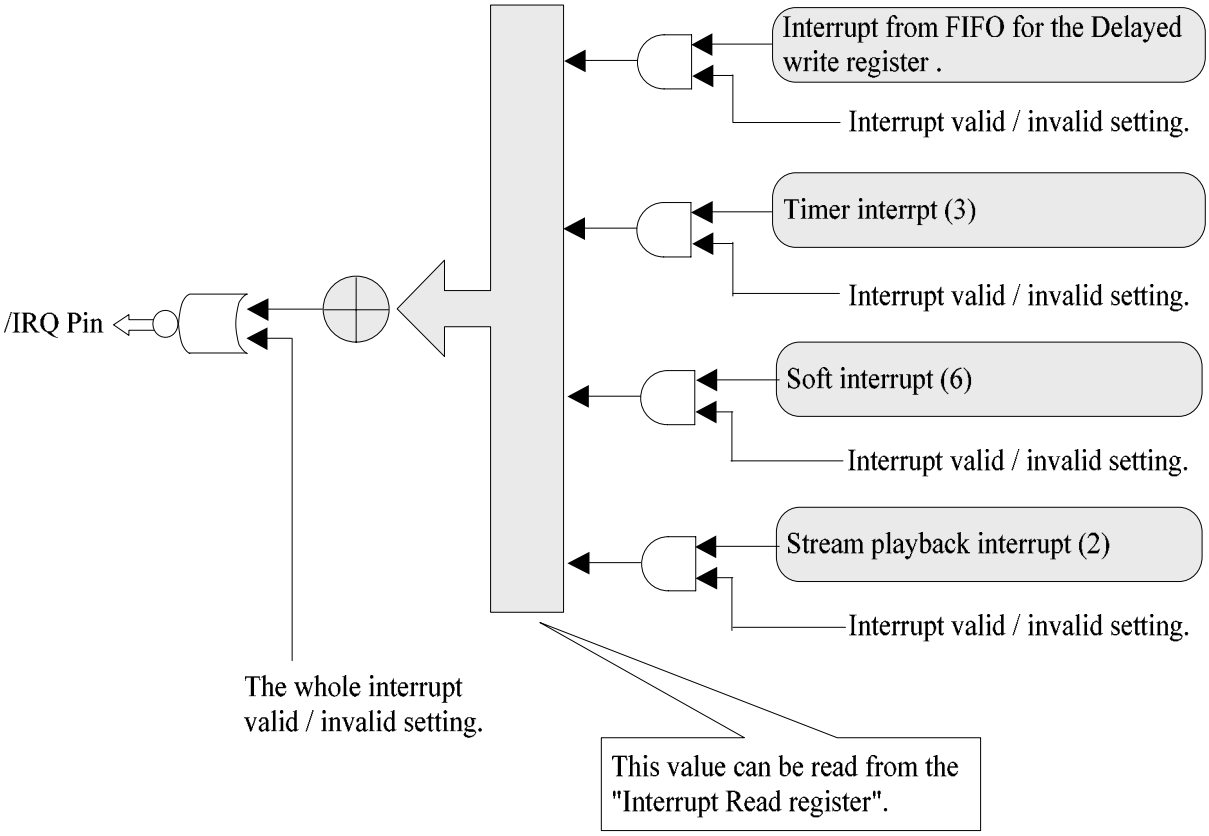
After the access is finished completely to the byte which includes KeyOn bit, the time for NOP_2 is secured automatically.

L3.3 Interrupt

Outline of Interrupt Functions

An interrupt is generated by any of the following four causes.

- Interrupt from FIFO (512-byte) for Delayed write register
  (Interrupt can be generated depending on the amount of data remaining in the FIFO.)
- Interrupt from timer (Interrupt can be generated from three timers independently.)
- Software interrupt (Interrupt can be generated from six software interrupts independently.)
- Interrupt from Stream playback (Interrupt can be generated from two Stream playbacks independently.)



Description of figures

The “Interrupt valid / invalid setting” can be made for individual interrupt causes.
The setting is made by the Intermediate Registers #17 and #18.
Each interrupt is logically ANDed with the “Interrupt valid / invalid setting” signal, and the resulting signal can be read from the “Interrupt flag register (Intermediate registers #0 and #16)”.
The signals which are read from the Interrupt flag registers, in the word, the signals logically ANDed are logically ORed together, are outputted to /IRQ pin.
When IRQ bit of Status flag register is “1”, /IRQ pin is always logic “H” (Inactive).

L3.3.1 Interrupt Valid / Invalid setting

This is a register to set interrupt valid / invalid.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#17	W/R	EFIFO	ETM#2	ETM#1	ETM#0	ESIRQ#1	ESIRQ#0	ESTM#1	ESTM#0
#18	W/R	"0"	"0"	ESIRQ#5	ESIRQ#4	ESIRQ#3	ESIRQ#2	"0"	"0"

L3.3.1.1 EFIFO

This bit sets an interrupt-permission from FIFO for delayed write. "0" sets indicate the interrupt is invalid, and "1" sets indicate the interrupt is valid.

L3.3.1.2 ETM#

This bit sets a timer * interrupt-permission. "0" sets the interrupt is invalid, and "1" sets interrupt is valid. (*Represents a numeral from 0 to 2.)

L3.3.1.3 ESIRQ#

This bit sets the Software interrupt # * interrupt-permission. "0" sets the interrupt is invalid, and "1" sets the interrupt is valid. (*Represents a numeral from 0 to 5.)

L3.3.1.4 ESTM#

This bit sets the Stream playback * interrupt-permission. ("0" sets the interrupt is invalid, and "1" sets the interrupt is valid. (*Represents a numeral of 0 or 1.)

L3.3.2 Interrupt Flag

This is an Interrupt flag status register. It is assigned in the Intermediate registers #0 and #16.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	W/R	FIFO	TM#2	TM#1	TM#0	SIRQ#1	SIRQ#0	STM#1	STM#0
#16	W/R	"0"	"0"	SIRQ#5	SIRQ#4	SIRQ#3	SIRQ#2	"0"	"0"

For every bits, interrupt is cleared by writing "1" into the bit at the time of an interrupt.

L3.3.2.1 FIFO

This is an Interrupt flag from FIFO for delayed write. "0" indicates no interrupt is being generated, and "1" indicates an interrupt is generated.

L3.3.2.2 TM#

This is an Interrupt flag from timer *. "0" indicates no interrupt is being generated, and "1" indicates an interrupt is generated. (* represents a numeral from 0 to 2.)

L3.3.2.3 SIRQ#

This is an Interrupt flag from the Software interrupt # *. "0" indicates no interrupt is being generated, and "1" indicates an interrupt is generated. (* represents a numeral from 0 to 5.)

L3.3.2.4 STM#

This is an Interrupt flag from the Stream playback *. "0" indicates no interrupt is being generated, and "1" indicates an interrupt is generated. (* represents a numeral of 0 or 1.)

L3.3.3 Whole Interrupt Valid / Invalid setting

This is a register for setting whole interrupt valid / invalid. It is set with IRQ bit of the Status flag register.

Default 8'h00

A_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	W	IRQ	VALID_R	B_ADR					

IRQ: This is a bit to permit whole interrupt output.
"1" permits the interrupt output. "0" fixes /IRQ pin to logic "H".

L3.3.4 Interrupt from FIFO for Delayed Write Register

An interrupt can be outputted depending on the amount of data remaining in FIFO for Delayed write register. It is set with the Intermediate register #37.

Default8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#37	W/R	"0"	"0"	"0"	"0"	"0"	IRQ POINT		

L3.3.4.1 IRQ POINT

This is a bit to designate an interrupt position of FIFO for delayed write.

0: Interrupt is generated when the FIFO becomes Empty.
1: Interrupt is generated when the amount of data remaining in the FIFO becomes 64 bytes or less.
2: Interrupt is generated when the amount of data remaining in the FIFO becomes 128 bytes or less.
3: Interrupt is generated when the amount of data remaining in the FIFO becomes 192 bytes or less.
4: Interrupt is generated when the amount of data remaining in the FIFO becomes 256 bytes or less.
5: Interrupt is generated when the amount of data remaining in the FIFO becomes 320 bytes or less.
6: Interrupt is generated when the amount of data remaining in the FIFO becomes 384 bytes or less.
7: Interrupt is generated when the amount of data remaining in the FIFO becomes 448 bytes or less.

It is necessary to set an EFIFO bit of the Intermediate register #17 to "1" (interrupt valid) for generating an interrupt.

L3.3.4.2 FINT

As for an interrupt from FIFO, it is possible to select a level sense or an edge sense.
The setting is made with FINT of Intermediate register #55.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#55	W/R	SV_MUTE	SV_CHV	SV_PAN	MVSEL	NOP2E		FINT	DADJT

"0" selects a level sense that is the same as MA-3. "1" selects an edge sense.

Description of level sense and edge sense

Level sense: When the amount of data remaining in FIFO for delayed write is less than the number of bytes set in the IRQ POINT, even if clear of Interrupt flag (FIFO bit of Intermediate register #0) is attempted, the flag is not cleared and /IRQ pin is stayed at "L" level.

Edge sense: Attempting to clear Interrupt flag clears the flag and sets /IRQ pin to "H" level even when the amount of data remaining in FIFO for delayed write is less than the number of bytes set in the IRQ POINT.

L3.3.5 Interrupt from Timer

There are three timers which can be operated independently.
The timers can be counted down from a value set in the TIMER # of the Intermediate registers #47, #49, and #51, and an interrupt can be generated at the time the count value becomes “0”.
For more detail about timer, refer to “L3.12 Timer“.

L3.3.6 Software Interrupt

The Control registers #470 to #475 includes a register that is for generating Software interrupt.

Default 7’h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 470	W/R	RAM #0						
# 471	W/R	RAM #1						
# 472	W/R	RAM #2						
# 473	W/R	RAM #3						
# 474	W/R	RAM #4						
# 475	W/R	RAM #5						

L3.3.6.1 Software interrupt setup

An interrupt is generated when data is written into the Control register.
It can be operated with writing from any of the registers, the Instantaneous write register or the Delayed write register.
Interrupt valid / invalid is set with ESIRQ#5 to ESIRQ#0 bits of the Intermediate registers #17 and #18.
The Interrupt flag registers are SIRQ#5 to SIRQ#0 bits of the Intermediate registers #0 and #16.

L3.3.6.2 Software interrupt setup readout

The values set in the Control registers #470 to #475 (Software interrupt setting) can be read from the Intermediate registers #19 to #24. This is a Read Only register.

Default 8’h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#19	R	“0”	RAM#0						
#20	R	“0”	RAM#1						
#21	R	“0”	RAM#2						
#22	R	“0”	RAM#3						
#23	R	“0”	RAM#4						
#24	R	“0”	RAM#5						

The correspondence between Control register numbers and Intermediate register numbers are as follows.

- Control register#470 – Intermediate register#19
- Control register#471 – Intermediate register#20
- Control register#472 – Intermediate register#21
- Control register#473 – Intermediate register#22
- Control register#474 – Intermediate register#23
- Control register#475 – Intermediate register#24

L3.3.7 Stream Playback Interrupt

It is the register to perform an interrupt setup at the time of stream playback. Specify an interrupt generation point setup, and buffer size to be used. Interrupt valid / invalid is set with ESTM#0 and ESTM#1 bits of the Intermediate register #17. The Interrupt flag registers are STM#0 and STM#1 bits of the Intermediate register #0.

Default 8'h10

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#57	W/R	"0"	"0"	BUF SIZE		"0"	"0"	STM IRQPOINT	

L3.3.7.1 STM IRQPOINT

Selection of interrupt generation points is set.
An interrupt is generated when the number of bytes of waveform buffer becomes the following state.

0 : An interrupt is generated every time when (waveform buffer size designated by SIZE bit×1/4) is read to playback.

1 : An interrupt is generated every time when (waveform buffer size designated by SIZE bit×1/2) is read to playback.

2 : An interrupt is generated every time when (waveform buffer size designated by SIZE bit×3/4) is read to playback.

3 : An interrupt is generated every time when (waveform buffer size designated by SIZE bit) is read to play back.

For example, when IRQ POINT= "0" and SIZE= "1" (=1024 byte) are specified; an interrupt is generated every time when the data for 256 bytes is consumed.

L3.3.7.2 BUF SIZE

The number of bytes of a waveform buffer is set.
It designates the buffer size of SRAM that is used for Stream playback.

0 : 512 bytes

1 : 1024 bytes (default)

2 : 2048 bytes

3 : Set up is prohibited.

L3.4 Hybrid Synthesizer (Synthesizer Mode Selection)

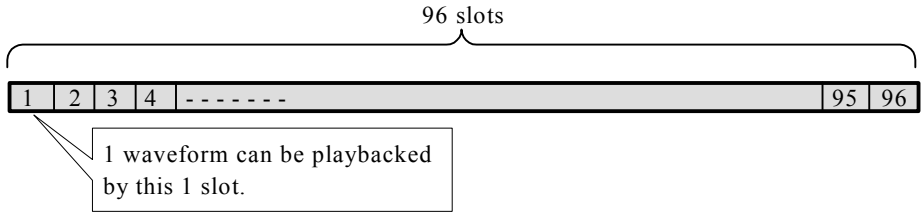
What is Hybrid Synthesizer?

This is a synthesizer that has several kinds of playback functions in one synthesizer core.
It has the following five different synthesizer functions.

- FM synthesizer
- WT synthesizer
- Stream playback
- HV synthesizer
- AL synthesizer

Hardware's Composition of Synthesizer

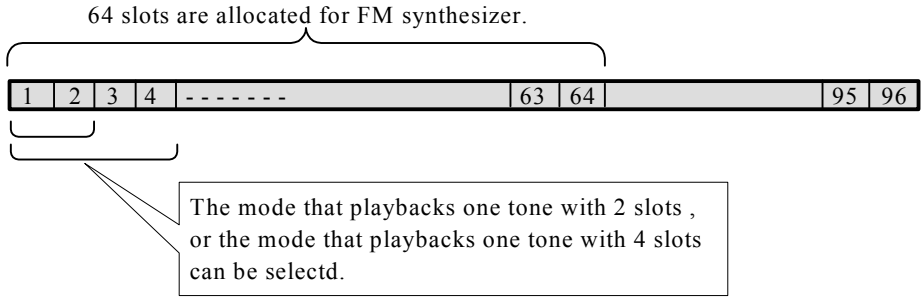
As hardware, it has a function to be able to play back 96 waveforms simultaneously.
A unit to play back one waveform is called a "Slot".
In other word, it has 96 slots as hardware.



Relationship between each Synthesizer Function and Slot

In the case of the FM synthesize

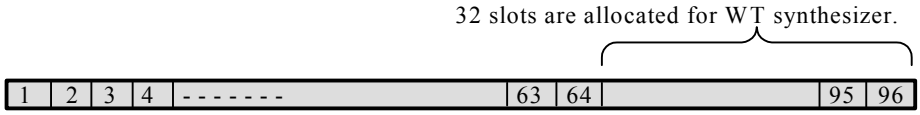
64 slots are allocated for FM synthesizer.
Playback one tone of FM requires 2 slots or 4 slots.
In other word, in the mode of which one tone is played back by using 2 slots, the number of simultaneously generated voices is 32 tones, and in the mode of which one voice is played back by using 4 slots, the number of simultaneously generated voices is 16 tones.
(However, 2 slots and 4 slots cannot be mixed. Either of 16 voices or 32 tones is used.)



A mode of which one tone is played back by using 2 slots is called “2 operator modes”.
A mode of which one tone is played back by using 4 slots is called “4 operator modes”.

In the case of the WT synthesizer

WT is able to playback one tone with one slot.
32 slots are allocated for WT synthesizer.
In other word, the maximum number of simultaneously generable voices becomes 32 tones.



In the case of HV playback

As for HV playback, by using nine slots one tone (maximum) is played back.
The slots for HV playback are common to the slots of WT section.
If the HV playback is performed as one sound, the generable sound of WT synthesizer is decreased by nine.
In the 32 slots of WT synthesizer (0 to 31), the slots common to HV synthesizer is 16 to 21slots.
Thus, specified slot numbers are allocated to HV.

In the case of Stream playback

For Stream playback, one tone is played back by using one slot, and up to two tones can be generated simultaneously.
The slots for Stream playback are common to the slots for WT section.
If Stream Playback is performed as one tone, the generable sound of Stream playback is decreased by one.
In the 32 slots of WT synthesizer (0 to 31), the slots common to Stream playback is 25 and 26.
Thus, specified slot numbers are allocated to Stream playback.

In the case of AL synthesizer

There is no slot for AL synthesizer.
One tone of FM or WT can be inputted to low pass filter.

L3.4.1 Mode Selection

The following three settings are available.

- Selection of 2 operator mode or 4 operator mode for FM synthesizer
- Selection of whether to use #16 to #24 of WT synthesizer as a HV synthesizer.
- Selection of whether to use #25 and #26 of WT synthesizer as Stream playback section.

L3.4.1.1 FM Mode Selection

FM synthesizer has the following two modes.
Which to choose is set by using FMMODE bit of the Intermediate register #56.

- A mode in which the maximum number of simultaneously generated sounds is 16 tones with FM 4 OP voices. This is called 4 operator modes.
- A mode in which the maximum number of simultaneously generated sounds is 32 tones with FM 2 OP voices. This is called 2 operator modes.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#56	W/R	"0"	"0"	"0"	"0"	"0"	HVMODE	STMMODE	FMMODE

FMMODE: This is the bit for selection of an FM synthesizer mode.

"0": Enables 4 operator modes in which the maximum number of simultaneously generated sounds is 16 tones with FM 4 OP voices.

"1": Enables 2 operator modes which the maximum number of simultaneously generated sounds is 32 tones with FM 2 OP voices.

L3.4.1.2 HV Mode Selection

It is possible to switch voice #16 to #24 of WT synthesizer to HV synthesizer and use.

HVMODE: "0": Voice #16 to #24 of WT synthesizer operates as WT synthesizer.
"1": Voice #16 to #24 of WT synthesizer operates as HV synthesizer.

L3.4.1.3 Stream Playback Mode Selection

It is possible to switch voice #25 and #26 of WT synthesizer to Stream playback and use.

STMMODE: "0": Voice #25 and #26 of WT synthesizer operates as WT synthesizer.
"1": Voice #25 and #26 of WT synthesizer operates as Stream playback.

Change of Setup value of FMMODE bit during voice generation is prohibited.
Even if FMMODE is switched after the voice setup (Voice Adr. Setup), in some case, it is not generated normally.

L3.5 FM Synthesizer

The functional details about FM synthesizer are divided into the following five elements and explained.

- L 3.5.1 The function which related to FM Sound Generatro
- L 3.5.2 The function which related to PG (Phase Generator)
- L 3.5.3 The function which related to EG (Envelope Generator)
- L 3.5.4 The function which related to FM algorithm.
- L 3.5.5 Others

Description of each Parameter

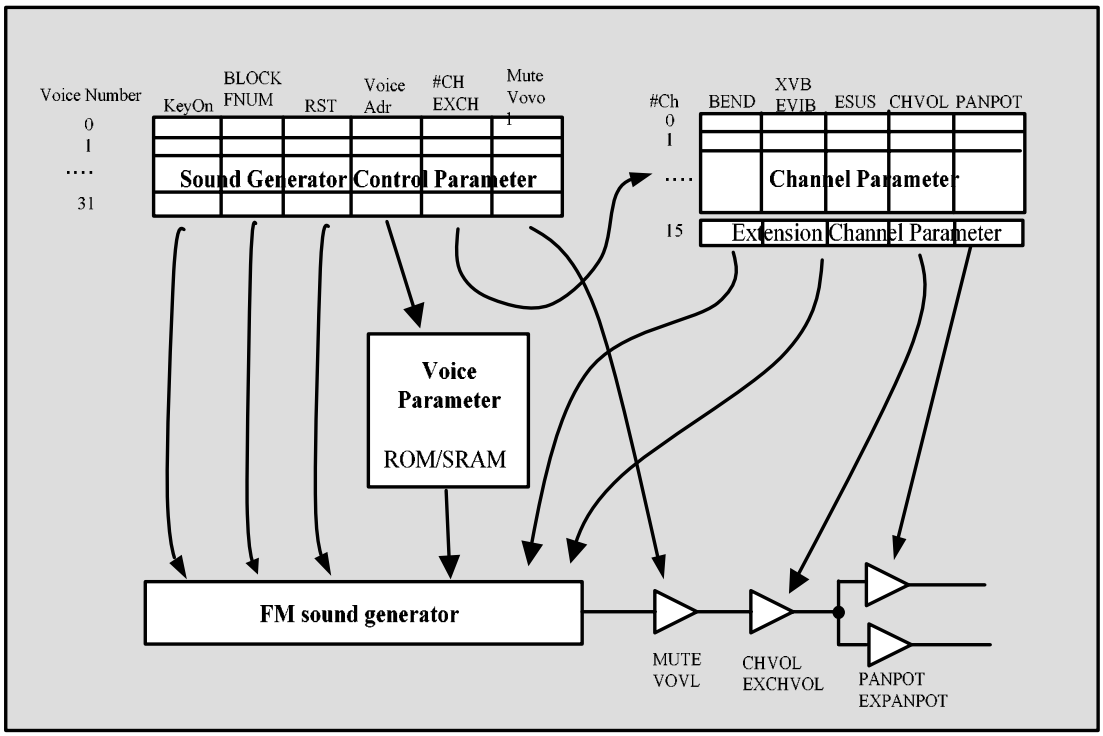
The following figure shows the connections of various parameters that are used to playback one FM tone. The hardware that generates one FM tone is called “FM Sound Generator”. The FM sound generator is controlled by various parameters to produce FM sound. There are the following three parameters to control the FM sound generator.

- Sound generator control parameters

  →It is in the Control register. Parameters such as ON/OFF of sound generation and tempo exist.
- Voice parameters

  →It is in the ROM or SRAM and indicates voice data such as piano or violin.
- Channel parameters and expanded channel parameters

  →They are channel parameters designated by #CH bit and EXCH bit included in the Sound generator control parameters. The channel parameters are composed of pitch bend, vibrato control, and volume control.



L3.5.1 Function Related to FM Sound Generator

This is a register to control FM sound generator.
The control registers #0 to #95 correspond to FM sound generator #0 to #15, and the Control Registers #272 to #367 correspond to FM sound generators #16 to #31 respectively.
FM sound generators #16 to #31 become valid only when FMMODE bit of the Intermediate Register #56 is "1".
For more details, refer to the "L3.4.1.1 FM Mode Selection".

The correspondence table of the Control Register and FM sound generator number

Control register	FM sound generator number	Control register	FM sound generator number
#0 ~ #5	0	#272 ~ #277	16
#6 ~ #11	1	#278 ~ #283	17
#12 ~ #17	2	#284 ~ #289	18
#18 ~ #23	3	#290 ~ #295	19
#24 ~ #29	4	#296 ~ #301	20
#30 ~ #35	5	#302 ~ #307	21
#36 ~ #41	6	#308 ~ #313	22
#42 ~ #47	7	#314 ~ #319	23
#48 ~ #53	8	#320 ~ #325	24
#54 ~ #59	9	#326 ~ #331	25
#60 ~ #65	10	#332 ~ #337	26
#66 ~ #71	11	#338 ~ #343	27
#72 ~ #77	12	#344 ~ #349	28
#78 ~ #83	13	#350 ~ #355	29
#84 ~ #89	14	#356 ~ #361	30
#90 ~ #95	15	#362 ~ #367	31

Control register for FM sound generator #0

[C_Address #0 ~ #95, #272 ~ #367] Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 0	W/R	Voice Adr [14:8]						
# 1	W/R	Voice Adr [7:1]						
# 2	W/R	VOVOL					MTRON	LEDON
# 3	W/R	EXCH	BLOCK			FNUM (H)		
# 4	W/R	FNUM (L)						
# 5	W/R	KeyOn	MUTE	RST	#CH			

L3.5.1.1 VoiceAdr

Addresses of memories (ROM/SRAM) in which voice parameters are stored are set.
By setting VoiceAdr, the voices of the Sound generator are determined.
Since it is necessary to place the voice data on the 2-byte boundary, set high-order 14 bits of the memory address (15'h0000 to 15'h5FFF).
They become valid at the time low-order bits are written. They must be processed as a pair (continuously).
Make sure to transfer both high-order bits and low-order bits as one packet.
When they are not transferred as one packet, wrong VoiceAdr may be set.

Notes for Voice Adr settings

At the time of the VoiceAdr settings, be sure to perform the operation in the state of which the pronunciation of the corresponding sound generation is stopped completely. It is recommended that performing a change of VoiceAdr after an initialization of EG (Envelope Generator) with RST bit.

About the pair (Continuous) process

The pair (continuous) process fails when data are written into a different address not for the low-order bits and then the data are written into the address for low-order bits, after data are written into only high-order bits of a register of which pair processing are needed. In the following case, all of them are acceptable because the data are written as a pair.
The following example explains the writing of data into the Control register #0 VoiceAdr[14:8] and the Control register #1 VoiceAdr[7:1] as a pair.

- When Address section and Data section of the packet for writing are inputted to instantaneous path or delayed path in the order as shown below;
  - Adr #0, Data#0, Data #1
  - Adr #0, Data#0, Adr #1, Data#1 are also acceptable.
- When Write/Read of the Intermediate register (except instantaneous / delayed write) occurs in the middle of the process;
  The following case uses an instantaneous path for explanation, which is applicable also to the case of delay path
  - Instantaneous Adr #0, Instantaneous Data#0, Intermediate R/W, Instantaneous Adr #1, Instantaneous Data#1
- When writing of another path occurs in the middle of the process;
  The following case uses instantaneous path for explanation, which is applicable also to the case of delay path
  - Instantaneous Adr #0, Instantaneous Data#0, delay Adr #a, delay Data#a, Instantaneous Adr #1, Instantaneous Data#1
    (#0 can be used in place of #a.)

Example of VoiceAdr setting

For example, when setting VoiceAdr to 0800h, 14 bits are set into Voice Adr [14:1] register excluding one bit of LSB. The setting value becomes as described below.

7'b000 1000 to VoiceAdr[14:8]
7'b000 0000 to VoiceAdr [7:1]

L3.5.1.2 VOVOL

This is the volume setting for each Sound generator. VOVOL does not have interpolation function.
For more details, refer to the “L3.10 Volume Functions”.

L3.5.1.3 MTRON

“1” indicates that the voice has MTR synchronization. For more details, refer to the “L3.11 LED, Vibrator control”.

L3.5.1.4 LEDON

“1” indicates that the voice has LED synchronization. For more details, refer to the “L3.11 LED, Vibrator control”.

L3.5.1.5 EXCH

“0” uses the channel parameters of the Control registers #192 to #271
“1” uses the expanded channel parameters of the Control registers #483 to #487.

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 483	W/R	EXCHVOL					“0”	DRCT
# 484	W/R	EXPANPOT					“0”	“0”
# 485	W/R	“0”	“0”	EXESUS	“0”	EXXVB		
# 486	W/R	“0”	“0”	EXINT		EXFRAC(H)		
# 487	W/R	EXFRAC(L)						“0”

The number of channels of MA-3 is 16, but it is expanded to 17 for MA-5.
“EXCH” bit is assigned to each Sound generator setting registers, and the Sound generator of which EXCH bit is set to “1” uses the expanded channel parameters of the Control registers #483 to #487.
As for expanded channel setting section, only EXCHVOL supports for DRCT bit (For setting interpolation valid / invalid). EXPANPOT does not have interpolation function.

L3.5.1.6 BLOCK

This bit designates an octave. (0 to 7)
For more details of the operations, refer to the “L3.5.2 Function Related to PG (Phase Generator)”.

L3.5.1.7 FNUM

Set frequency information for one octave.
For more details of the operations, refer to the “L3.5.2 Function Related to PG (Phase Generator)”.
It becomes valid at the time FNUM (L) has been written. Be sure to transfer BLOCK, FNUM (H), and FNUM (L) as one packet.

L3.5.1.8 KeyOn

“1” enables Keyon (voice generation), and “0” enables Keyoff (voice generation control disabled).

L3.5.1.9 MUTE

This is the mute that is set for each Sound generator.
For more details, refer to the “L3.10 Volume Functions”.

L3.5.1.10 RST

This is a bit for forced silencing.
For more details of the operations, refer to the “L3.5.3 Function Related to EG (Envelope Generator)”.

L3.5.1.11 #CH

It designates a channel parameter numbers which associate with FM sound generator.

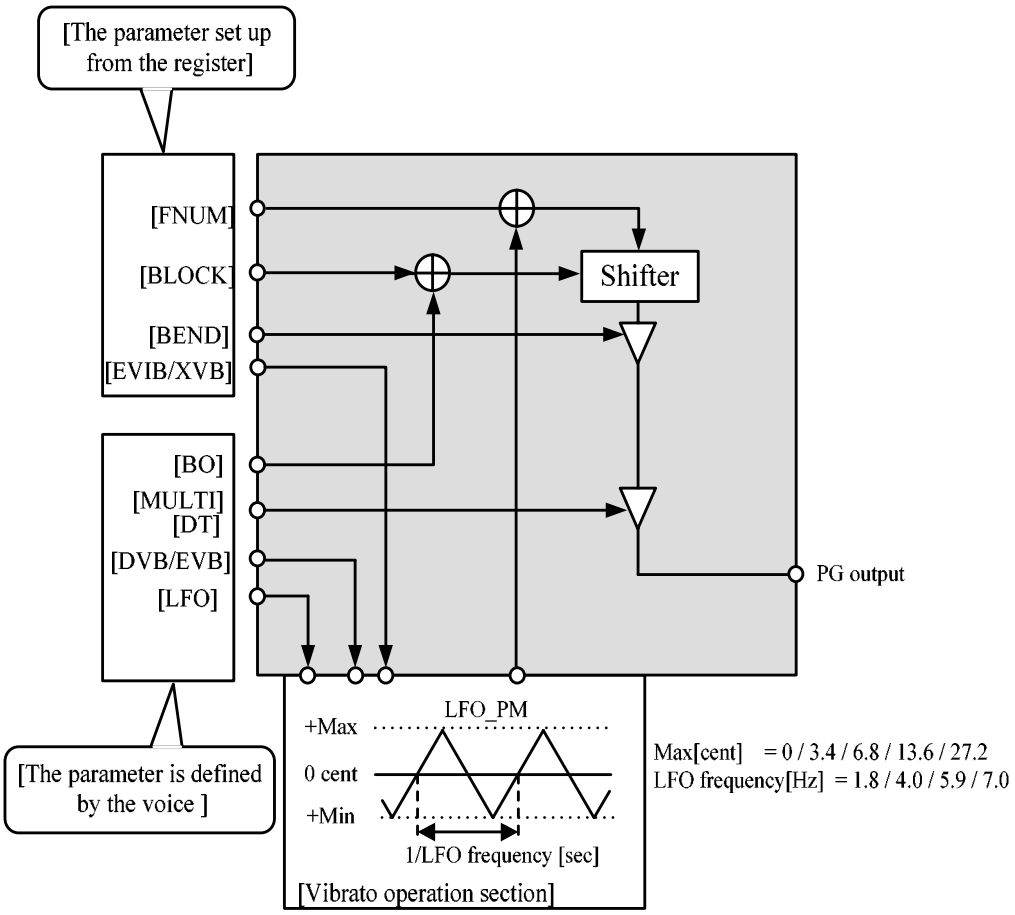
L3.5.2 Function Related to PG (Phase Generator)

Parameters that control phase are classified mainly into two types.

- Parameters which are set-up from registers.
- Parameters which is defined by voice.

This section gives an outline of parameters.

Fundamental configuration of PG



BLOCK	This is a parameter to sets an octave. Doubling a frequency increase the voice by one octave, and halving a frequency reduces a voice by one octave. For such occasion, it is realized by a shifter.
FNUM	Parameter to set a fine pitch in one octave (do-re-mi etc.).
BEND	Parameter to multiply a frequency by a factor of 0 to 3.999.
EVIB, XVB DVB, EVB, LFO	Parameter to control a vibrato.
BO	Stands for the “Basic Octave”, fundamental octave information hold on voices.
MULTI	Parameter to multiply a frequency by integer numbers.
DT	Parameter which stands for Detune, and be used for shifting a frequency slightly.

L3.5.2.1 BLOCK

This is one of the sound generator control parameters which designate a octave.
As concerns the relationship between the setting value and outputting frequency, refer to the following FNUM.
This bit becomes valid at the time FNUM (L) has been written.
Make sure to transfer BLOCK, EXCH, FNUM (H) and FNUM (L) as one packet.
Wrong FNUM may be set if they are not transferred as one packet.

L3.5.2.2 FNUM

This is one of Sound generator control parameters that set the frequency information for one octave.
D2 to D0 bits of FNUM (H) and D6 to D0 bits of FNUM(L) constitute FNUM that is used by the following formula. The Sound generator fundamental frequency f_Voice = FNUM × (2^(BLOCK - 1)) / (2^19) × fs × BO × BEND [Hz]

fs [Hz]: sampling frequency

BO: Fundamental octave that is set with voice parameters (Refer to the "L3.5.2.7 BO"

BEND: Pitch bend that is set with channel parameters (Refer to the "L3.5.2.3 INT, FRAC")

This bit becomes valid at the time FNUM (L) has been written. Make sure to transfer BLOCK, FNUM(H), and FNUM(L) as one packet. Wrong FNUM may be set if they are not transferred as one packet.

L3.5.2.3 INT, FRAC

This is for the setting of pitch bend. It is a channel parameter that is assigned to the Control registers #240 to #271.
This is a register that set a multiple for frequency of generated voices (phase).
The register consists of 11 bits in total, including 2 bits of INT section (integer section) and 9 bits of FRAC section (fractional section).

Default 7'h08 / 7'h00 (INT=2'b01,FRAC=9'h000)

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 240	W/R	"0"	"0"	INT #0		FRAC(H) #0		
# 241	W/R	FRAC (L) #0						"0"
▪ ▪ ▪ ▪ ▪ ▪								
# 270	W/R	"0"	"0"	INT #15		FRAC(H) #15		
# 271	W/R	FRAC (L) #15						"0"

- INT: Integer part of a multiple for frequency of generated voices (0 to 3)
- FRAC: Fractional part of a multiple for frequency of generated voices (9'h1ff to 9'h000)

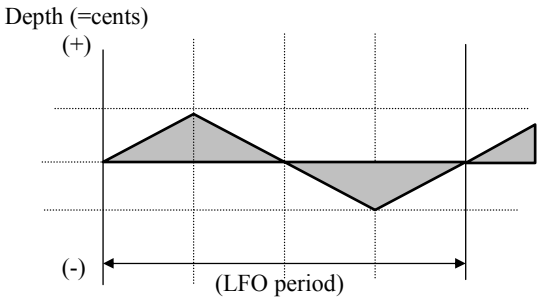
Example; (INT, FRAC)
(2'b10, 9'h000) = 2.0
(2'b01, 9'h000) = 1.0
(2'b00, 9'h1FF) = 0.999
(2'b00, 9'h100) = 0.5

Be sure to transfer INT, FRAC (H) and FRAC (L) as one packet.
The 9 bits of FRAC becomes valid at the time of the lower part of FRAC (L) is written.
Wrong FRAC may be set if they are not transferred as one packet.
As for HV synthesizer, phase is fluctuated by pitch-bend, but formant frequency is not fluctuated.

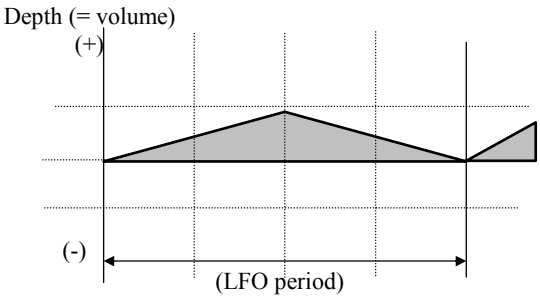
L3.5.2.4 DVB

DVB is a parameter which controls the depth of vibrato, and it exits in FM voice parameter.
For more details about Map of FM voice parameter, refer to the “L3.1.4 SRAM“.

- DVB= 0 : 3.4 cents
- DVB= 1 : 6.7 cents
- DVB= 2 : 13.5 cents
- DVB= 3 : 26.8 cents



Vibrato modulation



AM modulation

L3.5.2.5 EVB

This is a bit that designates a vibrato modulation. It is a FM voice parameter.
When this bit is set to “1”, vibrato modulation can be applied to a corresponding operator.
The vibrato modulation is applied when the both conditions, (EVB =“1”) and (XVB = other than 0) are met.
The modulating frequency is determined with the period that is set with LFO, and depth of the modulation is determined with DVB that is described later in this document.

L3.5.2.6 XVB, EVIB

These are channel parameters for setting vibrato. They are assigned in the Control Register #224 to #239.

Default 8'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 224 ~ #239	W/R	EVIB#0~ EVIB#15	"0"	ESUS#0~ ESUS#15	"0"	XVB#0 ~ XVB#15		

XVB is a bit to designate the depth of vibrato.
EVIB is a bit for selecting the "Relative designation" and the "Absolute designation".
EVIB= "0" indicates the relative designation, "1" indicates the absolute designation.
The Relative Designation is a method that adds a control to DVB / EVB setting that defined in the voice parameters.
The Absolute Designation is a method that neglects the setting defined in the voice parameters to control only with the channel parameters. In the case of MA-3, only the Relative Designation is used; however, in the case of MA-5, the Absolute Designation is added to the specifications.

In the case of Relative Designation (MA-3 compatible)

It changes a configuration of DVB/EVB. However, the configuration is performed in a range of DVB (0 to 3).

XVB	Depth of vibrato
0	Vibrato is off
1	DVB value is used as it is.
2, 3	DVB value +1
4, 5	DVB value +2
6, 7	DVB value +3

In the case of Absolute Designation

DVB/EVB setting is ignored, and the depth of vibrato is determined only with the channel parameters.

XVB	Depth of vibrato
0 ~ 2	Vibrato is off
3	3.4 cent
4	6.7 cent
5	13.5 cent
6	26.8 cent
7	53.6 cent

L3.5.2.7 BO

This is a setting value of a fundamental octave for FM voice parameter.
A formula of fundamental oscillation frequency is given by the following.
f_Voice = FNUM × (2^(BLOCK - 1)) / (2^19) × fs × BO × BEND [Hz]
The value of "BO" is as shown below.

0 : 2
1 : 1
2 : 1 / 2
3 : 1/ 4

L3.5.2.8 DT

It designates “Detune”, and it is a FM voice parameter.
The oscillation frequency of an operator can be shifted slightly by the detune functions.

DETUNE coefficient

DETUNE coefficient is obtained from 3-bits of BLOCK+BO, high-order 4-bits of FNUM, and 2-bits of DT[1:0].
(However, the following conversion value is used for BO part of BLOCK+BO.
BO= “0” : +1, BO= “1” : 0, BO= “2”:-1, BO= “3” : -2)

DT[2] (MSB) is a sign bit, which designates polarity of frequency change.
No effect is applied when DT[2:0] = “0”.
Detune frequency is affected by MULTI setting. When MULTI= 2, the values shown in the table of “L5.1.4 FM Synthesizer Detune Correspondence Table“ are doubled.

L3.5.2.9 MULTI

It designates the multiple for frequency, and it is a FM voice parameter.

MULTI	0	1	2	3	4	5	6	7	8	9	10, 11	12, 13	14, 15
Multiple	1/2	1	2	3	4	5	6	7	8	9	10	12	15

Operator oscillation frequency f_op = f_Voice × MULTI × (LFO_PM) [Hz]

L3.5.2.10 EXINT, EXFRAC

This is a pitch bend setup of the extended channel parameter.
It is assigned in the Control register #486, 487.
The operation specification is same as “L3.5.2.3 INT, FRAC“.

Default : 7’h08 / 7’h00 (INT=2’b01, FRAC=9’h000)

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 486	W/R	“0”	“0”	EXINT		EXFRAC(H)		
# 487	W/R	EXFRAC (L)						“0”

EXINT : It is an integer part to set up multiple of sound generation frequency. (0 to 3)
EXFRAC : It is a decimal part to set up multiple of sound generation frequency. (9’h1ff to 9’h000)

L3.5.2.11 EXXVB

This is a vibrato setup for the extended channel parameter.

Default : 8’h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 485	W/R	“0”	“0”	EXESUS	“0”	EXXVB		

The operation specification is same as “L3.5.2.6 XVB, EVIB“. However, it has no function corresponding to EVIB.

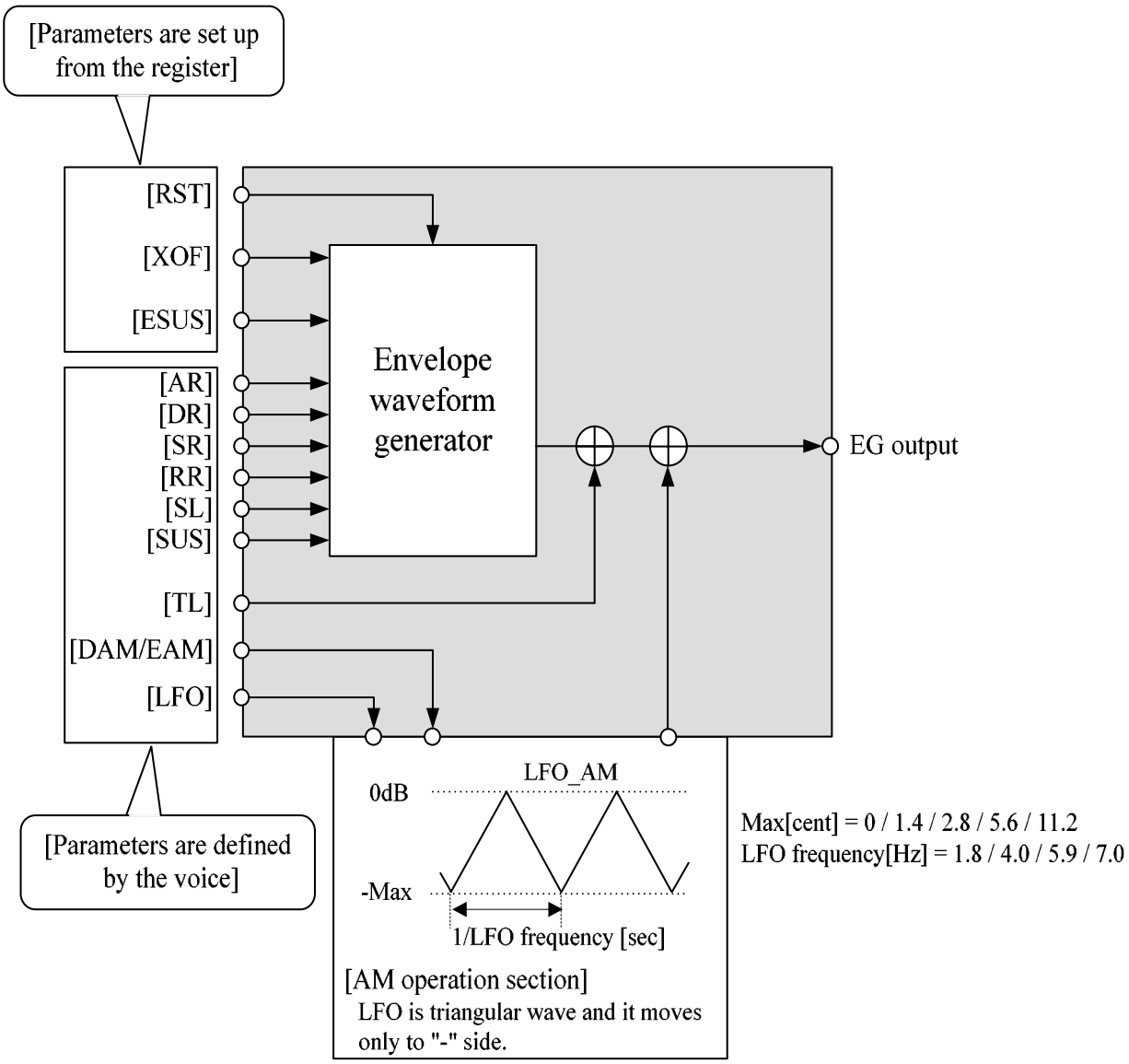
L3.5.3 Function Related to EG (Envelope Generator)

Fundamental Configuration of EG

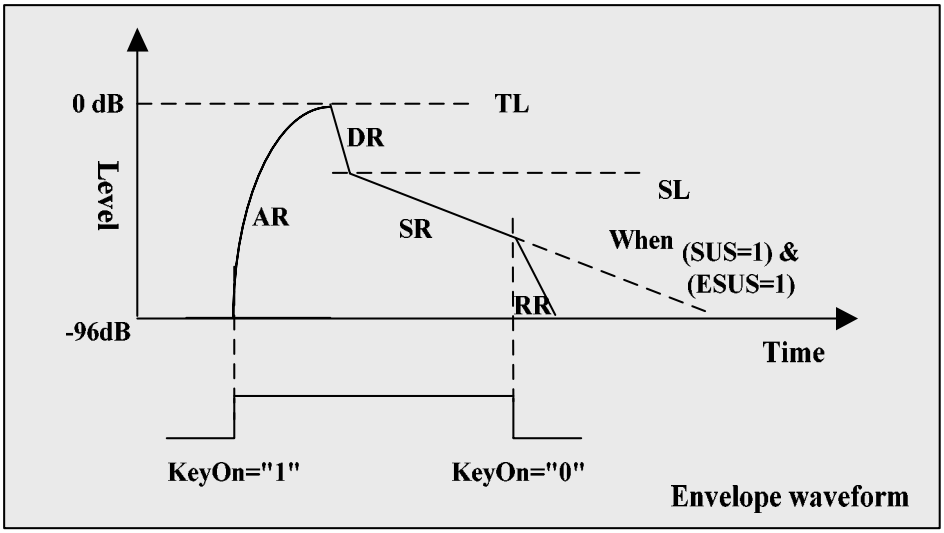
The fundamental configuration of EG is as shown below. It is classified mainly into the following two types.

– Parameters are set up by registers

– Parameters are defined by voices



From the above figure, the results of the output become as described below.



At KeyOn, EG goes up exponentially at the rate of AR from the current value (-96dB immediately after initialization) to the maximum value TL, and then it is changed to DR.
During DR, it goes down at the rate of the constant-multiple attenuation (log-linear decay) to SL, and then the rate is changed to the rate of SR and it goes down log-linearly.
At KeyOff, it is changed to the release state. The rate is same as the rate in SR when in (SUS=1)&(ESUS=1), or becomes log-linear decay of RR when in other SUS/ESUS combination.
Voice that has entered released state is changed to release rate that is obtained by ESUS change during voice generation.
RST bit is provided for realizing forced mute.

It supports XOF that neglects KeyOff. When XOF=1, the change of state with KeyOff does not occur.
The below table describes the outline about each parameters.

Each parameter name and the number of bits which control EG

AR	Attack Rate	4 bits
DR	Decay Rate	4 bits
SR	Sustain Rate	4 bits (When SR = 0, present level is maintained.)
RR	Release Rate	4 bits
TL	Total Level	6 bits
SL	Sustain Level	4 bits
SUS	Designation of rate-changeable after KeyOff	1 bit
ESUS	Designation of sustain	1 bit
DAM	LFO depth	2 bits
EAM	LFO switch	1 bit
RST	EG value reset	1 bit
XOF	KeyOff neglect	1 bit

L3.5.3.1 AR

AR stands for “Attack Rate”, and it sets the time from the moment which “KeyOn of FM Sound Generator” is set to “1” to the moment of 0 dB. It is a FM voice parameter. Only the attack rate changes exponentially.

L3.5.3.2 DR

DR stands for “Decay Rate”, and it sets the time from the “Attack Rate Terminate Point” to “SL Level”.
It is a FM voice parameter.

L3.5.3.3 SR

SR stands for “Sustain Rate”, and it sets the time from the “SL Level” to the moment of the “Silent Level” (-96dB).
It is a FM voice parameter.

L3.5.3.4 RR

RR stands for “Release Rate”, and it sets the time from “KeyOff” to the moment of the “Silent Level” (-96dB).
It is a FM voice parameter.

L3.5.3.5 SL

SL stands for “Sustain Level”. It is a FM voice parameter.
The relationship between the setting value of D3 to D0 bits and the level is represented with “(-24 × D3) + (-12 × D2) + (-6 × D1) + (-3 × D0) [dB]”.
The sustain level is “-93dB” when all of D3 to D0 bits are “1”.

L3.5.3.6 SUS

This is a bit for selecting the rate after KeyOff (KeyOn=“0”). It is a FM voice parameter.
Although KeyOn=“0” shifts the rate to a release rate, SR continues when both SUS and ESUS are “1”. For other cases, RR is enabled.
The voice generation during release can be changed by changing ESUS setting.
(ESUS is a channel parameter that is assigned to the Control registers #224 to #239.)

L3.5.3.7 ESUS

Default : 8'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 224 ~ #239	W/R	EVIB#0 ~ EVIB#15	"0"	ESUS # 0 ~ ESUS#15	"0"	XVB#0 ~ XVB #15		

This is the bit for designating Sustain to be set for each channel.
"0" turns off Sustain. "1" turns on Sustain.

L3.5.3.8 TL

TL stands for "Total Level" that designates the attenuation for the envelope waveform to control the volume or modulation factor.
The relationship between D7 to D2 bits and the amount of attenuation is given by the following formula.
TL = (24 × D7) + (12 × D6) + (6 × D5) + (3 × D4) + (1.5 × D3) + (0.75 × D2) [dB]
The total level is "47.25dB" when all of D7 to D2 bits are "1".

L3.5.3.9 XOF

It is a bit to make a control ignore KeyOff. It is a FM voice parameter.
When XOF=1, KeyOff does not cause any changes of state.

When changing voices from XOF="1" to XOF="0" as exactly the same type
When using it in NOP2E="0", be sure to set KeyOn to "1" after reserving time of 1 fs or more by NOP_2.
If it is performed without reserving a time, it may cause missing of voices of XOF=0.
As for NOP2, refer to "L3.2.5.3 NOP2E".

L3.5.3.10 DAM

It is a bit to set the depth of an AM modulation. It is a FM voice parameter.

0 : 1.3 dB
1 : 2.8 dB
2 : 5.8 dB
3 : 11.8 dB

L3.5.3.11 EAM

It is a bit to designate a AM modulation. It is a FM voice parameter.
When this bit is set to "1", AM modulation can be applied to the corresponding operator.
The modulation frequency is determined by the period set by LFO, and the depth of modulation is determined by DAM.

L3.5.3.12 RST

It is a bit for performing forced silencing.

0 : Instantaneously resets EG value (-96dB = silencing).
1 : Attains normal operation.

L3.5.3.13 KSR

It is a bit to set the "Key Scale" of rate. It is a FM voice parameter.
For natural musical instruments, generally, rising and falling time of voice become short as the interval becomes higher. This phenomenon is simulated by the "Key Scale" of rate. The details are explained in the method of calculation of rate time.

L3.5.3.14 KSL

This is a bit to designate the scaling of level. It is a FM voice parameter.
For natural musical instruments, generally, volume is attenuated as the interval becomes higher.
This phenomenon is simulated by the Key Scale of rate. This is the bit to set attenuation for each octave.

0 : OFF
1 : 3.0dB / oct
2 : 1.5dB / oct
3 : 6.0dB / oct

The attenuation of actual level is set by dividing one octave by high-order four bits of FNUM.
As for the attenuation of actual level, refer to “L5.1.3 FM Synthesizer Key Scale Level Correspondence Table”.

Rate Calculation Method

Find the RATE = [setting value of rate] × 4 + Rof by using setting values of AR, DR, SR, RR (0 to 15).
(However, if the setting value = 0, RATE=0 regardless of Rof value.

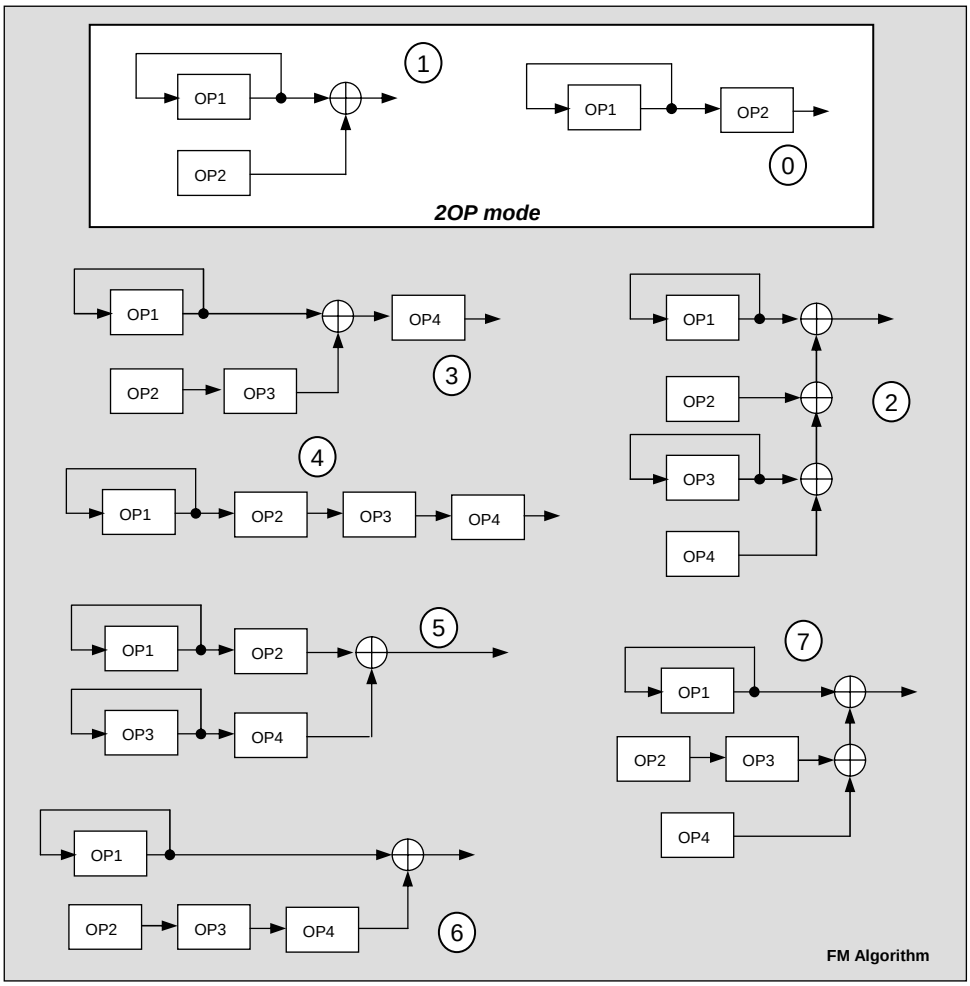
Find the actual time from the RATE value obtained on above formula with reference to the table shown in “L5.1.2 Envelope Rate Table of FM Synthesizer & WT Synthesizer“.
Rof is offset values which are determined by KSR bit and voice to generate (F-Number, Block + BO).

BLOCK + BO		0		1		2		3		4		5		6		7	
FMUM MSB bit		0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Rof	KSR=0	0				1				2				3			
	KSR=1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

L3.5.4 Functions Related to FM Algorithm

L3.5.4.1 ALG

This is a bit to set an algorithm of FM. (algorithm is a “Combination of Operators”.)
It is a FM voice parameter.
The 2OP (0 and 1 in the following figure) can be selected by Four 4OP mode (Intermediate register #56 FMMODE=“0”)
When 2 OP is selected, it is unnecessary to set voice parameters for OP3 and OP4.



L3.5.4.2 FB

This is a feedback function, that uses operator output as its modulating signals. It is a FM voice parameter.
FB bit is used to select a degree of modulations.

0 : feedback OFF
1 : π /16
2 : π / 8
3 : π / 4
4 : π / 2
5 : π
6 : 2π
7 : 4π

L3.5.4.3 WS

This is the bit for selecting waveform that is used for FM operation. It is a FM voice parameter.
For the correspondence between the set values and waveforms, refer to "L5.1.1 Basic Waveform Selection of FM Synthesizer & HV Synthesizer".
When the set values are 15, 23, and 31, FM operation is performed by using waveforms on the memories that are designated by the Control registers #464 to #469.
In other word, this function makes it possible to make voices freely because any waveforms can be set on SRAM.

[FM expanded waveform setting C_Address #464 to #469] Default 8'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 464	W/R	FM WAVE#15 [14:8]						
# 465	W/R	FM WAVE#15 [7:1]						
# 466	W/R	FM WAVE#23 [14:8]						
# 467	W/R	FM WAVE#23 [7:1]						
# 468	W/R	FM WAVE#31 [14:8]						
# 469	W/R	FM WAVE#31 [7:1]						

How to set FM expansion waveform?

In the Control registers #464 to #469, address locations of SRAM where waveforms are placed are set.
It is necessary to set two words per one waveform. A high-order word and a low-order word must be transferred as one packet.
Wrong value may be set if they are not transferred as one packet.
The range of address of SRAM is from 15'h4000 to 15'5FFF.
For example, when a waveform is placed in 15'h4000, it set 7'b100_0000 in FM WAVE [14:8] and 7'b000_0000 in FM WAVE [7:1]. The waveforms to be registered in SRAM must meet the following conditions.

- 16-bit PCM data, 2's complement format (Big-Endian)
- Number of samples of one waveform: 1024 (1 sample =16-bits)
- Make sure to set the head of waveform data on 2-byte boundary (even address).

L3.5.5 Other Functions

L3.5.5.1 PANPOT

This is a FM voice parameter to set the volume balance between the right and left channels. (The specifications are the same as the Control registers #208 to #223.)
For more details, refer to the “L3.10 Volume Functions”.

L3.5.5.2 PE

This is a bit for selecting either PANPOT settings designated with the channel parameters or PANPOT value designated in the voice parameters.
“1” selects PANPOT setting value in the voice parameters, and “0” selects PANPOT value designated with channel parameters.

L3.5.5.3 PANOFF

It is in the FM voice parameter. The Panpot function is disabled for voices of which PANOFF bit is “1”, and 0 dB is set for both Lch and Rch.
This operation is given priority over PE or PANPOT setting.
“0” set a normal operation. The operation follows PE or PANPOT setting.

L3.5.5.4 LFO

It is LFO frequency that is used each voice. It is a FM voice parameter

0 : 1.8Hz
1 : 4.0Hz
2 : 5.9Hz
3 : 7.0Hz

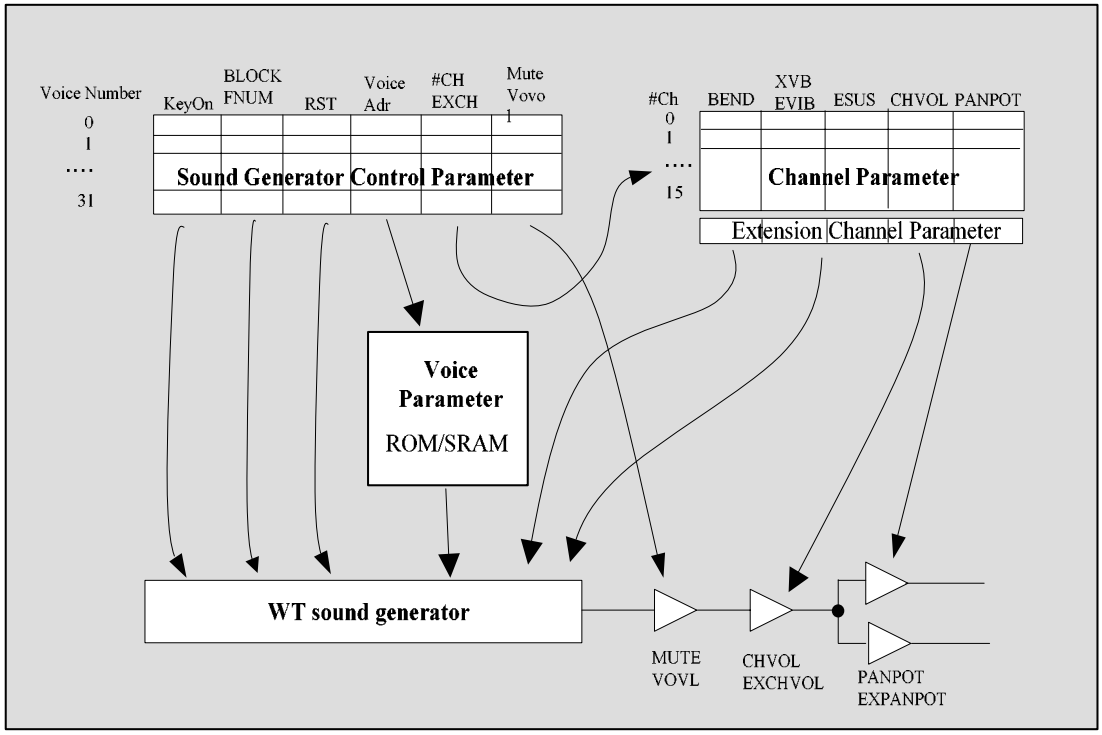
This LFO is used for vibrato and AM modulations. LFO is a triangular wave, and it oscillates toward positive and negative directions around “0”.

L3.6 WT Synthesizer

Control Parameters of WT Synthesizer

The following figure shows the connections of various parameters that are used to playback a WT voice. (The configuration is the same as the one described in “L3.5.1 Function Related to FM ”.
The hardware that generates one WT voice is called “WT Sound Generator”. The WT sound generator controls various parameters to create WT voices. There are the following three parameters that control the WT sound generator.

- Sound generator control parameters
- Voice parameters
- Channel parameters and expanded channel parameters



This is a WT synthesizer that has 32 voices. The synthesizer supports a pitch ranging from DC to fs.
This system places a voice on ROM/SRAM, and it designates voice numbers by using registers.

L3.6.1 Function Related to WT Sound Generator

This is a register that controls the WT Sound Generator. The Control registers #96 to #191 correspond to the WT Sound Generators No.0 to 15, and the Control Registers #368 to #463 correspond to the WT Sound Generators No.16 to 31 respectively.

Control register	WT sound generator number	Control register	WT sound generator number
#96 ~ #101	0	#368 ~ #373	16
#102 ~ #107	1	#374 ~ #379	17
#108 ~ #113	2	#380 ~ #385	18
#114 ~ #119	3	#386 ~ #391	19
#120 ~ #125	4	#392 ~ #397	20
#126 ~ #131	5	#398 ~ #403	21
#132 ~ #137	6	#404 ~ #409	22
#138 ~ #143	7	#410 ~ #415	23
#144 ~ #149	8	#416 ~ #421	24
#150 ~ #155	9	#422 ~ #427	25
#156 ~ #161	10	#428 ~ #433	26
#162 ~ #167	11	#434 ~ #439	27
#168 ~ #173	12	#440 ~ #445	28
#174 ~ #179	13	#446 ~ #451	29
#180 ~ #185	14	#452 ~ #457	30
#186 ~ #191	15	#458 ~ #463	31

Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 96	W/R	Voice Adr [14:8]						
# 97	W/R	Voice Adr [7:1]						
# 98	W/R	VOVOL					MTRON	LEDON
# 99	W/R	EXCH	BLOCK			FNUM (H)		
# 100	W/R	FNUM (L)						
# 101	W/R	KeyOn	MUTE	RST	#CH			

L3.6.1.1 VoiceAdr

Function description is same as those of FM synthesizer. (Refer to L3.5.1 Function Related to FM).

L3.6.1.2 VOVOL

Function description is same as those of FM synthesizer.

L3.6.1.3 MTRON

Function description is same as those of FM synthesizer. "1" indicates the voice generation is with MTR synchronization.

L3.6.1.4 LEDON

Function description is same as those of FM synthesizer. "1" indicates the voice generation is with LED synchronization.

L3.6.1.5 EXCH

Function description is same as those of FM synthesizer.

L3.6.1.6 BLOCK

This bit designates a octave.
The formula for calculation of the voice generation pitch that is derived from the setting values of BLOCK and FNUM is different from the one for FM.
For the details, refer to the "L3.6.2 Function Related to PG (Pitch Generator)".

L3.6.1.7 FNUM

This parameter is used with BLOCK to set pitches.
For the details, refer to the “L3.6.2 Function Related to PG (Pitch Generator)”.

L3.6.1.8 KeyOn

Function description is same as those of FM synthesizer. “1” enables KeyOn (voice generation) and “0” disables KeyOff (the voice generation control is terminated).

L3.6.1.9 MUTE

Function description is same as those of FM synthesizer. “1” enables mute, and “0” cancels mute.

L3.6.1.10 RST

Function description is same as those of FM synthesizer. This is the bit for performing forced silencing.

L3.6.1.11 #CH

It designates parameter numbers of channels that are linked with WT sound generator.

L3.6.2 Function Related to PG (Pitch Generator)

L3.6.2.1 BLOCK

This is a bit that designates an octave (0 to 7). For the details about the relationship between setting values and output frequency, refer to the following “FNUM”.
The bit becomes valid at the time FNUM (L) has been written.
Be sure to transfer BLOCK, FNUM (H), EXCH, and FNUM (L) as one packet.
Wrong FNUM may be set if they are not transferred as one packet.

L3.6.2.2 FNUM

This is a parameter to set the pitch of the WT Sound Generator.
Both D2 to D0 bits of FNUM (H) and D6 to D0 bits of FNUM (L) become FNUM that is used in the following formula.

The amount of change of pitch to the reference pitch (unit of [cent]) is given by the following formula.

$$F\ [cent] = 1200 * (BLOCK - 5) + 1200 \times \log_2 [(1024+FNUM) / 1024]$$

Frequency is given by the formula f_Voice = 2 ^ (F/ 1200) × fs × BEND.
Playbacking oscillation frequency f_play = f_Voice × (LFO_PM) [Hz]
fs [Hz] : Sampling frequency
BEND : Pitch bend set with channel parameters (Refer to the “L3.5.2.3 INT, FRAC”)

A pause occurs when “0” is set to both FNUM and BLOCK. When a value other than “0” is set, the operation restarts with pitch based on the setting value.
The bit becomes valid at the time FNUM (L) has been written. Be sure to transfer BLOCK, FNUM(H), and FNUM(L) as one packet. Wrong FNUM may be set if they are not transferred as one packet.

L3.6.2.3 Pitch bend (INT, FRAC)

Function description is same as those of FM synthesizer.

L3.6.2.4 DVB

Function description is same as those of FM synthesizer. This is in the WT voice parameter.

L3.6.2.5 EVB

Function description is same as those of FM synthesizer. This is in the WT voice parameter.
As for WT voice parameter map, refer to “L3.1.4 SRAM”.

L3.6.2.6 XVB, EVIB

Function description is same as those of FM synthesizer. These are channel parameters.

L3.6.3 Functions Related to EG (Envelope Generator)

L3.6.3.1 AR

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter.

L3.6.3.2 DR

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.3 SR

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.4 RR

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.5 SL

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.6 SUS

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.7 ESUS

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.8 TL

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.9 XOF

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.10 DAM

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

L3.6.3.11 EAM

Function description is same as those of FM synthesizer. This is existed in the WT voice parameter

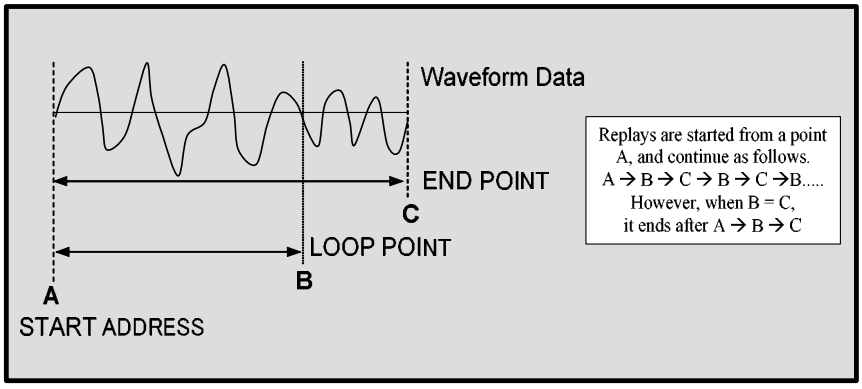
L3.6.3.12 RST

Function description is same as those of FM synthesizer. This is a WT voice parameter.

L3.6.4 Functions Related to Waveform Data

L3.6.4.1 START ADDRESS

This is in the WT Voice Parameter.
Be sure to specify the address of the head on the memory on which waveform data is put.
In addition, make sure to specify a two-byte boundary (even address).



L3.6.4.2 END POINT

This is in the WT Voice Parameter.
It designates an end point of playback and a loop end point of loop playback.
Set the number of data from START ADDRESS (including the number of samples of START ADDRESS) to END POINT (not including END POINT).

In case of stereo data (STEREO = "1")

It is set to one END POINT by both L Channels and R Channels. Therefore, in the case of 8-bit stereo data, although combining L Channel and R Channel, and making 100 samples in all, END POINT becomes 50.

In case of 16 bits stereo data

Although combining L Channel and R Channel, and making 100 samples in all, END POINT becomes 25.

L3.6.4.3 LOOP POINT

This is in the WT Voice Parameter.
It designates a loop point used to perform loop playback after waveform data has arrived at END POINT.
Set the number of data from START ADDRESS (including the number of samples of START ADDRESS) to LOOP POINT (not including LOOP POINT).
The same case as END POINT, the contents of stereophonic data become as described below.

In case of 8 bits stereo data

Although combining L channel and R channel, and making 100 samples in all, LOOP POINT becomes 50.

In case of 16 bits stereo data

Although combining L channel and R channel, and making 100 samples in all, LOOP POINT becomes 25.

L3.6.4.4 MODE END

This is a bit that designates a format of waveform data. This is in the WT Voice Parameter.
MODE bit of voice parameter is used for this setting.

"0" : 4-bit ADPCM (leading data on the low-order 4 bit of a byte, and next data on the high-order side)

"1" : 16-bit 2's complement PCM

"2" 8-bit (offset bin) PCM

"3" : 8-bit (2's comp) PCM

About Placement of Waveform Data

When using stereophonic data;

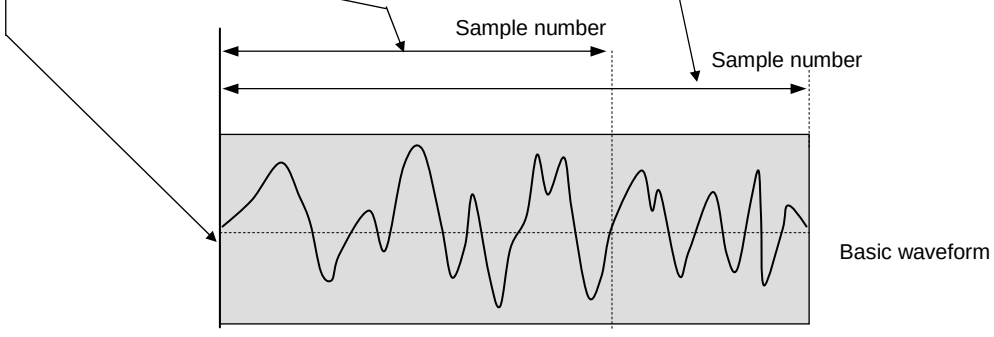
→ For 8-bit data : It is necessary to place a waveform data on the 2-byte boundary.

→ For 16-bit data : It is necessary to place a waveform data on the 4-byte boundary.

When using 16-bit monophonic data;

→ For 16-bit data : It is necessary to place a waveform data on the 2-byte boundary.

	D7	D6	D5	D4	D3	D2	D1	D0
# 0	PANPOT					"0"	STM	PE
# 1	LFO		"0"	"0"	"0"	PAN OFF	MODE	
# 2	SR				XOF	"0"	SUS	"0"
# 3	RR				DR			
# 4	AR				SL			
# 5	TL						"0"	"0"
# 6	"0"	DAM		EAM	"0"	DVB		EVB
# 7	START ADDRESS (H)							
# 8	START ADDRESS(L)							
# 9	LOOP POINT(H)							
# 10	LOOP POINT(L)							
# 11	END POINT (H)							
# 12	END POINT (L)							



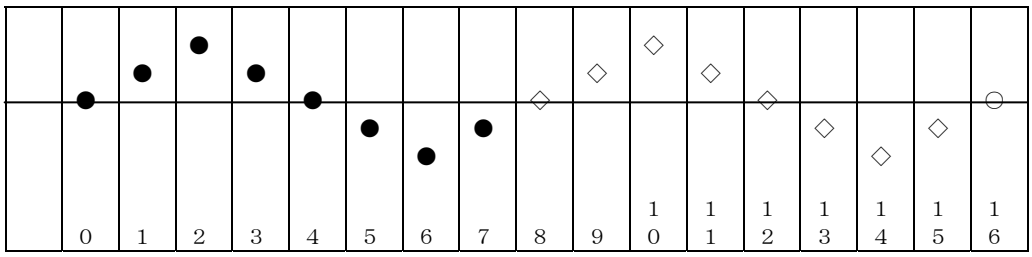
The Variety of Playback

There are the following two kinds of the waveform playback methods.

- Loop playback (Playback the specified loop section infinitely)
- One shot playback (Playback from the head to the end only once)

L3.6.4.5 LOOP Playback

It describes END POINT setting and LOOP POINT setting at the time of loop playback.
Here is mention about a triangular wave as an example. It is 16 samples in all, 8 samples of first half that do not loop (●) and 8 samples of second half that loops (◊).



Loop playback of PCM data

- Specify the End Point= 16 and the Loop Point= 8.
- Set the data (8) of the Loop Point as the data of 16.
- Total 17 samples of 0 to 16 are needed.

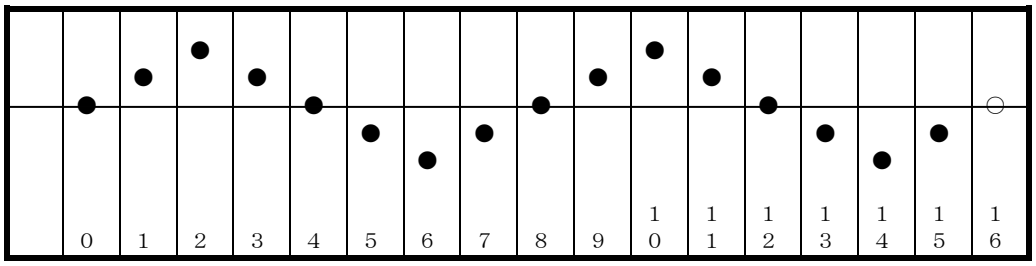
Loop playback of ADPCM data

In the case of ADPCM loop playback, it becomes the following.

- Specify the End Point= 16 and the Loop Point= 8.
- Unlike PCM loop playback, the data of 16 is not needed.
- Total 16 samples of 0 to 15 are needed.

L3.6.4.6 One shot playback

It describes END POINT setting and LOOP POINT setting at Voice Shot Playback.
Similarly explains using the following triangular wave.



One shot playback of PCM data

- Specify the End Point = Loop Point= 15. (Total sample number – 2)
- Set “0” or the data of 15 as the data of 16.
- Total 17 samples of 0 to 16 are needed.

The meaning of sample No. 16

When interpolation process of samples 15 and 16 are performed, the data of 16 is used.
If the waveform is like the above figure, the data of 16 are good at “0”, however, when the data of 15 is quite different from “0”, the same data as 15 may be set.

One shot playback of ADPCM data

- Specify the End Point = Loop Point= 15. (Total sample number – 1)
- The data of 16 is not needed.
- Total 16 samples of 0 to 15 are needed.

Be sure to set the waveform data value of “END POINT = LOOP POINT” to “0” as much as possible.

It can say in both cases PCM and ADPCM.

L3.6.5 Other Functions

L3.6.5.1 PANPOT

Function description is same as those of FM synthesizer. This is in the WT Voice Parameter.
This is a parameter to set the volume balance between the right and left channels. (The specifications are the same as the Control registers #208 to #223.)
For more details, refer to the “L3.10 Volume Functions“.

L3.6.5.2 PE

Same function description as FM synthesizer. This is in the WT Voice Parameter.

L3.6.5.3 PANOFF

Function description is same as those of FM synthesizer. This is in the WT Voice Parameter.

L3.6.5.4 LFO

Function description is same as those of FM synthesizer. This is in the WT Voice Parameter.

L3.6.5.5 STM

This is a bit to define whether voice parameter is for Stream playback or not.
“1” defines voice parameter for Stream playback, and “0” defines voice parameter for WT.
When STM bit is “1”, channel parameters are fixed as (ESUS=0, XVB=0, CHVOL=0dB and BEND= 1.0).
ENDPOINT data is read as LOOPPOINT data.
The following table collects the operational specifications of STM bit.

STM	Conversion of ENDPOINT data to LOOPPOINT	Channel parameters
1	Converts	ESUS=0, XVB=0, CHVOL=0dB, BEND= 1.0 time fixed
0	Does not convert.	It depends on the values set in the channel parameters of each #CH.

L3.7 Stream Playback Section

The Stream Playback Section is realized by switching resources of the WT Sound Generators #25 and #26. The functions are mostly the same as the WT synthesizer except the following two points.

- Stereophonic playback can be made only in the Stream Playback Section.
- Interrupt function can be used when supplementing waveform data.

Other features of the Stream Playback Section are described as follows.

- WT sound generators #25 and #26 are allocated to resources for the Stream Playback by setting STMMODE bit of the Intermediate register #56 to “1”.
- For monaural playback, two channels can be played back simultaneously.
- For waveform data, both ADPCM and PCM data can be used.
- For PCM data, both 8 bit data and 16 bit data can be used.
- As hardware, upper limit of sampling frequency is 48kHz.

L3.7.1 Functions Related to Stream Playback Sound Generator

This is a register to control a Sound generator for Stream playback.
This register shares resources with the WT Sound Generators #25 and #26.

Control register	WT sound generator number	Control register	WT sound generator number
#422 ~ #427	25	#428 ~ #433	26

By setting STMMODE bit of the Intermediate Register #56 to "1", WT Sound Generators #25 and #26 can be used for Stream playback. Setting STMMODE bit to "1" enables the following operation.
WT Sound Generator #25 and WT Sound Generator #26 are controlled by the "Volume setting for stream playback" of the Intermediate register #43. (When STMMODE="0", they are controlled with the Intermediate register #42.For the details, refer to the "L3.4.1.3 Stream Playback Mode Selection".

L3.7.1.1 VoiceAdr

Function description is same as those of FM synthesizer.

L3.7.1.2 VOVOL

Function description is same as those of FM synthesizer.

L3.7.1.3 MTRON

Function description is same as those of FM synthesizer.

L3.7.1.4 LEDON

Function description is same as those of FM synthesizer.

L3.7.1.5 EXCH

Function description is same as those of FM synthesizer.

L3.7.1.6 BLOCK

Function description is same as those of WT synthesizer.

L3.7.1.7 FNUM

Function description is same as those of WT synthesizer.

L3.7.1.8 KeyOn

Function description is same as those of FM synthesizer.

L3.7.1.9 MUTE

Function description is same as those of FM synthesizer..

L3.7.1.10 RST

Function description is same as those of FM synthesizer..

L3.7.1.11 #CH

It designates a channel parameter numbers that are linked with the Stream playback sound generator.

L3.7.2 Functions of PG (Pitch Generator)

L3.7.2.1 BLOCK

Function description is same as those of WT synthesizer.

L3.7.2.2 FNUM

Function description is same as those of WT synthesizer.

L3.7.2.3 Pitch bend (INT, FRAC)

Function description is same as those of FM synthesizer.

L3.7.2.4 DVB

Function description is same as those of FM synthesizer. It is a WT voice parameter

L3.7.2.5 EVB

Function description is same as those of FM synthesizer. It is a WT voice parameter

L3.7.2.6 XVB, EVIB

Function description is same as those of FM synthesizer. These are channel parameters.

L3.7.3 Functions Related to EG (Envelope Generator)

L3.7.3.1 AR

Function description is same as those of FM synthesizer.

L3.7.3.2 DR

Function description is same as those of FM synthesizer.

L3.7.3.3 SR

Function description is same as those of FM synthesizer.

L3.7.3.4 RR

Function description is same as those of FM synthesizer.

L3.7.3.5 SL

Function description is same as those of FM synthesizer.

L3.7.3.6 SUS

Function description is same as those of FM synthesizer.

L3.7.3.7 ESUS

Function description is same as those of FM synthesizer.

L3.7.3.8 TL

Function description is same as those of FM synthesizer.

L3.7.3.9 XOF

Function description is same as those of FM synthesizer.

L3.7.3.10 DAM

Function description is same as those of FM synthesizer.

L3.7.3.11 EAM

Function description is same as those of FM synthesizer.

L3.7.3.12 RST

Function description is same as those of FM synthesizer.

L3.7.4 Functions Related to Waveform Data

The specifications of a voice data (the following #0 to #12) are the same as those of WT synthesizer.
WT Sound Generator #25 and #26 should be set independently.

L3.7.4.1 START ADDRESS

Function description is same as those of WT synthesizer.

L3.7.4.2 END POINT

Function description is same as those of WT synthesizer.
There is a difference in value to set, between the case of ADPCM data to playback and the case of PCM data to playback.

When PCM data (monaural) is played back

For the setting value of END POINT, set the value of "buffer size reserved in SRAM - 1".
For example, when SRAM of 1024 bytes is reserved, set END POINT = 1023.

When ADPCM data (monaural) is played back,

For the setting value of END POINT, set the value of "buffer size reserved in SRAM ×2".
For example, when SRAM of 1024 bytes is reserved, set END POINT = 2048.

L3.7.4.3 LOOP POINT

Set "0".

L3.7.4.4 MODE

Function description is same as those of WT synthesizer..

About Supply of Waveform Data (In the Case of Monaural Data)

The data supply method is different between PCM data and ADPCM data.

In the case of 8-bit PCM stream playback

In the case of performing, Stream replay by using 1024-byte memory as a circulation buffer, is described here.
In this case, set as LOOPPOINT= 0 and ENDPOINT=1023.
In this memory, store the data as described below.

Mem. Address	0	1	2	.....	1022	1023
At the 1st loop	0	1	2	.....	1022	1023
At the 2nd loop	1023	1024	1025	.....	2045	2046
At the 3rd loop	2046	2047	2048	.....	3068	3069

Mem Address: Memory Address of ROM / SRAM.

In the case of 16-bit PCM stream playback

In the case of performing, Stream replay by using 1024-byte memory as a circulation buffer, is described here.
In this case, set as LOOPPOINT= 0 and ENDPOINT=511.
In this memory, store the data as described below.

Mem Address	0	1	2	.....	1022	1023
At the 1st loop	0L	0H	1L	.....	511L	511H
At the 2nd loop	511L	511H	512L	.....	1022L	1022H

(L and H means L side and H side of 16 bits.)

In the case of ADPCM stream playback

In the case of performing, Stream replay by using 1024-byte memory as a circulation buffer, is described here.
In this case, set as LOOPPOINT= 0 and ENDPOINT=2048.
In this memory, store the data as described below.
In the case of ADPCM, unlike PCM, the copy is not needed.
Since ADPCM data has two samples in 1-byte, the notation method is as shown like “0&1”.

Mem. Address	0	1	2	.....	1023
At the 1st loop	0&1	2&3	4&5	.....	2046&2047
At the 2nd loop	2048&2049	.....			

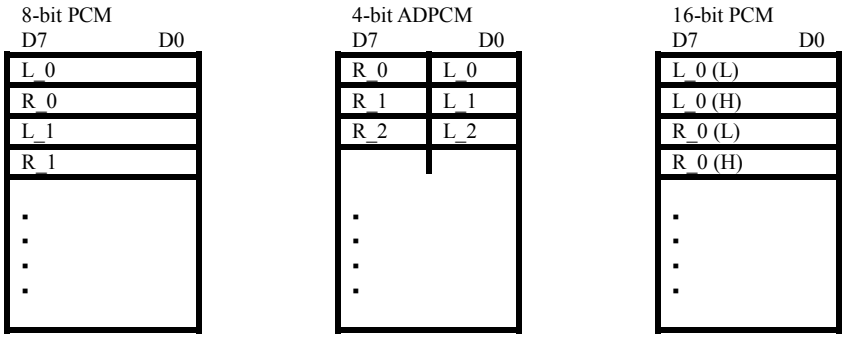
About Supply of Waveform Data (In the Case of Stereophonic Data)

The specifications of a voice data (the following #0 to #12) are used commonly to WT Sound Generators #25 and #26. For the setting value of START ADDRESS, set the address on which the waveform data of Lch side (=WT voice #25) is placed.
(LOOP POINT and END POINT should become the same setting in Lch side and Rch side.)

	D7	D6	D5	D4	D3	D2	D1	D0
# 0	PANPOT					“0”	STM	PE
# 1	LFO		“0”	“0”	“0”	PAN OFF	MODE	
# 2	SR				XOF	“0”	SUS	“0”
# 3	RR				DR			
# 4	AR				SL			
# 5	TL						“0”	“0”
# 6	“0”	DAM		EAM	“0”	DVB		EVB
# 7	START ADDRESS (H)							
# 8	START ADDRESS(L)							
# 9	LOOP POINT(H)							
# 10	LOOP POINT(L)							
# 11	END POINT (H)							
# 12	END POINT (L)							

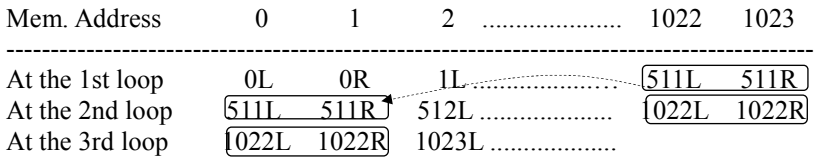
Waveform data

The method of placement of waveform data varies according to the bit length of data (ADPCM, 8 bits and 16 bits).



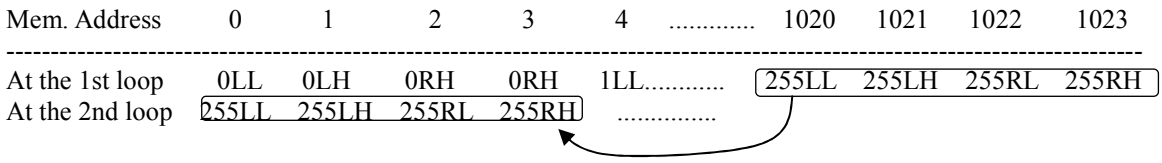
In the case of 8-bit PCM stream playback

In the case of performing, Stream replay by using 1024-byte memory as a circulation buffer is described here.
In this case, set as LOOPPOINT= 0 and ENDPOINT=511.
In this memory, store the data as described below.
In the case of stereophonic data, the copy for 2 bytes is needed.



In the case of 16-bit PCM stream playback

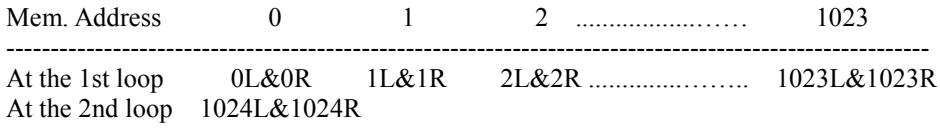
In the case of performing, Stream replay by using 1024-byte memory as a circulation buffer is described here.
In this case, set as LOOPPOINT= 0 and ENDPOINT=255.
In this memory, store the data as described below.
In the case of stereophonic data, the copy for 4 bytes is needed.



(0LH means the data of H side of Lch in the 0th sample.)

In the case of ADPCM stream playback

In the case of performing Stream replay by using 1024-byte memory as a circulation buffer is described here, also.
In this case, set as LOOPPOINT= 0 and ENDPOINT=1024.
In this memory, store the data as described below.
In the case of ADPCM, unlike PCM, the copy is not needed.
Since ADPCM data has two samples in 1-byte, the notation method is as shown like “A&B”.



L3.7.5 Stereophonic Playback Functions

L3.7.5.1 Selection of stereophonic or monaural

Intermediate Register #58 has a bit for selecting stereophonic or monaural.

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
# 58	W/R	"0"	"0"	"0"	STEREO	"0"	"0"	RSTM#1	RSTM#0

STEREO : When set to "1", stereophonic playback can be made by using two resources, WT Sound Generators #25 and #26. "0" enables the monaural playback.

Explanation of operations when STEREO bit = "1"

WT Sound Generator #25 playback the Lch data, and WT Sound Generator #26 playback the Rch data.
The number of simultaneously generated sounds in the Stream Playback becomes one tone when stereophonic system is used.

How to control Sound generator at stereophonic playback

Basically, the control of the Stereophonic Stream Playback is performed from the Control Registers (#422 to #427) of the WT Sound Generator #25, except following matters.

- WT Sound Generator #26 sides also have registers that need setting.

  For the Control Registers #428 to #430, set the same values as #422 to #424 of the WT Sound Generator #25 before starting stereophonic playback (before setting KeyOn bit of #427 to "1").
  This means that;
  Setting value of # 422 = Setting value of # 428
  Setting value of # 423 = Setting value of # 429
  Setting value of # 424 = Setting value of # 430

- Registers that do not need setting on the WT Sound Generator #26 side

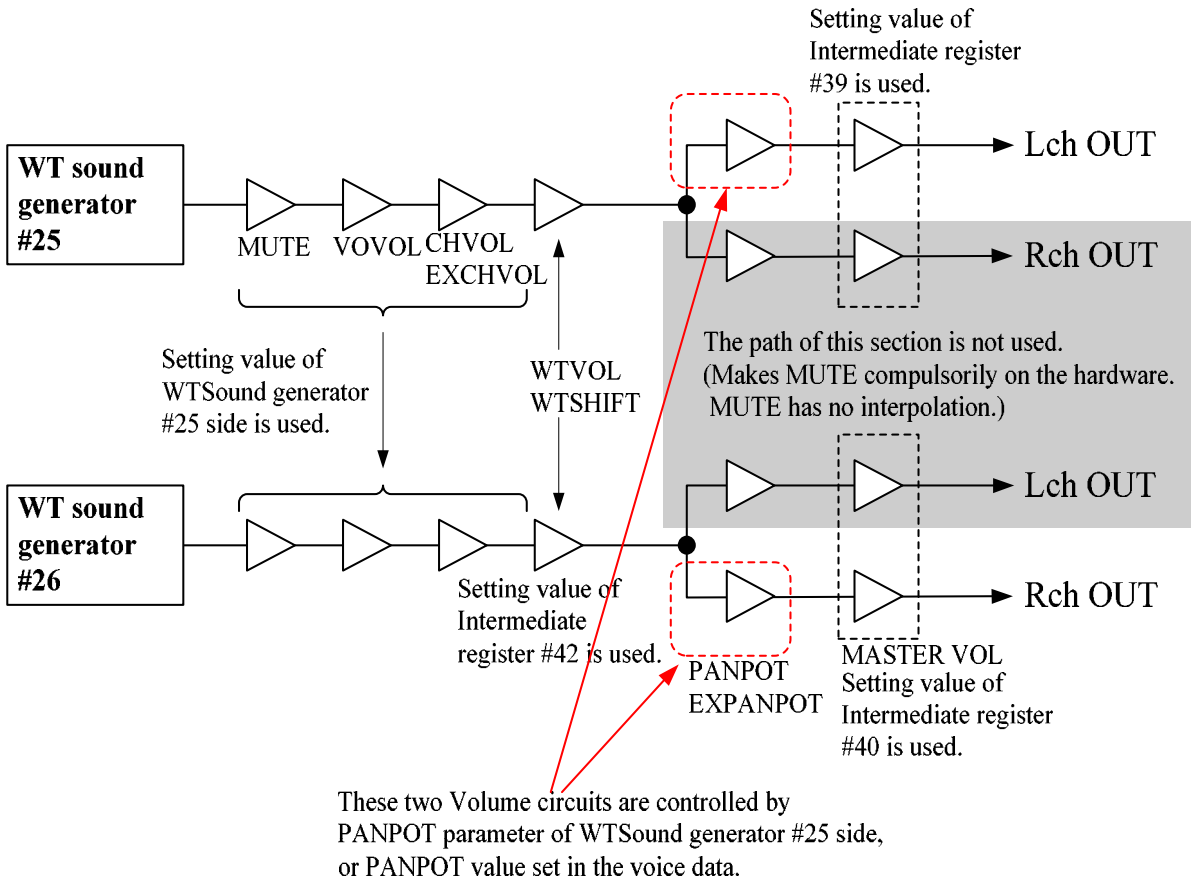
  #431 to #433 does not need setting. When STEREO bit = "1", the operation is not affected by the value of these registers.

Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 422 / 428	W/R	Voice Adr [14:8]						
# 423 / 429	W/R	Voice Adr [7:1]						
# 424 / 430	W/R	VOVOL					MTRON	LEDON
# 425 / 431	W/R	EXCH	BLOCK			FNUM (H)		
# 426 / 432	W/R	FNUM (L)						
# 427 / 433	W/R	KeyOn	MUTE	RST	#CH			

Explanation of operation of volume circuit at stereophonic playback

For MUTE, VOVOL, CHVOL/EXCHVOL, and CHPAN/EXPANPOT, the control on the WT Sound Generator #25 becomes valid.



L3.7.6 Other Functions

L3.7.6.1 Stream playback position reading function

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
# 25	R	"0"	"0"	STREAM PG#0					
# 26	R	"0"	"0"	STREAM PG#1					

STREAM PG# * : This register can be read the present playback position in the buffer size that is reserved for Stream playback.
Intermediate register #25 is the read-out register of WT Sound Generator #25, and the Intermediate Register #26 is the read register of WT Sound Generator #26.
Because of the acquired buffer size (SIZE bit setup) for a stream and the bit numbers per one sample, the sample numbers which are storable in the buffer are differed. In case that the sample size is 1024, the playback position changes from 10'h000 to 10'h3FF.
The value, which is read from this register, is high-order 6 bits of the 10 bits.
In other sample sizes also, the value which is read from this register is high-order 6 bits of the 10 bits.

	The number of bits per one sample			
SIZE[1:0]	4 bits (ADPCM mono)	8 bits (ADPCM stereo 8-bit PCM mono)	16 bits (8-bitPCM stereo 16-bitPCM mono)	32 bits (16-bitPCM stereo)
0 (=512 bytes)	Sample number is 1024	Sample number is 512	Sample number is 256	Sample number is 128
1 (=1024 bytes)	Sample number is 2048	Sample number is 1024	Sample number is 512	Sample number is 256
2 (=2048 bytes)	Sample number is 4096	Sample number is 2048	Sample number is 1024	Sample number is 512

L3.7.6.2 Interrupt from Stream playback

Interrupt can be generated according to the amount of consumption of waveform buffer

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
# 57	W/R	“0”	“0”	BUF SIZE		“0”	“0”	STM IRQPOINT	

For the details, refer to the “L3.3.7 Stream Playback Interrupt”.

L3.7.6.3 Playback position clearing bit

As described in “L3.7.6.1 Stream playback position reading function”, the playback position of a waveform data is operating during a Stream Playback.
(When one wave sample is played back, the playback point is also increased by +1.)
When KeyOn bit is set to “0”, the playback point is cleared to “0”. If you want to clear the playback position by a certain reason, set this bit to “1”.
“Read registers of playback position” of the Intermediate register #25 and #26 are also cleared.

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
# 58	W/R	“0”	“0”	“0”	STEREO	“0”	“0”	RSTM#1	RSTM#0

RSTM#0, RSTM#1 : By setting “1”, it clears the position.

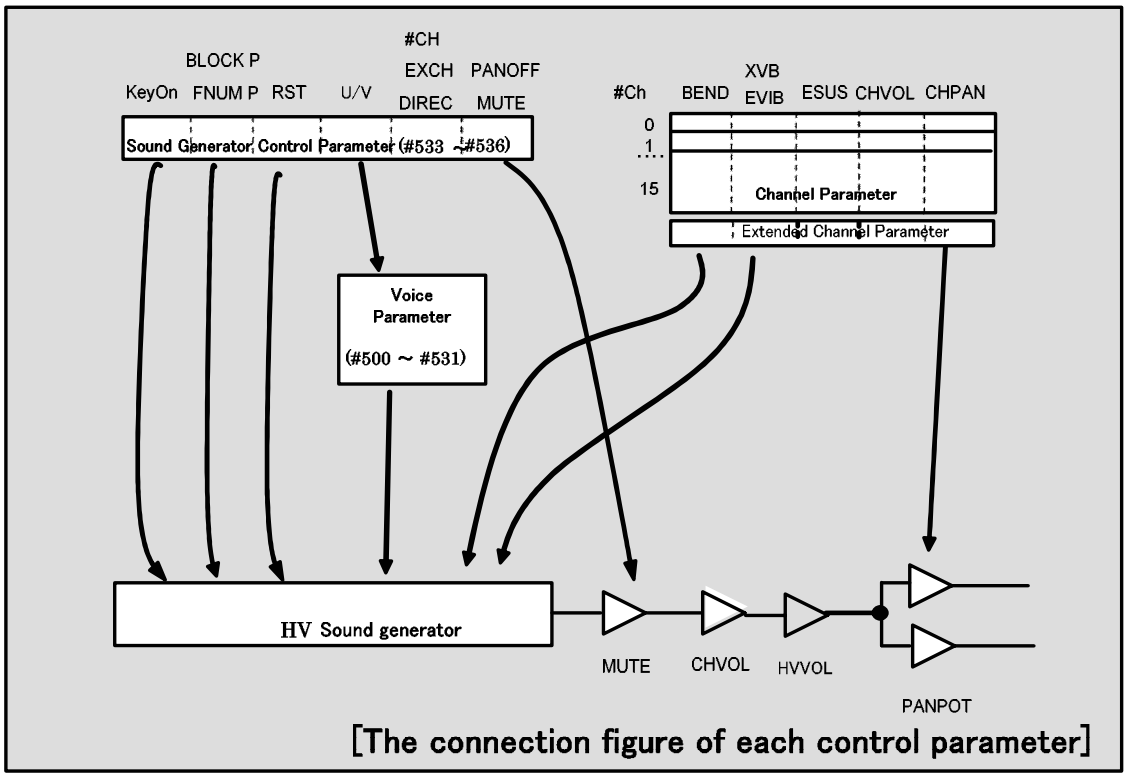
RSTM#0 is for the WT Sound Generator #25, and RSTM#1 is for the WT Sound Generator #26.
After setting the bits to “1”, it must be restored to “0”.
It is not necessary to reserve a time from setting “1” to setting “0”.

L3.8 HV Synthesizer

The Control Parameter of HV Synthesizer

The following figure shows a connection between the setup values (parameters) of each register for generating a HV voice. There are three parameters to control HV voices.

- Sound generator control parameter (Control register #533 to #536）
- Voice parameter (Control register #500 to #531）
- Channel parameter (Control register #192 to #271、#483 to #487）



L3.8.1 Functions Related to HV Voice

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0	
# 500	W/R	“0”	PAI_0	WS_0					Waveform selection at the time of a voiced sound
# 501	W/R	“0”	PAI_1	WS_1					
# 502	W/R	“0”	PAI_2	WS_2					
# 503	W/R	“0”	PAI_3	WS_3					
# 504	W/R	“0”	PAI_4	WS_4					
# 505	W/R	“0”	PAI_5	WS_5					
# 506	W/R	“0”	PAI_6	WS_6					
# 507	W/R	“0”	PAI_7	WS_7					
# 508	W/R	FMT Level 0							Formant 0
# 509	W/R	“0”	BLOCK_F 0			FNUM_F 0(H)			
# 510	W/R	FNUM_F 0(L)							
# 511	W/R	FMT Level 1							Formant 1
# 512	W/R	“0”	BLOCK_F 1			FNUM_F 1(H)			
# 513	W/R	FNUM_F 1(L)							
# 514	W/R	FMT Level 2							Formant 2
# 515	W/R	“0”	BLOCK_F 2			FNUM_F 2(H)			
# 516	W/R	FNUM_F 2(L)							
# 517	W/R	FMT Level 3							Formant 3
# 518	W/R	“0”	BLOCK_F 3			FNUM_F 3(H)			
# 519	W/R	FNUM_F 3(L)							
# 520	W/R	FMT Level 4							Formant 4
# 521	W/R	“0”	BLOCK_F 4			FNUM_F 4(H)			
# 522	W/R	FNUM_F 4(L)							
# 523	W/R	FMT Level 5							Formant 5
# 524	W/R	“0”	BLOCK_F 5			FNUM_F 5(H)			
# 525	W/R	FNUM_F 5(L)							
# 526	W/R	FMT Level 6							Formant 6
# 527	W/R	“0”	BLOCK_F 6			FNUM_F 6(H)			
# 528	W/R	FNUM_F 6(L)							
# 529	W/R	FMT Level 7							Formant 7
# 530	W/R	“0”	BLOCK_F 7			FNUM_F 7(H)			
# 531	W/R	FNUM_F 7(L)							
# 532	W/R	“0”	“0”	“0”	“0”	“0”	MTRON	LEDON	LED, MTR Synchronous control
# 533	W/R	EXCH	BLOCK_P			FNUM_P(H)			Pitch
# 534	W/R	FNUM_P(L)							
# 535	W/R	“0”	“0”	“0”	“0”	U/V	PANOFF	DIREC	PANOFF, DIREC, U/V
# 536	W/R	KeyOn	MUTE	RST	# CH				KeyOn etc.

Renewal timing of a setup of #500-#535

By the write operation to #535, a setup of #500 to #535 becomes valid.

L3.8.1.1 U/V

This is a bit to switch a voiced sound and non-voiced sound to generate.
"0": voiced sound, "1": non voiced sound

L3.8.1.2 EXCH

When the EXCH bit is set up to "1", a parameter of the Control Register #483 to #487 which is designated at the "Setup of extended channel" is used.
In addition, when the EXCH bit is "0", the parameter of channel numbers which are set up by #CH of #536 is used.
In the case of use an extended channel parameter, Vibrato, Sustain, and Pitch bend are carried out with original behave of HV synthesizer like channel parameters.

L3.8.1.3 LEDON

It is used in case LED is controlled synchronizing with the voice of HV.
(For the specific details, refer to the "L3.11 LED, Vibrator control")

L3.8.1.4 MTRON

It is used in case a vibrator is controlled synchronizing with the voice of HV.
(For the specific details, refer to the "L3.11 LED, Vibrator control")

L3.8.1.5 KeyOn

This is a control signal of HV voice generation.
By "1" → Sound generation (KeyOn), and by "0" → terminated sound generation (KeyOff).

L3.8.1.6 MUTE

This is a mute setup of HV voice.
By "1" → MUTE, and by "0" → Non-mute.

L3.8.1.7 #CH

It designates a channel parameter numbers which are related with HV voices.

L3.8.1.8 DIREC

If a DIREC bit is set as "1", it will be separated from the channel parameter set up by #CH, and the fixed value of (ESUS=0, XVB=0, CHVOL=0dB, BEND=1.0) will come to be used. When a DIREC bit is "0" EXCH or #CH setup is followed.

L3.8.2 Functions Related to Pitch

L3.8.2.1 BLOCK_P, FNUM_P

It is the registers to set up the pitch of a voiced sound. Although it is fundamentally the same as the formula of formant frequency, a pitch bend setup is possible. The relation between a pitch and a setting value is shown by the following formula.

Pitch [Hz] = FNUM_P × (2^ (BLOCK_P - 1)) / (2^19) ×BEND(*)×fs
(fs[Hz] : Sampling frequency)

(*) The value used for BEND is decided by the setting value of EXCH and #CH. In case of EXCH="1", it is the value of control register #486 to #487. In case of EXCH="0", the value of control register #240 to #271 which had the channel number specified by #CH is used.

It becomes valid when FNUM P (L) is written. Please be sure to transfer BLOCK_P, EXCH, and FNUM_P (H) and FNUM_P (L) as one packet. Wrong FNUM may be set up when it does not transfer as one packet. Pitch can be operated up to the maximum of fs/11 [Hz].
(In the case of fs=48000, the maximum of a pitch is set to 4.36 kHz)

L3.8.2.2 BLCK_F, FNUM_F

It is the registers to set up the frequency of each formant. A value of 0 to 1023 can be set up by 10 bits; the D2 to D0 bit of FNUM_F (H), and D6-D0 bits of FNUM_F (L). A value of 0 to 7 can be set to BLOCK_F

The relation between a formant frequency and a setup value are shown by the following formula.

Formant frequency [Hz] = FNUM_F × (2^ (BLOCK_F - 1)) / (2^19) × fs
(fs[Hz]: Sampling frequency)

For example, in the case of FNUM_F=500, BLOCK_F=4, and fs=48 kHz, the formant frequency becomes 366.2Hz. The minimum value of formant frequency is 0 Hz (at the time of FNUM=0), and the maximum value of formant frequency is 5994.1 Hz.

It becomes valid when FNUM_F (L) is written. Please be sure to transfer BLOCK_F, EXCH, FNUM_F (H), and FNUM_F (L) as one packet. Wrong value may be set up when it does not transfer as one packet. Formant frequency is not influenced of a pitch bend setup.

L3.8.2.3 Pitch bend (INT, FRAC)

Pitch bend is not applicable to each formant frequency. The pitch-bend is applicable only to the pitch frequency of a voiced sound. Specification of pitch bend is the same as those of FM and WT synthesizer.

L3.8.2.4 XVB, EVIB

To hang up a vibrato to HV voice is prohibited.
Be sure to fixate the XVB bit as “0”.

L3.8.3 Functions Related to Level

L3.8.3.1 FMT Level

It is a level setup for every formant. Signification for every bit is as follows.
FMT Level = (-48 × D6) + (-24 × D5) + (-12 × D4)
+ (-6 × D3) + (-3 × D2) + (-1.5 × D1) + (-0.75 × D0) [dB].
In the case of all D6 to D0 bit are "1", it becomes non-voice (=-96dB).

L3.8.3.2 RST

"1": the envelope circuits are reset. "0": the envelope circuits are not reset.

L3.8.3.3 ESUS

HV synthesizer is disregard a sustain specification.

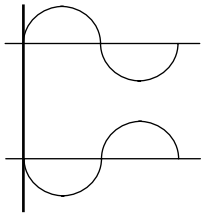
L3.8.4 Other Functions

L3.8.4.1 WS

It is a bit to select a basic waveform of each formant generation part.
At the time of a voiced sound (U/V bit ="0" of control register #535), 32 kinds of waveform are selectable as shown in "L5.1.1 Basic Waveform Selection of FM Synthesizer & HV Synthesizer".
At the time of non-voiced sound (U/V bit ="1" of control register #535), it becomes only a sign wave.
Refer to "L5.1.1 Basic Waveform Selection of FM Synthesizer & HV Synthesizer" for the relation between WS number and waveform form.

L3.8.4.2 PAI

It is a bit to perform a phase control of the basic waveform used in each formant.



"0": no phase shift

"1": Shifts a phase by π

L3.8.4.3 PANOFF

It is a bit to turn off the Panpot of HV voice compulsorily. It becomes an execution and
"0": no turn off
"1": off compulsorily

L3.9 AL Synthesizer

What is AL Synthesizer?

This is an abbreviation of Analog Lite synthesizer.

Function Outline of AL synthesizer

Functions can be classified into the “Function related to low pass filter section” and the “Function around low pass filter”.

Functions of low pass filter

- EG can be applied to cutoff frequency (It is called “filter EG”.)
  (For more details, refer to the “L3.9.1.5 Setting of cutoff frequency”, and “L3.9.1.6 Setting of cutoff frequency change rate”).
- LFO function is included. (For more details, refer to the “L3.9.1.7 LFO MODE”.
- Resonance setting can be made. (For more details, refer to the “L3.9.1.4 Resonance (Q)”.

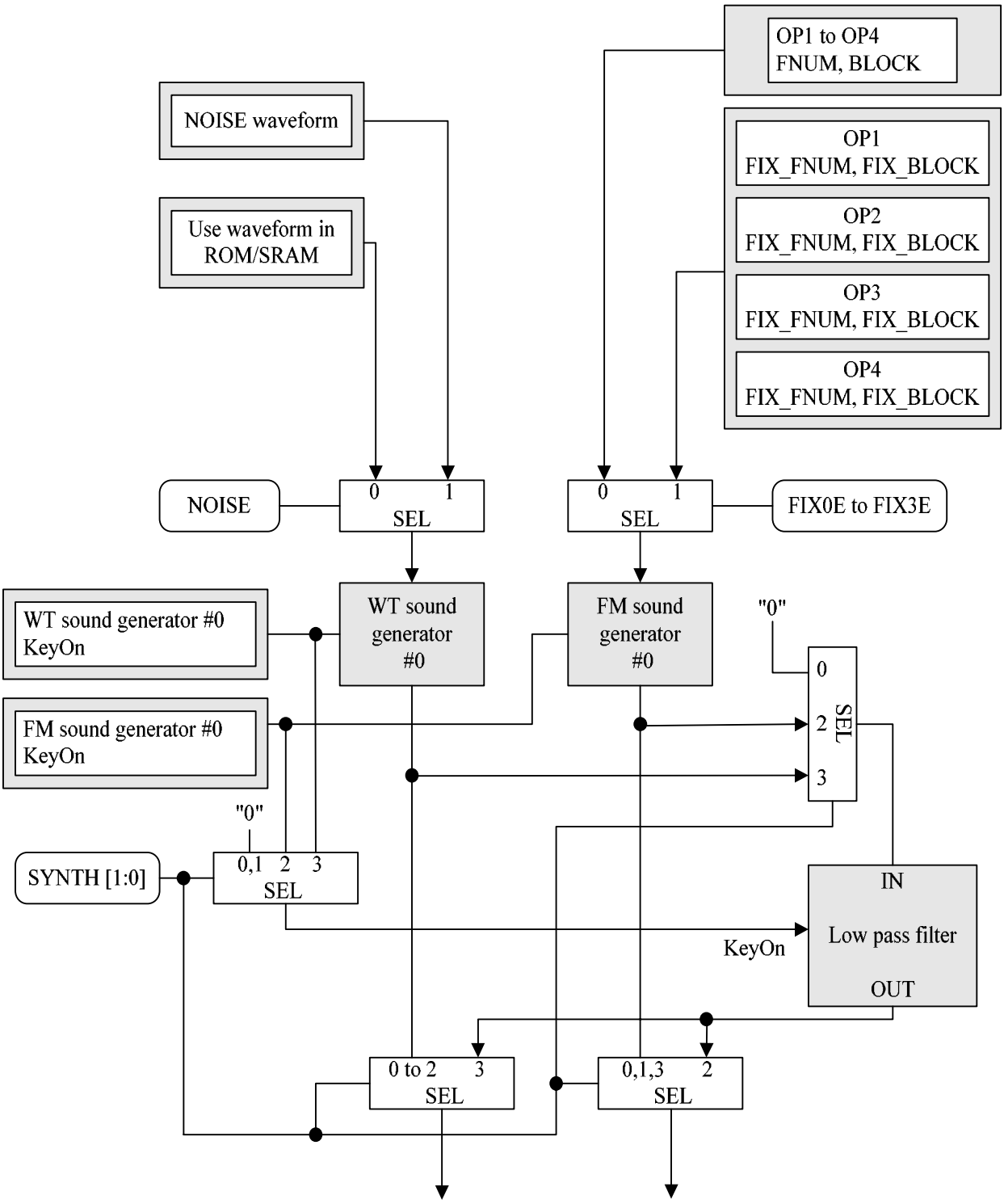
Functions around low pass filter

- Either FM sound generator #0 or WT sound generator #0 can be inputted to low pass filter.
- FIX function can be used only for FM sound generator #0. (For more details, refer to the “L0.0.0L3.9.1.11 FIX function“.

  Noise waveform can be outputted only for WT sound generator #0. (For more details, refer to the “L3.9.1 Register’s Explanation”.

Configurations of AL Synthesizer

I/O Configuration for Low Pass Filter



To the volume circuit of each sound generator

Supplementary Information about the Configuration Diagram

- Either FM Sound Generator #0 or WT Sound Generator #0 is inputted to low pass filter.

  It is selected with SYNTH bit.
- FM Sound Generator #0 has a function called FIX that is used to set FNUM and BLOCK for individual FM operators.

  SYNTH bit and FIX function operates independently.
- WT Sound Generator #0 has a function called NOISE that is used to change the output of WT Sound Generator #0 noise to one (with EG). It is selectable.

  SYNTH bit and noise selection operates independently.
- After outputting from low pass filter, the data for all Sound generators are mixed and outputted through the volume control.

L3.9.1 Register's Explanation

Control register #537 to #563 are registers to control AL synthesizer.

C Address	W/R	D6	D5	D4	D3	D2	D1	D0	
# 537	W/R	LPFCLR	"0"	SYNTH		"0"	NOISE	"0"	LPF control
# 538	W/R	"0"	"0"	Q					Resonance setting
# 539	W/R	"0"	Fc0(H)						Cut off frequency setting
# 540	W/R	Fc0(L)							
# 541	W/R	"0"	Fc1(H)						
# 542	W/R	Fc1(L)							
# 543	W/R	"0"	Fc2(H)						
# 544	W/R	Fc2(L)							
# 545	W/R	"0"	Fc3(H)						
# 546	W/R	Fc3(L)							
# 547	W/R	"0"	Fc4(H)						
# 548	W/R	Fc4(L)							
# 549	W/R	"0"	"0"	FAR					Change rate setting
# 550	W/R	"0"	"0"	FDR					
# 551	W/R	"0"	"0"	FSR					
# 552	W/R	"0"	"0"	FRR					
# 553	W/R	LFO DEPTH			LFO MODE	LFO FREQ			LFO setting
# 554	W/R	FIX0E	FIX_BLOCK0			FIX_FNUM0 (H)			FIX setting
# 555	W/R	FIX_FNUM0 (L)							
# 556	W/R	FIX1E	FIX_BLOCK1			FIX_FNUM1 (H)			
# 557	W/R	FIX_FNUM1 (L)							
# 558	W/R	FIX2E	FIX_BLOCK2			FIX_FNUM2 (H)			
# 559	W/R	FIX_FNUM2 (L)							
# 560	W/R	FIX3E	FIX_BLOCK3			FIX_FNUM3 (H)			
# 561	W/R	FIX_FNUM3 (L)							
# 562	W/R	LFORST	FcOFFSET(H)						Offset setting
# 563	W/R	FcOFFSET(L)							

L3.9.1.1 LPFCLR

Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 537	W/R	LPFCLR	"0"	SYNTH		"0"	NOISE	"0"

This is the bit to initialize a low pass filter operation section.
Writing "1" initializes the section. After ending the initialization, hardware automatically returns the state to "0".
(This means that writing back to "0" is not necessary.)
About 300ns is necessary to initialize the section.

In the following cases, be sure to initialize the section.

- When the value of SYNTH bits is rewritten (before a pronunciation start)
- When music reproduction is completed. (However, only when the low path filter of AL sound source part was used)

L3.9.1.2 SYNTH

Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 537	W/R	LPFCLR	"0"	SYNTH		"0"	NOISE	"0"

This bit selects a Sound Generator that is inputted to low pass filter.

0: OFF (Input to low pass filter section is "0" at all times.)
1: Setting is prohibited.
2: FM sound generator #0
3: WT sound generator #0

Limitation when changing setting value

Change of setting during voice generation is prohibited. Changing the setting during voice generation may cause generation of noise.

L3.9.1.3 NOISE

Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 537	W/R	LPFCLR	"0"	SYNTH		"0"	NOISE	"0"

It is able to make the waveform of the WT Sound Generator #0 a noise.

0: Normal operation (Voice data that is stored in the built-in ROM or playback waveform that is registered in SRAM)
1: Noise waveform

SYNTH bit and noise setting operates independently.
(It can be made into noise waveform without inputting WT sound generator #0 to low pass filter.)

Limitation when changing setting value

Change of setting during voice generation is prohibited. Changing the setting during voice generation may cause generation of noise.

L3.9.1.4 Resonance (Q)

Default 7'h00

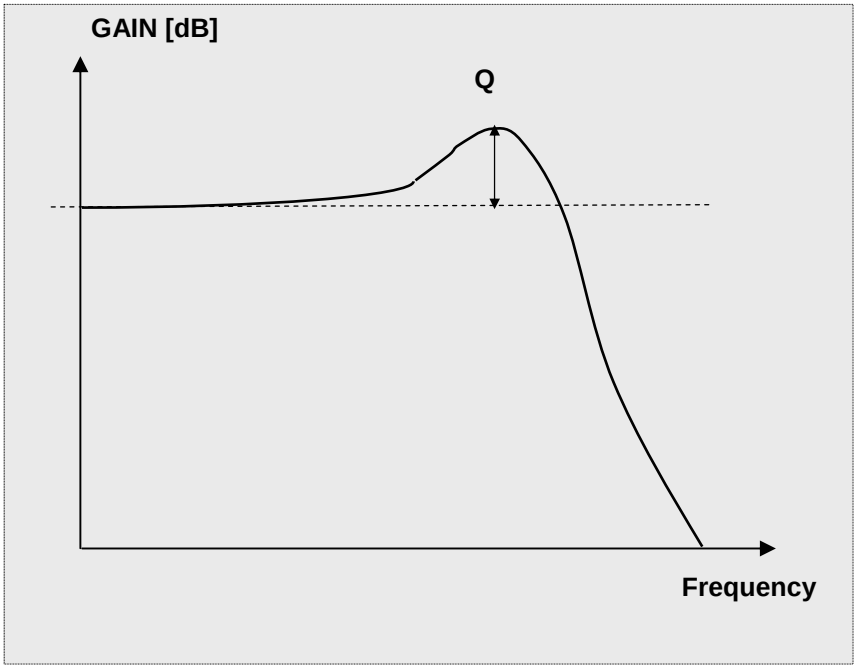
C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 538	W/R	"0"	"0"	Q				

It is able to set a resonance of filter in the range from -3.00 to +20.25 dB.

The relationship between the setting value and Q [dB] is described below.
Q [dB] = 0.75 × register setting value - 3
The value of Q can be changed during voice generation.

(Example of setting)

Setting value Q	GAIN [dB]	Setting value Q	GAIN [dB]
31	+20.25	6	+1.50
28	+18.00	4	± 0.00
24	+15.00	3	-0.75
16	+9.00	2	-1.50
12	+6.00	1	-2.25
8	+3.00	0	-3.00



What is resonance function?

Refer to the "L1.7 AL (Analog Lite) Synthesizer".

L3.9.1.5 Setting of cutoff frequency

Default 7'h00

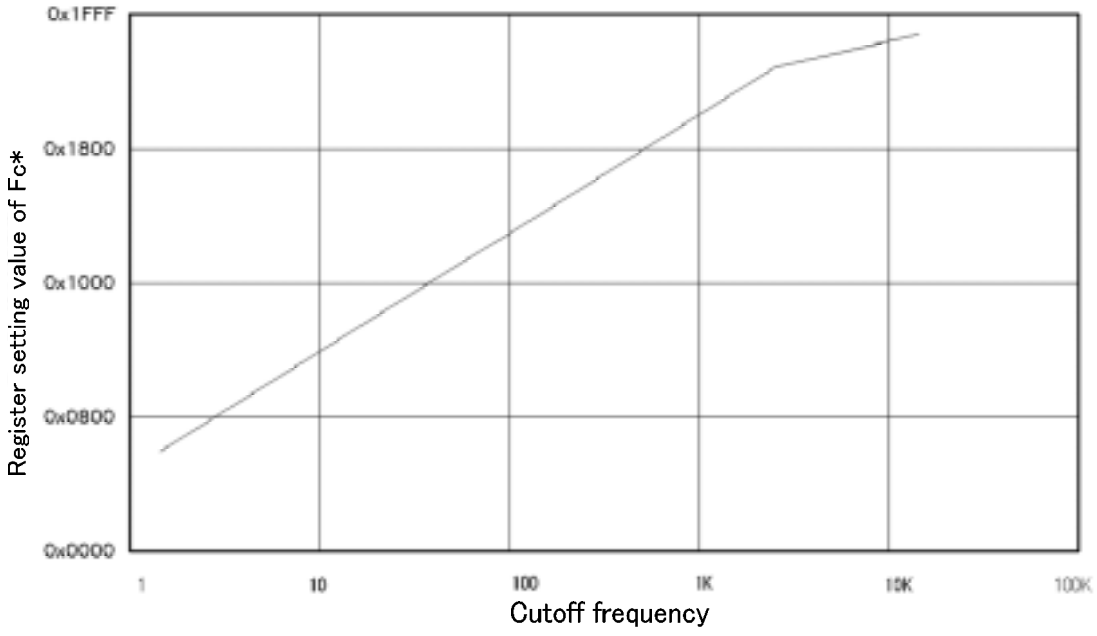
C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 539	W/R	"0"	Fc0(H)					
# 540	W/R	Fc0(L)						
# 541	W/R	"0"	Fc1(H)					
# 542	W/R	Fc1(L)						
# 543	W/R	"0"	Fc2(H)					
# 544	W/R	Fc2(L)						
# 545	W/R	"0"	Fc3(H)					
# 546	W/R	Fc3(L)						
# 547	W/R	"0"	Fc4(H)					
# 548	W/R	Fc4(L)						

# 562	W/R	LFORST	FcOFFSET(H)
# 563	W/R	FcOFFSET(L)	

Fc * : These are registers to set cutoff frequency.
13 bits in total including Fc * (H) and Fc * (L) become the setting value of the register.
(* represents a numeral from 0 to 4 or OFFSET.)
FcOFFSET is a register for setting offset value for Fc0 to Fc4.

- Fc0: cutoff frequency at the start of KeyOn
- Fc1: cutoff frequency at the end of attack (at the start of decay)
- Fc2: cutoff frequency at the end of decay (at the start of sustain)
- Fc3: cutoff frequency at the end of sustain
- Fc4: cutoff frequency at release
- FcOFFSET: Offset value setting to the cutoff frequency set by Fc0-Fc4

As a result of addition of FcOFFSET and Fc0 to Fc4, It becomes the final setting value of cutoff frequency.
The correspondence between the cutoff frequency of filter and register setting value Fc0 to Fc4 is similar to shown in the following graph.



What is addition of FcOFFSET and Fc0 to Fc4?

For example, When FcOFFSET is 13’h0100, and Fc0 is 13’h1400, the final cutoff frequency at KeyON is 13’h1500. (13’h0100 + 13’h1400)

The addition result of FcOFFSET and Fc* has restriction.

In the addition result of FcOFFSET and Fc*, please be sure to be set to 13 'h0008- 13' h1FF8.

The setting value can be changed during voice generation.

For example, when change of Fc2 → Fc3 occurs at the rate of FSR, and then the value of Fc3 is changed, it changes to the changed value of Fc3 at the rate of FSR.

L3.9.1.6 Setting of cutoff frequency change rate

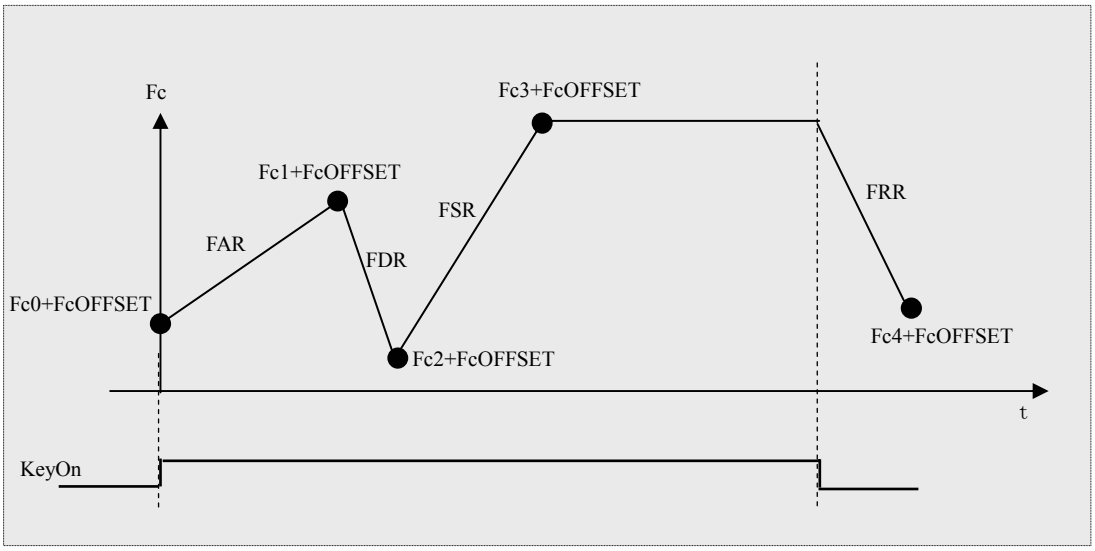
Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 549	W/R	"0"	"0"	FAR				
# 550	W/R	"0"	"0"	FDR				
# 551	W/R	"0"	"0"	FSR				
# 552	W/R	"0"	"0"	FRR				

F * R : These registers are for setting the change rate of cutoff frequency.
It consists of four types, FAR, FDR, FSR and FRR.

- FAR: cutoff frequency change rate in attack state (time for changing from Fc0 to Fc1)
- FDR: cutoff frequency change rate in decay state (time for changing from Fc1 to Fc2)
- FSR: cutoff frequency change rate in sustain state (time for changing from Fc2 to Fc3)
- FRR: cutoff frequency change rate in release state (time for changing from KeyOn="0" to Fc4)

The following figure shows the relationship between cutoff frequency and change rate.



The correspondence between the setting value of change rate and change time is shown in the following table. (Time for changing from 13'h0008 to 13'h1FF8)

Unit : ms

Setting value	Change time	Setting value	Change time
31	24.00	15	3584.00
30	33.60	14	4300.80
29	48.00	13	5376.00
28	67.20	12	6144.00
27	96.00	11	7168.00
26	134.40	10	8601.60
25	192.00	9	10752.01
24	268.80	8	12288.00
23	384.00	7	14336.00
22	537.60	6	17203.20
21	768.00	5	21504.00
20	1075.20	4	24576.00
19	1536.00	3	28672.00
18	2150.41	2	34406.40
17	2688.00	1	43008.00
16	3072.00	0	No change (∞)

L3.9.1.7 LFO MODE

Using LFO functions, it can change the present cutoff frequency to positive side or negative side at LFO period.
Triangular waveform and random waveform can be selected as the types of waveform that is changed to positive side or negative side.

Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 553	W/R	LFO DEPTH			LFO MODE	LFO FREQ		

# 562	W/R	LFORST	FcOFFSET(H)

0: Triangular waveform
1: Random waveform

L3.9.1.8 LFO DEPTH

It is the bit to select the width (depth) transition of cutoff frequency.
The following values are added to or subtracted from the present cutoff frequency value.
The correspondence between the setting value and the value to be added or subtracted is as follows.
The value of depth changes a little depending on the setting of LFO MODE bit.

Setting value	LFO MODE="0"	LFO MODE="1"
0	OFF	OFF
1	± 13'h0040	± 13'h003F
2	± 13'h0080	± 13'h007F
3	± 13'h0100	± 13'h00FF
4	± 13'h0200	± 13'h01FF
5	± 13'h0400	± 13'h03FF
6	± 13'h0800	± 13'h07FF
7	± 13'h1000	± 13'h0FFF

L3.9.1.9 LFO FREQ

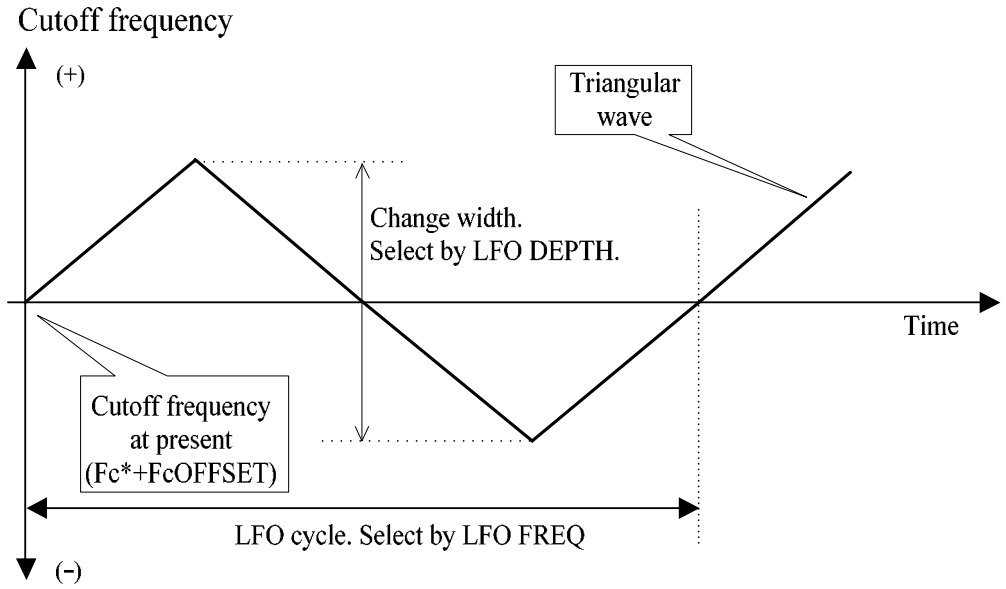
It is the bit to select the frequency of LFO.
However, when LFO MODE bit = 1 (when random waveform is selected), frequency is doubled.

0 : 0.18 Hz 1 : 0.37 Hz
2 : 0.73 Hz 3 : 1.83 Hz
4 : 4.03Hz 5 : 6.96Hz
6 : 11.35Hz 7 : 15.01Hz

L3.9.1.10 LFO RST

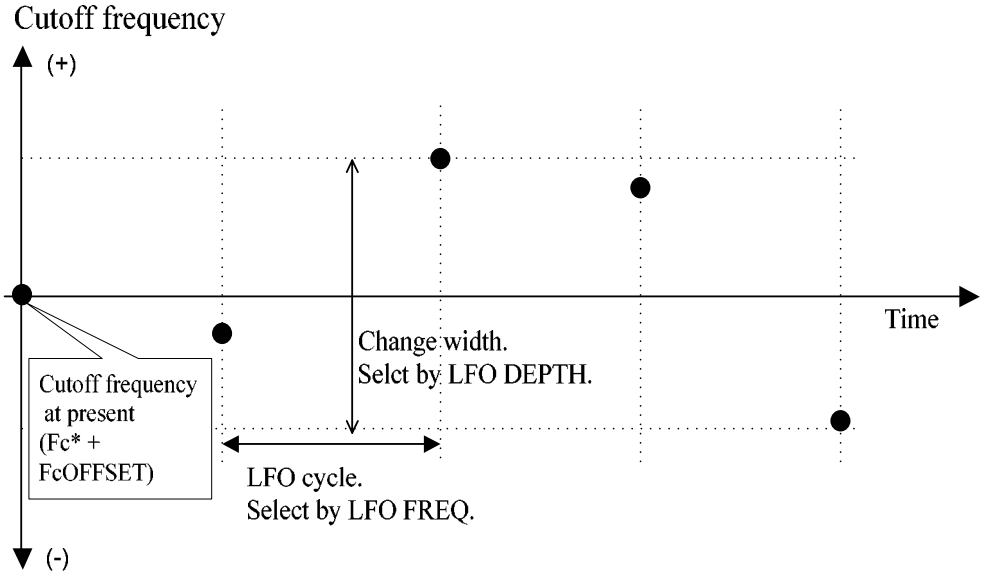
"1" is set when reset of LFO circuit is needed.
Note, it is unnecessary to rewrite the bit to "0" because hardware automatically returns this bit to "0".
Normally, LFO circuit is a free-running circuit; however, for the voices with deep LFO DEPTH and/or slow LFO FREQ, they may scarcely be generated when KeyOn timing comes, at the same time cutoff frequency is effective. If such voice occurs, set this bit to "1", by performing key-on it is able to make the LFO phase and the start of voice generation coincident to some extent.

The Situation of the Cutoff Frequency Change at the time of Using a Triangular Wave

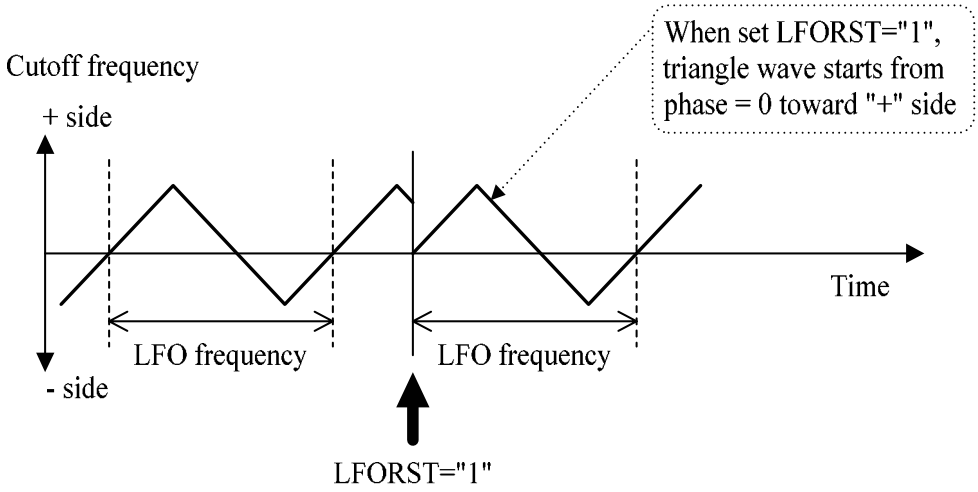


State of Change of Cutoff Frequency when Random Waveform is used

The difference from previous figure is only the change of waveform from triangular one to random one.
The settings of Fc * and F * R are valid also when using random waveform.
When using random waveform, cutoff frequency varies at random within the range of the change width for each LFO period to the present cutoff frequency.



Behavior of LFORST



L3.9.1.11 FIX function

Usually, the values of FNUM and BLOCK of FM section are common to all operators.
By using FIX function, independent values of FNUM and BLOCK can be used for individual operators.
The frequency ratio of between FM carrier and operator can be made non-integer, allowing creating non-integer harmonic voices.

Default 7'h00

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 554	W/R	FIX0E	FIX_BLOCK0			FIX_FNUM0 (H)		
# 555	W/R	FIX_FNUM0 (L)						
# 556	W/R	FIX1E	FIX_BLOCK1			FIX_FNUM1 (H)		
# 557	W/R	FIX_FNUM1 (L)						
# 558	W/R	FIX2E	FIX_BLOCK2			FIX_FNUM2 (H)		
# 559	W/R	FIX_FNUM2 (L)						
# 560	W/R	FIX3E	FIX_BLOCK3			FIX_FNUM3(H)		
# 561	W/R	FIX_FNUM3 (L)						

FIX * E : These bits select whether independent values of FNUM and BLOCK are set for individual Operators or not.
This function is limited only for the FM Sound Generator #0.

0 : Values of FNUM and BLOCK set with Control registers #3 to #4 are used.
1 : FIX_FNUM * and FIX_BLOCK * set with #554 to #561 are used.

FIX_FNUM *, FIX_BLOCK * :

These registers are used to set the values of FNUM and BLOCK that are used when FIX*E bit is "1".
"*" represents numbers from 0 to 3, and the numbers correspond to "FM operator number-1".
When FIX_FNUM*(L) is written, it becomes valid. Make sure to transfer FIX_BLOCK*, FIX_FNUM*(H) and FIX_FNUM(L) as one packet.

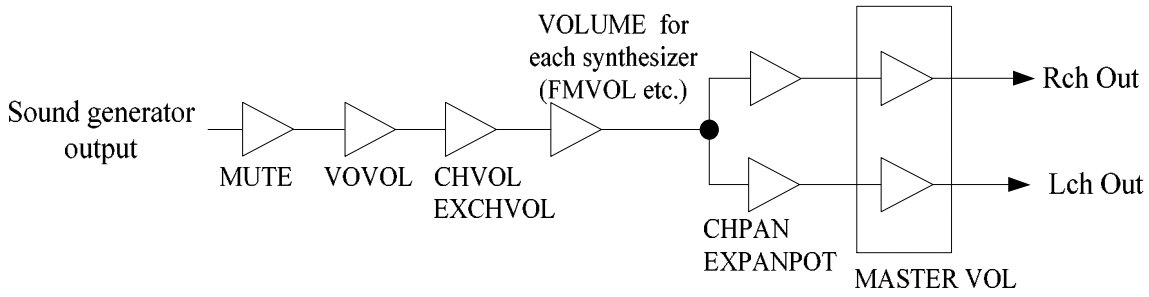
Effective range of FIX bit

FIX bit can change only FMUM and BLOCK.
For MULTI, DT, LFO, and BO, setting values that are defined at the voice data side are used.

L3.10 Volume Functions

Circuit Structure (Digital section)

The following figure shows a volume circuit for one tone of Sound Generator.



Each Sound generator data are added at the subsequent stages of RchOut and LchOut, and the data are sent to DAC.
The limiter processing (overflow and underflow) in the addition is performed for the data which are produced by adding all Sound generator data.

L3.10.1 Register's Explanation

L3.10.1.1 MUTE

It is a bit for the set of MUTE. "1": MUTE "0": release of MUTE
The specifications of both MUTE and VOVOL are common among any Sound generator.
However, HV Sound Generator has no VOVOL.
MUTE has "Interpolation function".

L3.10.1.2 VOVOL

It is a bit to set volume of each Sound generator. The volume can be obtained with the following formula.

$$GAIN\ [dB] = 40\ Log_{10}\ ((VOVOL \times 4 + 3)\ /127)$$

However, there is a little difference only at the time of VOVOL="1" setup.
The correspondence between the setting values of VOVOL and actual volume is shown in the following table.
VOVOL has no "interpolation function" that is described afterward.

Setting value	Volume (dB)	Setting value	Volume (dB)
0	- ∞	16	-11.11
1	-47.77	17	-10.10
2	-42.49	18	-9.14
3	-37.10	19	-8.25
4	-33.00	20	-7.38
5	-29.67	21	-6.56
6	-26.91	22	-5.79
7	-24.49	23	-5.04
8	-22.38	24	-4.34
9	-20.51	25	-3.63
10	-18.82	26	-2.98
11	-17.27	27	-2.34
12	-15.84	28	-1.71
13	-14.53	29	-1.13
14	-13.31	30	-0.56
15	-12.19	31	0

L3.10.1.3 CHVOL, EXCHVOL

These are the bits to set volume on each channel.
CHVOL is assigned to the Control Registers #192 to #207.
The expanded channel section has EXCHVOL of which specifications are the same as CHVOL.
It is assigned to the Control Register #483.

Default 8'h60 (CHVOL=5'b1_1000)

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 192 ~ #207	W/R	CHVOL#0 ~ CHVOL#15					"0"	DRCT

Default 8'h60

C_Address	WR	D6	D5	D4	D3	D2	D1	D0
# 483	WR	EXCHVOL					"0"	DRCT

The volume can be obtained with the following formula.

$$GAIN\ [dB] = 40\ Log_{10}\ ((setting\ value \times 4 + 3)\ /127)$$

The relationship between the setting value and volume is the same as VOVOL.

L3.10.1.4 FMVOL, FMSHIFT

Volumes for each synthesizer are assigned to the Intermediate Registers #41 to #44

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#41	W/R	FMVOL					"0"	FMSHIFT	
#42	W/R	WTVOL					"0"	WTSHIFT	
#43	W/R	STMVOL					"0"	STMSHIFT	
#44	W/R	HVVOL					"0"	HVSHIFT	

FMVOL: It is a volume setup to all FM Sound Generators. The relation between a setting value and volume is as same as CHVOL.

FMSHIFT: It is a bit for GAIN setting of all FM Sound Generators.
GAIN [dB] = 6 × FMSHIFT.

L3.10.1.5 WTVOL, WTSHIFT

WTVOL: It is a volume setup for all WT Sound Generators. The relation between a setting value and volume is the same as CHVOL.

WTSHIFT: It is the bit for GAIN setting of all WT Sound Generators.
GAIN [dB] = 6 × WTSHIFT

L3.10.1.6 STMVOL, STMSHIFT

STMVOL: It is a volume setup for all STM Sound Generators. The relation between a setting value and volume is the same as CHVOL.

STMSHIFT: It is the bit for GAIN setting of all Stream Playback Sound Generators.
GAIN [dB] = 6 × STMSHIFT

L3.10.1.7 HVVOL, HVSHIFT

HVVOL: It is a volume setup for HV Sound Generator. The relation between a setting value and volume is the same as CHVOL.

HVSHIFT: It is the bit for GAIN setting of HV Sound Generator.
GAIN [dB] = 6 × HVSHIFT

L3.10.1.8 MASTER VOLUME

This is a register that performs a master volume setting on digital side.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#39	W/R	MASTER VOLL					"0"	MASTER L SHIFT	
#40	W/R	MASTER VOLR					"0"	MASTER R SHIFT	

MASTER VOLL : Bit for setting a master volume on L channel side
GAIN [dB] = 40 Log $_{10}$((MASTER VOLL × 4 + 3) /127)

MASTER VOLR : Bit for setting a master volume on R channel side
The correspondence between the setting value and volume is the same as that of MASTER VOLL.

MASTER L SHIFT : Bit for setting GAIN on L channel side
The correspondence between the setting value and shift amount is the same as that of FMSHIFT.

MASTER R SHIFT : Bit for setting GAIN on R channel side
The correspondence between the setting value and shift amount is the same as that of FMSHIFT.

L3.10.1.9 MVSEL

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#55	W/R	SV_MUTE		SV_CHV	SV_PAN	MVSEL	NOP2E	FINT	DADJT

MVSEL can choose the Sound Generator of which MASTER VOL becomes valid.

"1" : The setting value in the #39 and #40 becomes valid only for FM Sound Generator, WT Sound Generator, and Stream playback. As for HV, the MASTER VOL section is fixed to 0dB(1 time).

"0" : The setting value in the #39 and #40 becomes valid for FM Sound Generator, WT Sound Generator, Stream playback, and HV voice.

L3.10.1.10 CHPAN, EXPANPOT

These registers are for setting Panpot on each individual channel.
They are assigned to the Control registers #208 to #223.
The expanded channel section has EXPANPOT with the same specifications that are assigned to the Control register #484. CHPAN has “Interpolation function” that is described later, but EXPANPOT does not have “Interpolation function”.

Default 8’h3C

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 208 ~ #223	W/R	CHPAN#0 ~ CHPAN#15					“0”	DRCT

Default 8’h3C

C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 484	W/R	EXPANPOT					“0”	“0”

These registers are for setting balance between the right and left channels.

Lch_GAIN [dB] = 20 Log_{10}(Cos(π / 2 × CHPAN × 63.5 / 15 / 127)) (CHPAN setting value: 0 to 15)
= 20 Log_{10} (Sin(π / 2 × (31 – CHPAN) × 63.5 / 15 / 127)) (CHPAN setting value: 16 to 31)

Rch_GAIN [dB] = 20 Log_{10} (Sin(π / 2 × CHPAN × 63.5 / 15 / 127)) (CHPAN setting value: 0 to 15)
= 20 Log_{10} (Cos(π / 2 × (31 – CHPAN) × 63.5 / 15 / 127)) (CHPAN setting value: 16 to 31)

EXPANPOT has same specifications.

The relationship between the setting value and volume is shown in the following table.

Setting value	Lch (dB)	Rch (dB)	Setting value	Lch (dB)	Rch (dB)
0	0	- ∞	16	-3.010	-3.010
1	-0.000	-25.624	17	-3.490	-2.579
2	-0.048	-19.615	18	-4.023	-2.190
3	-0.108	-16.113	19	-4.616	-1.841
4	-0.192	-13.642	20	-5.278	-1.528
5	-0.301	-11.740	21	-6.021	-1.249
6	-0.436	-10.200	22	-6.859	-1.002
7	-0.597	-8.913	23	-7.814	-0.785
8	-0.785	-7.814	24	-8.913	-0.597
9	-1.002	-6.859	25	-10.200	-0.436
10	-1.249	-6.021	26	-11.740	-0.301
11	-1.528	-5.278	27	-13.642	-0.192
12	-1.841	-4.616	28	-16.113	-0.108
13	-2.190	-4.023	29	-19.615	-0.048
14	-2.579	-3.490	30	-25.624	-0.000
15	-3.010	-3.010	31	- ∞	0

[Note]

When the PANPOT setting value is “0” or “31” (one side is – ∞, and the other side is 0dB), the level of output of EQ1 pin becomes half of 0dB side (– 6dB); because of,

Configuration of the Analog Block: Output of EQ1 = (Output of DAC Lch × 1/2) + (Output of DAC Rch × 1/2)

In addition, the above explanation is also able to be applied to the output of HPOUT-L/MONO pin at monaural setting (MONO=1) of HPOUT.

L3.10.1.11 PE

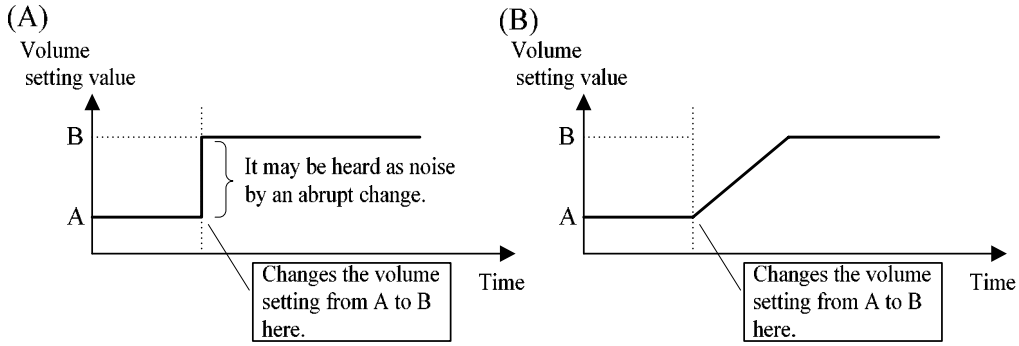
This bit selects whether CHPAN setting designated by the channel parameters is used, or PANPOT value designed in the voice parameters is used.
"1" selects PANPOT setting value in voices.
"0" selects CHPAN value designated by channel parameters.

L3.10.1.12 PANOFF

This bit turns off Panpot.
Panpot function is disabled for voices of which PANOFF bit is "1", and 0dB is set for both Lch and Rch.
Operation of this bit is given priority over PE or PANPOT setting value.
"0" enables Normal operation. The operation follows PE or PANPOT setting value.

L3.10.2 Interpolation Functions

When varying the setting value of volume, the amount of the change may cause noise in the case shown in the following figure (A). The occurrence of the noise can be suppressed by changing the setting value of volume smoothly as shown in (B). The mechanism that makes the change smooth is called “Interpolation function”.



The Interpolation function is provided by the following three volume setting section.

- CHVOL and EXCHVOL
- CHPAN
- MUTE

The Interpolation function has a setting of interpolation time and a setting of Interpolation function On/Off.
For CHVOL, EXCHVOL, and CHPAN, the setting of interpolation can be made for individual channels.
For MUTE, the setting of interpolation can be made for the Sound Generators.
The setting of Interpolation function is performed with the Intermediate Register #55 and DRCT that is in D0 bit of CHVOL, EXCHVOL, and CHPAN setting.

Default 8’h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#55	W/R	SV_MUTE		SV_CHV	SV_PAN	MVSEL	NOP2E	FINT	DADJT

L3.10.2.1 SV_MUTE

This bit sets an interpolation speed of MUTE.

0 : No interpolation
1 : Prohibited
2 : 128fs (fs [Hz] : sampling frequency. In the case of fs=48000, it becomes 2.7 ms.)
3 : 256fs (fs [Hz] : sampling frequency. In the case of fs=48000, it becomes 5.3 ms.)

When MUTE has been canceled, “No interpolation” is set at all times.

L3.10.2.2 SV_CHV

This bit sets an interpolation speed of CHVOL.

“0” : 256fs
“1” : 1024fs (In the case of fs=48000, it becomes 21.3 ms.)

L3.10.2.3 SV_PAN

This bit sets an interpolation speed of CHPAN.

“0” : 256fs
“1” : 1024fs

L3.10.2.4 DRCT

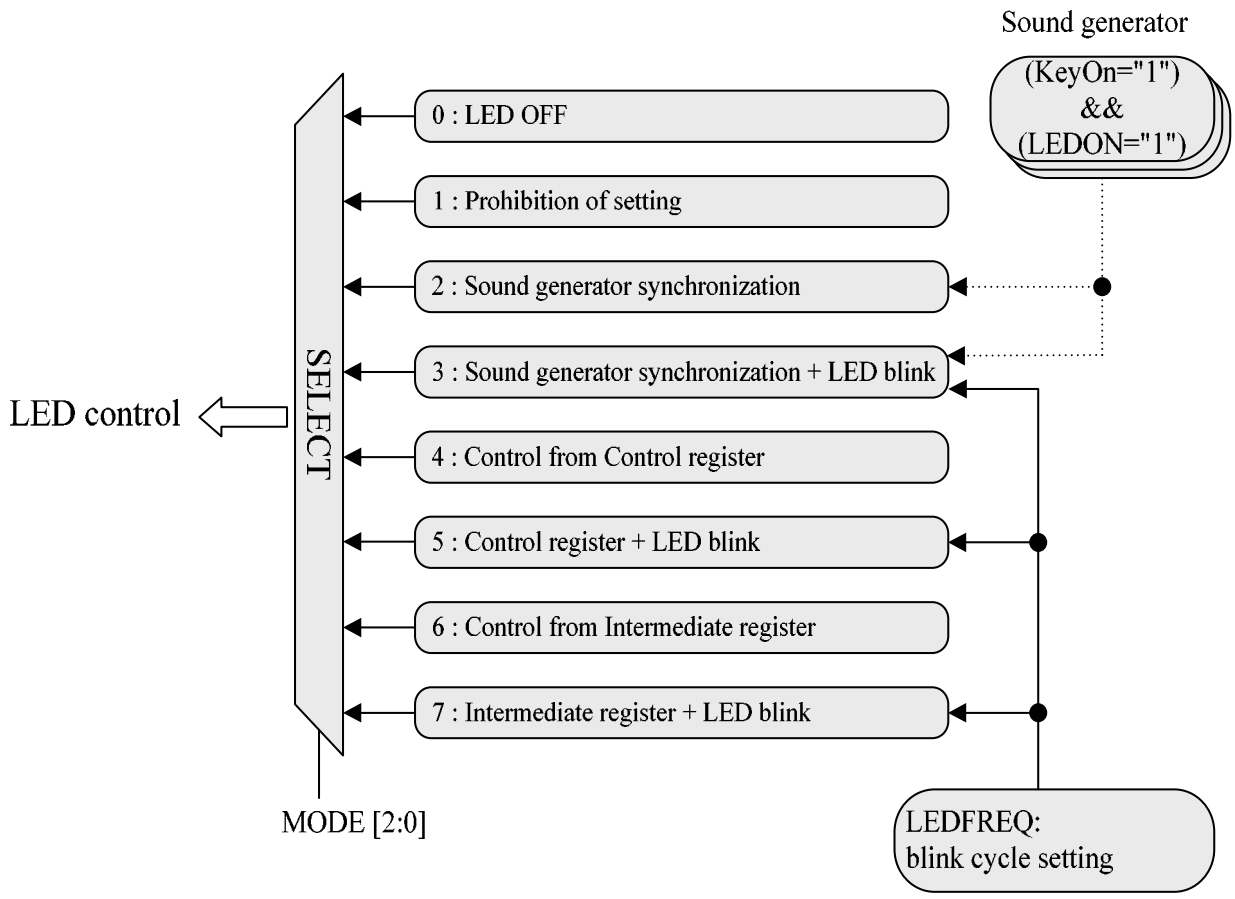
“0” : No interpolation.
“1” : The operation follows the interpolation designated by Intermediate register #55.

L3.11 LED, Vibrator control

This product is able to control external LED and vibrators.

- L3.11.1 Control from Intermediate Register (LED)
- L3.11.2 Control from Control Register (LED)
- L3.11.3 Control from Intermediate Register (Vibrator)
- L3.11.4 Control from Control Register (Vibrator)

Circuit Structure (LED)



L3.11.1 Control from Intermediate Register (LED)

External LED can be controlled from the Intermediate registers #11 and #12.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#11	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	MIDLED
#12	W/R	"0"	LED FREQ			"0"	LED MODE		

L3.11.1.1 LED MODE

This bit designates the LED control mode.
The correspondence between the setting value and control mode is as described below.
In the Sound Generator synchronization mode, LED is turned on if sound generator of which both KeyOn and LEDON bits is "1" exists, LED is turned off if not.
This operation applies to all Sound generators including FM, WT, HV, and Stream playback.

0 : LED is off.
1 : Setting is prohibited.
2 : Sound generator synchronization
3 : Sound generator synchronization + blinking control
4 : Direct designation of LED from Control register
5 : Direct designation of LED from Control register + blinking control
6 : Direct designation from Intermediate register (D0 bit of #11)
7 : Direct designation from Intermediate register + blinking control

L3.11.1.2 LED FREQ

This bit designates the blinking periods.

0 : 18Hz
1 : 16Hz
2 : 12Hz
3 : 8Hz
4 : 4Hz
5 to 7 : Setting is prohibited.

L3.11.1.3 MIDLED

This bit directly controls the operation (directly designates ON/OFF).

"0": LED is turned off.
"1": LED is turned on.

L3.11.2 Control from Control Register (LED)

LED is controlled at the Control register #476.

Default 8'h00

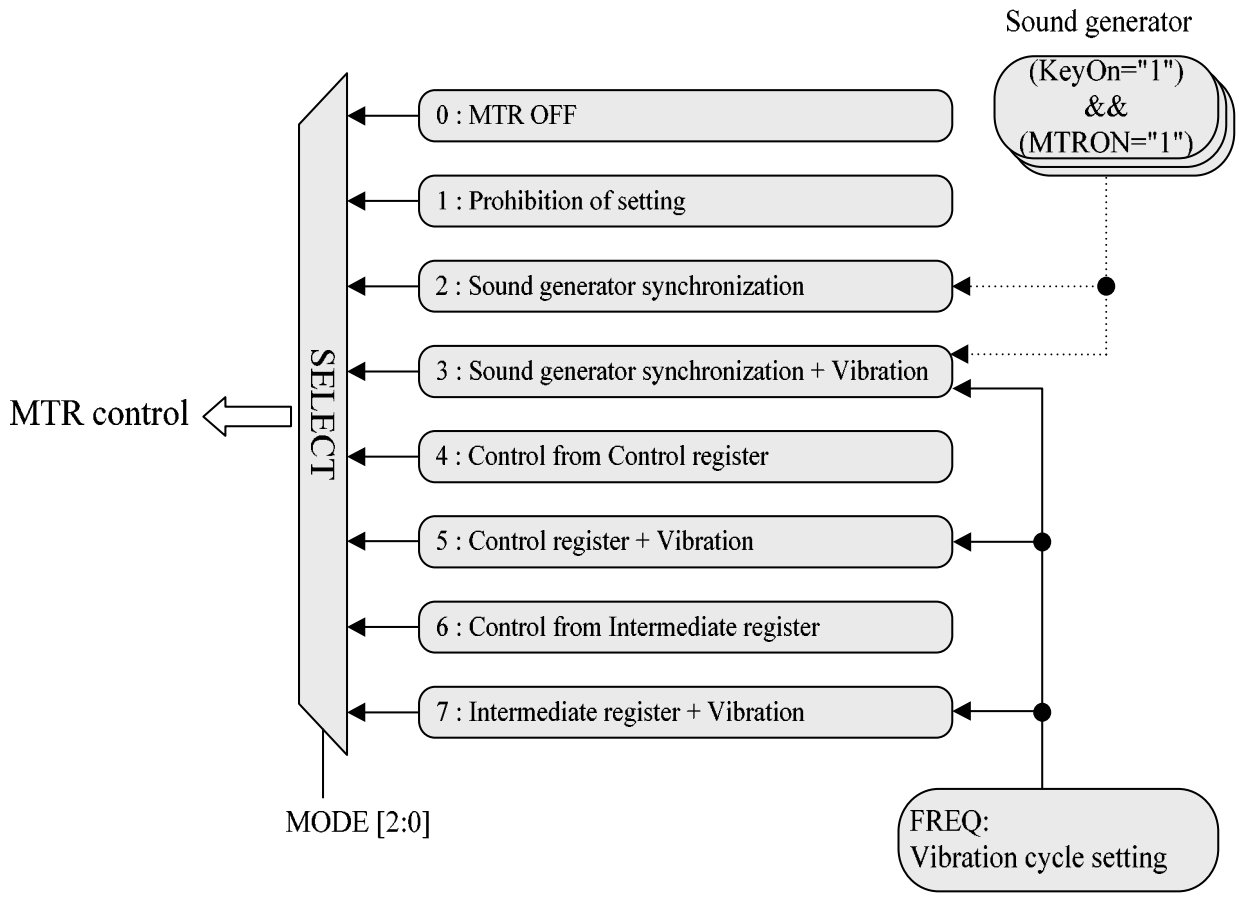
C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 476	W/R	"0"	"0"	"0"	"0"	"0"	"0"	LED

LED: This bit is used to control LED directly from Control register.

"0": LED is turned off.
"1": LED is turned on.

Circuit structure (Vibrator)

This is a control function for the vibrator that is connected externally to LSI.



L3.11.3 Control from Intermediate Register (Vibrator)

This is a register for controlling vibration of the vibrator that is connected externally to LSI.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#13	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	MIDMTR
#14	W/R	"0"	MTR FREQ			"0"	MTR MODE		

L3.11.3.1 MTR MODE

This bit is for designating a method of controlling the external vibrator.
The correspondence between the setting value and control method is described below.
In the Sound generator synchronization mode, the vibrator is turned on if sound generator of which both KeyOn and MTRON bits is "1" exists,, the vibrator is turned off if not.
This operation applies to all Sound generators including FM, WT, HV, and Stream playback.

0 : Off (no vibration)
1 : Setting is prohibited.
2 : Sound generator synchronization
3 : Sound generator synchronization + vibration frequency control
4 : Vibrator direct designation from control register
5 : Vibrator direct designation from control register + vibration frequency control
6 : Direct designation from Intermediate register #13 MTR bit
7 : Direct designation from Intermediate register #13 MTR bit + vibration frequency control

L3.11.3.2 MTR FREQ

This bit designates the vibration frequency.

0 : 2.25Hz
1 : 2.00Hz
2 : 1.50Hz
3 : 1.00Hz
4 : 0.50Hz
5 to 7 : Setting is prohibited.

L3.11.3.3 MIDMTR

This bit is used to control a vibrator directly from the Control register (directly controls ON/OFF).

"0" : Vibration disabled
"1" : Vibration enabled

L3.11.4 Control from Control Register (Vibrator)

This register controls an external vibrator with the Control register #477.

Default 8'h00

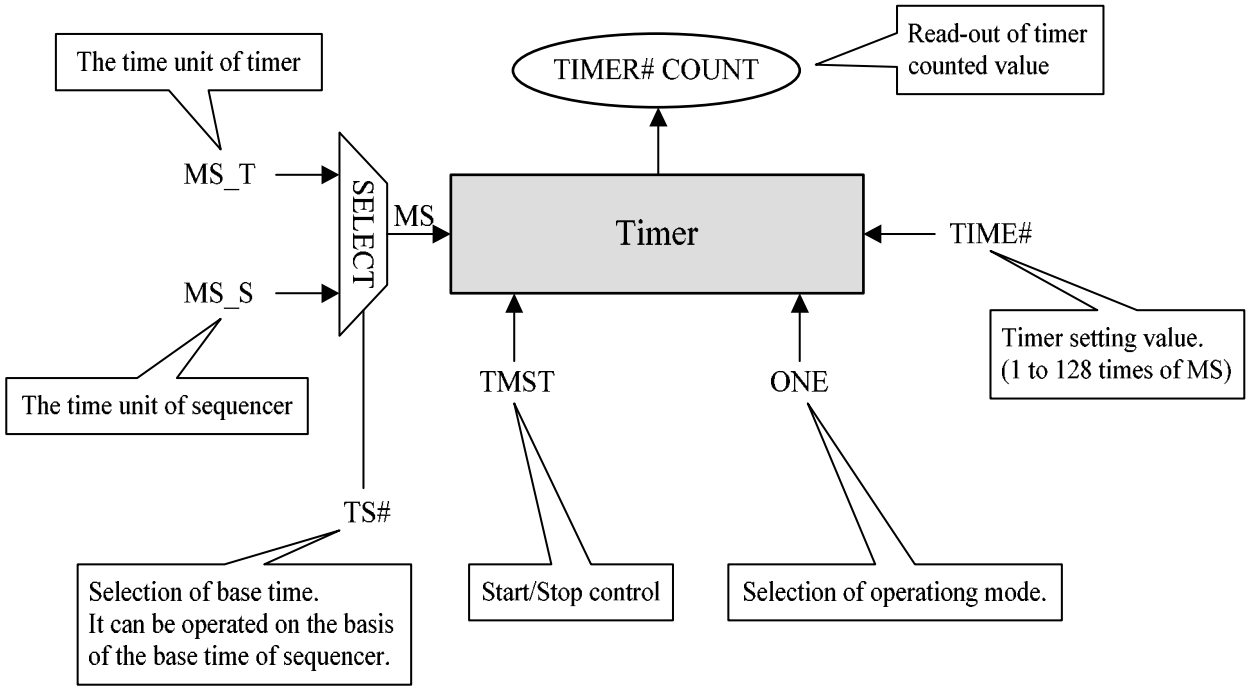
C_Address	W/R	D6	D5	D4	D3	D2	D1	D0
# 477	W/R	"0"	"0"	"0"	"0"	"0"	"0"	MTR

MTR: This bit is used to control vibrator directly from Control register.

"0" : Vibration disabled
"1" : Vibration enabled

L3.12 Timer

Three timers which can be controlled independently are equipped.
The following figure shows a diagrammatic illustration of the system for one timer and the parameter that control the timer.



Timer block diagram

L3.12.1 Timer Setting

The registers for setting the timer are assigned in the Intermediate registers #46 to #54.
The timer operates as a down counter. It is counted down from the value that is set with TIMER # of the Intermediate registers #47, #49, and #51, and an interrupt can be generated at the moment the count becomes "0".
ETM2, ETM1, and ETM0 bits of the Intermediate register #17 are used to valid / invalid the interrupt.
Interrupt flag registers are TM#2, TM#1, and TM#0 bits of the Intermediate register #0.

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#46	W/R	"0"	MS_T						
#47	W/R	"0"	TIMER #0						
#48	W/R	"0"	"0"	"0"	"0"	"0"	TS #0	ONE #0	TMST #0
#49	W/R	"0"	TIMER #1						
#50	W/R	"0"	"0"	"0"	"0"	"0"	TS #1	ONE #1	TMST #1
#51	W/R	"0"	TIMER #2						
#52	W/R	"0"	"0"	"0"	"0"	"0"	TS #2	ONE #2	"0"
#53	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	TMST#2A
#54	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	TMST#2B

L3.12.1.1 MS_T

This bit sets minimum time unit of the timer (0 to 127). 0 units mean "128".
Three timers use the same MS value.
Time unit [ms] = (MS_T) × 1 / (192fs / 342) (fs [Hz] : sampling frequency)
In the case of fs=48000, it becomes the maximum = 4.74 ms, and unit time = 0.037109 ms.

L3.12.1.2 TIMER#

This bit sets the timer setting value. "0" means "128".
Timer time = TIMER# × unit time MAX = approximately 0.607 sec

L3.12.1.3 TS#

This bit selects basic time.
"0" select the value of MS_T. "1" selects sequencer's basic time, MS_S.
(For the sequencer's basic time, refer to the "L3.2.1 Sequencer Setup.)

L3.12.1.4 ONE

This bit selects an operation mode of timer.
"1" selects one-shot (count ends when the count reaches to "0"), and "0" select continuous counting.

L3.12.1.5 TMST#

TMST#0: Timer #0 starting bit. "1" starts the timer and "0" stops it.
TMST#1: Timer #1 starting bit. "1" starts the timer and "0" stops it.
TMST#2A and TMST#2B : Timer #2 starting bits.
The timer starts when either TMST#2A or TMST#2B becomes "1" or both of them are "1".
The timer stops when both bits become "0".

The minimum unit time of MA-5 is a little different from MA-3.

Minimum unit time of MA-5 = 1 / (192fs / 342)
Minimum unit time of MA-3 = 1 / (9fs / 16) (In the case of fs=48000, It becomes 0.037037ms.)

L3.12.2 Read of Timer Count

Timer count can be read from the Intermediate registers #27 to #29.

Default 8'h7F

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#27	R	"0"	TIMER#0 COUNT						
#28	R	"0"	TIMER#1 COUNT						
#29	R	"0"	TIMER#2 COUNT						

The 3 bytes of count value are latched by the timing which specified the Intermediate register #27.

L3.13 Clock Control

L3.13.1 CKSEL setting (Synthesizer Section)

The clock ranging from 1.5MHz to 20MHz can be inputted from CLKI pin.
No input frequency is designated at power down, and it can be stopped.
As the amplitude of the input signal, CMOS input (V_{IH}=0.7*VDD or over, or V_{IL}=0.3*VDD or less), or TCXO (Temperature Compensated Crystal Oscillator) can be selected.
It is selected with CKSEL bit of Intermediate register #30.

#30 : Default 8'h0A, #31 : Default 8'h37

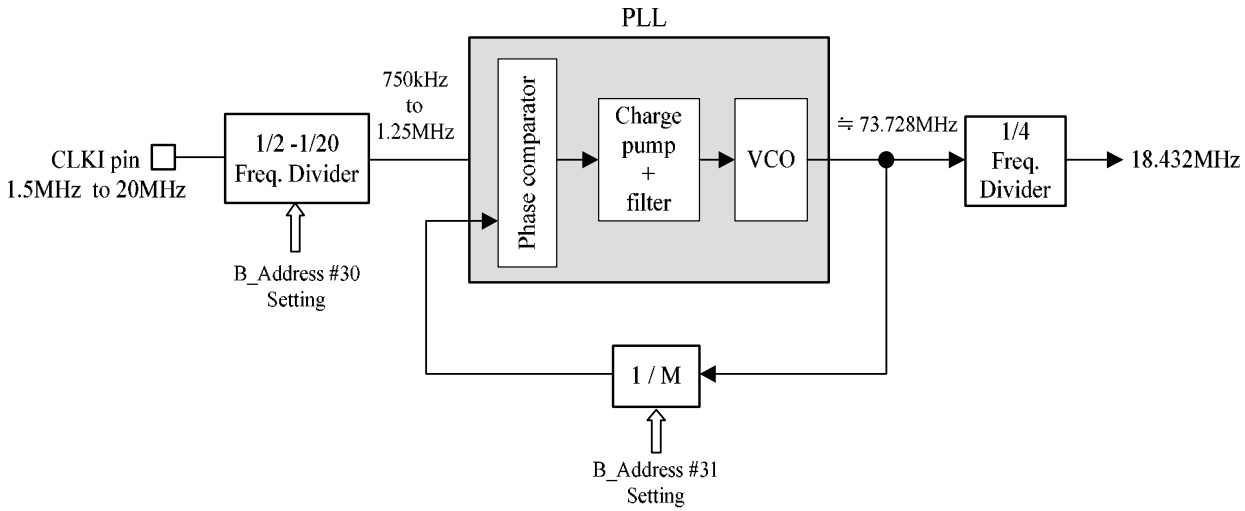
B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#30	W/R	CKSEL	"0"	"0"	ADJUST1				
#31	W/R	"0"	ADJUST2						

CKSEL:

"0" selects CMOS input
"1" selects TCXO input.
Default state (after initialization) is "0".

L3.13.2 ADJUST1, ADJUST 2 Setting (Synthesizer Section)

Though a clock ranging from 1.5MHz to 20MHz can be inputted from CLKI pin, it is necessary to set ADJUST for the Intermediate registers #30 and #31.



How to obtain a setting value of ADJUST1 and ADJUST2?

1. Calculate [input frequency of CLKI / setting value of #30 ADJUST1], and represent the result as “Y”.
   Make sure that the value of “Y” is in the range from 750 kHz to 1.25 MHz.
   Multiple “Y” may be obtained according to the frequency of CLKI.

2. Make the result of [Y × setting value of #31 ADJUST2] as close as possible to 73.728 MHz.
   Making the value closer to 73.728 MHz makes an error described later smaller.

Example of setup

When the frequency of the signal inputted from CLKI is 3 MHz, the setting value of ADJUST1 is “3” or “4”,

The values of “Y” become 1MHz and 750kHz.
When the value “Y” is 1 MHz, the value of ADJUST2 is 74.
When the value “Y” is 750 kHz, the value of ADJUST2 is 98.

L3.13.3 Error (Synthesizer Section)

Although settings of ADJUST1 and 2 are made, a little error occurs in most cases.
Although the error causes some difference in interval and tempo, it is not the level that affects the operation.
The difference is as shown below.

	Ideal value	Actual value
PLL output	73.728 [MHz]	Fp = (CLKI / setting value of #30) × setting value of #31 [MHz]
Sampling frequency	48.00 [kHz]	Fp / 1536 × 1000 [kHz]

Influence on Musical Interval

The difference of sampling frequency is equal to the difference of musical interval.
The difference of pitch and interval can be obtained by substituting “fs” obtained from the above calculation for the formula for calculating pitch (voice generation frequency) of FM synthesizer and WT synthesizer, “fs”.

Example : Playback frequency of WT section = 2 ^ (F / 1200) × fs × (LFO_PM) × BEND

The difference of musical interval (in cent) is given by the following formula.
Difference [cent] = $1200 \times \log_{10}(Fx / F0) / \log_{10}2$
F0 [Hz] : Reference frequency (=48000) Fx [Hz] : Frequency to compare

Influence on tempo

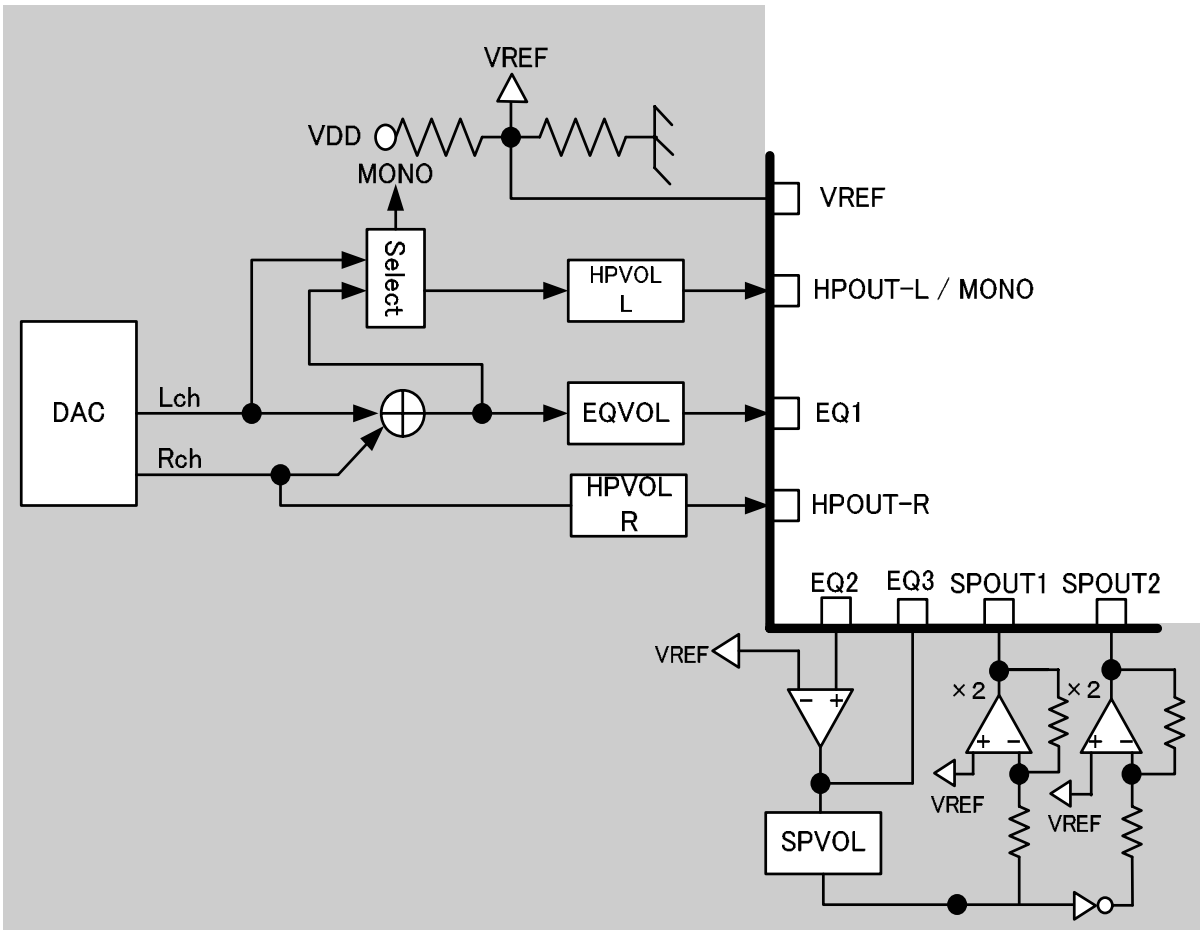
The minimum time unit of sequencer (MS_S: Intermediate registers #35 and #36) is determined based on “fs”.
Difference of “fs” affects tempo.

Influence on timer time

The minimum time unit of timer (MS_T: Intermediate register #46) is also determined based on “fs”.
Difference of “fs” affects timer time.

L3.14 Analog functions

The organization of whole Analog section is as follows.



L3.14.1 DAC

This is a stereophonic DAC that has a resolution of 16-bits.

L3.14.2 Headphone Amplifier

Volume circuit is provided for headphone output.
Both pins outputs stereophonic sounds. In addition, it is possible to output from HPOUT-L/MONO pin as monaural sound.
This register is also used to select the monaural setting.

Default 8'h00

B Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#8	W/R	MONO	"0"	"0"	HPVOLL				
#9	W/R	"0"	"0"	"0"	HPVOLR				

HPVOLL: This is a bit for setting volume circuit that is in the previous stage of HPOUT-L/MONO pin.
The relationship between the setting value and volume is the same as EQVOL (#7).

HPVOLR: This is a bit for setting volume circuit that is in the previous stage of HPOUT-R pin.
The relationship between the setting value and volume is the same as EQVOL (#7).

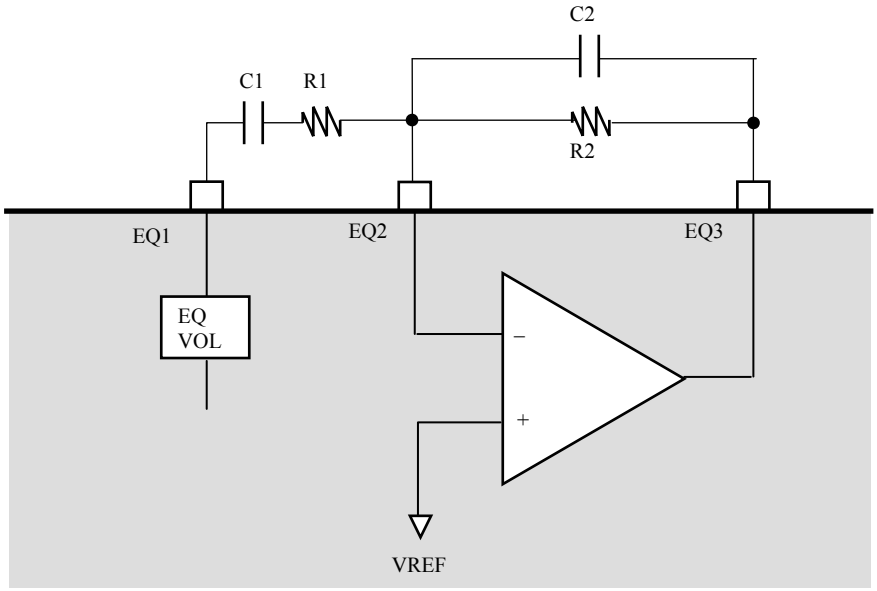
MONO: This bit is for selecting stereophonic sound or monaural sound as a headphone output (output from HPOUT-L/MONO pin and HPOUT-R pin).
"1" = monaural, "0" = stereophonic
In monaural mode, (DAC Lch output × 1/2) + (DAC Rch output × 1/2) is outputted from HPOUT-L/MONO pin.

For the relationship between the setting value and volume of EQVOL, HPVOLL, HPVOLR, and SPVOL, refer to "L5.1.5 Analog Section Volume Correspondence Table".

Volume control is provided before the output stage, and it is possible to control MUTE in the range from 0dB to -30dB by 1 dB.
It is set in the Intermediate registers #8 and #9.
When using it in monaural mode, set MONO bit of #8 to "1".

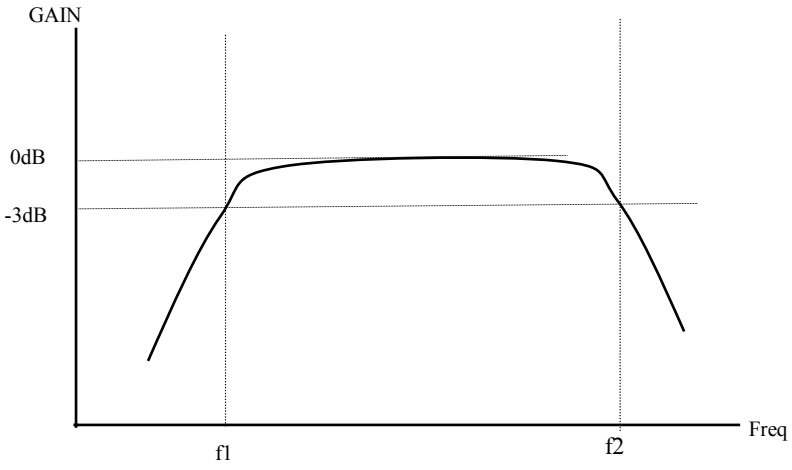
L3.14.3 EQ Amplifier

Voice quality and GAIN can be compensating with external circuit connected to EQ1 to EQ3 pins.
An example of the external circuit and configuration of circuit in the pins EQ1 to EQ3 is as follows.

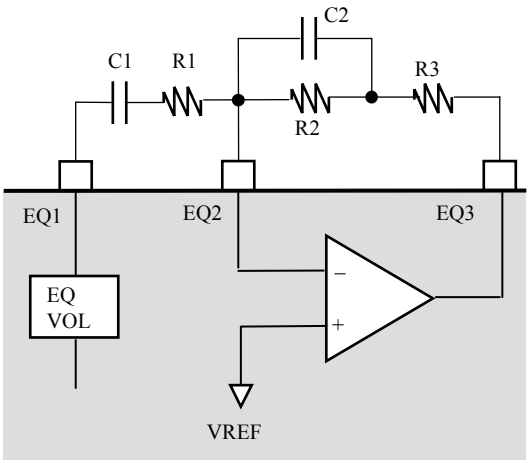


The GAIN and filter characteristic can be adjusted with the values of C1, C2, R1, and R2. GAIN = R2 / R1.
The filter cutoff frequencies f1 and f2 are as follows.

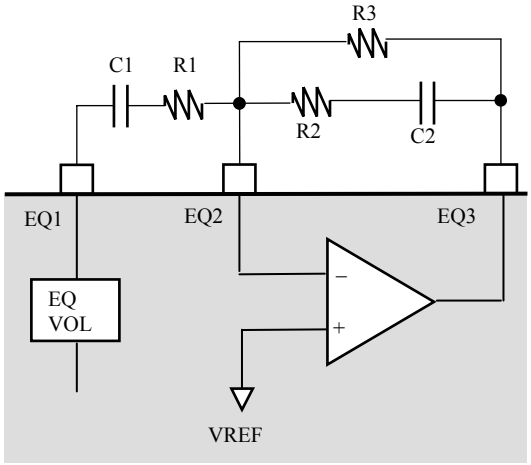
$f1 = 1 / (2 \pi \times R1 \times C1)$ $f2 = 1 / (2 \pi \times R2 \times C2)$



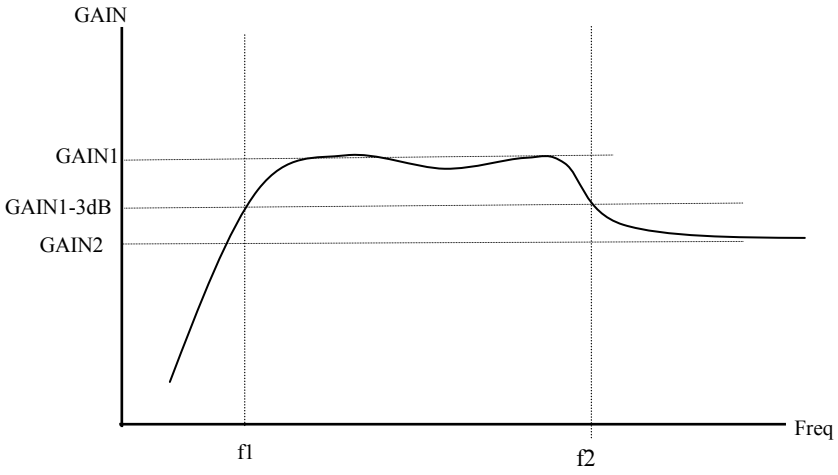
It is possible to obtain the following frequency responses by adding the resistor R3.



GAIN1 = (R2 + R3) / R1 and GAIN2 = R3 / R1
The filter cutoff frequencies f1 and f2
f1 = 1 / (2 π × R1 × C1)
f2 = 1 / (2 π × R2 × C2)



GAIN1 = R3 / R1 and GAIN2 = (R3 // R2) /R1
(R3 // R2 : Parallel resistance of R3 and R2)
f1 = 1 / (2 π × R1 × C1)
f2 = 1 / (2 π × R2 × C2)



Volume control is provided in the previous stage of the EQ amplifier, and it is possible to control MUTE in the range from 0dB to -30dB by 1 dB.
It is set in the Intermediate register #7.

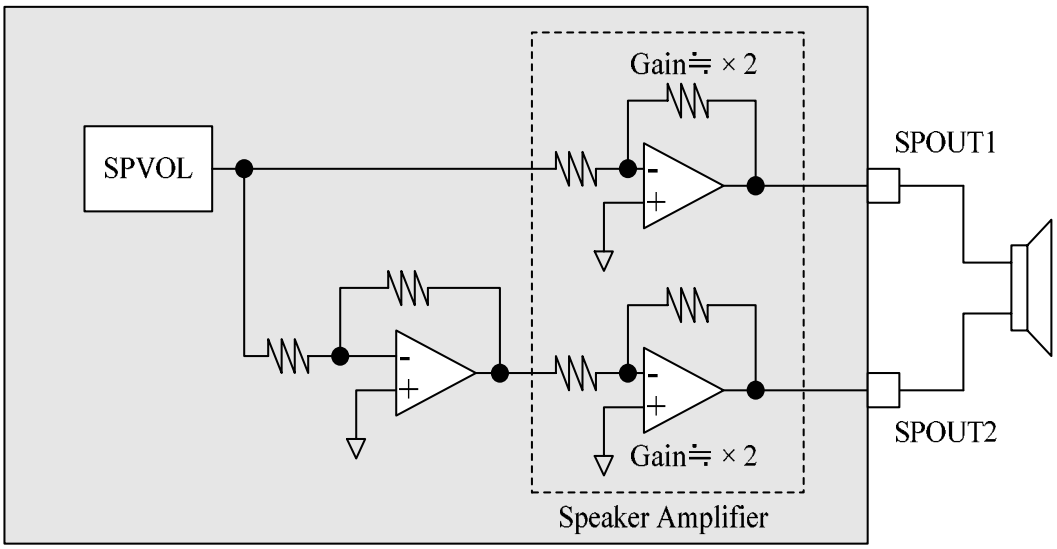
Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#7	W/R	"0"	"0"	"0"	EQVOL				

EQVOL: This is a bit for setting volume circuit that is in the previous stage of EQ amplifier.
For the relationship between the setting value and volume, please refer to "L5.1.5 Analog Section Volume Correspondence Table".

L3.14.4 Speaker Amplifier

This product is equipped with a speaker amplifier that can output up to 580 mW.
SPVOL (volume) is provided for entire speaker amplifier.



Volume control is provided in the previous stage of the speaker amplifier, in addition, it is possible to control MUTE in the range from 0dB to -30dB by 1 dB.
It is set in the Intermediate register #10.
The relationship between the setting value and volume is the same as the headphone volume (HPVOLL and HPVOLR).

Default 8'h00

B_Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#10	W/R	VSEL2	VSEL1	"0"	SPVOL				

SPVOL: This is a bit for setting the volume circuit in the previous stage of the speaker amplifier.
The relationship between the setting value and volume is the same as EQVOL (#7).

VSEL1 and VSEL2: These bits are for setting a center voltage on which the speaker amplifier operates.
The relationship between individual setting values and the center voltage is shown in the following table.
Select a proper setting value according to the power supply voltage of VDD and SPVDD.
If no combination coincides with the values, select the close combination.
The output from HPOUT and EQ1 pins swing from the center voltage of VDD*0.5, regardless of the setting value of VSEL.

VSEL2	VSEL1	Center voltage of speaker amplifier (V)	Voltage of VDD and SPVDD
0	0	0.6 × VDD	Assumes the operating environment of SPVDD=3.6V, VDD=3.0V
0	1	0.5 × VDD	Assumes the operating environment of SPVDD=3.0V, VDD=3.0V
1	0	0.67 × VDD	Assumes the operating environment of SPVDD=3.6V, VDD=2.7V
1	1	0.72 × VDD	Setting is prohibited

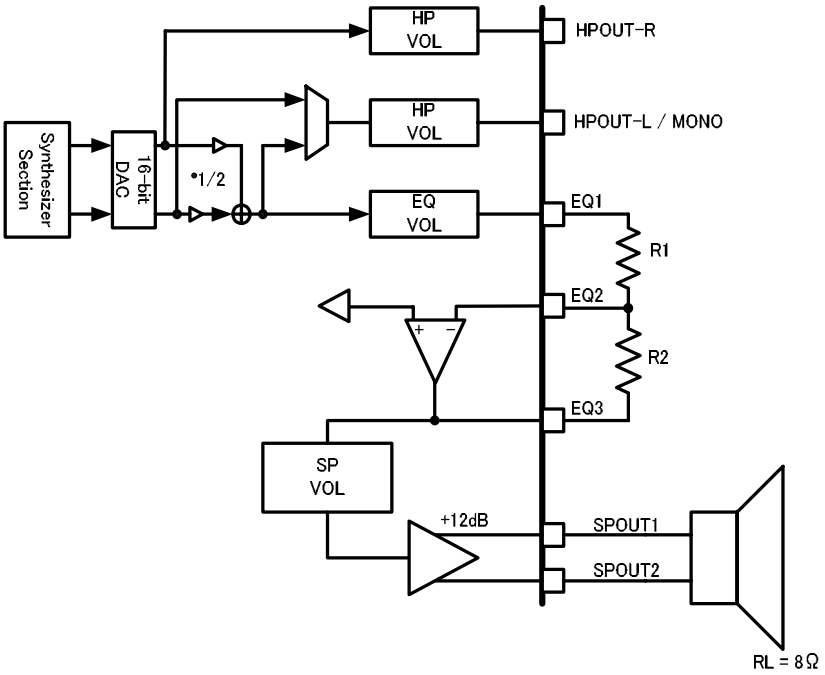
The load between SPOUT1 and SPOUT2 pins is 8 Ω @Typ. Do not connect more than 1000pF capacitor to SPOUT1 and SPOUT2 pins because there is possibility of oscillations.

L3.14.5 VREF

This is a circuit that makes a reference voltage for operating an Analog Block.
It is recommended connecting a 0.1μF of capacitor to the VREF pins.
The maximum of a rising time (the time until which gets to the reference voltage after the power-down cancellation) are as follows.
(Contents value which is used in the VREF pins [μF] / 0.1[μF]) * 10 [ms]

L3.14.6 Level Diagram

The peak power voltage amplitude of 16-bits DAC is about 1.5Vp-p (3.0V@VDD).
The maximum amplitude of data per one voice which are outputted from synthesizer section is 1.5Vp-p. (*)
When EQ1 and HPVOL are set as 0dB, the peak power voltage amplitude from EQ1 and HPOUT* pins become 1.5Vp-p.
GAIN outputted from EQ1 at the resistance value between EQ1 and EQ3 can be coordinated.
In addition, GAIN is determined by the friction ratio R1 and R2. GAIN = R2 / R1.
In the condition of "SPVOL = 0dB", when the friction of EQ3 pin becomes more than 1.5Vp-p, it is SPOUT1, and a waveform clips are generated by two power output.
Be sure to turn SPVOL and use when the friction of EQ3 pins becomes more than 1.5Vp-p.
In the Speaker Amplifier, be sure to "12dB (4 times) and output to speaker amplifier.
(*): Under the condition of each Volume are 0dB.
The levels per one voice are sometime minimized in the ROM's built-in data.

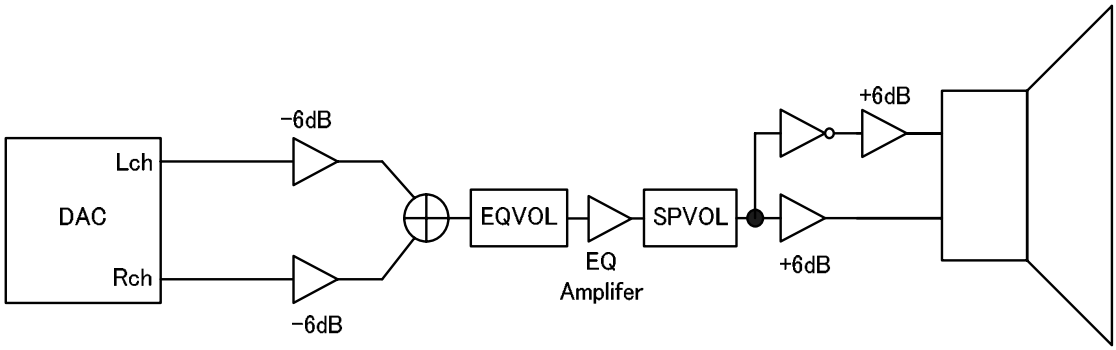


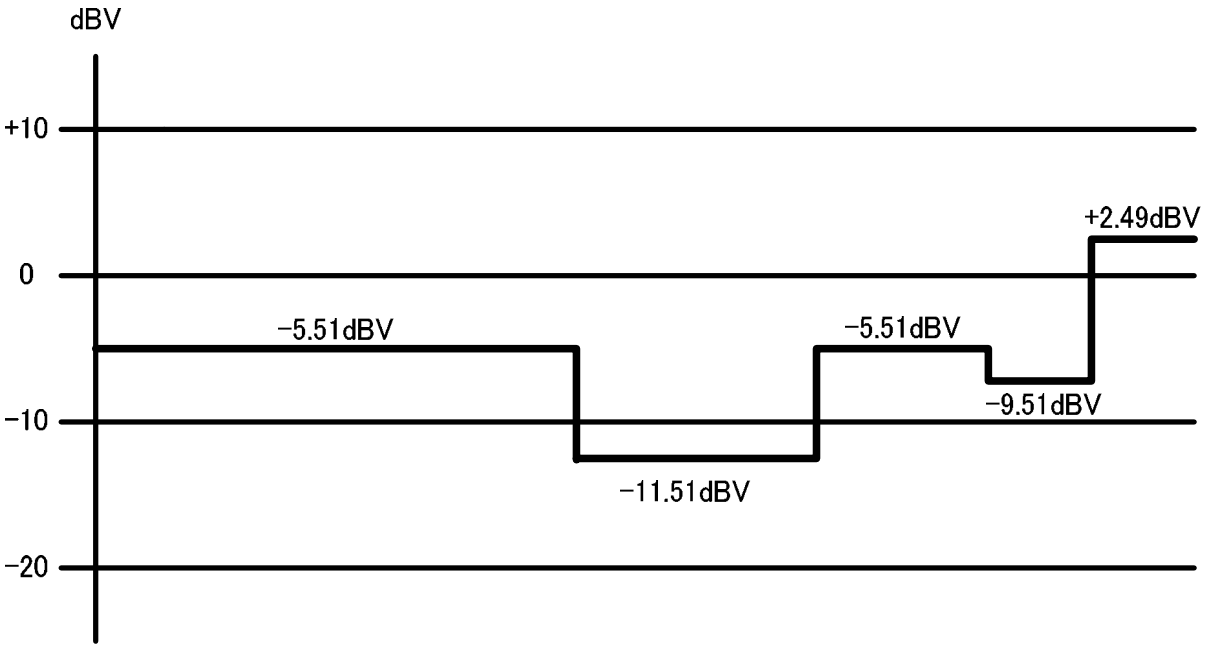
Assumption at the time of 500mW output

If RL = 8Ω, the speaker output of 500mW when voltage between SPOUT1 - 2 is 2.0V rms. At this time, the speaker amplifier output amplitude becomes 2.0 × 2 × 1.414 = 5.66Vp-p (when SPVOL=0dB), and thus, the voltage at EQ3 pin is 5.66 / 4 = 1.41Vp-p.

Level Diagram of Analog Section

The following level diagram shows the case when the output from DAC is 1.5Vpp, EQVOL is set to – 6dB, EQ amplifier is set to +6dB, and SPVOL is set to – 4dB.





What is dBV?

dBV = 20 × $\log_{10}$ Vrms (Vrms represents effective value of voltage)
1.5Vpp converted to effective voltage is 1.5 / 2√2 = 0.53033.
Substituting this value for the above formula gives – 5.5091dBV.

L4 Pins & Electrical Characteristics

L4 describes electrical characteristics including pin information.
Composition of this section is as follows.

L4.1 PIN ASSIGNMENTS

L4.2 PINS FUNCTIONS

L4.2.1 Power Supply (VDD, VSS, IOVDD, SPVDD, SPVSS)
L4.2.2 System Reset (/RST)
L4.2.3 Clock (CLKI, PLLC)
L4.2.4 CPU Interface (/CS, /WR, /RD, A0, D0 to D7, /IRQ)
L4.2.5 Digital Output (LED, MTR)
L4.2.6 Analog Input / Output

L4.3 PINS STATUS DURING EACH MODE

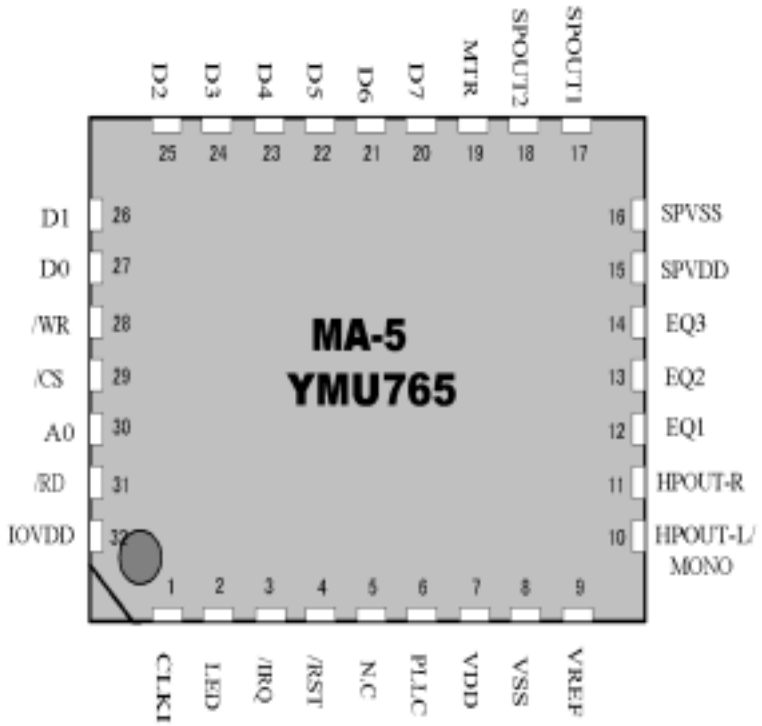
L4.3.1 Normal Operation Mode
L4.3.2 Hardware Reset Mode
L4.3.3 Power-off Mode
L4.3.4 Power Down Mode

L4.4 ELECTRICAL CHARACTERISTICS

L4.4.1 Absolute Maximum Rating
L4.4.2 Recommended Operation Condition
L4.4.3 Power Consumption
L4.4.4 DC Characteristics
L4.4.5 AC Characteristics
L4.4.6 Analog Characteristics

L4.1 Pin Assignments

It is the QFN plastic package of 52 pins.



L4.2 Pins Functions

No.	Pin name	I/O	Power supply	Function
1	CLKI	Ish	VDD	Clock input (1.5 MHz ~ 20 MHz) *Correspond with TCXO.
2	LED	O	IOVDD	External LED control
3	/IRQ	O	IOVDD	Interrupt output
4	/RST	Ish	IOVDD	Hardware reset input
5	N.C	–	–	No Connection (Be sure to use without connection.)
6	PLLC	A	VDD	Connection of capacitor for built-in PLL Connect a series connection of 1000 pF capacitor and 3.3 kΩ resistor between this pin and VSS(*). (*)Directly connect VSS used here and VSS of 8th pin.
7	VDD	–	–	Power supply (2.65 ~ 3.30V) Connect 0.1 µF and 4.7 µF capacitors between this pin and VSS.
8	VSS	–	–	Ground
9	VREF	A	VDD	Analog reference voltage: Connect 0.1 µF capacitor between this pin and VSS.
10	HPOUT-L / MONO	A	VDD	Headphone output Lch (Can be used as MONO output)
11	HPOUT-R	A	VDD	Headphone output Rch
12	EQ1	A	VDD	Equalizer pin 1
13	EQ2	A	VDD	Equalizer pin 2
14	EQ3	A	VDD	Equalizer pin 3
15	SPVDD	–	–	Speaker amplifier analog power supply (VDD ~ 4.50V) Connect 0.1 µF and 4.7 µF capacitors between this pin and SPVSS.
16	SPVSS	–	–	Speaker amplifier analog ground
17	SPOUT1	A	SPVDD	Speaker connection pin 1
18	SPOUT2	A	SPVDD	Speaker connection pin 2
19	MTR	O	IOVDD	External motor control pin
20	D7	I/O	IOVDD	CPU I/F data bus 7
21	D6	I/O	IOVDD	CPU I/F data bus 6
22	D5	I/O	IOVDD	CPU I/F data bus 5
23	D4	I/O	IOVDD	CPU I/F data bus 4
24	D3	I/O	IOVDD	CPU I/F data bus 3
25	D2	I/O	IOVDD	CPU I/F data bus 2
26	D1	I/O	IOVDD	CPU I/F data bus 1
27	D0	I/O	IOVDD	CPU I/F data bus 0
28	/WR	I	IOVDD	CPU I/F write enable
29	/CS	I	IOVDD	CPU I/F chip select
30	A0	I	IOVDD	CPU I/F address signal
31	/RD	I	IOVDD	CPU I/F read enable
32	IOVDD	–	–	Pin power supply (1.65 ~ VDD)

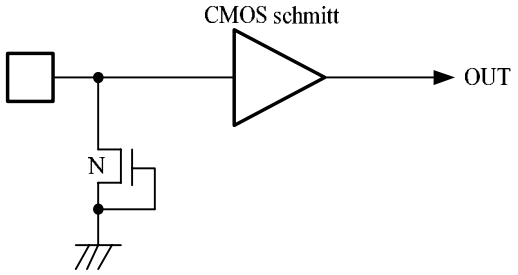
: Analog pin Ish : Schmitt input

L4.2.1 Power Supply (VDD, VSS, IOVDD, SPVDD, SPVSS)

- SPVDD : Power voltage supply pin dedicated to the speaker amplifier.
  The operation is guaranteed in the range from VDD to 4.50V.
- SPVSS : Grounding pin dedicated to the speaker amplifier.
  Connect capacitors of 0.1µF and 4.7µF between SPVDD and SPVSS.
- IOVDD :
  Power voltage supply pin dedicated to LSI pin.
  The operation is guaranteed in the range from 1.65V to VDD.
  It is prohibited to exceed the potential of VDD.
  Connect capacitors of 0.1µF and 4.7µF between IOVDD and VSS.
- VDD : Power voltage supply pin for circuits that operate with other than SPVDD and IOVDD (mainly internal core except speaker amplifier).
  The operation is guaranteed in the range from 2.65V to 3.30V
  Connect capacitors of 0.1µF and 4.7µF between VDD and VSS.
- VSS : Grounding pin.

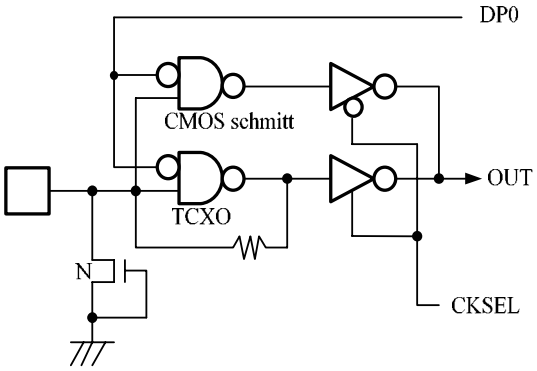
L4.2.2 System Reset (/RST)

This is a reset pin for initializing the LSI. Setting the level to “L” initializes the LSI.
The pin circuit is as shown in the following figure.

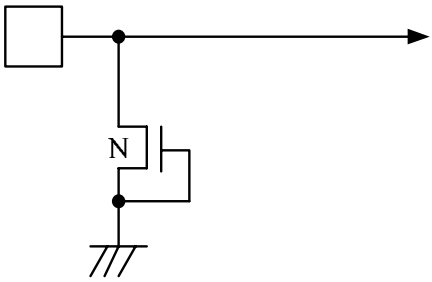


L4.2.3 Clock (CLKI, PLLC)

CLKI is the clock input pin.
The clock frequency ranging from 1.5MHz to 20MHz is inputted.
The inputting of clock can be stopped (=0Hz) at power down.
It is possible to select “CMOS input” or “TCXO input”.
The pin circuit is as shown in the following figure.



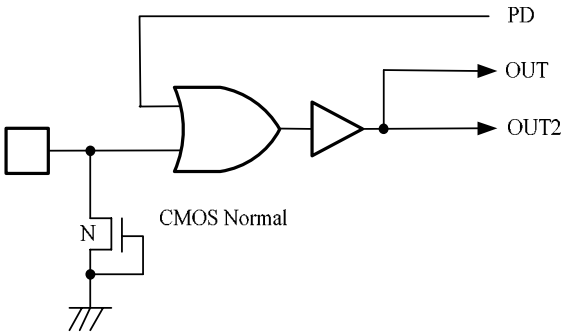
PLLC is a pin for connecting external capacitor that is used for the loop filter of PLL circuit.
Connect a 1000pF capacitor and a 3.3kΩ resistor in series between this pin and 8 pin VSS.



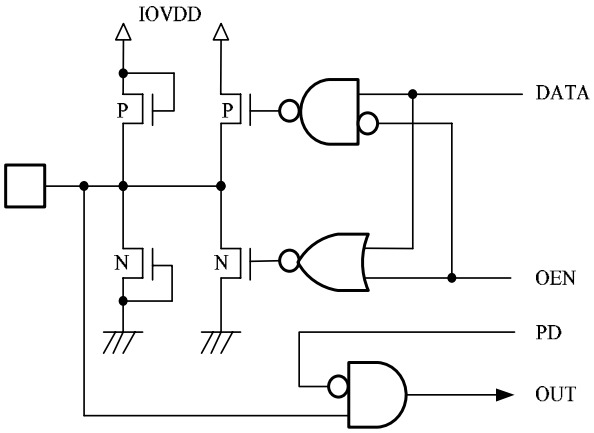
L4.2.4 CPU Interface (/CS, /WR, /RD, A0, D0 to D7, /IRQ)

/CS: Chip select pin of CPU interface
/WR: Write enable pin of CPU interface
/RD: Read enable pin of CPU interface
A0: Address pin of CPU interface

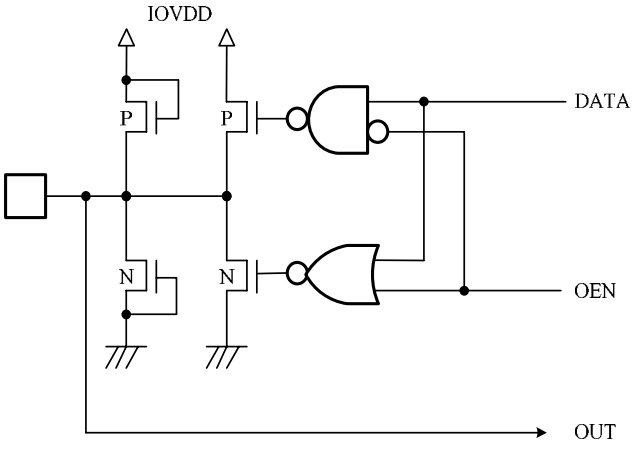
The pin circuit is shown in the following figure. OUT from /CS pin is connected to PD signal.
In the case of /CS pin, PD is fixed to "0".



D0 to D7 : Data bus pin of CPU interface
OUT from /CS pin is connected to PD signal.

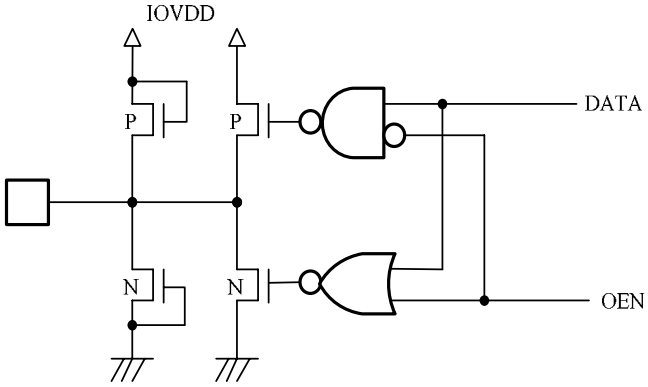


/IRQ : This pin outputs an interrupt. OUT signal is not used (open).



L4.2.5 Digital Output (LED, MTR)

LED, MTR : These are output pins in order to control LED and vibrator, which are connected to the exterior of this LSI.
The pin circuit is the same as /IRQ.



L4.2.6 Analog Input / Output

HPOUT-L / MONO	: It is a pin for a headphone output Lch. When monaural mode is selected, monaural signals are outputted from this pin.
HPOUT-R	: It is a pin for a headphone output Rch.
SPOUT1, SPOUT2	: It is a pin for speaker output.
VREF	: It is a pin for an analog standard voltage.
EQ1 to EQ3	: It is a pin for equalizers.

A pin circuit is the same as PLLC.

L4.3 Pins Status During each Mode

L4.3.1 Normal Operation Mode

It becomes pin operation explained by “L4.2 Pins Functions”.

L4.3.2 Hardware Reset Mode

Pin state during hardware reset (/RST=L) (All of VDD and IOVDD are supplied.)

Pin name	State
CLKI	CLKI pin is in power down state just after hardware reset. The clock input during hardware reset is arbitrary. However, the input level should be “H” or “L”, and intermediate level is prohibited.
/RST	Input “L” level during hardware reset.
LED, MTR	“L” output fixed
/IRQ	“H” output fixed
D0 ~ D7	It is in input state. Both level (“H”/”L”) can be input. However, intermediate level is prohibited.
/CS	“H” level should be inputted.
/WR, /RD	If /CS is “H” level, both level (“H”/”L”) can be input. “H” level input is recommended. However, intermediate level is prohibited.
A0	Both level (“H”/”L”) can be input. However, intermediate level is prohibited.

L4.3.3 Power-off Mode

Pin state at power off (IOVDD=VDD=0V)

Pin name	Voltage of the pin: X		
	X < -0.4V	-0.4V ≤ X ≤ 0.4V	0.4V < X
/WR, /RD, A0, /RST, /CS	Low impedance	High impedance	High impedance
D0 ~ D7, LED, MTR, /IRQ, CLKI	Low impedance	High impedance	Low impedance

L4.3.4 Power Down Mode

Analog pin state during power down mode

State / Pin name	AP0 = 1 AP1 = 1 AP2 = 1 AP3 = 1 AP4L = 1 AP4R = 1	AP0 = 0 AP1 = 1 AP2 = 1 AP3 = 1 AP4L = 1 AP4R = 1	AP0 = 0 AP1 = 0 AP2 = 1 AP3 = 1 AP4L = 1 AP4R = 1	AP0 = 0 AP1 = 0 AP2 = 1 AP3 = 0 AP4L = 1 AP4R = 1	AP0 = 0 AP1 = 0 AP2 = 1 AP3 = 0 AP4L = 0 AP4R = 1	AP0 = 0 AP1 = 0 AP2 = 1 AP3 = 0 AP4L = 0 AP4R = 0	AP0 = 0 AP1 = 0 AP2 = 0 AP3 = 0 AP4L = 0 AP4R = 0
VREF	Z (0V)	Z (VDD / 2)	←	←	←	←	←
HPOUT_L	F	←	←	←	D (VDD / 2)	←	←
HPOUT_R	F	←	Z (VDD / 2)	←	←	D (VDD / 2)	←
EQ1	F	←	D (VDD / 2)	←	←	←	←
EQ2	F or Z (0V) *	←	Z (VDD / 2)	←	←	←	←
EQ3	F or Z (0V) *	←	D (VDD / 2)	←	←	←	←
SPOUT1	F or Z (0V) *	←	D (VSEL)	←	←	←	←
SPOUT2	F or Z (0V) *	←	Z (VSEL)	←	←	←	D (VSEL)

Comment:

- F = High Impedance and floating potential.
- Z = High impedance and potential in () is decided.
- D = Low impedance and potential in () is driven.

The indication of (VSEL) is shown by the following potential according to setting value VSEL2 and VSEL1 of Intermediate register BANK=0 ID#10.

- (VSEL2, VSEL1) = (0, 0) : 0.6*VDD
- (VSEL2, VSEL1) = (0, 1) : 0.5*VDD
- (VSEL2, VSEL1) = (1, 0) : 0.67*VDD

(*)……Z (0V) is set at the times other than (VSEL2, VSEL1) = (0, 0). Others are F.

As a premise,

- A load is stuck between SPOUT1 and SPOUT2.
- Feedback resistance is added between EQ2 and EQ3.
- Capacity for the DC cut is added between EQ1 and EQ2.
- SP Volume, EQ Volume, and HP Volumes are MUTE condition.

L4.4 Electrical Characteristics

L4.4.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
SPVDD pin, power supply voltage (Speaker amplifier section)	SPVDD	-0.3	6.0	V
VDD pin, power supply voltage	VDD	-0.3	4.2	V
IOVDD pin, power supply voltage	IOVDD	-0.3	4.2	V
SPOUT1, SPOUT2 pin, applied voltage	V_{INSP}	-0.3	SPVDD+0.3	V
Analog input voltage	V_{INA}	-0.3	VDD+0.3	V
Digital input voltage 1 (*1)	V_{IND1}	-0.3	IOVDD+0.3	V
Digital input voltage 2 (*2)	V_{IND2}	-0.3	VDD+0.3	V
Permissible loss (*3)	Pd		1197	mW
Storage temperature	T_{STG}	-50	125	℃

[Condition] VSS = SPVSS = 0V

(*1) Target pin: D0 ~ D7, /CS, A0, /WR, /RD, /RST

(*2) Target pin: CLKI

(*3) Top=25°C, and it is mounted on glass epoxy PCB (30mm×100mm×1.0mm).
When operating above Top= 25 °C, permissible loss decreases 12 mW per 1 °C.

L4.4.2 Recommended Operation Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPVDD operating voltage (Speaker amplifier section)	SPVDD	VDD	3.60	4.50	V
VDD operating voltage	VDD	2.65	3.00	3.30	V
IOVDD operating voltage	IOVDD	1.65	1.80	VDD	V
Operating ambient temperature	T_{OP}	-20	25	85	℃

[Condition] VSS = SPVSS = 0V

L4.4.3 Power Consumption

Parameter	Conditions	Typ.	Max.	Unit
Power consumption of VDD+IOVDD	Normal operation (*1)	40		mA
At Silent sound generated SPVDD side		4		mA
At the time of output 400mW / 8ohm load SPVDD side		210		mA
Power down mode Ta = +25°C	VDD+IOVDD+SPVDD (*2)	0.5	2	µA
Power down mode Ta = +85°C	VDD+IOVDD+SPVDD (*2)		10	µA

(*1) VDD=IOVDD=3.00V, SPVDD=3.60V, T_{OP}=25°C

(*2) VDD=IOVDD=3.30V, SPVDD=4.50V
/CS input pin is fixed to V_{IH}=IOVDD, the other input pins are V_{IL}=VSS and V_{IH}=(IO)VDD.

L4.4.4 DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage “H” level 1	V_{IH}	(*1)	0.65 × IOVDD			V
Input voltage “L” level 1	V_{IL}	(*1)			0.35 × IOVDD	V
Input voltage “H” level 2	V_{IH}	(*2)	0.75 × IOVDD			V
Input voltage “L” level 2	V_{IL}	(*2)			0.25 × IOVDD	V
Input voltage “H” level 3	V_{IH}	(*3)	0.70 × VDD			V
Input voltage “L” level 3	V_{IL}	(*3)			0.30 × VDD	V
Output voltage “H” level	V_{OH}	(*4) I_{OH} = (*5)	0.80 × IOVDD			V
Output voltage “L” level	V_{OL}	(*4) I_{OL} = (*5)			0.20 × IOVDD	V
Schmitt width 1	Vsh1	/RST pin		0.10×IOVDD		V
Schmitt width 2	Vsh2	CLKI pin		0.10×VDD		V
Input leakage current	IL		-1		1	µA
Input capacity	CI				10	pF

[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, IOVDD=1.65 ~ VDD[V], Capacitor load=50 pF

(*1) Target pin: D0 ~ D7, /CS, A0, /WR, /RD

(*2) Target pin: /RST

(*3) Target pin: CLKI (In the case of CMOS mode)

(*4) Target pin: D0 ~ D7, /IRQ, LED, MTR

(*5) /IRQ, D0 ~ D7, are I_{OH}= –1 mA, I_{OL}= +1 mA

LED, MTR are I_{OH} = –4 mA, I_{OL}= +4 mA

However, when IOVDD is less than 2.65V, D0 ~ D7, /IRQ, LED, and MTR become I_{OH}=-0.2mA and I_{OL}=+0.2mA.

L4.4.5 AC Characteristics

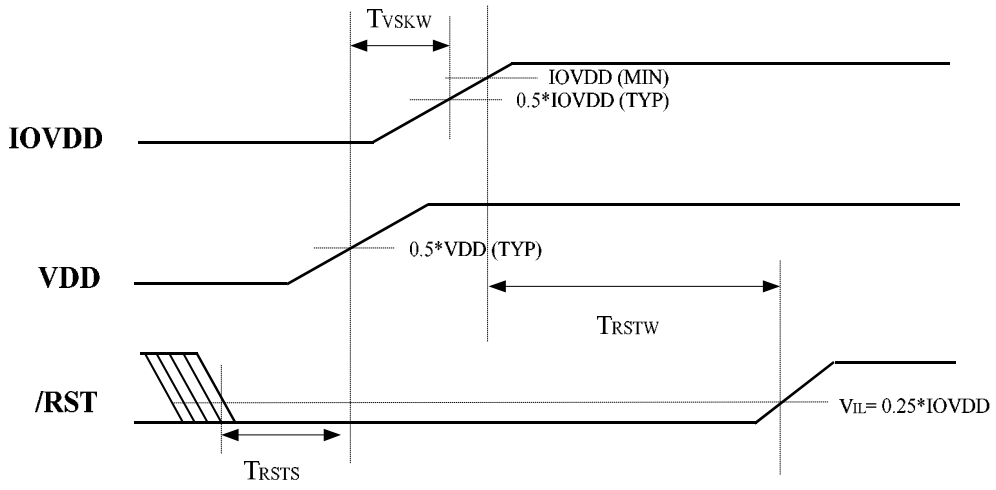
L4.4.5.1 Reset and clock timing

○ /RST, CLKI (CMOS mode), other input signals

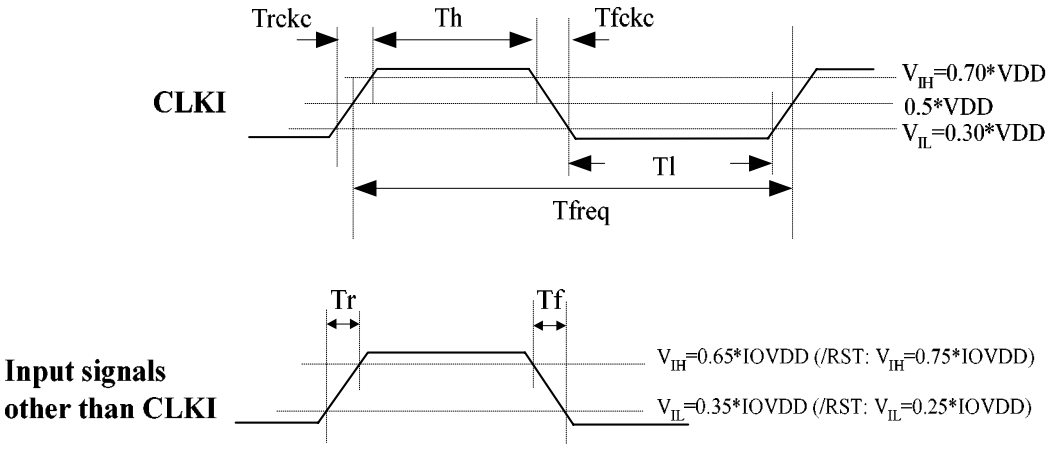
Parameter	Symbol	Min.	Typ.	Max.	Unit
/RST "L" pulse width	T_{RSTW}	100			μs
/RST (indefinite → L) setup time	T_{RSTS}	0			μs
VDD - IOVDD rise time difference	T_{VSKW}	0		3	ms
CLKI frequency	1 / Tfreq	1.5		20	MHz
CLKI rise / fall time	Trckc / Tfckc			30	ns
CLKI High time	Th	15			ns
CLKI Low time	Tl	15			ns
Input signals other than CLKI rise / fall time	Tr / Tf			20	ns

[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, IOVDD=1.65 ~ VDD[V], Capacitor load=50 pF

The input to Clock can be stopped (=0Hz) during reset period and power down state (DP0=1).
However, the input level is to be H or L, and input of intermediate level is prohibited.
When VDD and IOVDD are used by respectively different power supply, make sure to rise from VDD first.



The reset width is defined as the time from the moment IOVDD has risen to 1.65V.
/RST has to be settled at "L" level at the time VDD has risen to 50%.

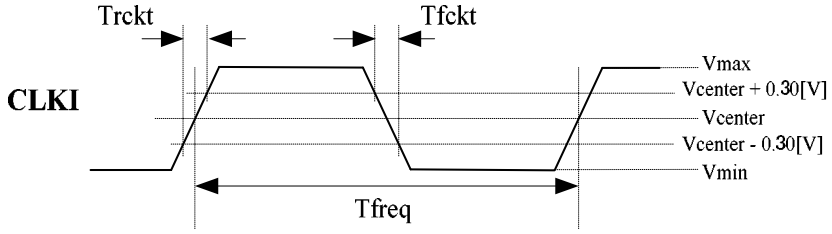


○ CLKI (TCXO mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLKI frequency	1 / Tfreq	1.5		20	MHz
CLKI rise / fall time	Trckt , Tfckt			250	ns
CLKI amplitude H	Vmax - Vcenter	0.30		0.35 × VDD	V
CLKI amplitude L	Vcenter - Vmin	0.30		0.35 × VDD	V
Wait time to stable operation (*1)	Twait	2			ms
Feedback resistance	Rck	30	45	63	kΩ

[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, Capacitor load=50pF

(*1) : The value at the AC coupling of TCXO parts and the CLKI pin by the capacity of 1000pF.



- The voltage level which Duty of CLKI becomes 50% (High time = Low time) is defined as Vcenter.
- Trckt and Tfckt are defined by the change time between Vcenter + 0.30[v] and Vcenter - 0.30[v].
- The timing observation level of Tfreq is to be Vcenter (Duty=50%).

L4.4.5.2 CPU interface timing

The AC characteristics of a CPU interface are measured on condition as follows.

The input conditions at the time of measurement : V_{IH} = 0.8×IOVDD, V_{IL}=0.2×IOVDD

The measurement points : V_{IH} = 0.65×IOVDD, V_{IL}=0.35×IOVDD

V_{OH} = 0.65×IOVDD, V_{OL}=0.35×IOVDD

• CPU interface 1 (In the case of IOVDD≧2.65V)

(Write cycle)

Parameter	Symbol	Min	Max.	Unit
Address setup time	T_{ADS}	50		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	50		ns
Chip select hold time	T_{CSH}	0		ns
Write pulse width	T_{WW}	50		ns
Data setup time	T_{WDS}	30		ns
Data hold time	T_{WDH}	0		ns

[Condition] T_{OP}=-20 ~ 85°C, VDD=IOVDD=2.65 ~ 3.30V, Capacitor load=50 pF

(Read cycle)

Parameter	Symbol	Min	Max.	Unit
Access time from /RD pin	T_{ACCRD}		70	ns
Access time from /CS pin	T_{ACCCS}		70	ns
Access time from /A0 pin	T_{ACCA0}		70	ns
Data hold time from /RD pin	T_{DHRD}	0		ns
Data hold time from /CS pin	T_{DHCS}	0		ns
Data hold time from A0 pin	T_{DHA0}	0		ns
High-impedance transition time from /RD pin	T_{DZRD}		30	ns
High-impedance transition time from /CS pin	T_{DZCS}		30	ns

[Condition] T_{OP}=-20 ~ 85°C, VDD=IOVDD=2.65 ~ 3.30V, Capacitor load=50 pF

I_{OH}= -1.0mA, I_{OL}= +1.0mA (D0 ~ D7 pin)

● CPU interface 2 (In the case of IOVDD < 2.65V)

(Write cycle)

Parameter	Symbol	Min	Max.	Unit
Address setup time	T_{ADS}	50		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	50		ns
Chip select hold time	T_{CSH}	0		ns
Write pulse width	T_{WW}	50		ns
Data setup time	T_{WDS}	50		ns
Data hold time	T_{WDH}	0		ns

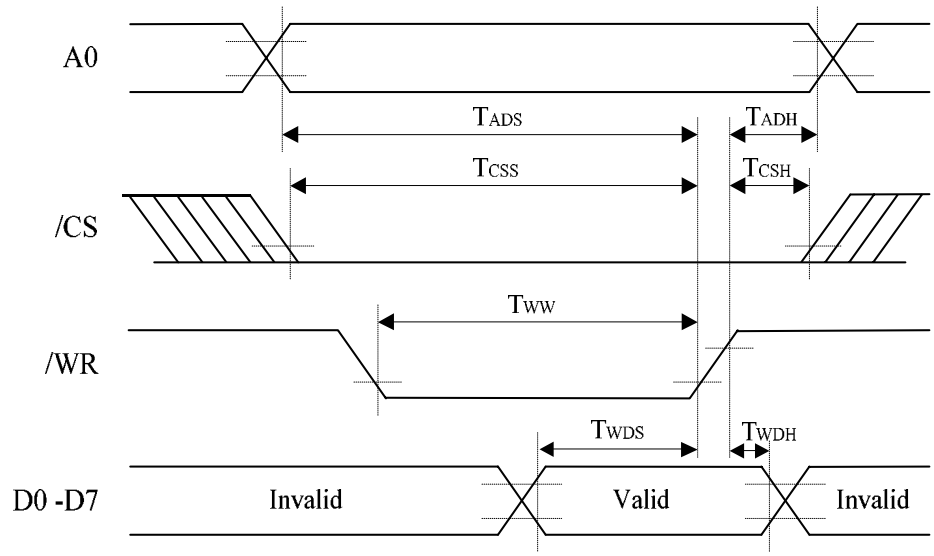
[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, IOVDD=1.65 ~ less than 2.65V, Capacitor load=30 pF

(Read cycle)

Parameter	Symbol	Min	Max.	Unit
Access time from /RD pin	T_{ACCRD}		80	ns
Access time from /CS pin	T_{ACCCS}		80	ns
Access time from /A0 pin	T_{ACCA0}		80	ns
Data hold time from /RD pin	T_{DHRD}	0		ns
Data hold time from /CS pin	T_{DHCS}	0		ns
Data hold time from A0 pin	T_{DHA0}	0		ns
High-impedance transition time from /RD pin	T_{DZRD}		50	ns
High-impedance transition time from /CS pin	T_{DZCS}		50	ns

[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, IOVDD=1.65 ~ less than 2.65V, Capacitor load=30 pF
I_{OH}= -0.2mA, I_{OL}= +0.2mA (D0 ~ D7 pin)

Write cycle



Note :

T_{ADH} : The hold time of A0 pin, which is defined with respect to the point where the rise of /WR has reached 0.65*IOVDD under the condition that both two specifications (T_{CSH} , T_{WDH}) are secured more than minimum value (=0ns).

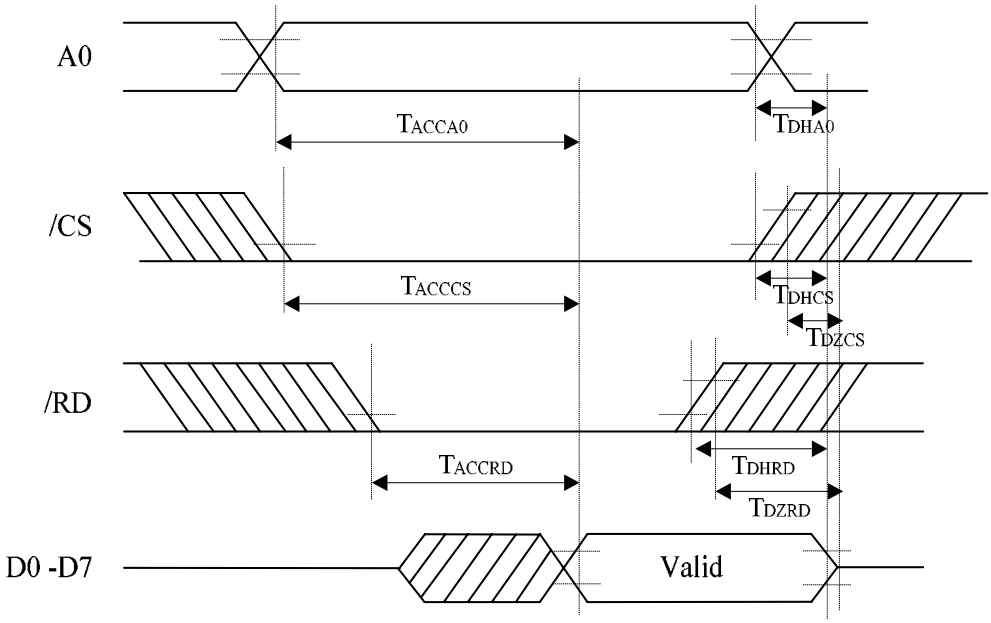
T_{CSH} : The hold time of /CS pin, which is defined with respect to the point where the rise of /WR has reached 0.65*IOVDD under the condition that both two specifications (T_{ADH} , T_{WDH}) are secured more than minimum value (=0ns).

T_{WDH} : The hold time of D0 ~ D7 pins, which is defined with respect to the point where the rise of /WR has reached 0.65*IOVDD under the condition that both two specifications (T_{ADH} , T_{CSH}) are secured more than minimum value (=0ns).

T_{ADS} : The hold time of A0 pin, which is defined with respect to the point where /WR has become invalid (0.35*IOVDD) under the condition that all of three specifications (T_{CSS}, T_{WW}, T_{WDS}) are secured more than minimum value.

T_{CSS} : The hold time of /CS pin, which is defined with respect to the point where /WR has become invalid (0.35*IOVDD) under the condition that all of three specifications (T_{ADS}, T_{WW}, T_{WDS}) are secured more than minimum value.

Read cycle



Note :

T_{ACCA0} : The access time until D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD) after A0 is defined (0.65*IOVDD or 0.35*IOVDD).
Considers that /RD and /CS are defined beforehand (*1).

T_{ACCCS} : The access time until D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD) after /CS is defined (0.35*IOVDD).
Considers that A0 and /RD are defined beforehand (*1).

T_{ACCRD} : The access time until D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD) after /RD is defined (0.35*IOVDD).
Considers that A0 and /CS are defined beforehand (*1).

T_{DHRD} : The time (Hold time) until D0 ~ D7 output valid data after /RD becomes enable (=0.35*IOVDD) under the condition that A0 and /CS secure sufficient hold time (*2).

T_{DHCS} : The time (Hold time) until D0 ~ D7 output valid data after /CS becomes enable (=0.35*IOVDD) under the condition that A0 and /RD secure sufficient hold time (*2).

T_{DHA0} : The time (Hold time) until D0 ~ D7 output valid data after A0 becomes enable (0.65*IOVDD or 0.35*IOVDD) under the condition that /RD and /CS secure sufficient hold time (*2).

T_{DZRD} : The time until D0 ~ D7 become high impedance status after /RD becomes disable (=0.65*IOVDD) under the condition that A0 and /CS secure sufficient hold time (*2).

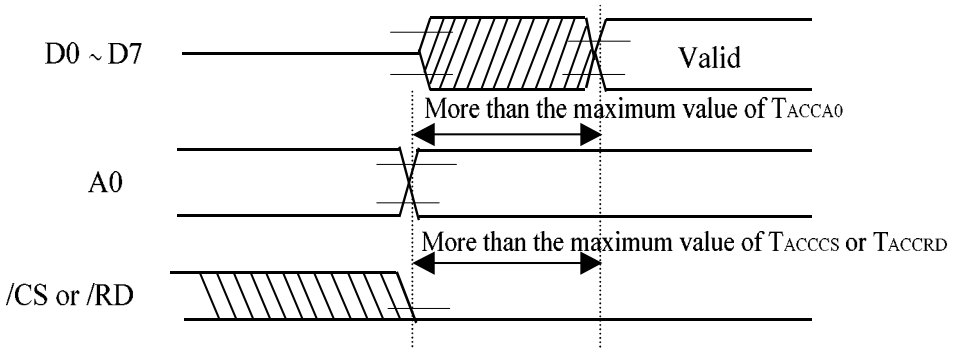
T_{DZCS} : The time until D0 ~ D7 become high impedance status after /CS becomes disable (=0.65*IOVDD) under the condition that A0 and /RD secure sufficient hold time (*2).

(*1) "~ defined beforehand." means,

In the case of /CS : The status that /CS is defined (0.35*IOVDD) before more than the time of T_{ACCCS} with respect to the point where D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD).

In the case of /RD : The status that /RD is defined (0.35*IOVDD) before more than the time of T_{ACCRD} with respect to the point where D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD).

In the case of A0 : The status that A0 is defined (0.35*IOVDD or 0.65*IOVDD) before more than the time of T_{ACCA0} with respect to the point where D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD).



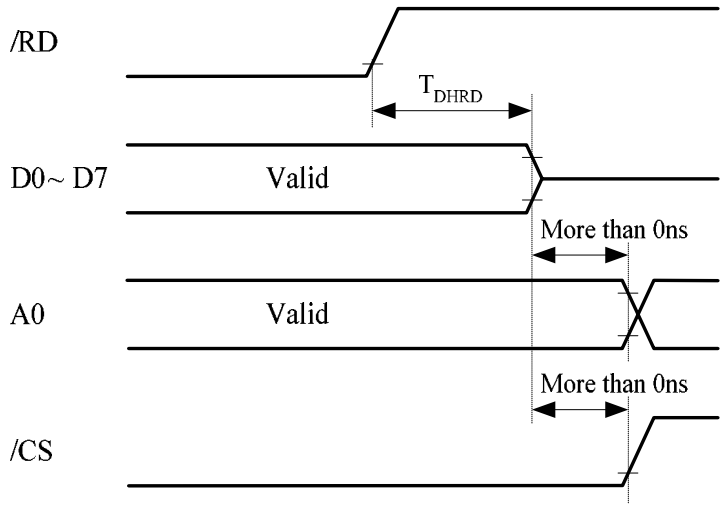
(*2) "~ sufficient hold time" means,

At T_{DHRD} measurement: The status that the enable time of A0 and /CS pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

At T_{DHCS} measurement: The status that the enable time of A0 and /RD pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

AT T_{DHA0} measurement: The status that the enable time of /CS and /RD pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

(Example: At T_{DHRD} measurement)



L4.4.6 Analog Characteristics

Conditions of T_{OP}=25°C, VDD=3.00V, IOVDD=1.80V, and SPVDD=3.60V apply to all items.

○ SP amplifier

Parameter	Min.	Typ.	Max.	Unit
GAIN setting (fixed)		±2		times
Min. load resistance (RL)		8		Ω
Max. output voltage amplitude (RL=8Ω)		6.0		Vp-p
Max. output power (RL=8Ω, THD+N≤1.0%)		580		mW
THD + N (RL=8Ω, f=1 kHz, output = 400mW)		0.025		%
Noise at no signal (A-filter: weighting filter)		-90		dBV
PSRR (f=1 kHz)		90		dB
Amplitude center potential (VSEL2, VSEL1 =0, 0)		0.6×VDD		V
(VSEL2, VSEL1 =0, 1)		0.5×VDD		V
(VSEL2, VSEL1 =1, 0)		0.67×VDD		V
Differential Output Voltage		10	50	mV
Max. load capacity connectable to SPOUT1 and SPOUT2 pin (*)			1000	pF

(*) : The maximum of 1000pF can be connected to SPOUT1 pin,
and the maximum of 1000pF can be connected to SPOUT2 pin.

○ EQ amplifier

Parameter	Min.	Typ.	Max.	Unit
GAIN settable range			30	dB
Max. output voltage amplitude		2.7		Vp-p
THD + N (f=1 kHz)			0.05	%
Noise at no signal (A-filter)		-90		dBV
Input impedance	10			MΩ
Feedback resistance between EQ2 and EQ3	20			kΩ

○ SP Volume

Parameter	Min.	Typ.	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
THD + N (f=1 kHz)			0.05	%

○ EQ Volume

Parameter	Min.	Typ.	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBV
Max. output current	120			μA
Max. output voltage amplitude		1.5		Vp-p
Output impedance		300	600	Ω

○ HP Volume

Parameter	Min.	Typ.	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBV
Max. output current	120			μA
Max. output voltage. amplitude		1.5		Vp-p
Output impedance		300	600	Ω

○ VREF

Parameter	Min.	Typ.	Max.	Unit
VREF voltage		0.5×VDD		V

○ DAC

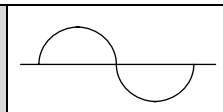
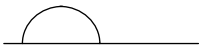
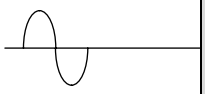
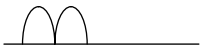
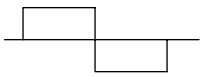
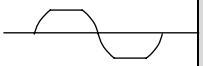
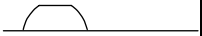
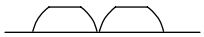
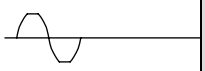
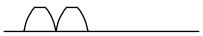
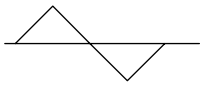
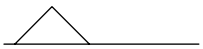
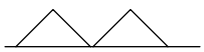
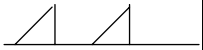
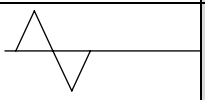
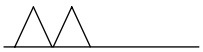
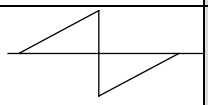
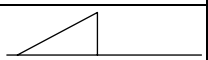
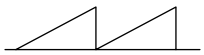
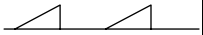
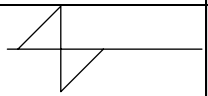
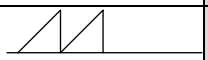
Parameter	Min.	Typ.	Max.	Unit
Resolution		16		Bit
Full scale output voltage		1.5		Vp-p
THD+N (f= 1 kHz)			0.5	%
Noise at no signal (A-filter)		-85	-80	dBV
Frequency response (f=50Hz to 20 kHz)	-3.0 (*)		+0.5	dB

(*): Reduction of response in high frequency range caused by aperture effect

L5 Appendix

L5.1 Information from L3 “Functional Details”

L5.1.1 Basic Waveform Selection of FM Synthesizer & HV Synthesizer

0		1		2		3	
4		5		6		7	
8		9		**10**		11	
12		13		14		15	Any waveform on SRAM is used.
16		17		18		19	
20		21		22		23	Any waveform on SRAM is used.
24		25		26		27	
28		29		30		31	Any waveform on SRAM is used.

L5.1.2 Envelope Rate Table of FM Synthesizer & WT Synthesizer

Unit : ms

RATE	0dB － 96dB	
	ATTACK	DECAY, RELEASE
63~60	0	2.63
59	0.26	3.00
58	0.30	3.50
57	0.34	4.20
56	0.38	5.25
55	0.43	6.01
54	0.53	7.00
53	0.62	8.40
52	0.71	10.50
51	0.82	12.00
50	0.96	14.00
49	1.15	16.80
48	1.44	21.00
47	1.65	24.00
46	1.92	28.00
45	2.23	33.60
44	2.88	42.00
43	3.28	48.00
42	3.83	56.00
41	4.60	67.20
40	5.75	84.00
39	6.56	96.00
38	7.66	112.00
37	9.19	134.40
36	11.49	168.00
35	13.14	192.00
34	15.32	224.00
33	18.39	268.80
32	22.99	336.00
31	26.28	384.00
30	30.66	448.00
29	36.79	537.60
28	45.98	672.00
27	52.55	768.00
26	61.31	896.00
25	73.57	1075.20
24	91.97	1344.00
23	105.09	1536.00
22	122.61	1792.00
21	147.14	2150.41
20	183.92	2688.00
19	210.20	3072.00
18	245.23	3584.00
17	294.28	4300.80
16	367.85	5376.00
15	420.40	6144.00
14	490.47	7168.00
13	588.55	8601.60
12	735.69	10752.01
11	840.80	12288.00
10	980.92	14336.00
9	1177.11	17203.20
8	1471.39	21504.00
7	1681.59	24576.00
6	1961.86	28672.00
5	2354.23	34406.40
4	2942.78	43008.00
0~3	Level maintenance	Level maintenance

L5.1.3 FM Synthesizer Key Scale Level Correspondence Table

Octave / Fnum	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	3.000	6.000	9.000
2	0	0	0	0	3.000	6.000	9.000	12.000
3	0	0	0	1.875	4.875	7.875	10.875	13.875
4	0	0	0	3.000	6.000	9.000	12.000	15.000
5	0	0	1.125	4.125	7.125	10.125	13.125	16.125
6	0	0	1.875	4.875	7.875	10.875	13.875	16.875
7	0	0	2.625	5.625	8.625	11.625	14.625	17.625
8	0	0	3.000	6.000	9.000	12.000	15.000	18.000
9	0	0.750	3.750	6.750	9.750	12.750	15.750	18.750
10	0	1.125	4.125	7.125	10.125	13.125	16.125	19.125
11	0	1.500	4.500	7.500	10.500	13.500	16.500	19.500
12	0	1.875	4.875	7.875	10.875	13.875	16.875	19.875
13	0	2.250	5.250	8.250	11.250	14.250	17.250	20.250
14	0	2.625	5.625	8.625	11.625	14.625	17.625	20.625
15	0	3.000	6.000	9.000	12.000	15.000	18.000	21.000

Note) 1.5 dB/oct is 1/2 of above, 6dB/oct is twice.

Octave = BLOCK + BO

The value of above formula is , if BO=(0, 0): –1, BO=(0, 1): 0, BO=(1, 0): +1, BO=(1, 1): +2.

L5.1.4 FM Synthesizer Detune Correspondence Table

Correspondence table of Setting value – Frequency gap unit : Hz

BLOCK + BO	Key[1:0]	DT[1:0]= 01b	DT[1:0] =10b	DT[1:0] = 11b
0	0	0	0.05	0.09
0	1	0	0.05	0.09
0	2	0	0.05	0.09
0	3	0	0.05	0.09
1	0	0.05	0.09	0.14
1	1	0.05	0.09	0.14
1	2	0.05	0.09	0.14
1	3	0.05	0.09	0.14
2	0	0.05	0.09	0.18
2	1	0.05	0.14	0.18
2	2	0.05	0.14	0.18
2	3	0.05	0.14	0.23
3	0	0.09	0.18	0.23
3	1	0.09	0.18	0.27
3	2	0.09	0.18	0.27
3	3	0.09	0.23	0.32
4	0	0.09	0.23	0.37
4	1	0.14	0.27	0.37
4	2	0.14	0.27	0.41
4	3	0.14	0.32	0.46
5	0	0.18	0.37	0.50
5	1	0.18	0.37	0.55
5	2	0.18	0.41	0.59
5	3	0.23	0.46	0.64
6	0	0.23	0.50	0.73
6	1	0.27	0.55	0.78
6	2	0.27	0.59	0.87
6	3	0.32	0.64	0.91
7	0	0.37	0.73	1.00
7	1	0.37	0.73	1.00
7	2	0.37	0.73	1.00
7	3	0.37	0.73	1.00

How to calculate KEY [1:0] is as follows. (“|” ... OR logic, “&” ... AND logic, “/” ... it is the meaning of bit reversal)

Key1 = FNUM[9]

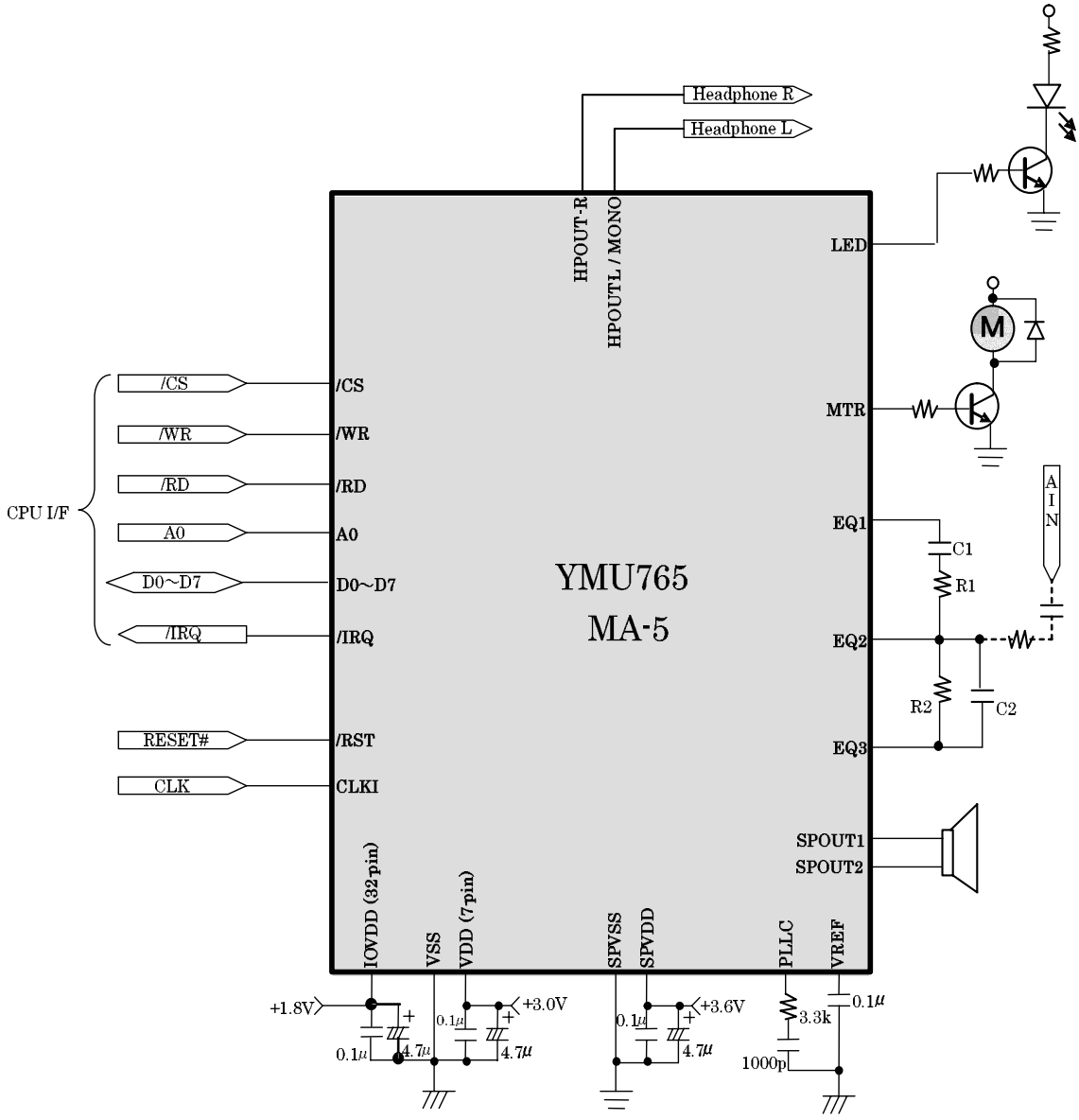
Key0 = FNUM[9] & (FNUM[8] | FNUM[7] | FNUM[6])

+ (/ FNUM[9]) & (FNUM[8] & FNUM[7] & FNUM[6])

L5.1.5 Analog Section Volume Correspondence Table

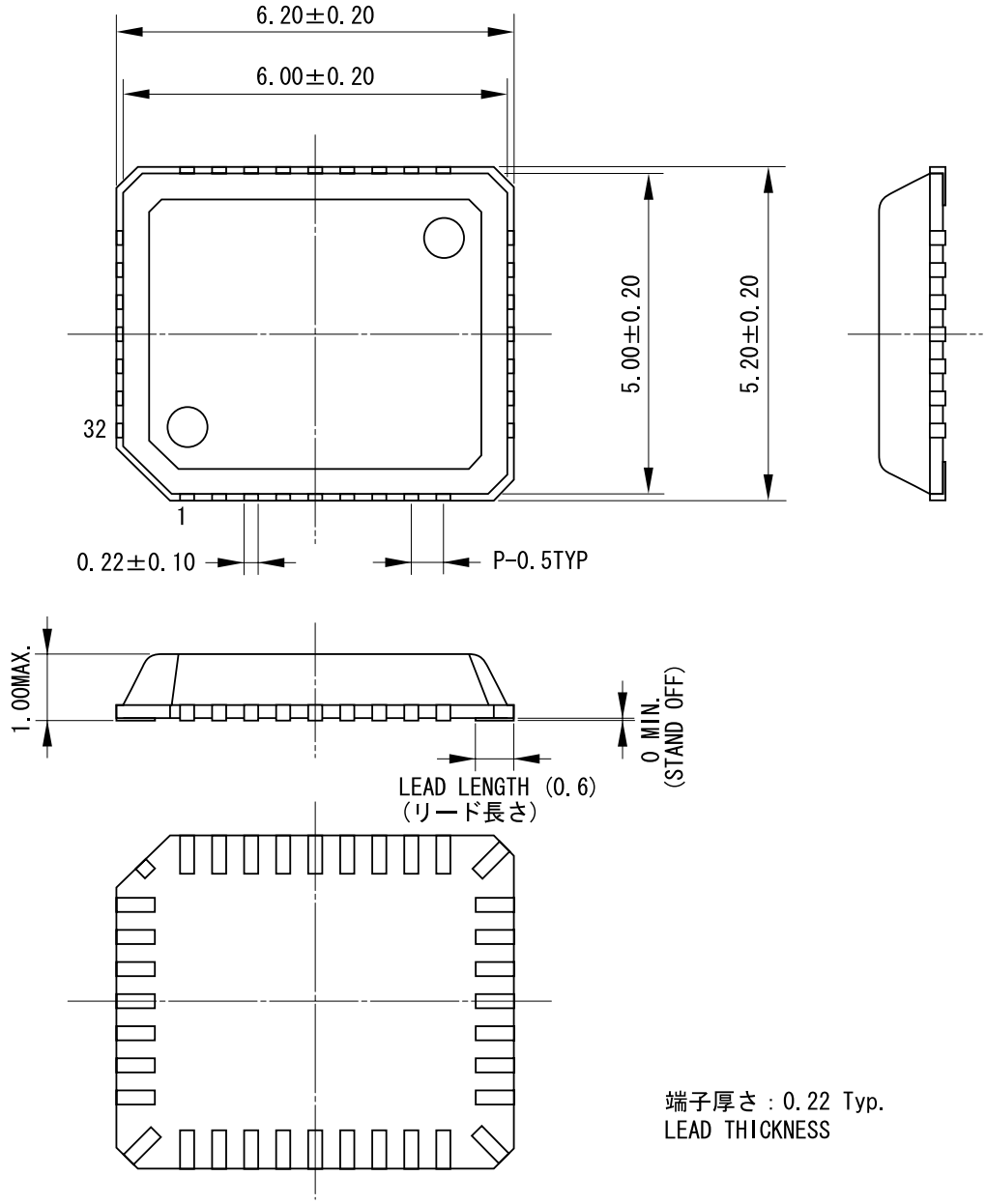
Setting value	Volume (dB)	Setting value	Volume (dB)
0	– ∞	16	–23
1	–30	17	–22
2	–29	18	–21
3	–28	19	–20
4	–27	20	–19
5	–26	21	–18
6	–25	22	–17
7	–24	23	–16
8	–23	24	– 7
9	–22	25	– 6
10	–21	26	– 5
11	–20	27	– 4
12	–19	28	– 3
13	–18	29	– 2
14	–17	30	– 1
15	–16	31	0

L5.2 Example of a Circumference Circuit



L5.3 External Dimensions of Package

C-PK32QP-2



モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注) 表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。
Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
For detailed information, Please contact your nearest Yamaha agent.

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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