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Preliminary
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LM4857 Boomer® Audio Power Amplifier Series
Stereo Audio Sub-system with 3D Enhancement

General Description

The LM4857 is an integrated audio sub-system designed for stereo cell phone applications. Operating on a 3.3V supply, it combines a stereo speaker amplifier delivering 475mW per channel into an 8Ω load, a stereo headphone amplifier delivering 30mW per channel into a 32Ω load, a mono earpiece amplifier delivering 30mW into a 32Ω load, and a line output for an external powered handsfree speaker. It integrates the audio amplifiers, volume control, mixer, power management control, and National 3D enhancement all into a single package. In addition, the LM4857 routes and mixes the stereo and mono inputs into 16 distinct output modes. The LM4857 is controlled through an I^2C compatible interface.

Boomer audio power amplifiers are designed specifically to provide high quality output power with a minimal amount of external components.

The LM4857 is available in a 30-bump ITL package.

Key Specifications

- Pout, Stereo BTL, 8Ω, 3.3V, 1% — 475mW (typ.)
- Pout H/P, 32Ω, 3.3V, 1% — 30mW (typ.)
- Pout Mono Earpiece, 32Ω, 1% — 30mW (typ.)
- Shutdown current — 1μA (typ.)

Features

- Stereo speaker amplifier, 475mW/ch
- Stereo headphone amplifier, 30mW/ch
- Mono earpiece amplifier, 30mW
- Mono Line Output for external handsfree carkit
- Independent Left, Right, and Mono volume controls
- National 3D enhancement
- I^2C compatible interface
- Ultra low shutdown current
- Click and Pop Suppression circuit
- 16 distinct output modes

Applications

- Cell Phones
- PDA,s

Block Diagram

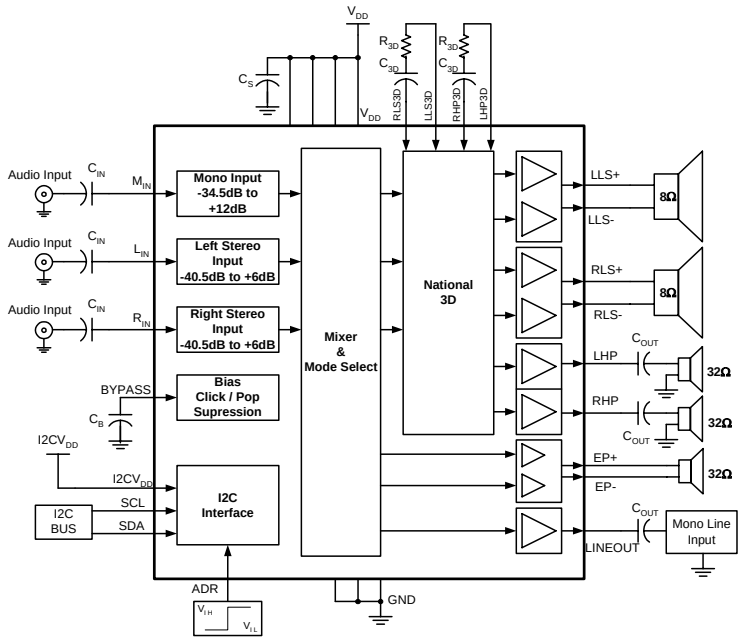

FIGURE 1: Audio Sub-system Block Diagram

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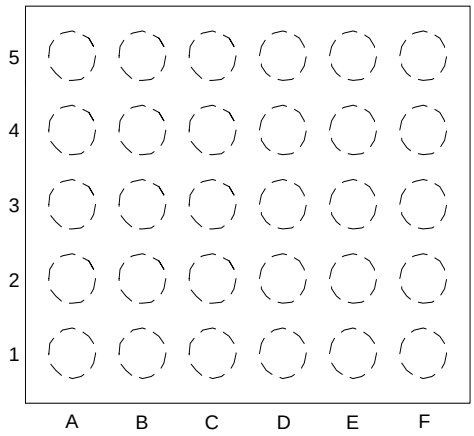
30 Bump ITL Package



Top View
(Bump side down)
Order Number LM4857ITL
See NS Package Number TLA30XXX

Pin Connection

Pin	Name	Pin Description
A1	RLS-	Right Loudspeaker Negative Output
A2	V_{DD}	Power Supply
A3	SDA	Data
A4	RHP3D	Right Headphone 3D
A5	HPR	Right Headphone Output
B1	GND	Ground
B2	I^2CV_{DD}	I^2C Interface Power Supply
B3	ADR	I^2C Address Select
B4	LHP3D	Left Headphone 3D
B5	V_{DD}	Power Supply
C1	RLS+	Right Loudspeaker Positive Output
C2	NC	No Connect
C3	SCL	Clock
C4	LINEOUT	Mono Line Output
C5	GND	Ground
D1	LLS+	Left Loudspeaker Positive Output
D2	V_{DD}	Power Supply
D3	M_{IN}	Mono Input
D4	NC	No Connect
D5	EP-	Mono Earpiece Negative Output
E1	GND	Ground
E2	BYPASS	Half-supply bypass
E3	LLS3D	Left Loudspeaker 3D
E4	R_{IN}	Right Stereo Input
E5	EP+	Mono Earpiece Positive Output
F1	LLS-	Left Loudspeaker Negative Output
F2	V_{DD}	Power Supply
F3	RLS3D	Right Loudspeaker 3D
F4	L_{IN}	Left Stereo Input
F5	HPL	Left Headphone Output

Absolute Maximum Ratings (Note 1, 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150°C

Thermal Resistance

θ_{JA} (TLA30CZA)	TBD

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	-40°C ≤ T_A ≤ +85°C
Supply Voltage	
	2.7V ≤ V_{DD} ≤ 5.5V
	2.7V ≤ I^2CV_{DD} ≤ 5.5V

Audio Amplifier Electrical Characteristics V_{DD} = 5.0V (Notes 1, 2)

The following specifications apply V_{DD} = 5.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4857 Typical (Note 6)	LM4857 Limit (Note 7, 8)	Units (Limits)
I_{DD}	Supply Current	Vin = 0; No Load; LD5 = RD5 = 0			
		Mode 1, 6, 11	6.6	TBD	mA (max)
		Mode 4, 5, 9, 10, 14, 15	5.3	TBD	mA (max)
		Mode 2, 3, 7, 8, 12, 13	14	TBD	mA (max)
I_{SD}	Shutdown Current	Mode 0	1	10	µA (max)
P_O	Output Power	Speaker; THD=1%; f=1kHz, 8Ω BTL	1.1	0.9	W (min)
		Headphone; THD=1%; f=1kHz, 32Ω SE	60	50	mW (min)
		Earpiece; THD=1%; f=1kHz, 32Ω BTL; CD4 = 0	85	65	mW (min)
		Earpiece; THD=1%; f=1kHz, 32Ω BTL; CD4 = 1	100		mW
THD+N	Total Harmonic Distortion	LD5 = RD5 = 0			
		Speaker; Po = 500mW; f=1kHz; 8Ω BTL	0.2		%
		Headphone; Po = 30mW; f = 1kHz; 32Ω SE	0.1		%
		Earpiece; Po =40mW; f = 1kHz; 32Ω BTL; CD4 = 0	0.1		%
		Line Out; Vo = 1Vrms; f=1kHz; 10kΩ SE	0.1		%
Vos	Offset Voltage	Speaker; LD5 = RD5 = 0	5	30	mV (max)
		Earpiece; LD5 = RD5 = 0	5	30	mV (max)
Nout	Output Noise	A=weighted; 0dB gain; LD5 = RD5 = 0			
		Speaker; Mode 2, 3, 7, 8	34		µV
		Speaker; Mode 12, 13	47		µV

		Headphone; Mode 3, 4, 8, 9	13		µV
		Headphone; Mode 13, 14	19		µV
		Earpiece; Mode 1; CD4 = 0	18		µV
		Earpiece; Mode 6	25		µV
		Earpiece; Mode 11	28		µV
		Line Out; Mode 5	13		µV
		Line Out; Mode 10	19		µV
		Line Out; Mode 15	26		µV
PSRR	Power Supply Rejection	f = 217Hz; Vrip=200mVpp; 0dB Gain Setting; C_B = 2.2uF LD5 = RD5 = 0			
		Speaker; Mode 2, 3, 7, 8	68		dB
		Speaker; Mode 12, 13	62	TBD	dB (min)
		Headphone; Mode 3, 4, 8, 9	70		dB
		Headphone; Mode 13, 14	70	TBD	dB (min)
		Earpiece; Mode 1	70		dB
		Earpiece; Mode 6	70		dB
		Earpiece; Mode 11	66	TBD	dB (min)
		Line Out; Mode 5	70		dB
		Line Out; Mode 10	70		dB
		Line Out; Mode 15	66	TBD	dB (min)
Xtalk	Crosstalk	LD5 = RD5 = 0			
		Loudspeaker; Po=400mW; f = 1kHz	55		dB
		Headphone; Po=15mW; f = 1kHz	55		dB
T_{WU}	Wake-up Time	CD5 = 0; C_B = 2.2uF	120	TBD	ms (max)
		CD5 = 1; C_B = 2.2uF	230	TBD	ms (max)

Audio Amplifier Electrical Characteristics V_{DD} = 3.0V (Notes 1, 2)

The following specifications apply V_{DD} = 3.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4857		Units (Limits)
			Typical (Note 6)	Limit (Note 7, 8)	
I_{DD}	Supply Current	Vin = 0; No Load; LD5 = RD5 = 0			
		Mode 1, 6, 11	6	TBD	mA (max)
		Mode 4, 5, 9, 10, 14, 15	5	TBD	mA (max)

		Mode 2, 3, 7, 8, 12, 13	12	TBD	mA (max)
I_{SD}	Shutdown Current	Mode 0	1	10	μA (max)
P_O	Output Power	Speaker; THD=1%; f=1kHz, 8Ω BTL	350	320	mW (min)
		Headphone; THD=1%; f=1kHz, 32Ω SE	25	18	mW (min)
		Earpiece; THD=1%; f=1kHz, 32Ω BTL; CD4 = 0	25	18	mW (min)
		Earpiece; THD=1%; f=1kHz, 32Ω BTL; CD4 = 1	25		mW
THD+N	Total Harmonic Distortion	LD5 = RD5 = 0			
		Speaker; Po = 200mW; f=1kHz; 8Ω BTL	0.2		%
		Headphone; Po = 10mW; f = 1kHz; 32Ω SE	0.1		%
		Earpiece; Po =10mW; f = 1kHz; 32Ω BTL; CD4 = 0	0.1		%
		Line Out; Vo = 1Vrms; f=1kHz; 10kΩ SE	0.1		%
Vos	Offset Voltage	Speaker; LD5 = RD5 = 0	5	30	mV (max)
		Earpiece; LD5 = RD5 = 0	5	30	mV (max)
Nout	Output Noise	A=weighted; 0dB gain; LD5 = RD5 = 0			
		Speaker; Mode 2, 3, 7, 8	34		μV
		Speaker; Mode 12, 13	47		μV
		Headphone; Mode 3, 4, 8, 9	13		μV
		Headphone; Mode 13, 14	19		μV
		Earpiece; Mode 1	18		μV
		Earpiece; Mode 6	25		μV
		Earpiece; Mode 11	28		μV
		Line Out; Mode 5	13		μV
		Line Out; Mode 10	19		μV
		Line Out; Mode 15	26		μV
PSRR	Power Supply Rejection	f = 217Hz; Vrip=200mVpp; 0dB Gain Setting; C_B = 2.2uF LD5 = RD5 = 0			
		Speaker; Mode 2, 3, 7, 8	68		dB
		Speaker; Mode 12, 13	62	TBD	dB (min)
		Headphone; Mode 3, 4, 8, 9	70		dB
		Headphone; Mode 13, 14	70	TBD	dB (min)
		Earpiece; Mode 1	70		dB

		Earpiece; Mode 6	70		dB
		Earpiece; Mode 11	66	TBD	dB (min)
		Line Out; Mode 5	70		dB
		Line Out; Mode 10	70		dB
		Line Out; Mode 15	66	TBD	dB (min)
Xtalk	Crosstalk	LD5 = RD5 = 0			
		Loudspeaker; Po=200mW; f = 1kHz	55		dB
		Headphone; Po=10mW; f = 1kHz	55		dB
Twu	Wake-up Time	CD5 = 0; C_B = 2.2uF	80	TBD	ms (max)
		CD5 = 1; C_B = 2.2uF	140	TBD	ms (max)

Volume Control Electrical Characteristics (Notes 1, 2)

The following specifications apply for $3V \le V_{DD} \le 5V$ and $3V \le I^2CV_{DD} \le 5V$, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4857		Units (Limits)
			Typical (Note 6)	Limit (Note 7, 8)	
	Stereo Volume Control Range	maximum gain setting	6	5.5	dB (min)
				6.5	dB (max)
		minimum gain setting	-40.5	-41	dB (min)
				-40	dB (max)
	Mono Volume Control Range	maximum gain setting	12	11.5	dB (min)
				12.5	dB (max)
		minimum gain setting	-34.5	-35	dB (min)
				-34	dB (max)
	Volume Control Step Size		1.5		dB
	Volume Control Step Size Error		+/- 0.2	+/- 0.5	dB (max)
	Stereo Channel to Channel Gain Mismatch		0.3		dB
	Mute Attenuation	mode 12; Vin = 1Vrms			
		Headphone	70	TBD	dB (min)
		Line Out	70	TBD	dB (min)
	L_{IN} and R_{IN} Input Impedance	maximum gain setting	33.5	25	kΩ (min)
				42	kΩ (max)
		minimum gain setting	100	75	kΩ (min)
				125	kΩ (max)
	M_{IN} Input Impedance	maximum gain setting	20	15	kΩ (min)
				25	kΩ (max)

		minimum gain setting	98	73	kΩ (min)
				123	kΩ (max)

Control Interface Electrical Characteristics (Notes 1, 2)

The following specifications apply for $3V \le V_{DD} \le 5V$ and $3V \le I^2CV_{DD} \le 5V$, unless otherwise specified.
Limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	LM4857		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7, 8)	
t_1	SCL period			2.5	µs (min)
t_2	SDA Setup Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}	Digital Input High Voltage			0.7 x I^2CV_{DD}	V (min)
V_{IL}	Digital Input Low Voltage			0.3 x I^2CV_{DD}	V (max)

Note 1: All voltages are measured with respect to the GND pin unless other wise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4857 typical application with $V_{DD} = 3.3V$, $R_L = 8\Omega$ stereo operation the total power dissipation isTBDW. θ_{JA} = TBD°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Machine Model, 220pF-240pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: Shutdown current is measured in a normal room environment.

Application Information

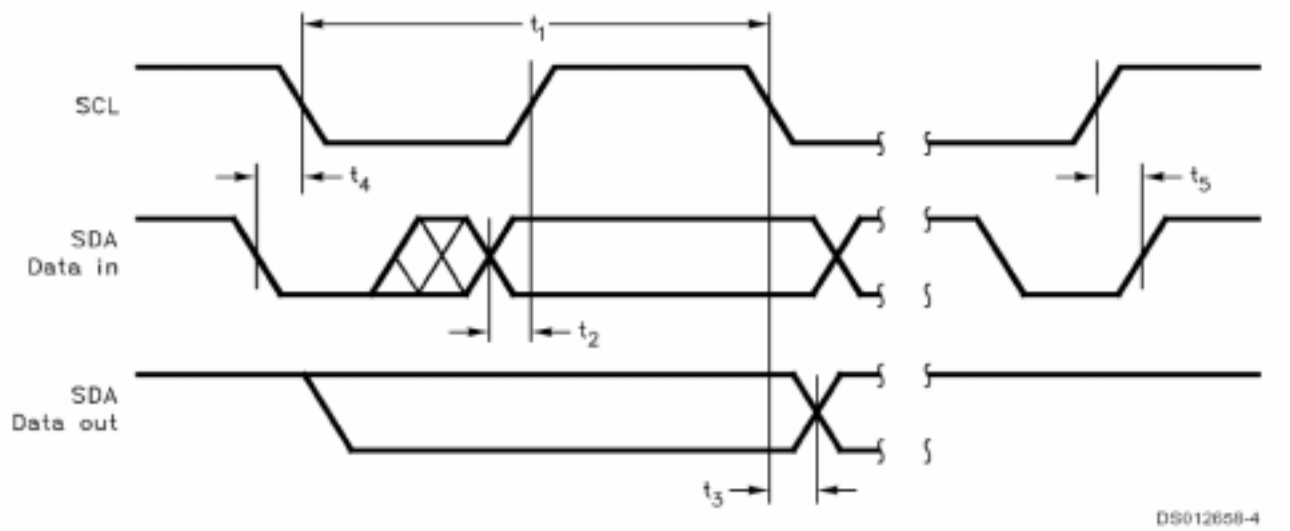


FIGURE 2: I²C Timing Diagram

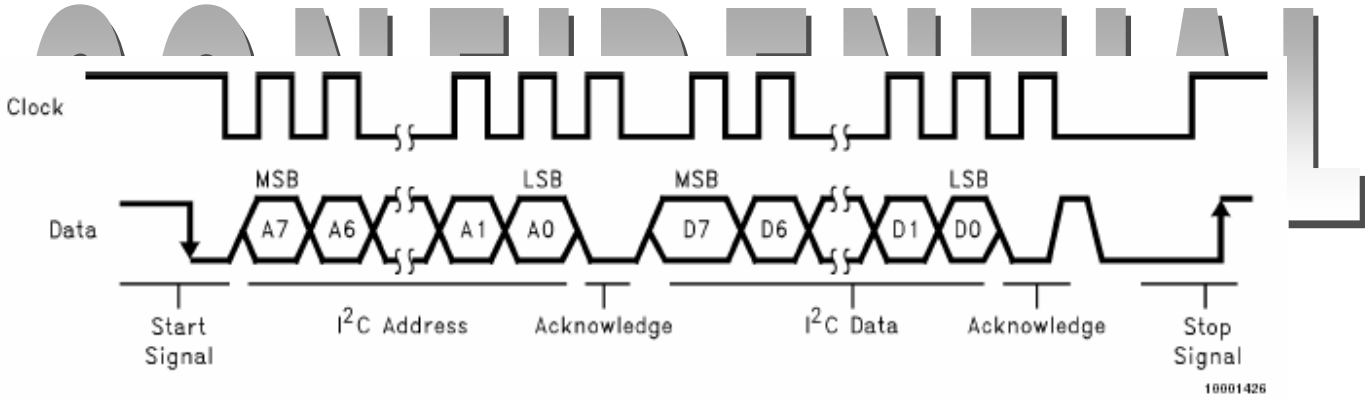


FIGURE 3: I²C Bus Format

Table 1. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	EC	0
ADR = 0	1	1	1	1	1	0	0	0
ADR = 1	1	1	1	1	1	0	1	0

EC – externally configured by ADR pin

Table 2. Control Registers

	D7	D6	D5	D4	D3	D2	D1	D0
Mono Volume control	0	0	0	MD4	MD3	MD2	MD1	MD0
Left Volume control	0	1	LD5	LD4	LD3	LD2	LD1	LD0
Right Volume control	1	0	RD5	RD4	RD3	RD2	RD1	RD0
Mode Control	1	1	CD5	CD4	CD3	CD2	CD1	CD0

Table 3. Mono Volume Control

MD4	MD3	MD2	MD1	MD0	Gain (dB)
0	0	0	0	0	-34.5
0	0	0	0	1	-33
0	0	0	1	0	-31.5
0	0	0	1	1	-30
0	0	1	0	0	-28.5
0	0	1	0	1	-27
0	0	1	1	0	-25.5
0	0	1	1	1	-24
0	1	0	0	0	-22.5
0	1	0	0	1	-21
0	1	0	1	0	-19.5
0	1	0	1	1	-18
0	1	1	0	0	-16.5
0	1	1	0	1	-15
0	1	1	1	0	-13.5
0	1	1	1	1	-12
1	0	0	0	0	-10.5
1	0	0	0	1	-9
1	0	0	1	0	-7.5
1	0	0	1	1	-6
1	0	1	0	0	-4.5
1	0	1	0	1	-3
1	0	1	1	0	-1.5
1	0	1	1	1	0
1	1	0	0	0	1.5
1	1	0	0	1	3
1	1	0	1	0	4.5
1	1	0	1	1	6
1	1	1	0	0	7.5
1	1	1	0	1	9
1	1	1	1	0	10.5
1	1	1	1	1	12

Table 4. Stereo Volume Control

LD4 // RD4	LD3 // RD3	LD2 // RD2	LD1 // RD1	LD0 // RD0	Gain (dB)
0	0	0	0	0	-40.5
0	0	0	0	1	-39
0	0	0	1	0	-37.5
0	0	0	1	1	-36
0	0	1	0	0	-34.5
0	0	1	0	1	-33
0	0	1	1	0	-31.5
0	0	1	1	1	-30
0	1	0	0	0	-28.5
0	1	0	0	1	-27
0	1	0	1	0	-25.5
0	1	0	1	1	-24
0	1	1	0	0	-22.5
0	1	1	0	1	-21
0	1	1	1	0	-19.5
0	1	1	1	1	-18
1	0	0	0	0	-16.5
1	0	0	0	1	-15
1	0	0	1	0	-13.5
1	0	0	1	1	-12
1	0	1	0	0	-10.5
1	0	1	0	1	-9
1	0	1	1	0	-7.5
1	0	1	1	1	-6
1	1	0	0	0	-4.5
1	1	0	0	1	-3
1	1	0	1	0	-1.5
1	1	0	1	1	0
1	1	1	0	0	1.5
1	1	1	0	1	3
1	1	1	1	0	4.5
1	1	1	1	1	6

Table 5. Mixer and Output Mode Control

Mode	CD 3	CD 2	CD 1	CD 0	Mono Line Out	Mono Earpiece		Loud-speaker L	Loud-speaker R	Head-phone L	Head-phone R
						(CD4 = 0)	(CD4 = 1)				
0	0	0	0	0	SD	SD	SD	SD	SD	SD	SD
1	0	0	0	1	MUTE	(G_M x M)	2(G_M x M)	SD	SD	MUTE	MUTE
2	0	0	1	0	MUTE	SD	SD	2(G_M x M)	2(G_M x M)	MUTE	MUTE
3	0	0	1	1	MUTE	SD	SD	2(G_M x M)	2(G_M x M)	(G_M x M)	(G_M x M)
4	0	1	0	0	MUTE	SD	SD	SD	SD	(G_M x M)	(G_M x M)
5	0	1	0	1	(G_M x M)	SD	SD	SD	SD	MUTE	MUTE
6	0	1	1	0	MUTE	(G_L x L) + (G_R x R)	2(G_L x L) + 2(G_R x R)	SD	SD	MUTE	MUTE
7	0	1	1	1	MUTE	SD	SD	2(G_L x L)	2(G_R x R)	MUTE	MUTE
8	1	0	0	0	MUTE	SD	SD	2(G_L x L)	2(G_R x R)	(G_L x L)	(G_R x R)
9	1	0	0	1	MUTE	SD	SD	SD	SD	(G_L x L)	(G_R x R)
10	1	0	1	0	(G_L x L) + (G_R x R)	SD	SD	SD	SD	MUTE	MUTE
11	1	0	1	1	MUTE	(G_M x M) + (G_L x L) + (G_R x R)	2(G_M x M) + 2(G_L x L) + 2(G_R x R)	SD	SD	MUTE	MUTE
12	1	1	0	0	MUTE	SD	SD	2(G_L x L) + 2(G_M x M)	2(G_R x R) + 2(G_M x M)	MUTE	MUTE
13	1	1	0	1	MUTE	SD	SD	2(G_L x L) + 2(G_M x M)	2(G_R x R) + 2(G_M x M)	(G_L x L) + (G_M x M)	(G_R x R) + (G_M x M)
14	1	1	1	0	MUTE	SD	SD	SD	SD	(G_L x L) + (G_M x M)	(G_R x R) + (G_M x M)
15	1	1	1	1	(G_M x M) + (G_L x L) + (G_R x R)	SD	SD	SD	SD	MUTE	MUTE

M – M_{IN} Input Level
L – L_{IN} Input Level
R – R_{IN} Input Level
G_M – Mono Volume Control Gain
G_L – Left Stereo Volume Control Gain
G_R – Right Stereo Volume Control Gain
SD – Shutdown
MUTE – Mute

Table 6. National 3D Enhancement

LD5	0	Internal HandsFree National 3D Off
	1	Internal HandsFree National 3D ON
RD5	0	HeadPhone National 3D Off
	1	HeadPhone National 3D ON

Table 7. Wake-up Time Select

CD5	0	Fast Wake-up Setting
	1	Slow Wake-up Setting

Table 8. Earpiece Amplifier Gain Select

CD4	0	0dB Earpiece Output Stage Gain Setting
	1	6dB Earpiece Output Stage Gain Setting

Application Information

I^2C Compatible Interface

The LM4857 uses a serial bus, which conforms to the I^2C protocol, to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector) with a pullup resistor (typically 10kΩ). The maximum clock

frequency specified by the I^2C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4857.

The I^2C address for the LM4857 is determined using the ADR pin. The LM4857's two possible I^2C chip addresses are of the form $111110X_10$ (binary), where X_1 = 0, if ADR is logic low; and X_1 = 1, if ADR is logic high. If the I^2C interface is used to address a number of chips in a system, the LM4857's chip address can be changed to avoid any possible address conflicts.

The bus format for the I^2C interface is shown in Figure 3. The data is latched in on the rising edge of the clock. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the clock level is high.

After the last bit of the address bit is sent, the master checks for the LM4857's acknowledge. The master releases the data line high (through a pullup resistor). Then the master sends a clock pulse. If the LM4857 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not low, then the master should send a "stop" signal (discussed later) and abort the transfer.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must check for another acknowledge to see if the LM4857 received the data.

If the master has more data bytes to send to the LM4857, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes high while the clock signal is high. The data line should be held high when not in use.

I^2C Interface Power Supply Pin (I^2CV_{DD})

The LM4857's I^2C interface is powered up through the I^2CV_{DD} pin. The LM4857's I^2C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I^2C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

Application Information

National 3D Enhancement

The LM4857 features a 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement improves the apparent stereo channel separation whenever the left and right speakers are too close to one another, due to system size constraints or equipment limitations.

An external RC network, shown in Figure 1, is required to enable the 3D effect. There are separate RC networks for both the stereo loudspeaker outputs as well as the stereo headphone outputs, so the 3D effect can be set independently for each set of stereo outputs.

The amount of the 3D effect is set by the R_{3D} resistor. Decreasing the value of R_{3D} will increase the 3D effect. The C_{3D} capacitor sets the low cutoff frequency of the 3D effect. Increasing the value of C_{3D} will decrease the low cutoff frequency at which the 3D effect starts to occur, as shown by Equation 1.

$$f_{3D(-3dB)} = 1 / 2\Pi(R_{3D})(C_{3D}) \quad (1)$$

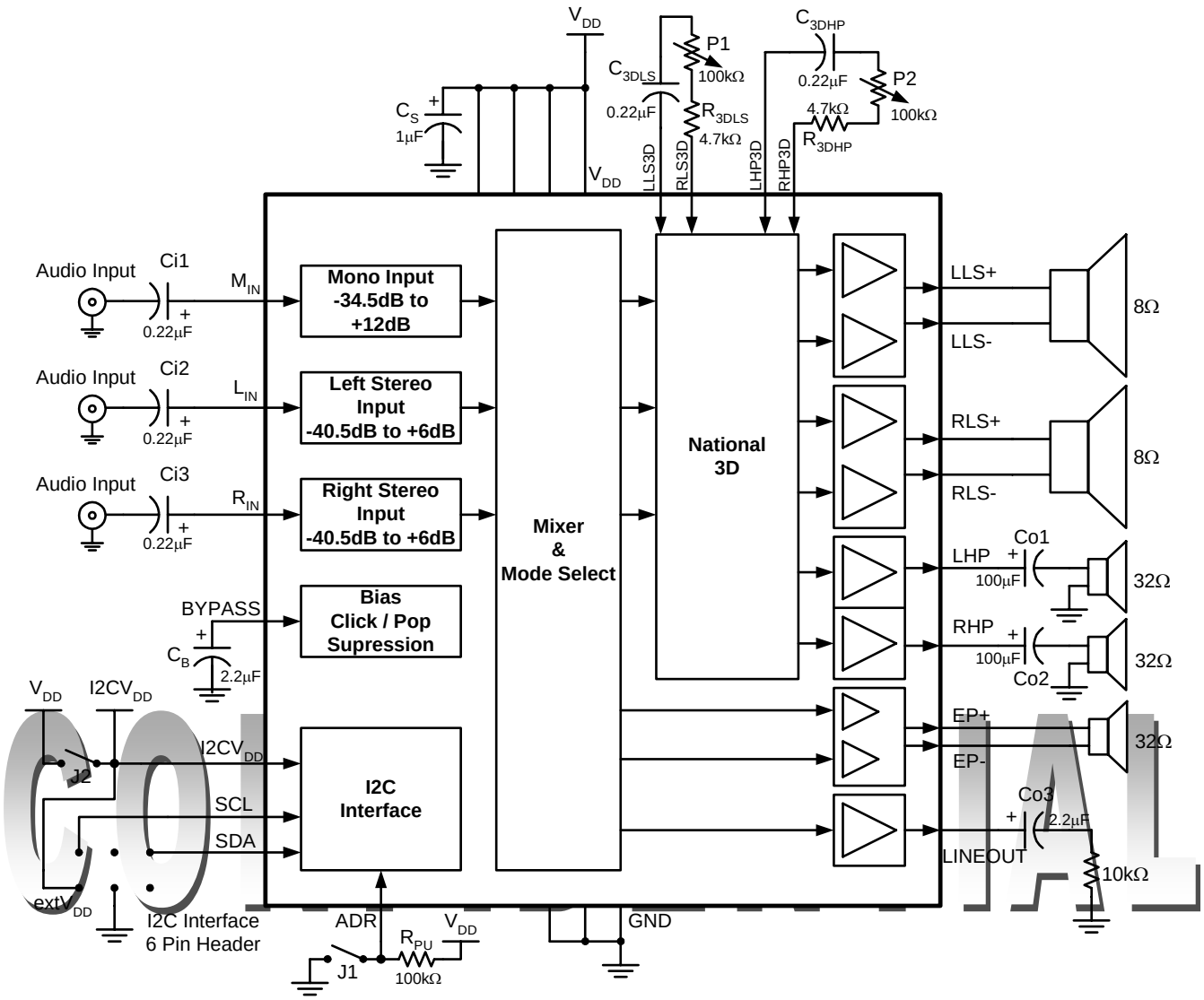


Figure 4: Reference Design Board Schematic

Demonstration Board Layout

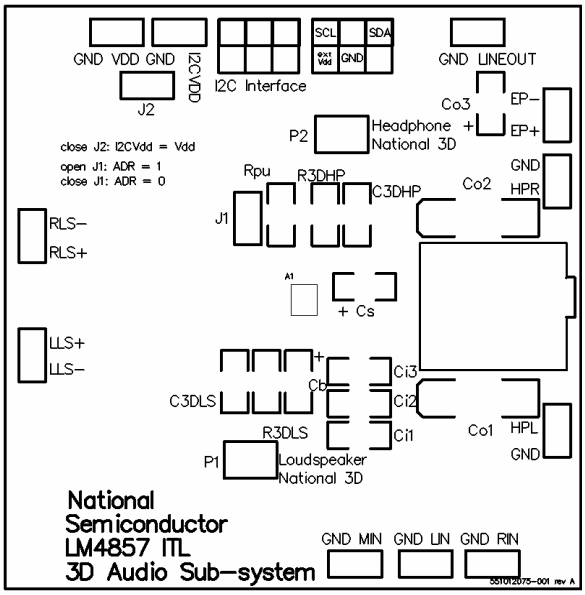


Figure 5. Recommended ITL PCB Layout
Top Silkscreen

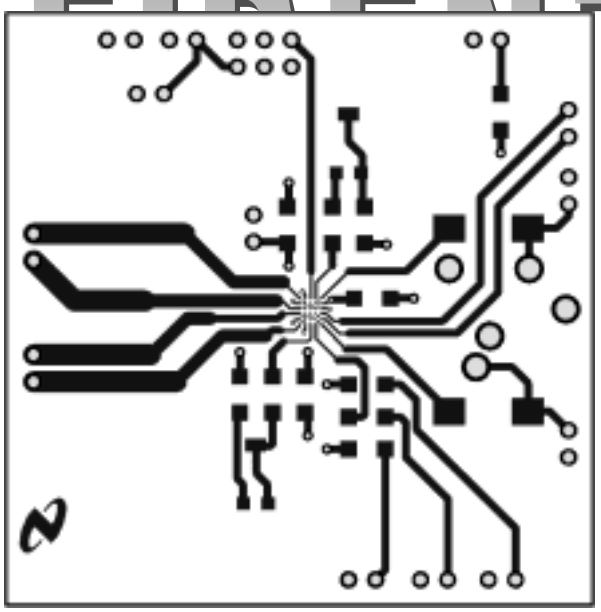


Figure 6. Recommended ITL PCB Layout
Top Layer

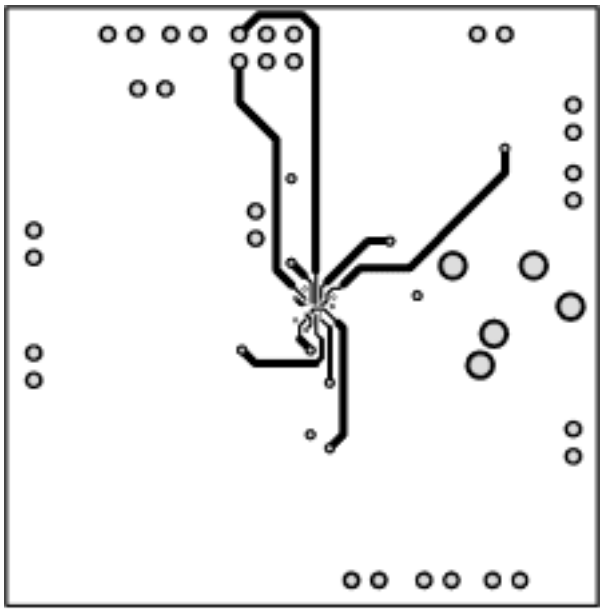


Figure 7. Recommended ITL PCB Layout
Inner Layer 1

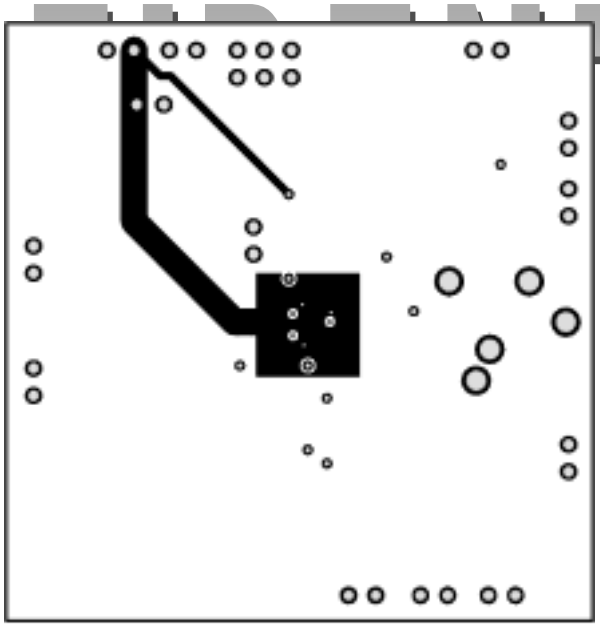


Figure 8. Recommended ITL PCB Layout
Inner Layer 2

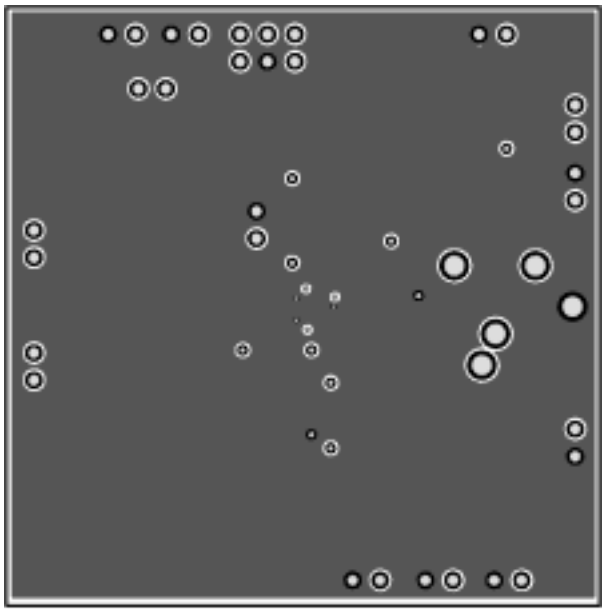
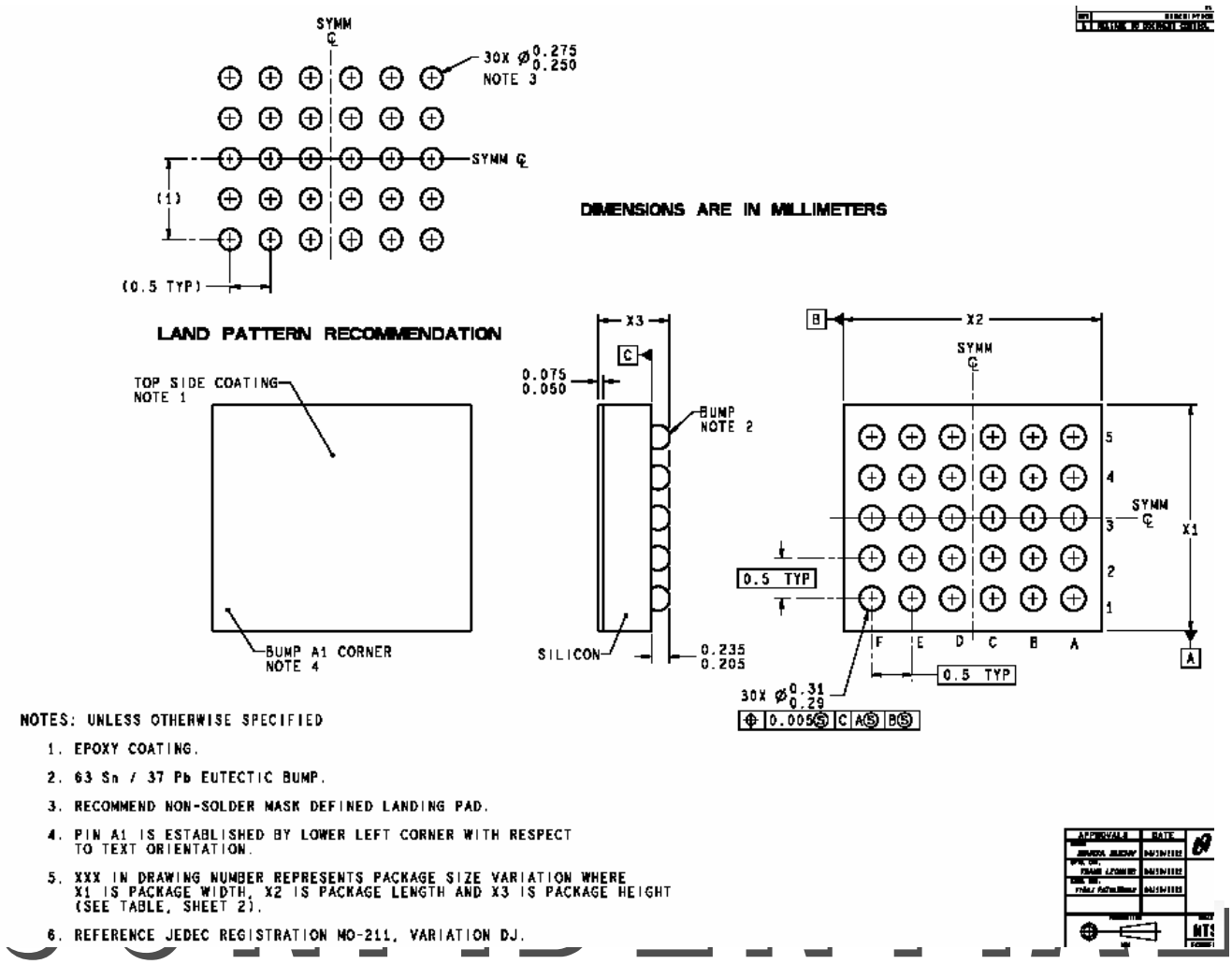


Figure 9. Recommended ITL PCB Layout
Bottom Layer

Physical Dimensions (millimeters unless otherwise noted)



30 Bump ITL
Order Number LM4857ITL
NS Package Number TLA30CZA
$X_1 = 2.543 \pm 0.03$ $X_2 = 2.949 \pm 0.03$ $X_3 = 0.6 \pm 0.075$

Notes

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