Challenge_19_Combined Report Binary LIF Neuron and DC-DC Converter Topologies

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1. Introduction

This report integrates two domains: neuromorphic computing using binary Leaky Integrate-and-Fire (LIF) neurons, and energy transformation via DC-DC converters. It includes simulations, Verilog implementations, behavioral models, and conceptual schematics to illustrate both computational and electrical characteristics.

2. Binary Leaky Integrate-and-Fire (LIF) Neuron

2.1 Model Description

The LIF neuron integrates input pulses over time, applies a leak factor, and fires when a threshold is reached. It resets after spiking, mimicking real neural firing behavior.

2.2 Python Code

Python code is used to simulate multiple input conditions and observe how the neuron behaves under various stimuli.

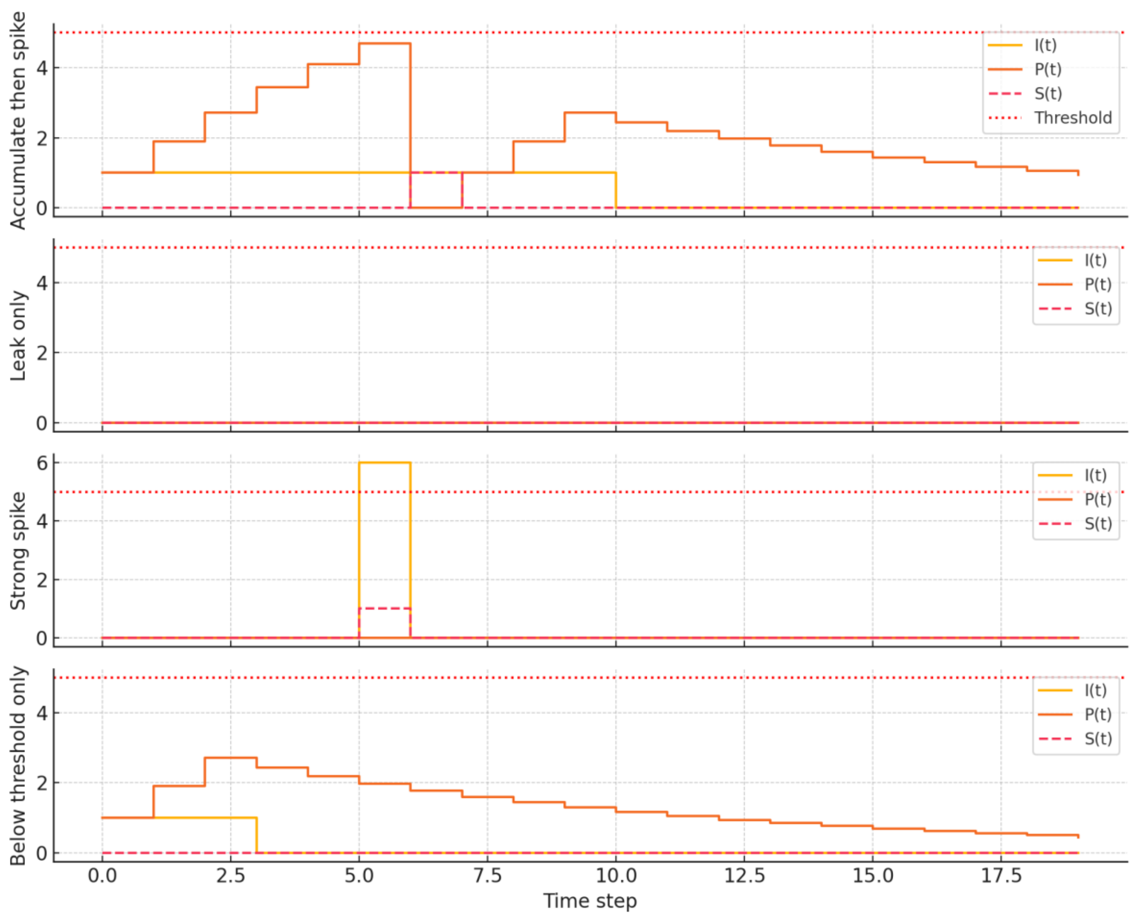

Figure: LIF Neuron Simulation under multiple input conditions.

2.3 Conceptual Schematic

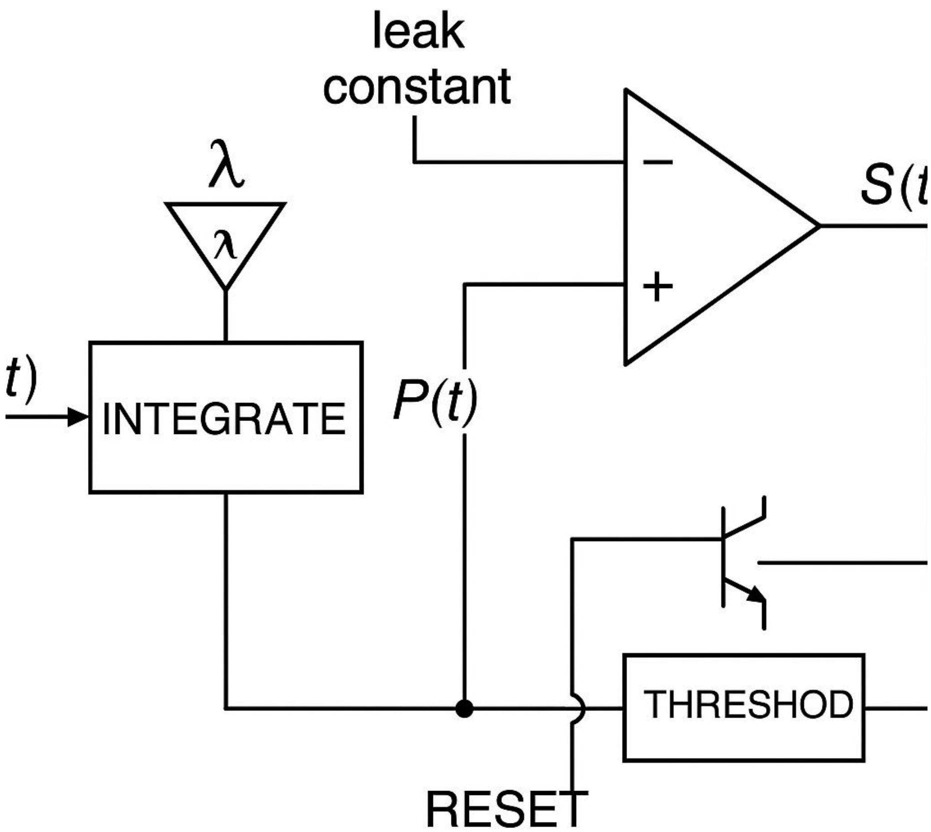

Figure: Conceptual Schematic of the Binary LIF Neuron.

3. DC-DC Converter Topologies

3.1 Behavioral Models

The following are simplified behavioral Verilog models:

• Buck Converter

Verilog behavioral code for the Buck converter is included in the full report.

• Boost Converter

Verilog behavioral code for the Boost converter is included in the full report.

• Buck-Boost Converter

Verilog behavioral code for the Buck-Boost converter is included in the full report.

• Ćuk Converter

Verilog behavioral code for the Ćuk converter is included in the full report.

4. Simulation Results

The following plot shows the output voltage of each converter as a function of duty cycle.

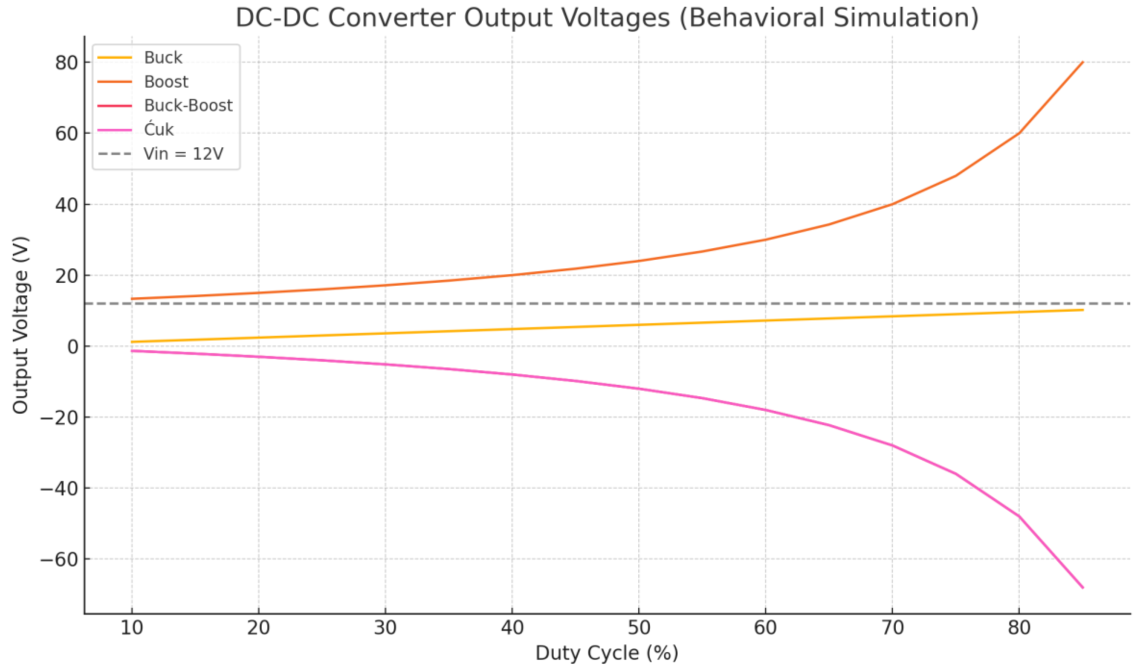

Figure: DC-DC Converter Output Voltages vs Duty Cycle.

5. Conclusion

Both the LIF neuron and the DC-DC converters exhibit dynamic behaviors that can be modeled using Verilog. Their simulation and schematic representation help in understanding the fundamentals of neuromorphic hardware and power electronics.

6. Appendix: Figure Descriptions

Figure A1: The schematic shows how input is integrated, compared, and reset in the LIF model.
Figure A2: Simulates four different input scenarios and shows how the neuron reacts.
Figure A3: Illustrates the behavior of four DC-DC converters across varying PWM duty cycles.