ECE510 Final Project Report

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Section 14: Documentation Audit and Reflection (Challenge #29)

Challenge #29 Documentation Audit: ECE510 Final Project

Project Title:
Comparative Analysis and Acceleration of Buck, Boost, Buck-Boost, and Ćuk Converters

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1. Technical Success Criteria (Project Goals Achieved)
Criterion	Status	Evidence
SW Benchmarking & Bottleneck ID	✅	Identified Buck as fastest; detailed waveform comparison
HW Accelerator Design	✅	Fast Buck topology using reduced LC, GaN/SiC transistors
ASIC-Level Synthesis Consideration	✅ Planned (❌ Implemented)	Mentioned OpenLane in Future Work
Co-Design Methodology	✅	LSTM + Verilog + LIF SNN integration
Full-System Benchmarking	✅	Waveform simulations for each converter and co-processor

2. Project Organization
- Structured Sections: Clear organization by topics (Converter Theory, PWM Simulations, Neuromorphic Control, etc.)
- Early Overview: Introduction answers Heilmeier questions in plain English.
- Architecture Visuals: Diagrams of converter circuits and simulation waveforms included.

3. Architecture Documentation
- Partitioning Rationale: Buck converter selected for acceleration due to fastest analog response.
- Communication Protocols: LIF spike signals used to control PWM, simulating biological neuron input.
- Design Decisions:
  - Lowered L, increased C to achieve critical damping
  - Used GaN switches for MHz-class PWM

4. Code and Documentation Standards

Code Type	Comments/Docstrings Present	Functional Description	AI Acknowledgement
Python	✅	LSTM, waveform generation, and PWM control simulation	
Verilog	✅	LIF neuron, ML coprocessor, PWM module all explained	
CUDA	✅	Parallel PWM analogy kernel	

5. Hardware-Specific Documentation
- Verification Strategy: Waveform outputs interpreted with time-domain results.
- Key Metrics:
  - PWM frequency sweep: 100kHz to 1MHz
  - Output voltage stabilization time measured
- Tools: Python + Verilog + SPICE/PECS-based simulation.

6. Graduate-Level Depth
- Heilmeier Qs: Fully answered in Intro
- References:
  1. Erickson & Maksimovic (Power Electronics)
  2. Sedra & Smith (Microelectronics)
  3. Johns Hopkins LLM Neuron Paper
  4. Mead (Analog VLSI)
  5. BrainChip Akida Datasheet
- Results: All topologies compared quantitatively via waveform simulation
- Future Work: ASIC flow (OpenLane), SNN-LSTM hybrid logic, FPGA prototyping

PDF Summary Sheet (to Accompany Submission)
Title: Buck, Boost, Buck-Boost, and Ćuk Converter Acceleration via Neuromorphic Co-Processing

Highlights:
- Buck Converter = Fastest in output rise and stability
- Acceleration via:
  - Lower L, Higher C, MHz PWM
  - GaN-based switching
  - LSTM for prediction
  - LIF neuron for control

Waveform Evidence:
- Included: Buck voltage rise vs frequency (100kHz to 1MHz)
- Included: 4 topology comparisons of Vout

Conclusion:

Project meets or exceeds all ECE510 Challenge #29 documentation requirements. Strong blend of simulation, architecture explanation, co-processor integration, and AI-guided design rationale.