Computer Organization

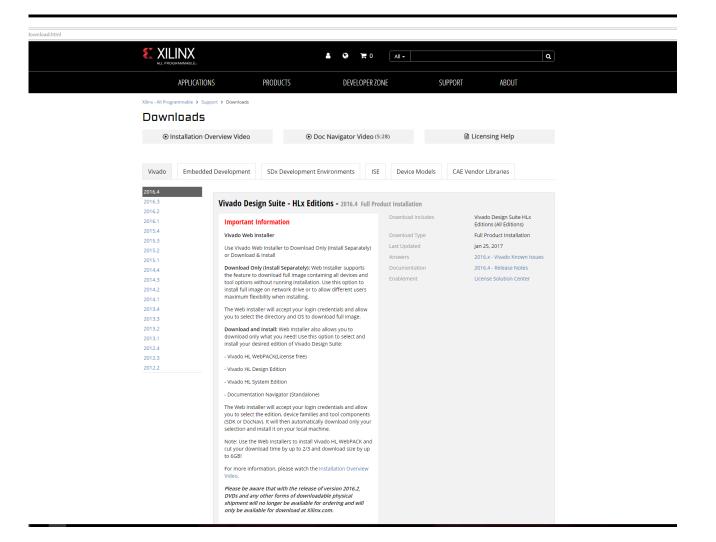
[Introduction to VIVADO]

Sunghwa Lee (sunghwa2@snu.ac.kr)
High Performance Computer Systems (HPCS) Lab.
March 16th, 2017

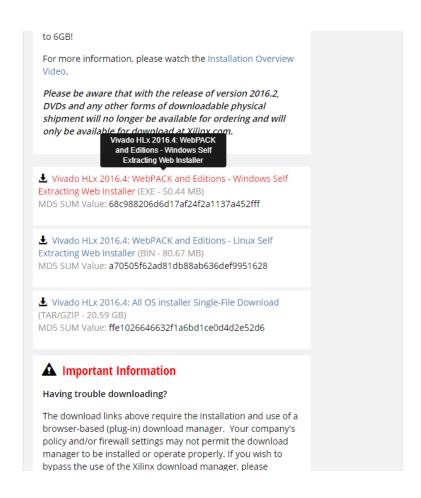
1. Go to Xilinx Website

Use below link:

https://www.xilinx.com/support/download.html

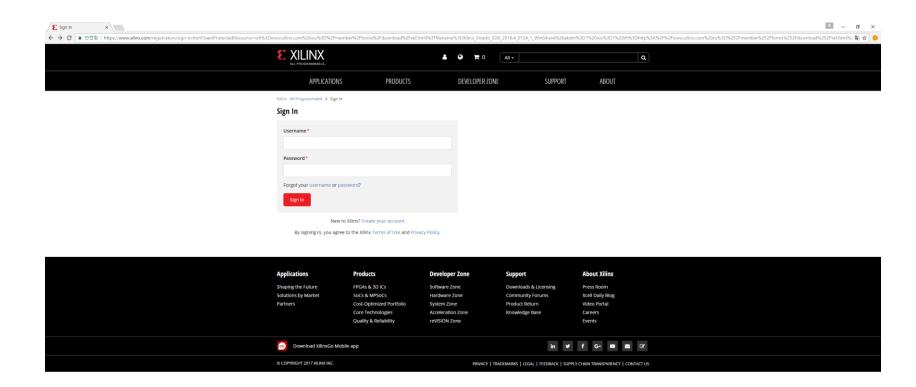


2. Download Vivado HLx 2016.4: WebPACK and Editions



In this guide, we assume you are using Microsoft Windows 10. You may want to use other distributions (e.g., linux), but we recommend to use Windows, because we will use Windows 10 for grading.

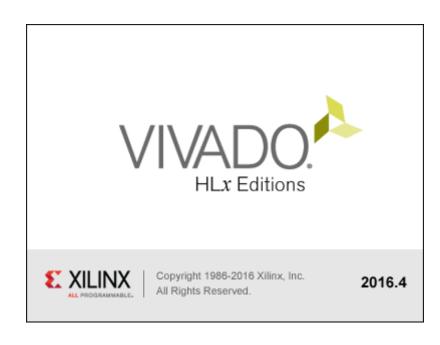
2-1. Sign in the Xilinx account. If you don't have the account, the you should create your account.



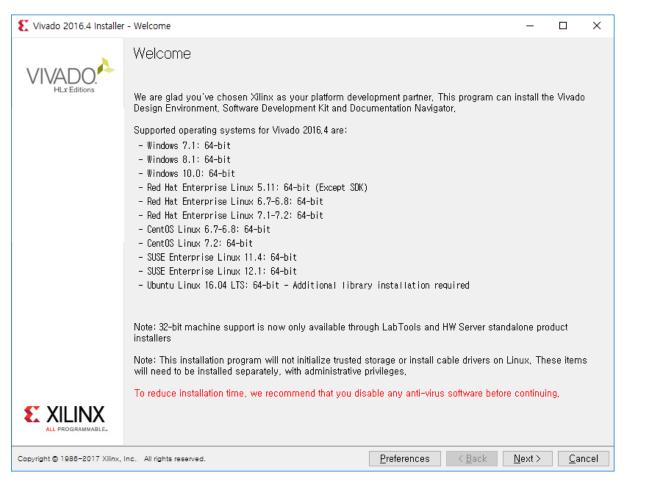


3. Execute Xilinx setup file



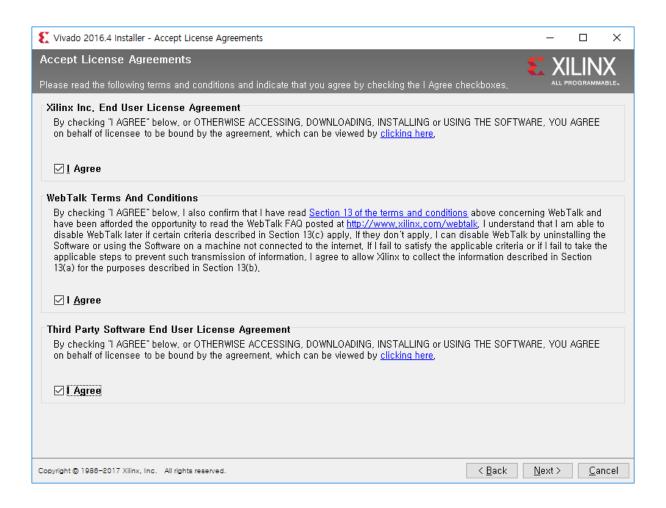


4. 5. Press Next

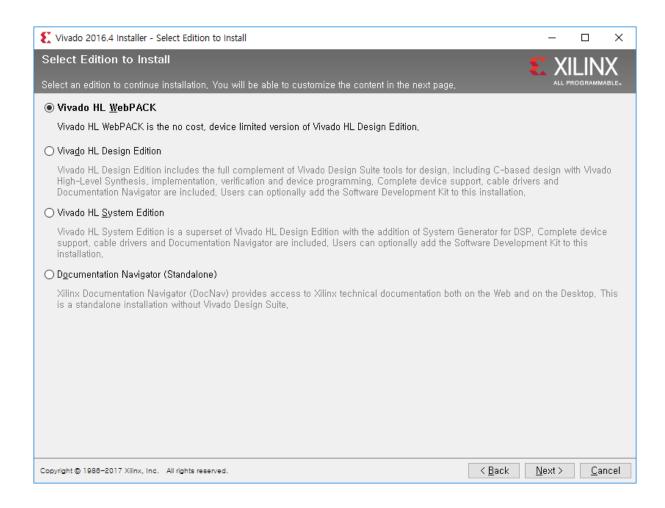


₹ Vivado 2016.4 Installer - Select Install Type	- □ ×
Select Install Type	ST XII INX
Please select install type and provide your Xilinx, com user ID and password for authentication,	ALL PROGRAMMABLE.
User Authentication	
Please provide your Xilinx user account credentials to download the required files, If you don't have an account, <u>please create one</u> , If you forgot your password, you can reset it here,	
User ID bw Password ●◀	
• Download and Install Now Select your desired device and tool installation options and the installer will download and install just what is re installation files will be saved for future use. NOTE: Future installs using these downloaded files will be restrict selected during this install. For access to all options later, choose "Download Full Image".	
O Download Full Image (Install Separately)	
The installer will download an image containing all devices and tool options for later installation. Use this optio full image on a network drive or allow different users maximum flexibility when installing,	n if you wish to install a
Copyright © 1988-2017 Xilinx, Inc. All rights reserved.	<u>N</u> ext > <u>C</u> ancel

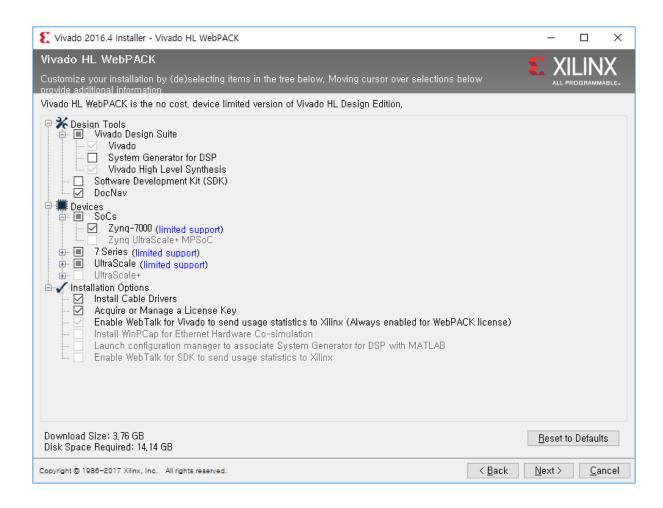
6. Check three "I Agree"s, and press next



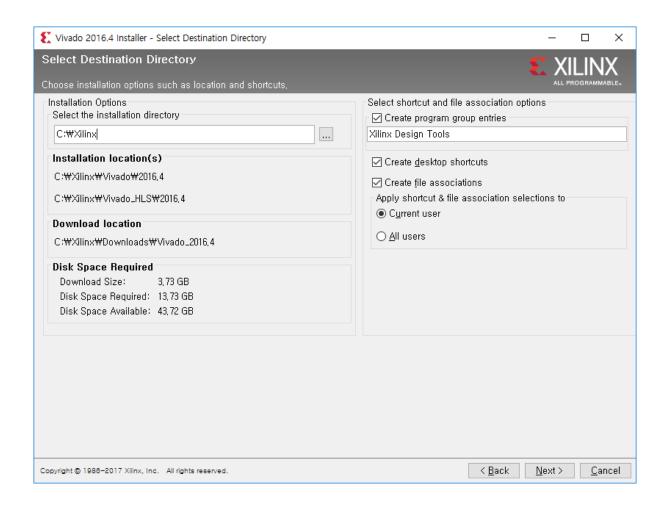
7. Choose WebPack Edition (It's free!!)



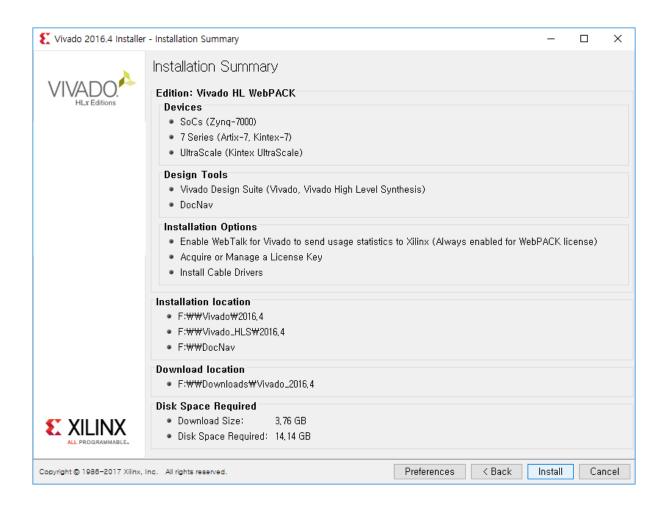
8. Press next



9. Press next



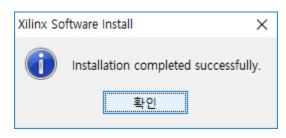
10. Press "Install"



11. Wait until installing is finished.



12. Finish!

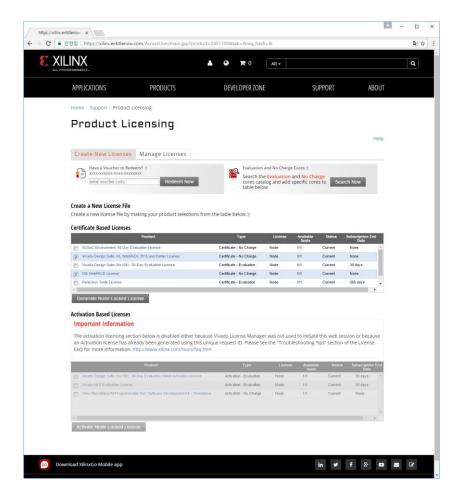


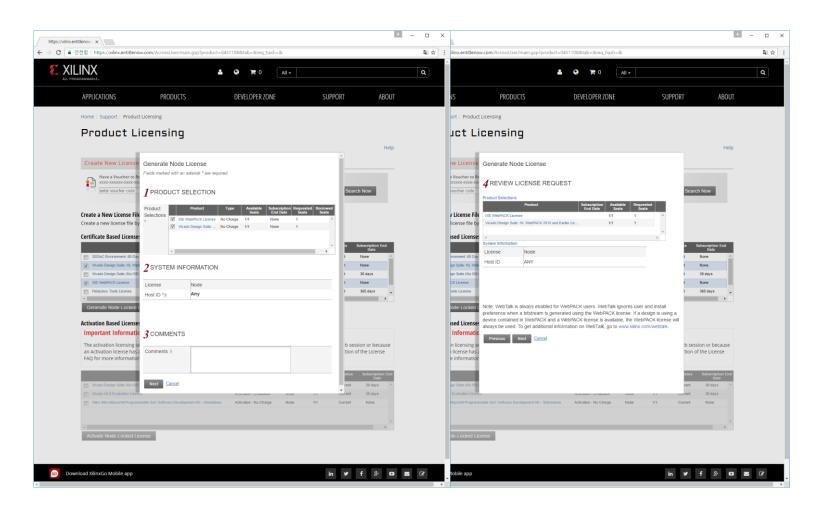
13. License Manager: Check "Get Free ISE WebPack ISE/Vivado or PetaLinux License", and click "Connect Now".



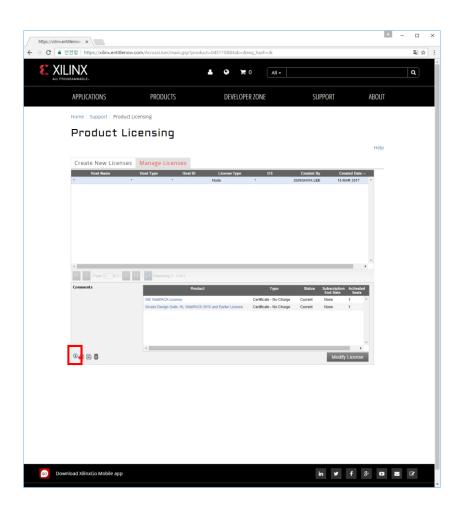
You may open License Manager manually

14. Create a Vivado WebPACK license.

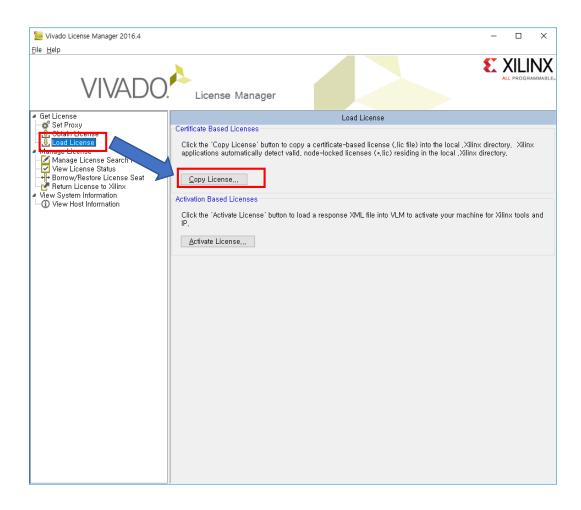




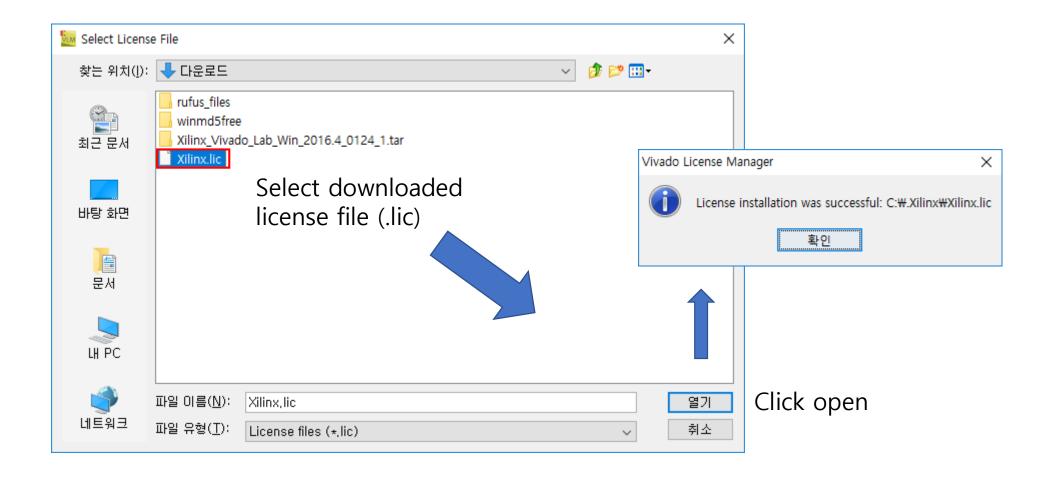
15. Select licenses and Download it



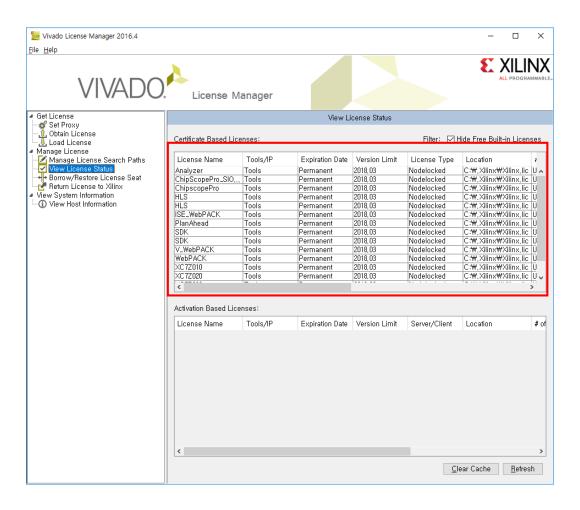
16. Load License



17. Copy License

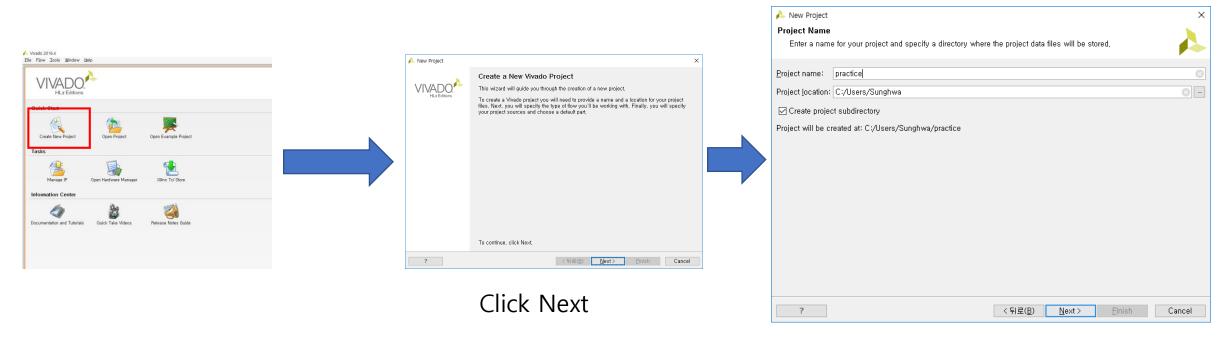


18. Check License Status (FINISH)



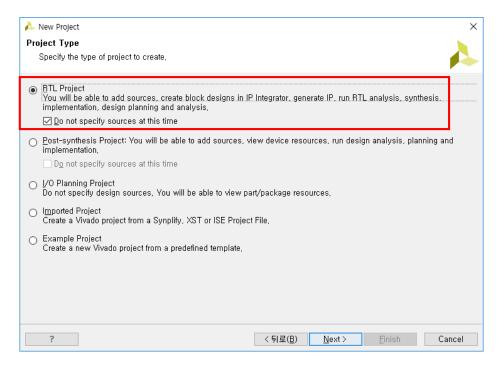
How to make a project

1. Run Vivado and create a new project

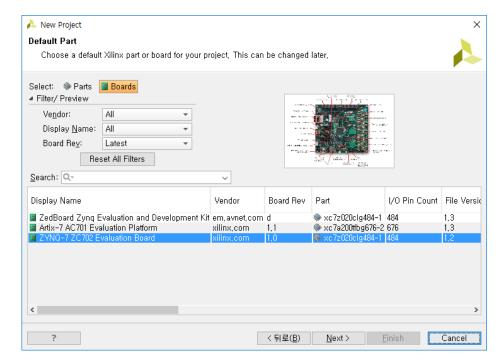


Enter a project name

2. Create a new project



Choose RTL Project



Choose Parts/Boards

 We don't use any boards in this course, so just ignore this part and press next.

3. Create a new project



Simple Verilog Tutorial using Vivado

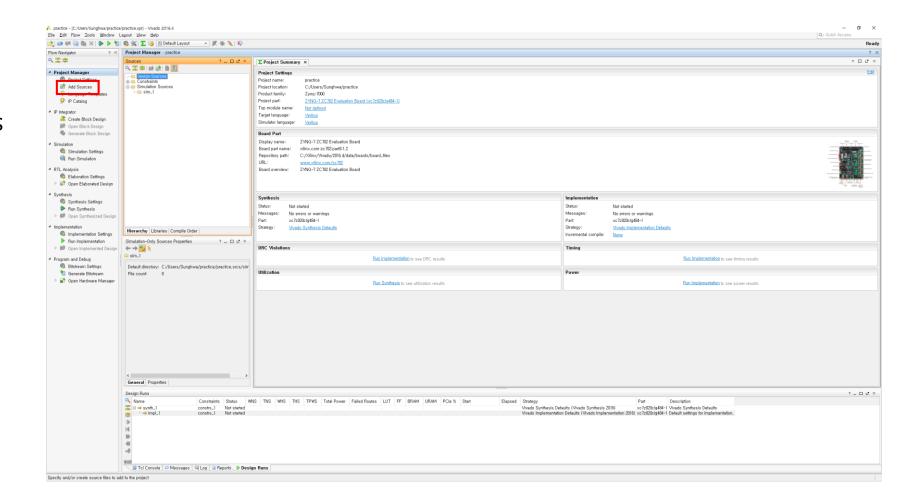
Counter

- 4-bit synchronous up-counter
- That is, the counter is incremented when the clock signal is positive edge.



1. Add Design Sources

Click Add Sources

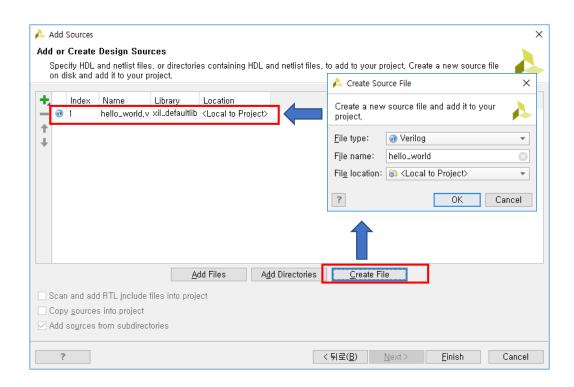


2. Add Design Sources





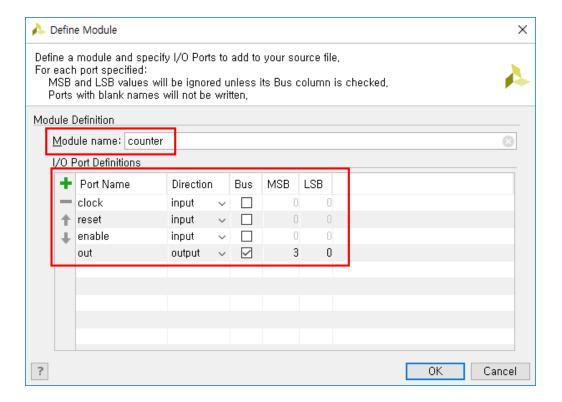
To continue, click Next



- 1. Click Create File
- 2. Enter file name ("hello_world")
- 3. Click Finish

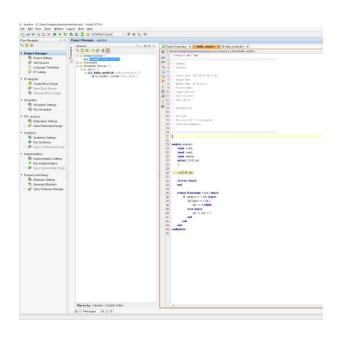
3. Add Design Sources

Change module name and enter I/O Port Deifinitions



4. Write code

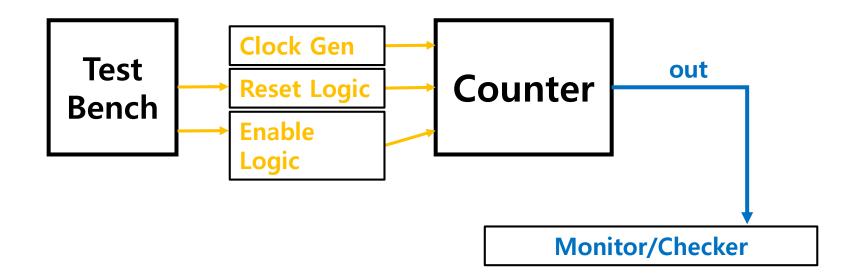
(* Copy this code and paste it *)



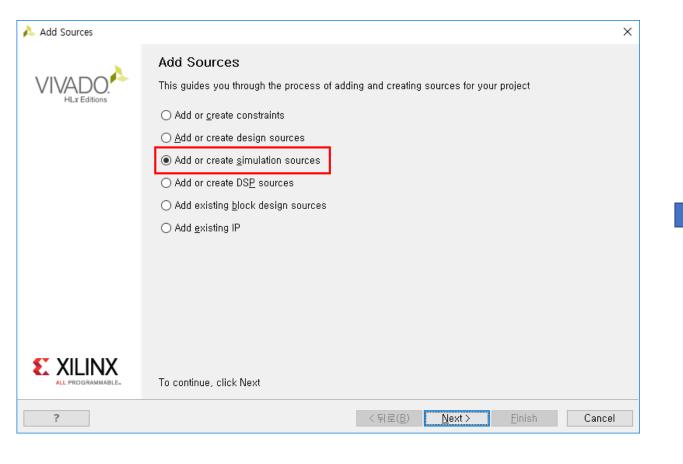
```
`timescale 1ns / 100ps
module counter (input clock, input reset, input enable, output [3:0] out);
           reg [3:0] out;
           initial begin
           end
          always @(posedge clock) begin
if (enable == 1'b1) begin
if (reset == 1'b1)
                                             out <= 4'b0000;
                                  else begin
                                             out <= out+1;
                                  end
                      end
           end
endmodule
```

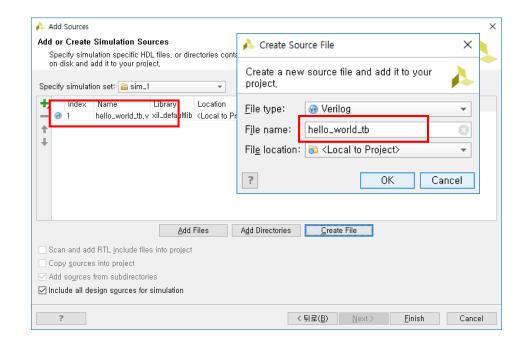
5. Write down your testbench

• To test the counter, a testbench file is needed.

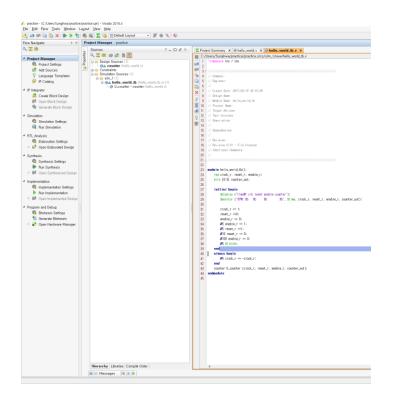


6. Add a testbench sources Clock "Add Sources"





7. Write code

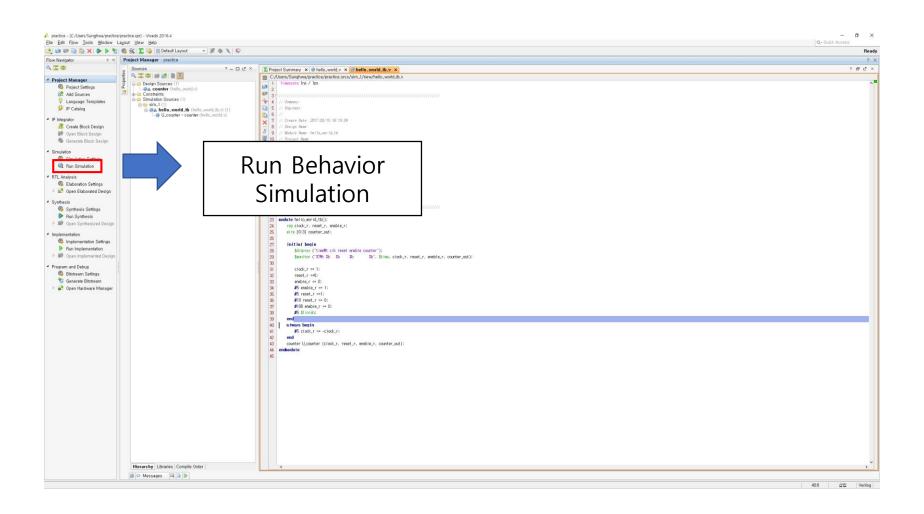


(* Copy this code and paste it *)

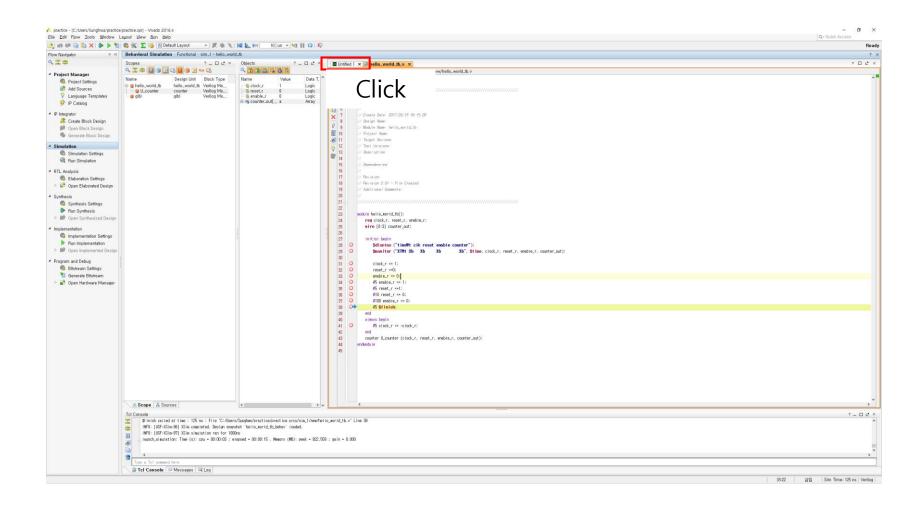
```
module hello_world_tb();
          reg clock_r, reset_r, enable_r;
          wire [3:0] counter out;
          initial begin
                     $display ("time\t clk reset enable counter");
smonitor ("%T₩t %b %b reset_r, enable_r, counter_out);
                                                     %b
                                                              %b", $time, clock r,
                    clock r <= 1;
                     reset r <=0;
                     enable r <= 0;
                    #5 enable r <= 1;
                    \#5 reset r <=1;
                     #10 \text{ reset } r <= 0;
                     #100 enable r <= 0;
                     #5 $finish;
          end
          always begin
                    #5 clock r <= \sim clock r;
          end
          counter U_counter (clock_r, reset_r, enable_r, counter_out);
```

endmodule

8. Run Simulation!



9. Run simulation



10. Check the result

