Coral Dev Board Micro: PoE Add-on Cover Page
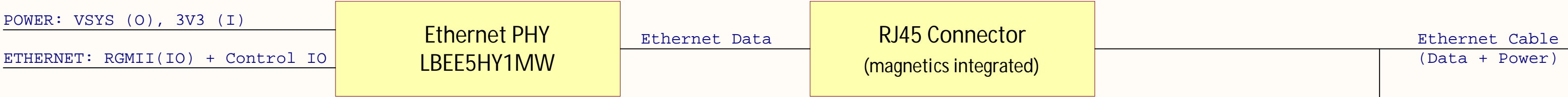
Table of Contents

Revision History

Rev. Code	Date	By	Description
1.0	2022-08-12	Stefan	Schematics prepared for release

Ethernet Overview

POWER: VSYS (O), 3V3 (I)

ETHERNET: RGMII(IO) + Control IO

Ethernet PHY
LBEE5HY1MW

Ethernet Data

RJ45 Connector
(magnetics integrated)

Ethernet Cable
(Data + Power)

Low Voltage Power

WiFI_POWER_EN

POWER: 3V3

Load Switch

3V3
for PHY

PHY Internal LDO

1.8V
for PHY (DVDD_RG)

PoE

PoE Power

POWER: VSYS (O) to Mainboard

Rectification & Regulation
Circuitry

3V3
for PHY

RJ45 Connector

PoE 7W Max
(44V-57V 48V Nominal)
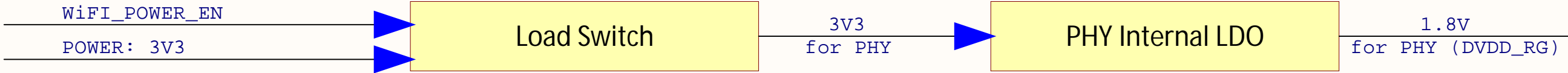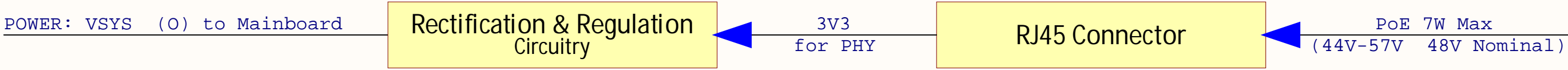
Project:	Coral Dev Board Micro: PoE Add-on		
Engineer:	Stefan	Revision:	PVT
Date:	8/12/2022	Sheet	1 of 3
File:	01 COVER.SchDoc		

Google LLC
1600 Amphitheatre Parkway
Mountain View, CA 94043
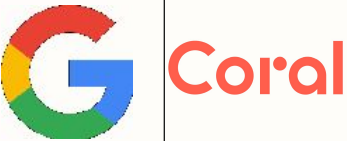
Coral

Coral Dev Board Micro: PoE Add-on RJ45 and PoE

Letters and colored background are placement and routing regions used during design process
eg. [D] is output 5V region, while [C] is a high noise high voltage region with careful routing
consideration required

GND Symbol Summary

GND_CHASSIS	POE_GND	GND_5V	GND
RJ45 Shield	POE Side GND (Isolated)	5V GND - Shorted to Mainboard/Phy GND	Mainboard/Phy

Inside RJ45 Jack — J1

ETH_TRX0_P
ETH_TRX0_N
ETH_TRX1_P
ETH_TRX1_N
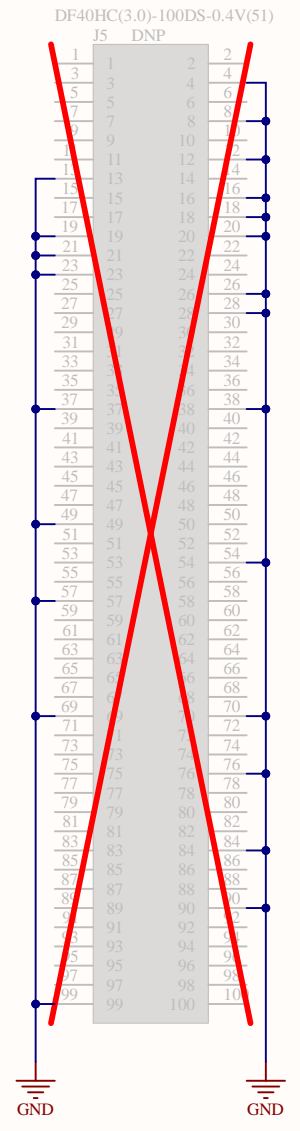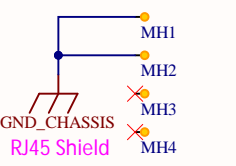ETH_TRX2_P
ETH_TRX2_N
ETH_TRX3_P
ETH_TRX3_N

5V_OUT-VSYS_MAINBOARD
GND_MAINBOARD
GND

[F]
[H]
[B]
[G]
[A]
[C]
[D]
[E]

HV HV
LV LV

L1 SRN3015TA-6R8M 6.8µH
R2 6.49K 2010
C28 2.2UF 100V 1206
C7 2.2UF 100V 1206
C13 0.1UF 100V 0603
C8 2.2UF 100V 1206
R1 24.9K 1206
C9 0.047µF 100V
D15 B1100-13-F
POE_GND

R25 1206 10
C31 0603 1nF 100V
D12 DB2440400L
C10 47UF 10V 0805
C11 47UF 10V 0805
C12 47UF 10V 0805
C39 100UF 10V 1210
C43 100UF 10V 1210
C44 47UF 10V 0805
Expensive caps. Hard to find
Consider sizing up
5V_OUT-VSYS_MAINBOARD
GND

T1 PA1283NL
TRANS_P1_1
TRANS_P1_2
TRANS_P2_1
TRANS_S1_1
Q1 FDMS86252L
R5 FET_G 24.9
R26 16K 0603
R7 FET_SRC 0603 1K
R9 1210 270m
R9 can be 5%
C18 100PF 16V 0201
R10 0603 1K
C27 1210 1nF 2000V (2kV)
GND_5V

U1 KTA1137A
VDD48I VDD48O VDD48O
RCURR ATDET
RCLASS FSEL
LVMODE NDRV
        CS
NC   FB
NC   CSS
NC   COMP
GND   VBN
GND   VDD5
VDD5

R27 100K RCLASS 0603
R4 71.5K 0603 POE_GND
FSEL
NDRV
CS
FB
CSS
COMP
VBN
VDD5
POE_GND

D7 BAS19-7-F
D8 BZT52C5V6
VBN
C20 1UF 16V 0402
POE_GND

R11 can be 5%
R11 0603 4.02K
VDD5 CSS COMP
C25 0.1UF 16V 0201
C21 0603 220nF 25V
C22 2.2UF 16V 0402
C26 0603 0.22uF 16V DNP
R18 2K 0603
COMP_C
POE_GND

U2 OPTO_TLP183 TLP183(GB-TPL_E)
OPTO_LEDP
OPTO_DRN_R
R24 820 0603
R22 3.3K 0603
C36 100nF 10V 0402
OPTO_LEDN
R17 6.2K 0603
OPTO_LEDN_R
C24 0.15uF 16V 0603
REFERENCE
C35 470pF 50V 0402 DNP
R20 9.1K 0603
R50 0 0603
R21 3K 0603
D3 TS432ILT
Sensing: Route as diff pair
This circuit [E] is isolated from everything else
Do not connect to ground plane. Use only sensing diff pair

[G]:
220R @100M 2.2A
FB2 2.2A 0603
VDD48I
R13 25.5K 0603
C23 0603 0.068uF 100V
D11 SMBG6SKA-E3-52
POE_GND
D1 ABS10-HF
D2 ABS10-HF
TAP1 TAP_P
TAP2 TAP_N TAP4
              TAP3
FB1 0603
POE_GND

R40 10 1206 DNP
C32 1000PF 0603 2kV DNP
GND GND_CHASSIS

P1 P2 P3 P6 P7 P8 P9 P10
P4 P5 P11 P12 P13 P14 P15 P16 P17 P18
TAP1 TAP2 TAP3 TAP4
C1 10nF 100V GND
VDD_3V3
R3 DNP 1201 10K
R6 DNP 201
R8 DNP 1201 10K
GND

LINK_3V3 R51 0 0201 VDD_3V3
LINK_1G   R12 470 0201 LED2_CFG_LDO1
LINK_10M R14 470 0201 LED0_CFG_EXT / LED1_CFG_LDO0
C2 680PF 25V 0201
C3 680PF 25V 0201
C4 680PF 25V 0201
GreenLED YellowLED
Shield
GND_CHASSIS
A70-112A331L126

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Coral Dev Board Micro: B2B and Ethernet PHY

NOTE:
2x MH near RJ45 are chassis GND
All other Valiant MH are floating

MH1
MH2
MH3
MH4
GND_CHASSIS
RJ45 Shield

DF40HC(3.0)-100DS-0.4V(51)
J5 DNP

DF40HC(3.0)-100DS-0.4V(51)
J6

5V_OUT-VSYS_MAINBOARD
GND_MAINBOARD
5V_OUT-VSYS_MAINBOARD
GND

5V_OUT-VSYS_MAINBOARD
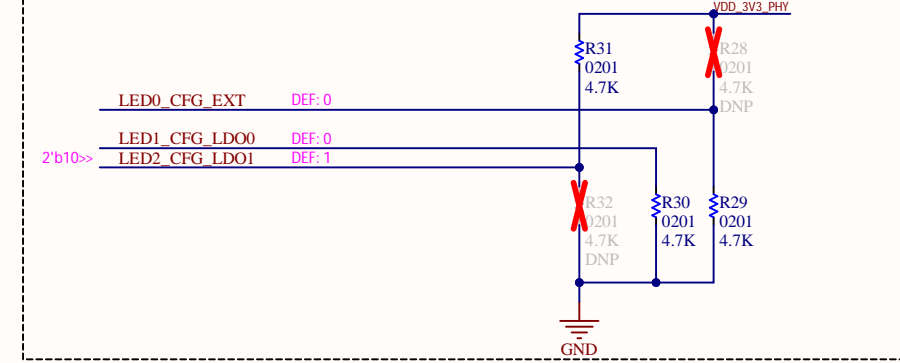VDD_1V8
TP4

VDD_3V3   No driving source suppression

GPIO_DISP_B1_04   ENET_RGMII_RXD2
GPIO_DISP_B1_03   ENET_RGMII_RXD1
GPIO_DISP_B1_02   ENET_RGMII_RXD0
GPIO_DISP_B1_05   ENET_RGMII_RXD3
GPIO_DISP_B1_00   ENET_RGMII_RX_EN
GPIO_DISP_B1_01   ENET_RGMII_RXC

ENET_RGMII_TXD3
ENET_RGMII_TXD2
ENET_RGMII_TXD1
ENET_RGMII_TXD0
ENET_RGMII_TX_EN
ENET_RGMII_TXC

GPIO_EMC_B2_02   RGMII1_PHY_INTB
GPIO_EMC_B2_03   ETHPHY_RST_B
GPIO_EMC_B2_19   ENET_RGMII_MDC
GPIO_EMC_B2_20   ENET_RGMII_MDIO
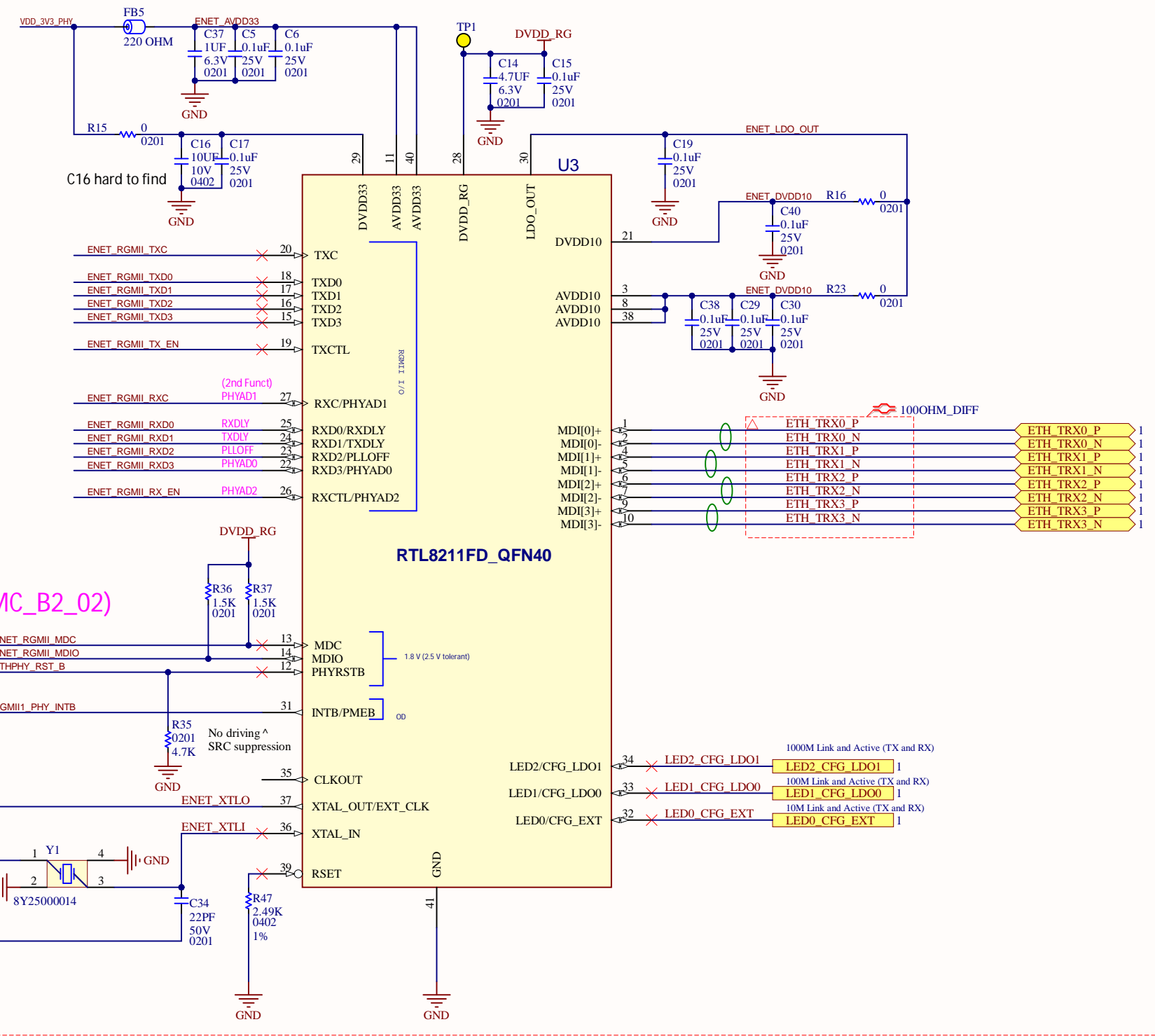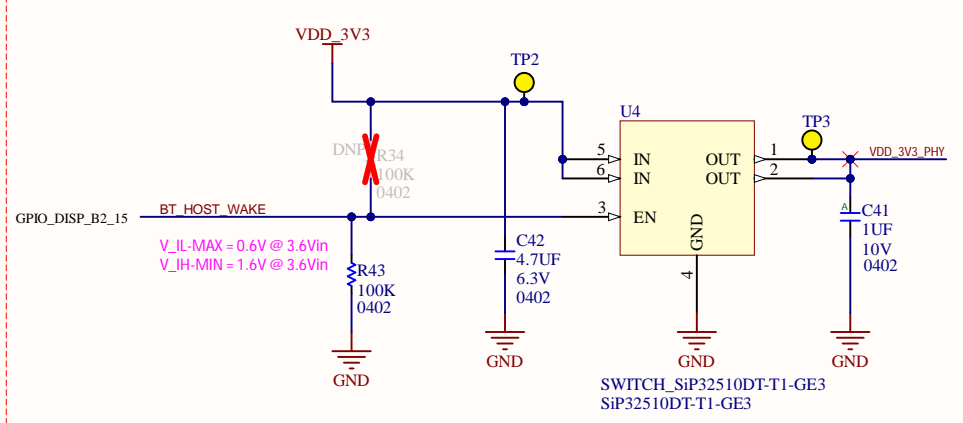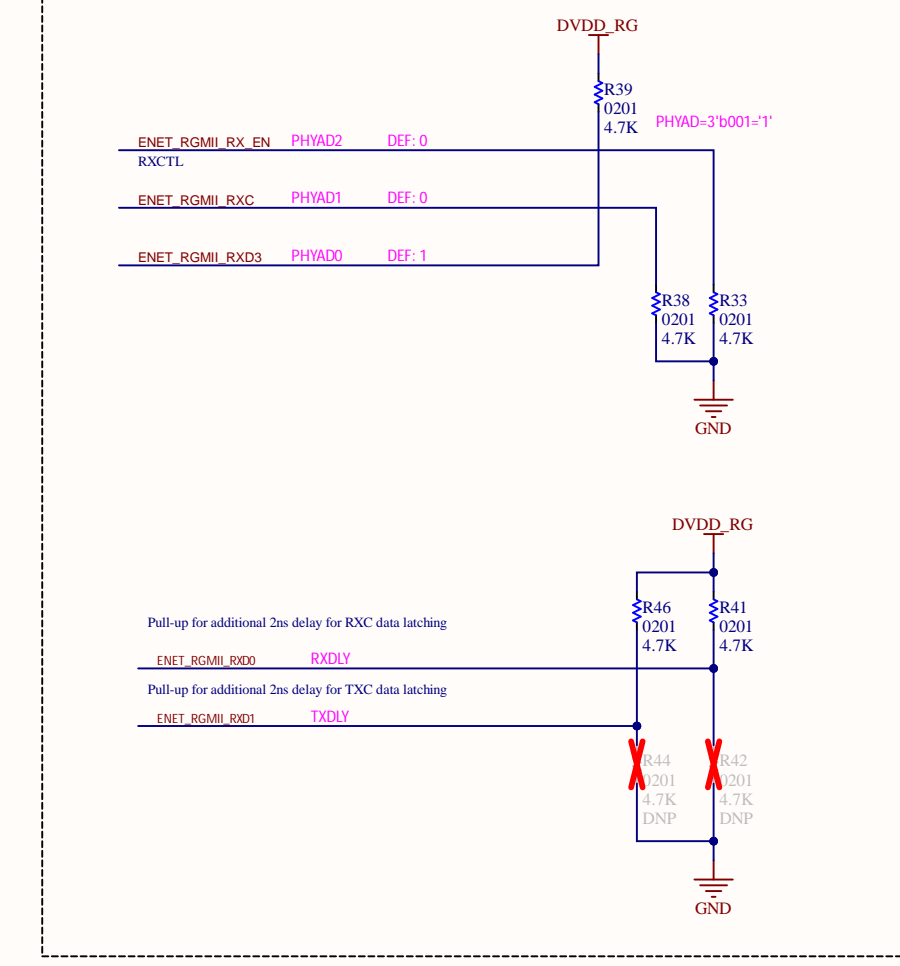
RGMII1_PHY_INTB
ETHPHY_RST_B
ENET_RGMII_MDC
ENET_RGMII_MDIO
BT_HOST_WAKE   GPIO_DISP_B2_15

ENET_RGMII_TXD3
ENET_RGMII_TXD2
ENET_RGMII_TXD1
ENET_RGMII_TXD0
ENET_RGMII_TX_EN
ENET_RGMII_TXC

ENET_RGMII_RXD2
ENET_RGMII_RXD1
ENET_RGMII_RXD0
ENET_RGMII_RXD3
ENET_RGMII_RX_EN
ENET_RGMII_RXC
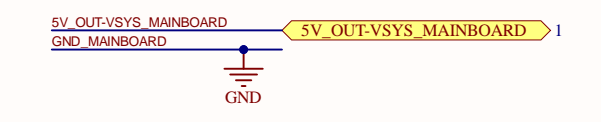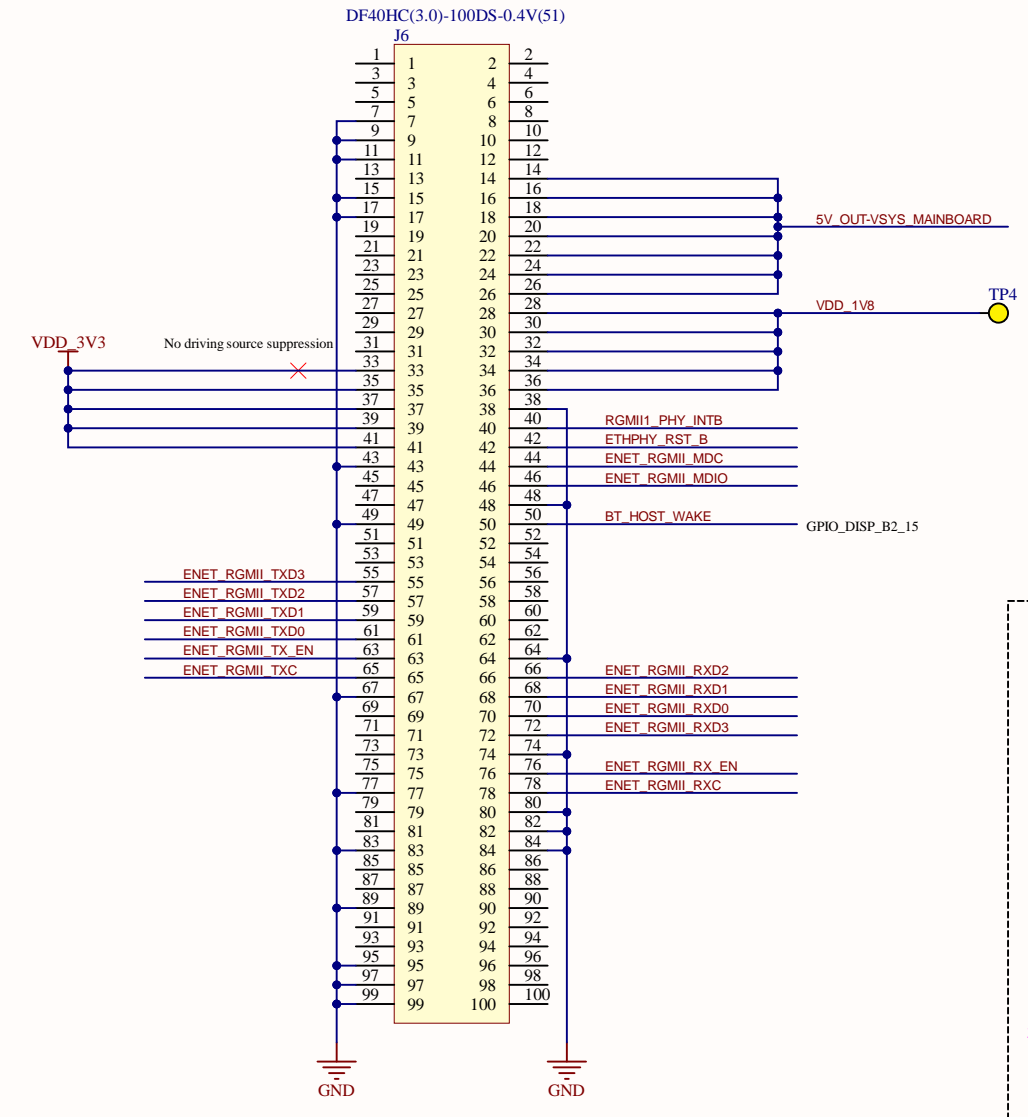
Power-on Strapping Pins

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'B1	2'B00
External 1.8	1'B1	2'B10
Internal 1.8V (Default)	1'B0	2'B10

R31 0201 4.7K
R28 0201 4.7K DNP
LED0_CFG_EXT   DEF: 0
LED1_CFG_LDO0   DEF: 0
2'b10>> LED2_CFG_LDO1   DEF: 1
R32 0201 4.7K
R30 0201 4.7K
R29 0201 4.7K DNP
VDD_3V3_PHY
GND

PHY Address Config

PHYAD3=3'b001='1'
ENET_RGMII_RX_EN   PHYAD2   DEF: 0   RXCTL
ENET_RGMII_RXC   PHYAD1   DEF: 0
ENET_RGMII_RXD3   PHYAD0   DEF: 1
R39 0201 4.7K
R38 0201 4.7K
R33 0201 4.7K
DVDD_RG
GND

R46 0201 4.7K
R41 0201 4.7K
Pull-up for additional 2ns delay for RXC data latching
ENET_RGMII_RXD0   RXDLY
Pull-up for additional 2ns delay for TXC data latching
ENET_RGMII_RXD1   TXDLY
R44 0201 4.7K DNP
R42 0201 4.7K DNP
DVDD_RG
GND

VDD_3V3_PHY
FB5 220 OHM
ENET_AVDD33
C37 1UF 6.3V 0201
C5 0.1uF 25V 0201
C6 0.1uF 25V 0201
GND

TP1
DVDD_RG
C14 4.7UF 6.3V 0201
C15 0.1uF 25V 0201

ENET_LDO_OUT
C19 0.1uF 25V 0201
ENET_DVDD10
R16 0 0201
C40 0.1uF 25V 0201
ENET_DVDD10
R23 0 0201

R15 0 0201
C16 10UF 10V 0402
C17 0.1uF 25V 0201
C16 hard to find
GND

VDD_3V3
TP2
U4
IN 5
IN 6
EN 3
OUT 1
OUT 2
TP3   VDD_3V3_PHY
C41 1UF 10V 0402
DNP R34 100K 0402
GND
BT_HOST_WAKE
GPIO_DISP_B2_15
C42 4.7UF 6.3V 0402
R43 100K 0402
V_IL-MAX = 0.6V @ 3.6Vin
V_IH-MIN = 1.6V @ 3.6Vin
SWITCH_SiP32510DT-T1-GE3
SiP32510DT-T1-GE3
GND

U3 RTL8211FD_QFN40

ENET_RGMII_TXC   TXC 20
ENET_RGMII_TXD0   TXD0 18
ENET_RGMII_TXD1   TXD1 17
ENET_RGMII_TXD2   TXD2 16
ENET_RGMII_TXD3   TXD3 15
ENET_RGMII_TX_EN   TXCTL 19

ENET_RGMII_RXC   RXC/PHYAD1 27   (2nd Funct) PHYAD1
ENET_RGMII_RXD0   RXD0/RXDLY 25   RXDLY
ENET_RGMII_RXD1   RXD1/TXDLY 24   TXDLY
ENET_RGMII_RXD2   RXD2/PLLOFF 23   PLLOFF
ENET_RGMII_RXD3   RXD3/PHYAD0 22   PHYAD0
ENET_RGMII_RX_EN   RXCTL/PHYAD2 26   PHYAD2

DVDD33
AVDD33
AVDD33
DVDD_RG
LDO_OUT
DVDD10 21
AVDD10 3
AVDD10 38

C38 0.1uF 25V 0201
C29 0.1uF 25V 0201
C30 0.1uF 25V 0201
GND

MDI[0]+   ETH_TRX0_P
MDI[0]-   ETH_TRX0_N
MDI[1]+   ETH_TRX1_P
MDI[1]-   ETH_TRX1_N
MDI[2]+   ETH_TRX2_P
MDI[2]-   ETH_TRX2_N
MDI[3]+   ETH_TRX3_P
MDI[3]-   ETH_TRX3_N
100OHM_DIFF

DVDD_RG
R36 1.5K 0201
R37 1.5K 0201

Require MCU internal pullup on PHY_INTB (GPIO_EMC_B2_02)

ENET_RGMII_MDC   MDC 13
ENET_RGMII_MDIO   MDIO 14   1.8 V (2.5 V tolerant)
ETHPHY_RST_B   PHYRSTB 12
RGMII1_PHY_INTB   INTB/PMEB 31
R35 0201 4.7K
No driving ^ SRC suppression
GND

CLKOUT 35
ENET_XTLO   XTAL_OUT/EXT_CLK 37
ENET_XTLI   XTAL_IN 36
RSET 39

LED2/CFG_LDO1 34   LED2_CFG_LDO1   1000M Link and Active (TX and RX)   LED2_CFG_LDO1
LED1/CFG_LDO0 33   LED1_CFG_LDO0   100M Link and Active (TX and RX)   LED1_CFG_LDO0
LED0/CFG_EXT 32   LED0_CFG_EXT   10M Link and Active (TX and RX)   LED0_CFG_EXT

Y1 8Y25000014
GND
C33 22PF 50V 0201
C34 22PF 50V 0201
R47 2.49K 0402 1%
GND