

# Unit Project Report

## CS 425 Compiler Construction

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## 1 Chaitin-Briggs Algorithm

Chaitin-Briggs algorithm[1] is a register allocation algorithm that utilizes graph coloring on the interference graph that are derived from the live ranges of registers, to allocate physical register for each virtual register. There are 4 major steps for this algorithm: **Live Range Computation**, **Interference Graph Construction**, **Spill Cost Calculation**, **Graph Coloring**. These steps are described in detail in the following.

### 1.1 Live Range Computation

The Global Live Ranges of a virtual register *vreg* is a partition of the references (definitions or uses) of *vreg*. If one definition *def* of *vreg* is in the Live Range *lr*, then all uses reachable from *def* are also in *lr*. If one use of *vreg* is in the Live Range *lr*, then all defs that reaches the use are also in *lr*. Using the Live Variable Analysis, we can compute the def-use chain for each virtual register. And therefore we can compute the live ranges with **union-find** algorithm.

### 1.2 Interference Graph Construction

### 1.3 Spill Cost Calculation

### 1.4 Graph Coloring

## 2 Heuristic Approach for Spilling

Mass of empty crucible	7.28 g
Mass of crucible and magnesium before heating	8.59 g
Mass of crucible and magnesium oxide after heating	9.46 g
Balance used	#4
Magnesium from sample bottle	#1

### 3 Project Status

#### 3.1 What is Working?

#### 3.2 What is Not Working?

#### 3.3 Potential Improvement

Mass of magnesium metal = 8.59 g - 7.28 g  
= 1.31 g

Mass of magnesium oxide = 9.46 g - 7.28 g  
= 2.18 g

Mass of oxygen = 2.18 g - 1.31 g  
= 0.87 g

Because of this reaction, the required ratio is the atomic weight of magnesium: 16.00g of oxygen as experimental mass of Mg: experimental mass of oxygen or  $\frac{x}{1.31} = \frac{16}{0.87}$  from which, atomic weight of magnesium =  $16.00 \times \frac{1.31}{0.87} = 24.1 = 24$  g/mol (to two significant figures).

### 4 Experimentnal Results

#### 4.1 Benchmark Programs

#### 4.2 Execution Time

#### 4.3 Number of Sills

### References

- [1] G. J. Chaitin, "Register allocation & spilling via graph coloring," in *Proceedings of the 1982 SIGPLAN symposium on Compiler construction*, ser. SIGPLAN '82. New York, NY, USA: ACM, 1982, pp. 98–105. [Online]. Available: <http://doi.acm.org/10.1145/800230.806984>