

# Microcontroller-Based Peak Current Mode Control Using Digital Slope Compensation

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**Abstract**—Microcontroller-based peak current mode control of a buck converter is investigated. The new solution uses a discrete time controller with digital slope compensation. This is implemented using only a single-chip microcontroller to achieve desirable cycle-by-cycle peak current limiting. The digital controller is implemented as a two-pole, two-zero linear difference equation designed using a continuous time model of the buck converter and a discrete time transform. Subharmonic oscillations are removed with digital slope compensation using a discrete staircase ramp. A 16 W hardware implementation directly compares analog and digital control. Frequency response measurements are taken and it is shown that the crossover frequency and expected phase margin of the digital control system match that of its analog counterpart.

**Index Terms**—DC–DC switch mode power supplies (SMPS), digital peak current mode control, digital slope compensation, discrete controller.

## NOMENCLATURE

$C_O$	Output filter capacitor.
$D$	Duty ratio.
$I_O$	Output current.
$L_O$	Output filter inductor.
$Q_C$	Double pole quality factor.
Ramp	Digital ramp height.
Steps	Number of digital steps per slope compensation period.
$S_E$	External ramp slope.
$S_N$	Output inductor current slope.
$T_S$	Switching period.
$T_{\text{SLOPE}}$	Digital slope compensation period.
$T_{\text{STEP}}$	Time taken to decrement digital ramp.
$V_{\text{DAC}}$	DAC voltage range.
$V_{\text{IN}}$	Input voltage.
$V_O$	Output voltage.
$V_{PP}$	Compensation ramp height.
$m_C$	Slope compensation factor.
$n$	Turns ratio, $n = N_S/N_P$ .
$n_{\text{DAC}}$	Number of DAC bits.
$\Delta\text{Ramp}$	Change in digital ramp height per step.
$\Phi_E$	Phase erosion.

$\Phi_M$   
 $\omega_{CP0}$   
 $\omega_{CP1}$   
 $\omega_{CZ1}$   
 $\omega_N$   
 $\omega_{P1}$   
 $\omega_{P1}$   
 $\omega_X$

Required open-loop phase margin.  
 Compensator pole at origin.  
 Compensator pole.  
 Compensator zero.  
 Plant double pole.  
 Plant pole.  
 Plant zero.  
 Required open-loop crossover frequency.

## I. INTRODUCTION

**P**EAK current mode control is one of the most popular control methods for switched-mode power supplies (SMPS) due to the inherent cycle-by-cycle current limiting, feed-forward control, and improved load regulation over voltage mode control [1]. Until recently, all peak current mode implementations have been exclusively analog in nature; the compensator in the feedback loop consisted of an analog operational amplifier, operating in the continuous time domain, with a capacitor and resistor network providing compensation.

Digital control is gaining in popularity due to its flexibility, repeatability, lack of sensitivity to environmental conditions, and possibility of advanced or multiloop control [2]–[4]. With a digital controller the compensation poles and zeros can be accurately set and easily changed by updating the controller coefficients.

A worldwide forecast into digital power by the Darnell Group noted that digital control is currently experiencing a growth phase, with 50% penetration in certain technologies, and is expected to enter the maturity phase around 2014 [5]. The current digital power market stands at around 5 billion units shipped in 2009 and is expected to increase to 12.3 billion by 2014. Clearly, research into the effective implementation of digital control is essential. The study presented in this paper is particularly relevant at present as there are no examples of a digital single-chip solution including slope compensation. The research presented in this paper fulfils the demand for digital peak current mode control and addresses the issues associated with porting this control method into the digital domain.

In a like-for-like comparison of simple single rail SMPS, the analog implementation will certainly be more cost effective than the digital solution and would, therefore, be the better choice. However, in a more complex system the digital implementation would offer some advantages and would become more cost effective as it allows for additional control features to be easily implemented with a single microcontroller. These could include controllable soft start or soft stop, power-up sequencing of multiple power rails, adaptable control loops, combined power factor correction, and even motor control.

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In the scheme proposed here, only 26% of the microprocessor's bandwidth is being used for running the SMPS as shown in Section IX. This would allow one microprocessor to control the multiple power rails of a complex system. The digital solution would, therefore, be more cost effective than an analog solution that would require multiple integrated circuits and passive components. Furthermore, in many applications such as digital cameras or mobile phones, the microcontroller is already present within the system. This would result save valuable board space and reduce costs because all of the components used for analog control could be removed.

Implementations of digital controllers with current mode control fall into two categories: digital average current mode and digital peak current mode. Digital average current mode, investigated in [6] and [7], samples both the inductor current and the output voltage and implements a digital controller to compensate both loops. The sampling requirements of average current mode are less demanding than with peak current mode, especially if a prediction method is used [8], allowing a simpler transition to digital control.

With peak current mode, two rapidly changing ramps need to be compared. These are the slope compensated reference voltage and the sensed output inductor current. The peak current limit is reached when these two ramps are equal. This peak current detection is practically impossible to detect through sampling [3]. The current changes from a minimum to a maximum within one switching cycle, requiring impractically high analog-to-digital converter (ADC) bandwidth and processing requirements when operating at high switching frequencies [2].

To mitigate this problem, previous investigations focused on sampling the inductor current once per cycle and predicting the slope of the current [2], [3], [9]. This type of control, based on a prediction, is not a true example of peak current mode control. The effects of sampling the inductor current at different points during the switching cycle and using alternative edge modulation schemes have also been thoroughly investigated [10].

However, these implementations result in a variant of peak current mode control that updates the duty such that the inductor current aims to follow a reference value. Unlike the scheme proposed here, these types of implementations predict the future value of duty based on a mathematical model of the converter and, therefore, lose the desirable real-time cycle-by-cycle current limiting ability [11] and are prone to errors due to variations from the mathematical model. Furthermore, many of these schemes seldom address the slope compensation issue needed for stable peak current mode control and instead opt for alternative modulation schemes [10] or use predictive slopes to avoid this issue [9].

The solution presented in this paper uses a continuous time comparator built into the microcontroller to achieve the real-time cycle-by-cycle current limiting. This is similar to the mixed-signal implementation given in [12]. However, in [12] the controller is implemented through lookup tables and the duty cycle is limited to 50% as slope compensation is not used. Therefore, the solution presented in this paper allows for greater design flexibility and a more realistic implementation than [12].

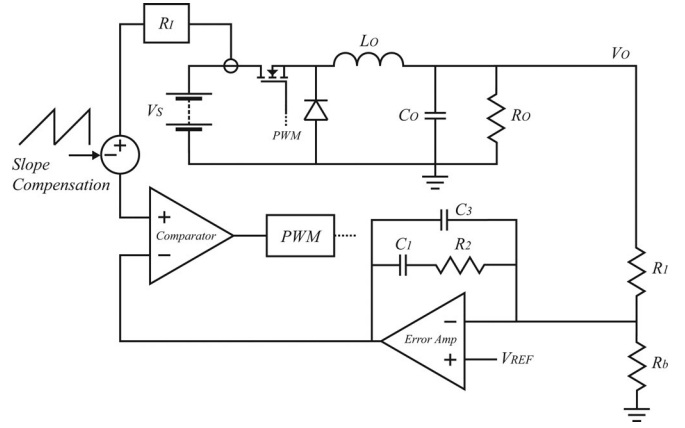


Fig. 1. Analog peak current mode control of a buck converter.

This paper presents a new digital single-chip solution combining the benefits of using a digital controller with the advantage of continuous time cycle-by-cycle peak current limiting. The implementation is achieved using a single microcontroller with no external analog ICs, replacing all of the analog control and inductor slope compensation components normally used for peak current mode control. Digital slope compensation is implemented within the microcontroller as a digital staircase using the on-board modules. The results are verified through hardware experimentation and it is shown that this implementation of digital peak current mode control is as effective as an analog control implementation in continuous time.

A review of peak current mode control is given in Section II. Section III summarizes the calculation of slope compensation given in [13]. Section IV describes how the poles and zeros of the compensation network can be calculated in order to achieve the desired phase margin and crossover frequency with a design example given in Section V. Section VI transforms the continuous time-domain compensator into a discrete time controller. Section VII describes how the digital staircase compensation ramp, which removes the subharmonic oscillations, can be implemented with a microcontroller. The effects of phase erosion are discussed in Section VIII. Finally, experimental results are presented in Section IX.

## II. REVIEW OF PEAK CURRENT MODE CONTROL

Fig. 1 depicts the typical setup for analog peak current mode control of a buck converter. The output voltage along with a reference voltage is used as inputs to an error amplifier. The capacitors and resistors in the feedback path of the error amplifier form the poles and zeros of the compensation network. The output of the error amplifier forms the current reference voltage before slope compensation.

The peak of the output inductor current is sensed by measuring the current through the switch using either a small current sense resistor or a current transformer, both of which have an equivalent current-to-voltage gain of  $R_I$ . The sensed current is effectively a ramp, as the switch is turned ON at the beginning of the pulse width modulation (PWM) period the current through



#### IV. COMPENSATOR DESIGN

Using the simplified model of a PWM switch [16], an accurate model for the small-signal characteristics of peak current mode control is presented in [13] with further information in [15]. Other models are available [17] and could be investigated; however, the model in [13] is used because it performs well when compared to the hardware measurements. The subharmonic oscillations observed with peak current mode control due to small perturbations in the inductor current are predicted by this model. The compensation ramp discussed in the previous section is added to the sensed switch current to damp these oscillations.

Many implementations take an intuitive approach to compensator design. However, this paper uses an exact method to calculate the compensator poles and zeros such that the specified open-loop crossover and phase margin are achieved. Using the accurate control-to-output model proposed by Ridley in [13] a Type II compensator can be analytically designed.

With peak current mode control the compensator is placed within the outer voltage loop. The inner current loop has a bandwidth of between 1/6 and 2/3 of the switching frequency [18], [19]. Therefore, the crossover frequency of the outer voltage loop should be less than this, between 1/20 and 1/10 of the switching frequency. The transfer function of the Type II compensator, given in 7, has one pole, one zero and a pole at the origin

$$H_C(s) = \frac{\omega_{CP0}}{s} \times \frac{(1 + (s/\omega_{CZ1}))}{(1 + (s/\omega_{CP1}))}. \quad (7)$$

The compensator pole  $\omega_{CP1}$  is placed at the frequency of the plant's zero formed by the capacitor and its parasitic equivalent series resistance (ESR)

$$\omega_{CP1} = \omega_{ESR} = \frac{1}{R_{ESR}C_O}. \quad (8)$$

Intuitive placement of the compensator zero is normally used to add phase into the open-loop system around the crossover frequency. However, in this paper, an exact equation is derived that analytically places the compensator zero so as to achieve the phase margin specification precisely.

At the crossover frequency, the combined control-to-output and compensator transfer functions must satisfy (9). Where  $\phi_M$  is the required phase margin in radians and  $\omega_X$  is the required crossover frequency.  $H_P(j\omega)$  and  $H_C(j\omega)$  are the control-to-output and controller transfer functions, respectively

$$\angle(H_P(j\omega_X) \times H_C(j\omega_X)) = -\pi + \phi_M. \quad (9)$$

Through knowledge of the control-to-output transfer function as given in [13] and [15] and (7), an equation for calculating the compensator zero is derived in this paper and given in (10) to precisely achieve a specified phase margin and crossover frequency concurrently

$$\omega_{CZ1} = \frac{\omega_X}{\tan[\phi_V]} \quad (10)$$

where

$$\phi_V = -\frac{\pi}{2} + \phi_M + \tan^{-1}\left(\frac{\omega_X}{\omega_{P1}}\right) + \tan^{-1}\left(\frac{\omega_X}{\omega_{N1}}\right) + \tan^{-1}\left(\frac{\omega_X}{\omega_{N2}}\right) \quad (11)$$

$$\omega_{P1} = \frac{1}{R_O.C_O} + \frac{T_S}{L_O.C_O} \cdot (m_C \cdot (1-D) - 0.5) \quad (12)$$

$$\omega_{N1} = \frac{-\omega_N}{2.Q_C} + \sqrt{\frac{1}{Q_C^2 \cdot \omega_N^2} - 2} \quad (13)$$

$$\omega_{N2} = \frac{-\omega_N}{2.Q_C} - \sqrt{\frac{1}{Q_C^2 \cdot \omega_N^2} - 2}. \quad (14)$$

In (11), the  $\omega_{N1}$  and  $\omega_{N2}$  terms are the complex conjugate poles of the high-frequency double-pole  $\omega_N$ . The inverse tangent of these pairs must be calculated accordingly. The phase contribution from  $\omega_{CP1}$  negates that of  $\omega_{ESR}$  and as such these terms have been omitted from (11).

Finally, the gain of the compensator can be analytically calculated to achieve the specified crossover frequency of the open-loop system. This is the pole at the origin of the compensator and is the frequency at which this pole has unity gain. However, the complete open-loop system should have unity gain at the specified crossover frequency. This is described as follows:

$$20 \log_{10}[H_P(j\omega_X)] + 20 \log_{10}[H_C(j\omega_X)] = 0. \quad (15)$$

Using the control-to-output transfer function and (7), an equation for calculating the compensator pole at the origin is given in (16) to achieve a specific crossover frequency

$$\omega_{CP0} = \frac{\omega_X}{K_{DC} \times K_1 \times K_2} \quad (16)$$

where

$$K_{DC} = \frac{R_O}{n.R_I} \times \frac{1}{\left[1 + \frac{R_O.T_S}{L_O} \cdot (m_C \cdot (1-D) - 0.5)\right]} \quad (17)$$

$$K_1 = \frac{\sqrt{1 + \left(\frac{\omega}{\omega_{CZ1}}\right)^2}}{\sqrt{1 + \frac{\omega_X^2}{\omega_{P1}^2}}} \quad (18)$$

$$K_2 = \frac{1}{\sqrt{\left(1 + \frac{\omega_X^2}{\omega_N^2}\right)^2 + \left(\frac{\omega_X}{\omega_N \cdot Q_C}\right)^2}} \quad (19)$$

#### V. DESIGN EXAMPLE

A 16 W buck converter is designed and constructed. An input voltage of 16 V and output of 8 V at 2 A is used. The full converter specification is given in Table I(a).

First, the slope compensation requirements are calculated given that the quality factor of the double pole at half the switching frequency is set to 1. The remaining operational parameters are calculated using the converter specification and equations presented in the previous sections. Table I(b) lists the parameters calculated for this design example.



TABLE I  
PEAK CURRENT MODE DESIGN EXAMPLE

Parameter	Value	Parameter	Value
$V_{IN}$	16Vdc	$R_I$	0.48
$V_O$	8Vdc	$R_{ESR}$	31mΩ
$I_O$	2A	$V_{DIODE}$	0.6V
$C_O$	440μF	$F_S$	200kHz
$L_O$	22μH	$F_X$	15kHz
$n$	1	$\phi_M$	75°

(a) Specification

Parameter	Value	Parameter	Value
$Q_C$	1	$\omega_{P1}$	732.6rad.s <sup>-1</sup>
$D$	0.5375	$\omega_{Z1}$	7.331 × 10 <sup>4</sup> rad.s <sup>-1</sup>
$m_C$	1.7693	$\omega_N$	6.283 × 10 <sup>5</sup> rad.s <sup>-1</sup>
$V_{PP}$	0.621V	$K_{DC}$	6.4631

(b) Operational parameters

Pole/Zero	Value
$\omega_{CP1}$	7.331 × 10 <sup>4</sup> rad.s <sup>-1</sup>
$\omega_{CZ1}$	1.111 × 10 <sup>4</sup> rad.s <sup>-1</sup>
$\omega_{CP0}$	2.171 × 10 <sup>5</sup> rad.s <sup>-1</sup>

(c) Compensator poles and zeros

Using the exact analytical design method presented in this paper, the compensator is designed to meet the specified phase margin and crossover frequency. For a Type II compensator, using (8), the pole is placed at the frequency of the power stage ESR zero. Equation (10) calculates the frequency of the compensator zero required to meet the phase margin specification. Finally, (16) calculates the gain of the compensator to meet the crossover specification.

The compensator poles and zeros are given in Table I(c). These exact values will be used in the next section to design the digital controller.

This design example is simulated using MATLAB. Fig. 3 depicts the theoretical frequency response of the control-to-output and controller transfer functions for the peak current mode converter design example. The controller has been designed using the exact method presented in this paper. The plot of the combined open-loop response is stable as slope compensation is used and shows that the crossover frequency and phase margin, specified in Table I(a), are achieved precisely in the open-loop system.

## VI. DIGITAL CONTROLLER DESIGN

Within one switching period the microcontroller must sample the analog output voltage, convert this to a digital value, calculate the error, execute a controller based on this error, and run the slope compensation algorithm using the controller output to calculate the reference current. This is then compared to the sensed inductor current in order to implement the peak current limit. When the sensed inductor current reaches the reference current a trip is set within the microcontroller and the PWM duty is disabled.

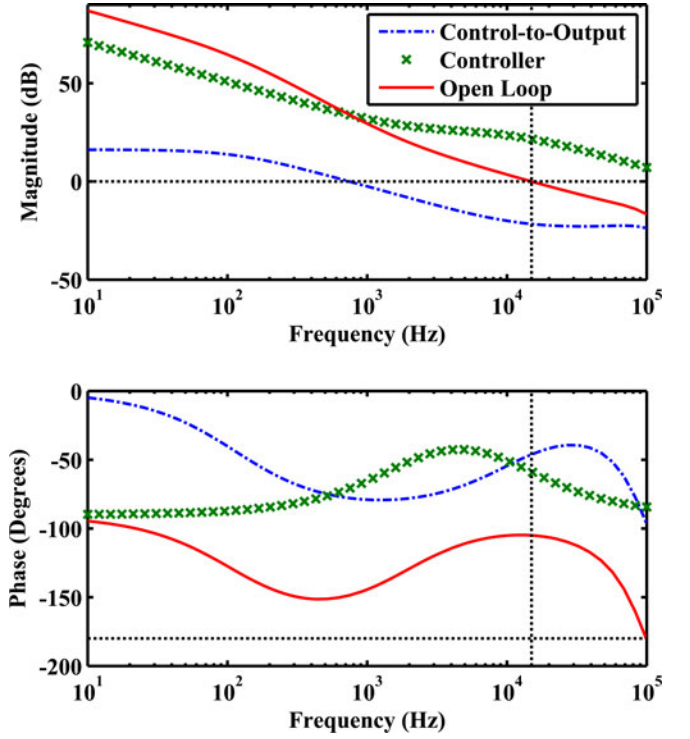


Fig. 3. Theoretical frequency response plots of the control-to-output transfer, analytically designed controller, and combined open loop. Open-loop crossover frequency: 15 kHz, phase margin: 75°.

In this digital implementation, the controller has been designed in the continuous time domain and will be converted to the discrete time domain using the bilinear transform. The bilinear transform will be used as it provides good results up to half the switching frequency and the poles and zeros are within the unit circle [20]. Using the substitution

$$s = \frac{2}{T_S} \frac{z - 1}{z + 1} \quad (20)$$

the continuous time compensator transfer function is converted into a discrete time transfer function as follows:

$$H_C[z] = \frac{\omega_{CP0}}{\left(\frac{2}{T_S} \frac{z - 1}{z + 1}\right)} \times \frac{1 + \frac{\left(\frac{2}{T_S} \frac{z - 1}{z + 1}\right)}{\omega_{CZ1}}}{1 + \frac{\omega_{CP1}}{\left(\frac{2}{T_S} \frac{z - 1}{z + 1}\right)}} \quad (21)$$

After simplification, a two-pole, two-zero digital controller is derived as follows:

$$H_C[z] = \frac{B_2 z^{-2} + B_1 z^{-1} + B_0}{-A_2 z^{-2} - A_1 z^{-1} + 1} \quad (23)$$

The coefficients of the digital two-pole, two-zero controller are calculated from the compensator poles and zeros. All of the variables in these coefficients have now been defined and, therefore, the coefficients can be calculated analytically

$$B_0 = \frac{T_S \cdot \omega_{CP0} \cdot \omega_{CP1} \times (2 + T_S \cdot \omega_{CZ1})}{2 \times (2 + T_S \cdot \omega_{CP1}) \times \omega_{CZ1}} \quad (23)$$

TABLE II  
DESIGN EXAMPLE CONTROLLER COEFFICIENTS

Coefficient	Value
$B_0$	3.112327
$B_1$	0.168173
$B_2$	-2.944154
$A_1$	1.690211
$A_2$	-0.690211

$$B_1 = \frac{T_S^2 \cdot \omega_{CP0} \cdot \omega_{CP1}}{2 + T_S \cdot \omega_{CP1}} \quad (24)$$

$$B_2 = \frac{T_S \cdot \omega_{CP0} \cdot \omega_{CP1} \times (-2 + T_S \cdot \omega_{CZ1})}{2 \times (2 + T_S \cdot \omega_{CP1}) \times \omega_{CZ1}} \quad (25)$$

$$A_1 = \frac{4}{2 + T_S \cdot \omega_{CP1}} \quad (26)$$

$$A_2 = \frac{-2 + T_S \cdot \omega_{CP1}}{2 + T_S \cdot \omega_{CP1}}. \quad (27)$$

In the microcontroller, the controller is executed as a linear difference equation (LDE). This is a digital convolution algorithm. The LDE is obtained in (30) using (22) and (28)

$$H_C[z] = \frac{y[z]}{x[z]} \quad (28)$$

$$y[n] \times (-A_2 z^{-2} - A_1 z^{-1} + 1) = x[n] \times (B_2 z^{-2} + B_1 z^{-1} + B_0) \quad (29)$$

$$x[n] = B_0 \cdot x[n] + B_1 \cdot x[n-1] + B_2 \cdot x[n-2] + A_1 \cdot y[n-1] + A_2 \cdot y[n-2] \quad (30)$$

Using the compensator poles and zeros in Table I(c), the numerical values for the controller coefficients are calculated in Table II using (23)–(27).

## VII. DIGITAL SLOPE COMPENSATION

Under analog peak current mode, the compensating ramp is a voltage that is added to the sensed inductor current. Careful consideration is required as to the component values to ensure that enough ramp is generated in order to damp the oscillations otherwise instability will be observed.

Under digital peak current mode, a discrete digital ramp can be subtracted from digital output of the controller at subintervals within the switching period. This task is particularly suited to the many microcontrollers on the market that have two or more cores. The Texas Instruments TMX320F28035 used in this example has a main core and a control law accelerator (CLA), which allows the execution of both the control and slope compensation code in parallel.

The DAC connects the output of the digital controller to the input of the continuous time comparator for peak current detection. At the beginning of the switching period in Fig. 4, the DAC module is loaded with the output of the digital controller, the peak current reference before slope compensation. The input to the DAC is then decremented at fixed subintervals throughout

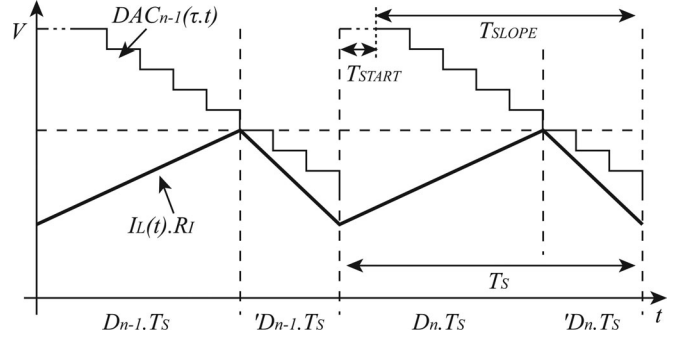


Fig. 4. Slope compensation using a digital staircase.

the switching period, simulating the compensation ramp necessary to damp any subharmonic oscillations. This digital slope compensation is in the form of a staircase with a fixed number of steps and step height over the switching period. Several parameters are defined to calculate the digital slope compensation

$$\text{Ramp} = V_{PP} \times \frac{2^{n_{DAC}} - 1}{V_{DAC}}. \quad (31)$$

The DAC has a specific number of bits  $n_{DAC}$ , which represent the output voltage range  $V_{DAC}$ . The peak-to-peak compensation ramp value,  $V_{PP}$  calculated in Section III, is converted to a discrete number using the calculation in (31). The result is the digital staircase height. The DAC resolution can be improved by setting the external DAC voltage reference pins  $V_{DDA}$  and  $V_{SSA}$ . This would be especially useful for configurations that require small values of slope compensation

$$\text{Steps} = \frac{T_{SLOPE}}{T_{STEP}}. \quad (32)$$

The individual number of steps and the change in height per step are calculated based on the microcontroller specification. Several microcontroller instruction cycles will be required to decrement the input to the DAC for each step of the staircase type compensation. The total time for each step will be specific to the microcontroller. However, it is referred to as  $T_{STEP}$  for the equations herein. Equation (32) calculates the number of discrete steps that the microcontroller can execute for one digital slope compensation period  $T_{SLOPE}$  within each switching period. Given this, (33) calculates the change in DAC value for each step

$$\Delta \text{Ramp} = -\frac{\text{Ramp}}{\text{Steps}}. \quad (33)$$

The digital slope compensation parameters required for the design example given in Section V are calculated in Table III. Ideally,  $T_{SLOPE}$  would be equal to the switching period. However, in practice it will take a number of time steps to begin the digital slope compensation function within each switching period  $T_{START}$ . This is the time taken for the PWM interrupt to trigger the flushing of the pipeline and start of the CLA code execution.  $T_{START}$  has been measured as 400 ns on the TI microcontroller used herein. This time is comparable to the reverse recovery time of the diode often used in the analog slope

TABLE III  
DIGITAL SLOPE COMPENSATION PARAMETERS

Parameter	Value	Parameter	Value
$V_{PP}$	0.621V	$T_{STEP}$	50ns
$n_{DAC}$	10bits	$T_{SLOPE}$	3950ns
$V_{DAC}$	3.3V	Steps	79
Ramp	192.53	$\Delta Ramp$	-2.437

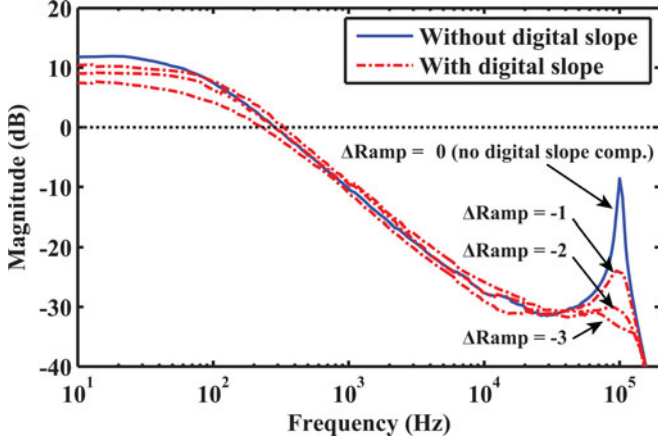


Fig. 5. Measured control-to-output frequency response using an OMICRON Lab Bode 100 network analyzer comparing with and without digital slope compensation for varying  $\Delta Ramp$  values.

compensation circuit and forms only a small fraction of the entire duty cycle. Therefore, it has no impact on the damping of subharmonic oscillations. The time step for the microcontroller used in this design example is 50 ns. The time available for slope compensation  $T_{SLOPE}$  is calculated as 4600 ns as eight time steps are required to start the slope compensation function within each switching period.

In Fig. 5, the control-to-output transfer function of the hardware experimentation has been measured using a frequency analyzer in order to illustrate the effectiveness of the digital staircase slope compensation. Detailed open-loop experimental results will be given in Section IX. The figure illustrates the damping effect for different values of  $\Delta Ramp$ .

The first measurement taken has no digital slope compensation,  $\Delta Ramp = 0$ ; the DAC value remains constant throughout the switching period. The characteristic resonant peak at half the switching frequency is visible. The proportional gain had to be reduced such that the resonant peak did not cross the unity gain axis, allowing stable operation and a frequency response measurement to be obtained. This does not change the shape of the magnitude plot.

The remaining measurements are taken with digital slope compensation applied using varying values of  $\Delta Ramp$ . As expected, damping of the resonant peak increases as the digital compensation ramp is increased. When  $\Delta Ramp$  is between -2 and -3, the resonant peak is sufficiently damped and the converter operation is stable with the proportional gain returned to the correct value. This indicates that the novel digital staircase implementation of slope compensation achieves the same damping effect as analog slope compensation.

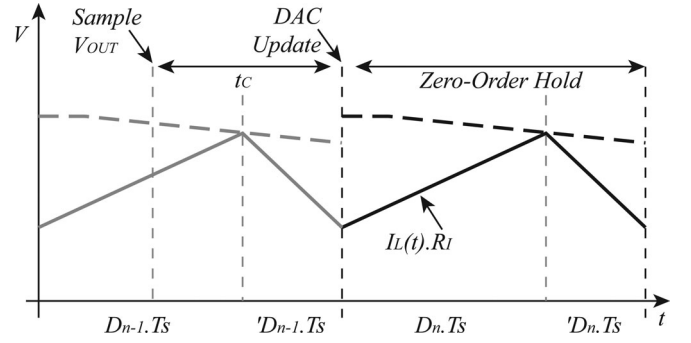


Fig. 6. Time delays introduced with a digital controller.  $t_c$  is the time spent sampling and performing calculations within the controller.

### VIII. PHASE EROSION

With digital control, care must be taken to calculate the sources of delay within the system. These delays manifest themselves as a phase margin erosion that is significant for high crossover frequencies. Therefore, with digital control it is necessary to calculate these delays and ensure that the compensator is designed to allow for this phase erosion.

Two factors contribute to phase erosion: the phase delay due to the sampling and calculation time [21]  $\phi_{CALC}$  and the phase delay due to the zero-order hold  $\phi_{ZOH}$ . The sampling and calculation time begins when the output voltage is sampled and ends when the LDE output has been calculated and is ready to be used. The output voltage is sampled and the controller value is calculated in one period and the output of this is used in the following period. Therefore, as illustrated in Fig. 6, the sampling point should be as near to the end of the switching period as possible in order to minimize this delay. Furthermore, it is up to the designer to write efficient code that minimizes the time spent performing calculations. Ideally, the output voltage is sampled in one period and the output of the controller is ready just before the beginning of the next period taking a total time  $t_c$ .

The controller output remains fixed for the duration of the following switching period. This zero-order hold introduces a time delay of half the switching period  $T_S$  [22]. The total time delay is the sum of the sampling and calculation delay and the delay introduced by the zero-order hold. However, the sampled data analysis used to derive the peak current mode model by Ridley in [13] already includes the effects of the zero-order hold. Therefore, when using this particular peak current mode model, only the sampling and calculation delay need be considered

$$\phi_E = \phi_{CALC} + \phi_{ZOH} \quad (34)$$

$$\phi_{CALC} = 360^\circ \times F_X \times t_c \quad (35)$$

$$\phi_{ZOH} = 360^\circ \times F_X \times \frac{T_S}{2}. \quad (36)$$

For digital peak current mode, using this model,  $\phi_{ZOH} = 0$ . The required phase margin has already been specified as  $\phi_M = 75^\circ$ . The stability of the digital controller must be considered after phase erosion. In this case, the phase erosion is caused by the delay between sampling and update of the DAC value



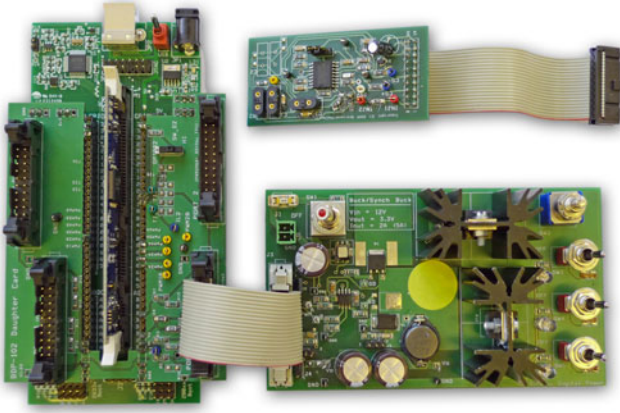


Fig. 7. Peak current mode buck converter with 16 W load (bottom right), analog control board (top right) and digital control board (left).

only. This hardware- and software-dependent time can be measured either by counting the number of instructions executed or by toggling an output pin at the appropriate intervals. For this design example, the sampling and calculation time has been measured as  $2.35 \mu\text{s}$  by toggling an output pin as sampling begins and as the controller calculation ends. The expected phase erosion is calculated as follows:

$$\begin{aligned}\phi_E &= 360^\circ \times F_X \times t_C \\ &= 360^\circ \times (15 \times 10^3) \times (2.35 \times 10^{-6}) \\ &= 12.69^\circ\end{aligned}\quad (37)$$

$\therefore$

$$\phi_D = \phi_M - \phi_E = 62.31^\circ. \quad (38)$$

The expected phase margin of the digital open-loop system after phase erosion (38) is still sufficiently large allowing stable operation as the analog converter was purposely designed with a good phase margin of  $75^\circ$ .

## IX. EXPERIMENTAL RESULTS

The hardware experimentation shown in Fig. 7 uses a common power stage with connectable analog and digital control boards to ensure an exact comparison between the two domains. The component values of the compensation network on the analog controller board are calculated from the compensator poles and zeros given in Table I(c). The analog board is populated with component values nearest to those calculated for the Type II error amplifier.

The digital system is implemented using a Texas Instruments TMX320F28035 microcontroller and the precise controller coefficients required are entered in software. This microcontroller was chosen because of its on-board comparator, DAC and CLA modules. The CLA allows the digital slope compensation code to be executed in parallel to the main controller. For the power stage, a Texas Instruments UCC27200 high side driver is used to drive an IRFR3708PBF N-channel MOSFET.

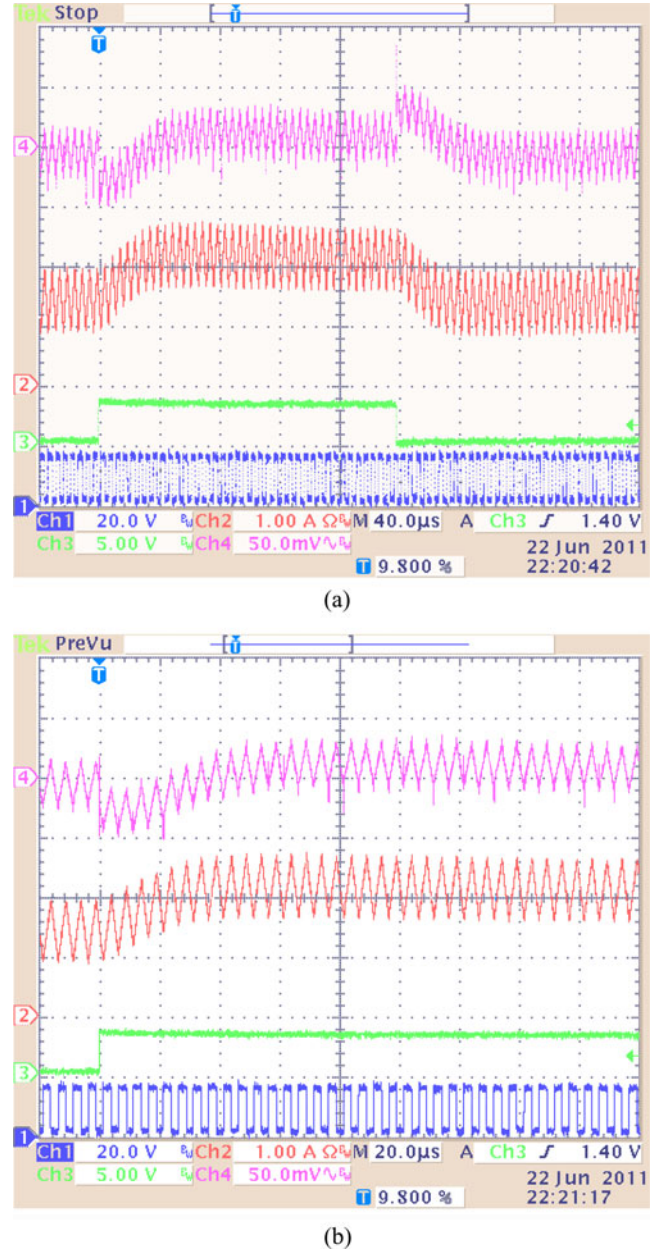
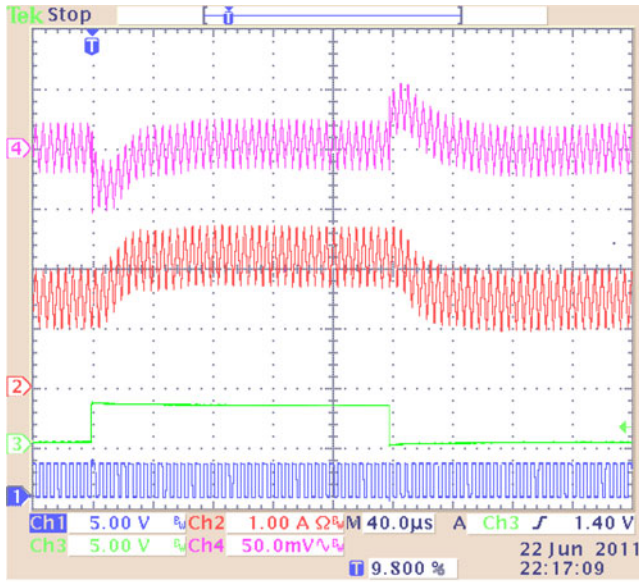


Fig. 8. Measured CCM transient response of the analog system using Tektronix TDS3014B as load is switched from 67% ( $6 \Omega$ ) to 100% ( $4 \Omega$ ) and vice versa. Ch1 denotes switch PWM. Ch2 denotes output inductor current. Ch3 denotes load switching (high: 100%, low: 67%). Ch4 denotes ac coupled output voltage. (a) Measured transient response of analog system. (b) Close up view of analog system transient response.

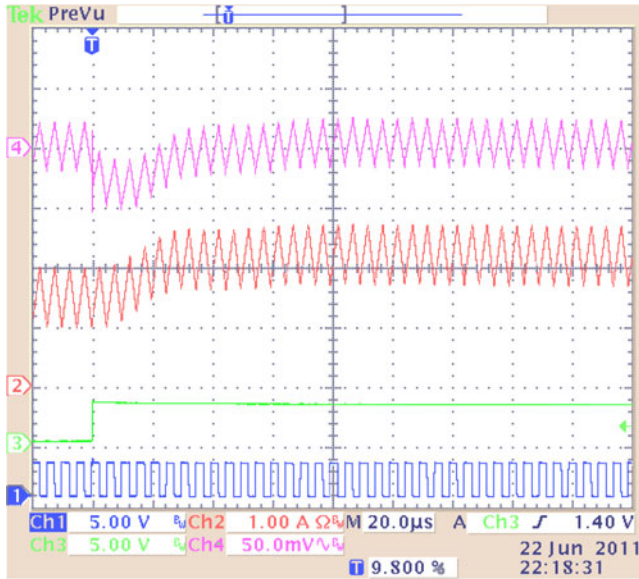
Both control schemes result in stable steady-state operation for varying loads. Oscilloscope plots of the transient response of the analog and digital control methods under continuous conduction mode (CCM) are given in Figs. 8 and 9, respectively. The tests are performed as the load is switched from 67% to 100% and vice versa. Automatic switching of the load in and out of the circuit is performed by a low side MOSFET.

The output voltage (Ch4) is ac coupled and shows the controller's response to a step change in load (Ch3). The repetitive sawtooth shape of the output voltage is due to the product of the ac component of the output current and the capacitor's parasitic





(a)

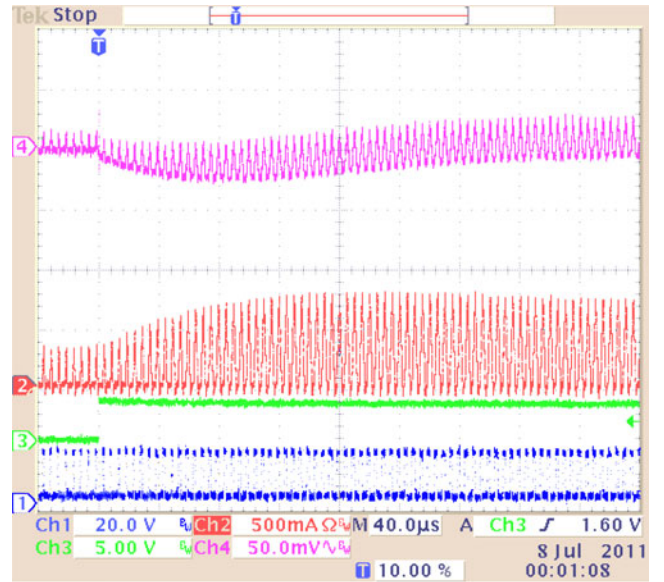


(b)

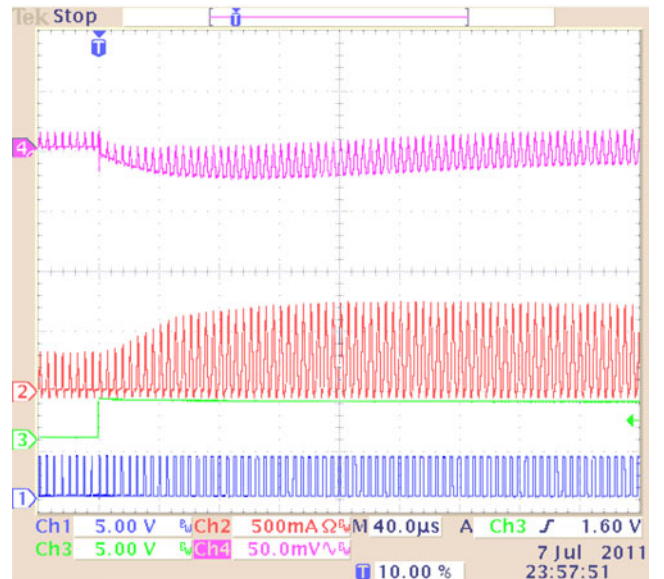
Fig. 9. Measured CCM transient response of the digital system using Tektronix TDS3014B as load is switched from 67% ( $6\ \Omega$ ) to 100% ( $4\ \Omega$ ) and vice versa. Ch1 denotes switch PWM. Ch2 denotes output inductor current. Ch3 denotes load switching (high: 100%, low: 67%). Ch4 denotes ac coupled output voltage. (a) Measured transient response of digital system. (b) Close up view of digital system transient response.

ESR. The transient response measurements should, therefore, be taken as the average of this waveform over each switching cycle. The inductor current (Ch2) of the analog and digital systems can be clearly seen in Figs. 8(b) and 9(b), respectively. The effective regulation of the peak current by the digital controller as the load changes is shown. The digital response in Fig. 9(b) is almost identical to the analog response in Fig. 8(b).

The transient responses in Figs. 8 and 9 both show a stable overdamped response with a settling time of approximately  $80\ \mu\text{s}$  and less than 50 mV overshoot. The overdamped response is indicative of a good phase margin. The digital transient re-



(a)



(b)

Fig. 10. Measured DCM transient response using Tektronix TDS3014B as load is switched from 1% ( $330\ \Omega$ ) to 10% ( $38\ \Omega$ ). (a) Measured transient response of analog system. (b) Measured transient response of digital system.

sponse in Fig. 9 is marginally better than the analog counterpart as the digital system has a lower phase margin. This is due to the phase margin erosion discussed earlier.

Under discontinuous conduction mode (DCM) the control-to-output transfer function of the peak current mode converter changes [23]. The controller has been designed to meet the crossover and phase margin specifications for CCM only. However, it is prudent to check the transient response of the converter when operating in both CCM and DCM modes to ensure stability and speed of response. The transient response of both analog and digital control methods under DCM operation is shown in Fig. 10(a) and (b). The response is stable as the load is switched from 1% to 10% and vice versa. The settling

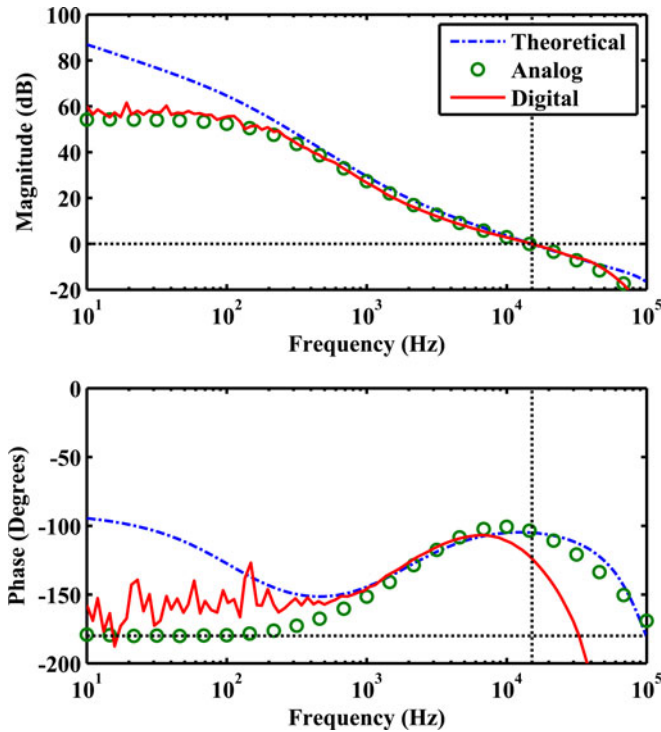


Fig. 11. Measured open-loop frequency response at full load, 16 W, using an OMICRON Lab Bode 100 vector network analyzer. Crossover frequency/phase margin: Analog (15 kHz, 76°.) Digital (15 kHz, 58°.)

time under DCM has increased to approximately  $300 \mu\text{s}$ , due to the change in control-to-output model, with the overshoot remaining less than 50 mV.

From the figures, under both CCM and DCM, it can be seen that the behavior of the novel digital peak current mode controller is equivalent to its analog counterpart as both control schemes show a similar response to the stepped change in load.

To further confirm the suitability of the proposed digital scheme, frequency domain analysis is used. The open-loop frequency response of the converter is measured in Fig. 11 using an OMICRON Lab Bode 100 vector network analyzer. Both analog and digital control methods have a 15 kHz crossover frequency for fast transient response. The measured analog phase margin of  $76^\circ$  matches the design specification and the lower digital phase margin of  $58^\circ$  is due to the phase margin erosion. The expected digital phase margin after phase erosion calculated in 38 was  $62^\circ$ . The difference would be due to any additional delays unaccounted for within the system.

The deviations from the theoretical results at the lower frequencies are expected. In order to achieve the high crossover frequency a large gain is required. However, in reality the gain bandwidth product of the error amplifier used in the analog design will limit this gain. As the frequency increases, and the required gain reduces, the amplifier re-enters its linear region.

An analogous effect occurs in the digital domain. Quantization errors occur in both the ADC and DAC. Furthermore, the microcontroller has a 32-bit word length and uses fixed point arithmetic resulting in additional quantization during calculations. This, combined with the limited output range of the DAC,

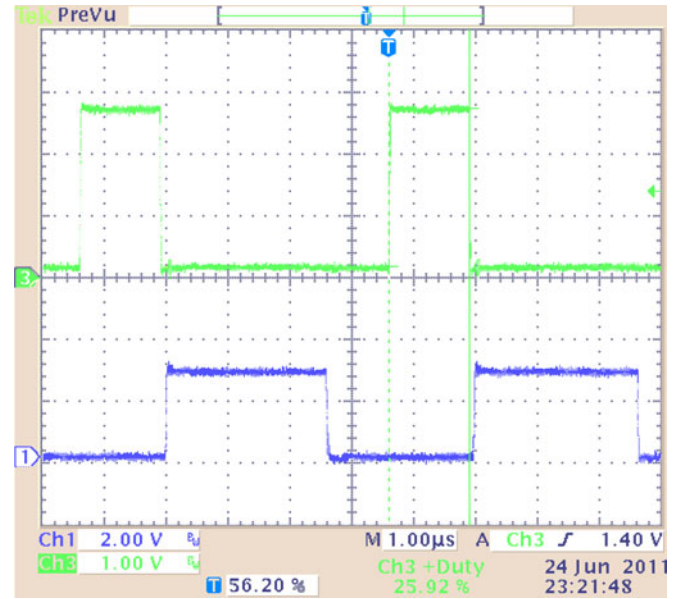


Fig. 12. Digital controller subroutine execution time versus the switching period. Controller occupies less than 26% of MCU bandwidth. Ch1 denotes switch PWM. Ch3 denotes toggle of output pin indicating controller start/finish.

has the effect of limiting the low-frequency gain, similar to the gain bandwidth product limitation of the analog domain. This can result in limit cycling if the microcontroller modules have insufficient resolution [24]. Therefore, it is necessary to calculate the minimum number of bits required for ADC, DAC (or DPWM) modules before selecting the appropriate microcontroller [25], [26]. The results obtained during this experiment show that, in both systems, the low-frequency gain is sufficiently large for this not to be an issue.

The controller is coded such that an output pin is toggled when the subroutine starts and finishes. Fig. 12 plots the duration of the controller subroutine against the switching period. The controller occupies 26% of the switching period leaving 74% of the period available to perform other tasks. As discussed in Section I, this could include running multiple converters, communications, condition monitoring, and a user interface. This presents a clear advantage over analog control in systems where a microcontroller is already used. Given sufficient bandwidth, the analog control components could be removed and this task would be performed by the microcontroller already within the system, reducing the overall cost of the design and increasing the flexibility.

Finally, the steady-state operation of the converter is shown in Fig. 13. The DAC and slope compensation modules are internal to the microcontroller and set in software. Thus, these cannot be included on the oscilloscope plot. However, the output of the peak current detection comparator is available (Ch3) and marks the end of the PWM duty cycle (Ch1) as the switch current has reached the reference value set by the controller. The duty at full load is 51% and no subharmonic oscillations are observed.

Fig. 5 in Section VII measures the control-to-output transfer function of the hardware converter with varying degrees of digital slope compensation. For the case where no digital slope



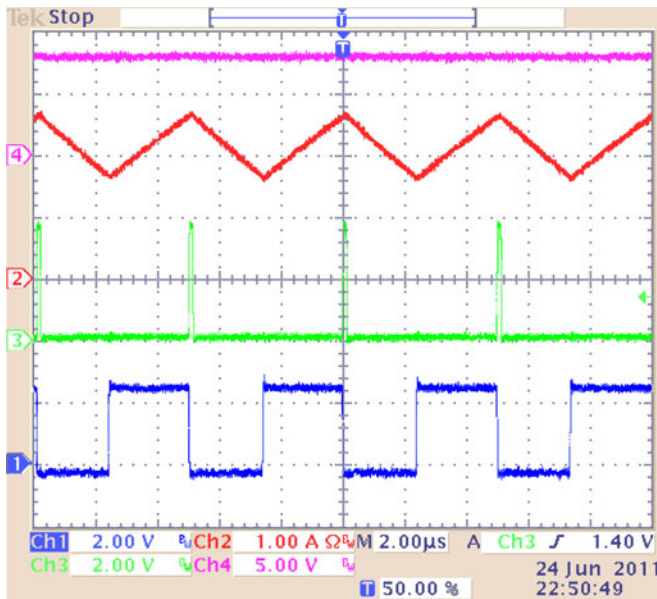


Fig. 13. Steady-state waveforms at 100% load. Ch1 denotes switch PWM. Ch2 denotes output inductor current. Ch3 denotes comparator output (PWM module trip input). Ch4 denotes output voltage.

compensation is added,  $\Delta\text{Ramp} = 0$ , the system is unstable as subharmonic oscillations are observed. The resonant peak at half the switching frequency is clearly underdamped. In the hardware experimentations presented in this section, the digital slope compensation method is used and the system is stable. This indicates that the novel digital staircase slope compensation method presented in this paper is effective.

## X. CONCLUSION

A new method of implementing peak current mode control using a discrete time controller, digital staircase slope compensation, and a mixed signal comparator that enables cycle-by-cycle current limiting and, therefore, true peak current mode operation has been described.

Using established continuous time domain models [13], the compensator poles and zeros are analytically calculated in the continuous time domain and converted into the discrete time domain using the bilinear transform. The discrete time two-pole, two-zero controller is implemented as a linear difference equation within the microcontroller.

A novel digital staircase ramp is used to implement the digital slope compensation required to damp subharmonic oscillations. Experimental measurements indicate that the digital staircase has the same effect as analog slope compensation and is able to accurately remove the resonant peak at half the switching frequency. Furthermore, the control-to-output transfer function is measured with and without digital slope compensation. The measurement indicates that the system will be unstable without the digital slope compensation and stable when the compensation is added. Thus, the effectiveness of this compensation scheme is shown. Equations are given to calculate the ramp parameters to implement this effective method of digital slope compensation.

Frequency response measurements confirm that the converter using digital control is able to match the performance of the converter using analog control in terms of a high crossover frequency and good phase margin for this design specification.

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