CY8C55, CY8C54, CY8C53, CY8C52

PSoC® 5 Registers TRM

(Technical Reference Manual)

Spec # 001-72718 Rev. *B

June 5, 2012

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

Phone (USA): 800.858.1810
Phone (Intnl): 408.943.2600
http://www.cypress.com

Copyrights

Copyright © 2011-2012 Cypress Semiconductor Corporation. All rights reserved.

PSoC® is a registered trademark and PSoC Designer™ is a trademark of Cypress Semiconductor Corporation (Cypress), along with Cypress® and Cypress Semiconductor™. All other trademarks or registered trademarks referenced herein are the property of their respective owners.

Purchase of I^2C components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips. As from October 1st, 2006 Philips Semiconductors has a new trade name - NXP Semiconductors.

The information in this document is subject to change without notice and should not be construed as a commitment by Cypress. While reasonable precautions have been taken, Cypress assumes no responsibility for any errors that may appear in this document. No part of this document may be copied, or reproduced for commercial use, in any form or by any means without the prior written consent of Cypress. Made in the U.S.A.

Disclaimer

CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Flash Code Protection

Cypress products meet the specifications contained in their particular Cypress PSoC Data Sheets. Cypress believes that its family of PSoC products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

Contents

Section J: Register Mapping **59**

1.1 Maneuvering Around the Registers 59
1.2 Register Conventions 59
1.3 PSoC 5 Register Map 60
1.3.1 FLASH_DATA[0..262143] 97
DATA
1.3.2 SRAM_CODE64K[0..16383] 98
Code System Memory Bank
1.3.3 SRAM_CODE32K[0..8191] 99
Code System Memory Bank
1.3.4 SRAM_CODE16K[0..4095] 100
Code System Memory Bank
1.3.5 SRAM_CODE[0..4095] 101
Code System Memory Bank
1.3.6 SRAM_DATA[0..4095] 102
Data System Memory Bank
1.3.7 SRAM_DATA16K[0..4095] 103
Data System Memory Bank
1.3.8 SRAM_DATA32K[0..8191] 104
Data System Memory Bank
1.3.9 SRAM_DATA64K[0..16383] 105
Data System Memory Bank
1.3.10 CLKDIST_CR 106
Configuration Register CR
1.3.11 CLKDIST_LD 108
LOAD Register
1.3.12 CLKDIST_WRK0 109
LSB Shadow Divider Value Register
1.3.13 CLKDIST_WRK1 110
MSB Shadow Divider Value Register
1.3.14 CLKDIST_MSTR0 111
Master clock (clk_sync_d) Divider Value Register
1.3.15 CLKDIST_MSTR1 112
Master (clk_sync_d) Configuration Register/CPU Divider Value
1.3.16 CLKDIST_BCFG0 113
CLK_BUS LSB Divider Value Register
1.3.17 CLKDIST_BCFG1 114
CLK_BUS MSB Divider Value Register
1.3.18 CLKDIST_BCFG2 115
CLK_BUS Configuration Register
1.3.19 CLKDIST_UCFG 116
USB Configuration Register
1.3.20 CLKDIST_DLY0 117

Delay block Configuration Register
1.3.21 CLKDIST_DLY1 118
Delay block Configuration Register
1.3.22 CLKDIST_DMASK 120
Digital Clock Mask Register
1.3.23 CLKDIST_AMASK 121
Analog Clock Mask Register
1.3.24 CLKDIST_DCFG[0..7]_CFG0 122
LSB Divider Value Register
1.3.25 CLKDIST_DCFG[0..7]_CFG1 123
MSB Divider Value Register
1.3.26 CLKDIST_DCFG[0..7]_CFG2 124
Configuration Register
1.3.27 CLKDIST_ACFG[0..3]_CFG0 126
LSB Divider Value Register
1.3.28 CLKDIST_ACFG[0..3]_CFG1 127
MSB Divider Value Register
1.3.29 CLKDIST_ACFG[0..3]_CFG2 128
Configuration Register
1.3.30 CLKDIST_ACFG[0..3]_CFG3 130
Analog clocks Configuration Register
1.3.31 FASTCLK_IMO_CR 131
Internal Main Oscillator Control Register
1.3.32 FASTCLK_XMHZ_CSR 133
External 4-33 MHz Crystal Oscillator Status and Control Register
1.3.33 FASTCLK_XMHZ_TST 135
External 4-33 MHz Crystal Oscillator Test Register
1.3.34 FASTCLK_XMHZ_CFG0 136
External 4-33 MHz Crystal Oscillator Configuration Register 0
1.3.35 FASTCLK_XMHZ_CFG1 138
RESERVED REGISTER LOCATION NOT USED IN THIS DEVICE
1.3.36 FASTCLK_PLL_CFG0 139
PLL Configuration Register
1.3.37 FASTCLK_PLL_CFG1 140
PLL Control Register
1.3.38 FASTCLK_PLL_P 141
PLL P-Counter Configuration Register
1.3.39 FASTCLK_PLL_Q 142
PLL Q-Counter Configuration Register
1.3.40 FASTCLK_PLL_TST 143
PLL Test Register
1.3.41 FASTCLK_PLL_SR 144
PLL Status Register
1.3.42 SLOWCLK_ILO_CR0 145
Internal Low-speed Oscillator Control Register 0
1.3.43 SLOWCLK_ILO_CR1 146
Internal Low-speed Oscillator Control Register 1
1.3.44 SLOWCLK_X32_CR 147
External 32kHz Crystal Oscillator Control Register
1.3.45 SLOWCLK_X32_CFG 149
External 32kHz Crystal Oscillator Configuration Register
1.3.46 SLOWCLK_X32_TST 150
External 32kHz Crystal Oscillator Test Register
1.3.47 BOOST_CR0 151

Boost Control 0
1.3.48 BOOST_CR1 153
Boost Control 1
1.3.49 BOOST_CR2 154
Boost Control 2
1.3.50 BOOST_CR3 155
Boost Control 3
1.3.51 BOOST_SR 156
Boost Status
1.3.52 PWRSYS_CR0 157
Power System Control Register 0
1.3.53 PWRSYS_CR1 158
Power System Control Register 1
1.3.54 PM_TW_CFG0 159
Timewheel Configuration Register 0
1.3.55 PM_TW_CFG1 160
Timewheel Configuration Register 1
1.3.56 PM_TW_CFG2 161
Timewheel Configuration Register 2
1.3.57 PM_WDT_CFG 162
Watchdog Timer Configuration Register
1.3.58 PM_WDT_CR 163
Watchdog Timer Control Register
1.3.59 PM_INT_SR 164
Power Manager Interrupt Status Register
1.3.60 PM_MODE_CFG0 165
Power Mode Configuration Register 0
1.3.61 PM_MODE_CFG1 166
Power Mode Configuration Register 1
1.3.62 PM_MODE_CSR 167
Power Mode Control/Status Register
1.3.63 PM_ACT_CFG0 169
Active Power Mode Configuration Register 0
1.3.64 PM_ACT_CFG1 170
Active Power Mode Configuration Register 1
1.3.65 PM_ACT_CFG2 171
Active Power Mode Configuration Register 2
1.3.66 PM_ACT_CFG3 172
Active Power Mode Configuration Register 3
1.3.67 PM_ACT_CFG4 173
Active Power Mode Configuration Register 4
1.3.68 PM_ACT_CFG5 174
Active Power Mode Configuration Register 5
1.3.69 PM_ACT_CFG6 175
Active Power Mode Configuration Register 6
1.3.70 PM_ACT_CFG7 176
Active Power Mode Configuration Register 7
1.3.71 PM_ACT_CFG8 177
Active Power Mode Configuration Register 8
1.3.72 PM_ACT_CFG9 178
Active Power Mode Configuration Register 9
1.3.73 PM_ACT_CFG10 179
Active Power Mode Configuration Register 10
1.3.74 PM_ACT_CFG11 180

Active Power Mode Configuration Register 11
1.3.75 PM_STBY_CFG0 181
Standby Power Mode Configuration Register 0
1.3.76 PM_STBY_CFG1 182
Standby Power Mode Configuration Register 1
1.3.77 PM_STBY_CFG2 183
Standby Power Mode Configuration Register 2
1.3.78 PM_STBY_CFG3 184
Standby Power Mode Configuration Register 3
1.3.79 PM_STBY_CFG4 185
Standby Power Mode Configuration Register 4
1.3.80 PM_STBY_CFG5 186
Standby Power Mode Configuration Register 5
1.3.81 PM_STBY_CFG6 187
Standby Power Mode Configuration Register 6
1.3.82 PM_STBY_CFG7 188
Standby Power Mode Configuration Register 7
1.3.83 PM_STBY_CFG8 189
Standby Power Mode Configuration Register 8
1.3.84 PM_STBY_CFG9 190
Standby Power Mode Configuration Register 9
1.3.85 PM_STBY_CFG10 191
Standby Power Mode Configuration Register 10
1.3.86 PM_STBY_CFG11 192
Standby Power Mode Configuration Register 11
1.3.87 PM_AVAIL_CR0 193
Power Mode Available Subsystem Control Register 0
1.3.88 PM_AVAIL_CR1 194
Power Mode Available Subsystem Control Register 1
1.3.89 PM_AVAIL_CR2 195
Power Mode Available Subsystem Control Register 2
1.3.90 PM_AVAIL_CR3 196
Power Mode Available Subsystem Control Register 3
1.3.91 PM_AVAIL_CR4 197
Power Mode Available Subsystem Control Register 4
1.3.92 PM_AVAIL_CR5 198
Power Mode Available Subsystem Control Register 5
1.3.93 PM_AVAIL_CR6 199
Power Mode Available Subsystem Control Register 6
1.3.94 PM_AVAIL_SR0 200
Power Mode Available Subsystem Status Register 0
1.3.95 PM_AVAIL_SR1 201
Power Mode Available Subsystem Status Register 1
1.3.96 PM_AVAIL_SR2 202
Power Mode Available Subsystem Status Register 2
1.3.97 PM_AVAIL_SR3 203
Power Mode Available Subsystem Status Register 3
1.3.98 PM_AVAIL_SR4 204
Power Mode Available Subsystem Status Register 4
1.3.99 PM_AVAIL_SR5 205
Power Mode Available Subsystem Status Register 5
1.3.100 PM_AVAIL_SR6 206
Power Mode Available Subsystem Status Register 6
1.3.101 PICU[0..15]_INTTYPE[0..7] 207

Port Interrupt Control Type Register
1.3.102PICU[0..15]_INTSTAT 209
Port Interrupt Control Status Register
1.3.103PICU[0..15]_SNAP 210
Port Interrupt Control Snap Shot Register
1.3.104CMP[0..3]_TR 211
Comparator Trim Register
1.3.105DAC[0..3]_TR 213
DAC Block Trim Register
1.3.106NPUMP_DSM_TR0 214
Delta Sigma Modulator (DSM) Negative Pump Trim Register 0
1.3.107NPUMP_ABUF_TR0 215
Analog Linear Output Buffer (ABUF) Negative Pump Trim Register 0
1.3.108SAR[0..1]_TR0 216
SAR trim register 0
1.3.109ABUF[0..3]_TR0 217
Analog Output Buffer Trim Register 0
1.3.110ABUF[0..3]_TR1 218
Analog Output Buffer Trim Register 1
1.3.111PWRSYS_HIB_TR0 219
Hibernate Trim Register 0
1.3.112PWRSYS_HIB_TR1 220
Hibernate Trim Register 1
1.3.113PWRSYS_I2C_TR 221
I2C Regulator Trim Register 1
1.3.114PWRSYS_SLP_TR 222
Sleep Regulator Trim Register
1.3.115PWRSYS_BUZZ_TR 223
Power Mode Buzz Trim Register
1.3.116PWRSYS_WAKE_TR0 224
Power Mode Wakeup Trim Register
1.3.117PWRSYS_WAKE_TR1 225
Power Mode Wakeup Trim Register
1.3.118PWRSYS_BREF_TR 226
Boot Reference Trim Register
1.3.119PWRSYS_BG_TR 227
Bandgap Trim
1.3.120ILO_TR0 228
Internal Low-speed Oscillator Trim Register
1.3.121ILO_TR1 229
Internal Low-speed Oscillator Coarse Trim Register
1.3.122X32_TR 230
32 kHz Watch Crystal Oscillator Trim Register
1.3.123IMO_TR0 231
Internal Main Oscillator Trim Register 0
1.3.124IMO_TR1 232
Internal Main Oscillator Trim Register 1
1.3.125IMO_GAIN 233
Internal Main Oscillator Gain Trim Register
1.3.126IMO_C36M 234
Internal Main Oscillator 36 MHz clock control register {INTERNAL}
1.3.127IMO_TR2 235
Internal Main Oscillator Trim Register 2
1.3.128XMHZ_TR 236

External 4-25 MHz Crystal Oscillator Trim Register
1.3.129MLOGIC_DMP_DMY 237
Dumpster Register
1.3.130MLOGIC_SEG_CR 238
Segment Control Register
1.3.131MLOGIC_SEG_CFG0 239
Segment Configuration Register
1.3.132MLOGIC_DBG_DBE 240
Debug Enable Register
1.3.133MLOGIC_CPU_SCR 241
System Status and Control Register
1.3.134RESET_IPOR_CR0 242
Imprecise Power On Reset Control Register 0
1.3.135RESET_IPOR_CR1 243
Imprecise Power On Reset Control Register 1
1.3.136RESET_IPOR_CR2 244
Imprecise Power On Reset Control Register 2
1.3.137RESET_IPOR_CR3 245
Imprecise Power On Reset Control Register 3
1.3.138RESET_CR0 246
LVI Set Point Control Register
1.3.139RESET_CR1 247
Reset System Control Register
1.3.140RESET_CR2 248
Software Reset Control Register
1.3.141RESET_CR3 249
LVD/POR Test Mode Control Register
1.3.142RESET_SR0 250
Reset and Voltage Detection Status Register 0
1.3.143RESET_SR1 251
Reset and Voltage Detection Status Register 1
1.3.144RESET_SR2 252
Reset and Voltage Detection Status Register 2
1.3.145RESET_TR 253
PRES Trim Register
1.3.146SPC_FM_EE_CR 254
FM_EE_CR
1.3.147SPC_FM_EE_WAKE_CNT 255
FM_EE_WAKE_CNT
1.3.148SPC_EE_SCR 256
EEPROM Status & Control Register
1.3.149SPC_EE_ERR 257
EEPROM Error Register
1.3.150SPC_CPU_DATA 258
SPC CPU Data Register
1.3.151SPC_DMA_DATA 259
SPC DMA Data Register
1.3.152SPC_SR 260
SPC Status Register
1.3.153SPC_CR 261
SPC Control Register
1.3.154SPC_DMM_MAP_SRAM[0..127] 262
SPC Direct Memory Mapping
1.3.155CACHE_CC_CTL 263

Cache Control Register
1.3.156CACHE_ECC_CORR 265
Error Correction detected
1.3.157CACHE_ECC_ERR 266
Error Correction failed
1.3.158CACHE_FLASH_ERR 267
FLASH error
1.3.159CACHE_HITMISS 268
HIT/MISS counters
1.3.160I2C_XCFG 270
I2C Extended Configuration Register
1.3.161I2C_ADR 271
I2C Slave Adddress Register
1.3.162I2C_CFG 272
I2C Configuration Register
1.3.163I2C_CSR 274
I2C Control and Status Register
1.3.164I2C_D 276
I2C Data Register
1.3.165I2C_MCSR 277
I2C Master Control and Status Register
1.3.166I2C_CLK_DIV 278
I2C Clock Divide Factor Register
1.3.167DEC_CR 279
Decimator Control Register
1.3.168DEC_SR 281
Decimator Status Register
1.3.169DEC_SHIFT1 283
Decimator Shifter 1 (Input)
1.3.170DEC_SHIFT2 284
Decimator Shifter 2 (Output)
1.3.171DEC_DR2 285
Decimator Decimation Rate (2)
1.3.172DEC_DR2H 286
Decimator Decimation Rate (2)
1.3.173DEC_DR1 287
Decimator Decimation Rate (1) of CIC Filter
1.3.174DEC_OCOR 288
Decimator Offset Correction Coefficient (Low Byte)
1.3.175DEC_OCORM 289
Decimator Offset Correction Coefficient (Middle Byte)
1.3.176DEC_OCORH 290
Decimator Offset Correction Coefficient (High Byte)
1.3.177DEC_GCOR 291
Decimator Gain Correction Coefficient (Low Byte)
1.3.178DEC_GCORH 292
Decimator Gain Correction Coefficient (High Byte)
1.3.179DEC_GVAL 293
Decimator Gain Correction Size Register
1.3.180DEC_OUTSAMP 294
Decimator Output Data Sample (Low Byte)
1.3.181DEC_OUTSAMPM 295
Decimator Output Data Sample (Middle Byte)
1.3.182DEC_OUTSAMPH 296

Decimator Output Data Sample (High Byte)
1.3.183DEC_OUTSAMPS 297
Decimator Output Data Sample (Sign Extension)
1.3.184DEC_COHER 298
Decimator Coherency Register
1.3.185TMR[0..3]_CFG0 300
Configuration Register CFG0
1.3.186TMR[0..3]_CFG1 301
Configuration Register CFG1
1.3.187TMR[0..3]_PER0 303
Timer Period Register PER0
1.3.188TMR[0..3]_PER1 304
Timer Period Register PER1
1.3.189TMR[0..3]_CNT_CMP0 305
Count/Comparator value CNT/CMP0
1.3.190TMR[0..3]_CNT_CMP1 306
Count/Comparator value CNT/CMP1
1.3.191TMR[0..3]_CAP0 307
Capture Value CAP0
1.3.192TMR[0..3]_CAP1 308
Capture Value CAP1
1.3.193TMR[0..3]_SR0 309
Status Register SR0
1.3.194TMR[0..3]_RT0 310
Configuration Register RT0
1.3.195TMR[0..3]_RT1 311
Configuration Register RT1
1.3.196PRT[0..15]_PC[0..7] 312
Port Pin Configuration Register
1.3.197PRT[0..15]_DR_ALIAS 314
Aliased Port Data Output Register
1.3.198PRT[0..15]_PS_ALIAS 315
Aliased Port Pin State Register
1.3.199PRT[0..11]_DR 316
Port Data Output Register
1.3.200PRT[0..11]_PS 317
Port Pin State Register1
1.3.201PRT[0..11]_DM[0..2] 318
Port Drive Mode Register
1.3.202PRT[0..11]_SLW 320
Port slew rate control
1.3.203PRT[0..11]_BYP 321
Port Bypass enable
1.3.204PRT[0..11]_BIE 322
Port Bidirection enable
1.3.205PRT[0..11]_INP_DIS 323
Input buffer disable override
1.3.206PRT[0..11]_CTL 324
Port wide control signals
1.3.207PRT[0..11]_PRT 325
Port wide configuration register
1.3.208PRT[0..11]_BIT_MASK 326
Bit-mask for Aliased Register access
1.3.209PRT[0..11]_AMUX 327

Port Analog global mux bus enable
1.3.210PRT[0..11]_AG 328
Port Analog global enable
1.3.211PRT[0..11]_LCD_COM_SEG 329
Port LCD Com seg bits.
1.3.212PRT[0..11]_LCD_EN 330
Port LCD enable register.
1.3.213PRT12_DR 331
Port Data Output Register
1.3.214PRT12_PS 332
Port Pin State Register1
1.3.215PRT12_DM[0..2] 333
Port Drive Mode Register
1.3.216PRT12_SLW 334
Port slew rate control
1.3.217PRT12_BYP 335
Port Bypass enable
1.3.218PRT12_BIE 336
Port Bidirection enable
1.3.219PRT12_INP_DIS 337
Input buffer disable override
1.3.220PRT12_SIO_HYST_EN 338
SIO Hysteresis enable
1.3.221PRT12_PRT 339
Port wide configuration register
1.3.222PRT12_BIT_MASK 340
Bit-mask for Aliased Register access
1.3.223PRT12_SIO_REG_HIFREQ 341
Regulated pull-up driver DC current setting
1.3.224PRT12_AG 342
Port Analog global enable
1.3.225PRT12_SIO_CFG 343
SIO Input Output Configuration
1.3.226PRT12_SIO_DIFF 344
Differential Input Buffer reference voltage selection
1.3.227PRT15_DR 345
Port Data Output Register
1.3.228PRT15_PS 346
Port Pin State Register1
1.3.229PRT15_DM[0..2] 347
Port Drive Mode Register
1.3.230PRT15_SLW 348
Port slew rate control
1.3.231PRT15_BYP 349
Port Bypass enable
1.3.232PRT15_BIE 350
Port Bidirection enable
1.3.233PRT15_INP_DIS 351
Input buffer disable override
1.3.234PRT15_CTL 352
Port wide control signals
1.3.235PRT15_PRT 353
Port wide configuration register
1.3.236PRT15_BIT_MASK 354

Bit-mask for Aliased Register access
1.3.237PRT15_AMUX 355
Port Analog global mux bus enable
1.3.238PRT15_AG 356
Port Analog global enable
1.3.239PRT15_LCD_COM_SEG 357
Port LCD Com seg bits.
1.3.240PRT15_LCD_EN 358
Port LCD enable register.
1.3.241PRT0_OUT_SEL0 359
Digital System Interconnect Port Pin Output Select Registers.
1.3.242PRT0_OUT_SEL1 360
Digital System Interconnect Port Pin Output Select Registers.
1.3.243PRT0_OE_SEL0 361
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.244PRT0_OE_SEL1 362
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.245PRT0_DBL_SYNC_IN 363
DSI double sync enable register.
1.3.246PRT0_SYNC_OUT 364
DSI sync out enable register.
1.3.247PRT0_CAPS_SEL 365
Global DSI select register.
1.3.248PRT1_OUT_SEL0 366
Digital System Interconnect Port Pin Output Select Registers.
1.3.249PRT1_OUT_SEL1 367
Digital System Interconnect Port Pin Output Select Registers.
1.3.250PRT1_OE_SEL0 368
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.251PRT1_OE_SEL1 369
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.252PRT1_DBL_SYNC_IN 370
DSI double sync enable register.
1.3.253PRT1_SYNC_OUT 371
DSI sync out enable register.
1.3.254PRT1_CAPS_SEL 372
Global DSI select register.
1.3.255PRT2_OUT_SEL0 373
Digital System Interconnect Port Pin Output Select Registers.
1.3.256PRT2_OUT_SEL1 374
Digital System Interconnect Port Pin Output Select Registers.
1.3.257PRT2_OE_SEL0 375
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.258PRT2_OE_SEL1 376
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.259PRT2_DBL_SYNC_IN 377
DSI double sync enable register.
1.3.260PRT2_SYNC_OUT 378
DSI sync out enable register.
1.3.261PRT2_CAPS_SEL 379
Global DSI select register.
1.3.262PRT3_OUT_SEL0 380
Digital System Interconnect Port Pin Output Select Registers.
1.3.263PRT3_OUT_SEL1 381

Digital System Interconnect Port Pin Output Select Registers.
1.3.264PRT3_OE_SEL0 382
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.265PRT3_OE_SEL1 383
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.266PRT3_DBL_SYNC_IN 384
DSI double sync enable register.
1.3.267PRT3_SYNC_OUT 385
DSI sync out enable register.
1.3.268PRT3_CAPS_SEL 386
Global DSI select register.
1.3.269PRT4_OUT_SEL0 387
Digital System Interconnect Port Pin Output Select Registers.
1.3.270PRT4_OUT_SEL1 388
Digital System Interconnect Port Pin Output Select Registers.
1.3.271PRT4_OE_SEL0 389
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.272PRT4_OE_SEL1 390
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.273PRT4_DBL_SYNC_IN 391
DSI double sync enable register.
1.3.274PRT4_SYNC_OUT 392
DSI sync out enable register.
1.3.275PRT4_CAPS_SEL 393
Global DSI select register.
1.3.276PRT5_OUT_SEL0 394
Digital System Interconnect Port Pin Output Select Registers.
1.3.277PRT5_OUT_SEL1 395
Digital System Interconnect Port Pin Output Select Registers.
1.3.278PRT5_OE_SEL0 396
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.279PRT5_OE_SEL1 397
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.280PRT5_DBL_SYNC_IN 398
DSI double sync enable register.
1.3.281PRT5_SYNC_OUT 399
DSI sync out enable register.
1.3.282PRT5_CAPS_SEL 400
Global DSI select register.
1.3.283PRT6_OUT_SEL0 401
Digital System Interconnect Port Pin Output Select Registers.
1.3.284PRT6_OUT_SEL1 402
Digital System Interconnect Port Pin Output Select Registers.
1.3.285PRT6_OE_SEL0 403
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.286PRT6_OE_SEL1 404
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.287PRT6_DBL_SYNC_IN 405
DSI double sync enable register.
1.3.288PRT6_SYNC_OUT 406
DSI sync out enable register.
1.3.289PRT6_CAPS_SEL 407
Global DSI select register.
1.3.290PRT12_OUT_SEL0 408

Digital System Interconnect Port Pin Output Select Registers.
1.3.291PRT12_OUT_SEL1 409
Digital System Interconnect Port Pin Output Select Registers.
1.3.292PRT12_OE_SEL0 410
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.293PRT12_OE_SEL1 411
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.294PRT12_DBL_SYNC_IN 412
DSI double sync enable register.
1.3.295PRT12_SYNC_OUT 413
DSI sync out enable register.
1.3.296PRT15_OUT_SEL0 414
Digital System Interconnect Port Pin Output Select Registers.
1.3.297PRT15_OUT_SEL1 415
Digital System Interconnect Port Pin Output Select Registers.
1.3.298PRT15_OE_SEL0 416
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.299PRT15_OE_SEL1 417
Dynamic Drive Stength of Port Output Enable Select registers.
1.3.300PRT15_DBL_SYNC_IN 418
DSI double sync enable register.
1.3.301PRT15_SYNC_OUT 419
DSI sync out enable register.
1.3.302PRT15_CAPS_SEL 420
Global DSI select register.
1.3.303EMIF_NO_UDB 421
EMIF UDB Generation Register
1.3.304EMIF_WAIT_STATES 422
External Memory Interface Wait States Register
1.3.305EMIF_MEM_DWN 423
External Memory Power Down Register
1.3.306EMIF_MEMCLK_DIV 424
External Memory Clock Divider Register
1.3.307EMIF_CLOCK_EN 425
EMIF Clock Enable Register
1.3.308SC[0..3]_CR0 426
Switched Capacitor Control Register 0
1.3.309SC[0..3]_CR1 427
Switched Capacitor Control Register 1
1.3.310SC[0..3]_CR2 429
Switched Capacitor Control Register 2
1.3.311DAC[0..3]_CR0 431
DAC Block Control Register 0
1.3.312DAC[0..3]_CR1 432
DAC Block Control Register 1
1.3.313DAC[0..3]_TST 434
DAC Block Test Register
1.3.314CMP[0..3]_CR 436
Comparator Control Register
1.3.315LUT[0..3]_CR 438
LUT Config Register
1.3.316LUT[0..3]_MX 439
LUT Input Mux Config Register
1.3.317ABUF[0..3]_CR 440

Analog Output Buffer Configuration Register
1.3.318ABUF[0..3]_RSVD 441
ABUF reserved
1.3.319LCDDAC_CR0 442
LCD Control Register 0
1.3.320LCDDAC_CR1 443
LCDDAC Control Register 1
1.3.321LCDDRV_CR 444
LCD Control Register
1.3.322BG_CR0 445
Bandgap Precision Reference Control 0
1.3.323BG_RSVD 446
Bandgap Precision Reference Reserved Register
1.3.324BG_DFT0 447
Bandgap Precision Reference DFT Register 0
1.3.325BG_DFT1 448
Bandgap Precision Reference DFT Register 1
1.3.326CAPSL_CFG0 449
Capsense Reference Driver Configuration Register
1.3.327CAPSL_CFG1 451
Capsense IO Configuration Register
1.3.328CAPSR_CFG0 452
Capsense Reference Driver Configuration Register
1.3.329CAPSR_CFG1 454
Capsense IO Configuration Register
1.3.330CAPS_DFT 455
Capsense DFT register
1.3.331PUMP_CR0 456
Pump Configuration Register 0
1.3.332PUMP_CR1 457
Pump Configuration Register 1
1.3.333LPF0_CR0 458
Low Pass Filter Control Register
1.3.334LPF0_RSVD 460
LPF Reserved
1.3.335LPF1_CR0 461
Low Pass Filter Control Register
1.3.336LPF1_RSVD 463
LPF Reserved
1.3.337ANAIF_CFG_MISC_CR0 464
MISC Control Register 0
1.3.338TFAULT_CR0 465
Timing Fault Control Register 0
1.3.339TFAULT_CR1 466
Timing Fault Control Register 1
1.3.340DSM[0..0]_CR0 468
Delta Sigma Modulator Control Register 0
1.3.341DSM[0..0]_CR1 469
Delta Sigma Modulator Control Register 1
1.3.342DSM[0..0]_CR2 470
Delta Sigma Modulator Control Register 2
1.3.343DSM[0..0]_CR3 472
Delta Sigma Modulator Control Register 3
1.3.344DSM[0..0]_CR4 474

Delta Sigma Modulator Control Register 4
1.3.345DSM[0..0]_CR5 475
Delta Sigma Modulator Control Register 5
1.3.346DSM[0..0]_CR6 476
Delta Sigma Modulator Control Register 6
1.3.347DSM[0..0]_CR7 477
Delta Sigma Modulator Control Register 7
1.3.348DSM[0..0]_CR8 479
Delta Sigma Modulator Control Register 8
1.3.349DSM[0..0]_CR9 481
Delta Sigma Modulator Control Register 9
1.3.350DSM[0..0]_CR10 483
Delta Sigma Modulator Control Register 10
1.3.351DSM[0..0]_CR11 485
Delta Sigma Modulator Control Register 11
1.3.352DSM[0..0]_CR12 487
Delta Sigma Modulator Control Register 12
1.3.353DSM[0..0]_CR13 489
Delta Sigma Modulator Control Register 13
1.3.354DSM[0..0]_CR14 490
Delta Sigma Modulator Control Register 14
1.3.355DSM[0..0]_CR15 491
Delta Sigma Modulator Control Register 15
1.3.356DSM[0..0]_CR16 492
Delta Sigma Modulator Control Register 0
1.3.357DSM[0..0]_CR17 493
Delta Sigma Modulator Control Register
1.3.358DSM[0..0]_REF0 495
Delta Sigma Modulator Reference Register 0
1.3.359DSM[0..0]_REF1 496
Delta Sigma Modulator Reference Register 1
1.3.360DSM[0..0]_REF2 497
Delta Sigma Modulator Reference Register 2
1.3.361DSM[0..0]_REF3 498
Delta Sigma Modulator Reference Register 1
1.3.362DSM[0..0]_DEM0 499
Delta Sigma Modulator Dynamic Element Matching Register 0
1.3.363DSM[0..0]_DEM1 501
Delta Sigma Modulator Dynamic Element Matching Register 1
1.3.364DSM[0..0]_TST0 502
Delta Sigma Modulator Test Register 0
1.3.365DSM[0..0]_TST1 503
Delta Sigma Modulator Test Register 1
1.3.366DSM[0..0]_BUF0 504
Delta Sigma Modulator Buffer Register 0
1.3.367DSM[0..0]_BUF1 505
Delta Sigma Modulator Buffer Register 1
1.3.368DSM[0..0]_BUF2 506
Delta Sigma Modulator Buffer Register 2
1.3.369DSM[0..0]_BUF3 507
Delta Sigma Modulator Buffer Register 2
1.3.370DSM[0..0]_MISC 508
Delta Sigma Modulator Miscellaneous register
1.3.371DSM[0..0]_RSVD1 509

Delta Sigma Modulator RSVD 1
1.3.372SAR[0..1]_CSR0 510
SAR status and control register 0
1.3.373SAR[0..1]_CSR1 512
SAR status and control register 1
1.3.374SAR[0..1]_CSR2 514
SAR status and control register 2
1.3.375SAR[0..1]_CSR3 515
SAR status and control register 3
1.3.376SAR[0..1]_CSR4 517
SAR status and control register 4
1.3.377SAR[0..1]_CSR5 518
SAR status and control register 5
1.3.378SAR[0..1]_CSR6 520
SAR status and control register 6
1.3.379SAR[0..1]_CSR7 521
SAR status and control register 7
1.3.380SC0_SW0 522
Switched Capacitor Analog Routing Register 0
1.3.381SC0_SW2 523
Switched Capacitor Analog Routing Register 2
1.3.382SC0_SW3 524
Switched Capacitor Analog Routing Register 3
1.3.383SC0_SW4 525
Switched Capacitor Analog Routing Register 4
1.3.384SC0_SW6 526
Switched Capacitor Analog Routing Register 6
1.3.385SC0_SW7 527
Switched Capacitor Analog Routing Register 7
1.3.386SC0_SW8 528
Switched Capacitor Analog Routing Register 8
1.3.387SC0_SW10 529
Switched Capacitor Analog Routing Register 10
1.3.388SC0_CLK 530
Switched Capacitor Clock Selection Register
1.3.389SC0_BST 531
Switched Capacitor Boost Clock Selection Register
1.3.390SC1_SW0 532
Switched Capacitor Analog Routing Register 0
1.3.391SC1_SW2 533
Switched Capacitor Analog Routing Register 2
1.3.392SC1_SW3 534
Switched Capacitor Analog Routing Register 3
1.3.393SC1_SW4 535
Switched Capacitor Analog Routing Register 4
1.3.394SC1_SW6 536
Switched Capacitor Analog Routing Register 6
1.3.395SC1_SW7 537
Switched Capacitor Analog Routing Register 7
1.3.396SC1_SW8 538
Switched Capacitor Analog Routing Register 8
1.3.397SC1_SW10 539
Switched Capacitor Analog Routing Register 10
1.3.398SC1_CLK 540

Switched Capacitor Clock Selection Register
1.3.399SC1_BST 541
Switched Capacitor Boost Clock Selection Register
1.3.400SC2_SW0 542
Switched Capacitor Analog Routing Register 0
1.3.401SC2_SW2 543
Switched Capacitor Analog Routing Register 2
1.3.402SC2_SW3 544
Switched Capacitor Analog Routing Register 3
1.3.403SC2_SW4 545
Switched Capacitor Analog Routing Register 4
1.3.404SC2_SW6 546
Switched Capacitor Analog Routing Register 6
1.3.405SC2_SW7 547
Switched Capacitor Analog Routing Register 7
1.3.406SC2_SW8 548
Switched Capacitor Analog Routing Register 8
1.3.407SC2_SW10 549
Switched Capacitor Analog Routing Register 10
1.3.408SC2_CLK 550
Switched Capacitor Clock Selection Register
1.3.409SC2_BST 551
Switched Capacitor Boost Clock Selection Register
1.3.410SC3_SW0 552
Switched Capacitor Analog Routing Register 0
1.3.411SC3_SW2 553
Switched Capacitor Analog Routing Register 2
1.3.412SC3_SW3 554
Switched Capacitor Analog Routing Register 3
1.3.413SC3_SW4 555
Switched Capacitor Analog Routing Register 4
1.3.414SC3_SW6 556
Switched Capacitor Analog Routing Register 6
1.3.415SC3_SW7 557
Switched Capacitor Analog Routing Register 7
1.3.416SC3_SW8 558
Switched Capacitor Analog Routing Register 8
1.3.417SC3_SW10 559
Switched Capacitor Analog Routing Register 10
1.3.418SC3_CLK 560
Switched Capacitor Clock Selection Register
1.3.419SC3_BST 561
Switched Capacitor Boost Clock Selection Register
1.3.420DAC0_SW0 562
DAC Analog Routing Register 0
1.3.421DAC0_SW2 563
DAC Analog Routing Register 2
1.3.422DAC0_SW3 564
DAC Analog Routing Register 3
1.3.423DAC0_SW4 565
DAC Analog Routing Register 4
1.3.424DAC0_STROBE 566
DAC Strobe Register
1.3.425DAC1_SW0 567

DAC Analog Routing Register 0
1.3.426DAC1_SW2 568
DAC Analog Routing Register 2
1.3.427DAC1_SW3 569
DAC Analog Routing Register 3
1.3.428DAC1_SW4 570
DAC Analog Routing Register 4
1.3.429DAC1_STROBE 571
DAC Strobe Register
1.3.430DAC2_SW0 572
DAC Analog Routing Register 0
1.3.431DAC2_SW2 573
DAC Analog Routing Register 2
1.3.432DAC2_SW3 574
DAC Analog Routing Register 3
1.3.433DAC2_SW4 575
DAC Analog Routing Register 4
1.3.434DAC2_STROBE 576
DAC Strobe Register
1.3.435DAC3_SW0 577
DAC Analog Routing Register 0
1.3.436DAC3_SW2 578
DAC Analog Routing Register 2
1.3.437DAC3_SW3 579
DAC Analog Routing Register 3
1.3.438DAC3_SW4 580
DAC Analog Routing Register 4
1.3.439DAC3_STROBE 581
DAC Strobe Register
1.3.440CMP0_SW0 582
Comparator Analog Routing Register 0
1.3.441CMP0_SW2 583
Comparator Analog Routing Register 2
1.3.442CMP0_SW3 584
Comparator Analog Routing Register 3
1.3.443CMP0_SW4 585
Comparator Analog Routing Register 4
1.3.444CMP0_SW6 586
Comparator Analog Routing Register 6
1.3.445CMP0_CLK 587
Comparator Clock Control Register
1.3.446CMP1_SW0 588
Comparator Analog Routing Register 0
1.3.447CMP1_SW2 589
Comparator Analog Routing Register 2
1.3.448CMP1_SW3 590
Comparator Analog Routing Register 3
1.3.449CMP1_SW4 591
Comparator Analog Routing Register 4
1.3.450CMP1_SW6 592
Comparator Analog Routing Register 6
1.3.451CMP1_CLK 593
Comparator Clock Control Register
1.3.452CMP2_SW0 594

Comparator Analog Routing Register 0
1.3.453CMP2_SW2 595
Comparator Analog Routing Register 2
1.3.454CMP2_SW3 596
Comparator Analog Routing Register 3
1.3.455CMP2_SW4 597
Comparator Analog Routing Register 4
1.3.456CMP2_SW6 598
Comparator Analog Routing Register 6
1.3.457CMP2_CLK 599
Comparator Clock Control Register
1.3.458CMP3_SW0 600
Comparator Analog Routing Register 0
1.3.459CMP3_SW2 601
Comparator Analog Routing Register 2
1.3.460CMP3_SW3 602
Comparator Analog Routing Register 3
1.3.461CMP3_SW4 603
Comparator Analog Routing Register 4
1.3.462CMP3_SW6 604
Comparator Analog Routing Register 6
1.3.463CMP3_CLK 605
Comparator Clock Control Register
1.3.464DSM0_SW0 606
Delta Sigma Modulator Analog Routing Register 0
1.3.465DSM0_SW2 607
Delta Sigma Modulator Analog Routing Register 2
1.3.466DSM0_SW3 608
Delta Sigma Modulator Analog Routing Register 3
1.3.467DSM0_SW4 609
Delta Sigma Modulator Analog Routing Register 4
1.3.468DSM0_SW6 610
Delta Sigma Modulator Analog Routing Register 6
1.3.469DSM0_CLK 611
Delta Sigma Modulator Clock Selection Register
1.3.470SAR0_SW0 612
SAR Analog Routing Register 0
1.3.471SAR0_SW2 613
SAR Analog Routing Register 2
1.3.472SAR0_SW3 614
SAR Analog Routing Register 3
1.3.473SAR0_SW4 615
SAR Analog Routing Register 4
1.3.474SAR0_SW6 616
SAR Analog Routing Register 6
1.3.475SAR0_CLK 617
SAR Clock Selection Register
1.3.476SAR1_SW0 619
SAR Analog Routing Register 0
1.3.477SAR1_SW2 620
SAR Analog Routing Register 2
1.3.478SAR1_SW3 621
SAR Analog Routing Register 3
1.3.479SAR1_SW4 622

SAR Analog Routing Register 4
1.3.480SAR1_SW6 623
SAR Analog Routing Register 6
1.3.481SAR1_CLK 624
SAR Clock Selection Register
1.3.482ABUF0_MX 626
Analog Buffer Input Selection Register
1.3.483ABUF0_SW 627
Analog Buffer Routing Switch Register
1.3.484ABUF1_MX 628
Analog Buffer Input Selection Register
1.3.485ABUF1_SW 629
Analog Buffer Routing Switch Register
1.3.486ABUF2_MX 630
Analog Buffer Input Selection Register
1.3.487ABUF2_SW 631
Analog Buffer Routing Switch Register
1.3.488ABUF3_MX 632
Analog Buffer Input Selection Register
1.3.489ABUF3_SW 633
Analog Buffer Routing Switch Register
1.3.490LCDDAC_SW0 634
LCDDAC Switch Register 0
1.3.491LCDDAC_SW1 635
LCDDAC Switch Register 1
1.3.492LCDDAC_SW2 636
LCDDAC Switch Register 2
1.3.493LCDDAC_SW3 637
LCDDAC Switch Register 3
1.3.494LCDDAC_SW4 638
LCDDAC Switch Register 3
1.3.495SC_MISC 639
Switched Cap Miscellaneous Control Register
1.3.496BUS_SW0 640
Bus Switch Register 0
1.3.497BUS_SW2 642
Bus Switch Register 2
1.3.498BUS_SW3 643
Bus Switch Register 3
1.3.499DFT_CR0 644
DFT Control Register 0
1.3.500DFT_CR1 645
DFT Control Register 1
1.3.501DFT_CR2 646
DFT Control Register 2
1.3.502DFT_CR3 647
DFT Control Register 3
1.3.503DAC[0..3]_D 648
DAC Data Register
1.3.504DSM[0..0]_OUT0 649
DSM Output Register 0
1.3.505DSM[0..0]_OUT1 650
DSM Output Register 1
1.3.506SC_SR 651

Switched Capacitor Status Register
1.3.507SC_MSK 652
SC IRQ Mask Register
1.3.508LUT_SR 653
LUT Status Register
1.3.509LUT_MSK 654
LUT Interrupt ReQuest (IRQ) Mask Register
1.3.510CMP_WRK 655
Comparator output working register
1.3.511CMP_LTRI 656
Comparator LTRI working register
1.3.512TFAULT_WRK0 657
Timing Fault Working Register 0
1.3.513TFAULT_WRK1 658
Timing Fault Working Register 1
1.3.514TFAULT_WRK2 659
Timing Fault Working Register 2
1.3.515TFAULT_WRK3 660
Timing Fault Working Register 1
1.3.516SAR[0..1]_WRK0 661
SAR working register 0
1.3.517SAR[0..1]_WRK1 662
SAR register 1
1.3.518ANAIF_WRK_SARS_SOF 663
SAR Global Start-of-frame register
1.3.519USB_EP0_DR[0..7] 664
Control End point EP0 Data Register
1.3.520USB_CR0 665
USB control 0 Register
1.3.521USB_CR1 666
USB control 1 Register
1.3.522USB_SIE_EP_INT_EN 667
USB SIE Data Endpoints Interrupt Enable Register
1.3.523USB_SIE_EP_INT_SR 668
SIE Data Endpoint Interrupt Status
1.3.524USB_SIE_EP1_CNT0 669
Non-control endpoint count register
1.3.525USB_SIE_EP1_CNT1 670
Non-control endpoint count register
1.3.526USB_SIE_EP1_CR0 671
1.3.527USB_USBIO_CR0 672
USBIO Control 0 Register
1.3.528USB_USBIO_CR2 673
USBIO control 2 Register
1.3.529USB_USBIO_CR1 674
USBIO control 1 Register
1.3.530USB_SOF0 675
Start Of Frame Register
1.3.531USB_SOF1 676
Start Of Frame Register
1.3.532USB_SIE_EP2_CNT0 677
Non-control endpoint count register
1.3.533USB_SIE_EP2_CNT1 678
Non-control endpoint count register

1.3.534USB_SIE_EP2_CR0 679
1.3.535USB_OSCLK_DR0 680
Oscillator lock data register 0
1.3.536USB_OSCLK_DR1 681
Oscillator lock data register 1
1.3.537USB_EP0_CR 682
Endpoint0 control Register
1.3.538USB_EP0_CNT 683
Endpoint0 count Register
1.3.539USB_SIE_EP3_CNT0 684
Non-control endpoint count register
1.3.540USB_SIE_EP3_CNT1 685
Non-control endpoint count register
1.3.541USB_SIE_EP3_CR0 686
1.3.542USB_SIE_EP4_CNT0 687
Non-control endpoint count register
1.3.543USB_SIE_EP4_CNT1 688
Non-control endpoint count register
1.3.544USB_SIE_EP4_CR0 689
1.3.545USB_SIE_EP5_CNT0 690
Non-control endpoint count register
1.3.546USB_SIE_EP5_CNT1 691
Non-control endpoint count register
1.3.547USB_SIE_EP5_CR0 692
1.3.548USB_SIE_EP6_CNT0 693
Non-control endpoint count register
1.3.549USB_SIE_EP6_CNT1 694
Non-control endpoint count register
1.3.550USB_SIE_EP6_CR0 695
1.3.551USB_SIE_EP7_CNT0 696
Non-control endpoint count register
1.3.552USB_SIE_EP7_CNT1 697
Non-control endpoint count register
1.3.553USB_SIE_EP7_CR0 698
1.3.554USB_SIE_EP8_CNT0 699
Non-control endpoint count register
1.3.555USB_SIE_EP8_CNT1 700
Non-control endpoint count register
1.3.556USB_SIE_EP8_CR0 701
1.3.557USB_ARB_EP1_CFG 702
Endpoint Configuration Register
1.3.558USB_ARB_EP1_INT_EN 703
Endpoint Interrupt Enable Register
1.3.559USB_ARB_EP1_SR 704
Endpoint Status Register
1.3.560USB_ARB_RW1_WA 705
Endpoint Write Address value
1.3.561USB_ARB_RW1_WA_MSB 706
Endpoint Write Address value
1.3.562USB_ARB_RW1_RA 707
Endpoint Read Address value
1.3.563USB_ARB_RW1_RA_MSB 708
Endpoint Read Address value
1.3.564USB_ARB_RW1_DR 709

Endpoint Data Register
1.3.565USB_BUF_SIZE 710
Dedicated Endpoint Buffer Size Register
1.3.566USB_EP_ACTIVE 711
Endpoint Active Indication Register
1.3.567USB_EP_TYPE 712
Endpoint Type (IN/OUT) Indication
1.3.568USB_ARB_EP2_CFG 713
Endpoint Configuration Register
1.3.569USB_ARB_EP2_INT_EN 714
Endpoint Interrupt Enable Register
1.3.570USB_ARB_EP2_SR 715
Endpoint Status Register
1.3.571USB_ARB_RW2_WA 716
Endpoint Write Address value
1.3.572USB_ARB_RW2_WA_MSB 717
Endpoint Write Address value
1.3.573USB_ARB_RW2_RA 718
Endpoint Read Address value
1.3.574USB_ARB_RW2_RA_MSB 719
Endpoint Read Address value
1.3.575USB_ARB_RW2_DR 720
Endpoint Data Register
1.3.576USB_ARB_CFG 721
Arbiter Configuration Register
1.3.577USB_USB_CLK_EN 722
USB Block Clock Enable Register
1.3.578USB_ARB_INT_EN 723
Arbiter Interrupt Enable
1.3.579USB_ARB_INT_SR 724
Arbiter Interrupt Status
1.3.580USB_ARB_EP3_CFG 725
Endpoint Configuration Register
1.3.581USB_ARB_EP3_INT_EN 726
Endpoint Interrupt Enable Register
1.3.582USB_ARB_EP3_SR 727
Endpoint Status Register
1.3.583USB_ARB_RW3_WA 728
Endpoint Write Address value
1.3.584USB_ARB_RW3_WA_MSB 729
Endpoint Write Address value
1.3.585USB_ARB_RW3_RA 730
Endpoint Read Address value
1.3.586USB_ARB_RW3_RA_MSB 731
Endpoint Read Address value
1.3.587USB_ARB_RW3_DR 732
Endpoint Data Register
1.3.588USB_CWA 733
Common Area Write Address
1.3.589USB_CWA_MSB 734
Common Area Write Address
1.3.590USB_ARB_EP4_CFG 735
Endpoint Configuration Register
1.3.591USB_ARB_EP4_INT_EN 736

Endpoint Interrupt Enable Register
1.3.592USB_ARB_EP4_SR 737
Endpoint Status Register
1.3.593USB_ARB_RW4_WA 738
Endpoint Write Address value
1.3.594USB_ARB_RW4_WA_MSB 739
Endpoint Write Address value
1.3.595USB_ARB_RW4_RA 740
Endpoint Read Address value
1.3.596USB_ARB_RW4_RA_MSB 741
Endpoint Read Address value
1.3.597USB_ARB_RW4_DR 742
Endpoint Data Register
1.3.598USB_DMA_THRES 743
DMA Burst / Threshold Configuration
1.3.599USB_DMA_THRES_MSB 744
DMA Burst / Threshold Configuration
1.3.600USB_ARB_EP5_CFG 745
Endpoint Configuration Register
1.3.601USB_ARB_EP5_INT_EN 746
Endpoint Interrupt Enable Register
1.3.602USB_ARB_EP5_SR 747
Endpoint Status Register
1.3.603USB_ARB_RW5_WA 748
Endpoint Write Address value
1.3.604USB_ARB_RW5_WA_MSB 749
Endpoint Write Address value
1.3.605USB_ARB_RW5_RA 750
Endpoint Read Address value
1.3.606USB_ARB_RW5_RA_MSB 751
Endpoint Read Address value
1.3.607USB_ARB_RW5_DR 752
Endpoint Data Register
1.3.608USB_BUS_RST_CNT 753
Bus Reset Count Register
1.3.609USB_ARB_EP6_CFG 754
Endpoint Configuration Register
1.3.610USB_ARB_EP6_INT_EN 755
Endpoint Interrupt Enable Register
1.3.611USB_ARB_EP6_SR 756
Endpoint Status Register
1.3.612USB_ARB_RW6_WA 757
Endpoint Write Address value
1.3.613USB_ARB_RW6_WA_MSB 758
Endpoint Write Address value
1.3.614USB_ARB_RW6_RA 759
Endpoint Read Address value
1.3.615USB_ARB_RW6_RA_MSB 760
Endpoint Read Address value
1.3.616USB_ARB_RW6_DR 761
Endpoint Data Register
1.3.617USB_ARB_EP7_CFG 762
Endpoint Configuration Register
1.3.618USB_ARB_EP7_INT_EN 763

Endpoint Interrupt Enable Register
1.3.619USB_ARB_EP7_SR 764
Endpoint Status Register
1.3.620USB_ARB_RW7_WA 765
Endpoint Write Address value
1.3.621USB_ARB_RW7_WA_MSB 766
Endpoint Write Address value
1.3.622USB_ARB_RW7_RA 767
Endpoint Read Address value
1.3.623USB_ARB_RW7_RA_MSB 768
Endpoint Read Address value
1.3.624USB_ARB_RW7_DR 769
Endpoint Data Register
1.3.625USB_ARB_EP8_CFG 770
Endpoint Configuration Register
1.3.626USB_ARB_EP8_INT_EN 771
Endpoint Interrupt Enable Register
1.3.627USB_ARB_EP8_SR 772
Endpoint Status Register
1.3.628USB_ARB_RW8_WA 773
Endpoint Write Address value
1.3.629USB_ARB_RW8_WA_MSB 774
Endpoint Write Address value
1.3.630USB_ARB_RW8_RA 775
Endpoint Read Address value
1.3.631USB_ARB_RW8_RA_MSB 776
Endpoint Read Address value
1.3.632USB_ARB_RW8_DR 777
Endpoint Data Register
1.3.633B[0..3]_UDB00_A0 778
UDB00_A0
1.3.634B[0..3]_UDB01_A0 779
UDB01_A0
1.3.635B[0..3]_UDB02_A0 780
UDB02_A0
1.3.636B[0..3]_UDB03_A0 781
UDB03_A0
1.3.637B[0..3]_UDB04_A0 782
UDB04_A0
1.3.638B[0..3]_UDB05_A0 783
UDB05_A0
1.3.639B[0..3]_UDB06_A0 784
UDB06_A0
1.3.640B[0..3]_UDB07_A0 785
UDB07_A0
1.3.641B[0..3]_UDB08_A0 786
UDB08_A0
1.3.642B[0..3]_UDB09_A0 787
UDB09_A0
1.3.643B[0..3]_UDB10_A0 788
UDB10_A0
1.3.644B[0..3]_UDB11_A0 789
UDB11_A0
1.3.645B[0..3]_UDB12_A0 790

UDB12_A0
1.3.646B[0..3]_UDB13_A0 791
UDB13_A0
1.3.647B[0..3]_UDB14_A0 792
UDB14_A0
1.3.648B[0..3]_UDB15_A0 793
UDB15_A0
1.3.649B[0..3]_UDB00_A1 794
UDB00_A1
1.3.650B[0..3]_UDB01_A1 795
UDB01_A1
1.3.651B[0..3]_UDB02_A1 796
UDB02_A1
1.3.652B[0..3]_UDB03_A1 797
UDB03_A1
1.3.653B[0..3]_UDB04_A1 798
UDB04_A1
1.3.654B[0..3]_UDB05_A1 799
UDB05_A1
1.3.655B[0..3]_UDB06_A1 800
UDB06_A1
1.3.656B[0..3]_UDB07_A1 801
UDB07_A1
1.3.657B[0..3]_UDB08_A1 802
UDB08_A1
1.3.658B[0..3]_UDB09_A1 803
UDB09_A1
1.3.659B[0..3]_UDB10_A1 804
UDB10_A1
1.3.660B[0..3]_UDB11_A1 805
UDB11_A1
1.3.661B[0..3]_UDB12_A1 806
UDB12_A1
1.3.662B[0..3]_UDB13_A1 807
UDB13_A1
1.3.663B[0..3]_UDB14_A1 808
UDB14_A1
1.3.664B[0..3]_UDB15_A1 809
UDB15_A1
1.3.665B[0..3]_UDB00_D0 810
UDB00_D0
1.3.666B[0..3]_UDB01_D0 811
UDB01_D0
1.3.667B[0..3]_UDB02_D0 812
UDB02_D0
1.3.668B[0..3]_UDB03_D0 813
UDB03_D0
1.3.669B[0..3]_UDB04_D0 814
UDB04_D0
1.3.670B[0..3]_UDB05_D0 815
UDB05_D0
1.3.671B[0..3]_UDB06_D0 816
UDB06_D0
1.3.672B[0..3]_UDB07_D0 817

UDB07_D0
1.3.673B[0..3]_UDB08_D0 818
UDB08_D0
1.3.674B[0..3]_UDB09_D0 819
UDB09_D0
1.3.675B[0..3]_UDB10_D0 820
UDB10_D0
1.3.676B[0..3]_UDB11_D0 821
UDB11_D0
1.3.677B[0..3]_UDB12_D0 822
UDB12_D0
1.3.678B[0..3]_UDB13_D0 823
UDB13_D0
1.3.679B[0..3]_UDB14_D0 824
UDB14_D0
1.3.680B[0..3]_UDB15_D0 825
UDB15_D0
1.3.681B[0..3]_UDB00_D1 826
UDB00_D1
1.3.682B[0..3]_UDB01_D1 827
UDB01_D1
1.3.683B[0..3]_UDB02_D1 828
UDB02_D1
1.3.684B[0..3]_UDB03_D1 829
UDB03_D1
1.3.685B[0..3]_UDB04_D1 830
UDB04_D1
1.3.686B[0..3]_UDB05_D1 831
UDB05_D1
1.3.687B[0..3]_UDB06_D1 832
UDB06_D1
1.3.688B[0..3]_UDB07_D1 833
UDB07_D1
1.3.689B[0..3]_UDB08_D1 834
UDB08_D1
1.3.690B[0..3]_UDB09_D1 835
UDB09_D1
1.3.691B[0..3]_UDB10_D1 836
UDB10_D1
1.3.692B[0..3]_UDB11_D1 837
UDB11_D1
1.3.693B[0..3]_UDB12_D1 838
UDB12_D1
1.3.694B[0..3]_UDB13_D1 839
UDB13_D1
1.3.695B[0..3]_UDB14_D1 840
UDB14_D1
1.3.696B[0..3]_UDB15_D1 841
UDB15_D1
1.3.697B[0..3]_UDB00_F0 842
UDB00_F0
1.3.698B[0..3]_UDB01_F0 843
UDB01_F0
1.3.699B[0..3]_UDB02_F0 844

UDB02_F0
1.3.700B[0..3]_UDB03_F0 845
UDB03_F0
1.3.701B[0..3]_UDB04_F0 846
UDB04_F0
1.3.702B[0..3]_UDB05_F0 847
UDB05_F0
1.3.703B[0..3]_UDB06_F0 848
UDB06_F0
1.3.704B[0..3]_UDB07_F0 849
UDB07_F0
1.3.705B[0..3]_UDB08_F0 850
UDB08_F0
1.3.706B[0..3]_UDB09_F0 851
UDB09_F0
1.3.707B[0..3]_UDB10_F0 852
UDB10_F0
1.3.708B[0..3]_UDB11_F0 853
UDB11_F0
1.3.709B[0..3]_UDB12_F0 854
UDB12_F0
1.3.710B[0..3]_UDB13_F0 855
UDB13_F0
1.3.711B[0..3]_UDB14_F0 856
UDB14_F0
1.3.712B[0..3]_UDB15_F0 857
UDB15_F0
1.3.713B[0..3]_UDB00_F1 858
UDB00_F1
1.3.714B[0..3]_UDB01_F1 859
UDB01_F1
1.3.715B[0..3]_UDB02_F1 860
UDB02_F1
1.3.716B[0..3]_UDB03_F1 861
UDB03_F1
1.3.717B[0..3]_UDB04_F1 862
UDB04_F1
1.3.718B[0..3]_UDB05_F1 863
UDB05_F1
1.3.719B[0..3]_UDB06_F1 864
UDB06_F1
1.3.720B[0..3]_UDB07_F1 865
UDB07_F1
1.3.721B[0..3]_UDB08_F1 866
UDB08_F1
1.3.722B[0..3]_UDB09_F1 867
UDB09_F1
1.3.723B[0..3]_UDB10_F1 868
UDB10_F1
1.3.724B[0..3]_UDB11_F1 869
UDB11_F1
1.3.725B[0..3]_UDB12_F1 870
UDB12_F1
1.3.726B[0..3]_UDB13_F1 871

UDB13_F1
1.3.727B[0..3]_UDB14_F1 872
UDB14_F1
1.3.728B[0..3]_UDB15_F1 873
UDB15_F1
1.3.729B[0..3]_UDB00_ST 874
UDB00_ST
1.3.730B[0..3]_UDB01_ST 875
UDB01_ST
1.3.731B[0..3]_UDB02_ST 876
UDB02_ST
1.3.732B[0..3]_UDB03_ST 877
UDB03_ST
1.3.733B[0..3]_UDB04_ST 878
UDB04_ST
1.3.734B[0..3]_UDB05_ST 879
UDB05_ST
1.3.735B[0..3]_UDB06_ST 880
UDB06_ST
1.3.736B[0..3]_UDB07_ST 881
UDB07_ST
1.3.737B[0..3]_UDB08_ST 882
UDB08_ST
1.3.738B[0..3]_UDB09_ST 883
UDB09_ST
1.3.739B[0..3]_UDB10_ST 884
UDB10_ST
1.3.740B[0..3]_UDB11_ST 885
UDB11_ST
1.3.741B[0..3]_UDB12_ST 886
UDB12_ST
1.3.742B[0..3]_UDB13_ST 887
UDB13_ST
1.3.743B[0..3]_UDB14_ST 888
UDB14_ST
1.3.744B[0..3]_UDB15_ST 889
UDB15_ST
1.3.745B[0..3]_UDB00_CTL 890
UDB00_CTL
1.3.746B[0..3]_UDB01_CTL 891
UDB01_CTL
1.3.747B[0..3]_UDB02_CTL 892
UDB02_CTL
1.3.748B[0..3]_UDB03_CTL 893
UDB03_CTL
1.3.749B[0..3]_UDB04_CTL 894
UDB04_CTL
1.3.750B[0..3]_UDB05_CTL 895
UDB05_CTL
1.3.751B[0..3]_UDB06_CTL 896
UDB06_CTL
1.3.752B[0..3]_UDB07_CTL 897
UDB07_CTL
1.3.753B[0..3]_UDB08_CTL 898

UDB08_CTL
1.3.754B[0..3]_UDB09_CTL 899
UDB09_CTL
1.3.755B[0..3]_UDB10_CTL 900
UDB10_CTL
1.3.756B[0..3]_UDB11_CTL 901
UDB11_CTL
1.3.757B[0..3]_UDB12_CTL 902
UDB12_CTL
1.3.758B[0..3]_UDB13_CTL 903
UDB13_CTL
1.3.759B[0..3]_UDB14_CTL 904
UDB14_CTL
1.3.760B[0..3]_UDB15_CTL 905
UDB15_CTL
1.3.761B[0..3]_UDB00_MSK 906
UDB00_MSK
1.3.762B[0..3]_UDB01_MSK 907
UDB01_MSK
1.3.763B[0..3]_UDB02_MSK 908
UDB02_MSK
1.3.764B[0..3]_UDB03_MSK 909
UDB03_MSK
1.3.765B[0..3]_UDB04_MSK 910
UDB04_MSK
1.3.766B[0..3]_UDB05_MSK 911
UDB05_MSK
1.3.767B[0..3]_UDB06_MSK 912
UDB06_MSK
1.3.768B[0..3]_UDB07_MSK 913
UDB07_MSK
1.3.769B[0..3]_UDB08_MSK 914
UDB08_MSK
1.3.770B[0..3]_UDB09_MSK 915
UDB09_MSK
1.3.771B[0..3]_UDB10_MSK 916
UDB10_MSK
1.3.772B[0..3]_UDB11_MSK 917
UDB11_MSK
1.3.773B[0..3]_UDB12_MSK 918
UDB12_MSK
1.3.774B[0..3]_UDB13_MSK 919
UDB13_MSK
1.3.775B[0..3]_UDB14_MSK 920
UDB14_MSK
1.3.776B[0..3]_UDB15_MSK 921
UDB15_MSK
1.3.777B[0..3]_UDB00_ACTL 922
UDB00_ACTL
1.3.778B[0..3]_UDB01_ACTL 924
UDB01_ACTL
1.3.779B[0..3]_UDB02_ACTL 926
UDB02_ACTL
1.3.780B[0..3]_UDB03_ACTL 928

UDB03_ACTL
1.3.781B[0..3]_UDB04_ACTL 930
UDB04_ACTL
1.3.782B[0..3]_UDB05_ACTL 932
UDB05_ACTL
1.3.783B[0..3]_UDB06_ACTL 934
UDB06_ACTL
1.3.784B[0..3]_UDB07_ACTL 936
UDB07_ACTL
1.3.785B[0..3]_UDB08_ACTL 938
UDB08_ACTL
1.3.786B[0..3]_UDB09_ACTL 940
UDB09_ACTL
1.3.787B[0..3]_UDB10_ACTL 942
UDB10_ACTL
1.3.788B[0..3]_UDB11_ACTL 944
UDB11_ACTL
1.3.789B[0..3]_UDB12_ACTL 946
UDB12_ACTL
1.3.790B[0..3]_UDB13_ACTL 948
UDB13_ACTL
1.3.791B[0..3]_UDB14_ACTL 950
UDB14_ACTL
1.3.792B[0..3]_UDB15_ACTL 952
UDB15_ACTL
1.3.793B[0..3]_UDB00_MC 954
UDB00_MC
1.3.794B[0..3]_UDB01_MC 955
UDB01_MC
1.3.795B[0..3]_UDB02_MC 956
UDB02_MC
1.3.796B[0..3]_UDB03_MC 957
UDB03_MC
1.3.797B[0..3]_UDB04_MC 958
UDB04_MC
1.3.798B[0..3]_UDB05_MC 959
UDB05_MC
1.3.799B[0..3]_UDB06_MC 960
UDB06_MC
1.3.800B[0..3]_UDB07_MC 961
UDB07_MC
1.3.801B[0..3]_UDB08_MC 962
UDB08_MC
1.3.802B[0..3]_UDB09_MC 963
UDB09_MC
1.3.803B[0..3]_UDB10_MC 964
UDB10_MC
1.3.804B[0..3]_UDB11_MC 965
UDB11_MC
1.3.805B[0..3]_UDB12_MC 966
UDB12_MC
1.3.806B[0..3]_UDB13_MC 967
UDB13_MC
1.3.807B[0..3]_UDB14_MC 968

UDB14_MC
1.3.808B[0..3]_UDB15_MC 969
UDB15_MC
1.3.809B[0..3]_UDB00_01_A0 970
UDB00_01_A0
1.3.810B[0..3]_UDB01_02_A0 971
UDB01_02_A0
1.3.811B[0..3]_UDB02_03_A0 972
UDB02_03_A0
1.3.812B[0..3]_UDB03_04_A0 973
UDB03_04_A0
1.3.813B[0..3]_UDB04_05_A0 974
UDB04_05_A0
1.3.814B[0..3]_UDB05_06_A0 975
UDB05_06_A0
1.3.815B[0..3]_UDB06_07_A0 976
UDB06_07_A0
1.3.816B[0..3]_UDB07_08_A0 977
UDB07_08_A0
1.3.817B[0..3]_UDB08_09_A0 978
UDB08_09_A0
1.3.818B[0..3]_UDB09_10_A0 979
UDB09_10_A0
1.3.819B[0..3]_UDB10_11_A0 980
UDB10_11_A0
1.3.820B[0..3]_UDB11_12_A0 981
UDB11_12_A0
1.3.821B[0..3]_UDB12_13_A0 982
UDB12_13_A0
1.3.822B[0..3]_UDB13_14_A0 983
UDB13_14_A0
1.3.823B[0..3]_UDB14_15_A0 984
UDB14_15_A0
1.3.824B[0..3]_UDB00_01_A1 985
UDB00_01_A1
1.3.825B[0..3]_UDB01_02_A1 986
UDB01_02_A1
1.3.826B[0..3]_UDB02_03_A1 987
UDB02_03_A1
1.3.827B[0..3]_UDB03_04_A1 988
UDB03_04_A1
1.3.828B[0..3]_UDB04_05_A1 989
UDB04_05_A1
1.3.829B[0..3]_UDB05_06_A1 990
UDB05_06_A1
1.3.830B[0..3]_UDB06_07_A1 991
UDB06_07_A1
1.3.831B[0..3]_UDB07_08_A1 992
UDB07_08_A1
1.3.832B[0..3]_UDB08_09_A1 993
UDB08_09_A1
1.3.833B[0..3]_UDB09_10_A1 994
UDB09_10_A1
1.3.834B[0..3]_UDB10_11_A1 995

UDB10_11_A1
1.3.835B[0..3]_UDB11_12_A1 996
UDB11_12_A1
1.3.836B[0..3]_UDB12_13_A1 997
UDB12_13_A1
1.3.837B[0..3]_UDB13_14_A1 998
UDB13_14_A1
1.3.838B[0..3]_UDB14_15_A1 999
UDB14_15_A1
1.3.839B[0..3]_UDB00_01_D0 1000
UDB00_01_D0
1.3.840B[0..3]_UDB01_02_D0 1001
UDB01_02_D0
1.3.841B[0..3]_UDB02_03_D0 1002
UDB02_03_D0
1.3.842B[0..3]_UDB03_04_D0 1003
UDB03_04_D0
1.3.843B[0..3]_UDB04_05_D0 1004
UDB04_05_D0
1.3.844B[0..3]_UDB05_06_D0 1005
UDB05_06_D0
1.3.845B[0..3]_UDB06_07_D0 1006
UDB06_07_D0
1.3.846B[0..3]_UDB07_08_D0 1007
UDB07_08_D0
1.3.847B[0..3]_UDB08_09_D0 1008
UDB08_09_D0
1.3.848B[0..3]_UDB09_10_D0 1009
UDB09_10_D0
1.3.849B[0..3]_UDB10_11_D0 1010
UDB10_11_D0
1.3.850B[0..3]_UDB11_12_D0 1011
UDB11_12_D0
1.3.851B[0..3]_UDB12_13_D0 1012
UDB12_13_D0
1.3.852B[0..3]_UDB13_14_D0 1013
UDB13_14_D0
1.3.853B[0..3]_UDB14_15_D0 1014
UDB14_15_D0
1.3.854B[0..3]_UDB00_01_D1 1015
UDB00_01_D1
1.3.855B[0..3]_UDB01_02_D1 1016
UDB01_02_D1
1.3.856B[0..3]_UDB02_03_D1 1017
UDB02_03_D1
1.3.857B[0..3]_UDB03_04_D1 1018
UDB03_04_D1
1.3.858B[0..3]_UDB04_05_D1 1019
UDB04_05_D1
1.3.859B[0..3]_UDB05_06_D1 1020
UDB05_06_D1
1.3.860B[0..3]_UDB06_07_D1 1021
UDB06_07_D1
1.3.861B[0..3]_UDB07_08_D1 1022

UDB07_08_D1
1.3.862B[0..3]_UDB08_09_D1 1023
UDB08_09_D1
1.3.863B[0..3]_UDB09_10_D1 1024
UDB09_10_D1
1.3.864B[0..3]_UDB10_11_D1 1025
UDB10_11_D1
1.3.865B[0..3]_UDB11_12_D1 1026
UDB11_12_D1
1.3.866B[0..3]_UDB12_13_D1 1027
UDB12_13_D1
1.3.867B[0..3]_UDB13_14_D1 1028
UDB13_14_D1
1.3.868B[0..3]_UDB14_15_D1 1029
UDB14_15_D1
1.3.869B[0..3]_UDB00_01_F0 1030
UDB00_01_F0
1.3.870B[0..3]_UDB01_02_F0 1031
UDB01_02_F0
1.3.871B[0..3]_UDB02_03_F0 1032
UDB02_03_F0
1.3.872B[0..3]_UDB03_04_F0 1033
UDB03_04_F0
1.3.873B[0..3]_UDB04_05_F0 1034
UDB04_05_F0
1.3.874B[0..3]_UDB05_06_F0 1035
UDB05_06_F0
1.3.875B[0..3]_UDB06_07_F0 1036
UDB06_07_F0
1.3.876B[0..3]_UDB07_08_F0 1037
UDB07_08_F0
1.3.877B[0..3]_UDB08_09_F0 1038
UDB08_09_F0
1.3.878B[0..3]_UDB09_10_F0 1039
UDB09_10_F0
1.3.879B[0..3]_UDB10_11_F0 1040
UDB10_11_F0
1.3.880B[0..3]_UDB11_12_F0 1041
UDB11_12_F0
1.3.881B[0..3]_UDB12_13_F0 1042
UDB12_13_F0
1.3.882B[0..3]_UDB13_14_F0 1043
UDB13_14_F0
1.3.883B[0..3]_UDB14_15_F0 1044
UDB14_15_F0
1.3.884B[0..3]_UDB00_01_F1 1045
UDB00_01_F1
1.3.885B[0..3]_UDB01_02_F1 1046
UDB01_02_F1
1.3.886B[0..3]_UDB02_03_F1 1047
UDB02_03_F1
1.3.887B[0..3]_UDB03_04_F1 1048
UDB03_04_F1
1.3.888B[0..3]_UDB04_05_F1 1049

UDB04_05_F1
1.3.889B[0..3]_UDB05_06_F1 1050
UDB05_06_F1
1.3.890B[0..3]_UDB06_07_F1 1051
UDB06_07_F1
1.3.891B[0..3]_UDB07_08_F1 1052
UDB07_08_F1
1.3.892B[0..3]_UDB08_09_F1 1053
UDB08_09_F1
1.3.893B[0..3]_UDB09_10_F1 1054
UDB09_10_F1
1.3.894B[0..3]_UDB10_11_F1 1055
UDB10_11_F1
1.3.895B[0..3]_UDB11_12_F1 1056
UDB11_12_F1
1.3.896B[0..3]_UDB12_13_F1 1057
UDB12_13_F1
1.3.897B[0..3]_UDB13_14_F1 1058
UDB13_14_F1
1.3.898B[0..3]_UDB14_15_F1 1059
UDB14_15_F1
1.3.899B[0..3]_UDB00_01_ST 1060
UDB00_01_ST
1.3.900B[0..3]_UDB01_02_ST 1061
UDB01_02_ST
1.3.901B[0..3]_UDB02_03_ST 1062
UDB02_03_ST
1.3.902B[0..3]_UDB03_04_ST 1063
UDB03_04_ST
1.3.903B[0..3]_UDB04_05_ST 1064
UDB04_05_ST
1.3.904B[0..3]_UDB05_06_ST 1065
UDB05_06_ST
1.3.905B[0..3]_UDB06_07_ST 1066
UDB06_07_ST
1.3.906B[0..3]_UDB07_08_ST 1067
UDB07_08_ST
1.3.907B[0..3]_UDB08_09_ST 1068
UDB08_09_ST
1.3.908B[0..3]_UDB09_10_ST 1069
UDB09_10_ST
1.3.909B[0..3]_UDB10_11_ST 1070
UDB10_11_ST
1.3.910B[0..3]_UDB11_12_ST 1071
UDB11_12_ST
1.3.911B[0..3]_UDB12_13_ST 1072
UDB12_13_ST
1.3.912B[0..3]_UDB13_14_ST 1073
UDB13_14_ST
1.3.913B[0..3]_UDB14_15_ST 1074
UDB14_15_ST
1.3.914B[0..3]_UDB00_01_CTL 1075
UDB00_01_CTL
1.3.915B[0..3]_UDB01_02_CTL 1076

UDB01_02_CTL
1.3.916B[0..3]_UDB02_03_CTL 1077
UDB02_03_CTL
1.3.917B[0..3]_UDB03_04_CTL 1078
UDB03_04_CTL
1.3.918B[0..3]_UDB04_05_CTL 1079
UDB04_05_CTL
1.3.919B[0..3]_UDB05_06_CTL 1080
UDB05_06_CTL
1.3.920B[0..3]_UDB06_07_CTL 1081
UDB06_07_CTL
1.3.921B[0..3]_UDB07_08_CTL 1082
UDB07_08_CTL
1.3.922B[0..3]_UDB08_09_CTL 1083
UDB08_09_CTL
1.3.923B[0..3]_UDB09_10_CTL 1084
UDB09_10_CTL
1.3.924B[0..3]_UDB10_11_CTL 1085
UDB10_11_CTL
1.3.925B[0..3]_UDB11_12_CTL 1086
UDB11_12_CTL
1.3.926B[0..3]_UDB12_13_CTL 1087
UDB12_13_CTL
1.3.927B[0..3]_UDB13_14_CTL 1088
UDB13_14_CTL
1.3.928B[0..3]_UDB14_15_CTL 1089
UDB14_15_CTL
1.3.929B[0..3]_UDB00_01_MSK 1090
UDB00_01_MSK
1.3.930B[0..3]_UDB01_02_MSK 1091
UDB01_02_MSK
1.3.931B[0..3]_UDB02_03_MSK 1092
UDB02_03_MSK
1.3.932B[0..3]_UDB03_04_MSK 1093
UDB03_04_MSK
1.3.933B[0..3]_UDB04_05_MSK 1094
UDB04_05_MSK
1.3.934B[0..3]_UDB05_06_MSK 1095
UDB05_06_MSK
1.3.935B[0..3]_UDB06_07_MSK 1096
UDB06_07_MSK
1.3.936B[0..3]_UDB07_08_MSK 1097
UDB07_08_MSK
1.3.937B[0..3]_UDB08_09_MSK 1098
UDB08_09_MSK
1.3.938B[0..3]_UDB09_10_MSK 1099
UDB09_10_MSK
1.3.939B[0..3]_UDB10_11_MSK 1100
UDB10_11_MSK
1.3.940B[0..3]_UDB11_12_MSK 1101
UDB11_12_MSK
1.3.941B[0..3]_UDB12_13_MSK 1102
UDB12_13_MSK
1.3.942B[0..3]_UDB13_14_MSK 1103

UDB13_14_MSK
1.3.943B[0..3]_UDB14_15_MSK 1104
UDB14_15_MSK
1.3.944B[0..3]_UDB00_01_ACTL 1105
UDB00_01_ACTL
1.3.945B[0..3]_UDB01_02_ACTL 1107
UDB01_02_ACTL
1.3.946B[0..3]_UDB02_03_ACTL 1109
UDB02_03_ACTL
1.3.947B[0..3]_UDB03_04_ACTL 1111
UDB03_04_ACTL
1.3.948B[0..3]_UDB04_05_ACTL 1113
UDB04_05_ACTL
1.3.949B[0..3]_UDB05_06_ACTL 1115
UDB05_06_ACTL
1.3.950B[0..3]_UDB06_07_ACTL 1117
UDB06_07_ACTL
1.3.951B[0..3]_UDB07_08_ACTL 1119
UDB07_08_ACTL
1.3.952B[0..3]_UDB08_09_ACTL 1121
UDB08_09_ACTL
1.3.953B[0..3]_UDB09_10_ACTL 1123
UDB09_10_ACTL
1.3.954B[0..3]_UDB10_11_ACTL 1125
UDB10_11_ACTL
1.3.955B[0..3]_UDB11_12_ACTL 1127
UDB11_12_ACTL
1.3.956B[0..3]_UDB12_13_ACTL 1129
UDB12_13_ACTL
1.3.957B[0..3]_UDB13_14_ACTL 1131
UDB13_14_ACTL
1.3.958B[0..3]_UDB14_15_ACTL 1133
UDB14_15_ACTL
1.3.959B[0..3]_UDB00_01_MC 1135
UDB00_01_MC
1.3.960B[0..3]_UDB01_02_MC 1136
UDB01_02_MC
1.3.961B[0..3]_UDB02_03_MC 1137
UDB02_03_MC
1.3.962B[0..3]_UDB03_04_MC 1138
UDB03_04_MC
1.3.963B[0..3]_UDB04_05_MC 1139
UDB04_05_MC
1.3.964B[0..3]_UDB05_06_MC 1140
UDB05_06_MC
1.3.965B[0..3]_UDB06_07_MC 1141
UDB06_07_MC
1.3.966B[0..3]_UDB07_08_MC 1142
UDB07_08_MC
1.3.967B[0..3]_UDB08_09_MC 1143
UDB08_09_MC
1.3.968B[0..3]_UDB09_10_MC 1144
UDB09_10_MC
1.3.969B[0..3]_UDB10_11_MC 1145

UDB10_11_MC
1.3.970B[0..3]_UDB11_12_MC 1146
UDB11_12_MC
1.3.971B[0..3]_UDB12_13_MC 1147
UDB12_13_MC
1.3.972B[0..3]_UDB13_14_MC 1148
UDB13_14_MC
1.3.973B[0..3]_UDB14_15_MC 1149
UDB14_15_MC
1.3.974B[0..3]_UDB00_A0_A1 1150
UDB00_A0_A1
1.3.975B[0..3]_UDB01_A0_A1 1151
UDB01_A0_A1
1.3.976B[0..3]_UDB02_A0_A1 1152
UDB02_A0_A1
1.3.977B[0..3]_UDB03_A0_A1 1153
UDB03_A0_A1
1.3.978B[0..3]_UDB04_A0_A1 1154
UDB04_A0_A1
1.3.979B[0..3]_UDB05_A0_A1 1155
UDB05_A0_A1
1.3.980B[0..3]_UDB06_A0_A1 1156
UDB06_A0_A1
1.3.981B[0..3]_UDB07_A0_A1 1157
UDB07_A0_A1
1.3.982B[0..3]_UDB08_A0_A1 1158
UDB08_A0_A1
1.3.983B[0..3]_UDB09_A0_A1 1159
UDB09_A0_A1
1.3.984B[0..3]_UDB10_A0_A1 1160
UDB10_A0_A1
1.3.985B[0..3]_UDB11_A0_A1 1161
UDB11_A0_A1
1.3.986B[0..3]_UDB12_A0_A1 1162
UDB12_A0_A1
1.3.987B[0..3]_UDB13_A0_A1 1163
UDB13_A0_A1
1.3.988B[0..3]_UDB14_A0_A1 1164
UDB14_A0_A1
1.3.989B[0..3]_UDB15_A0_A1 1165
UDB15_A0_A1
1.3.990B[0..3]_UDB00_D0_D1 1166
UDB00_D0_D1
1.3.991B[0..3]_UDB01_D0_D1 1167
UDB01_D0_D1
1.3.992B[0..3]_UDB02_D0_D1 1168
UDB02_D0_D1
1.3.993B[0..3]_UDB03_D0_D1 1169
UDB03_D0_D1
1.3.994B[0..3]_UDB04_D0_D1 1170
UDB04_D0_D1
1.3.995B[0..3]_UDB05_D0_D1 1171
UDB05_D0_D1
1.3.996B[0..3]_UDB06_D0_D1 1172

UDB06_D0_D1
1.3.997B[0..3]_UDB07_D0_D1 1173
UDB07_D0_D1
1.3.998B[0..3]_UDB08_D0_D1 1174
UDB08_D0_D1
1.3.999B[0..3]_UDB09_D0_D1 1175
UDB09_D0_D1
1.3.1000B[0..3]_UDB10_D0_D1 1176
UDB10_D0_D1
1.3.1001B[0..3]_UDB11_D0_D1 1177
UDB11_D0_D1
1.3.1002B[0..3]_UDB12_D0_D1 1178
UDB12_D0_D1
1.3.1003B[0..3]_UDB13_D0_D1 1179
UDB13_D0_D1
1.3.1004B[0..3]_UDB14_D0_D1 1180
UDB14_D0_D1
1.3.1005B[0..3]_UDB15_D0_D1 1181
UDB15_D0_D1
1.3.1006B[0..3]_UDB00_F0_F1 1182
UDB00_F0_F1
1.3.1007B[0..3]_UDB01_F0_F1 1183
UDB01_F0_F1
1.3.1008B[0..3]_UDB02_F0_F1 1184
UDB02_F0_F1
1.3.1009B[0..3]_UDB03_F0_F1 1185
UDB03_F0_F1
1.3.1010B[0..3]_UDB04_F0_F1 1186
UDB04_F0_F1
1.3.1011B[0..3]_UDB05_F0_F1 1187
UDB05_F0_F1
1.3.1012B[0..3]_UDB06_F0_F1 1188
UDB06_F0_F1
1.3.1013B[0..3]_UDB07_F0_F1 1189
UDB07_F0_F1
1.3.1014B[0..3]_UDB08_F0_F1 1190
UDB08_F0_F1
1.3.1015B[0..3]_UDB09_F0_F1 1191
UDB09_F0_F1
1.3.1016B[0..3]_UDB10_F0_F1 1192
UDB10_F0_F1
1.3.1017B[0..3]_UDB11_F0_F1 1193
UDB11_F0_F1
1.3.1018B[0..3]_UDB12_F0_F1 1194
UDB12_F0_F1
1.3.1019B[0..3]_UDB13_F0_F1 1195
UDB13_F0_F1
1.3.1020B[0..3]_UDB14_F0_F1 1196
UDB14_F0_F1
1.3.1021B[0..3]_UDB15_F0_F1 1197
UDB15_F0_F1
1.3.1022B[0..3]_UDB00_ST_CTL 1198
UDB00_ST_CTL
1.3.1023B[0..3]_UDB01_ST_CTL 1199

UDB01_ST_CTL
1.3.1024B[0..3]_UDB02_ST_CTL 1200
UDB02_ST_CTL
1.3.1025B[0..3]_UDB03_ST_CTL 1201
UDB03_ST_CTL
1.3.1026B[0..3]_UDB04_ST_CTL 1202
UDB04_ST_CTL
1.3.1027B[0..3]_UDB05_ST_CTL 1203
UDB05_ST_CTL
1.3.1028B[0..3]_UDB06_ST_CTL 1204
UDB06_ST_CTL
1.3.1029B[0..3]_UDB07_ST_CTL 1205
UDB07_ST_CTL
1.3.1030B[0..3]_UDB08_ST_CTL 1206
UDB08_ST_CTL
1.3.1031B[0..3]_UDB09_ST_CTL 1207
UDB09_ST_CTL
1.3.1032B[0..3]_UDB10_ST_CTL 1208
UDB10_ST_CTL
1.3.1033B[0..3]_UDB11_ST_CTL 1209
UDB11_ST_CTL
1.3.1034B[0..3]_UDB12_ST_CTL 1210
UDB12_ST_CTL
1.3.1035B[0..3]_UDB13_ST_CTL 1211
UDB13_ST_CTL
1.3.1036B[0..3]_UDB14_ST_CTL 1212
UDB14_ST_CTL
1.3.1037B[0..3]_UDB15_ST_CTL 1213
UDB15_ST_CTL
1.3.1038B[0..3]_UDB00_MSK_ACTL 1214
UDB00_MSK_ACTL
1.3.1039B[0..3]_UDB01_MSK_ACTL 1216
UDB01_MSK_ACTL
1.3.1040B[0..3]_UDB02_MSK_ACTL 1218
UDB02_MSK_ACTL
1.3.1041B[0..3]_UDB03_MSK_ACTL 1220
UDB03_MSK_ACTL
1.3.1042B[0..3]_UDB04_MSK_ACTL 1222
UDB04_MSK_ACTL
1.3.1043B[0..3]_UDB05_MSK_ACTL 1224
UDB05_MSK_ACTL
1.3.1044B[0..3]_UDB06_MSK_ACTL 1226
UDB06_MSK_ACTL
1.3.1045B[0..3]_UDB07_MSK_ACTL 1228
UDB07_MSK_ACTL
1.3.1046B[0..3]_UDB08_MSK_ACTL 1230
UDB08_MSK_ACTL
1.3.1047B[0..3]_UDB09_MSK_ACTL 1232
UDB09_MSK_ACTL
1.3.1048B[0..3]_UDB10_MSK_ACTL 1234
UDB10_MSK_ACTL
1.3.1049B[0..3]_UDB11_MSK_ACTL 1236
UDB11_MSK_ACTL
1.3.1050B[0..3]_UDB12_MSK_ACTL 1238

UDB12_MSK_ACTL
1.3.1051B[0..3]_UDB13_MSK_ACTL 1240
UDB13_MSK_ACTL
1.3.1052B[0..3]_UDB14_MSK_ACTL 1242
UDB14_MSK_ACTL
1.3.1053B[0..3]_UDB15_MSK_ACTL 1244
UDB15_MSK_ACTL
1.3.1054B[0..3]_UDB00_MC_00 1246
UDB00_MC_00
1.3.1055B[0..3]_UDB01_MC_00 1247
UDB01_MC_00
1.3.1056B[0..3]_UDB02_MC_00 1248
UDB02_MC_00
1.3.1057B[0..3]_UDB03_MC_00 1249
UDB03_MC_00
1.3.1058B[0..3]_UDB04_MC_00 1250
UDB04_MC_00
1.3.1059B[0..3]_UDB05_MC_00 1251
UDB05_MC_00
1.3.1060B[0..3]_UDB06_MC_00 1252
UDB06_MC_00
1.3.1061B[0..3]_UDB07_MC_00 1253
UDB07_MC_00
1.3.1062B[0..3]_UDB08_MC_00 1254
UDB08_MC_00
1.3.1063B[0..3]_UDB09_MC_00 1255
UDB09_MC_00
1.3.1064B[0..3]_UDB10_MC_00 1256
UDB10_MC_00
1.3.1065B[0..3]_UDB11_MC_00 1257
UDB11_MC_00
1.3.1066B[0..3]_UDB12_MC_00 1258
UDB12_MC_00
1.3.1067B[0..3]_UDB13_MC_00 1259
UDB13_MC_00
1.3.1068B[0..3]_UDB14_MC_00 1260
UDB14_MC_00
1.3.1069B[0..3]_UDB15_MC_00 1261
UDB15_MC_00
1.3.1070PHUB_CFG 1262
PHUB Configuration
1.3.1071PHUB_ERR 1264
PHUB Error Detection
1.3.1072PHUB_ERR_ADR 1265
PHUB Error Address
1.3.1073PHUB_CH[0..23]_BASIC_CFG 1266
Channel Basic Configuration Register
1.3.1074PHUB_CH[0..23]_ACTION 1268
Channel Action
1.3.1075PHUB_CH[0..23]_BASIC_STATUS 1270
Channel Basic Status Register
1.3.1076PHUB_CFGMEM[0..23]_CFG0 1273
PHUB Channel Configuration Register 0
1.3.1077PHUB_CFGMEM[0..23]_CFG1 1275

PHUB Channel Configuration Register 1
1.3.1078PHUB_TDMEM[0..127]_ORIG_TD0 1277
PHUB Original Transaction Descriptor 0
1.3.1079PHUB_TDMEM[0..127]_ORIG_TD1 1283
PHUB Original Transaction Descriptor 0
1.3.1080CAN[0..0]_CSR_INT_SR 1288
INT_SR
1.3.1081CAN[0..0]_CSR_INT_EN 1290
INT_EN
1.3.1082CAN[0..0]_CSR_BUF_SR 1292
BUF_SR
1.3.1083CAN[0..0]_CSR_ERR_SR 1294
ERR_SR
1.3.1084CAN[0..0]_CSR_CMD 1295
CMD
1.3.1085CAN[0..0]_CSR_CFG 1296
CFG
1.3.1086CAN[0..0]_TX[0..7]_CMD 1298
TXCMD
1.3.1087CAN[0..0]_TX[0..7]_ID 1300
TXID
1.3.1088CAN[0..0]_TX[0..7]_DH 1301
TXDH
1.3.1089CAN[0..0]_TX[0..7]_DL 1302
TXDL
1.3.1090CAN[0..0]_RX[0..15]_CMD 1303
RXCMD
1.3.1091CAN[0..0]_RX[0..15]_ID 1305
RXID
1.3.1092CAN[0..0]_RX[0..15]_DH 1306
RXDH
1.3.1093CAN[0..0]_RX[0..15]_DL 1307
RXDL
1.3.1094CAN[0..0]_RX[0..15]_AMR 1308
RXAMR
1.3.1095CAN[0..0]_RX[0..15]_ACR 1309
RXACR
1.3.1096CAN[0..0]_RX[0..15]_AMRD 1310
RXAMRD
1.3.1097CAN[0..0]_RX[0..15]_ACRD 1311
RXACRD
1.3.1098DFB[0..0]_DPA_SRAM_DATA[0..127] 1312
Data RAM A
1.3.1099DFB[0..0]_DPB_SRAM_DATA[0..127] 1313
DFB Data RAM B
1.3.1100DFB[0..0]_CSA_SRAM_DATA[0..63] 1314
DFB Control Store A
1.3.1101DFB[0..0]_CSB_SRAM_DATA[0..63] 1315
DFB Control Store B
1.3.1102DFB[0..0]_FSM_SRAM_DATA[0..63] 1316
DFB Code Store B
1.3.1103DFB[0..0]_ACU_SRAM_DATA[0..15] 1317
DFB Address Store
1.3.1104DFB[0..0]_CR 1318

DFB Command Register
1.3.1105DFB[0..0]_SR 1319
DFB Status Register
1.3.1106DFB[0..0]_RAM_EN 1321
DFB RAM Enable Register
1.3.1107DFB[0..0]_RAM_DIR 1323
DFB RAM Direction Register
1.3.1108DFB[0..0]_SEMA 1324
DFB Semaphore Register
1.3.1109DFB[0..0]_DSI_CTRL 1325
DFB Global Control Register
1.3.1110DFB[0..0]_INT_CTRL 1326
DFB Interrupt Control Register
1.3.1111DFB[0..0]_DMA_CTRL 1327
DFB DMAREQ Control Register
1.3.1112DFB[0..0]_STAGEA 1328
DFB Low Byte Staging Register A
1.3.1113DFB[0..0]_STAGEAM 1329
DFB Middle Byte Staging Register A
1.3.1114DFB[0..0]_STAGEAH 1330
DFB High Byte Staging Register A
1.3.1115DFB[0..0]_STAGEB 1331
DFB Low Byte Staging Register B
1.3.1116DFB[0..0]_STAGEBM 1332
DFB Middle Byte Staging Register B
1.3.1117DFB[0..0]_STAGEBH 1333
DFB High Byte Staging Register B
1.3.1118DFB[0..0]_HOLDA 1334
DFB Low Byte Holding Register A
1.3.1119DFB[0..0]_HOLDAM 1335
DFB Middle Byte Holding Register A
1.3.1120DFB[0..0]_HOLDAH 1336
DFB High Byte Holding Register A
1.3.1121DFB[0..0]_HOLDAS 1337
DFB Holding Register A Sign Extension
1.3.1122DFB[0..0]_HOLDB 1338
DFB Low Byte Holding Register B
1.3.1123DFB[0..0]_HOLDBM 1339
DFB Middle Byte Holding Register B
1.3.1124DFB[0..0]_HOLDBH 1340
DFB High Byte Holding Register B
1.3.1125DFB[0..0]_HOLDBS 1341
DFB Holding Register B Sign Extension
1.3.1126DFB[0..0]_COHER 1342
DFB Coherency Register
1.3.1127DFB[0..0]_DALIGN 1343
DFB Data Alignment Register
1.3.1128B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] 1344
PLD_IT
1.3.1129B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3] 1354
PLD_ORT
1.3.1130B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST 1358
MC_CFG_CEN_CONST
1.3.1131B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB 1361

MC_CFG_XORFB
1.3.1132B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET 1363
MC_CFG_SET_RESET
1.3.1133B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS 1366
MC_CFG_BYPASS
1.3.1134B[0..3]_P[0..7]_U[0..1]_CFG0 1368
CFG0
1.3.1135B[0..3]_P[0..7]_U[0..1]_CFG1 1369
CFG1
1.3.1136B[0..3]_P[0..7]_U[0..1]_CFG2 1370
CFG2
1.3.1137B[0..3]_P[0..7]_U[0..1]_CFG3 1371
CFG3
1.3.1138B[0..3]_P[0..7]_U[0..1]_CFG4 1372
CFG4
1.3.1139B[0..3]_P[0..7]_U[0..1]_CFG5 1373
CFG5
1.3.1140B[0..3]_P[0..7]_U[0..1]_CFG6 1375
CFG6
1.3.1141B[0..3]_P[0..7]_U[0..1]_CFG7 1377
CFG7
1.3.1142B[0..3]_P[0..7]_U[0..1]_CFG8 1379
CFG8
1.3.1143B[0..3]_P[0..7]_U[0..1]_CFG9 1380
CFG9
1.3.1144B[0..3]_P[0..7]_U[0..1]_CFG10 1381
CFG10
1.3.1145B[0..3]_P[0..7]_U[0..1]_CFG11 1382
CFG11
1.3.1146B[0..3]_P[0..7]_U[0..1]_CFG12 1383
CFG12
1.3.1147B[0..3]_P[0..7]_U[0..1]_CFG13 1385
CFG13
1.3.1148B[0..3]_P[0..7]_U[0..1]_CFG14 1387
CFG14
1.3.1149B[0..3]_P[0..7]_U[0..1]_CFG15 1389
CFG15
1.3.1150B[0..3]_P[0..7]_U[0..1]_CFG16 1391
CFG16
1.3.1151B[0..3]_P[0..7]_U[0..1]_CFG20 1393
CFG20
1.3.1152B[0..3]_P[0..7]_U[0..1]_CFG21 1394
CFG21
1.3.1153B[0..3]_P[0..7]_U[0..1]_CFG22 1395
CFG22
1.3.1154B[0..3]_P[0..7]_U[0..1]_CFG23 1397
CFG23
1.3.1155B[0..3]_P[0..7]_U[0..1]_CFG24 1399
CFG24
1.3.1156B[0..3]_P[0..7]_U[0..1]_CFG25 1401
CFG25
1.3.1157B[0..3]_P[0..7]_U[0..1]_CFG26 1403
CFG26
1.3.1158B[0..3]_P[0..7]_U[0..1]_CFG27 1405

CFG27
1.3.1159B[0..3]_P[0..7]_U[0..1]_CFG28 1407
CFG28
1.3.1160B[0..3]_P[0..7]_U[0..1]_CFG29 1408
CFG29
1.3.1161B[0..3]_P[0..7]_U[0..1]_CFG30 1409
CFG30
1.3.1162B[0..3]_P[0..7]_U[0..1]_CFG31 1411
CFG31
1.3.1163B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] 1412
DCFG
1.3.1164B[0..3]_P[0..7]_ROUTE_HC[0..127] 1417
HC
1.3.1165B[0..3]_P[0..7]_ROUTE_HV_L[0..15] 1439
HV_L
1.3.1166B[0..3]_P[0..7]_ROUTE_HS[0..23] 1445
HS
1.3.1167B[0..3]_P[0..7]_ROUTE_HV_R[0..15] 1450
HV_R
1.3.1168B[0..3]_P[0..7]_ROUTE_PLD0IN0 1456
PLD0IN0
1.3.1169B[0..3]_P[0..7]_ROUTE_PLD0IN1 1457
PLD0IN1
1.3.1170B[0..3]_P[0..7]_ROUTE_PLD0IN2 1458
PLD0IN2
1.3.1171B[0..3]_P[0..7]_ROUTE_PLD1IN0 1459
PLD1IN0
1.3.1172B[0..3]_P[0..7]_ROUTE_PLD1IN1 1460
PLD1IN1
1.3.1173B[0..3]_P[0..7]_ROUTE_PLD1IN2 1461
PLD1IN2
1.3.1174B[0..3]_P[0..7]_ROUTE_DPIN0 1462
DPIN0
1.3.1175B[0..3]_P[0..7]_ROUTE_DPIN1 1463
DPIN1
1.3.1176B[0..3]_P[0..7]_ROUTE_SCIN 1464
SCIN
1.3.1177B[0..3]_P[0..7]_ROUTE_SCIOIN 1465
SCIOIN
1.3.1178B[0..3]_P[0..7]_ROUTE_RCIN 1466
RCIN
1.3.1179B[0..3]_P[0..7]_ROUTE_VS0 1467
VS0
1.3.1180B[0..3]_P[0..7]_ROUTE_VS1 1468
VS1
1.3.1181B[0..3]_P[0..7]_ROUTE_VS2 1469
VS2
1.3.1182B[0..3]_P[0..7]_ROUTE_VS3 1470
VS3
1.3.1183B[0..3]_P[0..7]_ROUTE_VS4 1471
VS4
1.3.1184B[0..3]_P[0..7]_ROUTE_VS5 1472
VS5
1.3.1185B[0..3]_P[0..7]_ROUTE_VS6 1473

VS6
1.3.1186B[0..3]_P[0..7]_ROUTE_VS7 1474
VS7
1.3.1187DSI[0..15]_HC[0..127] 1475
HC
1.3.1188DSI[0..15]_HV_L[0..15] 1497
HV_L
1.3.1189DSI[0..15]_HS[0..23] 1500
HS
1.3.1190DSI[0..15]_HV_R[0..15] 1505
HV_R
1.3.1191DSI[0..15]_DSIINP0 1508
DSIINP0
1.3.1192DSI[0..15]_DSIINP1 1509
DSIINP1
1.3.1193DSI[0..15]_DSIINP2 1510
DSIINP2
1.3.1194DSI[0..15]_DSIINP3 1511
DSIINP3
1.3.1195DSI[0..15]_DSIINP4 1512
DSIINP4
1.3.1196DSI[0..15]_DSIINP5 1513
DSIINP5
1.3.1197DSI[0..15]_DSIOUTP0 1514
DSIOUTP0
1.3.1198DSI[0..15]_DSIOUTP1 1515
DSIOUTP1
1.3.1199DSI[0..15]_DSIOUTP2 1516
DSIOUTP2
1.3.1200DSI[0..15]_DSIOUTP3 1517
DSIOUTP3
1.3.1201DSI[0..15]_DSIOUTT0 1518
DSIOUTT0
1.3.1202DSI[0..15]_DSIOUTT1 1519
DSIOUTT1
1.3.1203DSI[0..15]_DSIOUTT2 1520
DSIOUTT2
1.3.1204DSI[0..15]_DSIOUTT3 1521
DSIOUTT3
1.3.1205DSI[0..15]_DSIOUTT4 1522
DSIOUTT4
1.3.1206DSI[0..15]_DSIOUTT5 1523
DSIOUTT5
1.3.1207DSI[0..15]_VS0 1524
VS0
1.3.1208DSI[0..15]_VS1 1525
VS1
1.3.1209DSI[0..15]_VS2 1526
VS2
1.3.1210DSI[0..15]_VS3 1527
VS3
1.3.1211DSI[0..15]_VS4 1528
VS4
1.3.1212DSI[0..15]_VS5 1529

VS5
1.3.1213DSI[0..15]_VS6 1530
VS6
1.3.1214DSI[0..15]_VS7 1531
VS7
1.3.1215BCTL[0..3]_MDCLK_EN 1532
DCLK_EN
1.3.1216BCTL[0..3]_MBCLK_EN 1533
BCLK_EN
1.3.1217BCTL[0..3]_WAIT_CFG 1534
WAIT_CFG
1.3.1218BCTL[0..3]_BANK_CTL 1536
BANK_CTL
1.3.1219BCTL[0..3]_DCLK_EN0 1538
DCLK_EN
1.3.1220BCTL[0..3]_BCLK_EN0 1539
BCLK_EN
1.3.1221BCTL[0..3]_DCLK_EN1 1541
DCLK_EN
1.3.1222BCTL[0..3]_BCLK_EN1 1542
BCLK_EN
1.3.1223BCTL[0..3]_DCLK_EN2 1544
DCLK_EN
1.3.1224BCTL[0..3]_BCLK_EN2 1545
BCLK_EN
1.3.1225BCTL[0..3]_DCLK_EN3 1547
DCLK_EN
1.3.1226BCTL[0..3]_BCLK_EN3 1548
BCLK_EN
1.3.1227IDMUX_IRQ_CTL[0..7] 1550
Control Register IRQ_CTL
1.3.1228IDMUX_DRQ_CTL[0..5] 1551
Configuration Register DRQ_CTL
1.3.1229P3BA_Y_START 1552
Y_START
1.3.1230P3BA_YROLL 1553
YROLL
1.3.1231P3BA_YCFG 1554
YCFG
1.3.1232P3BA_X_START1 1555
X_START1
1.3.1233P3BA_X_START2 1556
X_START2
1.3.1234P3BA_XROLL1 1557
XROLL1
1.3.1235P3BA_XROLL2 1558
XROLL2
1.3.1236P3BA_XINC 1559
XINC
1.3.1237P3BA_XCFG 1560
XCFG
1.3.1238P3BA_OFFSETADDR1 1561
OFFSETADDR1
1.3.1239P3BA_OFFSETADDR2 1562

OFFSETADDR2
1.3.1240P3BA_OFFSETADDR3 1563
OFFSETADDR3
1.3.1241P3BA_ABSADDR1 1564
ABSADDR1
1.3.1242P3BA_ABSADDR2 1565
ABSADDR2
1.3.1243P3BA_ABSADDR3 1566
ABSADDR3
1.3.1244P3BA_ABSADDR4 1567
ABSADDR4
1.3.1245P3BA_DATCFG1 1568
DATCFG1
1.3.1246P3BA_DATCFG2 1569
DATCFG2
1.3.1247P3BA_CMP_RSLT1 1570
CMP_RSLT1
1.3.1248P3BA_CMP_RSLT2 1571
CMP_RSLT2
1.3.1249P3BA_CMP_RSLT3 1572
CMP_RSLT3
1.3.1250P3BA_CMP_RSLT4 1573
CMP_RSLT4
1.3.1251P3BA_DATA_REG1 1574
DATA_REG1
1.3.1252P3BA_DATA_REG2 1575
DATA_REG2
1.3.1253P3BA_DATA_REG3 1576
DATA_REG3
1.3.1254P3BA_DATA_REG4 1577
DATA_REG4
1.3.1255P3BA_EXP_DATA1 1578
EXP_DATA1
1.3.1256P3BA_EXP_DATA2 1579
EXP_DATA2
1.3.1257P3BA_EXP_DATA3 1580
EXP_DATA3
1.3.1258P3BA_EXP_DATA4 1581
EXP_DATA4
1.3.1259P3BA_MSTR_HRDATA1 1582
MSTR_HRDATA1
1.3.1260P3BA_MSTR_HRDATA2 1583
MSTR_HRDATA2
1.3.1261P3BA_MSTR_HRDATA3 1584
MSTR_HRDATA3
1.3.1262P3BA_MSTR_HRDATA4 1585
MSTR_HRDATA4
1.3.1263P3BA_BIST_EN 1586
BIST_EN
1.3.1264P3BA_PHUB_MASTER_SSR 1587
PHUB_MASTER_SSR
1.3.1265P3BA_SEQCFG1 1588
SEQCFG1
1.3.1266P3BA_SEQCFG2 1589

SEQCFG2
1.3.1267P3BA_Y_CURR 1590
Y_CURR
1.3.1268P3BA_X_CURR1 1591
X_CURR1
1.3.1269P3BA_X_CURR2 1592
X_CURR2
1.3.1270PANTHER_STCALIB_CFG 1593
SYSTICK Calibration register
1.3.1271PANTHER_WAITPIPE 1594
Wait State Pipeline
1.3.1272PANTHER_TRACE_CFG 1595
Debug Trace Configuration
1.3.1273PANTHER_ETMFIFO 1596
Embedded Trace Overflow Stall
1.3.1274PANTHER_PVTCFG1 1597
PVT Controller CFG1
1.3.1275PANTHER_PVTCFG2 1598
PVT Controller CFG2
1.3.1276EXTMEM_DATA[0..16777215] 1599
DATA
1.3.1277ITM_TRACE_EN 1600
ITM Trace Enable Register
1.3.1278ITM_TRACE_PRIVILEGE 1601
ITM Trace Privilege Register
1.3.1279ITM_TRACE_CTRL 1602
ITM Trace Control Register
1.3.1280ITM_INTEGRATION_WRITE 1604
ITM Integration Write Register
1.3.1281ITM_INTEGRATION_READ 1605
ITM Integration Read Register
1.3.1282ITM_INTEGRATION_MODE_CRTL 1606
ITM Integration Mode Control Register
1.3.1283ITM_LOCK_ACCESS 1607
ITM Lock Access Register
1.3.1284ITM_LOCK_STATUS 1608
ITM Lock Status Register
1.3.1285ITM_PID4 1609
ITM Peripheral Identification Register 4
1.3.1286ITM_PID5 1610
ITM Peripheral Identification Register 5
1.3.1287ITM_PID6 1611
ITM Peripheral Identification Register 6
1.3.1288ITM_PID7 1612
ITM Peripheral Identification Register 7
1.3.1289ITM_PID0 1613
ITM Peripheral Identification Register 0
1.3.1290ITM_PID1 1614
ITM Peripheral Identification Register 1
1.3.1291ITM_PID2 1615
ITM Peripheral Identification Register 2
1.3.1292ITM_PID3 1616
ITM Peripheral Identification Register 3
1.3.1293ITM_CID0 1617

ITM Component Identification Register 0
1.3.1294ITM_CID1 1618
ITM Component Identification Register 1
1.3.1295ITM_CID2 1619
ITM Component Identification Register 2
1.3.1296ITM_CID3 1620
ITM Component Identification Register 3
1.3.1297DWT_CTRL 1621
DWT Control Register
1.3.1298DWT_CYCLE_COUNT 1624
DWT Current PC Sampler Cycle Count Register
1.3.1299DWT_CPI_COUNT 1625
DWT CPI Count Register
1.3.1300DWT_EXC_OVHD_COUNT 1626
DWT Exception Overhead Count Register
1.3.1301DWT_SLEEP_COUNT 1627
DWT Sleep Count Register
1.3.1302DWT_LSU_COUNT 1628
DWT LSU Count Register
1.3.1303DWT_FOLD_COUNT 1629
DWT Fold Count Register
1.3.1304DWT_PC_SAMPLE 1630
DWT Program Counter Sample Register
1.3.1305DWT_COMP_0 1631
DWT Comparator Registers
1.3.1306DWT_MASK_0 1632
DWT Mask Registers
1.3.1307DWT_FUNCTION_0 1633
DWT Function registers
1.3.1308DWT_COMP_1 1635
DWT Comparator Registers
1.3.1309DWT_MASK_1 1636
DWT Mask Registers
1.3.1310DWT_FUNCTION_1 1637
DWT Function registers
1.3.1311DWT_COMP_2 1639
DWT Comparator Registers
1.3.1312DWT_MASK_2 1640
DWT Mask Registers
1.3.1313DWT_FUNCTION_2 1641
DWT Function registers
1.3.1314DWT_COMP_3 1643
DWT Comparator Registers
1.3.1315DWT_MASK_3 1644
DWT Mask Registers
1.3.1316DWT_FUNCTION_3 1645
DWT Function registers
1.3.1317FPB_CTRL 1647
Flash Patch Control Register
1.3.1318FPB_REMAP 1649
Flash Patch Remap Register
1.3.1319FPB_FP_COMP_0 1650
Flash Patch Comparator Registers
1.3.1320FPB_FP_COMP_1 1652

Flash Patch Comparator Registers
1.3.1321FPB_FP_COMP_2 1654
Flash Patch Comparator Registers
1.3.1322FPB_FP_COMP_3 1656
Flash Patch Comparator Registers
1.3.1323FPB_FP_COMP_4 1658
Flash Patch Comparator Registers
1.3.1324FPB_FP_COMP_5 1660
Flash Patch Comparator Registers
1.3.1325FPB_FP_COMP_6 1662
Flash Patch Comparator Registers
1.3.1326FPB_FP_COMP_7 1664
Flash Patch Comparator Registers
1.3.1327FPB_PID4 1666
FPB Peripheral Identification Register 4
1.3.1328FPB_PID5 1667
FPB Peripheral Identification Register 5
1.3.1329FPB_PID6 1668
FPB Peripheral Identification Register 6
1.3.1330FPB_PID7 1669
FPB Peripheral Identification Register 7
1.3.1331FPB_PID0 1670
FPB Peripheral Identification Register 0
1.3.1332FPB_PID1 1671
FPB Peripheral Identification Register 1
1.3.1333FPB_PID2 1672
FPB Peripheral Identification Register 2
1.3.1334FPB_PID3 1673
FPB Peripheral Identification Register 3
1.3.1335FPB_CID0 1674
FPB Component Identification Register 0
1.3.1336FPB_CID1 1675
FPB Component Identification Register 1
1.3.1337FPB_CID2 1676
FPB Component Identification Register 2
1.3.1338FPB_CID3 1677
FPB Component Identification Register 3
1.3.1339NVIC_INT_CTL_TYPE 1678
Interrupt Controller Type Register
1.3.1340NVIC_SYSTICK_CTL 1679
SYSTICK Control and Status register
1.3.1341NVIC_SYSTICK_RELOAD 1680
SYSTICK Reload value
1.3.1342NVIC_SYSTICK_CURRENT 1681
SYSTICK Counter
1.3.1343NVIC_SYSTICK_CAL 1682
SYSTICK Calibration register
1.3.1344NVIC_SETENA0 1683
Interrupt Enable Set 0-31
1.3.1345NVIC_CLRENA0 1684
Interrupt Enable Clear 0-31
1.3.1346NVIC_SETPEND0 1685
Interrupt Pending Set 0-31
1.3.1347NVIC_CLRPEND0 1686

Interrupt Pending Clear 0-31
1.3.1348NVIC_ACTIVE0 1687
Active Interrupts 0-31
1.3.1349NVIC_PRI_0 1688
Interrupt Priority 0-31
1.3.1350NVIC_PRI_1 1689
Interrupt Priority 0-31
1.3.1351NVIC_PRI_2 1690
Interrupt Priority 0-31
1.3.1352NVIC_PRI_3 1691
Interrupt Priority 0-31
1.3.1353NVIC_PRI_4 1692
Interrupt Priority 0-31
1.3.1354NVIC_PRI_5 1693
Interrupt Priority 0-31
1.3.1355NVIC_PRI_6 1694
Interrupt Priority 0-31
1.3.1356NVIC_PRI_7 1695
Interrupt Priority 0-31
1.3.1357NVIC_PRI_8 1696
Interrupt Priority 0-31
1.3.1358NVIC_PRI_9 1697
Interrupt Priority 0-31
1.3.1359NVIC_PRI_10 1698
Interrupt Priority 0-31
1.3.1360NVIC_PRI_11 1699
Interrupt Priority 0-31
1.3.1361NVIC_PRI_12 1700
Interrupt Priority 0-31
1.3.1362NVIC_PRI_13 1701
Interrupt Priority 0-31
1.3.1363NVIC_PRI_14 1702
Interrupt Priority 0-31
1.3.1364NVIC_PRI_15 1703
Interrupt Priority 0-31
1.3.1365NVIC_PRI_16 1704
Interrupt Priority 0-31
1.3.1366NVIC_PRI_17 1705
Interrupt Priority 0-31
1.3.1367NVIC_PRI_18 1706
Interrupt Priority 0-31
1.3.1368NVIC_PRI_19 1707
Interrupt Priority 0-31
1.3.1369NVIC_PRI_20 1708
Interrupt Priority 0-31
1.3.1370NVIC_PRI_21 1709
Interrupt Priority 0-31
1.3.1371NVIC_PRI_22 1710
Interrupt Priority 0-31
1.3.1372NVIC_PRI_23 1711
Interrupt Priority 0-31
1.3.1373NVIC_PRI_24 1712
Interrupt Priority 0-31
1.3.1374NVIC_PRI_25 1713

Interrupt Priority 0-31
1.3.1375NVIC_PRI_26 1714
Interrupt Priority 0-31
1.3.1376NVIC_PRI_27 1715
Interrupt Priority 0-31
1.3.1377NVIC_PRI_28 1716
Interrupt Priority 0-31
1.3.1378NVIC_PRI_29 1717
Interrupt Priority 0-31
1.3.1379NVIC_PRI_30 1718
Interrupt Priority 0-31
1.3.1380NVIC_PRI_31 1719
Interrupt Priority 0-31
1.3.1381NVIC_CPUID_BASE 1720
CPU ID Base Register
1.3.1382NVIC_INTR_CTRL_STATE 1721
Interrupt Control State Register
1.3.1383NVIC_VECT_OFFSET 1723
Interrupt Vector Table Offset
1.3.1384NVIC_APPLN_INTR 1724
Application Interrupt and Reset Control Register
1.3.1385NVIC_SYSTEM_CONTROL 1726
System Control Register
1.3.1386NVIC_CFG_CONTROL 1727
Configuration Control Register
1.3.1387NVIC_SYS_PRIO_HANDLER_4_7 1729
System Handler Priority Registers
1.3.1388NVIC_SYS_PRIO_HANDLER_8_11 1730
System Handler Priority Registers
1.3.1389NVIC_SYS_PRIO_HANDLER_12_15 1731
System Handler Priority Registers
1.3.1390NVIC_SYS_HANDLER_CSR 1732
System Handler Control and State Register
1.3.1391NVIC_MEMMAN_FAULT_STATUS 1734
Memory Manage Fault Status Registers.
1.3.1392NVIC_BUS_FAULT_STATUS 1735
Bus Fault Status Register
1.3.1393NVIC_USAGE_FAULT_STATUS 1736
Usage Fault Status Register
1.3.1394NVIC_HARD_FAULT_STATUS 1737
Hard Fault Status Register
1.3.1395NVIC_DEBUG_FAULT_STATUS 1738
Debug Fault Status Register
1.3.1396NVIC_MEMMAN_FAULT_ADD 1740
Memory Manage Fault Address Register
1.3.1397NVIC_BUS_FAULT_ADD 1741
Bus Fault Address Register
1.3.1398CORE_DBG_DBG_HLT_CS 1742
Debug Halting Control and Status register
1.3.1399CORE_DBG_DBG_REG_SEL 1744
Debug Core Register Selector Register
1.3.1400CORE_DBG_DBG_REG_DATA 1746
Debug Core Register Data Register
1.3.1401CORE_DBG_EXC_MON_CTL 1747

Debug Exception and Monitor Control register
1.3.1402TPIU_SUPPORTED_SYNC_PRT_SZ 1749
Supported Sync Port Sizes Register
1.3.1403TPIU_CURRENT_SYNC_PRT_SZ 1750
Current Sync Port Size Register
1.3.1404TPIU_ASYNC_CLK_PRESCALER 1751
Async Clock Prescaler Register
1.3.1405TPIU_PROTOCOL 1752
Selected Pin Protocol Register
1.3.1406TPIU_FORM_FLUSH_CTRL 1753
Formatter and Flush Control Register
1.3.1407TPIU_ITATBCTR2 1754
Integration Test Registers
1.3.1408TPIU_ITATBCTR0 1755
Integration Test Registers
1.3.1409ETM_CTL 1756
ETM Control register
1.3.1410ETM_CFG_CODE 1759
ETM Configuration code register
1.3.1411ETM_TRIG_EVENT 1761
Trigger Event Register
1.3.1412ETM_STATUS 1762
ETM Status Register
1.3.1413ETM_SYS_CFG 1763
System Configuration Register
1.3.1414ETM_TRACE_ENB_EVENT 1765
Trace Enable Event Register
1.3.1415ETM_TRACE_EN_CTRL1 1766
TraceEnable Control 1 Register
1.3.1416ETM_FIFOFULL_LEVEL 1768
FIFOFULL Level Register
1.3.1417ETM_SYNC_FREQ 1769
Synchronization Frequency Register
1.3.1418ETM_ETM_ID 1770
ETM ID Register
1.3.1419ETM_CFG_CODE_EXT 1772
Configuration Code Extension Register
1.3.1420ETM_TR_SS_EMBICE_CTRL 1774
Trace Start/Stop EmbeddedICE Control Register
1.3.1421ETM_CS_TRACE_ID 1775
CoreSight Trace ID Register
1.3.1422ETM_OS_LOCK_ACCESS 1776
OS Lock Access Register
1.3.1423ETM_OS_LOCK_STATUS 1777
OS Lock Status Register
1.3.1424ETM_INT_MODE_CTRL 1778
Integration Mode Control Register
1.3.1425ETM_CLM_TAG_SET 1779
Claim Tag Set Register
1.3.1426ETM_CLM_TAG_CLR 1780
Claim Tag Clear Register
1.3.1427ETM_LOCK_ACCESS 1781
Lock Access Register
1.3.1428ETM_LOCK_STATUS 1782

Lock Status Register
1.3.1429ETM_AUTH_STATUS 1783
Authentication Status Register
1.3.1430ETM_DEV_TYPE 1784
Device Type Register
1.3.1431ETM_PID4 1785
ETM Peripheral Identification Register 4
1.3.1432ETM_PID5 1786
ETM Peripheral Identification Register 5
1.3.1433ETM_PID6 1787
ETM Peripheral Identification Register 6
1.3.1434ETM_PID7 1788
ETM Peripheral Identification Register 7
1.3.1435ETM_PID0 1789
ETM Peripheral Identification Register 0
1.3.1436ETM_PID1 1790
ETM Peripheral Identification Register 1
1.3.1437ETM_PID2 1791
ETM Peripheral Identification Register 2
1.3.1438ETM_PID3 1792
ETM Peripheral Identification Register 3
1.3.1439ETM_CID0 1793
ETM Component Identification Register 0
1.3.1440ETM_CID1 1794
ETM Component Identification Register 1
1.3.1441ETM_CID2 1795
ETM Component Identification Register 2
1.3.1442ETM_CID3 1796
ETM Component Identification Register 3
1.3.1443ROM_TABLE_NVIC 1797
NVIC
1.3.1444ROM_TABLE_DWT 1798
DWT
1.3.1445ROM_TABLE_FPB 1799
FPB
1.3.1446ROM_TABLE_ITM 1800
ITM
1.3.1447ROM_TABLE_TPIU 1801
TPIU
1.3.1448ROM_TABLE_ETM 1802
ETM
1.3.1449ROM_TABLE_END 1803
END
1.3.1450ROM_TABLE_MEMTYPE 1804
MEMTYPE
1.3.1451ROM_TABLE_PID4 1805
ROM Table Peripheral Identification Register 4
1.3.1452ROM_TABLE_PID5 1806
ROM Table Peripheral Identification Register 5
1.3.1453ROM_TABLE_PID6 1807
ROM Table Peripheral Identification Register 6
1.3.1454ROM_TABLE_PID7 1808
ROM Table Peripheral Identification Register 7
1.3.1455ROM_TABLE_PID0 1809

ROM Table Peripheral Identification Register 0
1.3.1456ROM_TABLE_PID1 1810
ROM Table Peripheral Identification Register 1
1.3.1457ROM_TABLE_PID2 1811
ROM Table Peripheral Identification Register 2
1.3.1458ROM_TABLE_PID3 1812
ROM Table Peripheral Identification Register 3
1.3.1459ROM_TABLE_CID0 1813
ROM Table Component Identification Register 0
1.3.1460ROM_TABLE_CID1 1814
ROM Table Component Identification Register 1
1.3.1461ROM_TABLE_CID2 1815
ROM Table Component Identification Register 2
1.3.1462ROM_TABLE_CID3 1816
ROM Table Component Identification Register 3

Register Mapping

Register Mapping discusses the registers of the PSoC 5 device. It lists all the registers in mapping tables, in address order.

See the *PSoC 3, PSoC 5 Architecture TRM (Technical Reference Manual)* for complete functionality.

1.1 Maneuvering Around the Registers

For ease-of-use, this chapter is formatted so that there is one register per page, although some registers use two pages. On each page, from top to bottom, there are four sections:

1. Register name and address (from lowest to highest).
2. Register table showing the bit organization, with reserved bits grayed out.
3. Written description of register specifics or links to additional register information.
4. Detailed register bit descriptions.

1.2 Register Conventions

The following table lists the register conventions.

Convention	Example	Description
‘x’ in a register name	ACBxxCR1	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WOC	WOC:0	Write one to clear
WZC	WZC:0	Write zero to clear
RC	RC:0	Read to clear
WC	WC:0	Write to clear
NA	NA:000	Reserved
U	R:U	Undefined
00	RW : 00	Reset value is 0x00
XX	RW : XX	Register is not reset
Empty, grayed out table cell		Reserved bit or group of bits, unless otherwise stated. Write reserved bits to zero. Software cannot make any assumptions about return values.

1.3 PSoC 5 Register Map

The PSoC 5 device has a total register address space of 64 kbytes.

Register Name	Purpose	Address
FLASH_DATA[0..262143]	DATA	[0..262143 * 0x1]
SRAM_CODE64K[0..16383]	Code System Memory Bank	0x1fff8000 + [0..16383 * 0x1]
SRAM_CODE32K[0..8191]	Code System Memory Bank	0x1fffc000 + [0..8191 * 0x1]
SRAM_CODE16K[0..4095]	Code System Memory Bank	0x1fffe000 + [0..4095 * 0x1]
SRAM_CODE[0..4095]	Code System Memory Bank	0x1ffff000 + [0..4095 * 0x1]
SRAM_DATA[0..4095]	Data System Memory Bank	0x20000000 + [0..4095 * 0x1]
SRAM_DATA16K[0..4095]	Data System Memory Bank	0x20001000 + [0..4095 * 0x1]
SRAM_DATA32K[0..8191]	Data System Memory Bank	0x20002000 + [0..8191 * 0x1]
SRAM_DATA64K[0..16383]	Data System Memory Bank	0x20004000 + [0..16383 * 0x1]
CLKDIST_CR	Configuration Register CR	0x40004000
CLKDIST_LD	LOAD Register	0x40004001
CLKDIST_WRK0	LSB Shadow Divider Value Register	0x40004002
CLKDIST_WRK1	MSB Shadow Divider Value Register	0x40004003
CLKDIST_MSTR0	Master clock (clk_sync_d) Divider Value Register	0x40004004
CLKDIST_MSTR1	Master (clk_sync_d) Configuration Register/ CPU Divider Value	0x40004005
CLKDIST_BCFG0	CLK_BUS LSB Divider Value Register	0x40004006
CLKDIST_BCFG1	CLK_BUS MSB Divider Value Register	0x40004007
CLKDIST_BCFG2	CLK_BUS Configuration Register	0x40004008
CLKDIST_UCFG	USB Configuration Register	0x40004009
CLKDIST_DLY0	Delay block Configuration Register	0x4000400a
CLKDIST_DLY1	Delay block Configuration Register	0x4000400b
CLKDIST_DMASK	Digital Clock Mask Register	0x40004010
CLKDIST_AMASK	Analog Clock Mask Register	0x40004014
CLKDIST_DCFG[0..7]_CFG0	LSB Divider Value Register	0x40004080 + [0..7 * 0x4]
CLKDIST_DCFG[0..7]_CFG1	MSB Divider Value Register	0x40004080 + [0..7 * 0x4] + 0x1
CLKDIST_DCFG[0..7]_CFG2	Configuration Register	0x40004080 + [0..7 * 0x4] + 0x2
CLKDIST_ACFG[0..3]_CFG0	LSB Divider Value Register	0x40004100 + [0..3 * 0x4]
CLKDIST_ACFG[0..3]_CFG1	MSB Divider Value Register	0x40004100 + [0..3 * 0x4] + 0x1
CLKDIST_ACFG[0..3]_CFG2	Configuration Register	0x40004100 + [0..3 * 0x4] + 0x2
CLKDIST_ACFG[0..3]_CFG3	Analog clocks Configuration Register	0x40004100 + [0..3 * 0x4] + 0x3
FASTCLK_IMO_CR	Internal Main Oscillator Control Register	0x40004200
FASTCLK_XMHZ_CSR	External 4-33 MHz Crystal Oscillator Status and Control Register	0x40004210
FASTCLK_XMHZ_TST	External 4-33 MHz Crystal Oscillator Test Register	0x40004211
FASTCLK_XMHZ_CFG0	External 4-33 MHz Crystal Oscillator Configuration Register 0	0x40004212
FASTCLK_XMHZ_CFG1	RESERVED REGISTER LOCATION NOT USED IN THIS DEVICE	0x40004213
FASTCLK_PLL_CFG0	PLL Configuration Register	0x40004220

Register Name	Purpose	Address
FASTCLK_PLL_CFG1	PLL Control Register	0x40004221
FASTCLK_PLL_P	PLL P-Counter Configuration Register	0x40004222
FASTCLK_PLL_Q	PLL Q-Counter Configuration Register	0x40004223
FASTCLK_PLL_TST	PLL Test Register	0x40004224
FASTCLK_PLL_SR	PLL Status Register	0x40004225
SLOWCLK_ILO_CR0	Internal Low-speed Oscillator Control Register 0	0x40004300
SLOWCLK_ILO_CR1	Internal Low-speed Oscillator Control Register 1	0x40004301
SLOWCLK_X32_CR	External 32kHz Crystal Oscillator Control Register	0x40004308
SLOWCLK_X32_CFG	External 32kHz Crystal Oscillator Configuration Register	0x40004309
SLOWCLK_X32_TST	External 32kHz Crystal Oscillator Test Register	0x4000430a
BOOST_CR0	Boost Control 0	0x40004320
BOOST_CR1	Boost Control 1	0x40004321
BOOST_CR2	Boost Control 2	0x40004322
BOOST_CR3	Boost Control 3	0x40004323
BOOST_SR	Boost Status	0x40004324
PWRSYS_CR0	Power System Control Register 0	0x40004330
PWRSYS_CR1	Power System Control Register 1	0x40004331
PM_TW_CFG0	Timewheel Configuration Register 0	0x40004380
PM_TW_CFG1	Timewheel Configuration Register 1	0x40004381
PM_TW_CFG2	Timewheel Configuration Register 2	0x40004382
PM_WDT_CFG	Watchdog Timer Configuration Register	0x40004383
PM_WDT_CR	Watchdog Timer Control Register	0x40004384
PM_INT_SR	Power Manager Interrupt Status Register	0x40004390
PM_MODE_CFG0	Power Mode Configuration Register 0	0x40004391
PM_MODE_CFG1	Power Mode Configuration Register 1	0x40004392
PM_MODE_CSR	Power Mode Control/Status Register	0x40004393
PM_ACT_CFG0	Active Power Mode Configuration Register 0	0x400043a0
PM_ACT_CFG1	Active Power Mode Configuration Register 1	0x400043a1
PM_ACT_CFG2	Active Power Mode Configuration Register 2	0x400043a2
PM_ACT_CFG3	Active Power Mode Configuration Register 3	0x400043a3
PM_ACT_CFG4	Active Power Mode Configuration Register 4	0x400043a4
PM_ACT_CFG5	Active Power Mode Configuration Register 5	0x400043a5
PM_ACT_CFG6	Active Power Mode Configuration Register 6	0x400043a6
PM_ACT_CFG7	Active Power Mode Configuration Register 7	0x400043a7
PM_ACT_CFG8	Active Power Mode Configuration Register 8	0x400043a8
PM_ACT_CFG9	Active Power Mode Configuration Register 9	0x400043a9
PM_ACT_CFG10	Active Power Mode Configuration Register 10	0x400043aa
PM_ACT_CFG11	Active Power Mode Configuration Register 11	0x400043ab
PM_STBY_CFG0	Standby Power Mode Configuration Register 0	0x400043b0
PM_STBY_CFG1	Standby Power Mode Configuration Register 1	0x400043b1

Register Name	Purpose	Address
PM_STBY_CFG2	Standby Power Mode Configuration Register 2	0x400043b2
PM_STBY_CFG3	Standby Power Mode Configuration Register 3	0x400043b3
PM_STBY_CFG4	Standby Power Mode Configuration Register 4	0x400043b4
PM_STBY_CFG5	Standby Power Mode Configuration Register 5	0x400043b5
PM_STBY_CFG6	Standby Power Mode Configuration Register 6	0x400043b6
PM_STBY_CFG7	Standby Power Mode Configuration Register 7	0x400043b7
PM_STBY_CFG8	Standby Power Mode Configuration Register 8	0x400043b8
PM_STBY_CFG9	Standby Power Mode Configuration Register 9	0x400043b9
PM_STBY_CFG10	Standby Power Mode Configuration Register 10	0x400043ba
PM_STBY_CFG11	Standby Power Mode Configuration Register 11	0x400043bb
PM_AVAIL_CR0	Power Mode Available Subsystem Control Register 0	0x400043c0
PM_AVAIL_CR1	Power Mode Available Subsystem Control Register 1	0x400043c1
PM_AVAIL_CR2	Power Mode Available Subsystem Control Register 2	0x400043c2
PM_AVAIL_CR3	Power Mode Available Subsystem Control Register 3	0x400043c3
PM_AVAIL_CR4	Power Mode Available Subsystem Control Register 4	0x400043c4
PM_AVAIL_CR5	Power Mode Available Subsystem Control Register 5	0x400043c5
PM_AVAIL_CR6	Power Mode Available Subsystem Control Register 6	0x400043c6
PM_AVAIL_SR0	Power Mode Available Subsystem Status Register 0	0x400043d0
PM_AVAIL_SR1	Power Mode Available Subsystem Status Register 1	0x400043d1
PM_AVAIL_SR2	Power Mode Available Subsystem Status Register 2	0x400043d2
PM_AVAIL_SR3	Power Mode Available Subsystem Status Register 3	0x400043d3
PM_AVAIL_SR4	Power Mode Available Subsystem Status Register 4	0x400043d4
PM_AVAIL_SR5	Power Mode Available Subsystem Status Register 5	0x400043d5
PM_AVAIL_SR6	Power Mode Available Subsystem Status Register 6	0x400043d6
PICU[0..15]_INTTYPE[0..7]	Port Interrupt Control Type Register	(0x40004500 + [0..15 * 0x8]) + [0..7 * 0x1]
PICU[0..15]_INTSTAT	Port Interrupt Control Status Register	0x40004580 + [0..15 * 0x1]
PICU[0..15]_SNAP	Port Interrupt Control Snap Shot Register	0x40004590 + [0..15 * 0x1]
CMP[0..3]_TR	Comparator Trim Register	0x40004600 + [0..3 * 0x1]
DAC[0..3]_TR	DAC Block Trim Register	0x40004608 + [0..3 * 0x1]
NPUMP_DSM_TR0	Delta Sigma Modulator (DSM) Negative Pump Trim Register 0	0x40004610
NPUMP_ABUF_TR0	Analog Linear Output Buffer (ABUF) Negative Pump Trim Register 0	0x40004612
SAR[0..1]_TR0	SAR trim register 0	0x40004614 + [0..1 * 0x2]
ABUF[0..3]_TR0	Analog Output Buffer Trim Register 0	0x40004620 + [0..3 * 0x2]
ABUF[0..3]_TR1	Analog Output Buffer Trim Register 1	0x40004620 + [0..3 * 0x2] + 0x1

Register Name	Purpose	Address
PWRSYS_HIB_TR0	Hibernate Trim Register 0	0x40004680
PWRSYS_HIB_TR1	Hibernate Trim Register 1	0x40004681
PWRSYS_I2C_TR	I2C Regulator Trim Register 1	0x40004682
PWRSYS_SLP_TR	Sleep Regulator Trim Register	0x40004683
PWRSYS_BUZZ_TR	Power Mode Buzz Trim Register	0x40004684
PWRSYS_WAKE_TR0	Power Mode Wakeup Trim Register	0x40004685
PWRSYS_WAKE_TR1	Power Mode Wakeup Trim Register	0x40004686
PWRSYS_BREF_TR	Boot Reference Trim Register	0x40004687
PWRSYS_BG_TR	Bandgap Trim	0x40004688
ILO_TR0	Internal Low-speed Oscillator Trim Register	0x40004690
ILO_TR1	Internal Low-speed Oscillator Coarse Trim Register	0x40004691
X32_TR	32 kHz Watch Crystal Oscillator Trim Register	0x40004698
IMO_TR0	Internal Main Oscillator Trim Register 0	0x400046a0
IMO_TR1	Internal Main Oscillator Trim Register 1	0x400046a1
IMO_GAIN	Internal Main Oscillator Gain Trim Register	0x400046a2
IMO_C36M	Internal Main Oscillator 36 MHz clock control register {INTERNAL}	0x400046a3
IMO_TR2	Internal Main Oscillator Trim Register 2	0x400046a4
XMHZ_TR	External 4-25 MHz Crystal Oscillator Trim Register	0x400046a8
MLOGIC_DMP_DMY	Dumpster Register	0x400046e2
MLOGIC_SEG_CR	Segment Control Register	0x400046e4
MLOGIC_SEG_CFG0	Segment Configuration Register	0x400046e5
MLOGIC_DBG_DBE	Debug Enable Register	0x400046e8
MLOGIC_CPU_SCR	System Status and Control Register	0x400046ea
RESET_IPOR_CR0	Imprecise Power On Reset Control Register 0	0x400046f0
RESET_IPOR_CR1	Imprecise Power On Reset Control Register 1	0x400046f1
RESET_IPOR_CR2	Imprecise Power On Reset Control Register 2	0x400046f2
RESET_IPOR_CR3	Imprecise Power On Reset Control Register 3	0x400046f3
RESET_CR0	LVI Set Point Control Register	0x400046f4
RESET_CR1	Reset System Control Register	0x400046f5
RESET_CR2	Software Reset Control Register	0x400046f6
RESET_CR3	LVD/POR Test Mode Control Register	0x400046f7
RESET_SR0	Reset and Voltage Detection Status Register 0	0x400046f8
RESET_SR1	Reset and Voltage Detection Status Register 1	0x400046f9
RESET_SR2	Reset and Voltage Detection Status Register 2	0x400046fa
RESET_TR	PRES Trim Register	0x400046fb
SPC_FM_EE_CR	FM_EE_CR	0x40004700
SPC_FM_EE_WAKE_CNT	FM_EE_WAKE_CNT	0x40004701
SPC_EE_SCR	EEPROM Status & Control Register	0x40004702
SPC_EE_ERR	EEPROM Error Register	0x40004703
SPC_CPU_DATA	SPC CPU Data Register	0x40004720
SPC_DMA_DATA	SPC DMA Data Register	0x40004721

Register Name	Purpose	Address
SPC_SR	SPC Status Register	0x40004722
SPC_CR	SPC Control Register	0x40004723
SPC_DMM_MAP_SRAM[0..127]	SPC Direct Memory Mapping	0x40004780 + [0..127 * 0x1]
CACHE_CC_CTL	Cache Control Register	0x40004800
CACHE_ECC_CORR	Error Correction detected	0x40004880
CACHE_ECC_ERR	Error Correction failed	0x40004888
CACHE_FLASH_ERR	FLASH error	0x40004890
CACHE_HITMISS	HIT/MISS counters	0x40004898
I2C_XCFG	I2C Extended Configuration Register	0x400049c8
I2C_ADR	I2C Slave Adddress Register	0x400049ca
I2C_CFG	I2C Configuration Register	0x400049d6
I2C_CSR	I2C Control and Status Register	0x400049d7
I2C_D	I2C Data Register	0x400049d8
I2C_MCSR	I2C Master Control and Status Register	0x400049d9
I2C_CLK_DIV	I2C Clock Divide Factor Register	0x400049db
DEC_CR	Decimator Control Register	0x40004e00
DEC_SR	Decimator Status Register	0x40004e01
DEC_SHIFT1	Decimator Shifter 1 (Input)	0x40004e02
DEC_SHIFT2	Decimator Shifter 2 (Output)	0x40004e03
DEC_DR2	Decimator Decimation Rate (2)	0x40004e04
DEC_DR2H	Decimator Decimation Rate (2)	0x40004e05
DEC_DR1	Decimator Decimation Rate (1) of CIC Filter	0x40004e06
DEC_OCOR	Decimator Offset Correction Coefficient (Low Byte)	0x40004e08
DEC_OCORM	Decimator Offset Correction Coefficient (Middle Byte)	0x40004e09
DEC_OCORH	Decimator Offset Correction Coefficient (High Byte)	0x40004e0a
DEC_GCOR	Decimator Gain Correction Coefficient (Low Byte)	0x40004e0c
DEC_GCORH	Decimator Gain Correction Coefficient (High Byte)	0x40004e0d
DEC_GVAL	Decimator Gain Correction Size Register	0x40004e0e
DEC_OUTSAMP	Decimator Output Data Sample (Low Byte)	0x40004e10
DEC_OUTSAMPM	Decimator Output Data Sample (Middle Byte)	0x40004e11
DEC_OUTSAMPH	Decimator Output Data Sample (High Byte)	0x40004e12
DEC_OUTSAMPS	Decimator Output Data Sample (Sign Extension)	0x40004e13
DEC_COHER	Decimator Coherency Register	0x40004e14
TMR[0..3]_CFG0	Configuration Register CFG0	0x40004f00 + [0..3 * 0xc]
TMR[0..3]_CFG1	Configuration Register CFG1	0x40004f00 + [0..3 * 0xc] + 0x1
TMR[0..3]_PER0	Timer Period Register PER0	0x40004f00 + [0..3 * 0xc] + 0x2
TMR[0..3]_PER1	Timer Period Register PER1	0x40004f00 + [0..3 * 0xc] + 0x3
TMR[0..3]_CNT_CMP0	Count/Comparator value CNT/CMP0	0x40004f00 + [0..3 * 0xc] + 0x4
TMR[0..3]_CNT_CMP1	Count/Comparator value CNT/CMP1	0x40004f00 + [0..3 * 0xc] + 0x5

Register Name	Purpose	Address
TMR[0..3]_CAP0	Capture Value CAP0	0x40004f00 + [0..3 * 0xc] + 0x6
TMR[0..3]_CAP1	Capture Value CAP1	0x40004f00 + [0..3 * 0xc] + 0x7
TMR[0..3]_SR0	Status Register SR0	0x40004f00 + [0..3 * 0xc] + 0x8
TMR[0..3]_RT0	Configuration Register RT0	0x40004f00 + [0..3 * 0xc] + 0x9
TMR[0..3]_RT1	Configuration Register RT1	0x40004f00 + [0..3 * 0xc] + 0xa
PRT[0..15]_PC[0..7]	Port Pin Configuration Register	(0x40005000 + [0..15 * 0x8]) + [0..7 * 0x1]
PRT[0..15]_DR_ALIAS	Aliased Port Data Output Register	0x40005080 + [0..15 * 0x1]
PRT[0..15]_PS_ALIAS	Aliased Port Pin State Register	0x40005090 + [0..15 * 0x1]
PRT[0..11]_DR	Port Data Output Register	0x40005100 + [0..11 * 0x10]
PRT[0..11]_PS	Port Pin State Register1	0x40005100 + [0..11 * 0x10] + 0x1
PRT[0..11]_DM[0..2]	Port Drive Mode Register	(0x40005100 + [0..11 * 0x10]) + 0x2 + [0..2 * 0x1]
PRT[0..11]_SLW	Port slew rate control	0x40005100 + [0..11 * 0x10] + 0x5
PRT[0..11]_BYP	Port Bypass enable	0x40005100 + [0..11 * 0x10] + 0x6
PRT[0..11]_BIE	Port Bidirection enable	0x40005100 + [0..11 * 0x10] + 0x7
PRT[0..11]_INP_DIS	Input buffer disable override	0x40005100 + [0..11 * 0x10] + 0x8
PRT[0..11]_CTL	Port wide control signals	0x40005100 + [0..11 * 0x10] + 0x9
PRT[0..11]_PRT	Port wide configuration register	0x40005100 + [0..11 * 0x10] + 0xa
PRT[0..11]_BIT_MASK	Bit-mask for Aliased Register access	0x40005100 + [0..11 * 0x10] + 0xb
PRT[0..11]_AMUX	Port Analog global mux bus enable	0x40005100 + [0..11 * 0x10] + 0xc
PRT[0..11]_AG	Port Analog global enable	0x40005100 + [0..11 * 0x10] + 0xd
PRT[0..11]_LCD_COM_SEG	Port LCD Com seg bits.	0x40005100 + [0..11 * 0x10] + 0xe
PRT[0..11]_LCD_EN	Port LCD enable register.	0x40005100 + [0..11 * 0x10] + 0xf
PRT12_DR	Port Data Output Register	0x400051c0
PRT12_PS	Port Pin State Register1	0x400051c1
PRT12_DM[0..2]	Port Drive Mode Register	0x400051c2 + [0..2 * 0x1]
PRT12_SLW	Port slew rate control	0x400051c5
PRT12_BYP	Port Bypass enable	0x400051c6
PRT12_BIE	Port Bidirection enable	0x400051c7
PRT12_INP_DIS	Input buffer disable override	0x400051c8
PRT12_SIO_HYST_EN	SIO Hysteresis enable	0x400051c9
PRT12_PRT	Port wide configuration register	0x400051ca
PRT12_BIT_MASK	Bit-mask for Aliased Register access	0x400051cb
PRT12_SIO_REG_HIFREQ	Regulated pull-up driver DC current setting	0x400051cc
PRT12_AG	Port Analog global enable	0x400051cd
PRT12_SIO_CFG	SIO Input Output Configuration	0x400051ce
PRT12_SIO_DIFF	Differential Input Buffer reference voltage selec-tion	0x400051cf
PRT15_DR	Port Data Output Register	0x400051f0
PRT15_PS	Port Pin State Register1	0x400051f1
PRT15_DM[0..2]	Port Drive Mode Register	0x400051f2 + [0..2 * 0x1]
PRT15_SLW	Port slew rate control	0x400051f5
PRT15_BYP	Port Bypass enable	0x400051f6

Register Name	Purpose	Address
PRT15_BIE	Port Bidirection enable	0x400051f7
PRT15_INP_DIS	Input buffer disable override	0x400051f8
PRT15_CTL	Port wide control signals	0x400051f9
PRT15_PRT	Port wide configuration register	0x400051fa
PRT15_BIT_MASK	Bit-mask for Aliased Register access	0x400051fb
PRT15_AMUX	Port Analog global mux bus enable	0x400051fc
PRT15_AG	Port Analog global enable	0x400051fd
PRT15_LCD_COM_SEG	Port LCD Com seg bits.	0x400051fe
PRT15_LCD_EN	Port LCD enable register.	0x400051ff
PRT0_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005200
PRT0_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005201
PRT0_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005202
PRT0_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005203
PRT0_DBL_SYNC_IN	DSI double sync enable register.	0x40005204
PRT0_SYNC_OUT	DSI sync out enable register.	0x40005205
PRT0_CAPS_SEL	Global DSI select register.	0x40005206
PRT1_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005208
PRT1_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005209
PRT1_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x4000520a
PRT1_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x4000520b
PRT1_DBL_SYNC_IN	DSI double sync enable register.	0x4000520c
PRT1_SYNC_OUT	DSI sync out enable register.	0x4000520d
PRT1_CAPS_SEL	Global DSI select register.	0x4000520e
PRT2_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005210
PRT2_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005211
PRT2_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005212
PRT2_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005213
PRT2_DBL_SYNC_IN	DSI double sync enable register.	0x40005214
PRT2_SYNC_OUT	DSI sync out enable register.	0x40005215
PRT2_CAPS_SEL	Global DSI select register.	0x40005216
PRT3_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005218
PRT3_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005219
PRT3_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x4000521a
PRT3_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x4000521b

Register Name	Purpose	Address
PRT3_DBL_SYNC_IN	DSI double sync enable register.	0x4000521c
PRT3_SYNC_OUT	DSI sync out enable register.	0x4000521d
PRT3_CAPS_SEL	Global DSI select register.	0x4000521e
PRT4_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005220
PRT4_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005221
PRT4_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005222
PRT4_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005223
PRT4_DBL_SYNC_IN	DSI double sync enable register.	0x40005224
PRT4_SYNC_OUT	DSI sync out enable register.	0x40005225
PRT4_CAPS_SEL	Global DSI select register.	0x40005226
PRT5_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005228
PRT5_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005229
PRT5_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x4000522a
PRT5_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x4000522b
PRT5_DBL_SYNC_IN	DSI double sync enable register.	0x4000522c
PRT5_SYNC_OUT	DSI sync out enable register.	0x4000522d
PRT5_CAPS_SEL	Global DSI select register.	0x4000522e
PRT6_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005230
PRT6_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005231
PRT6_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005232
PRT6_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005233
PRT6_DBL_SYNC_IN	DSI double sync enable register.	0x40005234
PRT6_SYNC_OUT	DSI sync out enable register.	0x40005235
PRT6_CAPS_SEL	Global DSI select register.	0x40005236
PRT12_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005260
PRT12_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005261
PRT12_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005262
PRT12_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x40005263
PRT12_DBL_SYNC_IN	DSI double sync enable register.	0x40005264
PRT12_SYNC_OUT	DSI sync out enable register.	0x40005265
PRT15_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x40005278
PRT15_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x40005279

Register Name	Purpose	Address
PRT15_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x4000527a
PRT15_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x4000527b
PRT15_DBL_SYNC_IN	DSI double sync enable register.	0x4000527c
PRT15_SYNC_OUT	DSI sync out enable register.	0x4000527d
PRT15_CAPS_SEL	Global DSI select register.	0x4000527e
EMIF_NO_UDB	EMIF UDB Generation Register	0x40005400
EMIF_WAIT_STATES	External Memory Interface Wait States Register	0x40005401
EMIF_MEM_DWN	External Memory Power Down Register	0x40005402
EMIF_MEMCLK_DIV	External Memory Clock Divider Register	0x40005403
EMIF_CLOCK_EN	EMIF Clock Enable Register	0x40005404
SC[0..3]_CR0	Switched Capacitor Control Register 0	0x40005800 + [0..3 * 0x4]
SC[0..3]_CR1	Switched Capacitor Control Register 1	0x40005800 + [0..3 * 0x4] + 0x1
SC[0..3]_CR2	Switched Capacitor Control Register 2	0x40005800 + [0..3 * 0x4] + 0x2
DAC[0..3]_CR0	DAC Block Control Register 0	0x40005820 + [0..3 * 0x4]
DAC[0..3]_CR1	DAC Block Control Register 1	0x40005820 + [0..3 * 0x4] + 0x1
DAC[0..3]_TST	DAC Block Test Register	0x40005820 + [0..3 * 0x4] + 0x2
CMP[0..3]_CR	Comparator Control Register	0x40005840 + [0..3 * 0x1]
LUT[0..3]_CR	LUT Config Register	0x40005848 + [0..3 * 0x2]
LUT[0..3]_MX	LUT Input Mux Config Register	0x40005848 + [0..3 * 0x2] + 0x1
ABUF[0..3]_CR	Analog Output Buffer Configuration Register	0x40005858 + [0..3 * 0x2]
ABUF[0..3]_RSVD	ABUF reserved	0x40005858 + [0..3 * 0x2] + 0x1
LCDDAC_CR0	LCD Control Register 0	0x40005868
LCDDAC_CR1	LCDDAC Control Register 1	0x40005869
LCDDRV_CR	LCD Control Register	0x4000586a
BG_CR0	Bandgap Precision Reference Control 0	0x4000586c
BG_RSVD	Bandgap Precision Reference Reserved Register	0x4000586d
BG_DFT0	Bandgap Precision Reference DFT Register 0	0x4000586e
BG_DFT1	Bandgap Precision Reference DFT Register 1	0x4000586f
CAPSL_CFG0	Capsense Reference Driver Configuration Register	0x40005870
CAPSL_CFG1	Capsense IO Configuration Register	0x40005871
CAPSR_CFG0	Capsense Reference Driver Configuration Register	0x40005872
CAPSR_CFG1	Capsense IO Configuration Register	0x40005873
CAPS_DFT	Capsense DFT register	0x40005874
PUMP_CR0	Pump Configuration Register 0	0x40005876
PUMP_CR1	Pump Configuration Register 1	0x40005877
LPF0_CR0	Low Pass Filter Control Register	0x40005878
LPF0_RSVD	LPF Reserved	0x40005879
LPF1_CR0	Low Pass Filter Control Register	0x4000587a
LPF1_RSVD	LPF Reserved	0x4000587b
ANAIF_CFG_MISC_CR0	MISC Control Register 0	0x4000587c

Register Name	Purpose	Address
TFAULT_CR0	Timing Fault Control Register 0	0x4000587e
TFAULT_CR1	Timing Fault Control Register 1	0x4000587f
DSM[0..0]_CR0	Delta Sigma Modulator Control Register 0	0x40005880
DSM[0..0]_CR1	Delta Sigma Modulator Control Register 1	0x40005881
DSM[0..0]_CR2	Delta Sigma Modulator Control Register 2	0x40005882
DSM[0..0]_CR3	Delta Sigma Modulator Control Register 3	0x40005883
DSM[0..0]_CR4	Delta Sigma Modulator Control Register 4	0x40005884
DSM[0..0]_CR5	Delta Sigma Modulator Control Register 5	0x40005885
DSM[0..0]_CR6	Delta Sigma Modulator Control Register 6	0x40005886
DSM[0..0]_CR7	Delta Sigma Modulator Control Register 7	0x40005887
DSM[0..0]_CR8	Delta Sigma Modulator Control Register 8	0x40005888
DSM[0..0]_CR9	Delta Sigma Modulator Control Register 9	0x40005889
DSM[0..0]_CR10	Delta Sigma Modulator Control Register 10	0x4000588a
DSM[0..0]_CR11	Delta Sigma Modulator Control Register 11	0x4000588b
DSM[0..0]_CR12	Delta Sigma Modulator Control Register 12	0x4000588c
DSM[0..0]_CR13	Delta Sigma Modulator Control Register 13	0x4000588d
DSM[0..0]_CR14	Delta Sigma Modulator Control Register 14	0x4000588e
DSM[0..0]_CR15	Delta Sigma Modulator Control Register 15	0x4000588f
DSM[0..0]_CR16	Delta Sigma Modulator Control Register 0	0x40005890
DSM[0..0]_CR17	Delta Sigma Modulator Control Register	0x40005891
DSM[0..0]_REF0	Delta Sigma Modulator Reference Register 0	0x40005892
DSM[0..0]_REF1	Delta Sigma Modulator Reference Register 1	0x40005893
DSM[0..0]_REF2	Delta Sigma Modulator Reference Register 2	0x40005894
DSM[0..0]_REF3	Delta Sigma Modulator Reference Register 1	0x40005895
DSM[0..0]_DEM0	Delta Sigma Modulator Dynamic Element Matching Register 0	0x40005896
DSM[0..0]_DEM1	Delta Sigma Modulator Dynamic Element Matching Register 1	0x40005897
DSM[0..0]_TST0	Delta Sigma Modulator Test Register 0	0x40005898
DSM[0..0]_TST1	Delta Sigma Modulator Test Register 1	0x40005899
DSM[0..0]_BUF0	Delta Sigma Modulator Buffer Register 0	0x4000589a
DSM[0..0]_BUF1	Delta Sigma Modulator Buffer Register 1	0x4000589b
DSM[0..0]_BUF2	Delta Sigma Modulator Buffer Register 2	0x4000589c
DSM[0..0]_BUF3	Delta Sigma Modulator Buffer Register 2	0x4000589d
DSM[0..0]_MISC	Delta Sigma Modulator Miscellaneous register	0x4000589e
DSM[0..0]_RSVD1	Delta Sigma Modulator RSVD 1	0x4000589f
SAR[0..1]_CSR0	SAR status and control register 0	0x40005900 + [0..1 * 0x8]
SAR[0..1]_CSR1	SAR status and control register 1	0x40005900 + [0..1 * 0x8] + 0x1
SAR[0..1]_CSR2	SAR status and control register 2	0x40005900 + [0..1 * 0x8] + 0x2
SAR[0..1]_CSR3	SAR status and control register 3	0x40005900 + [0..1 * 0x8] + 0x3
SAR[0..1]_CSR4	SAR status and control register 4	0x40005900 + [0..1 * 0x8] + 0x4
SAR[0..1]_CSR5	SAR status and control register 5	0x40005900 + [0..1 * 0x8] + 0x5
SAR[0..1]_CSR6	SAR status and control register 6	0x40005900 + [0..1 * 0x8] + 0x6

Register Name	Purpose	Address
SAR[0..1]_CSR7	SAR status and control register 7	0x40005900 + [0..1 * 0x8] + 0x7
SC0_SW0	Switched Capacitor Analog Routing Register 0	0x40005a00
SC0_SW2	Switched Capacitor Analog Routing Register 2	0x40005a02
SC0_SW3	Switched Capacitor Analog Routing Register 3	0x40005a03
SC0_SW4	Switched Capacitor Analog Routing Register 4	0x40005a04
SC0_SW6	Switched Capacitor Analog Routing Register 6	0x40005a06
SC0_SW7	Switched Capacitor Analog Routing Register 7	0x40005a07
SC0_SW8	Switched Capacitor Analog Routing Register 8	0x40005a08
SC0_SW10	Switched Capacitor Analog Routing Register 10	0x40005a0a
SC0_CLK	Switched Capacitor Clock Selection Register	0x40005a0b
SC0_BST	Switched Capacitor Boost Clock Selection Register	0x40005a0c
SC1_SW0	Switched Capacitor Analog Routing Register 0	0x40005a10
SC1_SW2	Switched Capacitor Analog Routing Register 2	0x40005a12
SC1_SW3	Switched Capacitor Analog Routing Register 3	0x40005a13
SC1_SW4	Switched Capacitor Analog Routing Register 4	0x40005a14
SC1_SW6	Switched Capacitor Analog Routing Register 6	0x40005a16
SC1_SW7	Switched Capacitor Analog Routing Register 7	0x40005a17
SC1_SW8	Switched Capacitor Analog Routing Register 8	0x40005a18
SC1_SW10	Switched Capacitor Analog Routing Register 10	0x40005a1a
SC1_CLK	Switched Capacitor Clock Selection Register	0x40005a1b
SC1_BST	Switched Capacitor Boost Clock Selection Register	0x40005a1c
SC2_SW0	Switched Capacitor Analog Routing Register 0	0x40005a20
SC2_SW2	Switched Capacitor Analog Routing Register 2	0x40005a22
SC2_SW3	Switched Capacitor Analog Routing Register 3	0x40005a23
SC2_SW4	Switched Capacitor Analog Routing Register 4	0x40005a24
SC2_SW6	Switched Capacitor Analog Routing Register 6	0x40005a26
SC2_SW7	Switched Capacitor Analog Routing Register 7	0x40005a27
SC2_SW8	Switched Capacitor Analog Routing Register 8	0x40005a28
SC2_SW10	Switched Capacitor Analog Routing Register 10	0x40005a2a
SC2_CLK	Switched Capacitor Clock Selection Register	0x40005a2b
SC2_BST	Switched Capacitor Boost Clock Selection Register	0x40005a2c
SC3_SW0	Switched Capacitor Analog Routing Register 0	0x40005a30
SC3_SW2	Switched Capacitor Analog Routing Register 2	0x40005a32
SC3_SW3	Switched Capacitor Analog Routing Register 3	0x40005a33
SC3_SW4	Switched Capacitor Analog Routing Register 4	0x40005a34
SC3_SW6	Switched Capacitor Analog Routing Register 6	0x40005a36
SC3_SW7	Switched Capacitor Analog Routing Register 7	0x40005a37
SC3_SW8	Switched Capacitor Analog Routing Register 8	0x40005a38
SC3_SW10	Switched Capacitor Analog Routing Register 10	0x40005a3a
SC3_CLK	Switched Capacitor Clock Selection Register	0x40005a3b

Register Name	Purpose	Address
SC3_BST	Switched Capacitor Boost Clock Selection Register	0x40005a3c
DAC0_SW0	DAC Analog Routing Register 0	0x40005a80
DAC0_SW2	DAC Analog Routing Register 2	0x40005a82
DAC0_SW3	DAC Analog Routing Register 3	0x40005a83
DAC0_SW4	DAC Analog Routing Register 4	0x40005a84
DAC0_STROBE	DAC Strobe Register	0x40005a87
DAC1_SW0	DAC Analog Routing Register 0	0x40005a88
DAC1_SW2	DAC Analog Routing Register 2	0x40005a8a
DAC1_SW3	DAC Analog Routing Register 3	0x40005a8b
DAC1_SW4	DAC Analog Routing Register 4	0x40005a8c
DAC1_STROBE	DAC Strobe Register	0x40005a8f
DAC2_SW0	DAC Analog Routing Register 0	0x40005a90
DAC2_SW2	DAC Analog Routing Register 2	0x40005a92
DAC2_SW3	DAC Analog Routing Register 3	0x40005a93
DAC2_SW4	DAC Analog Routing Register 4	0x40005a94
DAC2_STROBE	DAC Strobe Register	0x40005a97
DAC3_SW0	DAC Analog Routing Register 0	0x40005a98
DAC3_SW2	DAC Analog Routing Register 2	0x40005a9a
DAC3_SW3	DAC Analog Routing Register 3	0x40005a9b
DAC3_SW4	DAC Analog Routing Register 4	0x40005a9c
DAC3_STROBE	DAC Strobe Register	0x40005a9f
CMP0_SW0	Comparator Analog Routing Register 0	0x40005ac0
CMP0_SW2	Comparator Analog Routing Register 2	0x40005ac2
CMP0_SW3	Comparator Analog Routing Register 3	0x40005ac3
CMP0_SW4	Comparator Analog Routing Register 4	0x40005ac4
CMP0_SW6	Comparator Analog Routing Register 6	0x40005ac6
CMP0_CLK	Comparator Clock Control Register	0x40005ac7
CMP1_SW0	Comparator Analog Routing Register 0	0x40005ac8
CMP1_SW2	Comparator Analog Routing Register 2	0x40005aca
CMP1_SW3	Comparator Analog Routing Register 3	0x40005acb
CMP1_SW4	Comparator Analog Routing Register 4	0x40005acc
CMP1_SW6	Comparator Analog Routing Register 6	0x40005ace
CMP1_CLK	Comparator Clock Control Register	0x40005acf
CMP2_SW0	Comparator Analog Routing Register 0	0x40005ad0
CMP2_SW2	Comparator Analog Routing Register 2	0x40005ad2
CMP2_SW3	Comparator Analog Routing Register 3	0x40005ad3
CMP2_SW4	Comparator Analog Routing Register 4	0x40005ad4
CMP2_SW6	Comparator Analog Routing Register 6	0x40005ad6
CMP2_CLK	Comparator Clock Control Register	0x40005ad7
CMP3_SW0	Comparator Analog Routing Register 0	0x40005ad8
CMP3_SW2	Comparator Analog Routing Register 2	0x40005ada
CMP3_SW3	Comparator Analog Routing Register 3	0x40005adb

Register Name	Purpose	Address
CMP3_SW4	Comparator Analog Routing Register 4	0x40005adc
CMP3_SW6	Comparator Analog Routing Register 6	0x40005ade
CMP3_CLK	Comparator Clock Control Register	0x40005adf
DSM0_SW0	Delta Sigma Modulator Analog Routing Register 0	0x40005b00
DSM0_SW2	Delta Sigma Modulator Analog Routing Register 2	0x40005b02
DSM0_SW3	Delta Sigma Modulator Analog Routing Register 3	0x40005b03
DSM0_SW4	Delta Sigma Modulator Analog Routing Register 4	0x40005b04
DSM0_SW6	Delta Sigma Modulator Analog Routing Register 6	0x40005b06
DSM0_CLK	Delta Sigma Modulator Clock Selection Register	0x40005b07
SAR0_SW0	SAR Analog Routing Register 0	0x40005b20
SAR0_SW2	SAR Analog Routing Register 2	0x40005b22
SAR0_SW3	SAR Analog Routing Register 3	0x40005b23
SAR0_SW4	SAR Analog Routing Register 4	0x40005b24
SAR0_SW6	SAR Analog Routing Register 6	0x40005b26
SAR0_CLK	SAR Clock Selection Register	0x40005b27
SAR1_SW0	SAR Analog Routing Register 0	0x40005b28
SAR1_SW2	SAR Analog Routing Register 2	0x40005b2a
SAR1_SW3	SAR Analog Routing Register 3	0x40005b2b
SAR1_SW4	SAR Analog Routing Register 4	0x40005b2c
SAR1_SW6	SAR Analog Routing Register 6	0x40005b2e
SAR1_CLK	SAR Clock Selection Register	0x40005b2f
ABUF0_MX	Analog Buffer Input Selection Register	0x40005b40
ABUF0_SW	Analog Buffer Routing Switch Register	0x40005b41
ABUF1_MX	Analog Buffer Input Selection Register	0x40005b42
ABUF1_SW	Analog Buffer Routing Switch Register	0x40005b43
ABUF2_MX	Analog Buffer Input Selection Register	0x40005b44
ABUF2_SW	Analog Buffer Routing Switch Register	0x40005b45
ABUF3_MX	Analog Buffer Input Selection Register	0x40005b46
ABUF3_SW	Analog Buffer Routing Switch Register	0x40005b47
LCDDAC_SW0	LCDDAC Switch Register 0	0x40005b50
LCDDAC_SW1	LCDDAC Switch Register 1	0x40005b51
LCDDAC_SW2	LCDDAC Switch Register 2	0x40005b52
LCDDAC_SW3	LCDDAC Switch Register 3	0x40005b53
LCDDAC_SW4	LCDDAC Switch Register 3	0x40005b54
SC_MISC	Switched Cap Miscellaneous Control Register	0x40005b56
BUS_SW0	Bus Switch Register 0	0x40005b58
BUS_SW2	Bus Switch Register 2	0x40005b5a
BUS_SW3	Bus Switch Register 3	0x40005b5b
DFT_CR0	DFT Control Register 0	0x40005b5c

Register Name	Purpose	Address
DFT_CR1	DFT Control Register 1	0x40005b5d
DFT_CR2	DFT Control Register 2	0x40005b5e
DFT_CR3	DFT Control Register 3	0x40005b5f
DAC[0..3]_D	DAC Data Register	0x40005b80 + [0..3 * 0x1]
DSM[0..0]_OUT0	DSM Output Register 0	0x40005b88
DSM[0..0]_OUT1	DSM Output Register 1	0x40005b89
SC_SR	Switched Capacitor Status Register	0x40005b8c
SC_MSK	SC IRQ Mask Register	0x40005b8d
LUT_SR	LUT Status Register	0x40005b8e
LUT_MSK	LUT Interrupt ReQuest (IRQ) Mask Register	0x40005b8f
CMP_WRK	Comparator output working register	0x40005b90
CMP_LTRI	Comparator LTRI working register	0x40005b91
TFAULT_WRK0	Timing Fault Working Register 0	0x40005b92
TFAULT_WRK1	Timing Fault Working Register 1	0x40005b93
TFAULT_WRK2	Timing Fault Working Register 2	0x40005b94
TFAULT_WRK3	Timing Fault Working Register 1	0x40005b95
SAR[0..1]_WRK0	SAR working register 0	0x40005ba0 + [0..1 * 0x2]
SAR[0..1]_WRK1	SAR register 1	0x40005ba0 + [0..1 * 0x2] + 0x1
ANAIF_WRK_SARS_SOF	SAR Global Start-of-frame register	0x40005ba8
USB_EP0_DR[0..7]	Control End point EP0 Data Register	0x40006000 + [0..7 * 0x1]
USB_CR0	USB control 0 Register	0x40006008
USB_CR1	USB control 1 Register	0x40006009
USB_SIE_EP_INT_EN	USB SIE Data Endpoints Interrupt Enable Register	0x4000600a
USB_SIE_EP_INT_SR	SIE Data Endpoint Interrupt Status	0x4000600b
USB_SIE_EP1_CNT0	Non-control endpoint count register	0x4000600c
USB_SIE_EP1_CNT1	Non-control endpoint count register	0x4000600d
USB_SIE_EP1_CR0		
USB_USBIO_CR0	USBIO Control 0 Register	0x40006010
USB_USBIO_CR2	USBIO control 2 Register	0x40006011
USB_USBIO_CR1	USBIO control 1 Register	0x40006012
USB_SOF0	Start Of Frame Register	0x40006018
USB_SOF1	Start Of Frame Register	0x40006019
USB_SIE_EP2_CNT0	Non-control endpoint count register	0x4000601c
USB_SIE_EP2_CNT1	Non-control endpoint count register	0x4000601d
USB_SIE_EP2_CR0		
USB_OSCLK_DR0	Oscillator lock data register 0	0x40006020
USB_OSCLK_DR1	Oscillator lock data register 1	0x40006021
USB_EP0_CR	Endpoint0 control Register	0x40006028
USB_EP0_CNT	Endpoint0 count Register	0x40006029
USB_SIE_EP3_CNT0	Non-control endpoint count register	0x4000602c
USB_SIE_EP3_CNT1	Non-control endpoint count register	0x4000602d
USB_SIE_EP3_CR0		

Register Name	Purpose	Address
USB_SIE_EP4_CNT0	Non-control endpoint count register	0x4000603c
USB_SIE_EP4_CNT1	Non-control endpoint count register	0x4000603d
USB_SIE_EP4_CR0		
USB_SIE_EP5_CNT0	Non-control endpoint count register	0x4000604c
USB_SIE_EP5_CNT1	Non-control endpoint count register	0x4000604d
USB_SIE_EP5_CR0		
USB_SIE_EP6_CNT0	Non-control endpoint count register	0x4000605c
USB_SIE_EP6_CNT1	Non-control endpoint count register	0x4000605d
USB_SIE_EP6_CR0		
USB_SIE_EP7_CNT0	Non-control endpoint count register	0x4000606c
USB_SIE_EP7_CNT1	Non-control endpoint count register	0x4000606d
USB_SIE_EP7_CR0		
USB_SIE_EP8_CNT0	Non-control endpoint count register	0x4000607c
USB_SIE_EP8_CNT1	Non-control endpoint count register	0x4000607d
USB_SIE_EP8_CR0		
USB_ARB_EP1_CFG	Endpoint Configuration Register	0x40006080
USB_ARB_EP1_INT_EN	Endpoint Interrupt Enable Register	0x40006081
USB_ARB_EP1_SR	Endpoint Status Register	0x40006082
USB_ARB_RW1_WA	Endpoint Write Address value	0x40006084
USB_ARB_RW1_WA_MSB	Endpoint Write Address value	0x40006085
USB_ARB_RW1_RA	Endpoint Read Address value	0x40006086
USB_ARB_RW1_RA_MSB	Endpoint Read Address value	0x40006087
USB_ARB_RW1_DR	Endpoint Data Register	0x40006088
USB_BUF_SIZE	Dedicated Endpoint Buffer Size Register	0x4000608c
USB_EP_ACTIVE	Endpoint Active Indication Register	0x4000608e
USB_EP_TYPE	Endpoint Type (IN/OUT) Indication	0x4000608f
USB_ARB_EP2_CFG	Endpoint Configuration Register	0x40006090
USB_ARB_EP2_INT_EN	Endpoint Interrupt Enable Register	0x40006091
USB_ARB_EP2_SR	Endpoint Status Register	0x40006092
USB_ARB_RW2_WA	Endpoint Write Address value	0x40006094
USB_ARB_RW2_WA_MSB	Endpoint Write Address value	0x40006095
USB_ARB_RW2_RA	Endpoint Read Address value	0x40006096
USB_ARB_RW2_RA_MSB	Endpoint Read Address value	0x40006097
USB_ARB_RW2_DR	Endpoint Data Register	0x40006098
USB_ARB_CFG	Arbiter Configuration Register	0x4000609c
USB_USB_CLK_EN	USB Block Clock Enable Register	0x4000609d
USB_ARB_INT_EN	Arbiter Interrupt Enable	0x4000609e
USB_ARB_INT_SR	Arbiter Interrupt Status	0x4000609f
USB_ARB_EP3_CFG	Endpoint Configuration Register	0x400060a0
USB_ARB_EP3_INT_EN	Endpoint Interrupt Enable Register	0x400060a1
USB_ARB_EP3_SR	Endpoint Status Register	0x400060a2
USB_ARB_RW3_WA	Endpoint Write Address value	0x400060a4

Register Name	Purpose	Address
USB_ARB_RW3_WA_MSB	Endpoint Write Address value	0x400060a5
USB_ARB_RW3_RA	Endpoint Read Address value	0x400060a6
USB_ARB_RW3_RA_MSB	Endpoint Read Address value	0x400060a7
USB_ARB_RW3_DR	Endpoint Data Register	0x400060a8
USB_CWA	Common Area Write Address	0x400060ac
USB_CWA_MSB	Common Area Write Address	0x400060ad
USB_ARB_EP4_CFG	Endpoint Configuration Register	0x400060b0
USB_ARB_EP4_INT_EN	Endpoint Interrupt Enable Register	0x400060b1
USB_ARB_EP4_SR	Endpoint Status Register	0x400060b2
USB_ARB_RW4_WA	Endpoint Write Address value	0x400060b4
USB_ARB_RW4_WA_MSB	Endpoint Write Address value	0x400060b5
USB_ARB_RW4_RA	Endpoint Read Address value	0x400060b6
USB_ARB_RW4_RA_MSB	Endpoint Read Address value	0x400060b7
USB_ARB_RW4_DR	Endpoint Data Register	0x400060b8
USB_DMA_THRES	DMA Burst / Threshold Configuration	0x400060bc
USB_DMA_THRES_MSB	DMA Burst / Threshold Configuration	0x400060bd
USB_ARB_EP5_CFG	Endpoint Configuration Register	0x400060c0
USB_ARB_EP5_INT_EN	Endpoint Interrupt Enable Register	0x400060c1
USB_ARB_EP5_SR	Endpoint Status Register	0x400060c2
USB_ARB_RW5_WA	Endpoint Write Address value	0x400060c4
USB_ARB_RW5_WA_MSB	Endpoint Write Address value	0x400060c5
USB_ARB_RW5_RA	Endpoint Read Address value	0x400060c6
USB_ARB_RW5_RA_MSB	Endpoint Read Address value	0x400060c7
USB_ARB_RW5_DR	Endpoint Data Register	0x400060c8
USB_BUS_RST_CNT	Bus Reset Count Register	0x400060cc
USB_ARB_EP6_CFG	Endpoint Configuration Register	0x400060d0
USB_ARB_EP6_INT_EN	Endpoint Interrupt Enable Register	0x400060d1
USB_ARB_EP6_SR	Endpoint Status Register	0x400060d2
USB_ARB_RW6_WA	Endpoint Write Address value	0x400060d4
USB_ARB_RW6_WA_MSB	Endpoint Write Address value	0x400060d5
USB_ARB_RW6_RA	Endpoint Read Address value	0x400060d6
USB_ARB_RW6_RA_MSB	Endpoint Read Address value	0x400060d7
USB_ARB_RW6_DR	Endpoint Data Register	0x400060d8
USB_ARB_EP7_CFG	Endpoint Configuration Register	0x400060e0
USB_ARB_EP7_INT_EN	Endpoint Interrupt Enable Register	0x400060e1
USB_ARB_EP7_SR	Endpoint Status Register	0x400060e2
USB_ARB_RW7_WA	Endpoint Write Address value	0x400060e4
USB_ARB_RW7_WA_MSB	Endpoint Write Address value	0x400060e5
USB_ARB_RW7_RA	Endpoint Read Address value	0x400060e6
USB_ARB_RW7_RA_MSB	Endpoint Read Address value	0x400060e7
USB_ARB_RW7_DR	Endpoint Data Register	0x400060e8
USB_ARB_EP8_CFG	Endpoint Configuration Register	0x400060f0

Register Name	Purpose	Address
USB_ARB_EP8_INT_EN	Endpoint Interrupt Enable Register	0x400060f1
USB_ARB_EP8_SR	Endpoint Status Register	0x400060f2
USB_ARB_RW8_WA	Endpoint Write Address value	0x400060f4
USB_ARB_RW8_WA_MSB	Endpoint Write Address value	0x400060f5
USB_ARB_RW8_RA	Endpoint Read Address value	0x400060f6
USB_ARB_RW8_RA_MSB	Endpoint Read Address value	0x400060f7
USB_ARB_RW8_DR	Endpoint Data Register	0x400060f8
B[0..3]_UDB00_A0	UDB00_A0	0x40006400 + [0..3 * 0x100]
B[0..3]_UDB01_A0	UDB01_A0	0x40006400 + [0..3 * 0x100] + 0x1
B[0..3]_UDB02_A0	UDB02_A0	0x40006400 + [0..3 * 0x100] + 0x2
B[0..3]_UDB03_A0	UDB03_A0	0x40006400 + [0..3 * 0x100] + 0x3
B[0..3]_UDB04_A0	UDB04_A0	0x40006400 + [0..3 * 0x100] + 0x4
B[0..3]_UDB05_A0	UDB05_A0	0x40006400 + [0..3 * 0x100] + 0x5
B[0..3]_UDB06_A0	UDB06_A0	0x40006400 + [0..3 * 0x100] + 0x6
B[0..3]_UDB07_A0	UDB07_A0	0x40006400 + [0..3 * 0x100] + 0x7
B[0..3]_UDB08_A0	UDB08_A0	0x40006400 + [0..3 * 0x100] + 0x8
B[0..3]_UDB09_A0	UDB09_A0	0x40006400 + [0..3 * 0x100] + 0x9
B[0..3]_UDB10_A0	UDB10_A0	0x40006400 + [0..3 * 0x100] + 0xa
B[0..3]_UDB11_A0	UDB11_A0	0x40006400 + [0..3 * 0x100] + 0xb
B[0..3]_UDB12_A0	UDB12_A0	0x40006400 + [0..3 * 0x100] + 0xc
B[0..3]_UDB13_A0	UDB13_A0	0x40006400 + [0..3 * 0x100] + 0xd
B[0..3]_UDB14_A0	UDB14_A0	0x40006400 + [0..3 * 0x100] + 0xe
B[0..3]_UDB15_A0	UDB15_A0	0x40006400 + [0..3 * 0x100] + 0xf
B[0..3]_UDB00_A1	UDB00_A1	0x40006400 + [0..3 * 0x100] + 0x10
B[0..3]_UDB01_A1	UDB01_A1	0x40006400 + [0..3 * 0x100] + 0x11
B[0..3]_UDB02_A1	UDB02_A1	0x40006400 + [0..3 * 0x100] + 0x12
B[0..3]_UDB03_A1	UDB03_A1	0x40006400 + [0..3 * 0x100] + 0x13
B[0..3]_UDB04_A1	UDB04_A1	0x40006400 + [0..3 * 0x100] + 0x14
B[0..3]_UDB05_A1	UDB05_A1	0x40006400 + [0..3 * 0x100] + 0x15
B[0..3]_UDB06_A1	UDB06_A1	0x40006400 + [0..3 * 0x100] + 0x16
B[0..3]_UDB07_A1	UDB07_A1	0x40006400 + [0..3 * 0x100] + 0x17
B[0..3]_UDB08_A1	UDB08_A1	0x40006400 + [0..3 * 0x100] + 0x18
B[0..3]_UDB09_A1	UDB09_A1	0x40006400 + [0..3 * 0x100] + 0x19
B[0..3]_UDB10_A1	UDB10_A1	0x40006400 + [0..3 * 0x100] + 0x1a
B[0..3]_UDB11_A1	UDB11_A1	0x40006400 + [0..3 * 0x100] + 0x1b
B[0..3]_UDB12_A1	UDB12_A1	0x40006400 + [0..3 * 0x100] + 0x1c
B[0..3]_UDB13_A1	UDB13_A1	0x40006400 + [0..3 * 0x100] + 0x1d
B[0..3]_UDB14_A1	UDB14_A1	0x40006400 + [0..3 * 0x100] + 0x1e
B[0..3]_UDB15_A1	UDB15_A1	0x40006400 + [0..3 * 0x100] + 0x1f
B[0..3]_UDB00_D0	UDB00_D0	0x40006400 + [0..3 * 0x100] + 0x20
B[0..3]_UDB01_D0	UDB01_D0	0x40006400 + [0..3 * 0x100] + 0x21
B[0..3]_UDB02_D0	UDB02_D0	0x40006400 + [0..3 * 0x100] + 0x22

Register Name	Purpose	Address
B[0..3]_UDB03_D0	UDB03_D0	0x40006400 + [0..3 * 0x100] + 0x23
B[0..3]_UDB04_D0	UDB04_D0	0x40006400 + [0..3 * 0x100] + 0x24
B[0..3]_UDB05_D0	UDB05_D0	0x40006400 + [0..3 * 0x100] + 0x25
B[0..3]_UDB06_D0	UDB06_D0	0x40006400 + [0..3 * 0x100] + 0x26
B[0..3]_UDB07_D0	UDB07_D0	0x40006400 + [0..3 * 0x100] + 0x27
B[0..3]_UDB08_D0	UDB08_D0	0x40006400 + [0..3 * 0x100] + 0x28
B[0..3]_UDB09_D0	UDB09_D0	0x40006400 + [0..3 * 0x100] + 0x29
B[0..3]_UDB10_D0	UDB10_D0	0x40006400 + [0..3 * 0x100] + 0x2a
B[0..3]_UDB11_D0	UDB11_D0	0x40006400 + [0..3 * 0x100] + 0x2b
B[0..3]_UDB12_D0	UDB12_D0	0x40006400 + [0..3 * 0x100] + 0x2c
B[0..3]_UDB13_D0	UDB13_D0	0x40006400 + [0..3 * 0x100] + 0x2d
B[0..3]_UDB14_D0	UDB14_D0	0x40006400 + [0..3 * 0x100] + 0x2e
B[0..3]_UDB15_D0	UDB15_D0	0x40006400 + [0..3 * 0x100] + 0x2f
B[0..3]_UDB00_D1	UDB00_D1	0x40006400 + [0..3 * 0x100] + 0x30
B[0..3]_UDB01_D1	UDB01_D1	0x40006400 + [0..3 * 0x100] + 0x31
B[0..3]_UDB02_D1	UDB02_D1	0x40006400 + [0..3 * 0x100] + 0x32
B[0..3]_UDB03_D1	UDB03_D1	0x40006400 + [0..3 * 0x100] + 0x33
B[0..3]_UDB04_D1	UDB04_D1	0x40006400 + [0..3 * 0x100] + 0x34
B[0..3]_UDB05_D1	UDB05_D1	0x40006400 + [0..3 * 0x100] + 0x35
B[0..3]_UDB06_D1	UDB06_D1	0x40006400 + [0..3 * 0x100] + 0x36
B[0..3]_UDB07_D1	UDB07_D1	0x40006400 + [0..3 * 0x100] + 0x37
B[0..3]_UDB08_D1	UDB08_D1	0x40006400 + [0..3 * 0x100] + 0x38
B[0..3]_UDB09_D1	UDB09_D1	0x40006400 + [0..3 * 0x100] + 0x39
B[0..3]_UDB10_D1	UDB10_D1	0x40006400 + [0..3 * 0x100] + 0x3a
B[0..3]_UDB11_D1	UDB11_D1	0x40006400 + [0..3 * 0x100] + 0x3b
B[0..3]_UDB12_D1	UDB12_D1	0x40006400 + [0..3 * 0x100] + 0x3c
B[0..3]_UDB13_D1	UDB13_D1	0x40006400 + [0..3 * 0x100] + 0x3d
B[0..3]_UDB14_D1	UDB14_D1	0x40006400 + [0..3 * 0x100] + 0x3e
B[0..3]_UDB15_D1	UDB15_D1	0x40006400 + [0..3 * 0x100] + 0x3f
B[0..3]_UDB00_F0	UDB00_F0	0x40006400 + [0..3 * 0x100] + 0x40
B[0..3]_UDB01_F0	UDB01_F0	0x40006400 + [0..3 * 0x100] + 0x41
B[0..3]_UDB02_F0	UDB02_F0	0x40006400 + [0..3 * 0x100] + 0x42
B[0..3]_UDB03_F0	UDB03_F0	0x40006400 + [0..3 * 0x100] + 0x43
B[0..3]_UDB04_F0	UDB04_F0	0x40006400 + [0..3 * 0x100] + 0x44
B[0..3]_UDB05_F0	UDB05_F0	0x40006400 + [0..3 * 0x100] + 0x45
B[0..3]_UDB06_F0	UDB06_F0	0x40006400 + [0..3 * 0x100] + 0x46
B[0..3]_UDB07_F0	UDB07_F0	0x40006400 + [0..3 * 0x100] + 0x47
B[0..3]_UDB08_F0	UDB08_F0	0x40006400 + [0..3 * 0x100] + 0x48
B[0..3]_UDB09_F0	UDB09_F0	0x40006400 + [0..3 * 0x100] + 0x49
B[0..3]_UDB10_F0	UDB10_F0	0x40006400 + [0..3 * 0x100] + 0x4a
B[0..3]_UDB11_F0	UDB11_F0	0x40006400 + [0..3 * 0x100] + 0x4b
B[0..3]_UDB12_F0	UDB12_F0	0x40006400 + [0..3 * 0x100] + 0x4c

Register Name	Purpose	Address
B[0..3]_UDB13_F0	UDB13_F0	0x40006400 + [0..3 * 0x100] + 0x4d
B[0..3]_UDB14_F0	UDB14_F0	0x40006400 + [0..3 * 0x100] + 0x4e
B[0..3]_UDB15_F0	UDB15_F0	0x40006400 + [0..3 * 0x100] + 0x4f
B[0..3]_UDB00_F1	UDB00_F1	0x40006400 + [0..3 * 0x100] + 0x50
B[0..3]_UDB01_F1	UDB01_F1	0x40006400 + [0..3 * 0x100] + 0x51
B[0..3]_UDB02_F1	UDB02_F1	0x40006400 + [0..3 * 0x100] + 0x52
B[0..3]_UDB03_F1	UDB03_F1	0x40006400 + [0..3 * 0x100] + 0x53
B[0..3]_UDB04_F1	UDB04_F1	0x40006400 + [0..3 * 0x100] + 0x54
B[0..3]_UDB05_F1	UDB05_F1	0x40006400 + [0..3 * 0x100] + 0x55
B[0..3]_UDB06_F1	UDB06_F1	0x40006400 + [0..3 * 0x100] + 0x56
B[0..3]_UDB07_F1	UDB07_F1	0x40006400 + [0..3 * 0x100] + 0x57
B[0..3]_UDB08_F1	UDB08_F1	0x40006400 + [0..3 * 0x100] + 0x58
B[0..3]_UDB09_F1	UDB09_F1	0x40006400 + [0..3 * 0x100] + 0x59
B[0..3]_UDB10_F1	UDB10_F1	0x40006400 + [0..3 * 0x100] + 0x5a
B[0..3]_UDB11_F1	UDB11_F1	0x40006400 + [0..3 * 0x100] + 0x5b
B[0..3]_UDB12_F1	UDB12_F1	0x40006400 + [0..3 * 0x100] + 0x5c
B[0..3]_UDB13_F1	UDB13_F1	0x40006400 + [0..3 * 0x100] + 0x5d
B[0..3]_UDB14_F1	UDB14_F1	0x40006400 + [0..3 * 0x100] + 0x5e
B[0..3]_UDB15_F1	UDB15_F1	0x40006400 + [0..3 * 0x100] + 0x5f
B[0..3]_UDB00_ST	UDB00_ST	0x40006400 + [0..3 * 0x100] + 0x60
B[0..3]_UDB01_ST	UDB01_ST	0x40006400 + [0..3 * 0x100] + 0x61
B[0..3]_UDB02_ST	UDB02_ST	0x40006400 + [0..3 * 0x100] + 0x62
B[0..3]_UDB03_ST	UDB03_ST	0x40006400 + [0..3 * 0x100] + 0x63
B[0..3]_UDB04_ST	UDB04_ST	0x40006400 + [0..3 * 0x100] + 0x64
B[0..3]_UDB05_ST	UDB05_ST	0x40006400 + [0..3 * 0x100] + 0x65
B[0..3]_UDB06_ST	UDB06_ST	0x40006400 + [0..3 * 0x100] + 0x66
B[0..3]_UDB07_ST	UDB07_ST	0x40006400 + [0..3 * 0x100] + 0x67
B[0..3]_UDB08_ST	UDB08_ST	0x40006400 + [0..3 * 0x100] + 0x68
B[0..3]_UDB09_ST	UDB09_ST	0x40006400 + [0..3 * 0x100] + 0x69
B[0..3]_UDB10_ST	UDB10_ST	0x40006400 + [0..3 * 0x100] + 0x6a
B[0..3]_UDB11_ST	UDB11_ST	0x40006400 + [0..3 * 0x100] + 0x6b
B[0..3]_UDB12_ST	UDB12_ST	0x40006400 + [0..3 * 0x100] + 0x6c
B[0..3]_UDB13_ST	UDB13_ST	0x40006400 + [0..3 * 0x100] + 0x6d
B[0..3]_UDB14_ST	UDB14_ST	0x40006400 + [0..3 * 0x100] + 0x6e
B[0..3]_UDB15_ST	UDB15_ST	0x40006400 + [0..3 * 0x100] + 0x6f
B[0..3]_UDB00_CTL	UDB00_CTL	0x40006400 + [0..3 * 0x100] + 0x70
B[0..3]_UDB01_CTL	UDB01_CTL	0x40006400 + [0..3 * 0x100] + 0x71
B[0..3]_UDB02_CTL	UDB02_CTL	0x40006400 + [0..3 * 0x100] + 0x72
B[0..3]_UDB03_CTL	UDB03_CTL	0x40006400 + [0..3 * 0x100] + 0x73
B[0..3]_UDB04_CTL	UDB04_CTL	0x40006400 + [0..3 * 0x100] + 0x74
B[0..3]_UDB05_CTL	UDB05_CTL	0x40006400 + [0..3 * 0x100] + 0x75
B[0..3]_UDB06_CTL	UDB06_CTL	0x40006400 + [0..3 * 0x100] + 0x76

Register Name	Purpose	Address
B[0..3]_UDB07_CTL	UDB07_CTL	0x40006400 + [0..3 * 0x100] + 0x77
B[0..3]_UDB08_CTL	UDB08_CTL	0x40006400 + [0..3 * 0x100] + 0x78
B[0..3]_UDB09_CTL	UDB09_CTL	0x40006400 + [0..3 * 0x100] + 0x79
B[0..3]_UDB10_CTL	UDB10_CTL	0x40006400 + [0..3 * 0x100] + 0x7a
B[0..3]_UDB11_CTL	UDB11_CTL	0x40006400 + [0..3 * 0x100] + 0x7b
B[0..3]_UDB12_CTL	UDB12_CTL	0x40006400 + [0..3 * 0x100] + 0x7c
B[0..3]_UDB13_CTL	UDB13_CTL	0x40006400 + [0..3 * 0x100] + 0x7d
B[0..3]_UDB14_CTL	UDB14_CTL	0x40006400 + [0..3 * 0x100] + 0x7e
B[0..3]_UDB15_CTL	UDB15_CTL	0x40006400 + [0..3 * 0x100] + 0x7f
B[0..3]_UDB00_MSK	UDB00_MSK	0x40006400 + [0..3 * 0x100] + 0x80
B[0..3]_UDB01_MSK	UDB01_MSK	0x40006400 + [0..3 * 0x100] + 0x81
B[0..3]_UDB02_MSK	UDB02_MSK	0x40006400 + [0..3 * 0x100] + 0x82
B[0..3]_UDB03_MSK	UDB03_MSK	0x40006400 + [0..3 * 0x100] + 0x83
B[0..3]_UDB04_MSK	UDB04_MSK	0x40006400 + [0..3 * 0x100] + 0x84
B[0..3]_UDB05_MSK	UDB05_MSK	0x40006400 + [0..3 * 0x100] + 0x85
B[0..3]_UDB06_MSK	UDB06_MSK	0x40006400 + [0..3 * 0x100] + 0x86
B[0..3]_UDB07_MSK	UDB07_MSK	0x40006400 + [0..3 * 0x100] + 0x87
B[0..3]_UDB08_MSK	UDB08_MSK	0x40006400 + [0..3 * 0x100] + 0x88
B[0..3]_UDB09_MSK	UDB09_MSK	0x40006400 + [0..3 * 0x100] + 0x89
B[0..3]_UDB10_MSK	UDB10_MSK	0x40006400 + [0..3 * 0x100] + 0x8a
B[0..3]_UDB11_MSK	UDB11_MSK	0x40006400 + [0..3 * 0x100] + 0x8b
B[0..3]_UDB12_MSK	UDB12_MSK	0x40006400 + [0..3 * 0x100] + 0x8c
B[0..3]_UDB13_MSK	UDB13_MSK	0x40006400 + [0..3 * 0x100] + 0x8d
B[0..3]_UDB14_MSK	UDB14_MSK	0x40006400 + [0..3 * 0x100] + 0x8e
B[0..3]_UDB15_MSK	UDB15_MSK	0x40006400 + [0..3 * 0x100] + 0x8f
B[0..3]_UDB00_ACTL	UDB00_ACTL	0x40006400 + [0..3 * 0x100] + 0x90
B[0..3]_UDB01_ACTL	UDB01_ACTL	0x40006400 + [0..3 * 0x100] + 0x91
B[0..3]_UDB02_ACTL	UDB02_ACTL	0x40006400 + [0..3 * 0x100] + 0x92
B[0..3]_UDB03_ACTL	UDB03_ACTL	0x40006400 + [0..3 * 0x100] + 0x93
B[0..3]_UDB04_ACTL	UDB04_ACTL	0x40006400 + [0..3 * 0x100] + 0x94
B[0..3]_UDB05_ACTL	UDB05_ACTL	0x40006400 + [0..3 * 0x100] + 0x95
B[0..3]_UDB06_ACTL	UDB06_ACTL	0x40006400 + [0..3 * 0x100] + 0x96
B[0..3]_UDB07_ACTL	UDB07_ACTL	0x40006400 + [0..3 * 0x100] + 0x97
B[0..3]_UDB08_ACTL	UDB08_ACTL	0x40006400 + [0..3 * 0x100] + 0x98
B[0..3]_UDB09_ACTL	UDB09_ACTL	0x40006400 + [0..3 * 0x100] + 0x99
B[0..3]_UDB10_ACTL	UDB10_ACTL	0x40006400 + [0..3 * 0x100] + 0x9a
B[0..3]_UDB11_ACTL	UDB11_ACTL	0x40006400 + [0..3 * 0x100] + 0x9b
B[0..3]_UDB12_ACTL	UDB12_ACTL	0x40006400 + [0..3 * 0x100] + 0x9c
B[0..3]_UDB13_ACTL	UDB13_ACTL	0x40006400 + [0..3 * 0x100] + 0x9d
B[0..3]_UDB14_ACTL	UDB14_ACTL	0x40006400 + [0..3 * 0x100] + 0x9e
B[0..3]_UDB15_ACTL	UDB15_ACTL	0x40006400 + [0..3 * 0x100] + 0x9f
B[0..3]_UDB00_MC	UDB00_MC	0x40006400 + [0..3 * 0x100] + 0xa0

Register Name	Purpose	Address
B[0..3]_UDB01_MC	UDB01_MC	0x40006400 + [0..3 * 0x100] + 0xa1
B[0..3]_UDB02_MC	UDB02_MC	0x40006400 + [0..3 * 0x100] + 0xa2
B[0..3]_UDB03_MC	UDB03_MC	0x40006400 + [0..3 * 0x100] + 0xa3
B[0..3]_UDB04_MC	UDB04_MC	0x40006400 + [0..3 * 0x100] + 0xa4
B[0..3]_UDB05_MC	UDB05_MC	0x40006400 + [0..3 * 0x100] + 0xa5
B[0..3]_UDB06_MC	UDB06_MC	0x40006400 + [0..3 * 0x100] + 0xa6
B[0..3]_UDB07_MC	UDB07_MC	0x40006400 + [0..3 * 0x100] + 0xa7
B[0..3]_UDB08_MC	UDB08_MC	0x40006400 + [0..3 * 0x100] + 0xa8
B[0..3]_UDB09_MC	UDB09_MC	0x40006400 + [0..3 * 0x100] + 0xa9
B[0..3]_UDB10_MC	UDB10_MC	0x40006400 + [0..3 * 0x100] + 0xaa
B[0..3]_UDB11_MC	UDB11_MC	0x40006400 + [0..3 * 0x100] + 0xab
B[0..3]_UDB12_MC	UDB12_MC	0x40006400 + [0..3 * 0x100] + 0xac
B[0..3]_UDB13_MC	UDB13_MC	0x40006400 + [0..3 * 0x100] + 0xad
B[0..3]_UDB14_MC	UDB14_MC	0x40006400 + [0..3 * 0x100] + 0xae
B[0..3]_UDB15_MC	UDB15_MC	0x40006400 + [0..3 * 0x100] + 0xaf
B[0..3]_UDB00_01_A0	UDB00_01_A0	0x40006800 + [0..3 * 0x200]
B[0..3]_UDB01_02_A0	UDB01_02_A0	0x40006800 + [0..3 * 0x200] + 0x2
B[0..3]_UDB02_03_A0	UDB02_03_A0	0x40006800 + [0..3 * 0x200] + 0x4
B[0..3]_UDB03_04_A0	UDB03_04_A0	0x40006800 + [0..3 * 0x200] + 0x6
B[0..3]_UDB04_05_A0	UDB04_05_A0	0x40006800 + [0..3 * 0x200] + 0x8
B[0..3]_UDB05_06_A0	UDB05_06_A0	0x40006800 + [0..3 * 0x200] + 0xa
B[0..3]_UDB06_07_A0	UDB06_07_A0	0x40006800 + [0..3 * 0x200] + 0xc
B[0..3]_UDB07_08_A0	UDB07_08_A0	0x40006800 + [0..3 * 0x200] + 0xe
B[0..3]_UDB08_09_A0	UDB08_09_A0	0x40006800 + [0..3 * 0x200] + 0x10
B[0..3]_UDB09_10_A0	UDB09_10_A0	0x40006800 + [0..3 * 0x200] + 0x12
B[0..3]_UDB10_11_A0	UDB10_11_A0	0x40006800 + [0..3 * 0x200] + 0x14
B[0..3]_UDB11_12_A0	UDB11_12_A0	0x40006800 + [0..3 * 0x200] + 0x16
B[0..3]_UDB12_13_A0	UDB12_13_A0	0x40006800 + [0..3 * 0x200] + 0x18
B[0..3]_UDB13_14_A0	UDB13_14_A0	0x40006800 + [0..3 * 0x200] + 0x1a
B[0..3]_UDB14_15_A0	UDB14_15_A0	0x40006800 + [0..3 * 0x200] + 0x1c
B[0..3]_UDB00_01_A1	UDB00_01_A1	0x40006800 + [0..3 * 0x200] + 0x20
B[0..3]_UDB01_02_A1	UDB01_02_A1	0x40006800 + [0..3 * 0x200] + 0x22
B[0..3]_UDB02_03_A1	UDB02_03_A1	0x40006800 + [0..3 * 0x200] + 0x24
B[0..3]_UDB03_04_A1	UDB03_04_A1	0x40006800 + [0..3 * 0x200] + 0x26
B[0..3]_UDB04_05_A1	UDB04_05_A1	0x40006800 + [0..3 * 0x200] + 0x28
B[0..3]_UDB05_06_A1	UDB05_06_A1	0x40006800 + [0..3 * 0x200] + 0x2a
B[0..3]_UDB06_07_A1	UDB06_07_A1	0x40006800 + [0..3 * 0x200] + 0x2c
B[0..3]_UDB07_08_A1	UDB07_08_A1	0x40006800 + [0..3 * 0x200] + 0x2e
B[0..3]_UDB08_09_A1	UDB08_09_A1	0x40006800 + [0..3 * 0x200] + 0x30
B[0..3]_UDB09_10_A1	UDB09_10_A1	0x40006800 + [0..3 * 0x200] + 0x32
B[0..3]_UDB10_11_A1	UDB10_11_A1	0x40006800 + [0..3 * 0x200] + 0x34
B[0..3]_UDB11_12_A1	UDB11_12_A1	0x40006800 + [0..3 * 0x200] + 0x36

Register Name	Purpose	Address
B[0..3]_UDB12_13_A1	UDB12_13_A1	0x40006800 + [0..3 * 0x200] + 0x38
B[0..3]_UDB13_14_A1	UDB13_14_A1	0x40006800 + [0..3 * 0x200] + 0x3a
B[0..3]_UDB14_15_A1	UDB14_15_A1	0x40006800 + [0..3 * 0x200] + 0x3c
B[0..3]_UDB00_01_D0	UDB00_01_D0	0x40006800 + [0..3 * 0x200] + 0x40
B[0..3]_UDB01_02_D0	UDB01_02_D0	0x40006800 + [0..3 * 0x200] + 0x42
B[0..3]_UDB02_03_D0	UDB02_03_D0	0x40006800 + [0..3 * 0x200] + 0x44
B[0..3]_UDB03_04_D0	UDB03_04_D0	0x40006800 + [0..3 * 0x200] + 0x46
B[0..3]_UDB04_05_D0	UDB04_05_D0	0x40006800 + [0..3 * 0x200] + 0x48
B[0..3]_UDB05_06_D0	UDB05_06_D0	0x40006800 + [0..3 * 0x200] + 0x4a
B[0..3]_UDB06_07_D0	UDB06_07_D0	0x40006800 + [0..3 * 0x200] + 0x4c
B[0..3]_UDB07_08_D0	UDB07_08_D0	0x40006800 + [0..3 * 0x200] + 0x4e
B[0..3]_UDB08_09_D0	UDB08_09_D0	0x40006800 + [0..3 * 0x200] + 0x50
B[0..3]_UDB09_10_D0	UDB09_10_D0	0x40006800 + [0..3 * 0x200] + 0x52
B[0..3]_UDB10_11_D0	UDB10_11_D0	0x40006800 + [0..3 * 0x200] + 0x54
B[0..3]_UDB11_12_D0	UDB11_12_D0	0x40006800 + [0..3 * 0x200] + 0x56
B[0..3]_UDB12_13_D0	UDB12_13_D0	0x40006800 + [0..3 * 0x200] + 0x58
B[0..3]_UDB13_14_D0	UDB13_14_D0	0x40006800 + [0..3 * 0x200] + 0x5a
B[0..3]_UDB14_15_D0	UDB14_15_D0	0x40006800 + [0..3 * 0x200] + 0x5c
B[0..3]_UDB00_01_D1	UDB00_01_D1	0x40006800 + [0..3 * 0x200] + 0x60
B[0..3]_UDB01_02_D1	UDB01_02_D1	0x40006800 + [0..3 * 0x200] + 0x62
B[0..3]_UDB02_03_D1	UDB02_03_D1	0x40006800 + [0..3 * 0x200] + 0x64
B[0..3]_UDB03_04_D1	UDB03_04_D1	0x40006800 + [0..3 * 0x200] + 0x66
B[0..3]_UDB04_05_D1	UDB04_05_D1	0x40006800 + [0..3 * 0x200] + 0x68
B[0..3]_UDB05_06_D1	UDB05_06_D1	0x40006800 + [0..3 * 0x200] + 0x6a
B[0..3]_UDB06_07_D1	UDB06_07_D1	0x40006800 + [0..3 * 0x200] + 0x6c
B[0..3]_UDB07_08_D1	UDB07_08_D1	0x40006800 + [0..3 * 0x200] + 0x6e
B[0..3]_UDB08_09_D1	UDB08_09_D1	0x40006800 + [0..3 * 0x200] + 0x70
B[0..3]_UDB09_10_D1	UDB09_10_D1	0x40006800 + [0..3 * 0x200] + 0x72
B[0..3]_UDB10_11_D1	UDB10_11_D1	0x40006800 + [0..3 * 0x200] + 0x74
B[0..3]_UDB11_12_D1	UDB11_12_D1	0x40006800 + [0..3 * 0x200] + 0x76
B[0..3]_UDB12_13_D1	UDB12_13_D1	0x40006800 + [0..3 * 0x200] + 0x78
B[0..3]_UDB13_14_D1	UDB13_14_D1	0x40006800 + [0..3 * 0x200] + 0x7a
B[0..3]_UDB14_15_D1	UDB14_15_D1	0x40006800 + [0..3 * 0x200] + 0x7c
B[0..3]_UDB00_01_F0	UDB00_01_F0	0x40006800 + [0..3 * 0x200] + 0x80
B[0..3]_UDB01_02_F0	UDB01_02_F0	0x40006800 + [0..3 * 0x200] + 0x82
B[0..3]_UDB02_03_F0	UDB02_03_F0	0x40006800 + [0..3 * 0x200] + 0x84
B[0..3]_UDB03_04_F0	UDB03_04_F0	0x40006800 + [0..3 * 0x200] + 0x86
B[0..3]_UDB04_05_F0	UDB04_05_F0	0x40006800 + [0..3 * 0x200] + 0x88
B[0..3]_UDB05_06_F0	UDB05_06_F0	0x40006800 + [0..3 * 0x200] + 0x8a
B[0..3]_UDB06_07_F0	UDB06_07_F0	0x40006800 + [0..3 * 0x200] + 0x8c
B[0..3]_UDB07_08_F0	UDB07_08_F0	0x40006800 + [0..3 * 0x200] + 0x8e
B[0..3]_UDB08_09_F0	UDB08_09_F0	0x40006800 + [0..3 * 0x200] + 0x90

Register Name	Purpose	Address
B[0..3]_UDB09_10_F0	UDB09_10_F0	0x40006800 + [0..3 * 0x200] + 0x92
B[0..3]_UDB10_11_F0	UDB10_11_F0	0x40006800 + [0..3 * 0x200] + 0x94
B[0..3]_UDB11_12_F0	UDB11_12_F0	0x40006800 + [0..3 * 0x200] + 0x96
B[0..3]_UDB12_13_F0	UDB12_13_F0	0x40006800 + [0..3 * 0x200] + 0x98
B[0..3]_UDB13_14_F0	UDB13_14_F0	0x40006800 + [0..3 * 0x200] + 0x9a
B[0..3]_UDB14_15_F0	UDB14_15_F0	0x40006800 + [0..3 * 0x200] + 0x9c
B[0..3]_UDB00_01_F1	UDB00_01_F1	0x40006800 + [0..3 * 0x200] + 0xa0
B[0..3]_UDB01_02_F1	UDB01_02_F1	0x40006800 + [0..3 * 0x200] + 0xa2
B[0..3]_UDB02_03_F1	UDB02_03_F1	0x40006800 + [0..3 * 0x200] + 0xa4
B[0..3]_UDB03_04_F1	UDB03_04_F1	0x40006800 + [0..3 * 0x200] + 0xa6
B[0..3]_UDB04_05_F1	UDB04_05_F1	0x40006800 + [0..3 * 0x200] + 0xa8
B[0..3]_UDB05_06_F1	UDB05_06_F1	0x40006800 + [0..3 * 0x200] + 0xaa
B[0..3]_UDB06_07_F1	UDB06_07_F1	0x40006800 + [0..3 * 0x200] + 0xac
B[0..3]_UDB07_08_F1	UDB07_08_F1	0x40006800 + [0..3 * 0x200] + 0xae
B[0..3]_UDB08_09_F1	UDB08_09_F1	0x40006800 + [0..3 * 0x200] + 0xb0
B[0..3]_UDB09_10_F1	UDB09_10_F1	0x40006800 + [0..3 * 0x200] + 0xb2
B[0..3]_UDB10_11_F1	UDB10_11_F1	0x40006800 + [0..3 * 0x200] + 0xb4
B[0..3]_UDB11_12_F1	UDB11_12_F1	0x40006800 + [0..3 * 0x200] + 0xb6
B[0..3]_UDB12_13_F1	UDB12_13_F1	0x40006800 + [0..3 * 0x200] + 0xb8
B[0..3]_UDB13_14_F1	UDB13_14_F1	0x40006800 + [0..3 * 0x200] + 0xba
B[0..3]_UDB14_15_F1	UDB14_15_F1	0x40006800 + [0..3 * 0x200] + 0xbc
B[0..3]_UDB00_01_ST	UDB00_01_ST	0x40006800 + [0..3 * 0x200] + 0xc0
B[0..3]_UDB01_02_ST	UDB01_02_ST	0x40006800 + [0..3 * 0x200] + 0xc2
B[0..3]_UDB02_03_ST	UDB02_03_ST	0x40006800 + [0..3 * 0x200] + 0xc4
B[0..3]_UDB03_04_ST	UDB03_04_ST	0x40006800 + [0..3 * 0x200] + 0xc6
B[0..3]_UDB04_05_ST	UDB04_05_ST	0x40006800 + [0..3 * 0x200] + 0xc8
B[0..3]_UDB05_06_ST	UDB05_06_ST	0x40006800 + [0..3 * 0x200] + 0xca
B[0..3]_UDB06_07_ST	UDB06_07_ST	0x40006800 + [0..3 * 0x200] + 0xcc
B[0..3]_UDB07_08_ST	UDB07_08_ST	0x40006800 + [0..3 * 0x200] + 0xce
B[0..3]_UDB08_09_ST	UDB08_09_ST	0x40006800 + [0..3 * 0x200] + 0xd0
B[0..3]_UDB09_10_ST	UDB09_10_ST	0x40006800 + [0..3 * 0x200] + 0xd2
B[0..3]_UDB10_11_ST	UDB10_11_ST	0x40006800 + [0..3 * 0x200] + 0xd4
B[0..3]_UDB11_12_ST	UDB11_12_ST	0x40006800 + [0..3 * 0x200] + 0xd6
B[0..3]_UDB12_13_ST	UDB12_13_ST	0x40006800 + [0..3 * 0x200] + 0xd8
B[0..3]_UDB13_14_ST	UDB13_14_ST	0x40006800 + [0..3 * 0x200] + 0xda
B[0..3]_UDB14_15_ST	UDB14_15_ST	0x40006800 + [0..3 * 0x200] + 0xdc
B[0..3]_UDB00_01_CTL	UDB00_01_CTL	0x40006800 + [0..3 * 0x200] + 0xe0
B[0..3]_UDB01_02_CTL	UDB01_02_CTL	0x40006800 + [0..3 * 0x200] + 0xe2
B[0..3]_UDB02_03_CTL	UDB02_03_CTL	0x40006800 + [0..3 * 0x200] + 0xe4
B[0..3]_UDB03_04_CTL	UDB03_04_CTL	0x40006800 + [0..3 * 0x200] + 0xe6
B[0..3]_UDB04_05_CTL	UDB04_05_CTL	0x40006800 + [0..3 * 0x200] + 0xe8
B[0..3]_UDB05_06_CTL	UDB05_06_CTL	0x40006800 + [0..3 * 0x200] + 0xea

Register Name	Purpose	Address
B[0..3]_UDB06_07_CTL	UDB06_07_CTL	0x40006800 + [0..3 * 0x200] + 0xec
B[0..3]_UDB07_08_CTL	UDB07_08_CTL	0x40006800 + [0..3 * 0x200] + 0xee
B[0..3]_UDB08_09_CTL	UDB08_09_CTL	0x40006800 + [0..3 * 0x200] + 0xf0
B[0..3]_UDB09_10_CTL	UDB09_10_CTL	0x40006800 + [0..3 * 0x200] + 0xf2
B[0..3]_UDB10_11_CTL	UDB10_11_CTL	0x40006800 + [0..3 * 0x200] + 0xf4
B[0..3]_UDB11_12_CTL	UDB11_12_CTL	0x40006800 + [0..3 * 0x200] + 0xf6
B[0..3]_UDB12_13_CTL	UDB12_13_CTL	0x40006800 + [0..3 * 0x200] + 0xf8
B[0..3]_UDB13_14_CTL	UDB13_14_CTL	0x40006800 + [0..3 * 0x200] + 0xfa
B[0..3]_UDB14_15_CTL	UDB14_15_CTL	0x40006800 + [0..3 * 0x200] + 0xfc
B[0..3]_UDB00_01_MSK	UDB00_01_MSK	0x40006800 + [0..3 * 0x200] + 0x100
B[0..3]_UDB01_02_MSK	UDB01_02_MSK	0x40006800 + [0..3 * 0x200] + 0x102
B[0..3]_UDB02_03_MSK	UDB02_03_MSK	0x40006800 + [0..3 * 0x200] + 0x104
B[0..3]_UDB03_04_MSK	UDB03_04_MSK	0x40006800 + [0..3 * 0x200] + 0x106
B[0..3]_UDB04_05_MSK	UDB04_05_MSK	0x40006800 + [0..3 * 0x200] + 0x108
B[0..3]_UDB05_06_MSK	UDB05_06_MSK	0x40006800 + [0..3 * 0x200] + 0x10a
B[0..3]_UDB06_07_MSK	UDB06_07_MSK	0x40006800 + [0..3 * 0x200] + 0x10c
B[0..3]_UDB07_08_MSK	UDB07_08_MSK	0x40006800 + [0..3 * 0x200] + 0x10e
B[0..3]_UDB08_09_MSK	UDB08_09_MSK	0x40006800 + [0..3 * 0x200] + 0x110
B[0..3]_UDB09_10_MSK	UDB09_10_MSK	0x40006800 + [0..3 * 0x200] + 0x112
B[0..3]_UDB10_11_MSK	UDB10_11_MSK	0x40006800 + [0..3 * 0x200] + 0x114
B[0..3]_UDB11_12_MSK	UDB11_12_MSK	0x40006800 + [0..3 * 0x200] + 0x116
B[0..3]_UDB12_13_MSK	UDB12_13_MSK	0x40006800 + [0..3 * 0x200] + 0x118
B[0..3]_UDB13_14_MSK	UDB13_14_MSK	0x40006800 + [0..3 * 0x200] + 0x11a
B[0..3]_UDB14_15_MSK	UDB14_15_MSK	0x40006800 + [0..3 * 0x200] + 0x11c
B[0..3]_UDB00_01_ACTL	UDB00_01_ACTL	0x40006800 + [0..3 * 0x200] + 0x120
B[0..3]_UDB01_02_ACTL	UDB01_02_ACTL	0x40006800 + [0..3 * 0x200] + 0x122
B[0..3]_UDB02_03_ACTL	UDB02_03_ACTL	0x40006800 + [0..3 * 0x200] + 0x124
B[0..3]_UDB03_04_ACTL	UDB03_04_ACTL	0x40006800 + [0..3 * 0x200] + 0x126
B[0..3]_UDB04_05_ACTL	UDB04_05_ACTL	0x40006800 + [0..3 * 0x200] + 0x128
B[0..3]_UDB05_06_ACTL	UDB05_06_ACTL	0x40006800 + [0..3 * 0x200] + 0x12a
B[0..3]_UDB06_07_ACTL	UDB06_07_ACTL	0x40006800 + [0..3 * 0x200] + 0x12c
B[0..3]_UDB07_08_ACTL	UDB07_08_ACTL	0x40006800 + [0..3 * 0x200] + 0x12e
B[0..3]_UDB08_09_ACTL	UDB08_09_ACTL	0x40006800 + [0..3 * 0x200] + 0x130
B[0..3]_UDB09_10_ACTL	UDB09_10_ACTL	0x40006800 + [0..3 * 0x200] + 0x132
B[0..3]_UDB10_11_ACTL	UDB10_11_ACTL	0x40006800 + [0..3 * 0x200] + 0x134
B[0..3]_UDB11_12_ACTL	UDB11_12_ACTL	0x40006800 + [0..3 * 0x200] + 0x136
B[0..3]_UDB12_13_ACTL	UDB12_13_ACTL	0x40006800 + [0..3 * 0x200] + 0x138
B[0..3]_UDB13_14_ACTL	UDB13_14_ACTL	0x40006800 + [0..3 * 0x200] + 0x13a
B[0..3]_UDB14_15_ACTL	UDB14_15_ACTL	0x40006800 + [0..3 * 0x200] + 0x13c
B[0..3]_UDB00_01_MC	UDB00_01_MC	0x40006800 + [0..3 * 0x200] + 0x140
B[0..3]_UDB01_02_MC	UDB01_02_MC	0x40006800 + [0..3 * 0x200] + 0x142
B[0..3]_UDB02_03_MC	UDB02_03_MC	0x40006800 + [0..3 * 0x200] + 0x144

Register Name	Purpose	Address
B[0..3]_UDB03_04_MC	UDB03_04_MC	0x40006800 + [0..3 * 0x200] + 0x146
B[0..3]_UDB04_05_MC	UDB04_05_MC	0x40006800 + [0..3 * 0x200] + 0x148
B[0..3]_UDB05_06_MC	UDB05_06_MC	0x40006800 + [0..3 * 0x200] + 0x14a
B[0..3]_UDB06_07_MC	UDB06_07_MC	0x40006800 + [0..3 * 0x200] + 0x14c
B[0..3]_UDB07_08_MC	UDB07_08_MC	0x40006800 + [0..3 * 0x200] + 0x14e
B[0..3]_UDB08_09_MC	UDB08_09_MC	0x40006800 + [0..3 * 0x200] + 0x150
B[0..3]_UDB09_10_MC	UDB09_10_MC	0x40006800 + [0..3 * 0x200] + 0x152
B[0..3]_UDB10_11_MC	UDB10_11_MC	0x40006800 + [0..3 * 0x200] + 0x154
B[0..3]_UDB11_12_MC	UDB11_12_MC	0x40006800 + [0..3 * 0x200] + 0x156
B[0..3]_UDB12_13_MC	UDB12_13_MC	0x40006800 + [0..3 * 0x200] + 0x158
B[0..3]_UDB13_14_MC	UDB13_14_MC	0x40006800 + [0..3 * 0x200] + 0x15a
B[0..3]_UDB14_15_MC	UDB14_15_MC	0x40006800 + [0..3 * 0x200] + 0x15c
B[0..3]_UDB00_A0_A1	UDB00_A0_A1	0x40006800 + [0..3 * 0x200]
B[0..3]_UDB01_A0_A1	UDB01_A0_A1	0x40006800 + [0..3 * 0x200] + 0x2
B[0..3]_UDB02_A0_A1	UDB02_A0_A1	0x40006800 + [0..3 * 0x200] + 0x4
B[0..3]_UDB03_A0_A1	UDB03_A0_A1	0x40006800 + [0..3 * 0x200] + 0x6
B[0..3]_UDB04_A0_A1	UDB04_A0_A1	0x40006800 + [0..3 * 0x200] + 0x8
B[0..3]_UDB05_A0_A1	UDB05_A0_A1	0x40006800 + [0..3 * 0x200] + 0xa
B[0..3]_UDB06_A0_A1	UDB06_A0_A1	0x40006800 + [0..3 * 0x200] + 0xc
B[0..3]_UDB07_A0_A1	UDB07_A0_A1	0x40006800 + [0..3 * 0x200] + 0xe
B[0..3]_UDB08_A0_A1	UDB08_A0_A1	0x40006800 + [0..3 * 0x200] + 0x10
B[0..3]_UDB09_A0_A1	UDB09_A0_A1	0x40006800 + [0..3 * 0x200] + 0x12
B[0..3]_UDB10_A0_A1	UDB10_A0_A1	0x40006800 + [0..3 * 0x200] + 0x14
B[0..3]_UDB11_A0_A1	UDB11_A0_A1	0x40006800 + [0..3 * 0x200] + 0x16
B[0..3]_UDB12_A0_A1	UDB12_A0_A1	0x40006800 + [0..3 * 0x200] + 0x18
B[0..3]_UDB13_A0_A1	UDB13_A0_A1	0x40006800 + [0..3 * 0x200] + 0x1a
B[0..3]_UDB14_A0_A1	UDB14_A0_A1	0x40006800 + [0..3 * 0x200] + 0x1c
B[0..3]_UDB15_A0_A1	UDB15_A0_A1	0x40006800 + [0..3 * 0x200] + 0x1e
B[0..3]_UDB00_D0_D1	UDB00_D0_D1	0x40006800 + [0..3 * 0x200] + 0x40
B[0..3]_UDB01_D0_D1	UDB01_D0_D1	0x40006800 + [0..3 * 0x200] + 0x42
B[0..3]_UDB02_D0_D1	UDB02_D0_D1	0x40006800 + [0..3 * 0x200] + 0x44
B[0..3]_UDB03_D0_D1	UDB03_D0_D1	0x40006800 + [0..3 * 0x200] + 0x46
B[0..3]_UDB04_D0_D1	UDB04_D0_D1	0x40006800 + [0..3 * 0x200] + 0x48
B[0..3]_UDB05_D0_D1	UDB05_D0_D1	0x40006800 + [0..3 * 0x200] + 0x4a
B[0..3]_UDB06_D0_D1	UDB06_D0_D1	0x40006800 + [0..3 * 0x200] + 0x4c
B[0..3]_UDB07_D0_D1	UDB07_D0_D1	0x40006800 + [0..3 * 0x200] + 0x4e
B[0..3]_UDB08_D0_D1	UDB08_D0_D1	0x40006800 + [0..3 * 0x200] + 0x50
B[0..3]_UDB09_D0_D1	UDB09_D0_D1	0x40006800 + [0..3 * 0x200] + 0x52
B[0..3]_UDB10_D0_D1	UDB10_D0_D1	0x40006800 + [0..3 * 0x200] + 0x54
B[0..3]_UDB11_D0_D1	UDB11_D0_D1	0x40006800 + [0..3 * 0x200] + 0x56
B[0..3]_UDB12_D0_D1	UDB12_D0_D1	0x40006800 + [0..3 * 0x200] + 0x58
B[0..3]_UDB13_D0_D1	UDB13_D0_D1	0x40006800 + [0..3 * 0x200] + 0x5a

Register Name	Purpose	Address
B[0..3]_UDB14_D0_D1	UDB14_D0_D1	0x40006800 + [0..3 * 0x200] + 0x5c
B[0..3]_UDB15_D0_D1	UDB15_D0_D1	0x40006800 + [0..3 * 0x200] + 0x5e
B[0..3]_UDB00_F0_F1	UDB00_F0_F1	0x40006800 + [0..3 * 0x200] + 0x80
B[0..3]_UDB01_F0_F1	UDB01_F0_F1	0x40006800 + [0..3 * 0x200] + 0x82
B[0..3]_UDB02_F0_F1	UDB02_F0_F1	0x40006800 + [0..3 * 0x200] + 0x84
B[0..3]_UDB03_F0_F1	UDB03_F0_F1	0x40006800 + [0..3 * 0x200] + 0x86
B[0..3]_UDB04_F0_F1	UDB04_F0_F1	0x40006800 + [0..3 * 0x200] + 0x88
B[0..3]_UDB05_F0_F1	UDB05_F0_F1	0x40006800 + [0..3 * 0x200] + 0x8a
B[0..3]_UDB06_F0_F1	UDB06_F0_F1	0x40006800 + [0..3 * 0x200] + 0x8c
B[0..3]_UDB07_F0_F1	UDB07_F0_F1	0x40006800 + [0..3 * 0x200] + 0x8e
B[0..3]_UDB08_F0_F1	UDB08_F0_F1	0x40006800 + [0..3 * 0x200] + 0x90
B[0..3]_UDB09_F0_F1	UDB09_F0_F1	0x40006800 + [0..3 * 0x200] + 0x92
B[0..3]_UDB10_F0_F1	UDB10_F0_F1	0x40006800 + [0..3 * 0x200] + 0x94
B[0..3]_UDB11_F0_F1	UDB11_F0_F1	0x40006800 + [0..3 * 0x200] + 0x96
B[0..3]_UDB12_F0_F1	UDB12_F0_F1	0x40006800 + [0..3 * 0x200] + 0x98
B[0..3]_UDB13_F0_F1	UDB13_F0_F1	0x40006800 + [0..3 * 0x200] + 0x9a
B[0..3]_UDB14_F0_F1	UDB14_F0_F1	0x40006800 + [0..3 * 0x200] + 0x9c
B[0..3]_UDB15_F0_F1	UDB15_F0_F1	0x40006800 + [0..3 * 0x200] + 0x9e
B[0..3]_UDB00_ST_CTL	UDB00_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xc0
B[0..3]_UDB01_ST_CTL	UDB01_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xc2
B[0..3]_UDB02_ST_CTL	UDB02_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xc4
B[0..3]_UDB03_ST_CTL	UDB03_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xc6
B[0..3]_UDB04_ST_CTL	UDB04_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xc8
B[0..3]_UDB05_ST_CTL	UDB05_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xca
B[0..3]_UDB06_ST_CTL	UDB06_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xcc
B[0..3]_UDB07_ST_CTL	UDB07_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xce
B[0..3]_UDB08_ST_CTL	UDB08_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xd0
B[0..3]_UDB09_ST_CTL	UDB09_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xd2
B[0..3]_UDB10_ST_CTL	UDB10_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xd4
B[0..3]_UDB11_ST_CTL	UDB11_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xd6
B[0..3]_UDB12_ST_CTL	UDB12_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xd8
B[0..3]_UDB13_ST_CTL	UDB13_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xda
B[0..3]_UDB14_ST_CTL	UDB14_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xdc
B[0..3]_UDB15_ST_CTL	UDB15_ST_CTL	0x40006800 + [0..3 * 0x200] + 0xde
B[0..3]_UDB00_MSK_ACTL	UDB00_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x100
B[0..3]_UDB01_MSK_ACTL	UDB01_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x102
B[0..3]_UDB02_MSK_ACTL	UDB02_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x104
B[0..3]_UDB03_MSK_ACTL	UDB03_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x106
B[0..3]_UDB04_MSK_ACTL	UDB04_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x108
B[0..3]_UDB05_MSK_ACTL	UDB05_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x10a
B[0..3]_UDB06_MSK_ACTL	UDB06_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x10c
B[0..3]_UDB07_MSK_ACTL	UDB07_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x10e

Register Name	Purpose	Address
B[0..3]_UDB08_MSK_ACTL	UDB08_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x110
B[0..3]_UDB09_MSK_ACTL	UDB09_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x112
B[0..3]_UDB10_MSK_ACTL	UDB10_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x114
B[0..3]_UDB11_MSK_ACTL	UDB11_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x116
B[0..3]_UDB12_MSK_ACTL	UDB12_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x118
B[0..3]_UDB13_MSK_ACTL	UDB13_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x11a
B[0..3]_UDB14_MSK_ACTL	UDB14_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x11c
B[0..3]_UDB15_MSK_ACTL	UDB15_MSK_ACTL	0x40006800 + [0..3 * 0x200] + 0x11e
B[0..3]_UDB00_MC_00	UDB00_MC_00	0x40006800 + [0..3 * 0x200] + 0x140
B[0..3]_UDB01_MC_00	UDB01_MC_00	0x40006800 + [0..3 * 0x200] + 0x142
B[0..3]_UDB02_MC_00	UDB02_MC_00	0x40006800 + [0..3 * 0x200] + 0x144
B[0..3]_UDB03_MC_00	UDB03_MC_00	0x40006800 + [0..3 * 0x200] + 0x146
B[0..3]_UDB04_MC_00	UDB04_MC_00	0x40006800 + [0..3 * 0x200] + 0x148
B[0..3]_UDB05_MC_00	UDB05_MC_00	0x40006800 + [0..3 * 0x200] + 0x14a
B[0..3]_UDB06_MC_00	UDB06_MC_00	0x40006800 + [0..3 * 0x200] + 0x14c
B[0..3]_UDB07_MC_00	UDB07_MC_00	0x40006800 + [0..3 * 0x200] + 0x14e
B[0..3]_UDB08_MC_00	UDB08_MC_00	0x40006800 + [0..3 * 0x200] + 0x150
B[0..3]_UDB09_MC_00	UDB09_MC_00	0x40006800 + [0..3 * 0x200] + 0x152
B[0..3]_UDB10_MC_00	UDB10_MC_00	0x40006800 + [0..3 * 0x200] + 0x154
B[0..3]_UDB11_MC_00	UDB11_MC_00	0x40006800 + [0..3 * 0x200] + 0x156
B[0..3]_UDB12_MC_00	UDB12_MC_00	0x40006800 + [0..3 * 0x200] + 0x158
B[0..3]_UDB13_MC_00	UDB13_MC_00	0x40006800 + [0..3 * 0x200] + 0x15a
B[0..3]_UDB14_MC_00	UDB14_MC_00	0x40006800 + [0..3 * 0x200] + 0x15c
B[0..3]_UDB15_MC_00	UDB15_MC_00	0x40006800 + [0..3 * 0x200] + 0x15e
PHUB_CFG	PHUB Configuration	0x40007000
PHUB_ERR	PHUB Error Detection	0x40007004
PHUB_ERR_ADR	PHUB Error Address	0x40007008
PHUB_CH[0..23]_BASIC_CFG	Channel Basic Configuration Register	0x40007010 + [0..23 * 0x10]
PHUB_CH[0..23]_ACTION	Channel Action	0x40007010 + [0..23 * 0x10] + 0x4
PHUB_CH[0..23]_BASIC_STATUS	Channel Basic Status Register	0x40007010 + [0..23 * 0x10] + 0x8
PHUB_CFGMEM[0..23]_CFG0	PHUB Channel Configuration Register 0	0x40007600 + [0..23 * 0x8]
PHUB_CFGMEM[0..23]_CFG1	PHUB Channel Configuration Register 1	0x40007600 + [0..23 * 0x8] + 0x4
PHUB_TDMEM[0..127]_ORIG_TD0	PHUB Original Transaction Descriptor 0	0x40007800 + [0..127 * 0x8]
PHUB_TDMEM[0..127]_ORIG_TD1	PHUB Original Transaction Descriptor 0	0x40007800 + [0..127 * 0x8] + 0x4
CAN[0..0]_CSR_INT_SR	INT_SR	0x4000a000
CAN[0..0]_CSR_INT_EN	INT_EN	0x4000a004
CAN[0..0]_CSR_BUF_SR	BUF_SR	0x4000a008
CAN[0..0]_CSR_ERR_SR	ERR_SR	0x4000a00c
CAN[0..0]_CSR_CMD	CMD	0x4000a010
CAN[0..0]_CSR_CFG	CFG	0x4000a014
CAN[0..0]_TX[0..7]_CMD	TXCMD	0x4000a020 + [0..7 * 0x10]
CAN[0..0]_TX[0..7]_ID	TXID	0x4000a020 + [0..7 * 0x10] + 0x4

Register Name	Purpose	Address
CAN[0..0]_TX[0..7]_DH	TXDH	0x4000a020 + [0..7 * 0x10] + 0x8
CAN[0..0]_TX[0..7]_DL	TXDL	0x4000a020 + [0..7 * 0x10] + 0xc
CAN[0..0]_RX[0..15]_CMD	RXCMD	0x4000a0a0 + [0..15 * 0x20]
CAN[0..0]_RX[0..15]_ID	RXID	0x4000a0a0 + [0..15 * 0x20] + 0x4
CAN[0..0]_RX[0..15]_DH	RXDH	0x4000a0a0 + [0..15 * 0x20] + 0x8
CAN[0..0]_RX[0..15]_DL	RXDL	0x4000a0a0 + [0..15 * 0x20] + 0xc
CAN[0..0]_RX[0..15]_AMR	RXAMR	0x4000a0a0 + [0..15 * 0x20] + 0x10
CAN[0..0]_RX[0..15]_ACR	RXACR	0x4000a0a0 + [0..15 * 0x20] + 0x14
CAN[0..0]_RX[0..15]_AMRD	RXAMRD	0x4000a0a0 + [0..15 * 0x20] + 0x18
CAN[0..0]_RX[0..15]_ACRD	RXACRD	0x4000a0a0 + [0..15 * 0x20] + 0x1c
DFB[0..0]_DPA_SRAM_DATA[0..127]	Data RAM A	0x4000c000 + [0..127 * 0x4]
DFB[0..0]_DPB_SRAM_DATA[0..127]	DFB Data RAM B	0x4000c200 + [0..127 * 0x4]
DFB[0..0]_CSA_SRAM_DATA[0..63]	DFB Control Store A	0x4000c400 + [0..63 * 0x4]
DFB[0..0]_CSB_SRAM_DATA[0..63]	DFB Control Store B	0x4000c500 + [0..63 * 0x4]
DFB[0..0]_FSM_SRAM_DATA[0..63]	DFB Code Store B	0x4000c600 + [0..63 * 0x4]
DFB[0..0]_ACU_SRAM_DATA[0..15]	DFB Address Store	0x4000c700 + [0..15 * 0x4]
DFB[0..0]_CR	DFB Command Register	0x4000c780
DFB[0..0]_SR	DFB Status Register	0x4000c784
DFB[0..0]_RAM_EN	DFB RAM Enable Register	0x4000c788
DFB[0..0]_RAM_DIR	DFB RAM Direction Register	0x4000c78c
DFB[0..0]_SEMA	DFB Semaphore Register	0x4000c790
DFB[0..0]_DSI_CTRL	DFB Global Control Register	0x4000c794
DFB[0..0]_INT_CTRL	DFB Interrupt Control Register	0x4000c798
DFB[0..0]_DMA_CTRL	DFB DMAREQ Control Register	0x4000c79c
DFB[0..0]_STAGEA	DFB Low Byte Staging Register A	0x4000c7a0
DFB[0..0]_STAGEAM	DFB Middle Byte Staging Register A	0x4000c7a1
DFB[0..0]_STAGEAH	DFB High Byte Staging Register A	0x4000c7a2
DFB[0..0]_STAGEB	DFB Low Byte Staging Register B	0x4000c7a4
DFB[0..0]_STAGEBM	DFB Middle Byte Staging Register B	0x4000c7a5
DFB[0..0]_STAGEBH	DFB High Byte Staging Register B	0x4000c7a6
DFB[0..0]_HOLDA	DFB Low Byte Holding Register A	0x4000c7a8
DFB[0..0]_HOLDAM	DFB Middle Byte Holding Register A	0x4000c7a9
DFB[0..0]_HOLDAH	DFB High Byte Holding Register A	0x4000c7aa
DFB[0..0]_HOLDAS	DFB Holding Register A Sign Extension	0x4000c7ab
DFB[0..0]_HOLDB	DFB Low Byte Holding Register B	0x4000c7ac
DFB[0..0]_HOLDBM	DFB Middle Byte Holding Register B	0x4000c7ad
DFB[0..0]_HOLDBH	DFB High Byte Holding Register B	0x4000c7ae
DFB[0..0]_HOLDBS	DFB Holding Register B Sign Extension	0x4000c7af
DFB[0..0]_COHER	DFB Coherency Register	0x4000c7b0
DFB[0..0]_DALIGN	DFB Data Alignment Register	0x4000c7b4
B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11]	PLD_IT	(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + [0..11 * 0x4]

Register Name	Purpose	Address
B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3]	PLD_ORT	(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x30 + [0..3 * 0x2]
B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST	MC_CFG_CEN_CONST	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x38
B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB	MC_CFG_XORFB	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x3a
B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET	MC_CFG_SET_RESET	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x3c
B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS	MC_CFG_BYPASS	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x3e
B[0..3]_P[0..7]_U[0..1]_CFG0	CFG0	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x40
B[0..3]_P[0..7]_U[0..1]_CFG1	CFG1	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x41
B[0..3]_P[0..7]_U[0..1]_CFG2	CFG2	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x42
B[0..3]_P[0..7]_U[0..1]_CFG3	CFG3	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x43
B[0..3]_P[0..7]_U[0..1]_CFG4	CFG4	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x44
B[0..3]_P[0..7]_U[0..1]_CFG5	CFG5	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x45
B[0..3]_P[0..7]_U[0..1]_CFG6	CFG6	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x46
B[0..3]_P[0..7]_U[0..1]_CFG7	CFG7	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x47
B[0..3]_P[0..7]_U[0..1]_CFG8	CFG8	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x48
B[0..3]_P[0..7]_U[0..1]_CFG9	CFG9	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x49
B[0..3]_P[0..7]_U[0..1]_CFG10	CFG10	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4a
B[0..3]_P[0..7]_U[0..1]_CFG11	CFG11	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4b
B[0..3]_P[0..7]_U[0..1]_CFG12	CFG12	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4c
B[0..3]_P[0..7]_U[0..1]_CFG13	CFG13	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4d
B[0..3]_P[0..7]_U[0..1]_CFG14	CFG14	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4e
B[0..3]_P[0..7]_U[0..1]_CFG15	CFG15	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4f
B[0..3]_P[0..7]_U[0..1]_CFG16	CFG16	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x50
B[0..3]_P[0..7]_U[0..1]_CFG20	CFG20	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x54
B[0..3]_P[0..7]_U[0..1]_CFG21	CFG21	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x55
B[0..3]_P[0..7]_U[0..1]_CFG22	CFG22	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x56
B[0..3]_P[0..7]_U[0..1]_CFG23	CFG23	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x57
B[0..3]_P[0..7]_U[0..1]_CFG24	CFG24	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x58

Register Name	Purpose	Address
B[0..3]_P[0..7]_U[0..1]_CFG25	CFG25	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x59
B[0..3]_P[0..7]_U[0..1]_CFG26	CFG26	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5a
B[0..3]_P[0..7]_U[0..1]_CFG27	CFG27	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5b
B[0..3]_P[0..7]_U[0..1]_CFG28	CFG28	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5c
B[0..3]_P[0..7]_U[0..1]_CFG29	CFG29	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5d
B[0..3]_P[0..7]_U[0..1]_CFG30	CFG30	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5e
B[0..3]_P[0..7]_U[0..1]_CFG31	CFG31	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5f
B[0..3]_P[0..7]_U[0..1]_DCFG[0..7]	DCFG	(((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x60 + [0..7 * 0x2]
B[0..3]_P[0..7]_ROUTE_HC[0..127]	HC	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x100 + [0..127 * 0x1]
B[0..3]_P[0..7]_ROUTE_HV_L[0..15]	HV_L	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x180 + [0..15 * 0x1]
B[0..3]_P[0..7]_ROUTE_HS[0..23]	HS	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x190 + [0..23 * 0x1]
B[0..3]_P[0..7]_ROUTE_HV_R[0..15]	HV_R	((0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x1a8 + [0..15 * 0x1]
B[0..3]_P[0..7]_ROUTE_PLD0IN0	PLD0IN0	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c0
B[0..3]_P[0..7]_ROUTE_PLD0IN1	PLD0IN1	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c2
B[0..3]_P[0..7]_ROUTE_PLD0IN2	PLD0IN2	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c4
B[0..3]_P[0..7]_ROUTE_PLD1IN0	PLD1IN0	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ca
B[0..3]_P[0..7]_ROUTE_PLD1IN1	PLD1IN1	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1cc
B[0..3]_P[0..7]_ROUTE_PLD1IN2	PLD1IN2	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ce
B[0..3]_P[0..7]_ROUTE_DPIN0	DPIN0	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d0
B[0..3]_P[0..7]_ROUTE_DPIN1	DPIN1	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d2
B[0..3]_P[0..7]_ROUTE_SCIN	SCIN	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d6
B[0..3]_P[0..7]_ROUTE_SCIOIN	SCIOIN	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d8
B[0..3]_P[0..7]_ROUTE_RCIN	RCIN	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1de
B[0..3]_P[0..7]_ROUTE_VS0	VS0	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e0
B[0..3]_P[0..7]_ROUTE_VS1	VS1	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e2
B[0..3]_P[0..7]_ROUTE_VS2	VS2	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e4
B[0..3]_P[0..7]_ROUTE_VS3	VS3	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e6

Register Name	Purpose	Address
B[0..3]_P[0..7]_ROUTE_VS4	VS4	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e8
B[0..3]_P[0..7]_ROUTE_VS5	VS5	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ea
B[0..3]_P[0..7]_ROUTE_VS6	VS6	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ec
B[0..3]_P[0..7]_ROUTE_VS7	VS7	(0x40010000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ee
DSI[0..15]_HC[0..127]	HC	(0x40014000 + [0..15 * 0x100]) + [0..127 * 0x1]
DSI[0..15]_HV_L[0..15]	HV_L	(0x40014000 + [0..15 * 0x100]) + 0x80 + [0..15 * 0x1]
DSI[0..15]_HS[0..23]	HS	(0x40014000 + [0..15 * 0x100]) + 0x90 + [0..23 * 0x1]
DSI[0..15]_HV_R[0..15]	HV_R	(0x40014000 + [0..15 * 0x100]) + 0xa8 + [0..15 * 0x1]
DSI[0..15]_DSIINP0	DSIINP0	0x40014000 + [0..15 * 0x100] + 0xc0
DSI[0..15]_DSIINP1	DSIINP1	0x40014000 + [0..15 * 0x100] + 0xc2
DSI[0..15]_DSIINP2	DSIINP2	0x40014000 + [0..15 * 0x100] + 0xc4
DSI[0..15]_DSIINP3	DSIINP3	0x40014000 + [0..15 * 0x100] + 0xc6
DSI[0..15]_DSIINP4	DSIINP4	0x40014000 + [0..15 * 0x100] + 0xc8
DSI[0..15]_DSIINP5	DSIINP5	0x40014000 + [0..15 * 0x100] + 0xca
DSI[0..15]_DSIOUTP0	DSIOUTP0	0x40014000 + [0..15 * 0x100] + 0xcc
DSI[0..15]_DSIOUTP1	DSIOUTP1	0x40014000 + [0..15 * 0x100] + 0xce
DSI[0..15]_DSIOUTP2	DSIOUTP2	0x40014000 + [0..15 * 0x100] + 0xd0
DSI[0..15]_DSIOUTP3	DSIOUTP3	0x40014000 + [0..15 * 0x100] + 0xd2
DSI[0..15]_DSIOUTT0	DSIOUTT0	0x40014000 + [0..15 * 0x100] + 0xd4
DSI[0..15]_DSIOUTT1	DSIOUTT1	0x40014000 + [0..15 * 0x100] + 0xd6
DSI[0..15]_DSIOUTT2	DSIOUTT2	0x40014000 + [0..15 * 0x100] + 0xd8
DSI[0..15]_DSIOUTT3	DSIOUTT3	0x40014000 + [0..15 * 0x100] + 0xda
DSI[0..15]_DSIOUTT4	DSIOUTT4	0x40014000 + [0..15 * 0x100] + 0xdc
DSI[0..15]_DSIOUTT5	DSIOUTT5	0x40014000 + [0..15 * 0x100] + 0xde
DSI[0..15]_VS0	VS0	0x40014000 + [0..15 * 0x100] + 0xe0
DSI[0..15]_VS1	VS1	0x40014000 + [0..15 * 0x100] + 0xe2
DSI[0..15]_VS2	VS2	0x40014000 + [0..15 * 0x100] + 0xe4
DSI[0..15]_VS3	VS3	0x40014000 + [0..15 * 0x100] + 0xe6
DSI[0..15]_VS4	VS4	0x40014000 + [0..15 * 0x100] + 0xe8
DSI[0..15]_VS5	VS5	0x40014000 + [0..15 * 0x100] + 0xea
DSI[0..15]_VS6	VS6	0x40014000 + [0..15 * 0x100] + 0xec
DSI[0..15]_VS7	VS7	0x40014000 + [0..15 * 0x100] + 0xee
BCTL[0..3]_MDCLK_EN	DCLK_EN	0x40015000 + [0..3 * 0x10]
BCTL[0..3]_MBCLK_EN	BCLK_EN	0x40015000 + [0..3 * 0x10] + 0x1
BCTL[0..3]_WAIT_CFG	WAIT_CFG	0x40015000 + [0..3 * 0x10] + 0x2
BCTL[0..3]_BANK_CTL	BANK_CTL	0x40015000 + [0..3 * 0x10] + 0x3
BCTL[0..3]_DCLK_EN0	DCLK_EN	0x40015000 + [0..3 * 0x10] + 0x8
BCTL[0..3]_BCLK_EN0	BCLK_EN	0x40015000 + [0..3 * 0x10] + 0x9
BCTL[0..3]_DCLK_EN1	DCLK_EN	0x40015000 + [0..3 * 0x10] + 0xa

Register Name	Purpose	Address
BCTL[0..3]_BCLK_EN1	BCLK_EN	0x40015000 + [0..3 * 0x10] + 0xb
BCTL[0..3]_DCLK_EN2	DCLK_EN	0x40015000 + [0..3 * 0x10] + 0xc
BCTL[0..3]_BCLK_EN2	BCLK_EN	0x40015000 + [0..3 * 0x10] + 0xd
BCTL[0..3]_DCLK_EN3	DCLK_EN	0x40015000 + [0..3 * 0x10] + 0xe
BCTL[0..3]_BCLK_EN3	BCLK_EN	0x40015000 + [0..3 * 0x10] + 0xf
IDMUX_IRQ_CTL[0..7]	Control Register IRQ_CTL	0x40015100 + [0..7 * 0x1]
IDMUX_DRQ_CTL[0..5]	Configuration Register DRQ_CTL	0x40015110 + [0..5 * 0x1]
P3BA_Y_START	Y_START	0x40050300
P3BA_YROLL	YROLL	0x40050301
P3BA_YCFG	YCFG	0x40050302
P3BA_X_START1	X_START1	0x40050303
P3BA_X_START2	X_START2	0x40050304
P3BA_XROLL1	XROLL1	0x40050305
P3BA_XROLL2	XROLL2	0x40050306
P3BA_XINC	XINC	0x40050307
P3BA_XCFG	XCFG	0x40050308
P3BA_OFFSETADDR1	OFFSETADDR1	0x40050309
P3BA_OFFSETADDR2	OFFSETADDR2	0x4005030a
P3BA_OFFSETADDR3	OFFSETADDR3	0x4005030b
P3BA_ABSADDR1	ABSADDR1	0x4005030c
P3BA_ABSADDR2	ABSADDR2	0x4005030d
P3BA_ABSADDR3	ABSADDR3	0x4005030e
P3BA_ABSADDR4	ABSADDR4	0x4005030f
P3BA_DATCFG1	DATCFG1	0x40050310
P3BA_DATCFG2	DATCFG2	0x40050311
P3BA_CMP_RSLT1	CMP_RSLT1	0x40050314
P3BA_CMP_RSLT2	CMP_RSLT2	0x40050315
P3BA_CMP_RSLT3	CMP_RSLT3	0x40050316
P3BA_CMP_RSLT4	CMP_RSLT4	0x40050317
P3BA_DATA_REG1	DATA_REG1	0x40050318
P3BA_DATA_REG2	DATA_REG2	0x40050319
P3BA_DATA_REG3	DATA_REG3	0x4005031a
P3BA_DATA_REG4	DATA_REG4	0x4005031b
P3BA_EXP_DATA1	EXP_DATA1	0x4005031c
P3BA_EXP_DATA2	EXP_DATA2	0x4005031d
P3BA_EXP_DATA3	EXP_DATA3	0x4005031e
P3BA_EXP_DATA4	EXP_DATA4	0x4005031f
P3BA_MSTR_HRDATA1	MSTR_HRDATA1	0x40050320
P3BA_MSTR_HRDATA2	MSTR_HRDATA2	0x40050321
P3BA_MSTR_HRDATA3	MSTR_HRDATA3	0x40050322
P3BA_MSTR_HRDATA4	MSTR_HRDATA4	0x40050323
P3BA_BIST_EN	BIST_EN	0x40050324

Register Name	Purpose	Address
P3BA_PHUB_MASTER_SSR	PHUB_MASTER_SSR	0x40050325
P3BA_SEQCFG1	SEQCFG1	0x40050326
P3BA_SEQCFG2	SEQCFG2	0x40050327
P3BA_Y_CURR	Y_CURR	0x40050328
P3BA_X_CURR1	X_CURR1	0x40050329
P3BA_X_CURR2	X_CURR2	0x4005032a
PANTHER_STCALIB_CFG	SYSTICK Calibration register	0x40080000
PANTHER_WAITPIPE	Wait State Pipeline	0x40080004
PANTHER_TRACE_CFG	Debug Trace Configuration	0x40080008
PANTHER_ETMFIFO	Embedded Trace Overflow Stall	0x4008000c
PANTHER_PVTCFG1	PVT Controller CFG1	0x40080010
PANTHER_PVTCFG2	PVT Controller CFG2	0x40080014
EXTMEM_DATA[0..16777215]	DATA	0x60000000 + [0..16777215 * 0x1]
ITM_TRACE_EN	ITM Trace Enable Register	0xe0000e00
ITM_TRACE_PRIVILEGE	ITM Trace Privilege Register	0xe0000e40
ITM_TRACE_CTRL	ITM Trace Control Register	0xe0000e80
ITM_INTEGRATION_WRITE	ITM Integration Write Register	0xe0000ef8
ITM_INTEGRATION_READ	ITM Integration Read Register	0xe0000efc
ITM_INTEGRATION_MODE_CRTL	ITM Integration Mode Control Register	0xe0000f00
ITM_LOCK_ACCESS	ITM Lock Access Register	0xe0000fb0
ITM_LOCK_STATUS	ITM Lock Status Register	0xe0000fb4
ITM_PID4	ITM Peripheral Identification Register 4	0xe0000fd0
ITM_PID5	ITM Peripheral Identification Register 5	0xe0000fd4
ITM_PID6	ITM Peripheral Identification Register 6	0xe0000fd8
ITM_PID7	ITM Peripheral Identification Register 7	0xe0000fdc
ITM_PID0	ITM Peripheral Identification Register 0	0xe0000fe0
ITM_PID1	ITM Peripheral Identification Register 1	0xe0000fe4
ITM_PID2	ITM Peripheral Identification Register 2	0xe0000fe8
ITM_PID3	ITM Peripheral Identification Register 3	0xe0000fec
ITM_CID0	ITM Component Identification Register 0	0xe0000ff0
ITM_CID1	ITM Component Identification Register 1	0xe0000ff4
ITM_CID2	ITM Component Identification Register 2	0xe0000ff8
ITM_CID3	ITM Component Identification Register 3	0xe0000ffc
DWT_CTRL	DWT Control Register	0xe0001000
DWT_CYCLE_COUNT	DWT Current PC Sampler Cycle Count Register	0xe0001004
DWT_CPI_COUNT	DWT CPI Count Register	0xe0001008
DWT_EXC_OVHD_COUNT	DWT Exception Overhead Count Register	0xe000100c
DWT_SLEEP_COUNT	DWT Sleep Count Register	0xe0001010
DWT_LSU_COUNT	DWT LSU Count Register	0xe0001014
DWT_FOLD_COUNT	DWT Fold Count Register	0xe0001018
DWT_PC_SAMPLE	DWT Program Counter Sample Register	0xe000101c
DWT_COMP_0	DWT Comparator Registers	0xe0001020

Register Name	Purpose	Address
DWT_MASK_0	DWT Mask Registers	0xe0001024
DWT_FUNCTION_0	DWT Function registers	0xe0001028
DWT_COMP_1	DWT Comparator Registers	0xe0001030
DWT_MASK_1	DWT Mask Registers	0xe0001034
DWT_FUNCTION_1	DWT Function registers	0xe0001038
DWT_COMP_2	DWT Comparator Registers	0xe0001040
DWT_MASK_2	DWT Mask Registers	0xe0001044
DWT_FUNCTION_2	DWT Function registers	0xe0001048
DWT_COMP_3	DWT Comparator Registers	0xe0001050
DWT_MASK_3	DWT Mask Registers	0xe0001054
DWT_FUNCTION_3	DWT Function registers	0xe0001058
FPB_CTRL	Flash Patch Control Register	0xe0002000
FPB_REMAP	Flash Patch Remap Register	0xe0002004
FPB_FP_COMP_0	Flash Patch Comparator Registers	0xe0002008
FPB_FP_COMP_1	Flash Patch Comparator Registers	0xe000200c
FPB_FP_COMP_2	Flash Patch Comparator Registers	0xe0002010
FPB_FP_COMP_3	Flash Patch Comparator Registers	0xe0002014
FPB_FP_COMP_4	Flash Patch Comparator Registers	0xe0002018
FPB_FP_COMP_5	Flash Patch Comparator Registers	0xe000201c
FPB_FP_COMP_6	Flash Patch Comparator Registers	0xe0002020
FPB_FP_COMP_7	Flash Patch Comparator Registers	0xe0002024
FPB_PID4	FPB Peripheral Identification Register 4	0xe0002fd0
FPB_PID5	FPB Peripheral Identification Register 5	0xe0002fd4
FPB_PID6	FPB Peripheral Identification Register 6	0xe0002fd8
FPB_PID7	FPB Peripheral Identification Register 7	0xe0002fdc
FPB_PID0	FPB Peripheral Identification Register 0	0xe0002fe0
FPB_PID1	FPB Peripheral Identification Register 1	0xe0002fe4
FPB_PID2	FPB Peripheral Identification Register 2	0xe0002fe8
FPB_PID3	FPB Peripheral Identification Register 3	0xe0002fec
FPB_CID0	FPB Component Identification Register 0	0xe0002ff0
FPB_CID1	FPB Component Identification Register 1	0xe0002ff4
FPB_CID2	FPB Component Identification Register 2	0xe0002ff8
FPB_CID3	FPB Component Identification Register 3	0xe0002ffc
NVIC_INT_CTL_TYPE	Interrupt Controller Type Register	0xe000e004
NVIC_SYSTICK_CTL	SYSTICK Control and Status register	0xe000e010
NVIC_SYSTICK_RELOAD	SYSTICK Reload value	0xe000e014
NVIC_SYSTICK_CURRENT	SYSTICK Counter	0xe000e018
NVIC_SYSTICK_CAL	SYSTICK Calibration register	0xe000e01c
NVIC_SETENA0	Interrupt Enable Set 0-31	0xe000e100
NVIC_CLRENA0	Interrupt Enable Clear 0-31	0xe000e180
NVIC_SETPEND0	Interrupt Pending Set 0-31	0xe000e200
NVIC_CLRPEND0	Interrupt Pending Clear 0-31	0xe000e280

Register Name	Purpose	Address
NVIC_ACTIVE0	Active Interrupts 0-31	0xe000e300
NVIC_PRI_0	Interrupt Priority 0-31	0xe000e400
NVIC_PRI_1	Interrupt Priority 0-31	0xe000e401
NVIC_PRI_2	Interrupt Priority 0-31	0xe000e402
NVIC_PRI_3	Interrupt Priority 0-31	0xe000e403
NVIC_PRI_4	Interrupt Priority 0-31	0xe000e404
NVIC_PRI_5	Interrupt Priority 0-31	0xe000e405
NVIC_PRI_6	Interrupt Priority 0-31	0xe000e406
NVIC_PRI_7	Interrupt Priority 0-31	0xe000e407
NVIC_PRI_8	Interrupt Priority 0-31	0xe000e408
NVIC_PRI_9	Interrupt Priority 0-31	0xe000e409
NVIC_PRI_10	Interrupt Priority 0-31	0xe000e40a
NVIC_PRI_11	Interrupt Priority 0-31	0xe000e40b
NVIC_PRI_12	Interrupt Priority 0-31	0xe000e40c
NVIC_PRI_13	Interrupt Priority 0-31	0xe000e40d
NVIC_PRI_14	Interrupt Priority 0-31	0xe000e40e
NVIC_PRI_15	Interrupt Priority 0-31	0xe000e40f
NVIC_PRI_16	Interrupt Priority 0-31	0xe000e410
NVIC_PRI_17	Interrupt Priority 0-31	0xe000e411
NVIC_PRI_18	Interrupt Priority 0-31	0xe000e412
NVIC_PRI_19	Interrupt Priority 0-31	0xe000e413
NVIC_PRI_20	Interrupt Priority 0-31	0xe000e414
NVIC_PRI_21	Interrupt Priority 0-31	0xe000e415
NVIC_PRI_22	Interrupt Priority 0-31	0xe000e416
NVIC_PRI_23	Interrupt Priority 0-31	0xe000e417
NVIC_PRI_24	Interrupt Priority 0-31	0xe000e418
NVIC_PRI_25	Interrupt Priority 0-31	0xe000e419
NVIC_PRI_26	Interrupt Priority 0-31	0xe000e41a
NVIC_PRI_27	Interrupt Priority 0-31	0xe000e41b
NVIC_PRI_28	Interrupt Priority 0-31	0xe000e41c
NVIC_PRI_29	Interrupt Priority 0-31	0xe000e41d
NVIC_PRI_30	Interrupt Priority 0-31	0xe000e41e
NVIC_PRI_31	Interrupt Priority 0-31	0xe000e41f
NVIC_CPUID_BASE	CPU ID Base Register	0xe000ed00
NVIC_INTR_CTRL_STATE	Interrupt Control State Register	0xe000ed04
NVIC_VECT_OFFSET	Interrupt Vector Table Offset	0xe000ed08
NVIC_APPLN_INTR	Application Interrupt and Reset Control Register	0xe000ed0c
NVIC_SYSTEM_CONTROL	System Control Register	0xe000ed10
NVIC_CFG_CONTROL	Configuration Control Register	0xe000ed14
NVIC_SYS_PRIO_HANDLER_4_7	System Handler Priority Registers	0xe000ed18
NVIC_SYS_PRIO_HANDLER_8_11	System Handler Priority Registers	0xe000ed1c
NVIC_SYS_PRIO_HANDLER_12_15	System Handler Priority Registers	0xe000ed20

Register Name	Purpose	Address
NVIC_SYS_HANDLER_CSR	System Handler Control and State Register	0xe000ed24
NVIC_MEMMAN_FAULT_STATUS	Memory Manage Fault Status Registers.	0xe000ed28
NVIC_BUS_FAULT_STATUS	Bus Fault Status Register	0xe000ed29
NVIC_USAGE_FAULT_STATUS	Usage Fault Status Register	0xe000ed2a
NVIC_HARD_FAULT_STATUS	Hard Fault Status Register	0xe000ed2c
NVIC_DEBUG_FAULT_STATUS	Debug Fault Status Register	0xe000ed30
NVIC_MEMMAN_FAULT_ADD	Memory Manage Fault Address Register	0xe000ed34
NVIC_BUS_FAULT_ADD	Bus Fault Address Register	0xe000ed38
CORE_DBG_DBG_HLT_CS	Debug Halting Control and Status register	0xe000edf0
CORE_DBG_DBG_REG_SEL	Debug Core Register Selector Register	0xe000edf4
CORE_DBG_DBG_REG_DATA	Debug Core Register Data Register	0xe000edf8
CORE_DBG_EXC_MON_CTL	Debug Exception and Monitor Control register	0xe000edfc
TPIU_SUPPORTED_SYNC_PRT_SZ	Supported Sync Port Sizes Register	0xe0040000
TPIU_CURRENT_SYNC_PRT_SZ	Current Sync Port Size Register	0xe0040004
TPIU_ASYNC_CLK_PRESCALER	Async Clock Prescaler Register	0xe0040010
TPIU_PROTOCOL	Selected Pin Protocol Register	0xe00400f0
TPIU_FORM_FLUSH_CTRL	Formatter and Flush Control Register	0xe0040304
TPIU_ITATBCTR2	Integration Test Registers	0xe0040ef0
TPIU_ITATBCTR0	Integration Test Registers	0xe0040ef8
ETM_CTL	ETM Control register	0xe0041000
ETM_CFG_CODE	ETM Configuration code register	0xe0041004
ETM_TRIG_EVENT	Trigger Event Register	0xe0041008
ETM_STATUS	ETM Status Register	0xe0041010
ETM_SYS_CFG	System Configuration Register	0xe0041014
ETM_TRACE_ENB_EVENT	Trace Enable Event Register	0xe0041020
ETM_TRACE_EN_CTRL1	TraceEnable Control 1 Register	0xe0041024
ETM_FIFOFULL_LEVEL	FIFOFULL Level Register	0xe004102c
ETM_SYNC_FREQ	Synchronization Frequency Register	0xe00411e0
ETM_ETM_ID	ETM ID Register	0xe00411e4
ETM_CFG_CODE_EXT	Configuration Code Extension Register	0xe00411e8
ETM_TR_SS_EMBICE_CTRL	Trace Start/Stop EmbeddedICE Control Register	0xe00411f0
ETM_CS_TRACE_ID	CoreSight Trace ID Register	0xe0041200
ETM_OS_LOCK_ACCESS	OS Lock Access Register	0xe0041300
ETM_OS_LOCK_STATUS	OS Lock Status Register	0xe0041304
ETM_INT_MODE_CTRL	Integration Mode Control Register	0xe0041f00
ETM_CLM_TAG_SET	Claim Tag Set Register	0xe0041fa0
ETM_CLM_TAG_CLR	Claim Tag Clear Register	0xe0041fa4
ETM_LOCK_ACCESS	Lock Access Register	0xe0041fb0
ETM_LOCK_STATUS	Lock Status Register	0xe0041fb4
ETM_AUTH_STATUS	Authentication Status Register	0xe0041fb8
ETM_DEV_TYPE	Device Type Register	0xe0041fcc
ETM_PID4	ETM Peripheral Identification Register 4	0xe0041fd0

Register Name	Purpose	Address
ETM_PID5	ETM Peripheral Identification Register 5	0xe0041fd4
ETM_PID6	ETM Peripheral Identification Register 6	0xe0041fd8
ETM_PID7	ETM Peripheral Identification Register 7	0xe0041fdc
ETM_PID0	ETM Peripheral Identification Register 0	0xe0041fe0
ETM_PID1	ETM Peripheral Identification Register 1	0xe0041fe4
ETM_PID2	ETM Peripheral Identification Register 2	0xe0041fe8
ETM_PID3	ETM Peripheral Identification Register 3	0xe0041fec
ETM_CID0	ETM Component Identification Register 0	0xe0041ff0
ETM_CID1	ETM Component Identification Register 1	0xe0041ff4
ETM_CID2	ETM Component Identification Register 2	0xe0041ff8
ETM_CID3	ETM Component Identification Register 3	0xe0041ffc
ROM_TABLE_NVIC	NVIC	0xe00ff000
ROM_TABLE_DWT	DWT	0xe00ff004
ROM_TABLE_FPB	FPB	0xe00ff008
ROM_TABLE_ITM	ITM	0xe00ff00c
ROM_TABLE_TPIU	TPIU	0xe00ff010
ROM_TABLE_ETM	ETM	0xe00ff014
ROM_TABLE_END	END	0xe00ff018
ROM_TABLE_MEMTYPE	MEMTYPE	0xe00fffcc
ROM_TABLE_PID4	ROM Table Peripheral Identification Register 4	0xe00fffd0
ROM_TABLE_PID5	ROM Table Peripheral Identification Register 5	0xe00fffd4
ROM_TABLE_PID6	ROM Table Peripheral Identification Register 6	0xe00fffd8
ROM_TABLE_PID7	ROM Table Peripheral Identification Register 7	0xe00fffdc
ROM_TABLE_PID0	ROM Table Peripheral Identification Register 0	0xe00fffe0
ROM_TABLE_PID1	ROM Table Peripheral Identification Register 1	0xe00fffe4
ROM_TABLE_PID2	ROM Table Peripheral Identification Register 2	0xe00fffe8
ROM_TABLE_PID3	ROM Table Peripheral Identification Register 3	0xe00fffec
ROM_TABLE_CID0	ROM Table Component Identification Register 0	0xe00ffff0
ROM_TABLE_CID1	ROM Table Component Identification Register 1	0xe00ffff4
ROM_TABLE_CID2	ROM Table Component Identification Register 2	0xe00ffff8
ROM_TABLE_CID3	ROM Table Component Identification Register 3	0xe00ffffc

1.3.1 FLASH_DATA[0..262143]

DATA

Reset: N/A

Register : Address

FLASH_DATA: 0x0-0x3FFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	data							

(no description)

Bits	Name	Description
7:0	data[7:0]	(no description)

1.3.2 SRAM_CODE64K[0..16383]

Code System Memory Bank

Reset: N/A

Register : Address

SRAM_CODE64K: 0x1FFF8000-0x1FFFBFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	code_sram							

Code Storage SRAM The CODE segement is available in all SRAM variants of PSoC5. The other CODExxK segements are only available on PSoC5 variants with that much SRAM or larger. The Interrupt Vector Table, Interrupt Service Routines and other speed critical software should be located in this segment of RAM. Data variables can be placed here but performance will be sub-optimal due to the access conflict with fetching instructions on the C bus. The RAM is physically 32-bits wide and is byte addressable. The RAM is zero wait-states for code fetches but data fetches will be slower due to the conflict on the C bus.

Bits	Name	Description
7:0	code_sram[7:0]	(no description)

1.3.3 SRAM_CODE32K[0..8191]

Code System Memory Bank

Reset: N/A

Register : Address

SRAM_CODE32K: 0x1FFFC000-0x1FFFDFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	code_sram							

Code Storage SRAM The CODE segement is available in all SRAM variants of PSoC5. The other CODExxK segements are only available on PSoC5 variants with that much SRAM or larger. The Interrupt Vector Table, Interrupt Service Routines and other speed critical software should be located in this segment of RAM. Data variables can be placed here but performance will be sub-optimal due to the access conflict with fetching instructions on the C bus. The RAM is physically 32-bits wide and is byte addressable. The RAM is zero wait-states for code fetches but data fetches will be slower due to the conflict on the C bus.

Bits	Name	Description
7:0	code_sram[7:0]	(no description)

1.3.4 SRAM_CODE16K[0..4095]

Code System Memory Bank

Reset: N/A

Register : Address

SRAM_CODE16K: 0x1FFFE000-0x1FFFEFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	code_sram							

Code Storage SRAM The CODE segement is available in all SRAM variants of PSoC5. The other CODExxK segements are only available on PSoC5 variants with that much SRAM or larger. The Interrupt Vector Table, Interrupt Service Routines and other speed critical software should be located in this segment of RAM. Data variables can be placed here but performance will be sub-optimal due to the access conflict with fetching instructions on the C bus. The RAM is physically 32-bits wide and is byte addressable. The RAM is zero wait-states for code fetches but data fetches will be slower due to the conflict on the C bus.

Bits	Name	Description
7:0	code_sram[7:0]	(no description)

1.3.5 SRAM_CODE[0..4095]

Code System Memory Bank

Reset: N/A

Register : Address

SRAM_CODE: 0x1FFFF000-0x1FFFFFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	code_sram							

Code Storage SRAM The CODE segement is available in all SRAM variants of PSoC5. The other CODExxK segements are only available on PSoC5 variants with that much SRAM or larger. The Interrupt Vector Table, Interrupt Service Routines and other speed critical software should be located in this segment of RAM. Data variables can be placed here but performance will be sub-optimal due to the access conflict with fetching instructions on the C bus. The RAM is physically 32-bits wide and is byte addressable. The RAM is zero wait-states for code fetches but data fetches will be slower due to the conflict on the C bus.

Bits	Name	Description
7:0	code_sram[7:0]	(no description)

1.3.6 SRAM_DATA[0..4095]

Data System Memory Bank

Reset: N/A

Register : Address

SRAM_DATA: 0x20000000-0x20000FFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	code_sram							

Data Storage SRAM The DATA segement is available in all SRAM variants of PSoC5. The other DATAxxK segements are only available on PSoC5 variants with that much SRAM or larger. The Stack pointer is normally located at the top of DATA SRAM and grows downward. All data should be placed in this segement of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the S bus. There is also a 1 clock wait wait state for all code fetches across the S bus. The RAM is physically 32-bits wide and is byte addressable.

Bits	Name	Description
7:0	code_sram[7:0]	(no description)

1.3.7 SRAM_DATA16K[0..4095]

Data System Memory Bank

Reset: N/A

Register : Address

SRAM_DATA16K: 0x20001000-0x20001FFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	code_sram							

Data Storage SRAM The DATA segement is available in all SRAM variants of PSoC5. The other DATAxxK segements are only available on PSoC5 variants with that much SRAM or larger. The Stack pointer is normally located at the top of DATA SRAM and grows downward. All data should be placed in this segement of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the S bus. There is also a 1 clock wait wait state for all code fetches across the S bus. The RAM is physically 32-bits wide and is byte addressable.

Bits	Name	Description
7:0	code_sram[7:0]	(no description)

1.3.8 SRAM_DATA32K[0..8191]

Data System Memory Bank

Reset: N/A

Register : Address

SRAM_DATA32K: 0x20002000-0x20003FFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	code_sram							

Data Storage SRAM The DATA segement is available in all SRAM variants of PSoC5. The other DATAxxK segements are only available on PSoC5 variants with that much SRAM or larger. The Stack pointer is normally located at the top of DATA SRAM and grows downward. All data should be placed in this segement of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the S bus. There is also a 1 clock wait wait state for all code fetches across the S bus. The RAM is physically 32-bits wide and is byte addressable.

Bits	Name	Description
7:0	code_sram[7:0]	(no description)

1.3.9 SRAM_DATA64K[0..16383]

Data System Memory Bank

Reset: N/A

Register : Address

SRAM_DATA64K: 0x20004000-0x20007FFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	code_sram							

Data Storage SRAM The DATA segement is available in all SRAM variants of PSoC5. The other DATAxxK segements are only available on PSoC5 variants with that much SRAM or larger. The Stack pointer is normally located at the top of DATA SRAM and grows downward. All data should be placed in this segement of SRAM. Code can be placed here but will result in performance degradation due to conflicts with data fetches on the S bus. There is also a 1 clock wait wait state for all code fetches across the S bus. The RAM is physically 32-bits wide and is byte addressable.

Bits	Name	Description
7:0	code_sram[7:0]	(no description)

1.3.10 CLKDIST_CR

Configuration Register CR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_CR: 0x40004000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:00		R/W:00		R/W:00	
HW Access	NA	R	R		R		R	
Name		IMO2X_SRC	IMO_OUT		ILO_OUT		PLL_SRC	

This register is used to configure the CLK sources. 1- The source from IMO to clock distribution block. 2- ILO source to the clock distribution block. 3- The source to the PLL reference clock input. 4- Source to IMO doubler. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
6	IMO2X_SRC	Select the input source to IMO doubler. See Table 1-2.
5:4	IMO_OUT[1:0]	Select the IMO output source to clock distribution. See Table 1-3.
3:2	ILO_OUT[1:0]	Select the ILO output source to clock distribution. See Table 1-1.
1:0	PLL_SRC[1:0]	Select the PLL reference clock input See Table 1-4.

Table 1-1. Bit field encoding: ILO_OUTPUT_SEL_ENUM

Value	Name	Description
2'h0	ILO100K	100KHz output is selected
2'h1	ILO33K	33KHz output is selected
2'h2	ILO1K	1KHz output is selected
2'h3	RSVD	Reserved

Table 1-2. Bit field encoding: IMO2X_INPUT_SEL_ENUM

Value	Name	Description
1'b0	DSI	Digital System Interconnect is used as a source to IMO doubler
1'b1	XTAL	External clock source is used as a source to IMO doubler

Table 1-3. Bit field encoding: IMO_OUTPUT_SEL_ENUM

Value	Name	Description
2'h0	IMO	IMO is selected
2'h1	IMO2X	IMO Doubler output is selected
2'h2	IMO36	IMO 36MHz output is selected
2'h3	RSVD	Reserved

1.3.10 CLKDIST_CR (continued)

Table 1-4. Bit field encoding: PLL_INPUT_SEL_ENUM

Value	Name	Description
2'h0	IMO	IMO is selected
2'h1	XTAL	33MHz XTAL is selected
2'h2	DIGK	Digital System Interconnect(k)
2'h3	RSVD	Reserved

1.3.11 CLKDIST_LD

LOAD Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_LD: 0x40004001

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	W:0
HW Access	NA						R	R/W
Name							SYNC_EN	LOAD

This register allows for clean updates of the dividers while running, and to align a starting point for a group of dividers. Setting the LOAD bit immediately copies the values of the WRK0 and WRK1 registers into all divider divide registers (DCFG0,1 and ACFG0,1, BCFG0,1), which are not masked off. Setting the SYNC_EN bit forces a restart of all the dividers which are not masked off (Excluding BUS_CLK). Upon restarting all affected dividers start phase aligned. In order for the divders to start phase aligned all the divide values must be integer multiples of one another. This allows for local control of the clock trees. All bits in this register are cleared upon completion of loading and/or restarting.

Bits	Name	Description
1	SYNC_EN	Restart all unmasked dividers in phase See Table 1-6.
0	LOAD	Load all unmasked dividers with a common shadow divider value See Table 1-5.

Table 1-5. Bit field encoding: LOAD_ENUM

Value	Name	Description
1'b0	LOAD_0	don't copy
1'b1	LOAD_1	copy shadow value defined in CLKDIST_WRK0 and CLKDIST_WRK1 registers to all dividers selected in CLKDIST_MSK0 and CLKDIST_MSK1 registers

Table 1-6. Bit field encoding: SYNC_SHADOW_ENUM

Value	Name	Description
1'b0	SYNC_0	don't use synchronized starting
1'b1	SYNC_1	enable all dividers selected in CLKDIST_MSK register (Excluding BUS_CLK) to start (or re start) in phase.

1.3.12 CLKDIST_WRK0

LSB Shadow Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_WRK0: 0x40004002

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register allows atomic loads of clock dividers, so that the 16 bits dividers can safely be updated dynamically.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.13 CLKDIST_WRK1

MSB Shadow Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_WRK1: 0x40004003

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register allows atomic loads of clock dividers, so that the 16 bits dividers can safely be updated dynamically.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.14 CLKDIST_MSTR0

Master clock (clk_sync_d) Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_MSTR0: 0x40004004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register holds the master source clock 8-bit divide value.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x00 source 0x01 source / 2 0x02 source / 3 ... ... 0xfe source / 255 0xff source / 256

1.3.15 CLKDIST_MSTR1

Master (clk_sync_d) Configuration Register/CPU Divider Value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CLKDIST_MSTR1: 0x40004005

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							SRC_SEL	

This register holds the master configuration and CPU clock divide value.

Bits	Name	Description
1:0	SRC_SEL[1:0]	Master clock source selection. See Table 1-7.

Table 1-7. Bit field encoding: MASTER_SRC_SEL_ENUM

Value	Name	Description
2'h0	IMO	imo output is selected
2'h1	PLL	pll output is selected
2'h2	XTAL	xtal_mhz output is selected
2'h3	DSI	dsi_c output is selected

1.3.16 CLKDIST_BCFG0

CLK_BUS LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG0: 0x40004006

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register holds the LSB of the 16-bit divide value.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.17 CLKDIST_BCFG1

CLK_BUS MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG1: 0x40004007

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register holds the MSB of the 16-bit divide value.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.18 CLKDIST_BCFG2

CLK_BUS Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG2: 0x40004008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:000		
HW Access	R	R	R	R	R	NA		
Name	MASK	SSS	EARLY	DUTY	SYNC			

This register holds the 4-bit configuraton values.

Bits	Name	Description
7	MASK	Mask bits to enable shadow loads--0 disable, 1 enable
6	SSS	Sync source same as output frequency. Used to bypass synchronization with delay matched path. See Table 1-10.
5	EARLY	This bit in the configuration register can be used to set the early phase mode, with rising edge near the half-count of the divider. See Table 1-9.
4	DUTY	Force duty cycle to 50% See Table 1-8.
3	SYNC	Select output synchronization to master clock See Table 1-11.

Table 1-8. Bit field encoding: DUTY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable 50% duty cycle
1'b1	ENABLE	Enable 50% duty cycle clock output

Table 1-9. Bit field encoding: EARLY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable early phase mode
1'b1	ENABLE	Enable early phase mode

Table 1-10. Bit field encoding: SSS_ENUM

Value	Name	Description
1'b0	DISABLE	Sync source not same frequency
1'b1	ENABLE	Sync source is same frequency

Table 1-11. Bit field encoding: SYNC_ENUM

Value	Name	Description
1'b0	DISABLE	Disable synchronization
1'b1	ENABLE	Enable synchronization

1.3.19 CLKDIST_UCFG

USB Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_UCFG: 0x40004009

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	NA			R	R	R	R	
Name				TMODE	GPIPE	DIV2	SRC_SEL	

This register holds the USB clock configuration.

Bits	Name	Description
4	TMODE	Enable monitoring of clk_usb through DSI routing See Table 1-15.
3	GPIPE	Global DSI input pipeline configuration See Table 1-12.
2	DIV2	USB clock divide source by two See Table 1-13.
1:0	SRC_SEL[1:0]	USB clock source selection. See Table 1-14.

Table 1-12. Bit field encoding: CDSI_ENUM

Value	Name	Description
1'b0	BYPASS	Bypass pipeline stages
1'b1	ENABLE	Use pipeline stages

Table 1-13. Bit field encoding: DIV2_ENUM

Value	Name	Description
1'b0	DISABLE	Disable divide by two
1'b1	ENABLE	Enable divide by two

Table 1-14. Bit field encoding: SRC_SEL_ENUM

Value	Name	Description
2'h0	IMO2X	imo2x output is selected
2'h1	IMO	imo output is selected
2'h1	PLL	pll output is selected
2'h3	DSI	dsi_glb output is selected

Table 1-15. Bit field encoding: TMODE_ENUM

Value	Name	Description
1'b0	DISABLE	Disable clk_usb_test output to DSI
1'b1	ENABLE	Enable clk_usb_test output to DSI

1.3.20 CLKDIST_DLY0

Delay block Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DLY0: 0x4000400A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:00		R/W:00000				
HW Access	NA	R		R				
Name		CTRIM		FTRIM				

This register holds the delay block configuration.

Bits	Name	Description
6:5	CTRIM[1:0]	Course trim bits for delay block See Table 1-16.
4:0	FTRIM[4:0]	Fine trim bits for delay block 5'b00000 Lowest bias ... ... 5'bfffff Highest bias

Table 1-16. Bit field encoding: CTRIM_ENUM

Value	Name	Description
2'b00	ZERO	Highest bias setting
2'b10	TWO	Second highest bias setting
2'b01	ONE	Third highest bias setting
2'b11	THREE	Fourth highest bias setting

1.3.21 CLKDIST_DLY1

Delay block Configuration Register

Reset: Reset Signals Listed Below

Register : Address

CLKDIST_DLY1: 0x4000400B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						EN	ISEL	MODE

This register holds the configuration control for the clock delay cell. This cell is used to program delays between the system bus clock and each of the 4 individual analog clocks (ACLK). This is used to unalign analog and digital domain clock edges to reduce noise when the analog domain clocks. Normally the 5 domains are phase aligned for applications that need clock-edge-aligned interfaces. If clock-edge-aligned interfaces aren't needed and system noise is an issue, clock tree domains can be programmably skewed away from each other.

Bits	Name	Description
2	EN	The clk_sync_d reference clock is sourced by the clk0 output of the delay cell. This output can either be sourced from a 10-tap delay element or muxed directly (bypassed) from the delay cell's clock input (clk_sync). When bypassed (EN=0), the bus clock and all 4 analog clocks (clk_a[]) are balanced (clock-edge-aligned) if their skew delay registers are programmed to 0x0001. (see CLKDIST_ACFGx_CFG3) If EN=1 this enables the delay element on clk0 and allows the system to program delays on clk_sync_d. The delay amount is identical to the ACLK channels but is not controlled with a register, but rather with customer controlled non-volatile bits that are loaded at system POR. In this mode the clk0 has a inherent ~4ns delay, meaning BUSCLK lags the 4 ACLKs by ~4ns when all tap are programmed to 0x0001. Thus, any values programmed into the PHASE_DLY fields of the CLKDIST_ACFGx_CFG3 registers will skew the clocks relative to this ~4ns skew, as will changing the clk0 delay via CNVL setting. Note that it is not allowed that the system be configured such that clk_sync_d lag any clk_a[] by less than ~4ns for any values of the programmable delay values. The HW will fail in these cases and SW should avoid doing this. See ACFG3 register description for further details.
1	ISEL	Reference current selection See Table 1-17.
0	MODE	Clock mode. Used to put the delay cell in normal more or trim mode. See Table 1-18.

Reset Table

resetsignal	field(s)
System reset for retention flops [reset_all_retention]	MODE, ISEL
Domain reset for non-retention flops [reset_all_nonretention]	EN

1.3.21 CLKDIST_DLY1 (continued)

Table 1-17. Bit field encoding: ISEL_ENUM

Value	Name	Description
1'b0	BANDGAP	Use bandgap reference
1'b1	INTERNAL	Use internal reference

Table 1-18. Bit field encoding: MODE_ENUM

Value	Name	Description
1'b0	DELAY	Puts the cell in normal clock delay mode. This is mission mode and allows for programming of delays on the clock trees. See CLKDIST_ACFGx_CFG3
1'b1	RING	This mode is used only for trimming. While in this mode the output of a ring oscillator is monitored and tuned to 40MHz.

1.3.22 CLKDIST_DMASK

Digital Clock Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DMASK: 0x40004010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DMASK							

Enable shadow loads for digital clocks

Bits	Name	Description
7:0	DMASK[7:0]	Mask bits to enable shadow loads--0 disable, 1 enable

1.3.23 CLKDIST_AMASK

Analog Clock Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_AMASK: 0x40004014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					AMASK			

Enable shadow loads for analog clocks

Bits	Name	Description
3:0	AMASK[3:0]	Mask bits to enable shadow loads--0 disable, 1 enable

1.3.24 CLKDIST_DCFG[0..7]_CFG0

LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG0: 0x40004080

CLKDIST_DCFG1_CFG0: 0x40004084

CLKDIST_DCFG2_CFG0: 0x40004088

CLKDIST_DCFG3_CFG0: 0x4000408C

CLKDIST_DCFG4_CFG0: 0x40004090

CLKDIST_DCFG5_CFG0: 0x40004094

CLKDIST_DCFG6_CFG0: 0x40004098

CLKDIST_DCFG7_CFG0: 0x4000409C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register holds the LSB of the 16-bit divide value.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.25 CLKDIST_DCFG[0..7]_CFG1

MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG1: 0x40004081

CLKDIST_DCFG1_CFG1: 0x40004085

CLKDIST_DCFG2_CFG1: 0x40004089

CLKDIST_DCFG3_CFG1: 0x4000408D

CLKDIST_DCFG4_CFG1: 0x40004091

CLKDIST_DCFG5_CFG1: 0x40004095

CLKDIST_DCFG6_CFG1: 0x40004099

CLKDIST_DCFG7_CFG1: 0x4000409D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register holds the MSB of the 16-bit divide value.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.26 CLKDIST_DCFG[0..7]_CFG2

Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG2: 0x40004082

CLKDIST_DCFG1_CFG2: 0x40004086

CLKDIST_DCFG2_CFG2: 0x4000408A

CLKDIST_DCFG3_CFG2: 0x4000408E

CLKDIST_DCFG4_CFG2: 0x40004092

CLKDIST_DCFG5_CFG2: 0x40004096

CLKDIST_DCFG6_CFG2: 0x4000409A

CLKDIST_DCFG7_CFG2: 0x4000409E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R	R	R	R	R	R		
Name	PIPE	SSS	EARLY	DUTY	SYNC	SRC_SEL		

This register holds the 8-bit configuraton values.

Bits	Name	Description
7	PIPE	DSI input pipeline configuration See Table 1-21.
6	SSS	Sync source same as output frequency. Used to bypass synchronization with delay matched path. See Table 1-23.
5	EARLY	This bit in the configuration register can be used to set the early phase mode, with rising edge near the half-count of the divider. See Table 1-20.
4	DUTY	Force duty cycle to 50% See Table 1-19.
3	SYNC	Select output synchronization to master clock See Table 1-24.
2:0	SRC_SEL[2:0]	Clock source selection. See Table 1-22.

Table 1-19. Bit field encoding: DUTY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable 50% duty cycle
1'b1	ENABLE	Enable 50% duty cycle clock output

1.3.26 CLKDIST_DCFG[0..7]_CFG2 (continued)

Table 1-20. Bit field encoding: EARLY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable early phase mode
1'b1	ENABLE	Enable early phase mode

Table 1-21. Bit field encoding: PIPE_ENUM

Value	Name	Description
1'b0	BYPASS	Bypass pipeline stages
1'b1	ENABLE	Use pipeline stages

Table 1-22. Bit field encoding: SRC_SEL_ENUM

Value	Name	Description
3'h0	clk_sync_d	clk_sync_d output is selected
3'h1	imo	imo output is selected
3'h2	xtal_mhz	xtal_mhz output is selected
3'h3	ilo	ilo output is selected
3'h4	pll	pll output is selected
3'h5	xtal_khz	xtal_khz output is selected
3'h6	dsi_g	dsi_global[0] output is selected
3'h7	dsi_d	dsi_d output is selected

Table 1-23. Bit field encoding: SSS_ENUM

Value	Name	Description
1'b0	DISABLE	Sync source not same frequency
1'b1	ENABLE	Sync source is same frequency

Table 1-24. Bit field encoding: SYNC_ENUM

Value	Name	Description
1'b0	DISABLE	Disable synchronization
1'b1	ENABLE	Enable synchronization

1.3.27 CLKDIST_ACFG[0..3]_CFG0

LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG0: 0x40004100

CLKDIST_ACFG1_CFG0: 0x40004104

CLKDIST_ACFG2_CFG0: 0x40004108

CLKDIST_ACFG3_CFG0: 0x4000410C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register holds the LSB of the 16-bit divide value.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.28 CLKDIST_ACFG[0..3]_CFG1

MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG1: 0x40004101

CLKDIST_ACFG1_CFG1: 0x40004105

CLKDIST_ACFG2_CFG1: 0x40004109

CLKDIST_ACFG3_CFG1: 0x4000410D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DIV_VAL							

This register holds the MSB of the 16-bit divide value.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.29 CLKDIST_ACFG[0..3]_CFG2

Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG2: 0x40004102

CLKDIST_ACFG1_CFG2: 0x40004106

CLKDIST_ACFG2_CFG2: 0x4000410A

CLKDIST_ACFG3_CFG2: 0x4000410E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R	R	R	R	R	R		
Name	PIPE	SSS	EARLY	DUTY	SYNC	SRC_SEL		

This register holds the 8-bit configuraton values.

Bits	Name	Description
7	PIPE	DSI input pipeline configuration See Table 1-27.
6	SSS	Sync source same as output frequency. Used to bypass synchronization with delay matched path. See Table 1-29.
5	EARLY	This bit in the configuration register can be used to set the early phase mode, with rising edge near the half-count of the divider. See Table 1-26.
4	DUTY	Force duty cycle to 50% See Table 1-25.
3	SYNC	Select output synchronization to master clock See Table 1-30.
2:0	SRC_SEL[2:0]	Clock source selection. See Table 1-28.

Table 1-25. Bit field encoding: DUTY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable 50% duty cycle
1'b1	ENABLE	Enable 50% duty cycle clock output

Table 1-26. Bit field encoding: EARLY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable early phase mode
1'b1	ENABLE	Enable early phase mode

1.3.29 CLKDIST_ACFG[0..3]_CFG2 (continued)

Table 1-27. Bit field encoding: PIPE_ENUM

Value	Name	Description
1'b0	BYPASS	Bypass pipeline stages
1'b1	ENABLE	Use pipeline stages

Table 1-28. Bit field encoding: SRC_SEL_ENUM

Value	Name	Description
3'h0	clk_sync_a	clk_sync_a output is selected
3'h1	imo	imo output is selected
3'h2	xtal_mhz	xtal_mhz output is selected
3'h3	ilo	ilo output is selected
3'h4	pll	pll output is selected
3'h5	xtal_khz	xtal_khz output is selected
3'h6	dsi_g	dsi_global[0] output is selected
3'h7	dsi_a	dsi_a output is selected

Table 1-29. Bit field encoding: SSS_ENUM

Value	Name	Description
1'b0	DISABLE	Sync source not same frequency
1'b1	ENABLE	Sync source is same frequency

Table 1-30. Bit field encoding: SYNC_ENUM

Value	Name	Description
1'b0	DISABLE	Disable synchronization
1'b1	ENABLE	Enable synchronization

1.3.30 CLKDIST_ACFG[0..3]_CFG3

Analog clocks Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG3: 0x40004103

CLKDIST_ACFG1_CFG3: 0x40004107

CLKDIST_ACFG2_CFG3: 0x4000410B

CLKDIST_ACFG3_CFG3: 0x4000410F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					PHASE_DLY			

This register holds the analog clocks configuration.

Bits	Name	Description
3:0	PHASE_DLY[3:0]	Phase delay selection (1.0ns increments): 0x00 Clock Disabled 0x01 2.5ns delay 0x02 3.5ns delay ... 0x0a 11.5ns delay 0x0b 12.5ns delay 0x0c Clock Disabled 0x0d Clock Disabled 0x0e Clock Disabled 0x0f Clock Disabled

1.3.31 FASTCLK_IMO_CR

Internal Main Oscillator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_IMO_CR: 0x40004200

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA	R	R	R	R	R		
Name		usbclk_on	xclken	f2xon	fimo_en	f_range		

This register controls operation of the IMO.

Bits	Name	Description
6	usbclk_on	Configures IMO for higher precision for when the internal USB clock-locking function is being used. See Table 1-34.
5	xclken	External clock enable for the IMO doubler See Table 1-35.
4	f2xon	IMO Doubler enable See Table 1-31.
3	fimo_en	enable IMO fast startup See Table 1-32.
2:0	f_range[2:0]	Frequency range setting for the IMO See Table 1-33.

Table 1-31. Bit field encoding: F2XON_ENUM

Value	Name	Description
1'b0	F2XON_0	Doubler disabled (IMOCLK2X = 0)
1'b1	F2XON_1	Doubler enabled. Note: input freq range limited to 24 MHz max.

Table 1-32. Bit field encoding: FIMO_EN

Value	Name	Description
1'b0	FIMO_EN_NORMAL	Normal mode
1'b1	FIMO_EN_FASTSTART	Fast start mode

Table 1-33. Bit field encoding: F_RANGE_ENUM

Value	Name	Description
3'h0	F_RANGE_0	12 MHz (normal)
3'h1	F_RANGE_1	6 MHz (normal); 12 MHz (fast start)
3'h2	F_RANGE_2	24 MHz
3'h3	F_RANGE_3	3 MHz (normal); 12 MHz (fast start)
3'h4	F_RANGE_4	48 MHz
3'h5	F_RANGE_5	67 MHz
3'h6	F_RANGE_6	80 MHz (normal); 48 MHz (fast start)
3'h7	F_RANGE_7	96 MHz (normal); 48 MHz (fast start)

1.3.31 FASTCLK_IMO_CR (continued)

Table 1-34. Bit field encoding: USBCLK_ON_ENUM

Value	Name	Description
1'b0	USBCLK_ON_0	Normally used for non-USB modes, for lower IMO power
1'b0	USBCLK_ON_1	USB clock-locking used; IMO runs at higher power for highest USB clock precision.

Table 1-35. Bit field encoding: XCLKEN_ENUM

Value	Name	Description
1'b0	XCLKEN_0	IMO doubler runs from the IMOCLK
1'b1	XCLKEN_1	IMO doubler runs from the selected 'external' clock. This is a signal on a global - source is TBD.

1.3.32 FASTCLK_XMHZ_CSR

External 4-33 MHz Crystal Oscillator Status and Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_CSR: 0x40004210

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				xstart	xpump_dis	xfb_dis	xto_dis	en

This register is used to enable and configure modes of the XMHZ oscillator, and to read error status. In the table above, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
4	xstart	This INTERNAL bit selects the start-up mode for the oscillator. By default, the output is pulsed to initiate start-up. If a system clock is available at approximately the same frequency as the crystal, this signal can be selected to provide a faster start-up time. See Table 1-39.
3	xpump_dis	This bit disables the crystal oscillator voltage pumps. This bit must be left low and the pump always enabled. See Table 1-38.
2	xfb_dis	This bit disables an amplitude monitor on the oscillator signal. This bit must be set high by software after device boot. See Table 1-37.
1	xto_dis	This bit disables an unsupported time-out monitor in the oscillator. This bit must be set high by software after device boot. See Table 1-40.
0	en	This bit enables the 4 - 25 MHz crystal oscillator circuit when set high. This bit must be set high by software after device boot. See Table 1-36.

Table 1-36. Bit field encoding: EN_ENUM

Value	Name	Description
1'b0	EN_0	Not supported. This bit should not be zero for this device.
1'b1	EN_1	enabled. Note that the oscillator amplitude takes time to reach stable amplitude. This can be monitored with the XERR bit.

Table 1-37. Bit field encoding: XFB_DIS_ENUM

Value	Name	Description
1'b0	XFB_DIS_0	Not supported. This bit should not be zero for this device.
1'b1	XFB_DIS_1	disabled

Table 1-38. Bit field encoding: XPUMP_DIS_ENUM

Value	Name	Description

1.3.32 FASTCLK_XMHZ_CSR (continued)

Table 1-38. Bit field encoding: XPUMP_DIS_ENUM

1'b0	XPUMP_DIS_0	pumps Enabled. Use this setting if Vdd can be < 3V.
1'b1	XPUMP_DIS_1	pumps disabled - Only use this if Vdd will be >3V when oscillator is enabled.

Table 1-39. Bit field encoding: XSTART_ENUM

Value	Name	Description
1'b0	XSTART_0	use internal single pulse
1'b1	XSTART_1	use a clock close to the target frequency to improve start-up time.

Table 1-40. Bit field encoding: XTO_DIS_ENUM

Value	Name	Description
1'b0	XTO_DIS_0	Not supported. This bit should not be zero for this device.
1'b1	XTO_DIS_1	disabled

1.3.33 FASTCLK_XMHZ_TST

External 4-33 MHz Crystal Oscillator Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_TST: 0x40004211

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					test			

(no description)

Bits	Name	Description
3:0	test[3:0]	(no description) See Table 1-41.

Table 1-41. Bit field encoding: TEST_ENUM

Value	Name	Description
4'h0	TEST_0	High Impedance
4'h1	TEST_1	Trim current & test amplifier (production)
4'h2	TEST_2	Check startup pulses & watchdog (functional)
4'h3	TEST_3	Check amplifier NMOS (functional)
4'h4	TEST_4	Check feedback resistor (functional)
4'h5	TEST_5	Check charge pump clock and charge pump output (Production)
4'h6	TEST_6	Check charge pump output using external clock (functional)
4'h7	TEST_7	High Impedance
4'h8	TEST_8	High Impedance
4'h9	TEST_9	Brings the dc portion of the amplitude detect out, vdc (functional)
4'ha	TEST_10	Brings the peak of the amplitude detect out, vmax (functional)
4'hb	TEST_11	Brings the amplitude of the amplitude detect block out, vamp (functional)
4'hc	TEST_12	Brings the selected reference voltage, vrefout, onto the test (functional)
4'hd	TEST_13	A buffered version of the clock divider output, clk_div is put (production)
4'he	TEST_14	Allows an external voltage to be applied to the comparator (production)
4'hf	TEST_15	Checks that iadj counts down. Uses external clk to trigger (functional)

1.3.34 FASTCLK_XMHZ_CFG0

External 4-33 MHz Crystal Oscillator Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_CFG0: 0x40004212

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R/W				
Name				xcfg				

(no description)

Bits	Name	Description
4:0	xcfg[4:0]	Selects statup settings; Logic model outputs a frequency xcfg+4MHz when enabled. This is artificial as the actual frequency is determined by an attached external crystal. The values in the table are recommended settings to support various crystal types and frequencies See Table 1-42.

Table 1-42. Bit field encoding: AMPIADJ_ENUM

Value	Name	Description
5'h00	AMPIADJ_0	Reserved. not used for this device.
5'h01	AMPIADJ_1	Reserved. not used for this device.
5'h02	AMPIADJ_2	Reserved. not used for this device.
5'h03	AMPIADJ_3	Reserved. not used for this device.
5'h04	AMPIADJ_4	Reserved. not used for this device.
5'h05	AMPIADJ_5	Reserved. not used for this device.
5'h06	AMPIADJ_6	Reserved. not used for this device.
5'h07	AMPIADJ_7	Reserved. not used for this device.
5'h08	AMPIADJ_8	Reserved. not used for this device.
5'h09	AMPIADJ_9	Reserved. not used for this device.
5'h0a	AMPIADJ_10	Reserved. not used for this device.
5'h0b	AMPIADJ_11	Reserved. not used for this device.
5'h0c	AMPIADJ_12	Reserved. not used for this device.
5'h0d	AMPIADJ_13	Reserved. not used for this device.
5'h0e	AMPIADJ_14	Reserved. not used for this device.
5'h0f	AMPIADJ_15	f_crystal support for 4 to 8MHz.
5'h10	AMPIADJ_16	Reserved. not used for this device.
5'h11	AMPIADJ_17	Reserved. not used for this device.
5'h12	AMPIADJ_18	Reserved. not used for this device.
5'h13	AMPIADJ_19	Reserved. not used for this device.
5'h14	AMPIADJ_20	Reserved. not used for this device.
5'h15	AMPIADJ_21	Reserved. not used for this device.
5'h16	AMPIADJ_22	Reserved. not used for this device.
5'h17	AMPIADJ_23	Reserved. not used for this device.
5'h18	AMPIADJ_24	Reserved. not used for this device.
5'h19	AMPIADJ_25	f_crystal support for 8 to 25 MHz.
5'h1a	AMPIADJ_26	Reserved. not used for this device.
5'h1b	AMPIADJ_27	Reserved. not used for this device.
5'h1c	AMPIADJ_28	Reserved. not used for this device.
5'h1d	AMPIADJ_29	Reserved. not used for this device.
5'h1e	AMPIADJ_30	Reserved. not used for this device.

1.3.34 FASTCLK_XMHZ_CFG0 (continued)

Table 1-42. Bit field encoding: AMPIADJ_ENUM

5'h1f	AMPIADJ_31	Reserved. not used for this device.

1.3.35 FASTCLK_XMHZ_CFG1

RESERVED REGISTER LOCATION NOT USED IN THIS DEVICE

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_CFG1: 0x40004213

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R/W			
Name					RESERVED			

(no description)

Bits	Name	Description
3:0	RESERVED[3:0]	RESERVED

1.3.36 FASTCLK_PLL_CFG0

PLL Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_CFG0: 0x40004220

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:01		R/W:01		NA:000			R/W:0
HW Access	R		R		NA			R
Name	wait		delay					en

This register provides status and control for the PLL.

Bits	Name	Description
7:6	wait[1:0]	Lock detect wait time before declaring lock. PLL must show minimal phase error for this many cycles of the PFD input clock before lock is declared. See Table 1-45.
5:4	delay[1:0]	Lock detect delay time -- approximate delay time before sampling PFD output for lock detection. See Table 1-43.
0	en	Enable PLL See Table 1-44.

Table 1-43. Bit field encoding: DELAY_ENUM

Value	Name	Description
2'h0	DELAY_3NS	3 ns delay (nominal)
2'h1	DELAY_5NS	5 ns delay
2'h2	DELAY_7NS	7 ns delay
2'h3	DELAY_8NS	8 ns delay

Table 1-44. Bit field encoding: PLL_EN_ENUM

Value	Name	Description
1'b0	PLL_EN_DISABLE	PLL Disabled
1'b1	PLL_EN_ENABLE	PLL Enabled

Table 1-45. Bit field encoding: WAIT_ENUM

Value	Name	Description
2'h0	WAIT_0	7 PFD-clock periods (PFD clock period = 1 us if PFD input clock is 1 MHz)
2'h1	WAIT_1	15 PFD-clock periods
2'h2	WAIT_2	23 PFD-clock periods
2'h3	WAIT_3	31 PFD-clock periods

1.3.37 FASTCLK_PLL_CFG1

PLL Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_CFG1: 0x40004221

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:100			NA:00		R/W:10	
HW Access	NA	R			NA		R	
Name		icpsel					vco_gain	

This register sets trim levels and test modes in the PLL.

Bits	Name	Description
6:4	icpsel[2:0]	Charge Pump current select See Table 4-6 of BROS
1:0	vco_gain[1:0]	VCO loop gain

1.3.38 FASTCLK_PLL_P

PLL P-Counter Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_P: 0x40004222

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000011							
HW Access	R							
Name	p							

This register sets the P-Counter value, an 8-bit feedback divider

Bits	Name	Description
7:0	p[7:0]	P-Counter divide value. Settings less than 4 do not give valid outputs. Valid range is 4 - 255, but this must still give a divided frequency of 1 - 3 MHz (PLLOUT / P); this is the limit of the implementation. f_out = f_in*(P/Q) See Table 1-46.

Table 1-46. Bit field encoding: P_ENUM

Value	Name	Description
8'h04	P_DIV4	Divide by 4 (minimum valid value)
8'h05	P_DIV5	Divide by 5
8'h06	P_DIV6	Divide by 6
8'h07	P_DIV7	Divide by 7
8'h0f	P_DIV15	Divide by 15
8'hfe	P_DIV254	Divide by 254
8'hff	P_DIV255	Divide by 255

1.3.39 FASTCLK_PLL_Q

PLL Q-Counter Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_Q: 0x40004223

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0011			
HW Access	NA				R			
Name					q			

This register sets the Q-Counter value, a 4-bit divider on the input clock to the PLL.

Bits	Name	Description
3:0	q[3:0]	Q-Counter divide value. PLL input clock / Q must be in the range of 1 - 3 MHz. f_out = f_in*(P/Q) See Table 1-47.

Table 1-47. Bit field encoding: Q_ENUM

Value	Name	Description
4'h0	Q_DIV1	Divide by 1
4'h1	Q_DIV2	Divide by 2
4'h2	Q_DIV3	Divide by 3
4'h3	Q_DIV4	Divide by 4
4'h4	Q_DIV5	Divide by 5
4'h5	Q_DIV6	Divide by 6
4'h6	Q_DIV7	Divide by 7
4'h7	Q_DIV8	Divide by 8
4'h8	Q_DIV9	Divide by 9
4'h9	Q_DIV10	Divide by 10
4'ha	Q_DIV11	Divide by 11
4'hb	Q_DIV12	Divide by 12
4'hc	Q_DIV13	Divide by 13
4'hd	Q_DIV14	Divide by 14
4'he	Q_DIV15	Divide by 15
4'hf	Q_DIV16	Divide by 16

1.3.40 FASTCLK_PLL_TST

PLL Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_TST: 0x40004224

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						test		

(no description)

Bits	Name	Description
2:0	test[2:0]	Test Modes for the PLL. See BROS 001-08117 Table 4-12.

See Table 1-48.

Table 1-48. Bit field encoding: PLL_TEST_ENUM

Value	Name	Description
3'b000	PLL_TEST_NORMAL	Normal Operation with fast lock pre-charge
3'b001	PLL_TEST_PFD_DISABLE	PFD Disable Test (Loop filter leakage test, free-running VCO test
3'b010	PLL_TEST_VCTRL_INT	V_CTRL Internal Test Mode (Disables PFD, F_OUT=F_OFFSET+K_VCO*I_CP*(R_L+R_S)
3'b011	PLL_TEST_VCTRL_EXT	V_CTRL External Test Mode (Disables PFD, Shorts V_CTRL to external test pin)
3'b100	PLL_TEST_SENSE	Sense P Counter outputs, Sense Lock Detect Phase Error
3'b101	PLL_TEST_NORMAL_SLOW	Normal operation without fast lock pre-charge
3'b110	PLL_TEST_NORMAL_PLUS	Normal operation with fast lock circuit and with runaway detect
3'b111	PLL_TEST_CP_CURRENT	Charge Pump Current Test Mode (Disables PFD, Forces Pump UP in CP, Shorts V_CTRL to external test pin)

1.3.41 FASTCLK_PLL_SR

PLL Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

FASTCLK_PLL_SR: 0x40004225

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R:0	R:0
HW Access	NA						W	W
Name							ilock	lockdet

(no description)

Bits	Name	Description
1	ilock	Instantaneous lock signal
0	lockdet	Lock Status

1.3.42 SLOWCLK_ILO_CR0

Internal Low-speed Oscillator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_ILO_CR0: 0x40004300

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0	R/W:1	R/W:1	NA:0
HW Access	NA		R	R	NA	R	R	NA
Name			div3en	pd_mode		en_100k	en_1k	

This register controls operation of the ILO output clocks.

Register Segment: 0

Bits	Name	Description
5	div3en	Divide-by-3 enable for 100 kHz output See Table 1-49.
4	pd_mode	Power down mode for ILO See Table 1-50.
2	en_100k	Enables 100kHz ILO clock output when set. When clear, clock output is low.
1	en_1k	Enables 1kHz ILO clock output when set. When clear, clock output is low.

Table 1-49. Bit field encoding: DIV3EN_ENUM

Value	Name	Description
1'b0	DIV3EN_0	CLK33K disabled
1'b1	DIV3EN_1	CLK33K enabled, divides CLK100K by 3

Table 1-50. Bit field encoding: PD_MODE_ENUM

Value	Name	Description
1'b0	PD_MODE_0	Faster start-up, internal bias left on
1'b1	PD_MODE_1	Slower start-up, internal bias off

1.3.43 SLOWCLK_ILO_CR1

Internal Low-speed Oscillator Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_ILO_CR1: 0x40004301

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R/W	R	R
Name						freq_sel	bias_opt	dis_turbo

This register controls non-standard features of the ILO.

Register Segment: 0

Bits	Name	Description
2	freq_sel	Frequency select for CLK100K See Table 1-53.
1	bias_opt	Alternate bias for ILO See Table 1-51.
0	dis_turbo	Start-up speed control See Table 1-52.

Table 1-51. Bit field encoding: BIAS_OPT_ENUM

Value	Name	Description
1'b0	BIAS_OPT_0	sub-threshold bias (default)
1'b1	BIAS_OPT_1	Use saturated bias

Table 1-52. Bit field encoding: DIS_TURBO_ENUM

Value	Name	Description
1'b0	DIS_TURBO_0	Turbo enabled (recommended)
1'b1	DIS_TURBO_1	Turbo disabled

Table 1-53. Bit field encoding: FREQ_SEL_ENUM

Value	Name	Description
1'b0	FREQ_SEL_0	CLK100K defaults to 100 kHz
1'b1	FREQ_SEL_1	CLK100K defaults to 32 kHz

1.3.44 SLOWCLK_X32_CR

External 32kHz Crystal Oscillator Control Register

Reset: Reset Signals Listed Below

Register : Address

SLOWCLK_X32_CR: 0x40004308

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R:0	R:0	NA:00		R/W:0	R/W:0
HW Access	NA		W	W	NA		R	R
Name			ana_stat	dig_stat			lpm	x32en

This register controls operation of the 32K Crystal Oscillator, and provides status on the oscillator's stability.

Bits	Name	Description
5	ana_stat	Indicates oscillator status, using internal analog measurement. See Table 1-54.
4	dig_stat	Indicates oscillator status, using test against a reference clock. The ILO's CLK33K must be enabled for this function to operate. See Table 1-55.
1	lpm	Power setting for 32K crystal oscillator. This setting only takes effect in sleep modes. During active modes, the oscillator always runs in high power mode. See Table 1-56.
0	x32en	32K Crystal Oscillator Enable See Table 1-57.

Reset Table

resetsignal	field(s)
System reset for retention flops [reset_all_retention]	x32en, lpm
Domain reset for non-retention flops [reset_all_nonretention]	dig_stat, ana_stat

Table 1-54. Bit field encoding: ANA_STAT_ENUM

Value	Name	Description
1'b0	ANA_STAT_0	oscillator not stable
1'b1	ANA_STAT_1	oscillator stable

Table 1-55. Bit field encoding: DIG_STAT_ENUM

Value	Name	Description
1'b0	DIG_STAT_0	oscillator not stable
1'b1	DIG_STAT_1	oscillator stable

1.3.44 SLOWCLK_X32_CR (continued)

Table 1-56. Bit field encoding: LPM_ENUM

Value	Name	Description
1'b0	LPM_0	High Power Mode
1'b1	LPM_1	Low Power Mode (Only applies in chip sleep mode)

Table 1-57. Bit field encoding: X32EN_ENUM

Value	Name	Description
1'b0	X32_EN_0	Oscillator disabled, power down
1'b1	X32_EN_1	Oscillator enabled

1.3.45 SLOWCLK_X32_CFG

External 32kHz Crystal Oscillator Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_X32_CFG: 0x40004309

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:000			R/W:01		R/W:0	R/W:0
HW Access	R	NA			R		R	R
Name	lp_allow				lp		test	xrefclk

This register provides options for configuring the 32kHz Crystal Oscillator block. These options are normally only used for testing or factory calibration.

Bits	Name	Description
7	lp_allow	Low power oscillator mode configuration. See Table 1-60.
3:2	lp[1:0]	GM Setting for LPM=1. See Table 1-58.
1	test	Enables a test mode to bring the internal current reference out. See Table 1-59.
0	xrefclk	Allows external clock to be driving into the crystal oscillator input, normally for test. See Table 1-61.

Table 1-58. Bit field encoding: LP_ENUM

Value	Name	Description
2'b00	LP_MIN	Lowest power setting
2'b01	LP_DEFAULT	Default setting
2'b10	LP_SLEEP	Higher power setting for sleep
2'b11	LP_MAX	Highest power setting

Table 1-59. Bit field encoding: TEST_ENUM

Value	Name	Description
1'b0	TEST_0	Normal operation
1'b1	TEST_1	Enables ref current x1000 to come to a pad for test

Table 1-60. Bit field encoding: X32_CFG_ENUM

Value	Name	Description
1'b0	LP_OFF	Low power oscillator mode allowed only in sleep mode.
1'b1	LP_ON	Low power oscillator mode allowed in active mode.

Table 1-61. Bit field encoding: XREFCLK_ENUM

Value	Name	Description
1'b0	XREFCLK_0	Normal operation
1'b1	XREFCLK_1	Signal at crystal input assumed to be a clock, which is driven to the crystal output pad and to the internal CLK32K

1.3.46 SLOWCLK_X32_TST

External 32kHz Crystal Oscillator Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_X32_TST: 0x4000430A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:11111111							
HW Access	R							
Name	test							

This register provides for DFT options for the 32kHz external crystal oscillator block.

Bits	Name	Description
7:0	test[7:0]	Test bits -- leave high for normal operation

1.3.47 BOOST_CR0

Boost Control 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR0: 0x40004320

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:11		R/W:00011				
HW Access	R/W	R/W		R/W				
Name	thump	mode		vsel				

Boost output voltage and mode control register.

Register Segment: 1

Bits	Name	Description
7	thump	Generate a 1us pulse on 0->1 transition
6:5	mode[1:0]	Boost mode select. See Table 1-62.
4:0	vsel[4:0]	Boost voltage selection See Table 1-63.

Table 1-62. Bit field encoding: mode_enum

Value	Name	Description
2'b11	MODE_ACTIVE	Active mode
2'b01	MODE_STANDBY	Standby mode
2'b00	MODE_SLEEP	Sleep mode

Table 1-63. Bit field encoding: vsel_enum

Value	Name	Description
5'b00000	VSEL_OFF	Off (0V)
5'b00001	VSEL_1_60V	1.60V
5'b00010	VSEL_1_70V	1.70V
5'b00011	VSEL_1_80V	1.80V
5'b00100	VSEL_1_90V	1.90V
5'b00101	VSEL_2_00V	2.00V
5'b00110	VSEL_2_10V	2.10V
5'b00111	VSEL_2_20V	2.20V
5'b01000	VSEL_2_30V	2.30V
5'b01001	VSEL_2_40V	2.40V
5'b01010	VSEL_2_50V	2.50V
5'b01011	VSEL_2_60V	2.60V
5'b01100	VSEL_2_70V	2.70V
5'b01101	VSEL_2_80V	2.80V
5'b01110	VSEL_2_90V	2.90V
5'b01111	VSEL_3_00V	3.00V
5'b10000	VSEL_3_10V	3.10V
5'b10001	VSEL_3_20V	3.20V
5'b10010	VSEL_3_30V	3.30V
5'b10011	VSEL_3_40V	3.40V

1.3.47 BOOST_CR0 (continued)

Table 1-63. Bit field encoding: vsel_enum

5'b10100	VSEL_3_50V	3.50V
5'b10101	VSEL_3_60V	3.60V
5'b10110	VSEL_RSVD0	reserved
5'b10111	VSEL_RSVD1	reserved
5'b11000	VSEL_4_00V	(res) 4.00V -- Boost only, Schottky diode req'd
5'b11001	VSEL_4_25V	(res) 4.25V -- Boost only, Schottky diode req'd
5'b11010	VSEL_4_50V	(res) 4.50V -- Boost only, Schottky diode req'd
5'b11011	VSEL_4_75V	(res) 4.75V -- Boost only, Schottky diode req'd
5'b11100	VSEL_5_00V	5.00V -- Boost only, Schottky diode req'd
5'b11101	VSEL_5_25V	(res) 5.25V -- Boost only, Schottky diode req'd
5'b11110	VSEL_5_50V	(res) 5.50V -- Boost only, Schottky diode req'd
5'b11111	VSEL_RSVD2	reserved

1.3.48 BOOST_CR1

Boost Control 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR1: 0x40004321

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:1	R/W:0	R/W:01	
HW Access	R/W				R/W	R/W	R/W	
Name	tst				boosten	extmode	clk	

Boost test, clock, and mode control register.

Register Segment: 1

Bits	Name	Description
7:4	tst[3:0]	Test mode for IV char of drive transistors. Setting tst[0] also inhibits discontinuous operation. See Table 1-65.
3	boosten	When set, enables boost operation
2	extmode	When set, enables mode control from xmode[1:0] instead of control register 1
1:0	clk[1:0]	Boost clock frequency See Table 1-64.

Table 1-64. Bit field encoding: clk_enum

Value	Name	Description
2'b00	CLK_2MHZ	2.0 MHz
2'b01	CLK_500KHZ	0.5 MHz
2'b10	CLK_125KHZ	0.125 MHz
2'b11	CLK_EXT	External

Table 1-65. Bit field encoding: tst_enum

Value	Name	Description
4'b0000	TST_OFF	Test mode off
4'b0111	TST_ST_PMOS	PMOS on (strong)
4'b0110	TST_WE_PMOS	PMOS on (weak)
4'b0101	TST_ST_NMOS	NMOS on (strong)
4'b0100	TST_WE_NMOS	NMOS on (weak)

1.3.49 BOOST_CR2

Boost Control 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR2: 0x40004322

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0	R:0	R:0	R:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	disc	boosting	equal	bucking	erefsel	limoff	eqoff	enatm

Boost configuration and status register. The lower 4 bits are advanced configuration and the upper 4 bits are status.

Register Segment: 1

Bits	Name	Description
7	disc	When set, boost converter is operating in discontinuous mode
6	boosting	When set, converter is boosting (Vin < Vsel)
5	equal	When set, converter is bypassed (Vin=Vsel). Vin connected to Vout
4	bucking	When set, converter is bucking. This is always 0 for boost only converters.
3	erefsel	When set, selects external reference See Table 1-66.
2	limoff	When set, turns off skip cycle current limiter
1	eqoff	When set, disables auto battery connect to output when Vin=Vsel
0	enatm	When set, enables automatic standby regulator (See BROS)

Table 1-66. Bit field encoding: BOOST_EREFSEL_ENUM

Value	Name	Description
1'b0	BOOST_EREFSEL_INTERNAL	Select internal reference
1'b1	BOOST_EREFSEL_EXTERNAL	Select external 800mv precision reference (vref_800mv)

1.3.50 BOOST_CR3

Boost Control 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR3: 0x40004323

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	pwm							

Boost PWM value (not written during normal operation).

Register Segment: 1

Bits	Name	Description
7:0	pwm[7:0]	PWM value should not be written during normal operation.

1.3.51 BOOST_SR

Boost Status

Reset: N/A

Register : Address

BOOST_SR: 0x40004324

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:U	R:U	R:U	R:U	R:U	R:U	R:U	R:U
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ready	start	nobat	ov	vhi	vnom	vlo	uv

Boost status, including window comparator results.

Bits	Name	Description
7	ready	When set, internal circuits have been initialized
6	start	When set, converter is in startup mode
5	nobat	When set, battery input is grounded (no battery present)
4	ov	Output above overvoltage limit when 1, below limit when 0
3	vhi	Output is above vhigh limit when 1, below limit when 0
2	vnom	Output is above nominal when 1, below nominal when 0
1	vlo	Output is above vlow limit when 1, below limit when 0
0	uv	Output is above undervoltage limit when 1, below limit when 0

1.3.52 PWRSYS_CR0

Power System Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_CR0: 0x40004330

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:000			R/W:0
HW Access	NA		R	R	NA			R
Name			ext_vccd	ext_vcca				rbbnw_dis

This register controls the voltage regulators.

Register Segment: 0

Bits	Name	Description
5	ext_vccd	When set, the core digital (vccd) pin is driven with an externally regulated voltage. This disables the internal LDO-D regulator.
4	ext_vcca	When set, the core analog (vcca) pin is driven with an externally regulated voltage. This disables the internal LDO-A regulator.
0	rbbnw_dis	When set, disables the nwell reverse biasing during low power modes. Nwell reverse biasing is always disabled during active/standby modes.

1.3.53 PWRSYS_CR1

Power System Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_CR1: 0x40004331

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						i2creg_en	ldoa_dis	lvref_on_ldod

This register controls the voltage regulators.

Register Segment: 1

Bits	Name	Description
2	i2creg_en	When set, enables the I2C regulator
1	ldoa_dis	When set, disables the analog LDO regulator. This bit will not be set unless the lvref_on_ldod field is already set. Attempts to set this field while simultaneously clearing lvref_on_ldod will be ignored.
0	lvref_on_ldod	When set, the LV reference (bandgap) is supplied by the digital LDO. This can result in degraded accuracy, as described in the Power Modes chapter. All LV analog should be first marked un-available because the PRES-A is also disabled when this field is set. Once set, cannot be cleared unless ldoa_dis is already clear.

1.3.54 PM_TW_CFG0

Timewheel Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG0: 0x40004380

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R				
Name				ftw_interval				

This register controls settings for the fast timewheel. If using low power active (LPA) mode, the fast timewheel must be used to program the burst period.

Register Segment: 1

Bits	Name	Description
4:0	ftw_interval[4:0]	Sets the fast timewheel interval. The fast timewheel is programmed using a 5-bit terminal count (N-1) and is clocked by the ILO at 100 kHz. When the terminal count is reached, the timewheel automatically resets and begins counting again. This value can only be changed when {PM.TW_CFG2}.ftw_en is clear. After enabling, the duration before the first event is between 1 and 2 additional cycles, depending on synchronization with the ILO clock. Additional events occur periodically with a period of (1+ftw_interval).

1.3.55 PM_TW_CFG1

Timewheel Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG1: 0x40004381

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:1001			
HW Access	NA				R			
Name					ctw_interval			

This register controls settings for the central timewheel.

Register Segment: 1

Bits	Name	Description
3:0	ctw_interval[3:0]	Sets the central timewheel interval. The period is based on the ILO running at 1 kHz. When the interval is reached, it is automatically restarted. The first interval can range from 1 to (period + 1) ms. Additional intervals occur at the nominal period. This value can only be changed when {TW_CFG2}.ctw_en is clear. See Table 1-67.

Table 1-67. Bit field encoding: ctw_interval_enum

Value	Name	Description
4'b0000	CTW_1_TICK	not presently supported ==> is same as CTW_2_TICKS
4'b0001	CTW_2_TICKS	2 CTW ticks ==> 2ms (nominal)
4'b0010	CTW_4_TICKS	4 CTW ticks ==> 4ms (nominal)
4'b0011	CTW_8_TICKS	8 CTW ticks ==> 8ms (nominal)
4'b0100	CTW_16_TICKS	16 CTW ticks ==> 16ms (nominal)
4'b0101	CTW_32_TICKS	32 CTW ticks ==> 32ms (nominal)
4'b0110	CTW_64_TICKS	64 CTW ticks ==> 64ms (nominal)
4'b0111	CTW_128_TICKS	128 CTW ticks ==> 128ms (nominal)
4'b1000	CTW_256_TICKS	256 CTW ticks ==> 256ms (nominal)
4'b1001	CTW_512_TICKS	512 CTW ticks ==> 512ms (nominal)
4'b1010	CTW_1024_TICKS	1024 CTW ticks ==> 1024ms (nominal)
4'b1011	CTW_2048_TICKS	2048 CTW ticks ==> 2048ms (nominal)
4'b1100	CTW_4096_TICKS	4096 CTW ticks ==> 4096ms (nominal)

1.3.56 PM_TW_CFG2

Timewheel Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG2: 0x40004382

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Name			onepps_ie	onepps_en	ctw_ie	ctw_en	ftw_ie	ftw_en

This register controls settings for the central and fast timewheels.

Register Segment: 1

Bits	Name	Description
5	onepps_ie	When set and one pulse-per-second is enabled, an interrupt is issued when the pulse occurs. If onepps_en is not enabled, no interrupt is generated.
4	onepps_en	When set, the system returns to the active global power mode once every second. The 32 kHz external crystal oscillator must be enabled to use the one pulse-per-second function.
3	ctw_ie	When set and the central timewheel is enabled, an interrupt is issued when the central timewheel reaches the selected interval. If ctw_en is not enabled, no interrupt is generated.
2	ctw_en	When set, the system returns to the active global power mode when the central timewheel reaches the interval selected in {PM.TW_CFG1}.ctw_interval. The ILO 1 kHz clock source must be enabled to use the central timewheel.
1	ftw_ie	When set and the fast timewheel is enabled, an interrupt is issued when it reaches the terminal count. If ftw_en is not enabled, no interrupt is generated. This bit is ignored when LPA is enabled, and no interrupts are issued.
0	ftw_en	When set, the system returns to the active global power mode when the fast timewheel reaches the terminal count selected in {PM.TW_CFG0}.ftw_interval. This bit should be set when using Low Power Active (lpa) mode, since the fast timewheel is usually used to control the LPA burst period. The ILO 100 kHz clock source must be enabled to use the fast timewheel.

1.3.57 PM_WDT_CFG

Watchdog Timer Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WDT_CFG: 0x40004383

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	NA:0	R/W:0	R/W:0	NA:00		R/W:01	
HW Access	R	NA	R	R	NA		R	
Name	ctw_reset		wdt_lpmode	wdr_en			wdt_interval	

This register controls the watchdog timer (WDT) settings.

Register Segment: 0

Bits	Name	Description
7	ctw_reset	When a one is written to this field, the free-running central timewheel counter is reset to 0 and held there. Firmware must then write a zero to exit the reset state. Since the central timewheel is used for many timing tasks (including buzz timing and WDT), care must be taken when resetting it. It is generally recommended to reset it only once when the watchdog is enabled, to ensure that first watchdog period is full. Always reads as zero.
5	wdt_lpmode	When clear, the system will automatically use the longest WDT interval during sleep mode. It will also automatically feed the WDT when entering sleep mode. Upon wakeup, the interval will remain at the highest setting until the WDT is fed by the user. At this point, the system will automatically return to the normal wdt_interval setting. When this field is set, the system does not automatically change the interval or feed the WDT when entering sleep. This field cannot be changed once {PM.WDT_CFG}.wdr_en is set.
4	wdr_en	When set, enables the watchdog reset (WDR) using the current WDT settings. Once enabled, the WDT cannot be disabled except by a reset. Setting this bit automatically enables the ILO 1 kHz clock source.
1:0	wdt_interval[1:0]	Selects the central timewheel taps that control the WDT period. The accuracy of the intervals are dependent upon the accuracy of the oscillator used. A watchdog reset (WDR) may be issued at any time within the selected interval, so software should be programmed to service the WDT before the lower bound is reached (two tap periods). A WDR is always issued within three tap periods. Once {PM.WDT_CFG}.wdr_en is set, the watchdog interval cannot be changed. See Table 1-68.

Table 1-68. Bit field encoding: wdt_interval_enum

Value	Name	Description
2'b00	WDT_2_TICKS	2 CTW ticks ==> 4ms - 6ms
2'b01	WDT_16_TICKS	16 CTW ticks ==> 32ms - 48ms
2'b10	WDT_128_TICKS	128 CTW ticks ==> 256ms - 384ms
2'b11	WDT_1024_TICKS	1024 CTW ticks ==> 2.048s - 3.072s

1.3.58 PM_WDT_CR

Watchdog Timer Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WDT_CR: 0x40004384

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOC:00000000							
HW Access	NA							
Name	wdt_clear							

This register is used to feed the watchdog timer (WDT).

Register Segment: 1

Bits	Name	Description
7:0	wdt_clear[7:0]	Any write to this field feeds the WDT. After each feeding, there are at least two entire watchdog timer tap periods before a WDR occurs. Always reads as zero.

1.3.59 PM_INT_SR

Power Manager Interrupt Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_INT_SR: 0x40004390

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0	NA:000			RC:0	RC:0	RC:0	RC:0
HW Access	R/W	NA			R/W	R/W	R/W	R/W
Name	react_int				limact_int	onepps_int	ctw_int	ftw_int

This register indicates which interrupts occured since the last read of the register. All bits are automatically cleared on read. If an interrupt gets generated at the same time as a clear, the bit will remain set (which causes another interrupt).

Bits	Name	Description
7	react_int	When set, PM generated an interrupt to CM3 to wake CM3 when device has moved from limited active to active mode. Register should be read to avoid unintended interrupt at a later time. Sticky (whole field)
3	limact_int	When set, a limited active ready event has occured. The setting of limact_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)
2	onepps_int	When set, a onepps event has occured. The setting of onepps_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)
1	ctw_int	When set, a central timewheel event has occured. The setting of ctw_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)
0	ftw_int	When set, a fast timewheel event has occured. The setting of ftw_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)

1.3.60 PM_MODE_CFG0

Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_MODE_CFG0: 0x40004391

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	lpa_cycles							

This register controls settings for the low power modes.

Register Segment: 1

Bits	Name	Description
7:0	lpa_cycles[7:0]	A setting of N causes (N+1) cycles to execute during each burst

1.3.61 PM_MODE_CFG1

Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_MODE_CFG1: 0x40004392

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				dis_simpwr	limact_ie	lp_wake	lpa_fie	lpa_en

This register controls settings for the low power modes.

Register Segment: 1

Bits	Name	Description
4	dis_simpwr	Setting this bit will disable simulated power modes during test mode. This bit can only be set in test mode.
3	limact_ie	Setting this bit will issue an interrupt when the system can return from limited active to fully active mode. To reliably generate the interrupt, this bit should be set prior to entering idle mode.
2	lp_wake	Setting this bit will automatically deactivate all subsystems when returning from hibernate, sleep, or idle modes. Subsystems can later be reactivated using {PM.MODE_CSR}.reactivate.
1	lpa_fie	When clear, interrupts are held off until next burst. This increases average interrupt latency, as compared to an active mode baseline design with identical throughput. When set, interrupts return the system to active mode, the on-time counter is reset, and the system will execute at least N cycles.
0	lpa_en	When set, LPA mode is enabled. LPA mode is compatible with all global power modes. If standby mode is specified, it is interpreted as an early return to standby, and the LPA scheduler will wake the system on the original schedule. If idle, sleep, or hibernate modes are specified, LPA is temporarily paused and resumed upon wakeup. Clearing this bit immediately disables LPA.

1.3.62 PM_MODE_CSR

Power Mode Control/Status Register

Reset: Reset Signals Listed Below

Register : Address

PM_MODE_CSR: 0x40004393

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WC:1	R:0	NA:0	R/WOC:0	R:0	R/W:000		
HW Access	W	W	NA	R	W	R/W		
Name	nonret_rst	limact_mode		reactivate	sim_mode	lp_mode		

This register controls settings for the global power mode.

Register Segment: 1

Bits	Name	Description
7	nonret_rst	Persistent status bit that indicates a non-retention reset occured for some chip registers. This bit is preset high by any chip reset, and it is cleared whenever the register is written. When the system automatically resets non-retention registers (such as when returning from low power modes or a reactivation), this field is set high to indicate some register state has changed. Sticky (whole field)
6	limact_mode	When set, the chip is in limited active mode. Some subsystems and domains are unavailable in this mode. A reactivation is required to return the chip to active mode.
4	reactivate	Setting this bit reactivates subsystems with pending availability. This is used to transition from limited active to active mode or to initiate the delayed activation procedure after change(s) to PM_AVAIL* register(s). The reactivation process simulates a transition from sleep to active mode. During the simulated transition, user clocks are stopped. After completion, the system is in active mode regardless of the LP_MODE setting. This bit always reads as zero.
3	sim_mode	When set, the chip is simulating power modes. Refer to the power mode chapter for details on simulated power modes.
2:0	lp_mode[2:0]	Sets the global power mode. See Table 1-69.

Reset Table

resetsignal	field(s)
System reset for retention flops [reset_all_retention]	lp_mode[2:0], sim_mode, reactivate, limact_mode
Domain reset for non-retention flops [reset_all_nonretention]	nonret_rst

Table 1-69. Bit field encoding: mode_enum

Value	Name	Description
3'b000	MODE_ACTIVE	Active mode
3'b001	MODE_STANDBY	Standby mode

1.3.62 PM_MODE_CSR (continued)

Table 1-69. Bit field encoding: mode_enum

3'b010	MODE_IDLE	Idle mode
3'b011	MODE_SLEEP	Sleep mode
3'b100	MODE_HIBERNATE	Hibernate mode
3'b110	MODE_HIBTIMERS	Hibernate+timewheels

1.3.63 PM_ACT_CFG0

Active Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG0: 0x400043A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1	R/W:0	R/W:0	R/W:1	R/W:0	R/W:1	R/W:1	R/W:1
HW Access	R	R	R	R	R	R	R	R
Name	en_fm_ee	en_udbarray	en_imo36m	en_imo	en_clk_spc	en_clk_bus	en_cpu	en_ic

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
7	en_fm_ee	Global enable for flash/EE.
6	en_udbarray	Global enable for UDB array.
5	en_imo36m	Enable IMO SPC clock source. Requires setting en_imo, as well.
4	en_imo	Enable IMO clock source
3	en_clk_spc	Enable clk_spc. This also internally enables the 36MHz IMO (similar to en_imo36m), since this is required for the SPC to function.
2	en_clk_bus	Enable clk_bus
1	en_cpu	Enable CPU. This also enables the flash, since the CPU requires the flash to function.
0	en_ic	Enable interrupt controller

1.3.64 PM_ACT_CFG1

Active Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG1: 0x400043A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_clk_a			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_clk_a[3:0]	Enable clk_a[3:0]

1.3.65 PM_ACT_CFG2

Active Power Mode Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG2: 0x400043A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	en_clk_d							

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
7:0	en_clk_d[7:0]	Enable clk_d[7:0]

1.3.66 PM_ACT_CFG3

Active Power Mode Configuration Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG3: 0x400043A3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_timer			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_timer[3:0]	Enable timer/counters.

1.3.67 PM_ACT_CFG4

Active Power Mode Configuration Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG4: 0x400043A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_abuf			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_abuf[3:0]	Enable analog linear output buffer.

1.3.68 PM_ACT_CFG5

Active Power Mode Configuration Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG5: 0x400043A5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		en_emif		en_lcd		en_i2c		en_fsusb

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
6	en_emif	Enable EMIF
4	en_lcd	Enable LCD.
2	en_i2c	Enable I2C block(s). Populated subsystems are counted from the LSB.
0	en_fsusb	Enable FS-USB.

1.3.69 PM_ACT_CFG6

Active Power Mode Configuration Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG6: 0x400043A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:000			R/W:0
HW Access	NA			R	NA			R
Name				en_dfb				en_can

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
4	en_dfb	Enable DFB(s). Populated subsystems are counted from the LSB.
0	en_can	Enable CAN block(s). Populated subsystems are counted from the LSB.

1.3.70 PM_ACT_CFG7

Active Power Mode Configuration Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG7: 0x400043A7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_cmp			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_cmp[3:0]	Enable comparator(s). Populated subsystems are counted from the LSB. Bits 1 and 2 are reversed. On these parts, bit 1 controls comparator2 and bit 2 controls comparator1.

1.3.71 PM_ACT_CFG8

Active Power Mode Configuration Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG8: 0x400043A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_dac			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_dac[3:0]	Enable DAC block(s). Populated subsystems are counted from the LSB.

1.3.72 PM_ACT_CFG9

Active Power Mode Configuration Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG9: 0x400043A9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_swcap			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_swcap[3:0]	Enable switchcap block(s). Populated subsystems are counted from the LSB. Bits 1 and 2 are reversed. On these parts, bit 1 controls swcap2 and bit 2 controls swcap1.

1.3.73 PM_ACT_CFG10

Active Power Mode Configuration Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG10: 0x400043AA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								en_dec

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
0	en_dec	Enable decimator(s). Populated subsystems are counted from the LSB.

1.3.74 PM_ACT_CFG11

Active Power Mode Configuration Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG11: 0x400043AB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:00		R/W:00	
HW Access	NA		R	R	NA		R	
Name			en_refbufr	en_refbufl			en_sar	

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
5	en_refbufr	Enable RIGHT analog reference buffer (refbufr)
4	en_refbufl	Enable LEFT analog reference buffer (refbufl)
1:0	en_sar[1:0]	Enable SAR(s). Populated subsystems are counted from the LSB.

1.3.75 PM_STBY_CFG0

Standby Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG0: 0x400043B0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	en_fm_ee	en_udbarray	en_imo36m	en_imo	en_clk_spc	en_clk_bus	en_cpu	en_ic

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
7	en_fm_ee	Global enable for flash/EE.
6	en_udbarray	Global enable for UDB array.
5	en_imo36m	Enable IMO SPC clock source. Requires setting en_imo, as well.
4	en_imo	Enable IMO clock source
3	en_clk_spc	Enable clk_spc. This also internally enables the 36MHz IMO (similar to en_imo36m), since this is required for the SPC to function.
2	en_clk_bus	Enable clk_bus
1	en_cpu	Enable CPU. This also enables the flash, since the CPU requires the flash to function.
0	en_ic	Enable interrupt controller

1.3.76 PM_STBY_CFG1

Standby Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG1: 0x400043B1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_clk_a			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_clk_a[3:0]	Enable clk_a[3:0]

1.3.77 PM_STBY_CFG2

Standby Power Mode Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG2: 0x400043B2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	en_clk_d							

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
7:0	en_clk_d[7:0]	Enable clk_d[7:0]

1.3.78 PM_STBY_CFG3

Standby Power Mode Configuration Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG3: 0x400043B3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_timer			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_timer[3:0]	Enable timer/counters.

1.3.79 PM_STBY_CFG4

Standby Power Mode Configuration Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG4: 0x400043B4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_abuf			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_abuf[3:0]	Enable analog linear output buffer.

1.3.80 PM_STBY_CFG5

Standby Power Mode Configuration Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG5: 0x400043B5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		en_emif		en_lcd		en_i2c		en_fsusb

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
6	en_emif	Enable EMIF
4	en_lcd	Enable LCD.
2	en_i2c	Enable I2C block(s). Populated subsystems are counted from the LSB.
0	en_fsusb	Enable FS-USB.

1.3.81 PM_STBY_CFG6

Standby Power Mode Configuration Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG6: 0x400043B6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:000			R/W:0
HW Access	NA			R	NA			R
Name				en_dfb				en_can

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
4	en_dfb	Enable DFB(s). Populated subsystems are counted from the LSB.
0	en_can	Enable CAN block(s). Populated subsystems are counted from the LSB.

1.3.82 PM_STBY_CFG7

Standby Power Mode Configuration Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG7: 0x400043B7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_cmp			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_cmp[3:0]	Enable comparator(s). Populated subsystems are counted from the LSB. Bits 1 and 2 are reversed. On these parts, bit 1 controls comparator2 and bit 2 controls comparator1.

1.3.83 PM_STBY_CFG8

Standby Power Mode Configuration Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG8: 0x400043B8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_dac			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_dac[3:0]	Enable DAC block(s). Populated subsystems are counted from the LSB.

1.3.84 PM_STBY_CFG9

Standby Power Mode Configuration Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG9: 0x400043B9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					en_swcap			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
3:0	en_swcap[3:0]	Enable switchcap block(s). Populated subsystems are counted from the LSB. Bits 1 and 2 are reversed. On these parts, bit 1 controls swcap2 and bit 2 controls swcap1.

1.3.85 PM_STBY_CFG10

Standby Power Mode Configuration Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG10: 0x400043BA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								en_dec

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
0	en_dec	Enable decimator(s). Populated subsystems are counted from the LSB.

1.3.86 PM_STBY_CFG11

Standby Power Mode Configuration Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG11: 0x400043BB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:00		R/W:00	
HW Access	NA		R	R	NA		R	
Name			en_refbufr	en_refbufl			en_sar	

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Register Segment: 1

Bits	Name	Description
5	en_refbufr	Enable RIGHT analog reference buffer (refbufr)
4	en_refbufl	Enable LEFT analog reference buffer (refbufl)
1:0	en_sar[1:0]	Enable SAR(s). Populated subsystems are counted from the LSB.

1.3.87 PM_AVAIL_CR0

Power Mode Available Subsystem Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR0: 0x400043C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:1111			
HW Access	NA				R			
Name					en_fm			

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Register Segment: 1

Bits	Name	Description
3:0	en_fm[3:0]	Each set bit requests a flash macro be available. Reactivation is delayed. Macro 0 can only be disabled during test_mode.

1.3.88 PM_AVAIL_CR1

Power Mode Available Subsystem Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR1: 0x400043C1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:1111			
HW Access	NA				R			
Name					en_sysmem			

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Register Segment: 1

Bits	Name	Description
3:0	en_sysmem[3:0]	Each set bit requests a sysmem macro be available. Reactivation is delayed. Populated subsystems are counted from the LSB.

1.3.89 PM_AVAIL_CR2

Power Mode Available Subsystem Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR2: 0x400043C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:1	NA:000			R/W:1
HW Access	NA			R	NA			R
Name				en_udb				en_ee

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Register Segment: 1

Bits	Name	Description
4	en_udb	Each set bit requests a UDB bank be available. Reactivation is delayed.
0	en_ee	Each set bit requests a EEPROM macro be available. Reactivation is delayed.

1.3.90 PM_AVAIL_CR3

Power Mode Available Subsystem Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR3: 0x400043C3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:1
HW Access	NA							R
Name								en_dfb

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Register Segment: 1

Bits	Name	Description
0	en_dfb	Each set bit requests a DFB be available. Reactivation is delayed.

1.3.91 PM_AVAIL_CR4

Power Mode Available Subsystem Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR4: 0x400043C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:1	NA:0	R/W:1	NA:0	R/W:1
HW Access	NA			R/W	NA	R	NA	R
Name						en_main		en_spc

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Register Segment: 1

Bits	Name	Description
4	RSVD	This bit is reserved and should stay set to the reset value of 1.
2	en_main	When set, requests main domain be available. Can only be disabled in test mode. Reactivation is delayed.
0	en_spc	When set, requests SPC be available. Can only be disabled in test mode. Reactivation is delayed.

1.3.92 PM_AVAIL_CR5

Power Mode Available Subsystem Control Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR5: 0x400043C5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:1
HW Access	NA							R
Name								en_dsm

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Register Segment: 1

Bits	Name	Description
0	en_dsm	Each set bit requests a delsig channel be available. Reactivation is immediate.

1.3.93 PM_AVAIL_CR6

Power Mode Available Subsystem Control Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR6: 0x400043C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:1	NA:0	R/W:1	R/W:1	R/W:1
HW Access	NA			W	NA	R	R	R
Name				en_fsusbio		en_analcd	en_anapump	en_anamisc

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Register Segment: 1

Bits	Name	Description
4	en_fsusbio	When set, requests FSUSB IO be available. Reactivation is immediate.
2	en_analcd	When set, requests LCD be available. Reactivation is immediate.
1	en_anapump	When set, requests analog pump be available. Reactivation is immediate.
0	en_anamisc	When set, requests miscellaneous analog be available. Reactivation is immediate.

1.3.94 PM_AVAIL_SR0

Power Mode Available Subsystem Status Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR0: 0x400043D0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:1111			
HW Access	NA				W			
Name					en_fm			

This register indicates whether a subsystem is available or not.

Bits	Name	Description
3:0	en_fm[3:0]	Each set bit indicates an available flash macro.

1.3.95 PM_AVAIL_SR1

Power Mode Available Subsystem Status Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR1: 0x400043D1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:1111			
HW Access	NA				W			
Name					en_sysmem			

This register indicates whether a subsystem is available or not.

Bits	Name	Description
3:0	en_sysmem[3:0]	Each set bit requests a sysmem macro be available. Reactivation is delayed. Populated subsystems are counted from the LSB.

1.3.96 PM_AVAIL_SR2

Power Mode Available Subsystem Status Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR2: 0x400043D2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:1	NA:000			R:1
HW Access	NA			W	NA			W
Name				en_udb				en_ee

This register indicates whether a subsystem is available or not.

Bits	Name	Description
4	en_udb	Each set bit indicates an available UDB bank.
0	en_ee	Each set bit indicates an available EEPROM macro.

1.3.97 PM_AVAIL_SR3

Power Mode Available Subsystem Status Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR3: 0x400043D3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R:1
HW Access	NA							W
Name								en_dfb

This register indicates whether a subsystem is available or not.

Bits	Name	Description
0	en_dfb	Each set bit indicates an available DFB.

1.3.98 PM_AVAIL_SR4

Power Mode Available Subsystem Status Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR4: 0x400043D4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:1	NA:0	R:1	NA:0	R:1
HW Access	NA			W	NA	W	NA	W
Name				en_i2c		en_main		en_spc

This register indicates whether a subsystem is available or not.

Bits	Name	Description
4	en_i2c	When set, I2C is available.
2	en_main	When set, main domain is available.
0	en_spc	When set, SPC is available.

1.3.99 PM_AVAIL_SR5

Power Mode Available Subsystem Status Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR5: 0x400043D5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R:1
HW Access	NA							W
Name								en_dsm

This register indicates whether a subsystem is available or not.

Bits	Name	Description
0	en_dsm	Each set bit indicates an available delsig channel.

1.3.100 PM_AVAIL_SR6

Power Mode Available Subsystem Status Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR6: 0x400043D6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:1	NA:0	R:1	R:1	R:1
HW Access	NA			W	NA	W	W	W
Name				en_fsusbio		en_analcd	en_anapump	en_anamisc

This register indicates whether a subsystem is available or not.

Bits	Name	Description
4	en_fsusbio	When set, FSUSB IO is available.
2	en_analcd	When set, LCD is available.
1	en_anapump	When set, analog pump is available.
0	en_anamisc	When set, miscellaneous analog is available.

1.3.101 PICU[0..15]_INTTYPE[0..7]

Port Interrupt Control Type Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

PICU0_INTTYPE0: 0x40004500	PICU0_INTTYPE1: 0x40004501
PICU0_INTTYPE2: 0x40004502	PICU0_INTTYPE3: 0x40004503
PICU0_INTTYPE4: 0x40004504	PICU0_INTTYPE5: 0x40004505
PICU0_INTTYPE6: 0x40004506	PICU0_INTTYPE7: 0x40004507
PICU1_INTTYPE0: 0x40004508	PICU1_INTTYPE1: 0x40004509
PICU1_INTTYPE2: 0x4000450A	PICU1_INTTYPE3: 0x4000450B
PICU1_INTTYPE4: 0x4000450C	PICU1_INTTYPE5: 0x4000450D
PICU1_INTTYPE6: 0x4000450E	PICU1_INTTYPE7: 0x4000450F
PICU2_INTTYPE0: 0x40004510	PICU2_INTTYPE1: 0x40004511
PICU2_INTTYPE2: 0x40004512	PICU2_INTTYPE3: 0x40004513
PICU2_INTTYPE4: 0x40004514	PICU2_INTTYPE5: 0x40004515
PICU2_INTTYPE6: 0x40004516	PICU2_INTTYPE7: 0x40004517
PICU3_INTTYPE0: 0x40004518	PICU3_INTTYPE1: 0x40004519
PICU3_INTTYPE2: 0x4000451A	PICU3_INTTYPE3: 0x4000451B
PICU3_INTTYPE4: 0x4000451C	PICU3_INTTYPE5: 0x4000451D
PICU3_INTTYPE6: 0x4000451E	PICU3_INTTYPE7: 0x4000451F
PICU4_INTTYPE0: 0x40004520	PICU4_INTTYPE1: 0x40004521
PICU4_INTTYPE2: 0x40004522	PICU4_INTTYPE3: 0x40004523
PICU4_INTTYPE4: 0x40004524	PICU4_INTTYPE5: 0x40004525
PICU4_INTTYPE6: 0x40004526	PICU4_INTTYPE7: 0x40004527
PICU5_INTTYPE0: 0x40004528	PICU5_INTTYPE1: 0x40004529
PICU5_INTTYPE2: 0x4000452A	PICU5_INTTYPE3: 0x4000452B
PICU5_INTTYPE4: 0x4000452C	PICU5_INTTYPE5: 0x4000452D
PICU5_INTTYPE6: 0x4000452E	PICU5_INTTYPE7: 0x4000452F
PICU6_INTTYPE0: 0x40004530	PICU6_INTTYPE1: 0x40004531
PICU6_INTTYPE2: 0x40004532	PICU6_INTTYPE3: 0x40004533
PICU6_INTTYPE4: 0x40004534	PICU6_INTTYPE5: 0x40004535
PICU6_INTTYPE6: 0x40004536	PICU6_INTTYPE7: 0x40004537
PICU12_INTTYPE0: 0x40004560	PICU12_INTTYPE1: 0x40004561
PICU12_INTTYPE2: 0x40004562	PICU12_INTTYPE3: 0x40004563
PICU12_INTTYPE4: 0x40004564	PICU12_INTTYPE5: 0x40004565
PICU12_INTTYPE6: 0x40004566	PICU12_INTTYPE7: 0x40004567

1.3.101 PICU[0..15]_INTTYPE[0..7] (continued)

Register : Address

PICU15_INTTYPE0: 0x40004578	PICU15_INTTYPE1: 0x40004579
PICU15_INTTYPE2: 0x4000457A	PICU15_INTTYPE3: 0x4000457B
PICU15_INTTYPE4: 0x4000457C	PICU15_INTTYPE5: 0x4000457D
PICU15_INTTYPE6: 0x4000457E	PICU15_INTTYPE7: 0x4000457F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							INTTYPE	

This register configures the type of interrupt for a pin. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
1:0	INTTYPE[1:0]	This field configures the type of interrupt type enabled. See Table 1-70.

Table 1-70. Bit field encoding: INTTYPE_ENUM

Value	Name	Description
2'b00	DISABLE	Disable Interrupts for pin.
2'b01	RISING_EDGE	Enable Rising Edge Interrupts for pin.
2'b10	FALLING_EDGE	Enable Falling Edge Interrupts for pin.
2'b11	CHANGE_MODE	Enable Both Edge Interrupts for pin.

1.3.102 PICU[0..15]_INTSTAT

Port Interrupt Control Status Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

PICU0_INTSTAT: 0x40004580
PICU1_INTSTAT: 0x40004581
PICU2_INTSTAT: 0x40004582
PICU3_INTSTAT: 0x40004583
PICU4_INTSTAT: 0x40004584
PICU5_INTSTAT: 0x40004585
PICU6_INTSTAT: 0x40004586
PICU12_INTSTAT: 0x4000458C
PICU15_INTSTAT: 0x4000458F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0	RC:0	RC:0	RC:0	RC:0	RC:0	RC:0	RC:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0

This register provides information on the recently posted interrupts.

Bits	Name	Description
7	Interrupt Status {STAT7}	Pin 7 Interrupt Status See Table 1-71.
6	Interrupt Status {STAT6}	Pin 6 Interrupt Status See Table 1-71.
5	Interrupt Status {STAT5}	Pin 5 Interrupt Status See Table 1-71.
4	Interrupt Status {STAT4}	Pin 4 Interrupt Status See Table 1-71.
3	Interrupt Status {STAT3}	Pin 3 Interrupt Status See Table 1-71.
2	Interrupt Status {STAT2}	Pin 2 Interrupt Status See Table 1-71.
1	Interrupt Status {STAT1}	Pin 1 Interrupt Status See Table 1-71.
0	Interrupt Status {STAT0}	Pin 0 Interrupt Status See Table 1-71.

Table 1-71. Bit field encoding: INTSTAT_ENUM

Value	Name	Description
1'b1	INT_PENDING	Indicates an interrupt is pending.
1'b0	NO_INT	Indicates no interrupt is pending.

1.3.103 PICU[0..15]_SNAP

Port Interrupt Control Snap Shot Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

PICU0_SNAP: 0x40004590
PICU1_SNAP: 0x40004591
PICU2_SNAP: 0x40004592
PICU3_SNAP: 0x40004593
PICU4_SNAP: 0x40004594
PICU5_SNAP: 0x40004595
PICU6_SNAP: 0x40004596
PICU12_SNAP: 0x4000459C
PICU15_SNAP: 0x4000459F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	SNAPSHOT							

This register provides information on the state of input pins at recent read to Status register.

Bits	Name	Description
7:0	SNAPSHOT[7:0]	Contains input pin values at recent read to status register

1.3.104 CMP[0..3]_TR

Comparator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_TR: 0x40004600 CMP1_TR: 0x40004601

CMP2_TR: 0x40004602 CMP3_TR: 0x40004603

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Name	tr2				tr1			

(no description)

Bits	Name	Description
7:4	tr2[3:0]	Sets the trim value to be added to the N-type load for offset calibration See Table 1-73.
3:0	tr1[3:0]	Sets the trim value to be added to the P-type load for offset calibration See Table 1-72.

Table 1-72. Bit field encoding: TRIM1_ENUM

Value	Name	Description
4'b0000	TRIM1_0	Does not add any offset look at trim section in P3comp BROS - spec #001-11660 for accurate values and more details.
4'b0001	TRIM1_POS_SIDE_1	Adds offset of ~1mV to the positive side
4'b0010	TRIM1_POS_SIDE_2	Adds offset of ~2mV to the positive side
4'b0011	TRIM1_POS_SIDE_3	Adds offset of ~3mV to the positive side
4'b0100	TRIM1_POS_SIDE_4	Adds offset of ~4mV to the positive side
4'b0101	TRIM1_POS_SIDE_5	Adds offset of ~5mV to the positive side
4'b0110	TRIM1_POS_SIDE_6	Adds offset of ~6mV to the positive side
4'b0111	TRIM1_POS_SIDE_7	Adds offset of ~7mV to the positive side
4'b1000	TRIM1_NEG_SIDE_1	Adds offset of ~1mV to the negative side
4'b1001	TRIM1_NEG_SIDE_2	Adds offset of ~2mV to the negative side
4'b1010	TRIM1_NEG_SIDE_3	Adds offset of ~3mV to the negative side
4'b1011	TRIM1_NEG_SIDE_4	Adds offset of ~4mV to the negative side
4'b1100	TRIM1_NEG_SIDE_5	Adds offset of ~5mV to the negative side
4'b1101	TRIM1_NEG_SIDE_6	Adds offset of ~6mV to the negative side
4'b1110	TRIM1_NEG_SIDE_7	Adds offset of ~7mV to the negative side
4'b1111	TRIM1_NEG_SIDE_8	Adds offset of ~8mV to the negative side

Table 1-73. Bit field encoding: TRIM2_ENUM

Value	Name	Description
4'b0000	TRIM2_0	Does not add any offset look at trim section in P3comp BROS - spec #001-11660 for accurate values and more details.
4'b0001	TRIM2_NEG_SIDE_1	Adds offset of ~1mV to the negative side
4'b0010	TRIM2_NEG_SIDE_2	Adds offset of ~2mV to the negative side
4'b0011	TRIM2_NEG_SIDE_3	Adds offset of ~3mV to the negative side
4'b0100	TRIM2_NEG_SIDE_4	Adds offset of ~4mV to the negative side
4'b0101	TRIM2_NEG_SIDE_5	Adds offset of ~5mV to the negative side
4'b0110	TRIM2_NEG_SIDE_6	Adds offset of ~6mV to the negative side

1.3.104 CMP[0..3]_TR (continued)

Table 1-73. Bit field encoding: TRIM2_ENUM

4'b0111	TRIM2_NEG_SIDE_7	Adds offset of ~7mV to the negative side
4'b1000	TRIM2_8	Does not add any offset
4'b1001	TRIM2_POS_SIDE_1	Adds offset of ~1mV to the positive side
4'b1010	TRIM2_POS_SIDE_2	Adds offset of ~2mV to the positive side
4'b1011	TRIM2_POS_SIDE_3	Adds offset of ~3mV to the positive side
4'b1100	TRIM2_POS_SIDE_4	Adds offset of ~4mV to the positive side
4'b1101	TRIM2_POS_SIDE_5	Adds offset of ~5mV to the positive side
4'b1110	TRIM2_POS_SIDE_6	Adds offset of ~6mV to the positive side
4'b1111	TRIM2_POS_SIDE_7	Adds offset of ~7mV to the positive side

1.3.105 DAC[0..3]_TR

DAC Block Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_TR: 0x40004608 DAC1_TR: 0x40004609

DAC2_TR: 0x4000460A DAC3_TR: 0x4000460B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	tr							

(no description)

Bits	Name	Description
7:0	tr[7:0]	8 Calibration bits

1.3.106 NPUMP_DSM_TR0

Delta Sigma Modulator (DSM) Negative Pump Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NPUMP_DSM_TR0: 0x40004610

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							npump_dsm_trim	

(no description)

Bits	Name	Description
1:0	npump_dsm_trim[1:0]	Delta Sigma Modulator (DSM) Negative Pump Trim

1.3.107 NPUMP_ABUF_TR0

Analog Linear Output Buffer (ABUF) Negative Pump Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NPUMP_ABUF_TR0: 0x40004612

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							npump_abuf_trim	

(no description)

Bits	Name	Description
1:0	npump_abuf_trim[1:0]	Analog Linear Output Buffer (ABUF) Negative Pump Trim

1.3.108 SAR[0..1]_TR0

SAR trim register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_TR0: 0x40004614 SAR1_TR0: 0x40004616

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:1	R/W:111		
HW Access	NA				R	R		
Name					trimunit	cap_trim		

These trim registers are not supported in this release.

Bits	Name	Description
3	trimunit	trim See Table 1-75.
2:0	cap_trim[2:0]	Capacitance Trim See Table 1-74.

Table 1-74. Bit field encoding: SAR_CAP_TRIM_ENUM

Value	Name	Description
3'h0	SAR_CAP_TRIM_0	decrease attenuation capacitor by 0
3'h1	SAR_CAP_TRIM_1	decrease attenuation capacitor by 0.5 LSB
3'h2	SAR_CAP_TRIM_2	decrease attenuation capacitor by 2*0.5 LSB = 1 LSB
3'h3	SAR_CAP_TRIM_3	decrease attenuation capacitor by 3*0.5 LSB = 1.5 LSB
3'h4	SAR_CAP_TRIM_4	decrease attenuation capacitor by 4*0.5 LSB = 2 LSB
3'h5	SAR_CAP_TRIM_5	decrease attenuation capacitor by 5*0.5 LSB = 2.5 LSB
3'h6	SAR_CAP_TRIM_6	decrease attenuation capacitor by 6*0.5 LSB = 3.0 LSB
3'h7	SAR_CAP_TRIM_7	decrease attenuation capacitor by 7*0.5 LSB = 3.5 LSB

Table 1-75. Bit field encoding: SAR_TRIMUNIT_ENUM

Value	Name	Description
1'b0	SAR_TRIMUNIT_0	default attenuation cap
1'b1	SAR_TRIMUNIT_1	Increase by 6fF

1.3.109 ABUF[0..3]_TR0

Analog Output Buffer Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF0_TR0: 0x40004620 ABUF1_TR0: 0x40004622

ABUF2_TR0: 0x40004624 ABUF3_TR0: 0x40004626

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R				
Name				offset_trim				

(no description)

Bits	Name	Description
4:0	offset_trim[4:0]	Offset Trim: 420uV typical step size; +/- 6.8mV offset trimmable range

1.3.110 ABUF[0..3]_TR1

Analog Output Buffer Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF0_TR1: 0x40004621

ABUF1_TR1: 0x40004623

ABUF2_TR1: 0x40004625

ABUF3_TR1: 0x40004627

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							nc	

(no description)

Bits	Name	Description
1:0	nc[1:0]	To be removed - CDT 36833

1.3.111 PWRSYS_HIB_TR0

Hibernate Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_HIB_TR0: 0x40004680

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1111				R/W:0000			
HW Access	R				R			
Name	trim				biasg			

This register trims the hibernate regulator, which generates the vpwrka supply.

Register Segment: 0

Bits	Name	Description
7:4	trim[3:0]	Hibernate regulator trim.
3:0	biasg[3:0]	Hibernate regulator biasg tweak trim. During powerup hib/slp holdoff specified in PWRSYS_SLP_TR, this trim is internally forced to 4'b0001 until the hib/slp powerup holdoff is finished. This register can be written and will readback normally during the force condition (ie the force condition will not be seen during readback). After the force condition ends, the contents of this register will be applied to the hib/slp regulator.

1.3.112 PWRSYS_HIB_TR1

Hibernate Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_HIB_TR1: 0x40004681

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:1011			
HW Access	R	R			R			
Name	dis_hibernate	rbb_trim			enleg			

This register trims the hibernate regulator and reverse body bias generator.

Register Segment: 0

Bits	Name	Description
7	dis_hibernate	Setting this bit will disable hibernate mode.
6:4	rbb_trim[2:0]	Reverse body bias generator trim.
3:0	enleg[3:0]	Each set bit enables a current leg of the hibernate regulator for the keepalive supply.

1.3.113 PWRSYS_I2C_TR

I2C Regulator Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_I2C_TR: 0x40004682

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:00		R/W:11	
HW Access	NA	R			NA		R	
Name		restrim					trim	

This register trims the I2C regulator.

Register Segment: 0

Bits	Name	Description
6:4	restrim[2:0]	I2C regulator series resistor trim.
1:0	trim[1:0]	I2C regulator trim.

1.3.114 PWRSYS_SLP_TR

Sleep Regulator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_SLP_TR: 0x40004683

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:111			R/W:0	R/W:0011			
HW Access	R			R	R			
Name	hibslp_holdoff			bypass	trim			

This register trims the sleep regulator.

Register Segment: 0

Bits	Name	Description
7:5	hibslp_holdoff[2:0]	Number of 1kHz ILO clocks before the hibernate/sleep regulator is ready after a chip reset. Before it is ready, the system will ignore power mode requests except active and standby. It also overrides trim settings for the hibernate/sleep regulator. See Table 1-76.
4	bypass	When set, disables the sleep regulator and shorts vccd to vpwrsleep. This bit can only be set in test mode.
3:0	trim[3:0]	Sleep regulator trim.

Table 1-76. Bit field encoding: holdoff_enum

Value	Name	Description
3'b000	HOLDOFF0	0 clocks => 0ms (disables holdoff)
3'b001	HOLDOFF1	1 clocks => 1ms
3'b010	HOLDOFF2	2 clocks => 2ms
3'b011	HOLDOFF3	3 clocks => 3ms
3'b100	HOLDOFF4	4 clocks => 4ms
3'b101	HOLDOFF5	5 clocks => 5ms
3'b110	HOLDOFF6	6 clocks => 6ms
3'b111	HOLDOFF7	7 clocks => 7ms

1.3.115 PWRSYS_BUZZ_TR

Power Mode Buzz Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BUZZ_TR: 0x40004684

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0011				R/W:0011			
HW Access	R				R			
Name	idle_buzz				slp_buzz			

This register trims the settings for system sampling (buzzing).

Register Segment: 0

Bits	Name	Description
7:4	idle_buzz[3:0]	Sets the buzz rate for digital and analog LDOs during idle mode See Table 1-77.
3:0	slp_buzz[3:0]	Sets the buzz rate for digital and analog LDOs during sleep mode See Table 1-77.

Table 1-77. Bit field encoding: pm_pwrsys_trim_buzz_enum

Value	Name	Description
4'b0000	BUZZ_2_TICKS	2 CTW ticks ==> 2ms
4'b0001	BUZZ_4_TICKS	4 CTW ticks ==> 4ms
4'b0010	BUZZ_8_TICKS	8 CTW ticks ==> 8ms
4'b0011	BUZZ_16_TICKS	16 CTW ticks ==> 16ms
4'b0100	BUZZ_32_TICKS	32 CTW ticks ==> 32ms
4'b0101	BUZZ_64_TICKS	64 CTW ticks ==> 64ms
4'b0110	BUZZ_128_TICKS	128 CTW ticks ==> 128ms
4'b0111	BUZZ_256_TICKS	256 CTW ticks ==> 256ms
4'b1000	BUZZ_512_TICKS	512 CTW ticks ==> 512ms

1.3.116 PWRSYS_WAKE_TR0

Power Mode Wakeup Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR0: 0x40004685

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0111				R/W:1100			
HW Access	R				R			
Name	wake_ho_interval				wake_to_tap			

This register configures the settings for waking up the regulators.

Register Segment: 0

Bits	Name	Description
7:4	wake_ho_interval[3:0]	Sets the holdoff time to wait until sampling PRES-A/D. The holdoff time is 16*wake_precnt*wake_ho_interval IMO cycles running at wake_imofreq.
3:0	wake_to_tap[3:0]	Sets the timeout time to wait until releasing the ignore_pres* conditioning for the PRES-A/D. The timeout time is 16*wake_precnt*wake_to_interval IMO cycles running at wake_imofreq.

1.3.117 PWRSYS_WAKE_TR1

Power Mode Wakeup Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR1: 0x40004686

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000			R/W:000		
HW Access	NA		R			R		
Name			wake_precnt			wake_imofreq		

This register configures the settings for waking up the regulators.

Register Segment: 0

Bits	Name	Description
5:3	wake_precnt[2:0]	Sets the wakeup precounter timeout used for wakeup holdoffs in {PWRSYS.WAKE_TR0}. Wakeup timing is spec'd at 12MHz. If a different wake_imofreq is used, the correct divide ratio should be set here (eg to compensate for 24MHz, set 3'b001).
2:0	wake_imofreq[2:0]	Sets the IMO frequency used during chip wakeup from a low power mode. See Table 1-78.

Table 1-78. Bit field encoding: fimo_freq_enum

Value	Name	Description
3'b000	FIMO_12MHZ	12 MHz
3'b001	FIMO_RSVD001	reserved (12MHz)
3'b010	FIMO_24MHZ	24 MHz
3'b011	FIMO_RSVD011	reserved (???)
3'b100	FIMO_48MHZ	48 MHz
3'b101	FIMO_RSVD101	reserved (48MHz)
3'b110	FIMO_RSVD110	reserved (???)
3'b111	FIMO_RSVD111	reserved (???)

1.3.118 PWRSYS_BREF_TR

Boot Reference Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BREF_TR: 0x40004687

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:1	R/W:1	R/W:1
HW Access	NA				R	R	R	R
Name					bref_testmode	bref_force_turbo	bref_force_outen	bref_force_refsw

This registers configures the power system boot reference..

Register Segment: 0

Bits	Name	Description
3	bref_testmode	When set, the bootref is in testmode.
2	bref_force_turbo	When set, the boot reference is forced to turbo mode. When clear, the power manager controls it.
1	bref_force_outen	When set, the boot reference output is forced enabled. When clear, the power manager controls it.
0	bref_force_refsw	When set, the power system references are forced to come from the bootref. When clear, the power manager controls the reference source for the power system (bootref or bandgap).

1.3.119 PWRSYS_BG_TR

Bandgap Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BG_TR: 0x40004688

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:00		R/W:00000				
HW Access	NA	R		R				
Name		inl_ctrl		trimbuf_lsb				

Bandgap Trim

Register Segment: 0

Bits	Name	Description
6:5	inl_ctrl[1:0]	Current Bandgap - nonlinear current control (fine tuning)
4:0	trimbuf_lsb[4:0]	Bandgap Trim Buffer - LSB trim bits

1.3.120 ILO_TR0

Internal Low-speed Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ILO_TR0: 0x40004690

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1000				R/W:1000			
HW Access	R				R			
Name	tr_100k				tr_1k			

This register is used to trim the frequency of the ILO output clocks.

Register Segment: 0

Bits	Name	Description
7:4	tr_100k[3:0]	Trim setting for 100 kHz output See Table 1-79.
3:0	tr_1k[3:0]	Trim setting for 1 kHz output See Table 1-80.

Table 1-79. Bit field encoding: TR_100K_ENUM

Value	Name	Description
4'b0000	TR_100K_MIN	Minimum Frequency
4'b1111	TR_100K_MAX	Maximum Frequency

Table 1-80. Bit field encoding: TR_1K_ENUM

Value	Name	Description
4'b0000	TR_1K_MIN	Minimum Frequency
4'b1111	TR_1K_MAX	Maximum Frequency

1.3.121 ILO_TR1

Internal Low-speed Oscillator Coarse Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ILO_TR1: 0x40004691

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:10	
HW Access	NA					R	R	
Name						ct_range	ctrim	

This register is used to trim the frequency of the ILO output clocks.

Register Segment: 0

Bits	Name	Description
2	ct_range	Coarse Trim Range select for ILO See Table 1-82.
1:0	ctrim[1:0]	Coarse Trim Setting for ILO See Table 1-81.

Table 1-81. Bit field encoding: CTRIM_ENUM

Value	Name	Description
2'h0	CTRIM_0	Full Resistor (lowest current, lowest frequency)
2'h1	CTRIM_1	3/4 * R
2'h2	CTRIM_2	1/2 * R
2'h3	CTRIM_3	1/4 * R (highest current, highest frequency)

Table 1-82. Bit field encoding: CT_RANGE_ENUM

Value	Name	Description
1'b0	CT_RANGE_0	Normal range
1'b1	CT_RANGE_1	Lower current range

1.3.122 X32_TR

32 kHz Watch Crystal Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

X32_TR: 0x40004698

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:100		
HW Access	NA					R		
Name						xgm		

(no description)

Bits	Name	Description
2:0	xgm[2:0]	Amplifier GM setting, applies to both High and Low power modes See Table 1-83.

Table 1-83. Bit field encoding: XGM_ENUM

Value	Name	Description
3'b000	XGM_MIN	Lowest current setting
3'b100	XGM_DEFAULT	Default setting
3'b111	XGM_MAX	Highest current setting

1.3.123 IMO_TR0

Internal Main Oscillator Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR0: 0x400046A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000			NA:00000				
HW Access	R			NA				
Name	imo_lsb							

This register contains the frequency trim for the IMO. For each frequency range, a separate factory trim should be loaded into this register. It is recommended that the user not change the value of this register. When changing frequency ranges, the new trim value should be applied at the lowest freqency range. For example, when switching to a high range, first apply the trim value of the higher range, then switch the IMO to that range. If switching to a lower range, change the range first and then apply the new trim value.

Bits	Name	Description
7:5	imo_lsb[2:0]	These are the 3 LSB of the IMO frequency trim. Normally these are not changed by the user, and are only modified by the hardware during USB clock-locking. These bits are locked from user write when the USB_LOCK bit (Register is TBD) is set. See Table 1-84.

Table 1-84. Bit field encoding: IMO_LSB_ENUM

Value	Name	Description
3'b000	IMO_LSB_MIN	minimum value
3'b111	IMO_LSB_MAX	maximum value

1.3.124 IMO_TR1

Internal Main Oscillator Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR1: 0x400046A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	imo_trim							

(no description)

Bits	Name	Description
7:0	imo_trim[7:0]	Frequency trim (8 MSbits) for the IMO. 8 MSbits of the trim. The factory trim only uses these 8 bits; the 3 LSbits (IMO_LSB[2:0]) are normally only used during USB operation. These bits are locked from user write when the USB_LOCK bit (Register is TBD) is set. See Table 1-85.

Table 1-85. Bit field encoding: IMO_TRIM_ENUM

Value	Name	Description
8'h00	IMO_TRIM_MIN	Minimum frequency
8'h00	IMO_TRIM_MAX	Maximum frequency

1.3.125 IMO_GAIN

Internal Main Oscillator Gain Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_GAIN: 0x400046A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:010000					
HW Access	NA		R					
Name			gain					

This register contains the gain trim for the IMO. This is normally set with a factory trim and not modified by the user.

Bits	Name	Description
5:0	gain[5:0]	Gain trim for the IMO. This controls the kHz/step of the trim setting in the IMO_TR register. See Table 1-86.

Table 1-86. Bit field encoding: GAIN_ENUM

Value	Name	Description
6'h00	GAIN_MAX	Maximum Gain
6'h3F	GAIN_MIN	Minimum Gain

1.3.126 IMO_C36M

Internal Main Oscillator 36 MHz clock control register {INTERNAL}

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_C36M: 0x400046A3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					tr36			

This register controls operation of the 36 Mhz output of the IMO.

Bits	Name	Description
3:0	tr36[3:0]	Frequency trim for the 36 MHz SPC clock. This value should not be changed by the user. See Table 1-87.

Table 1-87. Bit field encoding: TR36_ENUM

Value	Name	Description
4'h0	TR36_MIN	Minimum frequency
4'hf	TR36_MAX	Maximum frequency

1.3.127 IMO_TR2

Internal Main Oscillator Trim Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR2: 0x400046A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:000000					
HW Access	R	NA	R					
Name	pll_trim		fimo_trim					

This register contains the frequency trim for the IMO during fastwake mode.

Bits	Name	Description
7	pll_trim	PLL trim
5:0	fimo_trim[5:0]	Frequency trim for the IMO in fastwake mode (FIMO). This value should not be changed by the user. See Table 1-88.

Table 1-88. Bit field encoding: FIMO_TRIM_ENUM

Value	Name	Description
6'h0	FIMO_TRIM_MIN	Minimum frequency
6'hf	FIMO_TRIM_MAX	Maximum frequency

1.3.128 XMHZ_TR

External 4-25 MHz Crystal Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

XMHZ_TR: 0x400046A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					iref			

(no description)

Bits	Name	Description
3:0	iref[3:0]	This bit adjusts the output current of the oscillator circuit. The value is selected to match the output external crystal characteristics. See Table 1-89.

Table 1-89. Bit field encoding: IREF_ENUM

Value	Name	Description
4'h0	IREF_0	13 unit resistors
4'h1	IREF_1	14 unit resistors
4'h2	IREF_2	15 unit resistors
4'h3	IREF_3	16 unit resistors
4'h4	IREF_4	17 unit resistors
4'h5	IREF_5	18 unit resistors
4'h6	IREF_6	19 unit resistors
4'h7	IREF_7	20 unit resistors
4'h8	IREF_8	21 unit resistors
4'h9	IREF_9	22 unit resistors
4'ha	IREF_A	23 unit resistors
4'hb	IREF_B	24 unit resistors
4'hc	IREF_C	25 unit resistors
4'hd	IREF_D	26 unit resistors
4'he	IREF_E	27 unit resistors
4'hf	IREF_F	28 unit resistors

1.3.129 MLOGIC_DMP_DMY

Dumpster Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_DMP_DMY: 0x400046E2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name	debug_enable							

(no description)

Bits	Name	Description
7:0	debug_enable[7:0]	Dummy register used to pad the manufacturing configuration table

1.3.130 MLOGIC_SEG_CR

Segment Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_SEG_CR: 0x400046E4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:10110100							
HW Access	R							
Name	segment_control							

(no description)

Bits	Name	Description
7:0	segment_control[7:0]	Segment Control

1.3.131 MLOGIC_SEG_CFG0

Segment Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_SEG_CFG0: 0x400046E5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOSET:0	R/W:0	R/WOSET:0	R/W:0	R/WOSET:0	R/W:0	R/WOSET:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	lock_protect_3	lock_3	lock_protect_2	lock_2	lock_protect_1	lock_1	lock_protect_0	lock_0

(no description)

Bits	Name	Description
7	lock_protect_3	Segment Lock Protect
6	lock_3	Segment Lock
5	lock_protect_2	Segment Lock Protect
4	lock_2	Segment Lock
3	lock_protect_1	Segment Lock Protect
2	lock_1	Segment Lock
1	lock_protect_0	Segment Lock Protect
0	lock_0	Segment Lock

1.3.132 MLOGIC_DBG_DBE

Debug Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_DBG_DBE: 0x400046E8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							men_tst_acc	debug_enable

(no description)

Bits	Name	Description
1	men_tst_acc	Can only be set in test mode, allows access to TC registers
0	debug_enable	Debug Enable

1.3.133 MLOGIC_CPU_SCR

System Status and Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_CPU_SCR: 0x400046EA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:0	R/W:1	R:0	NA:0
HW Access	NA				R/W	R/W	R/W	NA
Name					wol	boot	tmode	

(no description)

Bits	Name	Description
3	wol	Write Once Latch Status
2	boot	Boot. Cleared by the Checksum block upon completion of the boot process. Can also be cleared in Test Mode to bypass the boot process.
1	tmode	Test Mode Status

1.3.134 RESET_IPOR_CR0

Imprecise Power On Reset Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR0: 0x400046F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Name	code							

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Register Segment: 0

Bits	Name	Description
7:0	code[7:0]	Write 0xD4 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset.

1.3.135 RESET_IPOR_CR1

Imprecise Power On Reset Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR1: 0x400046F1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Name	code							

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Register Segment: 0

Bits	Name	Description
7:0	code[7:0]	Write 0xAA to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset.

1.3.136 RESET_IPOR_CR2

Imprecise Power On Reset Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR2: 0x400046F2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Name	code							

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Register Segment: 0

Bits	Name	Description
7:0	code[7:0]	Write 0x56 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset.

1.3.137 RESET_IPOR_CR3

Imprecise Power On Reset Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR3: 0x400046F3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Name	code							

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Register Segment: 0

Bits	Name	Description
7:0	code[7:0]	Write 0xC9 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset.

1.3.138 RESET_CR0

LVI Set Point Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR0: 0x400046F4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Name	lvi_a				lvi_d			

Please reference voltage monitors on the device datasheet for voltage trip levels.

Register Segment: 1

Bits	Name	Description
7:4	lvi_a[3:0]	When LVI_A is enabled, these 4 bits select the trip point of the detector.
3:0	lvi_d[3:0]	When LVI_D is enabled, these 4 bits select the trip point of the detector.

1.3.139 RESET_CR1

Reset System Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR1: 0x400046F5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Name			dis_hbr1	dis_pres1	vmon_hvi_sel	en_hvi_a	en_lvi_a	en_lvi_d

This register enables circuits in the reset subsystem.

Register Segment: 1

Bits	Name	Description
5	dis_hbr1	When both this bit and dis_hbr2 are set, the HBR circuit is disabled. This bit is in segment 0.
4	dis_pres1	When both this bit and dis_pres2 are set, the PRES-A and PRES-D circuits are disabled. This bit is in segment 0.
3	vmon_hvi_sel	When set, this bit enables the vmon to look at the VDDD. When this bit is cleared, the vmon looks at the VDDA.
2	en_hvi_a	When set, enables the high-voltage-interrupt feature on the external analog supply.
1	en_lvi_a	When set, enables the low-voltage-interrupt feature on the external analog supply.
0	en_lvi_d	When set, enables the low-voltage-interrupt feature on the external digital supply.

1.3.140 RESET_CR2

Software Reset Control Register

Reset: IPOR/PRES/HBR for retention flops [reset_hard_retention]

Register : Address

RESET_CR2: 0x400046F6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								swr

This register control the software reset (SWR).

Register Segment: 1

Bits	Name	Description
0	swr	Setting this bit will cause a system reset.

1.3.141 RESET_CR3

LVD/POR Test Mode Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR3: 0x400046F7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Name				dis_hbr2	dis_pres2	tmux_sel		

This register controls test mode settings for the LVDPOR subsystem.

Bits	Name	Description
4	dis_hbr2	When both this bit and dis_hbr1 are set, the HBR circuit is disabled. This bit is in segment 0
3	dis_pres2	When both this bit and dis_pres1 are set, the PRES-A and PRES-D circuits are disabled. This bit is in segment 0
2:0	tmux_sel[2:0]	Selects the circuit output to steer to the 'tmuxout' pin. See Table 1-90.

Table 1-90. Bit field encoding: tmux_sel

Value	Name	Description
3'b000	TMODE_000	Normal mode (output driven to vgnd)
3'b001	TMODE_001	pres-d
3'b010	TMODE_010	pres_a
3'b011	TMODE_011	lvi_d
3'b100	TMODE_100	lvi_a
3'b101	TMODE_101	hvi_a
3'b110	TMODE_110	reserved
3'b111	TMODE_111	reserved

1.3.142 RESET_SR0

Reset and Voltage Detection Status Register 0

Reset: IPOR/PRES/HBR for retention flops [reset_hard_retention]

Register : Address

RESET_SR0: 0x400046F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		RC:0	NA:0	RC:0	RC:0	RC:0	RC:0
HW Access	NA		R/W	NA	R/W	R/W	R/W	R/W
Name	gpsws		swrs		wdrs	hvi_a_s	lvi_a_s	lvi_d_s

This register gives persistent status for the reset and voltage detection systems.

Bits	Name	Description
7:6	gpsws[1:0]	General purpose status for user software. These bits can be set/cleared by software and only reset by hard reset sources. They can be used to hold user defined status that persists through many resets.
5	swrs	Persistent status of the software reset. This bit will be set when a software reset occurs and will stay set until cleared by the user or reset. Sticky (whole field)
3	wdrs	Persistent status of the watchdog reset. This bit will be set when a watchdog reset occurs and will stay set until cleared by the user or reset. Sticky (whole field)
2	hvi_a_s	Persistent status of analog HVI. This bit will be set when the analog supply goes below the set point for the HVI detector and will stay set until cleared by the user or reset. Sticky (whole field)
1	lvi_a_s	Persistent status of analog LVI. This bit will be set when the analog supply goes below the set point for the LVI detector and will stay set until cleared by the user or reset. Sticky (whole field)
0	lvi_d_s	Persistent status of digital LVI. This bit will be set when the digital supply goes below the set point for the LVI detector and will stay set until cleared by the user or reset. Sticky (whole field)

1.3.143 RESET_SR1

Reset and Voltage Detection Status Register 1

Reset: IPOR/PRES/HBR for retention flops [reset_hard_retention]

Register : Address

RESET_SR1: 0x400046F9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0000				RC:0	RC:0	RC:0	RC:0
HW Access	R/W				R/W	R/W	R/W	R/W
Name	cksm_fail_cnts				segrs	hbrs	pres_a_s	pres_d_s

This register gives persistent status for the reset and voltage detection systems.

Bits	Name	Description
7:4	cksm_fail_cnts[3:0]	Count of the number of times the Checksum process has failed, causing a reset. These 4 bits will hold the count value and it will stay until cleared by a reset.
3	segrs	Persistent status of the segment reset. This bit will be set when the segment reset occurs circuit and will stay set until cleared by the user or reset. Note a segment reset occurs when a value other than 0xB4 or 0xB5 is written to the Segment Control Register. Sticky (whole field)
2	hbrs	Persistent status of HBR. This bit will be set when the digital supply goes below the trip point for the HBR circuit and will stay set until cleared by the user or reset. Note that this field is only useful during test mode when the HBR circuit does not cause a system reset. Sticky (whole field)
1	pres_a_s	Persistent status of analog PRES. This bit will be set when the analog supply goes below the trip point for the PRES circuit and will stay set until cleared by the user or reset. Note that this field is only useful during test mode when the PRES-A circuit does not cause a system reset. Sticky (whole field)
0	pres_d_s	Persistent status of digital PRES. This bit will be set when the digital supply goes below the trip point for the PRES circuit and will stay set until cleared by the user or reset. Note that this field is only useful during test mode when the PRES-D circuit does not cause a system reset. Sticky (whole field)

1.3.144 RESET_SR2

Reset and Voltage Detection Status Register 2

Reset: IPOR/PRES/HBR for retention flops [reset_hard_retention]

Register : Address

RESET_SR2: 0x400046FA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0	RC:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	W	W	W	W	W	W	W	W
Name	cm3_lockup	cm3_sysres_req	hbrs_r	pres_a_r	pres_d_r	hvi_a_r	lvi_a_r	lvi_d_r

This register gives real-time status for the reset and voltage detection systems.

Bits	Name	Description
7	cm3_lockup	CM3 Processor Lockup Status
6	cm3_sysres_req	CM3 System Reset Request
5	hbrs_r	Real-time status of HBR. This is only useful when the HBR does not cause a system level reset.
4	pres_a_r	Real-time status of analog PRES. This is only useful during test mode.
3	pres_d_r	Real-time status of digital PRES. This is only useful during test mode.
2	hvi_a_r	Real-time status of analog HVI.
1	lvi_a_r	Real-time status of analog LVI.
0	lvi_d_r	Real-time status of digital LVI.

1.3.145 RESET_TR

PRES Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_TR: 0x400046FB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0110				R/W:0110			
HW Access	R				R			
Name	pres_a				pres_d			

This register sets the trim for the precision voltage detectors (PRES).

Register Segment: 0

Bits	Name	Description
7:4	pres_a[3:0]	Trim for PRES-A.
3:0	pres_d[3:0]	Trim for PRES-D.

1.3.146 SPC_FM_EE_CR

FM_EE_CR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_FM_EE_CR: 0x40004700

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R:1	R/W:0	R/W:0	NA:0	R/W:0	R/W:0
HW Access	NA		R/W	R	R	NA	R	R
Name			EE_AWAKE	EE_SLP_REQ	FM_KEEP_AWAKE		EE_Priority	FM_Priority

This register contains control bits for the flash and eeprom arrays

Bits	Name	Description
5	EE_AWAKE	Status signal to denote that the EEPROM array is awake, when set equal to 1. On power up this value is 0. However after the 5 us holdoff time, for the EEPROM to ramp up, has elapsed, the bit will automatically be set to a 1. This all occurs before the boot process is complete, so the user will always read this bit as having a reset value of 1.
4	EE_SLP_REQ	Request for user firmware to put the EEPROM array into sleep mode.
3	FM_KEEP_AWAKE	Flash Macro Keep Awake See Table 1-91.
1	EE_Priority	Sets priority between the PHUB and the SPC for who gets control of the EEPROM array upon simultaneous access requests. 1-> SPC has priority. 0-> PHUB has priority.
0	FM_Priority	Sets priority between the cache controller and the SPC for who gets control of the flash array upon simultaneous access requests. 1-> SPC has priority. 0-> Cache controller has priority.

Table 1-91. Bit field encoding: FM_SLP_ENUM

Value	Name	Description
1'h0	FM_KEEP_AWAKE_LOW	Doesn't prevent the Flash macro from being put to sleep by the Cache.
1'h1	FM_KEEP_AWAKE_HIGH	Prevents the Flash macro from being put to sleep by the Cache

1.3.147 SPC_FM_EE_WAKE_CNT

FM_EE_WAKE_CNT

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_FM_EE_WAKE_CNT: 0x40004701

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:10111001							
HW Access	R							
Name	Wake_Count							

Flash/EEPROM Wake Count Register

Bits	Name	Description
7:0	Wake_Count[7:0]	The wake count defines the number of BUS clock cycles (in granularity of 2) it takes for the flash or eeprom to wake up. The reset value of this register can be 1 of 2 values, based on the value of the CFGSPEED in the customer NVL (bit 0 of byte 3). If CFGSPEED = 0 at boot (IMO is in slow mode - 12MHz typical), the reset value of this register is 0x2E. If CFGSPEED = 1 at boot (IMO is in fast mode - 48MHz typical), the reset value of this register is 0xB9.

1.3.148 SPC_EE_SCR

EEPROM Status & Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_EE_SCR: 0x40004702

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R:0	R/W:0
HW Access	NA						R/W	R
Name							EE_AHB_ACK	AHB_EE_REQ

This register contains status and control bits for the EEPROM array.

Bits	Name	Description
1	EE_AHB_ACK	Once the AHB_EE_REQ bit is set, this bit is set high once the EEPROM is available to be read across the PHUB interface.
0	AHB_EE_REQ	This bit is set high when a read access of the EEPROM, through the PHUB interface, is desired. This is a request bit and is part of a two bit interface with the EE_AHB_ACK bit.

1.3.149 SPC_EE_ERR

EEPROM Error Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_EE_ERR: 0x40004703

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							RC:0
HW Access	NA							R/W
Name								EEPROM_error

This register has an error bit for the EEPROM array on the chip. The error bit indicates whether or not the array has had a collision error where two masters (the SPC and the PHUB interface) attempted to access the array simultaneously. The bits are cleared upon a read of this register.

Bits	Name	Description
0	EEPROM_error	Error bit for EEPROM array 0

1.3.150 SPC_CPU_DATA

SPC CPU Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_CPU_DATA: 0x40004720

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	CPU_Data							

This register is the command interface to the SPC that allows SPC instructions to be executed by the host CPU writing a sequential series of parameters to this location. This register is meant only for the CPU and not the DMA controller to prevent collisions between the CPU and the DMAC when both attempt to call a function in the SPC

Bits	Name	Description
7:0	CPU_Data[7:0]	CPU Data.

1.3.151 SPC_DMA_DATA

SPC DMA Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_DMA_DATA: 0x40004721

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	DMA_Data							

This register is the command interface to the SPC that allows SPC instructions to be executed by the DMA controller writing a sequential series of parameters to this location. This register is meant only for the DMA Controller and not the CPU to prevent collisions between the CPU and the DMAC when both attempt to call a function in the SPC

Bits	Name	Description
7:0	DMA_Data[7:0]	DMA Data.

1.3.152 SPC_SR

SPC Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_SR: 0x40004722

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:000000						R:1	R:0
HW Access	R/W						R/W	R/W
Name	Status_Code						SPC_Idle	Data_Ready

This register returns the current status of the SPC and the exit status of the last complete SPC instruction.

Bits	Name	Description
7:2	Status_Code[5:0]	The Status Code represents the exit status of the last executed SPC instruction. The values of this field are detailed in the PSoC3 SPC BROS.
1	SPC_Idle	This bit indicates whether or not the SPC is currently executing an instruction. The bit asserts as soon as the 1st byte of the 2-byte command key (0xB6) is written into the SPC CPU or DMA Data Register. The bit is negated as soon as an instruction completes or if the 2nd byte of the command key is invalid. See Table 1-93.
0	Data_Ready	This bit indicates whether or not the SPC has data that is ready to be read from the SPC CPU or DMA Data Register. See Table 1-92.

Table 1-92. Bit field encoding: DATA_RDY_ENUM

Value	Name	Description
1'h0	DATA_IS_NOT_RDY	The SPC isn't ready for the next byte to be written
1'h1	DATA_IS_RDY	The SPC is read for the next byte to be written

Table 1-93. Bit field encoding: INSTR_IDLE_ENUM

Value	Name	Description
1'h0	INSTR_IS_NOT_IDLE	SPC is currently executing an SPC instruction.
1'h1	INSTR_IS_IDLE	SPC is idle and not busy executing an instruction.

1.3.153 SPC_CR

SPC Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_CR: 0x40004723

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:11		NA:000			R/W:0	R/W:0	R/W:0
HW Access	R		NA			R	R	R/W
Name						ADC_Att_En	SPC_Busclock_Frequency	SPC_Manual_Reset

This register contains control bits for the SPC.

Bits	Name	Description
7:6	RSVD[1:0]	(no description)
2	ADC_Att_En	When using the SPC ADC to convert an external analog signal, the voltage may be passed directly through to the ADC or routed through an internal divide-by-4 voltage attenuator. A value of 1 for this bit will select the path through the attenuator while a value of 0 will select the direct connection.
1	SPC_Busclock_Frequency	This bit is used to define the frequency of the bus (AHB) clock. The SPC uses this bit to determine the number of stall cycles when accessing the Flash or the EEPROM . See Table 1-94.
0	SPC_Manual_Reset	Setting this bit manually resets the SPC. The SPC hardware automatically clears the bit after being held high for 2 cycles of the AHB Bus Clock. See Table 1-95.

Table 1-94. Bit field encoding: SPC_BUSFREQ_ENUM

Value	Name	Description
1'h0	SPC_BUSFREQ_LOW	Tells the SPC that the Bus Clock Frequency is: 50 < Frequency <= 100.
1'h1	SPC_BUSFREQ_HIGH	Tells the SPC that the Bus Clock Frequency is: Frequency <= 50.

Table 1-95. Bit field encoding: SPC_RESET_ENUM

Value	Name	Description
1'h0	SPC_RST_LOW	SPC is in normal execution mode.
1'h1	SPC_RST_HIGH	SPC is in a reset state.

1.3.154 SPC_DMM_MAP_SRAM[0..127]

SPC Direct Memory Mapping

Reset: N/A

Register : Address

SPC_DMM_MAP_SRAM: 0x40004780-0x400047FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	spcsramdata							

Maps one of 5 possible 128-byte pages from the 128-Data Store SRAM or 512-byte Code Store SRAM

Bits	Name	Description
7:0	spcsramdata[7:0]	(no description)

1.3.155 CACHE_CC_CTL

Cache Control Register

Reset: Reset Signals Listed Below

Register : Address

CACHE_CC_CTL: 0x40004800

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		NA:000			R/W:0	R:U	R/W:0
HW Access	R		NA			R/W	R/W	R/W
Name	FLASH_CYCLES					FLUSH	FLASH_LOWPWR	DISABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:11111111							
HW Access	R/W							
Name	LP_MODE							

CC_CTL is used to configure the behavior of the cache.

Bits	Name	Description
15:8	LP_MODE[7:0]	0x0 - 0xfe: Specifies the number of cache hits after which the cache controller 0xff: Low Power Mode disabled. Assert SLEEP_REQ which will put the FLASH into a low-power mode. To put the FLASH immediately into a low-power state, set LP_MODE to 0. Normally this should only be done when executing code from SRAM.
7:6	FLASH_CYCLES[1:0]	Specifies the number of clock cycles the cache will wait before it samples data coming back from Flash. 0x0: 4 cycles. -> 50 MHz upto less than 67 MHz 0x1: 1 cycle. -> 0 MHz upto less than 16 MHz 0x2: 2 cycles. -> 16 MHz upto less than 33 MHz 0x3: 3 cycles. -> 33 MHz upto less than 50 MHz The following stalls are computed using: Flash access time: 32.5 ns ECC enable delay: 4.4 ns Cache delay: ?.? ns CM3 setup delay: ?.? ns Margin: ?.? ns
2	FLUSH	Writing a 1 will cause the cache to be flushed. All entries in the cache are invalidated on the next clock cycle. Note that invalidating the cache must be done with care as the prefetch logic in the CM3 will have already fetched several instructions before the write to this register is executed. Either a string of NOPs or other special instructions are required to insure data integrity. Reading this bit will always return 0 as the bit is automatically cleared once the cache has been flushed.
1	FLASH_LOWPWR	0=FLASH is at full power and ready for access. 1=FLASH is in a low-power mode and will take several microseconds on the first access. See the description for LP_MODE for more details on when FLASH is in a low-power mode. Note that this is a read-only bit.
0	DISABLE	0=enable CACHE. 1=disable CACHE.

1.3.155 CACHE_CC_CTL (continued)

Reset Table

resetsignal	field(s)
N/A	FLASH_LOWPWR
Domain reset for non-retention flops [reset_all_nonretention]	DISABLE, FLUSH, FLASH_CYCLES[1:0], LP_MODE[7:0]

1.3.156 CACHE_ECC_CORR

Error Correction detected

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_ECC_CORR: 0x40004880

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000					NA:0	R/W:0	R/W:0
HW Access	R/W					NA	R/W	R/W
Name	ECC_ADDR						INT_ENB	INT_VALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ECC_ADDR							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ECC_ADDR							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ECC_ADDR							

A Single Bit error was detected and corrected. The address where the error occurred is stored in this register. An ECC correction at address 0x1234_5678 would result in this register containing 0x1234_567b. Note that the 3 LSBs have the INT_VALID, INT_ENB and a reserved bit in them. Note that the interrupts from all sources within the cache are logically ORed together. Software must read all of the registers to determine which interrupts have caused the interrupt.

Bits	Name	Description
31:3	ECC_ADDR[28:0]	Flash address where error was detected and corrected. Note that the 3 LSBs are not captured but contain the fields above.
1	INT_ENB	0=Disable interrupt. 1=Enable interrupt on ECC correction. This bit is logically ANDed with INT_VALID before the interrupt is sent to the CPU.
0	INT_VALID	0=ECC_ADDR field is invalid. No ECC correction has occurred. 1=ECC_ADDR field contains the address where a single bit error was detected. ECC_ADDR is frozen until INT_VALID is written with a 0.

1.3.157 CACHE_ECC_ERR

Error Correction failed

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_ECC_ERR: 0x40004888

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000					NA:0	R/W:0	R/W:0
HW Access	R/W					NA	R/W	R/W
Name	ERR_ADDR						INT_ENB	INT_VALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ERR_ADDR							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ERR_ADDR							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ERR_ADDR							

A multi-Bit error was detected and cannot be corrected. The address where the error occurred is stored in this register.

Bits	Name	Description
31:3	ERR_ADDR[28:0]	Flash address where error was detected. Note that the LSBs of the address are dropped since FLASH is 64 bits wide. The INT_VALID and INT_ENB and a reserved bit are in the 3 LSBs.
1	INT_ENB	0=Disable interrupt. 1=Enable interrupt on ECC error. This bit is logically ANDed with INT_VALID before the interrupt is sent to the CPU.
0	INT_VALID	0=ERR_ADDR field is invalid. No ECC detection has occurred. 1=ERR_ADDR field contains the address where a mult-bit error was detected. ERR_ADDR is frozen until INT_VALID is written with a 0.

1.3.158 CACHE_FLASH_ERR

FLASH error

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_FLASH_ERR: 0x40004890

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000					NA:0	R/W:0	R/W:0
HW Access	R/W					NA	R/W	R/W
Name	ERR_ADDR						INT_ENB	INT_VALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ERR_ADDR							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ERR_ADDR							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ERR_ADDR							

Attempted write to Flash error. FLASH cannot be written to via the PHUB port. Only the SPC can write to FLASH. Typically this indicates that the code has failed and should be reset.

Bits	Name	Description
31:3	ERR_ADDR[28:0]	Flash address where error was detected. Note that the 3 LSBs are not captured but contain the fields above.
1	INT_ENB	0=Disable interrupt. 1=Enable interrupt on FLASH write error. This bit is logically ANDed with INT_VALID before the interrupt is sent to the CPU.
0	INT_VALID	0=ERR_ADDR field is invalid. 1=ERR_ADDR field contains the address where a write to flash was attempted. ERR_ADDR is frozen until INT_VALID is written with a 0.

1.3.159 CACHE_HITMISS

HIT/MISS counters

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_HITMISS: 0x40004898

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	MISS_COUNT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	MISS_COUNT							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	HIT_COUNT							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	HIT_COUNT							

This register contains two 16-bit counters which count the number of cache hits and misses. The hit/miss ratio can be used to optimize code performance by analyzing where the code misses cache. When the cache misses, a fetch from FLASH is required which typically takes several wait states. Minimizing the cache misses will improve performance. If excessive cache misses are determined for a particular section of code, the code can either be rewritten to fit better in cache or relocate speed critical code to SRAM. To measure cache perfomance, the HITMISS register should be written with 0 at the start of a block of code to be measured. Then the code is executed and at the end of the code under measurement, the HITMISS register will be read. The cache hit ratio is computed with: hit% = HITMISS[31:16]*100/(HITMISS[31:16]+HITMISS[15:0]; Note that when either the HIT_COUNT or MISS_COUNT register reaches their maximum value, both counters will stop counting. This allows the HIT/MISS ratio to be computed even if there are more than 64K hits/misses from the start of the code to the end. However the computation will only include the first 64K hits or misses from when the counter was zeroed. Often an interrupt service routine can be triggered at regular intervals and measure the hit/miss ratio over time as the code is being executed.

Bits	Name	Description

1.3.159 CACHE_HITMISS (continued)

31:16	HIT_COUNT[15:0]	The HIT_COUNT register operates in 2 modes based on the value in LP_MODE of the cache control register (CC_CTL.LP_MODE). When LP_MODE is 0xff, HIT_COUNT will increment every time cache is able to provide the data to the CPU from it's local copy of the FLASH data (a cache hit). Once the maximum value of either HIT_COUNT or MISS_COUNT is reached, HIT_COUNT will stop counting. Writing a 0 will clear the counter but always write all 32-bits to insure both counters are cleared at the same time. When LP_MODE is any value other than 0xff, the HIT_COUNT is reserved for internal use. HIT_COUNT in this mode is used to keep track of the number of hits from the last MISS. When HIT_COUNT=LP_MODE, then the FLASH is put into a low-power mode until a MISS occurs. Note that HIT_COUNT becomes read-only when LP_MODE!=0xff.
15:0	MISS_COUNT[15:0]	The MISS_COUNT register operates only when LP_MODE is equal to 0xff. The counter is incremented each time the cache controller has to fetch data from FLASH. When either MISS_COUNT or HIT_COUNT reaches the maximum count value of 0xffff, then both counters stop counting. Writing a 0 will clear MISS_COUNT and enable counting.

1.3.160 I2C_XCFG

I2C Extended Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

I2C_XCFG: 0x400049C8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:000000						R/W:0
HW Access	R	NA						R
Name	csr_clk_en							hw_addr_en

This register configures enhanced features. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Always write reserved bits with a value of '0'.

Bits	Name	Description
7	csr_clk_en	This bit is used for gating system clock for the blocks core logic that is not associated with AHB interface. Clock is made available to the core logic only when this bit is set to 1 and the input pin ext_clk_en is also active. If either of them is not active, the blocks core logic does not receive the system clock. See Table 1-96.
0	hw_addr_en	When this bit is set to a '1', hardware address compare is enabled. When enabled, there is no interrupt generated on an address reception and bit 3 in the CSR register is not set. On a compare, the address is automatically ACKed, and on a mismatch, the address is automatically NACKed, and the hardware reverts to an idle state waiting for the next Start detection. You must configure the compare address in the ADR register. When this bit is a '0', bit 3 of the CSR register is set and the bus stalls, and the received address is available in the Data register, to enable the CPU to do a firmware address compare. The functionality of this bit is independent of the data buffering mode. See Table 1-97.

Table 1-96. Bit field encoding: csr_clk_en_enum

Value	Name	Description
1'b1	CSR_CLK_EN	CLK gating for block core logic is enabled
1'b0	CSR_CLK_DIS	CLK gating for blobk core logic is disabled

Table 1-97. Bit field encoding: hw_addr_en_enum

Value	Name	Description
1'b1	HW_ADDR_EN	HW Address comparison is enabled
1'b0	HW_ADDR_DIS	HW Address comparison is disabled

1.3.161 I2C_ADR

I2C Slave Adddress Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

I2C_ADR: 0x400049CA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R						
Name		slave_address						

This register holds the slave's 7-bit address. When hardware address compare mode is not enabled in the XCFG register, this register is not in use. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Always write reserved bits with a value of '0'.

Bits	Name	Description
6:0	slave_address[6:0]	These seven bits hold the slave's own device address.

1.3.162 I2C_CFG

I2C Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

I2C_CFG: 0x400049D6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	NA	R	R	R
Name	sio_select	pselect	bus_error_ie	stop_ie		clock_rate	en_mstr	en_slave

This register is used to set the basic operating modes, baud rate, and interrupt selection. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Alweays write reserved bits with a value of '0'.

Bits	Name	Description
7	sio_select	I2C Pin Select for SCL/SDA lines from SIO1/SIO2, 0 = SCL and SDA lines get their inputs from SIO1 module.sclk_str1 and sda_ack1 are driven to SIO1 module and they get asserted once device wakes up from sleep. 1 = SCL and SDA lines get their inputs from SIO2 module. sclk_str2 and sda_ack2 are driven to SIO2 module and they get asserted once device wakes up from sleep. This bit is valid only when i2C.CFG[6] is asserted. See Table 1-103.
6	pselect	I2C Pin Select for SCL/SDA lines from GPIO/SIO, 0 = SCL and SDA lines get their inputs from GPIO module.sclk_str0 and sda_ack0 are driven to GPIO module and they get asserted once device wakes up from sleep. 1 = SCL and SDA lines get their inputs from one of the SIO Blocks that is chosen based on the configuration of bit I2C.CFG[7] See Table 1-102.
5	bus_error_ie	Bus Error Interrupt Enable 0 disabled 1 enabled. An interrupt is generated on the detection of a Bus error condition. See Table 1-98.
4	stop_ie	Stop Interrupt Enable 0 disabled 1 enabled. An interrupt is generated on the detection of a Stop condition. See Table 1-104.
2	clock_rate	0 Samples/bit is 16, 1 Samples/bit is 32. See Table 1-99.
1	en_mstr	0 Disabled 1 enabled See Table 1-100.
0	en_slave	0 Disabled 1 enabled See Table 1-101.

Table 1-98. Bit field encoding: bus_error_ie_enum

Value	Name	Description
1'b1	BUS_ERROR_IE_EN	Bus Error Interrupt is enabled

1.3.162 I2C_CFG (continued)

Table 1-98. Bit field encoding: bus_error_ie_enum

1'b0	BUS_ERROR_IE_DIS	Bus Error Interrupt is disabled

Table 1-99. Bit field encoding: clock_rate_enum

Value	Name	Description
1'b0	RATE_1	Samples/bit is 16. For 100k Standard mode OR 400K Fast mode.
1'b1	RATE_2	Samples/bit is 32. For 50k Standard mode

Table 1-100. Bit field encoding: en_mstr_enum

Value	Name	Description
1'b1	MASTER_EN	Master mode is enabled for the device
1'b0	MASTER_DIS	Master mode is disabled for the device

Table 1-101. Bit field encoding: en_slave_enum

Value	Name	Description
1'b1	SLAVE_EN	Slave mode is enabled for the device
1'b0	SLAVE_DIS	Slave mode is disabled for the device

Table 1-102. Bit field encoding: pselect_enum

Value	Name	Description
1'b1	PSELECT_EN	SCL/SDA lines get their inputs from SIO blocks
1'b0	PSELECT_DIS	SCL/SDA lines get their inputs from GPIO blocks

Table 1-103. Bit field encoding: sio_select_enum

Value	Name	Description
1'b1	SIO_SELECT_EN	SCL/SDA lines get their inputs from SIO2 block
1'b0	SIO_SELECT_DIS	SCL/SDA lines get their inputs from SIO1 block

Table 1-104. Bit field encoding: stop_ie_enum

Value	Name	Description
1'b1	STOP_IE_EN	Stop Interrupt is enabled
1'b0	STOP_IE_DIS	Stop Interrupt is disabled

1.3.163 I2C_CSR

I2C Control and Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

I2C_CSR: 0x400049D7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC/W:0	R/W:0	RC/W:0	R/W:0	RC/W:0	R/W:0	RC/W:0	RC/W:0
HW Access	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Name	bus_error	lost_arb	stop_status	ack	address	transmit	lrb	byte_complete

This register is used by the slave to control the flow of data bytes and to keep track of the bus state during a transfer. Bits in this register are held in reset until one of the enable bits in CFG is set. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
7	bus_error	0 Status bit. It must be cleared by firmware by writing a '0' to the bit position. It is never cleared by the hardware. 1 a misplaced Start or Stop condition was detected.
6	lost_arb	0 This bit is set immediately on lost arbitration; however, it does not cause an interrupt. This status may be checked after the following Byte Complete interrupt. Any Start detect or a write to the Start or Restart generate bits (MCSR register), when operating in Master mode, will also clear the bit. 1 lost Arbitration
5	stop_status	0 Status bit. It must be cleared by firmware with write of '0' to the bit position. It is never cleared by the hardware. 1 a Stop condition was detected.
4	ack	Acknowledge Out. Bit is automatically cleared by hardware on a Byte Complete event. 0 nack the last received byte. 1 ack the last received byte
3	address	0 Status bit. It must be cleared by firmware with write of '0' to the bit position. 1 the received byte is a slave address.
2	transmit	Bit is set by firmware to define the direction of the byte transfer. Any Start detect or a write to the Start or restart generate bits, when operating in Master mode, will also clear the bit. 0 receive mode 1 transmit mode See Table 1-105.
1	lrb	Last Received Bit. The value of the 9th bit in a Transmit sequence. Normally this bit is used as a status bit for the ACK/NACK value from a slave (receiver) device. A zero means the last transmitted byte was ACK'ed from the slave (receiver). A one means last transmitted byte was NACK'ed by the slave (receiver). In master mode, bit 4 (ack) is set to start the acknowledge event and this bit will need to be set to one (NACK). A zero means the last transmitted byte was ACK'ed from the slave (receiver). A one means last transmitted byte was NACK'ed by the slave (receiver)
0	byte_complete	Transmit/Receive Mode: 0 no completed transmit/receive since last cleared by firmware. Any Start detect or a write to the start or Restart generate bits, when operating in Master mode, will also clear the bit. Transmit mode: 1 eight bits of data have been transmitted and an ACK or NACK has been received. Receive mode: 1 eight bits of data have been received.

Table 1-105. Bit field encoding: transmit_enum

Value	Name	Description

1.3.163 I2C_CSR (continued)

Table 1-105. Bit field encoding: transmit_enum

1'b1	TRANSMIT_EN	Bytes are transferred from the device
1'b0	TRANSMIT_DIS	Bytes are received from the device

1.3.164 I2C_D

I2C Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

I2C_D: 0x400049D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data							

This register provides read/write access to the Shift register. This register is read only for received data and write only for transmitted data.

Bits	Name	Description
7:0	data[7:0]	Read received data or write data to transmit.

1.3.165 I2C_MCSR

I2C Master Control and Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

I2C_MCSR: 0x400049D9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:0	R:0	R/W:0	R/W:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					bus_busy	master_mode	restart_gen	start_gen

This register implements I2C framing controls and provides Bus Busy status. Bits in this register are held in reset until one of the enable bits in CFG is set. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
3	bus_busy	This bit is set to the following. 0 when a Stop condition is detected (from any bus master). 1 when a Start condition is detected (from any bus master).
2	master_mode	This bit is set/cleared by hardware when the device is operating as a master. 0 stop condition detected, generated by this device. 1 start condition detected, generated by this device.
1	restart_gen	This bit is cleared by hardware when the Restart generation is complete. 0 restart generation complete. 1 generate a Restart condition.
0	start_gen	This bit is cleared by hardware when the Start generation is complete. 0 start generation complete. 1 generate a Start condition and send a byte (address) to the I2C bus, if bus is not busy.

1.3.166 I2C_CLK_DIV

I2C Clock Divide Factor Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

I2C_CLK_DIV: 0x400049DB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						divide_factor		

Based on this register value, internal glitch clock enable is derived using system clock.

Bits	Name	Description
2:0	divide_factor[2:0]	000b /1 001b /2 010b /4 011b /8 100b /16 101b /32 110b /64.

1.3.167 DEC_CR

Decimator Control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_CR: 0x40004E00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:0	R/W:0
HW Access	R	R	R	R	R		R	R/W
Name	sat_en	fir_en	ocor_en	gcor_en	conv_mode		xstart_en	start_conv

This register provides information about start, stop, mode, and feature enables. A read of this register produces the last value written to this register with the exception of bit 0. If a 1 is read this indicates the filter is running. If a 0 is read in bit 0 the block is in the standby state.

Bits	Name	Description
7	sat_en	This bit controls the saturation feature of the Post Processor's ALU. If this bit is set it enables the saturation logic in the Post Processor's ALU. When enabled the ALU is forced to never roll over or under when the max/min value is reached in any operation it performs. See Table 1-110.
6	fir_en	This bit controls whether or not the Post Processing filter implements a sinc FIR filter function. If this bit is set it enables the Post Processor to do a sinc FIR filter. The decimation period of this post processing filter is controlled by the DR2 bits in register DR2 and DR2H. Conversion results are unpredictable if this bit is changed while the filter is running. See Table 1-107.
5	ocor_en	This bit controls the offset correction feature of the Post Processing filter. If this bit is set high it enables the post Processing filter to do offset correction. The 24-bit signed offset value is programmed in the registers OCOR, OCORM and OCORH. Conversion results are unpredictable if this bit is changed while the filter is running. See Table 1-109.
4	gcor_en	This bit controls the gain correction feature of the Post Processing filter. If this bit is set high it enables the Post processing filter. The gain coefficient is programmed in the 16 bits of registers GCOR and GCORH. Which bits in this 16-bit field that are valid is set in register GVAL. Conversion results are unpredictable if this bit is changed while the filter is running. When this feature is enabled, the DR1 register field must be set to a value higher than 32 for proper operation. See Table 1-108.
3:2	conv_mode[1:0]	The value in these two bits controls the sampling mode the decimator runs in. Single Sample mode resets all values in the ADC path, captures one sample (4 decimation cycles) and returns to the Standby state. Fast Filter mode is a continuous running Single Sample mode the ADC path being reset between each sample. Continuous mode resets the ADC path, generates a sample and then without resetting the ADC path, generates a new sample every decimation cycle thereafter. Fast FIR mode is the same as the Continuous mode except it resets the ADC channel and starts again at the termination of the DR2 (FIR Filter) period. If Fast FIR mode is selected and FIR Enable is not set in bit 6, Fast FIR and Continuous mode function the same. Conversion results are unpredictable if these bits are changed while the filter is running. See Table 1-106.

1.3.167 DEC_CR (continued)

1	xstart_en	This bit controls whether the DSI signal ext_start is active or not. If xstart_en is high, the ext_start DSI input to the Decimator is used to start the conversion. If low, the ext_start input is ignored. See Table 1-112.
0	start_conv	A write of 1 to this bit kicks off a conversion (regardless of the state of XSTART_EN) according to the conv_mode set in bits 2, 3. If 0 is written it forces the block into the Standby start via a SW reset. See Table 1-111.

Table 1-106. Bit field encoding: conv_modes_enum

Value	Name	Description
2'b00	SINGLE_SAMPLE	Single Sample Mode.
2'b01	FAST_FILTER	Fast Filter Mode.
2'b10	CONTINUOUS	Continuous Mode.
2'b11	FAST_FIR	Fast FIR.

Table 1-107. Bit field encoding: fir_en_enum

Value	Name	Description
1'b1	FIR_EN	FIR filter function is on.
1'b0	FIR_DIS	FIR filter function disabled.

Table 1-108. Bit field encoding: gcor_en_enum

Value	Name	Description
1'b1	GCOR_EN	Gain correction enabled.
1'b0	GCOR_DIS	Default: no gain correction.

Table 1-109. Bit field encoding: ocor_en_enum

Value	Name	Description
1'b1	OCOR_EN	Offset correction enabled.
1'b0	OCOR_DIS	No offset correction.

Table 1-110. Bit field encoding: sat_en_enum

Value	Name	Description
1'b1	SAT_EN	Saturation Control Enabled.
1'b0	SAT_DIS	No saturation control.

Table 1-111. Bit field encoding: start_conv_enum

Value	Name	Description
1'b1	DEC_START	Initiate a conversion.
1'b0	DEC_STOP	Kill current conversion (if running) and enter Standby state (SW reset).

Table 1-112. Bit field encoding: xstart_en_enum

Value	Name	Description
1'b1	XSTART_EN	Enable the DSI input signal ext_start to start a conversion.
1'b0	XSTART_DIS	Default: DSI signal ext_start is disabled.

1.3.168 DEC_SR

Decimator Status Register

Reset: Reset Signals Listed Below

Register : Address

DEC_SR: 0x40004E01

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	W:0	R/W:0	R:0
HW Access	NA		R	R	R	R	R	R/W
Name			coreclk_disable	intr_pulse	out_align	intr_clr	intr_mask	conv_done

This register provides information about interrupt, polling, status, and control features.

Bits	Name	Description
5	coreclk_disable	This bit controls the clock gating of the core clock. This bit and the primary block input cic_clk_en must both be asserted to allow the core clock to run. The core clock in this blocks case is the adc_clk input. See Table 1-114.
4	intr_pulse	This read/write bit selects if cic_intr is a pulse or level signal. If level, a sample completion sets cic_intr high where it remains until intr_clr is written, the block is soft-reset or an OUTSAMP register is read. If set to pulse mode, a single cycle (pclk) strobe is generated on cic_intr to be used as a edge sensed interrupt. Note that cic_intr can be used as an interrupt or DMAREQ. Regardless of which of the two modes is selected, the interrupt output is still subject to masking bit intr_mask See Table 1-117.
3	out_align	This bit controls the 8-bit shift of the SAMP registers. It's intended to allow data alignment with the AHB bus should the resultant output data be 8 to 16 bits wide and aligned in OUTSAMPM and OUTSAMPH. In this case setting this bit allows the data in these two register to be read on OUTSAMPM and OUTSAMP - which is effectively a 8-bit right shift of the 24-bit field. See Table 1-118.
2	intr_clr	INTR_CLR is a write-only bit that clears bit0 and cic_intr. A read always produces a 0. See Table 1-115.
1	intr_mask	INTR_MASK is a RD/WR bit that controls the generation of the conversion done interrupt. A read produces the last value written to this bit. See Table 1-116.
0	conv_done	CONV_DONE is a read-only bit indicating that the most recently started conversion has completed if it has been cleared since the last sample read. This same bit is the interrupt signal cic_intr signal if not masked by bit 1. This bit is intended to provide a poling mechanism should this be preferred to receiving interrupts. It is cleared by writing a 1 to bit 2, a SW reset or a read of register OUTSAMP, OUTSAMPM or OUTSAMPH. See Table 1-113.

Reset Table

resetsignal	field(s)

1.3.168 DEC_SR (continued)

Reset Table

System reset for retention flops [reset_all_retention]	intr_mask, out_align, intr_pulse, coreclk_disable
Domain reset for non-retention flops [reset_all_nonretention]	conv_done, intr_clr

Table 1-113. Bit field encoding: conv_done_enum

Value	Name	Description
1'b1	CONV_COMP	Most recently started conversion completed.
1'b0	CONV_NOTCOMP	Conversion not completed since last clear.

Table 1-114. Bit field encoding: coreclk_disable_enum

Value	Name	Description
1'b1	CORECLK_DISABLE_HIGH	Core Clock is Disabled
1'b0	CORECLK_DISABLE_LOW	Core Clock is Enabled

Table 1-115. Bit field encoding: intr_clr_enum

Value	Name	Description
1'b1	INTR_CLEAR	Clears CONV_DONE and the interrupt on cic_intr (if enabled).
1'b0	INTR_NOP	No affect.

Table 1-116. Bit field encoding: intr_mask_enum

Value	Name	Description
1'b1	INTR_MASKED	Masks the interrupt generation on cic_intr.
1'b0	INTR_ENABLED	Allows CONV_DONE to generate an interrupt.

Table 1-117. Bit field encoding: intr_pulse_enum

Value	Name	Description
1'b1	INTR_PULSE	Selects a pulse interrupt on cic_intr.
1'b0	INTR_LEVEL	Selects a level interrupt on cic_intr.

Table 1-118. Bit field encoding: out_align_enum

Value	Name	Description
1'b1	OUT_ALIGN_HIGH	Shifts SAMP registers right by 8-bits
1'b0	OUT_ALIGN_LOW	No affect on SAMP Registers

1.3.169 DEC_SHIFT1

Decimator Shifter 1 (Input)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_SHIFT1: 0x40004E02

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R				
Name				shift1				

This register provides control information to the input (left) shifter. SHIFT1 is a 5-bit field that sets the amount of left shift that the Modulator input will be shifted. Disturbing this field during a conversion will disturb the output value. This register should only be updated while the CIC filter is in the Standby state. Conversion results are unpredictable if these bits are changed while the filter is running. Not all values from 0 to 31 make computational sense. A read of this register produces the last value written to this register.

Bits	Name	Description
4:0	shift1[4:0]	Value for left shift amount of modulator input data. 0 = no shift, 1 = left shift by 1 bit, ... up to the max supported 31.

1.3.170 DEC_SHIFT2

Decimator Shifter 2 (Output)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_SHIFT2: 0x40004E03

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					shift2			

This register provides control of the post CIC (output) shifter. This shifter sits at the input of the Post Processor and is only functional on the CIC output sample when the Post Processor is in use. SHIFT2 is a 4-bit field that sets the amount of right shift on the output of the CIC filter as it enters the Post Processor. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. Shift2 shifts right by the amount held in this register. Not all values from 0 to 15 make computational sense. A read of this register produces the last value written to this register.

Bits	Name	Description
3:0	shift2[3:0]	Value for the amount of right shift for the output of the CIC filter prior to entering the Post Processor. Functional values range from 0 to 15, 0 = no shift.

1.3.171 DEC_DR2

Decimator Decimation Rate (2)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR2: 0x40004E04

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dr2_low							

This register provides information to the Post Processor about the decimation rate of the FIR filter. This is a 10-bit field that sets the decimation ratio in the Post Processing filter. The upper 2 bits are found in register DR2H. The decimation ratio minus 1 in binary is the number to program in this 10-bit field. Valid decimation ratios are 2 to 1024. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. A read of this register produces the last value written to this register.

Bits	Name	Description
7:0	dr2_low[7:0]	FIR Filter decimation ratio bits [7:0] (of [9:0]).

1.3.172 DEC_DR2H

Decimator Decimation Rate (2)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR2H: 0x40004E05

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							dr2_high	

This register provides information about the decimation rate of the FIR filter (high). DR2 is a 10-bit field that sets the decimation ratio in the Post Processing filter. The lower 8 bits are found in register DR2. The decimation ratio minus 1 in binary is the number to program in this register. Valid decimation ratios are 2 to 1024. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. A read of this register produces the last value written to this register.

Bits	Name	Description
1:0	dr2_high[1:0]	FIR Filter decimation ratio bits [9:8] (of [9:0]).

1.3.173 DEC_DR1

Decimator Decimation Rate (1) of CIC Filter

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR1: 0x40004E06

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dr1							

This register provides the decimation rate value to the CIC filter. This 8-bit field sets the decimation ratio of the four-stage CIC filter. The decimation ratio minus 1 in binary is the number to program in this register. Although not always compuationally valid, supported decimation ratios range from 2 to 256. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. A read of this register produces the last value written to this register.

Bits	Name	Description
7:0	dr1[7:0]	CIC Filter decimation rate (2-256).

1.3.174 DEC_OCOR

Decimator Offset Correction Coefficient (Low Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCOR: 0x40004E08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	ocor_low							

This register provides information to the Post Processor about offset correction. The correction coefficient is a 24-bit 2's compliment signed field that is the offset correction value. The field is specified in the registers OCOR, OCORM, and OCORH. These 3 registers may be written while the Decimator is running. HW coherency interlocks are provide to make sure that the correction coefficient value is complete before the Post Processor is allowed to use it. See register COHER for details. A read of this register produces the last value written to this register.

Bits	Name	Description
7:0	ocor_low[7:0]	Offset correction coefficient bits [7:0] (of [23:0]).

1.3.175 DEC_OCORM

Decimator Offset Correction Coefficient (Middle Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCORM: 0x40004E09

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	ocor_mid							

This register provides information to the Post Processor about offset correction. The correction coefficient is a 24-bit 2's compliment signed field that is the offset correction value. The field is specified in the registers OCOR, OCORM, and OCORH. These 3 registers may be written while the Decimator is running. HW coherency interlocks are provide to make sure that the correction coefficient value is complete before the Post Processor is allowed to use it. See register COHER for details. A read of this register produces the last value written to this register.

Bits	Name	Description
7:0	ocor_mid[7:0]	Offset correction coefficient bits [15:8] (of [23:0]).

1.3.176 DEC_OCORH

Decimator Offset Correction Coefficient (High Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCORH: 0x40004E0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	ocor_high							

This register provides information to the Post Processor about offset correction. The correction coefficient is a 24-bit 2's compliment signed field that is the offset correction value. The field is specified in the registers OCOR, OCORM, and OCORH. These 3 registers may be written while the Decimator is running. HW coherency interlocks are provide to make sure that the correction coefficient value is complete before the Post Processor is allowed to use it. See register COHER for details. A read of this register produces the last value written to this register.

Bits	Name	Description
7:0	ocor_high[7:0]	Offset correction coefficient bits [23:16] (of [23:0]).

1.3.177 DEC_GCOR

Decimator Gain Correction Coefficient (Low Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GCOR: 0x40004E0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	gcor_low							

This register provides information to the Post Processor about the gain correction. This 16-bit field is the gain correction coefficient value. The 16-bit field is specified in registers GCOR and GCORH. Updates to the gain correction value are allowed when the Decimator is running. Coherency interlocking HW is provided for registers GCOR, GCORH and GVAL to make sure the gain coefficient and size is complete before the Post Processor is allowed to use it. See the COHER register for more details. Which bits are valid in the 16 bit field is signified by the value in the GVAL register. The implementation in HW is a shift-add multiply which consumes a clock cycle (adc_clk) for each valid bit signified by the GVAL register. A read of this register produces the last value written to this register.

Bits	Name	Description
7:0	gcor_low[7:0]	Gain correction coefficient bits [7:0] (of [15:0]).

1.3.178 DEC_GCORH

Decimator Gain Correction Coefficient (High Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GCORH: 0x40004E0D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	gcor_high							

This register provides information to the Post Processor about the gain correction. This 16-bit field is the gain correction coefficient value. The 16-bit field is specified in registers GCOR and GCORH. Updates to the gain correction value are allowed when the Decimator is running. Coherency interlocking HW is provided for registers GCOR, GCORH and GVAL to make sure the gain coefficient and size is complete before the Post Processor is allowed to use it. See the COHER register for more details. Which bits are valid in the 16 bit field is signified by the value in the GVAL register. The implementation in HW is a shift-add multiply which consumes a clock cycle (adc_clk) for each valid bit signified by the GVAL register. A read of this register produces the last value written to this register.

Bits	Name	Description
7:0	gcor_high[7:0]	Gain correction coefficient bits [15:8] (of [15:0]).

1.3.179 DEC_GVAL

Decimator Gain Correction Size Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GVAL: 0x40004E0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					gval			

This register provides information about the gain coefficient size (valid bits). GVAL is a 4-bit field that signifies to the HW how many bits of the 16-bit gain coefficient (GCOR/GCORH) are valid. The number of valid bits minus one should be written ('0000' = 1 bit, '0001' = 2 bits ..... '1111' = all 16 bits). The size is measured from LSB of GCOR (bit 0) up. For example, if it is desired to multiply by a gain coefficient of 1.5 decimal (1.1b) then GCOR is programmed with a value of '00000011', GCORH with '00000000' and GVAL with '0001' - meaning there are 2 valid bits. If the gain coefficient is to be 0.25 decimal (0.01b), GCOR = '00000001', GCORH = '00000000' and GVAL = '0010' because there are 3 valid bits. Note the implied binary point in the gain coefficient is always between the first and second most significant (left) bits in the GVAL range. For example, if GVAL = '1101' (13d), then there are 14d valid bits in the coefficient. If the coefficient in GCORH/GCOR is 'xx11000000000001' then the implied binary point is here: '1.1000000000001' - note the values of the two bits xx are ignored. The multiplier thus has a coefficient range of 1/(2^15) to 2.0-(1/(2^15)) in steps of 1/(2^15). This register is writable while the Decimator is running. GCOR, GCORH and GVAL are coherency interlocked in HW. See the COHER register for details. A read of this register produces the last value written to this register.

Bits	Name	Description
3:0	gval[3:0]	Number of valid bits minus one in Gain Coefficient registers GCORH and GCOR.

1.3.180 DEC_OUTSAMP

Decimator Output Data Sample (Low Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMP: 0x40004E10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	samp_low							

This register provides the output data sample. This register is read-only and contains, with OUTSAMPM and OUTSAMPH, the conversion result of the Decimator. This register is coherency interlock protected in HW. See register COHER for details. If the out_align bit in the CR register is set, the 16-bit result in OUTSAMPH and OUTSAMPM ([23:8]) is right-shifted by 8-bits to OUTSAMPM and OUTSAMP ([15:0]). This feature allows 16-bit results in the high two bytes to be read as one 16-bit AHB access on the low two byte lanes. Writes to this register are ignored.

Bits	Name	Description
7:0	samp_low[7:0]	Low order byte of the filter conversion result, bits [7:0] (of [23:0]) --- Or if the out_align bit is set it contains bits [15:8] (of [23:0]).

1.3.181 DEC_OUTSAMPM

Decimator Output Data Sample (Middle Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMPM: 0x40004E11

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	samp_middle							

This register provides the output data sample. This register is read-only and contains, with OUTSAMP and OUTSAMPH, the conversion result of the Decimator. This register is coherency interlock protected in HW. See register COHER for details. If the out_align bit in the CR register is set, the 16-bit result in OUTSAMPH and OUTSAMPM ([23:8]) is right-shifted by 8-bits to OUTSAMPM and OUTSAMP ([15:0]). This feature allows 16-bit results in the high two bytes to be read as one 16-bit AHB access on the low two byte lanes. Writes to this register are ignored.

Bits	Name	Description
7:0	samp_middle[7:0]	Middle order byte of the filter conversion result, bits [15:8] (of [23:0]) --- Or if the out_align bit is set it contains bits [23:16] (of [23:0]).

1.3.182 DEC_OUTSAMPH

Decimator Output Data Sample (High Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMPH: 0x40004E12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	samp_high							

This register provides the output data sample. This register is read-only and contains, with OUTSAMP and OUTSAMPM, the conversion result of the Decimator. This register is coherency interlock protected in HW. See register COHER for details. Writes to this register are ignored.

Bits	Name	Description
7:0	samp_high[7:0]	High order byte of the filter conversion result, bits [23:16] (of [23:0]).

1.3.183 DEC_OUTSAMPS

Decimator Output Data Sample (Sign Extension)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMPS: 0x40004E13

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	samp_signext							

This register provides the output data sign extension. This register is read-only and always contains 0x0 if read as a byte and always contains the sign extension of OUTSAMP when OUTSAMPH is read as a 16-bit value.

Bits	Name	Description
7:0	samp_signext[7:0]	Sign extension of the value held in OUTSAMP.

1.3.184 DEC_COHER

Decimator Coherency Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_COHER: 0x40004E14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:00		R/W:00	
HW Access	NA		R		R		R	
Name			gcor_key		ocor_key		samp_key	

The three 2-bit fields of this register are used to select which of the 3 bytes (of the OCOR, GCOR/GVAL and OUTSAMP fields) will be used as the Key Coherency Byte (KCB). Or, if no coherency checking is desired, to turn it off. The KCB selected is SW's way of tell the HW which byte of the 3-byte field it will access to signify the completion of a coherent operation. For the OCOR and GCOR/GVAL 3-byte fields, selecting the key byte tells the HW which of the bytes it will write last to note that all of the bytes it wants to update have been written. When any non-Key byte is written, the coherency HW locks the underlying ALU hardware from seeing the potentially incoherent value. While incoherent the ALU uses a shadow copy of the last coherent value received. The SW lastly writes the KCB and the HW flags the field as coherent and the next ALU operation needing that coefficient will get a copy of the newly written value. The OUTSAMP field is basically the same other than it's a read only register and the coherency protects the output sample from being overwritten by a subsequent sample if the present sample is in the process of being read. If no byte of the previous sample has been read, a new sample will overwrite the last. If the previous sample is in the process of being read, a new sample will be dropped. Coherency doesn't protect againt over/under flow, it only makes sure the sample read is coherent.

Bits	Name	Description
5:4	gcor_key[1:0]	Sets the Key Coherency Byte of the GCOR/GCORH/GVAL field See Table 1-119.
3:2	ocor_key[1:0]	Sets the Key Coherency Byte of the OCOR/OCORM/OCORH field See Table 1-120.
1:0	samp_key[1:0]	Sets the Key Coherency Byte of the OUTSAMP/OUTSAMPM/OUTSAMPH field See Table 1-121.

Table 1-119. Bit field encoding: gcor_key_enum

Value	Name	Description
2'b00	GCOR_KEY_OFF	Gain Coefficient Coherency checking off.
2'b01	GCOR_KEY_LOW	Key Byte is low byte (GCOR).
2'b10	GCOR_KEY_MID	Key Byte is med byte (GCORH).
2'b11	GCOR_KEY_HIGH	Key Byte is high byte (GVAL).

Table 1-120. Bit field encoding: ocor_key_enum

Value	Name	Description
2'b00	OCOR_KEY_OFF	Offset Coefficient Coherency checking off.
2'b01	OCOR_KEY_LOW	Key Byte is low byte (OCOR).
2'b10	OCOR_KEY_MID	Key Byte is med byte (OCORM).
2'b11	OCOR_KEY_HIGH	Key Byte is high byte (OCORH).

Table 1-121. Bit field encoding: samp_key_enum

Value	Name	Description

1.3.184 DEC_COHER (continued)

Table 1-121. Bit field encoding: samp_key_enum

2'b00	SAMP_KEY_OFF	Output Sample Coherency checking off.
2'b01	SAMP_KEY_LOW	Key Byte is low byte (OUTSAMP).
2'b10	SAMP_KEY_MID	Key Byte is med byte (OUTSAMPM).
2'b11	SAMP_KEY_HIGH	Key Byte is high byte (OUTSAMPH).

1.3.185 TMR[0..3]_CFG0

Configuration Register CFG0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CFG0: 0x40004F00 TMR1_CFG0: 0x40004F0C

TMR2_CFG0: 0x40004F18 TMR3_CFG0: 0x40004F24

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R		R	R	R	R	R	R
Name	DEADBAND_PERIOD		DB	INV	CMP_BUFF	ONESHOT	MODE	EN

This register is used to configure the timer block.

Bits	Name	Description
7:6	DEADBAND_PERIOD[1:0]	Deadband Period
5	DB	Deadband mode--routes cmpb to TC output port See Table 1-122.
4	INV	Invert sense of TIMEREN signal
3	CMP_BUFF	Buffer compare register. Compare register updates only on timer terminal count.
2	ONESHOT	Timer stops upon reaching stop condition defined by MODE_CFG bits. Can be restarted by asserting TIMER RESET or disabling and re-enabling block.
1	MODE	Mode. (0 = Timer; 1 = Comparator) See Table 1-123.
0	EN	Enables timer/comparator.

Table 1-122. Bit field encoding: db_enum

Value	Name	Description
1'b0	Terminal Count	Timer terminal count goes out on TC output port.
1'b1	CMPB	Comparator cmpb goes out on TC output port.

Table 1-123. Bit field encoding: mode_enum

Value	Name	Description
1'b0	Timer	Timer mode. CNT/CMP register holds timer count value.
1'b1	Comparator	Comparator mode. CNT/CMP register holds comparator threshold value.

1.3.186 TMR[0..3]_CFG1

Configuration Register CFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CFG1: 0x40004F01 TMR1_CFG1: 0x40004F0D

TMR2_CFG1: 0x40004F19 TMR3_CFG1: 0x40004F25

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:000			R/W:0
HW Access	R	R			R			R
Name	BUS_CLK_SEL	CLK_BUS_EN_SEL			MODE_CFG			IRQ_SEL

This register is used to configure the timer block.

Bits	Name	Description
7	BUS_CLK_SEL	Bus Clock selection. See Table 1-124.
6:4	CLK_BUS_EN_SEL[2:0]	Digital Global Clock selection. See Table 1-125.
3:1	MODE_CFG[2:0]	Timer configuration (MODE = 0): 000 = Continuous; 001 = Pulsewidth; 010 = Period; 011 = Stop on IRQ Comparator configuration (MODE = 1): 000 = '=='; 001 = '<'; 010 = '<=' 011 = '>'; 100 = '>=' See Table 1-127.
0	IRQ_SEL	Irq selection. (0 = raw interrupts; 1 = status register interrupts) See Table 1-126.

Table 1-124. Bit field encoding: bus_sel_enum

Value	Name	Description
1'b0	clk_d	Use the digital clocks, clk_d[*], as system clock.
1'b1	clk_bus	Use the system bus clock, clk_bus, as system clock.

Table 1-125. Bit field encoding: clk_cfg_enum

Value	Name	Description
3'b000	clk_d0	Select digital clock 0, clk_d[0], as clock enable.
3'b001	clk_d1	Select digital clock 1, clk_d[1], as clock enable.
3'b010	clk_d2	Select digital clock 2, clk_d[2], as clock enable.
3'b011	clk_d3	Select digital clock 3, clk_d[3], as clock enable.
3'b100	clk_d4	Select digital clock 4, clk_d[4], as clock enable.
3'b101	clk_d5	Select digital clock 5, clk_d[5], as clock enable.
3'b110	clk_d6	Select digital clock 6, clk_d[6], as clock enable.
3'b111	clk_d7	Select digital clock 7, clk_d[7], as clock enable.

Table 1-126. Bit field encoding: irq_sel_enum

Value	Name	Description
1'b0	Raw IRQ	IRQ from raw signals, maskable by corresponding mask bit in SR0 register.

1.3.186 TMR[0..3]_CFG1 (continued)

Table 1-126. Bit field encoding: irq_sel_enum

1'b1	Status IRQ	IRQ from status signals, maskable by corresponding mask bit in SR0 register. Clear interrupt by writing '0' to corresponding status bit of SR0 register.

Table 1-127. Bit field encoding: mode_cfg_enum

Value	Name	Description
3'b000	Continuous	Timer runs while EN bit of CFG0 register is set to '1'.
3'b001	Pulsewidth	Timer runs from positive to negative edge of TIMEREN.
3'b010	Period	Timer runs from positive to positive edge of TIMEREN.
3'b011	Irq	Timer runs until IRQ.
3'b000	Equal	Compare Equal '=='
3'b001	Less than	Compare Less Than '<'.
3'b010	Less than or equal	Compare Less Than or Equal '<='.
3'b011	Greater	Compare Greater Than '>'.
3'b100	Greater than or equal	Compare Greater Than or Equal '>='.

1.3.187 TMR[0..3]_PER0

Timer Period Register PER0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_PER0: 0x40004F02 TMR1_PER0: 0x40004F0E

TMR2_PER0: 0x40004F1A TMR3_PER0: 0x40004F26

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	TIMER_PERIOD0							

This register contains the count value the timer is loaded with. When enabled the counter down counts from the value of this register to zero.

Bits	Name	Description
7:0	TIMER_PERIOD0[7:0]	Determines the high byte of the period for the timer.

1.3.188 TMR[0..3]_PER1

Timer Period Register PER1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_PER1: 0x40004F03 TMR1_PER1: 0x40004F0F

TMR2_PER1: 0x40004F1B TMR3_PER1: 0x40004F27

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	TIMER_PERIOD1							

This register contains the count value the timer is loaded with. When enabled the counter down counts from the value of this register to zero.

Bits	Name	Description
7:0	TIMER_PERIOD1[7:0]	Determines the low byte of the period for the timer.

1.3.189 TMR[0..3]_CNT_CMP0

Count/Comparator value CNT/CMP0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CNT_CMP0: 0x40004F04 TMR1_CNT_CMP0: 0x40004F10

TMR2_CNT_CMP0: 0x40004F1C TMR3_CNT_CMP0: 0x40004F28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	COUNT_COMPARE0							

This register is a shared register. Its meaning depends upon the value of the MODE bit in the CFG0 register. (MODE = 0--Count value; MODE = 1--Comparator value) Register is software writeable only when MODE = 1. This register is cleared whenever the MODE bit of CFG0 register is changed.

Bits	Name	Description
7:0	COUNT_COMPARE0[7:0]	MODE = 0--LSB of current count value; MODE = 1--LSB of comparator threshold.

1.3.190 TMR[0..3]_CNT_CMP1

Count/Comparator value CNT/CMP1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CNT_CMP1: 0x40004F05 TMR1_CNT_CMP1: 0x40004F11

TMR2_CNT_CMP1: 0x40004F1D TMR3_CNT_CMP1: 0x40004F29

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	COUNT_COMPARE1							

This register is a shared register. Its meaning depends upon the value of the MODE bit in the CFG0 register. (MODE = 0--Count value; MODE = 1--Comparator value) Register is software writeable only when MODE = 1. This register is cleared whenever the MODE bit of CFG0 register is changed.

Bits	Name	Description
7:0	COUNT_COMPARE1[7:0]	MODE = 0--MSB of current count value; MODE = 1--MSB of comparator threshold.

1.3.191 TMR[0..3]_CAP0

Capture Value CAP0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CAP0: 0x40004F06 TMR1_CAP0: 0x40004F12

TMR2_CAP0: 0x40004F1E TMR3_CAP0: 0x40004F2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CAPTURE_VALUE0							

This register holds the captured LSB of the timer count value. A 16-bit read of the CNT register returns the current timer value and captures. An 8-bit LSB read of the CNT register returns the LSB and captures both the LSB and MSB. This register only has meaning when MODE = 0 and is not to be used for any purpose when MODE = 1.

Bits	Name	Description
7:0	CAPTURE_VALUE0[7:0]	Captured LSB of the timer count value.

1.3.192 TMR[0..3]_CAP1

Capture Value CAP1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CAP1: 0x40004F07 TMR1_CAP1: 0x40004F13

TMR2_CAP1: 0x40004F1F TMR3_CAP1: 0x40004F2B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CAPTURE_VALUE1							

This register holds the captured MSB of the timer count value. A 16-bit read of the CNT register returns the current timer value and captures. An 8-bit LSB read of the CNT register returns the LSB and captures both the LSB and MSB. This register only has meaning when MODE = 0 and is not to be used for any purpose when MODE = 1.

Bits	Name	Description
7:0	CAPTURE_VALUE1[7:0]	Captured MSB of the timer count value.

1.3.193 TMR[0..3]_SR0

Status Register SR0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_SR0: 0x40004F08 TMR1_SR0: 0x40004F14

TMR2_SR0: 0x40004F20 TMR3_SR0: 0x40004F2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0	RC:0	RC:0	RC:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R/W	R/W	R/W	R/W	R	R	R	R
Name	TC	CAP_CMP	TEN	TSTOP	MTC	MCAP_CMP	MTEN	MTSTOP

This register us used to configure interrupt masking and obtain status. Status bits 7-4 are cleared on read.

Bits	Name	Description
7	TC	Terminal count status. Interrupt,Sticky (individual bits)
6	CAP_CMP	Capture/Compare status (MODE = 0--Capture; MODE = 1--Compare). Interrupt,Sticky (individual bits)
5	TEN	Timer enable status. Interrupt,Sticky (individual bits)
4	TSTOP	Timer stop status. Interrupt,Sticky (individual bits)
3	MTC	Terminal count interrupt mask. (0 = Masked; 1 = Unmasked)
2	MCAP_CMP	Capture/Compare interrupt mask (MODE = 0--Capture; MODE = 1--Compare). (0 = Masked; 1 = Unmasked)
1	MTEN	Timer enable interrupt mask. (0 = Masked; 1 = Unmasked)
0	MTSTOP	Timer stop interrupt mask. (0 = Masked; 1 = Unmasked)

1.3.194 TMR[0..3]_RT0

Configuration Register RT0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_RT0: 0x40004F09

TMR1_RT0: 0x40004F15

TMR2_RT0: 0x40004F21

TMR3_RT0: 0x40004F2D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Name	TIMER_RST_SRC_SEL		TIMER_EN_SRC_SEL		CAPTURE_SRC_SEL		KILL_SRC_SEL	

This register is used to configure the dsi input routing to the timer block.

Bits	Name	Description
7:6	TIMER_RST_SRC_SEL[1:0]	Selects the driver for the timer reset signal See Table 1-128.
5:4	TIMER_EN_SRC_SEL[1:0]	Selects the driver for the timer enable signal See Table 1-128.
3:2	CAPTURE_SRC_SEL[1:0]	Selects the driver for the capture signal See Table 1-128.
1:0	KILL_SRC_SEL[1:0]	Selects the driver for the kill signal See Table 1-128.

Table 1-128. Bit field encoding: src_enum

Value	Name	Description
2'b00	dsi_in0	dsi_in0 selected as source.
2'b01	dsi_in1	dsi_in1 selected as source.
2'b10	dsi_in2	dsi_in2 selected as source.
2'b11	dsi_in3	dsi_in3 selected as source.

1.3.195 TMR[0..3]_RT1

Configuration Register RT1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_RT1: 0x40004F0A

TMR1_RT1: 0x40004F16

TMR2_RT1: 0x40004F22

TMR3_RT1: 0x40004F2E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Name			SYNCTC	SYNCCMP	SYNCDSI3	SYNCDSI2	SYNCDSI1	SYNCDSI0

This register is used to configure the dsi input routing to the timer block.

Bits	Name	Description
5	SYNCTC	Synchronize TC/TC-IRQ to selected clk_bus_en (0 = no synchronization; 1 = synchronization)
4	SYNCCMP	Synchronize CMP/CMPB output to selected clk_bus_en (0 = no synchronization; 1 = synchronization)
3	SYNCDSI3	Synchronize DSI input, dsi_in3, to clk_bus (0 = no synchronization; 1 = synchronization)
2	SYNCDSI2	Synchronize DSI input, dsi_in2, to clk_bus (0 = no synchronization; 1 = synchronization)
1	SYNCDSI1	Synchronize DSI input, dsi_in1, to clk_bus (0 = no synchronization; 1 = synchronization)
0	SYNCDSI0	Synchronize DSI input, dsi_in0, to clk_bus (0 = no synchronization; 1 = synchronization)

1.3.196 PRT[0..15]_PC[0..7]

Port Pin Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PC0: 0x40005000	PRT0_PC1: 0x40005001
PRT0_PC2: 0x40005002	PRT0_PC3: 0x40005003
PRT0_PC4: 0x40005004	PRT0_PC5: 0x40005005
PRT0_PC6: 0x40005006	PRT0_PC7: 0x40005007
PRT1_PC0: 0x40005008	PRT1_PC1: 0x40005009
PRT1_PC2: 0x4000500A	PRT1_PC3: 0x4000500B
PRT1_PC4: 0x4000500C	PRT1_PC5: 0x4000500D
PRT1_PC6: 0x4000500E	PRT1_PC7: 0x4000500F
PRT2_PC0: 0x40005010	PRT2_PC1: 0x40005011
PRT2_PC2: 0x40005012	PRT2_PC3: 0x40005013
PRT2_PC4: 0x40005014	PRT2_PC5: 0x40005015
PRT2_PC6: 0x40005016	PRT2_PC7: 0x40005017
PRT3_PC0: 0x40005018	PRT3_PC1: 0x40005019
PRT3_PC2: 0x4000501A	PRT3_PC3: 0x4000501B
PRT3_PC4: 0x4000501C	PRT3_PC5: 0x4000501D
PRT3_PC6: 0x4000501E	PRT3_PC7: 0x4000501F
PRT4_PC0: 0x40005020	PRT4_PC1: 0x40005021
PRT4_PC2: 0x40005022	PRT4_PC3: 0x40005023
PRT4_PC4: 0x40005024	PRT4_PC5: 0x40005025
PRT4_PC6: 0x40005026	PRT4_PC7: 0x40005027
PRT5_PC0: 0x40005028	PRT5_PC1: 0x40005029
PRT5_PC2: 0x4000502A	PRT5_PC3: 0x4000502B
PRT5_PC4: 0x4000502C	PRT5_PC5: 0x4000502D
PRT5_PC6: 0x4000502E	PRT5_PC7: 0x4000502F
PRT6_PC0: 0x40005030	PRT6_PC1: 0x40005031
PRT6_PC2: 0x40005032	PRT6_PC3: 0x40005033
PRT6_PC4: 0x40005034	PRT6_PC5: 0x40005035
PRT6_PC6: 0x40005036	PRT6_PC7: 0x40005037
PRT12_PC0: 0x40005060	PRT12_PC1: 0x40005061
PRT12_PC2: 0x40005062	PRT12_PC3: 0x40005063
PRT12_PC4: 0x40005064	PRT12_PC5: 0x40005065
PRT12_PC6: 0x40005066	PRT12_PC7: 0x40005067

1.3.196 PRT[0..15]_PC[0..7] (continued)

Register : Address

PRT15_PC0: 0x40005078	PRT15_PC1: 0x40005079
PRT15_PC2: 0x4000507A	PRT15_PC3: 0x4000507B
PRT15_PC4: 0x4000507C	PRT15_PC5: 0x4000507D
PRT15_PC6: 0x4000507E	PRT15_PC7: 0x4000507F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	bypass	slew	bidirEn	pin_state	driveMode_2	driveMode_1	driveMode_0	data_out

The Port Pin Configuration Registers (PRTxPC0 through PRTxPC7) access several configuration or status bits of a single I/O port pin at once. Please reference the register description of the aliased register for detailed information the port configuration controlled by a given bit.

Bits	Name	Description
7	bypass	The Bypass bit is the same as the corresponding bit in the port bypass register. See Table 1-130.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirEn	The BiDir En bit is the same as the corresponding bit in the port bidirection enable register. See Table 1-129.
4	pin_state	The Pin State bit (read only) is the same as the corresponding bit in the port pin state register.
3	driveMode_2	The DM2 bit is the same as the corresponding bit in the drive mode 2 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations.
2	driveMode_1	The DM1 bit is the same as the corresponding bit in the drive mode 1 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations.
1	driveMode_0	The DM0 bit is the same as the corresponding bit in the drive mode 0 register. Please refer to the IO chapter section on IO drive modes for detailed information on the 8 different drive mode configurations.
0	data_out	The data out bit is the same as the corresponding bit in the data register.

Table 1-129. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-130. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.197 PRT[0..15]_DR_ALIAS

Aliased Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DR_ALIAS: 0x40005080
PRT1_DR_ALIAS: 0x40005081
PRT2_DR_ALIAS: 0x40005082
PRT3_DR_ALIAS: 0x40005083
PRT4_DR_ALIAS: 0x40005084
PRT5_DR_ALIAS: 0x40005085
PRT6_DR_ALIAS: 0x40005086
PRT12_DR_ALIAS: 0x4000508C
PRT15_DR_ALIAS: 0x4000508F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DataReg_alias							

This register is used to set the output data output state for the corresponding GPIO port.

Bits	Name	Description
7:0	DataReg_alias[7:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set.

1.3.198 PRT[0..15]_PS_ALIAS

Aliased Port Pin State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PS_ALIAS: 0x40005090
PRT1_PS_ALIAS: 0x40005091
PRT2_PS_ALIAS: 0x40005092
PRT3_PS_ALIAS: 0x40005093
PRT4_PS_ALIAS: 0x40005094
PRT5_PS_ALIAS: 0x40005095
PRT6_PS_ALIAS: 0x40005096
PRT12_PS_ALIAS: 0x4000509C
PRT15_PS_ALIAS: 0x4000509F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name	PinState_alias							

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
7:0	PinState_alias[7:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0 Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin. This register is only accessible if the PRTxBIT_MASK register bits are set.

1.3.199 PRT[0..11]_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DR: 0x40005100
PRT1_DR: 0x40005110
PRT2_DR: 0x40005120
PRT3_DR: 0x40005130
PRT4_DR: 0x40005140
PRT5_DR: 0x40005150
PRT6_DR: 0x40005160

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DataReg							

This register is used to set the output data state for the corresponding GPIO port.

Bits	Name	Description
7:0	DataReg[7:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port.

1.3.200 PRT[0..11]_PS

Port Pin State Register1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PS: 0x40005101
PRT1_PS: 0x40005111
PRT2_PS: 0x40005121
PRT3_PS: 0x40005131
PRT4_PS: 0x40005141
PRT5_PS: 0x40005151
PRT6_PS: 0x40005161

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name	PinState							

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
7:0	PinState[7:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin.

1.3.201 PRT[0..11]_DM[0..2]

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DM0: 0x40005102	PRT0_DM1: 0x40005103
PRT0_DM2: 0x40005104	PRT1_DM0: 0x40005112
PRT1_DM1: 0x40005113	PRT1_DM2: 0x40005114
PRT2_DM0: 0x40005122	PRT2_DM1: 0x40005123
PRT2_DM2: 0x40005124	PRT3_DM0: 0x40005132
PRT3_DM1: 0x40005133	PRT3_DM2: 0x40005134
PRT4_DM0: 0x40005142	PRT4_DM1: 0x40005143
PRT4_DM2: 0x40005144	PRT5_DM0: 0x40005152
PRT5_DM1: 0x40005153	PRT5_DM2: 0x40005154
PRT6_DM0: 0x40005162	PRT6_DM1: 0x40005163
PRT6_DM2: 0x40005164	

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DriveMode							

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO chapter section on IO drive modes for detailed information on the eight different drive mode configurations.

Drive mode is configured on a pad by pad basis using the combination of three drive mode registers per port. Please refer to the IO chapter section on drive modes for detailed information on the eight different drive mode configurations.

DM [2:0] = {PRTx.DM2 [y] ,PRTx.DM1 [y] ,PRTx.DM0 [y] }

DM [2:0] : Drive mode setting for pin [y] 3'b000 : pin [y] drive mode set to mode 0 3'b001 : pin [y] drive mode set to mode 1 3'b010 : pin [y] drive mode set to mode 2 3'b011 : pin [y] drive mode set to mode 3 3'b100 : pin [y] drive mode set to mode 4 3'b101 : pin [y] drive mode set to mode 5 3'b110 : pin [y] drive mode set to mode 6 3'b111 : pin [y] drive mode set to mode 7

Bits	Name	Description

1.3.201 PRT[0..11]_DM[0..2] (continued)

7:0	DriveMode[7:0]	1'b0 Corresponding DM register bit asserted low. 1'b1 Corresponding DM register asserted high. The combination of the 3 drive mode register bits determines the drive mode setting for each pin. For detailed information please reference the IO section in the IROS book 1.

1.3.202 PRT[0..11]_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_SLW: 0x40005105
PRT1_SLW: 0x40005115
PRT2_SLW: 0x40005125
PRT3_SLW: 0x40005135
PRT4_SLW: 0x40005145
PRT5_SLW: 0x40005155
PRT6_SLW: 0x40005165

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	SlwCtl							

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

Bits	Name	Description
7:0	SlwCtl[7:0]	Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode

1.3.203 PRT[0..11]_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BYP: 0x40005106
PRT1_BYP: 0x40005116
PRT2_BYP: 0x40005126
PRT3_BYP: 0x40005136
PRT4_BYP: 0x40005146
PRT5_BYP: 0x40005156
PRT6_BYP: 0x40005166

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	Bypass							

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus.

Bits	Name	Description
7:0	Bypass[7:0]	1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 Port logic data register drives the corresponding port pin. *The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the ouput enable for the pad.*

1.3.204 PRT[0..11]_BIE

Port Bidirection enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BIE: 0x40005107
PRT1_BIE: 0x40005117
PRT2_BIE: 0x40005127
PRT3_BIE: 0x40005137
PRT4_BIE: 0x40005147
PRT5_BIE: 0x40005157
PRT6_BIE: 0x40005167

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	BidirectEn							

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

Bits	Name	Description
7:0	BidirectEn[7:0]	Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer

1.3.205 PRT[0..11]_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_INP_DIS: 0x40005108
PRT1_INP_DIS: 0x40005118
PRT2_INP_DIS: 0x40005128
PRT3_INP_DIS: 0x40005138
PRT4_INP_DIS: 0x40005148
PRT5_INP_DIS: 0x40005158
PRT6_INP_DIS: 0x40005168

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	Inp_dis							

The bits asserted force the input buffers off.

Bits	Name	Description
7:0	Inp_dis[7:0]	1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings.

1.3.206 PRT[0..11]_CTL

Port wide control signals

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_CTL: 0x40005109
PRT1_CTL: 0x40005119
PRT2_CTL: 0x40005129
PRT3_CTL: 0x40005139
PRT4_CTL: 0x40005149
PRT5_CTL: 0x40005159
PRT6_CTL: 0x40005169

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:000			R/W:0
HW Access	NA				R			R
Name					portEmifCfg			vtrip_sel

The port wide vtrip select register is used to select the input buffer trip point select. The emif configuration bits are used to configure the port for external memory access.

Bits	Name	Description
3:1	portEmifCfg[2:0]	GPIO emif selection option configures the port for External memory interface. See Table 1-131.
0	vtrip_sel	The GPIO cells include a vtrip_sel signal to alter the input buffer voltage. See Table 1-132.

Table 1-131. Bit field encoding: emif_cfg_enum

Value	Name	Description
3'b000	NOT_EMIF	Port not selected for EMIF control
3'b001	LSB_ADDR	Port selected as Address LS byte range
3'b010	UPR_ADDR	Port selected as Address upper byte range
3'b011	MSB_ADDR	Port selected as Address MS byte range
3'b101	LSB_DATA	Port selected as Data lower byte range
3'b110	MSB_DATA	Port selected as Data upper byte range

Table 1-132. Bit field encoding: vtrip_sel_enum

Value	Name	Description
1'b0	VTRIP_CMOS	Input buffer functions as a CMOS input buffer.
1'b1	VTRIP_LVTTL	Input buffer functions as a LVTTL input buffer.

1.3.207 PRT[0..11]_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PRT: 0x4000510A
PRT1_PRT: 0x4000511A
PRT2_PRT: 0x4000512A
PRT3_PRT: 0x4000513A
PRT4_PRT: 0x4000514A
PRT5_PRT: 0x4000515A
PRT6_PRT: 0x4000516A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	W:0	W:0	NA:0	W:0	W:0	W:0	NA:0
HW Access	R	R	R	NA	R	R	R	NA
Name	byPass	slew	bidirectEn		driveMode2	driveMode1	driveMode0	

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write.

Bits	Name	Description
7	byPass	The Bypass bit sets all the bits for the port bypass register. See Table 1-134.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirectEn	The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-133.
3	driveMode2	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
2	driveMode1	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
1	driveMode0	A write to this bit sets all bits for the corresponding drive mode register of the entire port.

Table 1-133. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-134. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.208 PRT[0..11]_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BIT_MASK: 0x4000510B
PRT1_BIT_MASK: 0x4000511B
PRT2_BIT_MASK: 0x4000512B
PRT3_BIT_MASK: 0x4000513B
PRT4_BIT_MASK: 0x4000514B
PRT5_BIT_MASK: 0x4000515B
PRT6_BIT_MASK: 0x4000516B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	Bit_mask							

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

Bits	Name	Description
7:0	Bit_mask[7:0]	1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space.

1.3.209 PRT[0..11]_AMUX

Port Analog global mux bus enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_AMUX: 0x4000510C
PRT1_AMUX: 0x4000511C
PRT2_AMUX: 0x4000512C
PRT3_AMUX: 0x4000513C
PRT4_AMUX: 0x4000514C
PRT5_AMUX: 0x4000515C
PRT6_AMUX: 0x4000516C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	Amux							

Analog global mux switch.

Bits	Name	Description
7:0	Amux[7:0]	Connects analog mux bus to the pad when asserted.

1.3.210 PRT[0..11]_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_AG: 0x4000510D
PRT1_AG: 0x4000511D
PRT2_AG: 0x4000512D
PRT3_AG: 0x4000513D
PRT4_AG: 0x4000514D
PRT5_AG: 0x4000515D
PRT6_AG: 0x4000516D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	AnalogGlobal							

Analog global switch.

Bits	Name	Description
7:0	AnalogGlobal[7:0]	Connects analog global to the pad when asserted.

1.3.211 PRT[0..11]_LCD_COM_SEG

Port LCD Com seg bits.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_LCD_COM_SEG: 0x4000510E

PRT1_LCD_COM_SEG: 0x4000511E

PRT2_LCD_COM_SEG: 0x4000512E

PRT3_LCD_COM_SEG: 0x4000513E

PRT4_LCD_COM_SEG: 0x4000514E

PRT5_LCD_COM_SEG: 0x4000515E

PRT6_LCD_COM_SEG: 0x4000516E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	com_seg							

Selects whether a pin is set as a common or segment drive pin.

Bits	Name	Description
7:0	com_seg[7:0]	Specify whether the pin will drive common or segment mode when LCD is enabled. 1'b0 Segment 1'b1 Common

1.3.212 PRT[0..11]_LCD_EN

Port LCD enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_LCD_EN: 0x4000510F
PRT1_LCD_EN: 0x4000511F
PRT2_LCD_EN: 0x4000512F
PRT3_LCD_EN: 0x4000513F
PRT4_LCD_EN: 0x4000514F
PRT5_LCD_EN: 0x4000515F
PRT6_LCD_EN: 0x4000516F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	Lcd_en							

Enables a given pin for LCD drive mode

Bits	Name	Description
7:0	Lcd_en[7:0]	Enable the pin for LCD mode. 1'b0 Disabled 1'b1 Enabled

1.3.213 PRT12_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DR: 0x400051C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DataReg							

This register is used to set the output data state for the corresponding GPIO port.

Bits	Name	Description
7:0	DataReg[7:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port.

1.3.214 PRT12_PS

Port Pin State Register1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_PS: 0x400051C1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name	PinState							

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
7:0	PinState[7:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin.

1.3.215 PRT12_DM[0..2]

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DM0: 0x400051C2 PRT12_DM1: 0x400051C3

PRT12_DM2: 0x400051C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	DriveMode							

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO chapter section on IO drive modes for detailed information on the eight different drive mode configurations.

Drive mode is configured on a pad by pad basis using the combination of three drive mode registers per port. Please refer to the IO chapter section on drive modes for detailed information on the eight different drive mode configurations.

DM [2:0] = {PRTx.DM2 [y] ,PRTx.DM1 [y] ,PRTx.DM0 [y] }

DM [2:0] : Drive mode setting for pin [y] 3'b000 : pin [y] drive mode set to mode 0 3'b001 : pin [y] drive mode set to mode 1 3'b010 : pin [y] drive mode set to mode 2 3'b011 : pin [y] drive mode set to mode 3 3'b100 : pin [y] drive mode set to mode 4 3'b101 : pin [y] drive mode set to mode 5 3'b110 : pin [y] drive mode set to mode 6 3'b111 : pin [y] drive mode set to mode 7

Bits	Name	Description
7:0	DriveMode[7:0]	1'b0 Corresponding DM register bit asserted low. 1'b1 Corresponding DM register asserted high. The combination of the 3 drive mode register bits determines the drive mode setting for each pin. For detailed information please reference the IO section in the IROS book 1.

1.3.216 PRT12_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SLW: 0x400051C5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	SlwCtl							

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

Bits	Name	Description
7:0	SlwCtl[7:0]	Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode

1.3.217 PRT12_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BYP: 0x400051C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	Bypass							

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus.

Bits	Name	Description
7:0	Bypass[7:0]	1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 Port logic data register drives the corresponding port pin. *The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the ouput enable for the pad.*

1.3.218 PRT12_BIE

Port Bidirection enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BIE: 0x400051C7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	BidirectEn							

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

Bits	Name	Description
7:0	BidirectEn[7:0]	Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer

1.3.219 PRT12_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_INP_DIS: 0x400051C8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	Inp_dis							

The bits asserted force the input buffers off.

Bits	Name	Description
7:0	Inp_dis[7:0]	1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings.

1.3.220 PRT12_SIO_HYST_EN

SIO Hysteresis enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_HYST_EN: 0x400051C9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sio_diff_hyst_en							

The SIO hysteresis enable for the SIO differential input buffer.

Bits	Name	Description
7:0	sio_diff_hyst_en[7:0]	(no description)

1.3.221 PRT12_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_PRT: 0x400051CA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	W:0	W:0	NA:0	W:0	W:0	W:0	NA:0
HW Access	R	R	R	NA	R	R	R	NA
Name	byPass	slew	bidirectEn		driveMode2	driveMode1	driveMode0	

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write.

Bits	Name	Description
7	byPass	The Bypass bit sets all the bits for the port bypass register. See Table 1-136.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirectEn	The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-135.
3	driveMode2	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
2	driveMode1	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
1	driveMode0	A write to this bit sets all bits for the corresponding drive mode register of the entire port.

Table 1-135. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-136. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.222 PRT12_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BIT_MASK: 0x400051CB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	Bit_mask							

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

Bits	Name	Description
7:0	Bit_mask[7:0]	1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space.

1.3.223 PRT12_SIO_REG_HIFREQ

Regulated pull-up driver DC current setting

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_REG_HIFREQ: 0x400051CC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Name	sio_reg_hifreq_7_6		sio_reg_hifreq_5_4		sio_reg_hifreq_3_2		sio_reg_hifreq_1_0	

Sets each SIO pair's pull-up driver DC current.

Bits	Name	Description
7	sio_reg_hifreq_7_6	pull-up driver DC current
5	sio_reg_hifreq_5_4	pull-up driver DC current
3	sio_reg_hifreq_3_2	pull-up driver DC current
1	sio_reg_hifreq_1_0	pull-up driver DC current

1.3.224 PRT12_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_AG: 0x400051CD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Name	AnalogGlobal_7_6		AnalogGlobal_5_4		AnalogGlobal_3_2		AnalogGlobal_1_0	

Analog global switch.

Bits	Name	Description
7:6	AnalogGlobal_7_6[1:0]	Connects analog global when asserted. See Table 1-137.
5:4	AnalogGlobal_5_4[1:0]	Connects analog global when asserted. See Table 1-137.
3:2	AnalogGlobal_3_2[1:0]	Connects analog global when asserted. See Table 1-137.
1:0	AnalogGlobal_1_0[1:0]	Connects analog global when asserted. See Table 1-137.

Table 1-137. Bit field encoding: pr12_ag_enum

Value	Name	Description
2'b00	NO_AG	No AG selected.
2'b01	AG0_SEL	low bit AG connection selected.
2'b10	AG1_SEL	high bit AG connection selected.
2'b11	VCCD_SEL	VCCD selected.

1.3.225 PRT12_SIO_CFG

SIO Input Output Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_CFG: 0x400051CE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	ibuf_sel_7_6	vreg_en_7_6	ibuf_sel_5_4	vreg_en_5_4	ibuf_sel_3_2	vreg_en_3_2	ibuf_sel_1_0	vreg_en_1_0

Sets each SIO pair's input output Configuration. vreg_en=0 & ibuf_sel=0 sets the mode to Single Ended Input Buffer, Non-regulated Output Buffer. vreg_en=0 & ibuf_sel=1 sets the mode to Differential Input Buffer, Non-regulated Output Buffer. vreg_en=1 & ibuf_sel=0 sets the mode to Single Ended Input Buffer, Regulated Output Buffer. vreg_en=1 & ibuf_sel=1 sets the mode to Differential Input Buffer, Regulated Output Buffer.

Bits	Name	Description
7	ibuf_sel_7_6	sets the ibuf_sel for the corresponding SIO pair
6	vreg_en_7_6	sets the vreg_en for the corresponding SIO pair
5	ibuf_sel_5_4	sets the ibuf_sel for the corresponding SIO pair
4	vreg_en_5_4	sets the vreg_en for the corresponding SIO pair
3	ibuf_sel_3_2	sets the ibuf_sel for the corresponding SIO pair
2	vreg_en_3_2	sets the vreg_en for the corresponding SIO pair
1	ibuf_sel_1_0	sets the ibuf_sel for the corresponding SIO pair
0	vreg_en_1_0	sets the vreg_en for the corresponding SIO pair

1.3.226 PRT12_SIO_DIFF

Differential Input Buffer reference voltage selection

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_DIFF: 0x400051CF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vref_sel_7_6	vtrip_sel_7_6	vref_sel_5_4	vtrip_sel_5_4	vref_sel_3_2	vtrip_sel_3_2	vref_sel_1_0	vtrip_sel_1_0

Sets each SIO pair's input reference voltage. vref_sel=0 & vtrip_sel=0 sets the differential input buffer to 0.5*vcc_io. vref_sel=0 & vtrip_sel=1 sets the differential input buffer to 0.4*vcc_io. vref_sel=1 & vtrip_sel=0 sets the differential input buffer to 0.5*vohref. vref_sel=1 & vtrip_sel=1 sets the differential input buffer to vohref.

Bits	Name	Description
7	vref_sel_7_6	sets the vref_sel for the corresponding SIO pair
6	vtrip_sel_7_6	sets the vtrip_sel for the corresponding SIO pair
5	vref_sel_5_4	sets the vref_sel for the corresponding SIO pair
4	vtrip_sel_5_4	sets the vtrip_sel for the corresponding SIO pair
3	vref_sel_3_2	sets the vref_sel for the corresponding SIO pair
2	vtrip_sel_3_2	sets the vtrip_sel for the corresponding SIO pair
1	vref_sel_1_0	sets the vref_sel for the corresponding SIO pair
0	vtrip_sel_1_0	sets the vtrip_sel for the corresponding SIO pair

1.3.227 PRT15_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DR: 0x400051F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			DataReg					

This register is used to set the output data state for the corresponding GPIO port.

Bits	Name	Description
5:0	DataReg[5:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port.

1.3.228 PRT15_PS

Port Pin State Register1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_PS: 0x400051F1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R:000000					
HW Access	NA		R					
Name			PinState					

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
5:0	PinState[5:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to High-Z Analog, the pin state will read 0 independent of the voltage on the pin.

1.3.229 PRT15_DM[0..2]

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DM0: 0x400051F2 PRT15_DM1: 0x400051F3

PRT15_DM2: 0x400051F4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			DriveMode					

These registers, PRT15.DM2, PRT15.DM1, and PRT15.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0].

Drive mode is configured on a pad by pad basis using the combination of three drive mode registers per port. Please refer to the IO chapter section on drive modes for detailed information on the eight different drive mode configurations.

DM [2:0] = {PRT15.DM2 [y] ,PRT15.DM1 [y] ,PRT15.DM0 [y] }

DM [2:0] : Drive mode setting for pin [y] 3'b000 : pin [y] drive mode set to mode 0 3'b001 : pin [y] drive mode set to mode 1 3'b010 : pin [y] drive mode set to mode 2 3'b011 : pin [y] drive mode set to mode 3 3'b100 : pin [y] drive mode set to mode 4 3'b101 : pin [y] drive mode set to mode 5 3'b110 : pin [y] drive mode set to mode 6 3'b111 : pin [y] drive mode set to mode 7

Bits	Name	Description
5:0	DriveMode[5:0]	1'b0 Corresponding DM register bit asserted low. 1'b1 Corresponding DM register asserted high. The combination of the 3 drive mode register bits determines the drive mode setting for each pin. For detailed information please reference the IO section in the IROS book 1.

1.3.230 PRT15_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_SLW: 0x400051F5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			SlwCtl					

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

Bits	Name	Description
5:0	SlwCtl[5:0]	Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode

1.3.231 PRT15_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BYP: 0x400051F6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:000000					
HW Access	R		R					
Name	Bypass_usb		Bypass					

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus. Shared USB pins must be set to GPIO mode.

Bits	Name	Description
7:6	Bypass_usb[1:0]	1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 DMI/DPI outputs from USB drives the corresponding port pin configured in IO mode. *GPIO mode must be enabled in order to bypass the shared function USB/IO pins.*
5:0	Bypass[5:0]	1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 Port logic data register drives the corresponding port pin. *The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the ouput enable for the pad.*

1.3.232 PRT15_BIE

Port Bidirection enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BIE: 0x400051F7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			BidirectEn					

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

Bits	Name	Description
5:0	BidirectEn[5:0]	Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer

1.3.233 PRT15_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_INP_DIS: 0x400051F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			Inp_dis					

The bits asserted force the input buffers off.

Bits	Name	Description
5:0	Inp_dis[5:0]	1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings.

1.3.234 PRT15_CTL

Port wide control signals

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_CTL: 0x400051F9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								vtrip_sel

The port wide vtrip select register is used to select the input buffer trip point select

Bits	Name	Description
0	vtrip_sel	The GPIO cells include a vtrip_sel signal to alter the input buffer voltage. See Table 1-138.

Table 1-138. Bit field encoding: vtrip_sel_enum

Value	Name	Description
1'b0	VTRIP_CMOS	Input buffer functions as a CMOS input buffer.
1'b1	VTRIP_LVTTL	Input buffer functions as a LVTTL input buffer.

1.3.235 PRT15_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_PRT: 0x400051FA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	W:0	W:0	NA:0	W:0	W:0	W:0	NA:0
HW Access	R	R	R	NA	R	R	R	NA
Name	byPass	slew	bidirectEn		driveMode2	driveMode1	driveMode0	

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write.

Bits	Name	Description
7	byPass	The Bypass bit sets all the bits for the port bypass register. See Table 1-140.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirectEn	The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-139.
3	driveMode2	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
2	driveMode1	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
1	driveMode0	A write to this bit sets all bits for the corresponding drive mode register of the entire port.

Table 1-139. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-140. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.236 PRT15_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BIT_MASK: 0x400051FB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			Bit_mask					

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

Bits	Name	Description
5:0	Bit_mask[5:0]	1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space.

1.3.237 PRT15_AMUX

Port Analog global mux bus enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_AMUX: 0x400051FC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			Amux					

Analog global mux switch.

Bits	Name	Description
5:0	Amux[5:0]	Connects analog mux bus to the pad when asserted.

1.3.238 PRT15_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_AG: 0x400051FD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			AnalogGlobal					

Analog global switch.

Bits	Name	Description
5:0	AnalogGlobal[5:0]	Connects analog global to the pad when asserted.

1.3.239 PRT15_LCD_COM_SEG

Port LCD Com seg bits.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_LCD_COM_SEG: 0x400051FE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			com_seg					

Selects whether a pin is set as a common or segment drive pin.

Bits	Name	Description
5:0	com_seg[5:0]	Specify whether the pin will drive common or segment mode when LCD is enabled. 1'b0 Segment 1'b1 Common

1.3.240 PRT15_LCD_EN

Port LCD enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_LCD_EN: 0x400051FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			Lcd_en					

Enables a given pin for LCD drive mode

Bits	Name	Description
5:0	Lcd_en[5:0]	Enable the pin for LCD mode. 1'b0 Disabled 1'b1 Enabled

1.3.241 PRT0_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OUT_SEL0: 0x40005200

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.242 PRT0_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OUT_SEL1: 0x40005201

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.243 PRT0_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OE_SEL0: 0x40005202

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.244 PRT0_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OE_SEL1: 0x40005203

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.245 PRT0_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DBL_SYNC_IN: 0x40005204

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.246 PRT0_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_SYNC_OUT: 0x40005205

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.247 PRT0_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_CAPS_SEL: 0x40005206

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.248 PRT1_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OUT_SEL0: 0x40005208

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.249 PRT1_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OUT_SEL1: 0x40005209

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.250 PRT1_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OE_SEL0: 0x4000520A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.251 PRT1_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OE_SEL1: 0x4000520B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.252 PRT1_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_DBL_SYNC_IN: 0x4000520C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.253 PRT1_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_SYNC_OUT: 0x4000520D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.254 PRT1_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_CAPS_SEL: 0x4000520E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.255 PRT2_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OUT_SEL0: 0x40005210

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.256 PRT2_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OUT_SEL1: 0x40005211

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.257 PRT2_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OE_SEL0: 0x40005212

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.258 PRT2_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OE_SEL1: 0x40005213

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.259 PRT2_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_DBL_SYNC_IN: 0x40005214

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.260 PRT2_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_SYNC_OUT: 0x40005215

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.261 PRT2_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_CAPS_SEL: 0x40005216

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.262 PRT3_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OUT_SEL0: 0x40005218

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.263 PRT3_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OUT_SEL1: 0x40005219

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.264 PRT3_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OE_SEL0: 0x4000521A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.265 PRT3_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OE_SEL1: 0x4000521B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.266 PRT3_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_DBL_SYNC_IN: 0x4000521C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.267 PRT3_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_SYNC_OUT: 0x4000521D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.268 PRT3_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_CAPS_SEL: 0x4000521E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.269 PRT4_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OUT_SEL0: 0x40005220

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.270 PRT4_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OUT_SEL1: 0x40005221

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.271 PRT4_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OE_SEL0: 0x40005222

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.272 PRT4_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OE_SEL1: 0x40005223

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.273 PRT4_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_DBL_SYNC_IN: 0x40005224

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.274 PRT4_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_SYNC_OUT: 0x40005225

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.275 PRT4_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_CAPS_SEL: 0x40005226

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.276 PRT5_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OUT_SEL0: 0x40005228

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.277 PRT5_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OUT_SEL1: 0x40005229

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.278 PRT5_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OE_SEL0: 0x4000522A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.279 PRT5_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OE_SEL1: 0x4000522B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.280 PRT5_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_DBL_SYNC_IN: 0x4000522C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.281 PRT5_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_SYNC_OUT: 0x4000522D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.282 PRT5_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_CAPS_SEL: 0x4000522E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.283 PRT6_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OUT_SEL0: 0x40005230

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.284 PRT6_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OUT_SEL1: 0x40005231

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.285 PRT6_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OE_SEL0: 0x40005232

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.286 PRT6_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OE_SEL1: 0x40005233

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.287 PRT6_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_DBL_SYNC_IN: 0x40005234

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.288 PRT6_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_SYNC_OUT: 0x40005235

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.289 PRT6_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_CAPS_SEL: 0x40005236

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.290 PRT12_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OUT_SEL0: 0x40005260

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.291 PRT12_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OUT_SEL1: 0x40005261

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.292 PRT12_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OE_SEL0: 0x40005262

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.293 PRT12_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OE_SEL1: 0x40005263

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.294 PRT12_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DBL_SYNC_IN: 0x40005264

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.295 PRT12_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SYNC_OUT: 0x40005265

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.296 PRT15_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OUT_SEL0: 0x40005278

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*]** } TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.297 PRT15_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OUT_SEL1: 0x40005279

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.298 PRT15_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OE_SEL0: 0x4000527A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			portOEsel					

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
5:0	portOEsel[5:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.299 PRT15_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OE_SEL1: 0x4000527B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			portOEsel					

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
5:0	portOEsel[5:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.300 PRT15_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DBL_SYNC_IN: 0x4000527C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.301 PRT15_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_SYNC_OUT: 0x4000527D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			sync_out					

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
5:0	sync_out[5:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.302 PRT15_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_CAPS_SEL: 0x4000527E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			sync_out					

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
5:0	sync_out[5:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.303 EMIF_NO_UDB

EMIF UDB Generation Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_NO_UDB: 0x40005400

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								no_udb

This register indicates whether UDBs are generating external memory control signals or to enable EMIF to generate them for Flow Through Sync SRAM. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
0	no_udb	1'b0: UDBs are generating control signals for external memory. 1`b1: EMIF to generate control signals for Flow through Sync SRAM external memory

1.3.304 EMIF_WAIT_STATES

External Memory Interface Wait States Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_WAIT_STATES: 0x40005401

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						wait_states		

This register configures the wait states for PHUB. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
2:0	wait_states[2:0]	No of additional clock cycles (wait states) required to complete the data transfer to Flow Through Sync SRAM.

1.3.305 EMIF_MEM_DWN

External Memory Power Down Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_MEM_DWN: 0x40005402

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								mem_pd

This register puts the external memory into power down mode. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
0	mem_pd	1`b1: External Memory power down. 1`b0: External memory power up

1.3.306 EMIF_MEMCLK_DIV

External Memory Clock Divider Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_MEMCLK_DIV: 0x40005403

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							memclk_div	

This register sets the divider for external memory clock frequency. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
1:0	memclk_div[1:0]	2'b00: External Memory clock frequency is equal to HCLK frequency. 2'b01: External Memory clock frequency is equal to half of HCLK frequency. 2'b10: External Memory clock frequency is equal to one-fourth of HCLK frequency. 2'b11: same as 2'b00

1.3.307 EMIF_CLOCK_EN

EMIF Clock Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_CLOCK_EN: 0x40005404

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								clock_en

This register enables the clock for EMIF core logic.

Bits	Name	Description
0	clock_en	1'b0: Disable Clock for EMIF core logic. 1'b1: Enable Clock for EMIF core. Along with this bit, the input 'emif_clk_en' to EMIF block should also be 1'b1 to enable the clock. This input can be made 1'b1 by setting corresponding bit in PM.ACT.CFG5 register in Power Manager.

1.3.308 SC[0..3]_CR0

Switched Capacitor Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR0: 0x40005800 SC1_CR0: 0x40005804

SC2_CR0: 0x40005808 SC3_CR0: 0x4000580C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:000			NA:0
HW Access	NA		R		R			NA
Name			dft		mode			

(no description)

Bits	Name	Description
5:4	dft[1:0]	Enables DFT mode for the switch cap block See Table 1-141.
3:1	mode[2:0]	Configuration select for the SC block See Table 1-142.

Table 1-141. Bit field encoding: SC_DFT_ENUM

Value	Name	Description
2'h0	SC_DFT_NORMAL	Normal Operation
2'h1	SC_DFT_VBOOST	Vboost DFT
2'h2	SC_DFT_NOTUSED	Not Used
2'h3	SC_DFT_RESET	DFT Rreset

Table 1-142. Bit field encoding: SC_MODE_ENUM

Value	Name	Description
3'b000	SC_MODE_NAKED_OP AMP	Naked Op-Amp
3'b001	SC_MODE_TIA	TIA
3'b010	SC_MODE_CTMIXER	Continuous Time Mixer
3'b011	SC_MODE_NRZ_SH	NRZ S/H
3'b100	SC_MODE_UNITY_1	Unity Gain Buffer
3'b101	SC_MODE_1ST_MOD	First Order Modulator
3'b110	SC_MODE_PGA	Programmable Gain Amplifier
3'b111	SC_MODE_UNITY_2	Unity Gain Buffer

1.3.309 SC[0..3]_CR1

Switched Capacitor Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR1: 0x40005801 SC1_CR1: 0x40005805

SC2_CR1: 0x40005809 SC3_CR1: 0x4000580D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	NA		R	R	R		R	
Name			gain	div2	comp		drive	

(no description)

Bits	Name	Description
5	gain	Controls the ratio of the feedback cap for S/H Mixer mode and PGA mode See Table 1-146.
4	div2	When 0, the sample clock only needs to be half the desired sample frequency for S/H Mixer mode See Table 1-144.
3:2	comp[1:0]	Selects between various compensation capacitor sizes See Table 1-143.
1:0	drive[1:0]	Selects between current settings in the output buffer See Table 1-145.

Table 1-143. Bit field encoding: SC_COMP_ENUM

Value	Name	Description
2'b00	SC_COMP_3P0PF	3.0pF
2'b01	SC_COMP_3P6PF	3.6pF
2'b10	SC_COMP_4P35PF	4.35pF
2'b11	SC_COMP_5P1PF	5.1pF

Table 1-144. Bit field encoding: SC_DIV2_ENUM

Value	Name	Description
1'b0	SC_DIV2_DISABLE	no frequency division
1'b1	SC_DIV2_ENABLE	SC CLK is divided by two

Table 1-145. Bit field encoding: SC_DRIVE_ENUM

Value	Name	Description
2'b00	I_LOAD_280UA	280 uA
2'b01	I_LOAD_420UA	420 uA
2'b10	I_LOAD_530UA	530 uA
2'b11	I_LOAD_650UA	650 uA

Table 1-146. Bit field encoding: SC_GAIN_ENUM

Value	Name	Description
1'b0	GAIN_0DB	0 dB

1.3.309 SC[0..3]_CR1 (continued)

Table 1-146. Bit field encoding: SC_GAIN_ENUM

1'b1	GAIN_6DB	6 dB

1.3.310 SC[0..3]_CR2

Switched Capacitor Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR2: 0x40005802 SC1_CR2: 0x40005806

SC2_CR2: 0x4000580A SC3_CR2: 0x4000580E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:00		R/W:0	R/W:0
HW Access	R	R			R		R	R
Name	pga_gndvref	rval			redc		r20_40b	bias_ctrl

(no description)

Bits	Name	Description
7	pga_gndvref	Programmable Gain Amplifier Application - Ground VREF See Table 1-148.
6:4	rval[2:0]	Feedback resistor adjust control signals See Table 1-151.
3:2	redc[1:0]	Another stability control setting. Adjusts capactiance between amplifier output and first stage See Table 1-150.
1	r20_40b	Toggles the input impedance between 20k and 40k See Table 1-149.
0	bias_ctrl	Toggles the bias current in the amplifier between normal and 1/2 See Table 1-147.

Table 1-147. Bit field encoding: SC_BIAS_CONTROL_ENUM

Value	Name	Description
1'b0	BIAS_NORMAL	normal operation
1'b1	BIAS_LOW	reduces bandwidth to increase stability

Table 1-148. Bit field encoding: SC_PGA_GNDVREF_ENUM

Value	Name	Description
1'b0	SC_PGA_GNDVREF_DIS	VREF not grounded
1'b1	SC_PGA_GNDVREF_EN	VREF grounded

Table 1-149. Bit field encoding: SC_R20_40B_ENUM

Value	Name	Description
1'b0	SC_R20_40B_40K	40k
1'b1	SC_R20_40B_20K	20k

Table 1-150. Bit field encoding: SC_REDC_ENUM

Value	Name	Description

1.3.310 SC[0..3]_CR2 (continued)

Table 1-150. Bit field encoding: SC_REDC_ENUM

2'b00	SC_REDC_00	***TODO:change enum name and description***
2'b01	SC_REDC_01	***TODO:change enum name and description***
2'b10	SC_REDC_10	***TODO:change enum name and description***
2'b11	SC_REDC_11	***TODO:change enum name and description***

Table 1-151. Bit field encoding: SC_RVAL_ENUM

Value	Name	Description
3'b000	SC_RVAL_20	20kOhm
3'b001	SC_RVAL_30	30
3'b010	SC_RVAL_40	40
3'b011	SC_RVAL_60	60
3'b100	SC_RVAL_120	120
3'b101	SC_RVAL_250	250
3'b110	SC_RVAL_500	500
3'b111	SC_RVAL_1000	1000

1.3.311 DAC[0..3]_CR0

DAC Block Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_CR0: 0x40005820 DAC1_CR0: 0x40005824

DAC2_CR0: 0x40005828 DAC3_CR0: 0x4000582C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:00		R/W:0	NA:0
HW Access	NA			R	R		R	NA
Name				mode	range		hs	

(no description)

Bits	Name	Description
4	mode	Mode Bit See Table 1-153.
3:2	range[1:0]	Ranges for mode=0 (VDAC) and mode=1 (IDAC) See Table 1-154.
1	hs	High Speed Bit See Table 1-152.

Table 1-152. Bit field encoding: DAC_HS_ENUM

Value	Name	Description
1'b0	DAC_HS_LOWPOWER	regular (low power)
1'b1	DAC_HS_HIGHSPEED	high speed (higher power)

Table 1-153. Bit field encoding: DAC_MODE_ENUM

Value	Name	Description
1'b0	DAC_MODE_V	voltage DAC
1'b1	DAC_MODE_I	current DAC

Table 1-154. Bit field encoding: DAC_RANGE_ENUM

Value	Name	Description
2'b00	DAC_RANGE_0	x0=0V to 4*vref (1.024V); 0 to 31.875uA
2'b01	DAC_RANGE_1	x1=0V to 16*vref (4.096V); 0 to 255uA
2'b10	DAC_RANGE_2	x0=0V to 4*vref (1.024V); 0 to 2.040mA
2'b11	DAC_RANGE_3	x1=0V to 16*vref (4.096V); not used

1.3.312 DAC[0..3]_CR1

DAC Block Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_CR1: 0x40005821 DAC1_CR1: 0x40005825

DAC2_CR1: 0x40005829 DAC3_CR1: 0x4000582D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Name			mx_data	reset_udb_en	mx_idir	idirbit	mx_ioff	ioffbit

(no description)

Bits	Name	Description
5	mx_data	Select DATA source See Table 1-155.
4	reset_udb_en	DAC reset enable See Table 1-158.
3	mx_idir	Mux selection for DAC current direction control See Table 1-156.
2	idirbit	register source for DAC current direction
1	mx_ioff	Mux selection for DAC current off control See Table 1-157.
0	ioffbit	register source for DAC current off

Table 1-155. Bit field encoding: MX_DATA_ENUM

Value	Name	Description
1'b0	MX_DATA_REG	Select register source (DACxn_D)
1'b1	MX_DATA_UDB	Select UDB source

Table 1-156. Bit field encoding: MX_IDIR_ENUM

Value	Name	Description
1'b0	MX_IDIR_REG	Register source idirbit selected
1'b1	MX_IDIR_UDB	UDB ictrl selected

Table 1-157. Bit field encoding: MX_IOFF_ENUM

Value	Name	Description
1'b0	MX_IOFF_REG	Register source ioffbit selected
1'b1	MX_IOFF_UDB	UDB ictrl selected

Table 1-158. Bit field encoding: RESET_UDB_EN_ENUM

Value	Name	Description
1'b0	RESET_UDB_EN_DISABLE	Disable DAC Reset Source from UDB (System reset always resets)

1.3.312 DAC[0..3]_CR1 (continued)

Table 1-158. Bit field encoding: RESET_UDB_EN_ENUM

1'b1	RESET_UDB_EN_ENABLE	Enable DAC Reset Source from UDB

1.3.313 DAC[0..3]_TST

DAC Block Test Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_TST: 0x40005822 DAC1_TST: 0x40005826

DAC2_TST: 0x4000582A DAC3_TST: 0x4000582E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R				
Name				test				

(no description)

Bits	Name	Description
4:0	test[4:0]	5 test-select bits for bringing out internal nodes through an analog mux. Table shows internal net and test description See Table 1-159.

Table 1-159. Bit field encoding: DAC_TEST_SEL

Value	Name	Description
5'h0	DAC_TEST_SEL_0	N/A | no operation
5'h1	DAC_TEST_SEL_1	en_hv | level-shifted enable bit (1 = 0N)
5'h0	DAC_TEST_SEL_2	hs_hv | level-shifted high-speed bit (1 = high-speed ON)
5'h0	DAC_TEST_SEL_3	en_vref | level-shifted vmode enable bit (1 = vmode)
5'h0	DAC_TEST_SEL_4	en_iref | level-shifted imode enable bit (1 = imode)
5'h0	DAC_TEST_SEL_5	vref | vref input level (256mV DC)
5'h0	DAC_TEST_SEL_6	vfb | vref level across reference resistor (256mV DC)
5'h0	DAC_TEST_SEL_7	en_1v | level-shifted 1V vmode range bit (1 = 0 to 1V range)
5'h0	DAC_TEST_SEL_8	en_4v | level-shifted 4V vmode range bit (1 = 0 to 4V range)
5'h0	DAC_TEST_SEL_9	mode_hv | level-shifted mode bit (1 = imode)
5'h0	DAC_TEST_SEL_10	en_1x_source | level-shifted enable bit for 1X output current source
5'h0	DAC_TEST_SEL_11	en_7x_source | level-shifted enable bit for 7X output current source
5'h0	DAC_TEST_SEL_12	en_63x_source | level-shifted enable bit for 63X output current source
5'h0	DAC_TEST_SEL_13	en_1x_sink | level-shifted enable bit for 1X output current sink
5'h0	DAC_TEST_SEL_14	en_7x_sink | level-shifted enable bit for 7X output current sink
5'h0	DAC_TEST_SEL_15	en_63x_sink | level-shifted enable bit for 63X output current sink
5'h0	DAC_TEST_SEL_16	en_cal[7] | Internal calibration select bit [7] (64*LSB adjust)
5'h0	DAC_TEST_SEL_17	en_cal[6] | Internal calibration select bit [6] (32*LSB adjust)
5'h0	DAC_TEST_SEL_18	en_cal[5] | Internal calibration select bit [5] (16*LSB adjust)
5'h0	DAC_TEST_SEL_19	en_cal[4] | Internal calibration select bit [4] (8*LSB adjust)
5'h0	DAC_TEST_SEL_20	en_cal[3] | Internal calibration select bit [3] (4*LSB adjust)
5'h0	DAC_TEST_SEL_21	en_cal[2] | Internal calibration select bit [2] (2*LSB adjust)
5'h0	DAC_TEST_SEL_22	en_cal[1] | Internal calibration select bit [1] (1*LSB adjust)
5'h0	DAC_TEST_SEL_23	en_cal[0] | Internal calibration select bit [0] (0.5*LSB adjust)
5'h0	DAC_TEST_SEL_24	vb | bias voltage from reference DAC to mirror DAC (approx 1.1V below vhv, eg if vhv = 4.1V, vb ~ 3V
5'h0	DAC_TEST_SEL_25	vhv | Measure locally to estimate IR drop
5'h0	DAC_TEST_SEL_26	vpwr | Measure locally to estimate IR drop
5'h0	DAC_TEST_SEL_27	vgnd | Measure locally to estimate IR drop
5'h0	DAC_TEST_SEL_28	resetb | inverted reset signal to reset FF's

1.3.313 DAC[0..3]_TST (continued)

Table 1-159. Bit field encoding: DAC_TEST_SEL

5'h0	DAC_TEST_SEL_29	dac_iout | measure DAC current output (at block pin)
5'h0	DAC_TEST_SEL_30	dac_vout | measure DAC voltage output (at block pin)
5'h0	DAC_TEST_SEL_31	i_dac_out | measure internal DAC current output

1.3.314 CMP[0..3]_CR

Comparator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_CR: 0x40005840 CMP1_CR: 0x40005841

CMP2_CR: 0x40005842 CMP3_CR: 0x40005843

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	NA	R	R	R	R	R	R	
Name		filt	hyst	cal_en	mx_ao	pd_override	sel	

(no description)

Bits	Name	Description
6	filt	enables a glitch filter at the output of the comparator See Table 1-161.
5	hyst	enables a hysteresis of 10mV typ. See Table 1-162.
4	cal_en	enables shorting of the two comparator inputs for trim calibration purposes See Table 1-160.
3	mx_ao	comparator sleep always-on logic mux control See Table 1-163.
2	pd_override	Power down override to allow comparator to continue operating during sleep See Table 1-164.
1:0	sel[1:0]	Selects the mode of operation of the comparator See Table 1-165.

Table 1-160. Bit field encoding: CMP_CAL_EN_ENUM

Value	Name	Description
1'b0	CMP_CAL_EN_DISABLE	Disable calibration
1'b1	CMP_CAL_EN_ENABLE	Enable calibration

Table 1-161. Bit field encoding: CMP_FILT_ENUM

Value	Name	Description
1'b0	CMP_FILT_DISABLE	Disable glitch filter
1'b1	CMP_FILT_ENABLE	Enable glitch filter

Table 1-162. Bit field encoding: CMP_HYST_ENUM

Value	Name	Description
1'b0	CMP_HYST_DISABLE	Disable hysteresis
1'b1	CMP_HYST_ENABLE	Enable hysteresis

1.3.314 CMP[0..3]_CR (continued)

Table 1-163. Bit field encoding: CMP_MX_AO_ENUM

Value	Name	Description
1'b0	CMP_MX_AO_BYPASS	Bypass comparator sleep always-on logic
1'b1	CMP_MX_AO_ENABLE	Enable comparator sleep always-on logic

Table 1-164. Bit field encoding: CMP_PD_OVERRIDE_ENUM

Value	Name	Description
1'b0	CMP_PD_OVERRIDE_DISABLE	Don't override power down
1'b1	CMP_PD_OVERRIDE_ENABLE	Override power down

Table 1-165. Bit field encoding: SEL_ENUM

Value	Name	Description
2'b00	SEL_SLOW	slow mode
2'b01	SEL_FAST	fast mode
2'b10	SEL_LP	ultra low power mode
2'b11	SEL_ILLEGAL	Illegal Mode

1.3.315 LUT[0..3]_CR

LUT Config Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT0_CR: 0x40005848 LUT1_CR: 0x4000584A

LUT2_CR: 0x4000584C LUT3_CR: 0x4000584E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					q			

(no description)

Bits	Name	Description
3:0	q[3:0]	LUT function See Table 1-166.

Table 1-166. Bit field encoding: LUT_Q_ENUM

Value	Name	Description
4'h0	LUT_Q_0	FALSE (0)
4'h1	LUT_Q_A_AND_B	A AND B
4'h2	LUT_Q_A_AND_NOTB	A AND !B
4'h3	LUT_Q_A	A
4'h4	LUT_Q_NOTA_AND_B	!A AND B
4'h5	LUT_Q_B	B
4'h6	LUT_Q_A_XOR_B	A XOR B
4'h7	LUT_Q_A_OR_B	A OR B
4'h8	LUT_Q_A_NOR_B	A NOR B
4'h9	LUT_Q_A_XNOR_B	A XNOR B
4'ha	LUT_Q_NOTB	!B
4'hb	LUT_Q_A_OR_NOTB	A OR !B
4'hc	LUT_Q_NOTA	!A
4'hd	LUT_Q_NOTA_OR_B	!A OR B
4'he	LUT_Q_A_NAND_B	A NAND B
4'hf	LUT_Q_1	TRUE (1)

1.3.316 LUT[0..3]_MX

LUT Input Mux Config Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT0_MX: 0x40005849 LUT1_MX: 0x4000584B

LUT2_MX: 0x4000584D LUT3_MX: 0x4000584F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		NA:00		R/W:00	
HW Access	NA		R		NA		R	
Name			mx_b				mx_a	

(no description)

Bits	Name	Description
5:4	mx_b[1:0]	Mux Select for LUT Input B See Table 1-167.
1:0	mx_a[1:0]	Mux Select for LUT Input A See Table 1-167.

Table 1-167. Bit field encoding: LUT_MUX_ENUM

Value	Name	Description
2'h0	LUT_MUX_0	CMP0 output selected
2'h1	LUT_MUX_1	CMP1 output selected
2'h2	LUT_MUX_2	CMP2 output selected
2'h3	LUT_MUX_3	CMP3 output selected

1.3.317 ABUF[0..3]_CR

Analog Output Buffer Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF0_CR: 0x40005858

ABUF1_CR: 0x4000585A

ABUF2_CR: 0x4000585C

ABUF3_CR: 0x4000585E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							pwr_mode	

(no description)

Bits	Name	Description
1:0	pwr_mode[1:0]	TBD See Table 1-168.

Table 1-168. Bit field encoding: ABUF_PWR_MODE_ENUM

Value	Name	Description
2'h0	ABUF_PWR_MODE_FAST_DEFAULT	Fast (default)
2'h1	ABUF_PWR_MODE_SLOW	Slow
2'h2	ABUF_PWR_MODE_MEDIUM	Medium
2'h3	ABUF_PWR_MODE_FAST	Fast

1.3.318 ABUF[0..3]_RSVD

ABUF reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF0_RSVD: 0x40005859	ABUF1_RSVD: 0x4000585B
ABUF2_RSVD: 0x4000585D	ABUF3_RSVD: 0x4000585F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name								

(no description)

Bits	Name	Description
7:0	RSVD[7:0]	Reserved for ABUF expansion

1.3.319 LCDDAC_CR0

LCD Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_CR0: 0x40005868

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:00		NA:0	R/W:0	R/W:00	
HW Access	NA	R	R		NA	R	R	
Name		dft_en	dft_sel			amp_disabl e	bias_sel	

(no description)

Bits	Name	Description
6	dft_en	DFT enable signal
5:4	dft_sel[1:0]	Selects which of four internal voltages to pass through the dft_out pin
2	amp_disable	LCD DAC Amplifier disable. V0=Vpwr_hv. Only if contrast control is not wanted
1:0	bias_sel[1:0]	Selects the LCD bias/multiplex ratio

1.3.320 LCDDAC_CR1

LCDDAC Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_CR1: 0x40005869

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R						
Name		contrast_ctl						

(no description)

Bits	Name	Description
6:0	contrast_ctl[6:0]	LCD Contrast control setting.

1.3.321 LCDDRV_CR

LCD Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDRV_CR: 0x4000586A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						invert	lo2	sleep_mode

(no description)

Bits	Name	Description
2	invert	Invert LCD Display (invert display data on all pins configured as segments) See Table 1-169.
1	lo2	Enables / Disables the high-current mode of LoDrive mode of the LCD DRIVER block
0	sleep_mode	LCD Sleep Mode See Table 1-170.

Table 1-169. Bit field encoding: LCD_INVERT_ENUM

Value	Name	Description
1'b0	LCD_INVERT_DISABLED	Normal display
1'b1	LCD_INVERT_ENABLED	Inverted display

Table 1-170. Bit field encoding: LCD_SLEEP_MODE_ENUM

Value	Name	Description
1'b0	LCD_SLEEP_MODE_BLANK	When in a low power mode, set output buffer in LCD Drivers to ground. Blanks the LCD display.
1'b1	LCD_SLEEP_MODE_HIZ	When in a low power mode, set output buffer in LCD Drivers to hi impedance. This leaves intact the last image driven to the LCD display (charge will slowly leak off and the image will fade unless updated).

1.3.322 BG_CR0

Bandgap Precision Reference Control 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_CR0: 0x4000586C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:00	
HW Access	NA				R	R	R	
Name					bg_vda_res_en	bg_vda_swabusl0	cmp_mxvn	

(no description)

Bits	Name	Description
3	bg_vda_res_en	Bandgap VDA See Table 1-171.
2	bg_vda_swabusl0	Switch Control for VDA Bandgap output to abusl0 connection See Table 1-172.
1:0	cmp_mxvn[1:0]	Mux for comparator reference cmp1_vref See Table 1-173.

Table 1-171. Bit field encoding: BG_VDA_RES_EN_ENUM

Value	Name	Description
1'h0	BG_VDA_RES_EN_VDA	VDA
1'h1	BG_VDA_RES_EN_HALFVDA	VDA/2

Table 1-172. Bit field encoding: BG_VDA_SWABUSL0_ENUM

Value	Name	Description
1'h0	BG_VDA_SWABUSL0_DISCONNECT	not connected
1'h1	BG_VDA_SWABUSL0_CONNECT	Connect VDA Bandgap output to abusl0

Table 1-173. Bit field encoding: CMP_MXVN_ENUM

Value	Name	Description
2'h0	CMP_MXVN_NC	not connected
2'h1	CMP_MXVN_VDA	Bandgap VREF_VDA output selected
2'h2	CMP_MXVN_CMP1	Bandgap VREF_CMP1 output selected

1.3.323 BG_RSVD

Bandgap Precision Reference Reserved Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_RSVD: 0x4000586D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name								

(no description)

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.324 BG_DFT0

Bandgap Precision Reference DFT Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_DFT0: 0x4000586E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	NA			R	R	R	R	
Name				bg_dft_vsel	bg_dft_sel	bg_dft_en	bg_dft_isel	

(no description)

Bits	Name	Description
4	bg_dft_vsel	Mux for DFT to select either vgnd or the reference voltage See Table 1-177.
3	bg_dft_sel	BG_DFT_OUT mux selection - V_DFT (voltage) or I_DFT (current) See Table 1-176.
2	bg_dft_en	DFT enable for bandgap See Table 1-174.
1:0	bg_dft_isel[1:0]	Mux for DFT to select the current signals See Table 1-175.

Table 1-174. Bit field encoding: BG_DFT_EN_ENUM

Value	Name	Description
1'b0	BG_DFT_EN_DISABLE	disabled
1'b1	BG_DFT_EN_ENABLE	enabled

Table 1-175. Bit field encoding: BG_DFT_ISEL

Value	Name	Description
2'h0	BG_DFT_ISEL_IPTAT	iptat
2'h1	BG_DFT_ISEL_ICTAT	ictat
2'h2	BG_DFT_ISEL_INL	inl
2'h3	BG_DFT_ISEL_IBG10U	ibg10u

Table 1-176. Bit field encoding: BG_DFT_SEL_ENUM

Value	Name	Description
1'b0	BG_DFT_SEL_V	voltage
1'b1	BG_DFT_SEL_I	current

Table 1-177. Bit field encoding: BG_DFT_VSEL_ENUM

Value	Name	Description
1'b0	BG_DFT_VSEL_VOUT	VOUT
1'b1	BG_DFT_VSEL_VGND	vgnd

1.3.325 BG_DFT1

Bandgap Precision Reference DFT Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_DFT1: 0x4000586F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Name					bgrefs_dft_sel			

(no description)

Bits	Name	Description
3:0	bgrefs_dft_sel[3:0]	BGREFS_DFT_OUT (routed to DFT_MUX3) mux selection See Table 1-178.

Table 1-178. Bit field encoding: BGREFS_DFT_SEL_ENUM

Value	Name	Description
4'h0	BGREFS_DFT_SEL_VGND_0	vgnd
4'h1	BGREFS_DFT_SEL_VGND_1	vgnd
4'h2	BGREFS_DFT_SEL_VREF_BOOST	VREF_BOOST
4'h3	BGREFS_DFT_SEL_VREF_DAC	VREF_DAC
4'h4	BGREFS_DFT_SEL_VREF_LCD	VREF_LCD
4'h5	BGREFS_DFT_SEL_VREF_TSENSE	VREF_TSENSE
4'h6	BGREFS_DFT_SEL_VREF_POR	VREF_POR
4'h7	BGREFS_DFT_SEL_VREF_SC0	VREF_SC0
4'h8	BGREFS_DFT_SEL_VREF_IMO	VREF_IMO
4'h9	BGREFS_DFT_SEL_V0P256	v0p256
4'hA	BGREFS_DFT_SEL_V0P6	v0p6
4'hB	BGREFS_DFT_SEL_V0P7	v0p7
4'hC	BGREFS_DFT_SEL_V0P8	v0p8
4'hD	BGREFS_DFT_SEL_V0P9	v0p9
4'hE	BGREFS_DFT_SEL_V1P024	v1p024
4'hF	BGREFS_DFT_SEL_V1P2	v1p2

1.3.326 CAPSL_CFG0

Capsense Reference Driver Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSL_CFG0: 0x40005870

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:0	R/W:0
HW Access	R	R	R	R	R		R	R
Name	mxcmp	nc2	nc1	ch_cont	refsel		boost	out_en

(no description)

Bits	Name	Description
7	mxcmp	Reference Buffer channel to comparator vp mux select See Table 1-181.
6	nc2	Not Connected - Reserved
5	nc1	Not Connected - Reserved
4	ch_cont	Reference Buffer Channel Selection Control See Table 1-180.
3:2	refsel[1:0]	Reference Selection See Table 1-183.
1	boost	High power mode See Table 1-179.
0	out_en	Reference Buffer Output enable See Table 1-182.

Table 1-179. Bit field encoding: CS_BOOST_ENUM

Value	Name	Description
1'b0	CS_BOOST_NORMAL	Normal Drive (typically 10-60pF)
1'b1	CS_BOOST_HIGH	High Drive (typical load = 0.1 to 20nF)

Table 1-180. Bit field encoding: CS_MXCH_ENUM

Value	Name	Description
1'b0	CS_MXCH_AG	Ch1: Analog Global Path
1'b1	CS_MXCH_VS	Ch2: Vssa path

Table 1-181. Bit field encoding: CS_MXCMP_ENUM

Value	Name	Description
1'b0	CS_MXCMP_AG	ch1: Analog Global path connected to comparator vp mux
1'b1	CS_MXCMP_VS	ch2: Vssa path connected to comparator vp mux

Table 1-182. Bit field encoding: CS_OUT_EN_ENUM

Value	Name	Description
1'b0	CS_OUT_EN_HIZ	tristate

1.3.326 CAPSL_CFG0 (continued)

Table 1-182. Bit field encoding: CS_OUT_EN_ENUM

1'b1	CS_OUT_EN_ON	connected

Table 1-183. Bit field encoding: CS_REFSEL_ENUM

Value	Name	Description
2'h0	CS_REFSEL_1P024	1.024 V Bandgap Reference
2'h1	CS_REFSEL_1P2	1.2 V Bandgap Reference
2'h2	CS_REFSEL_TREFSEL1	dac2_vout (left CapSense); dac3_vout (right CapSense)
2'h3	CS_REFSEL_TREFSEL1_ALSO	dac2_vout (left CapSense); dac3_vout (right CapSense)

1.3.327 CAPSL_CFG1

Capsense IO Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSL_CFG1: 0x40005871

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							io_ctrl	

(no description)

Bits	Name	Description
1:0	io_ctrl[1:0]	Capsense Pull-up/Pull-down control See Table 1-184.

Table 1-184. Bit field encoding: CS_IO_CTRL

Value	Name	Description
2'h0	CS_IO_CTRL_DEFAULT	Neither pull-up or pull-down (default)
2'h1	CS_IO_CTRL_PU	Capsense Pull-up mode
2'h2	CS_IO_CTRL_NONE	Neither pull-up or pull-down
2'h3	CS_IO_CTRL_PD	Capsense Pull-down mode

1.3.328 CAPSR_CFG0

Capsense Reference Driver Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSR_CFG0: 0x40005872

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:0	R/W:0
HW Access	R	R	R	R	R		R	R
Name	mxcmp	nc2	nc1	ch_cont	refsel		boost	out_en

(no description)

Bits	Name	Description
7	mxcmp	Reference Buffer channel to comparator vp mux select See Table 1-187.
6	nc2	Not Connected - Reserved
5	nc1	Not Connected - Reserved
4	ch_cont	Reference Buffer Channel Selection Control See Table 1-186.
3:2	refsel[1:0]	Reference Selection See Table 1-189.
1	boost	High power mode See Table 1-185.
0	out_en	Reference Buffer Output enable See Table 1-188.

Table 1-185. Bit field encoding: CS_BOOST_ENUM

Value	Name	Description
1'b0	CS_BOOST_NORMAL	Normal Drive (typically 10-60pF)
1'b1	CS_BOOST_HIGH	High Drive (typical load = 0.1 to 20nF)

Table 1-186. Bit field encoding: CS_MXCH_ENUM

Value	Name	Description
1'b0	CS_MXCH_AG	Ch1: Analog Global Path
1'b1	CS_MXCH_VS	Ch2: Vssa path

Table 1-187. Bit field encoding: CS_MXCMP_ENUM

Value	Name	Description
1'b0	CS_MXCMP_AG	ch1: Analog Global path connected to comparator vp mux
1'b1	CS_MXCMP_VS	ch2: Vssa path connected to comparator vp mux

Table 1-188. Bit field encoding: CS_OUT_EN_ENUM

Value	Name	Description
1'b0	CS_OUT_EN_HIZ	tristate

1.3.328 CAPSR_CFG0 (continued)

Table 1-188. Bit field encoding: CS_OUT_EN_ENUM

1'b1	CS_OUT_EN_ON	connected

Table 1-189. Bit field encoding: CS_REFSEL_ENUM

Value	Name	Description
2'h0	CS_REFSEL_1P024	1.024 V Bandgap Reference
2'h1	CS_REFSEL_1P2	1.2 V Bandgap Reference
2'h2	CS_REFSEL_TREFSEL1	dac2_vout (left CapSense); dac3_vout (right CapSense)
2'h3	CS_REFSEL_TREFSEL1_ALSO	dac2_vout (left CapSense); dac3_vout (right CapSense)

1.3.329 CAPSR_CFG1

Capsense IO Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSR_CFG1: 0x40005873

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							io_ctrl	

(no description)

Bits	Name	Description
1:0	io_ctrl[1:0]	Capsense Pull-up/Pull-down control See Table 1-190.

Table 1-190. Bit field encoding: CS_IO_CTRL

Value	Name	Description
2'h0	CS_IO_CTRL_DEFAULT	Neither pull-up or pull-down (default)
2'h1	CS_IO_CTRL_PU	Capsense Pull-up mode
2'h2	CS_IO_CTRL_NONE	Neither pull-up or pull-down
2'h3	CS_IO_CTRL_PD	Capsense Pull-down mode

1.3.330 CAPS_DFT

Capsense DFT register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPS_DFT: 0x40005874

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Name							tcap	

(no description)

Bits	Name	Description
1:0	tcap[1:0]	Applies test capacitor to GPIO pad (P5.0) See Table 1-191.

Table 1-191. Bit field encoding: CS_TCAP_ENUM

Value	Name	Description
2'h0	CS_TCAP_0	cap disconnected
2'h1	CS_TCAP_1	2 pF
2'h2	CS_TCAP_2	10 pF
2'h3	CS_TCAP_3	12 pF (2+10)

1.3.331 PUMP_CR0

Pump Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PUMP_CR0: 0x40005876

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R	R	R	NA	R	R	R
Name		pump_amx_selclk	pump_amx_force	pump_amx_auto		pump_ag_selclk	pump_ag_force	pump_ag_auto

(no description)

Bits	Name	Description
6	pump_amx_selclk	Analog Mux Bus Pump Clock Selection See Table 1-193.
5	pump_amx_force	force pumping - if block enabled enable pump regardless of voltage state
4	pump_amx_auto	enable autopumping - if block enabled pump when low voltage detected
2	pump_ag_selclk	Analog Global Pump Clock Selection See Table 1-192.
1	pump_ag_force	force pumping - if block enabled enable pump regardless of voltage state
0	pump_ag_auto	enable autopumping - if block enabled pump when low voltage detected

Table 1-192. Bit field encoding: PUMP_AG_SELCLK_ENUM

Value	Name	Description
1'b0	PUMP_AG_SELCLK_EXTERNAL	External (DSI) clock selected
1'b1	PUMP_AG_SELCLK_INTERNAL	Pump internal clock selected

Table 1-193. Bit field encoding: PUMP_AMX_SELCLK_ENUM

Value	Name	Description
1'b0	PUMP_AMX_SELCLK_EXTERNAL	External (DSI) clock selected
1'b1	PUMP_AMX_SELCLK_INTERNAL	Pump internal clock selected

1.3.332 PUMP_CR1

Pump Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PUMP_CR1: 0x40005877

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R	R	R	NA	R	R	R
Name		npump_abuf_selclk	npump_abuf_force	npump_abuf_auto		npump_dsm_selclk	npump_dsm_force	npump_dsm_auto

(no description)

Bits	Name	Description
6	npump_abuf_selclk	Abuf Negative Pump Clock Selection See Table 1-194.
5	npump_abuf_force	force pumping - if block enabled enable pump regardless of voltage state
4	npump_abuf_auto	enable autopumping - if block enabled pump when low voltage detected
2	npump_dsm_selclk	DSM Negative Pump Clock Selection See Table 1-195.
1	npump_dsm_force	force pumping - if block enabled enable pump regardless of voltage state
0	npump_dsm_auto	enable autopumping - if block enabled pump when low voltage detected

Table 1-194. Bit field encoding: NPUMP_ABUF_SELCLK_ENUM

Value	Name	Description
1'b0	NPUMP_ABUF_SELCLK_EXTERNAL	External (DSI) clock selected
1'b1	NPUMP_ABUF_SELCLK_INTERNAL	Negative pump internal clock selected

Table 1-195. Bit field encoding: NPUMP_DSM_SELCLK_ENUM

Value	Name	Description
1'b0	NPUMP_DSM_SELCLK_EXTERNAL	External (DSI) clock selected
1'b1	NPUMP_DSM_SELCLK_INTERNAL	Negative pump internal clock selected

1.3.333 LPF0_CR0

Low Pass Filter Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF0_CR0: 0x40005878

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0	R/W:0	R/W:00	
HW Access	NA		R	R	NA	R	R	
Name			csel	rsel		swout	swin	

(no description)

Bits	Name	Description
5	csel	Capacitance Selection See Table 1-196.
4	rsel	Resistance Selection See Table 1-197.
2	swout	Output Switch Control See Table 1-199.
1:0	swin[1:0]	Input Switch Control See Table 1-198.

Table 1-196. Bit field encoding: LPF_CSEL_ENUM

Value	Name	Description
1'b0	LPF_CSEL_1X	5pF
1'b1	LPF_CSEL_2X	10pF

Table 1-197. Bit field encoding: LPF_RSEL_ENUM

Value	Name	Description
1'b0	LPF_RSEL_1X	1x; 7 units; 7*28300ohms = 198100ohm = 198.1kOhm
1'b1	LPF_RSEL_5X	5x; 35 units; 35*28300ohms = 990500ohm = 990.5kOhm

Table 1-198. Bit field encoding: LPF_SWIN_ENUM

Value	Name	Description
2'h0	LPF_SWIN_NC	inputs not connected
2'h1	LPF_SWIN_AG0	Analog Global 0 connected LPF0 (left): AGL0 LPF1 (right): AGR0
2'h2	LPF_SWIN_AMX	Analog Muxbus connected LPF0 (left): AMUXBUSL LPF1 (right): AMUXBUSR
2'h3	LPF_SWIN_BOTH	Both Analog Global and Analog Mux Bus connected (other end of the wire can be disconnected through the port control)

Table 1-199. Bit field encoding: LPF_SWOUT_ENUM

Value	Name	Description
1'h0	LPF_SWOUT_NC	LPF output not connected

1.3.333 LPF0_CR0 (continued)

Table 1-199. Bit field encoding: LPF_SWOUT_ENUM

1'h1	LPF_SWOUT_ABUS0	LPF output connected to Analog local bus 0 LPF0 (left): ABUSL0 LPF1 (right): ABUSR0

1.3.334 LPF0_RSVD

LPF Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF0_RSVD: 0x40005879

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name								

(no description)

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.335 LPF1_CR0

Low Pass Filter Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF1_CR0: 0x4000587A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0	R/W:0	R/W:00	
HW Access	NA		R	R	NA	R	R	
Name			csel	rsel		swout	swin	

(no description)

Bits	Name	Description
5	csel	Capacitance Selection See Table 1-200.
4	rsel	Resistance Selection See Table 1-201.
2	swout	Output Switch Control See Table 1-203.
1:0	swin[1:0]	Input Switch Control See Table 1-202.

Table 1-200. Bit field encoding: LPF_CSEL_ENUM

Value	Name	Description
1'b0	LPF_CSEL_1X	5pF
1'b1	LPF_CSEL_2X	10pF

Table 1-201. Bit field encoding: LPF_RSEL_ENUM

Value	Name	Description
1'b0	LPF_RSEL_1X	1x; 7 units; 7*28300ohms = 198100ohm = 198.1kOhm
1'b1	LPF_RSEL_5X	5x; 35 units; 35*28300ohms = 990500ohm = 990.5kOhm

Table 1-202. Bit field encoding: LPF_SWIN_ENUM

Value	Name	Description
2'h0	LPF_SWIN_NC	inputs not connected
2'h1	LPF_SWIN_AG0	Analog Global 0 connected LPF0 (left): AGL0 LPF1 (right): AGR0
2'h2	LPF_SWIN_AMX	Analog Muxbus connected LPF0 (left): AMUXBUSL LPF1 (right): AMUXBUSR
2'h3	LPF_SWIN_BOTH	Both Analog Global and Analog Mux Bus connected (other end of the wire can be disconnected through the port control)

Table 1-203. Bit field encoding: LPF_SWOUT_ENUM

Value	Name	Description
1'h0	LPF_SWOUT_NC	LPF output not connected

1.3.335 LPF1_CR0 (continued)

Table 1-203. Bit field encoding: LPF_SWOUT_ENUM

1'h1	LPF_SWOUT_ABUS0	LPF output connected to Analog local bus 0 LPF0 (left): ABUSL0 LPF1 (right): ABUSR0

1.3.336 LPF1_RSVD

LPF Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF1_RSVD: 0x4000587B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name								

(no description)

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.337 ANAIF_CFG_MISC_CR0

MISC Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ANAIF_CFG_MISC_CR0: 0x4000587C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								sw_pulldown_en

(no description)

Bits	Name	Description
0	sw_pulldown_en	Analog Switch pulldown enable See Table 1-204.

Table 1-204. Bit field encoding: SW_PULLDOWN_EN_ENUM

Value	Name	Description
1'b0	SW_PULLDOWN_EN_DISABLE	Disable switch pulldown
1'b1	SW_PULLDOWN_EN_ENABLE	Enable switch pulldown

1.3.338 TFAULT_CR0

Timing Fault Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TFAULT_CR0: 0x4000587E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						out_en	mx_src	en_clk

(no description)

Bits	Name	Description
2	out_en	Output Enable See Table 1-207.
1	mx_src	Source selection See Table 1-206.
0	en_clk	Clock Gater control See Table 1-205.

Table 1-205. Bit field encoding: TFAULT_EN_CLK_ENUM

Value	Name	Description
1'b0	TFAULT_EN_CLK_DISABLE	Gate clock
1'b1	TFAULT_EN_CLK_ENABLE	Enable clock

Table 1-206. Bit field encoding: TFAULT_MX_SRC_ENUM

Value	Name	Description
1'b0	TFAULT_MX_SRC_CLKDIV2	clk_bus/2
1'b1	TFAULT_MX_SRC_ONESHOT	oneshot

Table 1-207. Bit field encoding: TFAULT_OUT_EN_ENUM

Value	Name	Description
1'b0	TFAULT_OUT_EN_DISABLE	Output to reset disabled
1'b1	TFAULT_OUT_EN_ENABLE	Output to reset enabled

1.3.339 TFAULT_CR1

Timing Fault Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TFAULT_CR1: 0x4000587F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Name			coarse_dly_sel		fine_dly_sel			

(no description)

Bits	Name	Description
5:4	coarse_dly_sel[1:0]	Coarse delay selection See Table 1-208.
3:0	fine_dly_sel[3:0]	Fine delay selection See Table 1-209.

Table 1-208. Bit field encoding: TFAULT_COARSE_DLY_SEL_ENUM

Value	Name	Description
2'h0	TFAULT_COARSE_DLY_SEL_1	+1 coarse unit delay
2'h1	TFAULT_COARSE_DLY_SEL_2	+2 coarse unit delay
2'h2	TFAULT_COARSE_DLY_SEL_3	+3 coarse unit delay
2'h3	TFAULT_COARSE_DLY_SEL_4	+4 coarse unit delay

Table 1-209. Bit field encoding: TFAULT_FINE_DLY_SEL_ENUM

Value	Name	Description
4'h0	TFAULT_FINE_DLY_SEL_1	+1 fine unit delay
4'h1	TFAULT_FINE_DLY_SEL_2	+2 fine unit delay
4'h2	TFAULT_FINE_DLY_SEL_3	+3 fine unit delay
4'h3	TFAULT_FINE_DLY_SEL_4	+4 fine unit delay
4'h4	TFAULT_FINE_DLY_SEL_5	+5 fine unit delay
4'h5	TFAULT_FINE_DLY_SEL_6	+6 fine unit delay
4'h6	TFAULT_FINE_DLY_SEL_7	+7 fine unit delay
4'h7	TFAULT_FINE_DLY_SEL_8	+8 fine unit delay
4'h8	TFAULT_FINE_DLY_SEL_9	+9 fine unit delay

1.3.339 TFAULT_CR1 (continued)

Table 1-209. Bit field encoding: TFAULT_FINE_DLY_SEL_ENUM

4'h9	TFAULT_FINE_DLY_SEL_10	+10 fine unit delay
4'hA	TFAULT_FINE_DLY_SEL_11	+11 fine unit delay
4'hB	TFAULT_FINE_DLY_SEL_12	+12 fine unit delay
4'hC	TFAULT_FINE_DLY_SEL_13	+13 fine unit delay
4'hD	TFAULT_FINE_DLY_SEL_14	+14 fine unit delay
4'hE	TFAULT_FINE_DLY_SEL_15	+15 fine unit delay
4'hF	TFAULT_FINE_DLY_SEL_16	+16 fine unit delay

1.3.340 DSM[0..0]_CR0

Delta Sigma Modulator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR0: 0x40005880

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		R/W:00	
HW Access	NA				R		R	
Name					nonov		qlev	

(no description)

Bits	Name	Description
3:2	nonov[1:0]	Non overlap delay of clock phases See Table 1-210.
1:0	qlev[1:0]	Quantization Level choice for modulator See Table 1-211.

Table 1-210. Bit field encoding: NONOV_ENUM

Value	Name	Description
2'h0	NONOV_LOW	low (1.57ns, typ)
2'h1	NONOV_MEDIUM	medium (3.54ns, typ)
2'h2	NONOV_HIGH	high (6.47ns, typ)
2'h3	NONOV_VERYHIGH	very high (9.91ns, typ)

Table 1-211. Bit field encoding: QLEV_ENUM

Value	Name	Description
2'b00	QLEV_2	2 level quantization
2'b01	QLEV_3	3 level quantization
2'b10	QLEV_9	9 level quantization
2'b11	QLEV_9_ALSO	9 level quantization

1.3.341 DSM[0..0]_CR1

Delta Sigma Modulator Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR1: 0x40005881

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:00000				
HW Access	NA	R	R	R				
Name		dpmode	oden	odet_th				

(no description)

Bits	Name	Description
6	dpmode	Datapath mode See Table 1-212.
5	oden	Overload detect scheme enable
4:0	odet_th[4:0]	Overload detection threshold. If the number of continuous 1s or 0s coming out of quantizer exceeds this number overload detection flag is set

Table 1-212. Bit field encoding: DPMODE_ENUM

Value	Name	Description
1'h0	DPMODE_NORMAL	normal
1'h1	DPMODE_LOWOFFSET	low offset

1.3.342 DSM[0..0]_CR2

Delta Sigma Modulator Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR2: 0x40005882

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R	R	R	R	R	R		
Name	mx_reset	reset3_en	reset2_en	reset1_en	mod_chop_en	fchop		

(no description)

Bits	Name	Description
7	mx_reset	select DSM reset source See Table 1-214.
6	reset3_en	allow third stage integrating capacitance to be reset See Table 1-217.
5	reset2_en	allow second stage integrating capacitance to be reset See Table 1-216.
4	reset1_en	Allow first stage integrating capacitance to be reset See Table 1-215.
3	mod_chop_en	Enable Modulator Chopping
2:0	fchop[2:0]	Chopping Frequency Selection. The Fclock is samply frequency clock See Table 1-213.

Table 1-213. Bit field encoding: FCHOP_ENUM

Value	Name	Description
3'h0	FCHOP_DIV2	Fclock/2
3'h1	FCHOP_DIV4	Fclock/4
3'h2	FCHOP_DIV8	Fclock/8
3'h3	FCHOP_DIV16	Fclock/16
3'h4	FCHOP_DIV32	Fclock/32
3'h5	FCHOP_DIV64	Fclock/64
3'h6	FCHOP_DIV128	Fclock/128
3'h7	FCHOP_DIV256	Fclock/256

Table 1-214. Bit field encoding: MXSELRESET_ENUM

Value	Name	Description
1'b0	MXSELRESET_0	Select Decimator for reset source
1'b1	MXSELRESET_1	Select UDB for reset source

Table 1-215. Bit field encoding: RESET1_EN_ENUM

Value	Name	Description

1.3.342 DSM[0..0]_CR2 (continued)

Table 1-215. Bit field encoding: RESET1_EN_ENUM

1'b0	RESET1_EN_0	First stage integrating capacitance can be reset (use when in overload, to allow for first order operation)
1'b1	RESET1_EN_1	First stage integrating capacitance cannot be reset

Table 1-216. Bit field encoding: RESET2_EN_ENUM

Value	Name	Description
1'b0	RESET2_EN_DISABLE	second stage integrating capacitance cannot be reset (use when in overload, to allow for second order operation, assuming the reset1_en bit is also cleared
1'b1	RESET2_EN_ENABLE	second stage integrating capacitance can be reset

Table 1-217. Bit field encoding: RESET3_EN_ENUM

Value	Name	Description
1'b0	RESET3_EN_DISABLE	third stage integrating capacitance cannot be reset (use only for debug purposes)
1'b1	RESET3_EN_ENABLE	third stage integrating capacitance can be reset

1.3.343 DSM[0..0]_CR3

Delta Sigma Modulator Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR3: 0x40005883

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0000			
HW Access	R	R	R	R	R			
Name	sign	modbit	mx_dout	modbitin_en	mx_modbitin			

(no description)

Bits	Name	Description
7	sign	Invert sign of input See Table 1-222.
6	modbit	enable modbit; (NOTE: this bit should be set along with modbitin_en (bit4) to enable the modbit functionality) See Table 1-219.
5	mx_dout	Select DSM dout routed to UDB See Table 1-220.
4	modbitin_en	modbitin enable See Table 1-218.
3:0	mx_modbitin[3:0]	Select modbitin input See Table 1-221.

Table 1-218. Bit field encoding: MODBITIN_EN_ENUM

Value	Name	Description
1'b0	MODBITIN_EN_DISABLE	Do not allow modbit input to be mixed with modulator input
1'b1	MODBITIN_EN_ENABLE	Allow modbit input to be mixed with modulator input

Table 1-219. Bit field encoding: MODBIT_ENUM

Value	Name	Description
1'b0	MODBIT_DISABLE	modbit functionality disabled
1'b1	MODBIT_ENABLE	modbit functionality enabled

Table 1-220. Bit field encoding: MX_DOUT_ENUM

Value	Name	Description
1'b0	MX_DOUT_8BIT	Select reg OUT0=dout[7:0] (synced; w/o post processing)
1'b1	MX_DOUT_2SCOMP	Select reg OUT1={2'b0,ovdcause,ovdflag,dout2scomp} (synced; overload cause, overload flag, dout 2s complement

Table 1-221. Bit field encoding: MX_MODBITIN_ENUM

Value	Name	Description

1.3.343 DSM[0..0]_CR3 (continued)

Table 1-221. Bit field encoding: MX_MODBITIN_ENUM

4'h0	MX_MODBITIN_LUT0	lut0_out
4'h1	MX_MODBITIN_LUT1	lut1_out
4'h2	MX_MODBITIN_LUT2	lut2_out
4'h3	MX_MODBITIN_LUT3	lut3_out
4'h4	MX_MODBITIN_LUT4	lut4_out (doesn't exist on Leopard, tied to 0)
4'h5	MX_MODBITIN_LUT5	lut5_out (doesn't exist on Leopard, tied to 0)
4'h6	MX_MODBITIN_LUT6	lut6_out (doesn't exist on Leopard, tied to 0)
4'h7	MX_MODBITIN_LUT7	lut7_out (doesn't exist on Leopard, tied to 0)
4'h8	MX_MODBITIN_UDB	UDB

Table 1-222. Bit field encoding: SIGN_ENUM

Value	Name	Description
1'b0	SIGN_NONINVERT	keep original polarity for the input
1'b1	SIGN_INVERT	Invert sign of input (use when trying to chop once and then average the offset value out)

1.3.344 DSM[0..0]_CR4

Delta Sigma Modulator Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR4: 0x40005884

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Name	fcap1_en	fcap1						

(no description)

Bits	Name	Description
7	fcap1_en	Enable/Disable Capacitance path meant for DFT (Design for Testability) of the first integrator's integrating capacitance path See Table 1-224.
6:0	fcap1[6:0]	binary weighted first stage integrating capacitance See Table 1-223.

Table 1-223. Bit field encoding: FCAP1_ENUM

Value	Name	Description
7'b0	FCAP1_MIN	0 fF
7'b1111111	FCAP1_MAX	Max Value = 12.7 pF
7'b0000001	FCAP1_BIT0	fcap[0] set -> +100 fF
7'b0000010	FCAP1_BIT1	fcap[1] set -> +200 fF
7'b0000100	FCAP1_BIT2	fcap[2] set -> +400 fF
7'b0001000	FCAP1_BIT3	fcap[3] set -> +800 fF
7'b0010000	FCAP1_BIT4	fcap[4] set -> +1600 fF
7'b0100000	FCAP1_BIT5	fcap[5] set -> +3200 fF
7'b1000000	FCAP1_BIT6	fcap[6] set -> +6400 fF

Table 1-224. Bit field encoding: FCAP1_EN_ENUM

Value	Name	Description
1'h0	FCAP1_EN_DISABLE	Disable the DFT 100fF capacitance path
1'h1	FCAP1_EN_ENABLE	Enable the DFT 100fF capacitance path

1.3.345 DSM[0..0]_CR5

Delta Sigma Modulator Control Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR5: 0x40005885

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Name	ipcap1_en	ipcap1						

(no description)

Bits	Name	Description
7	ipcap1_en	Enable/Disable Capacitance path meant for DFT (Design for Testability) of the first integrator's input sampling path See Table 1-226.
6:0	ipcap1[6:0]	Binary weighted first stage integrating capacitance See Table 1-225.

Table 1-225. Bit field encoding: IPCAP1_ENUM

Value	Name	Description
7'b0	IPCAP1_MIN	0 fF
7'b1111111	IPCAP1_MAX	Max Value = 12.7 pF
7'b0000001	IPCAP1_BIT0	ipcap1[0] set -> +100 fF
7'b0000010	IPCAP1_BIT1	ipcap1[1] set -> +200 fF
7'b0000100	IPCAP1_BIT2	ipcap1[2] set -> +400 fF
7'b0001000	IPCAP1_BIT3	ipcap1[3] set -> +800 fF
7'b0010000	IPCAP1_BIT4	ipcap1[4] set -> +1600 fF
7'b0100000	IPCAP1_BIT5	ipcap1[5] set -> +3200 fF
7'b1000000	IPCAP1_BIT6	ipcap1[6] set -> +6400 fF

Table 1-226. Bit field encoding: IPCAP1_EN_ENUM

Value	Name	Description
1'h0	IPCAP1_EN_DISABLE	Disable the DFT 100fF capacitance path
1'h1	IPCAP1_EN_ENABLE	Enable the DFT 100fF capacitance path

1.3.346 DSM[0..0]_CR6

Delta Sigma Modulator Control Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR6: 0x40005886

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:000000					
HW Access	NA	R	R					
Name		daccap_en	daccap					

(no description)

Bits	Name	Description
6	daccap_en	Enable/Disable Capacitance path meant for DFT (Design for Testability) of the DAC Reference sampling path See Table 1-228.
5:0	daccap[5:0]	Binary weighted first stage DAC capacitance See Table 1-227.

Table 1-227. Bit field encoding: DACCAP_ENUM

Value	Name	Description
6'b000001	DACCAP_BIT0	daccap[0] set -> add 12*8= +96 fF
6'b000010	DACCAP_BIT1	daccap[1] set -> add 24*8= +192 fF
6'b000100	DACCAP_BIT2	daccap[2] set -> add 50*8= +400 fF
6'b001000	DACCAP_BIT3	daccap[3] set -> add 100*8= +800 fF
6'b010000	DACCAP_BIT4	daccap[4] set -> add 200*8= +1600 fF
6'b100000	DACCAP_BIT5	daccap[5] set -> add 400*8= +3200 fF

Table 1-228. Bit field encoding: DACCAP_EN_ENUM

Value	Name	Description
1'h0	DACCAP_EN_DISABLE	Disable the DFT 12fF capacitance path
1'h1	DACCAP_EN_ENABLE	Enable the DFT 12fF capacitance path

1.3.347 DSM[0..0]_CR7

Delta Sigma Modulator Control Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR7: 0x40005887

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R	R	R	R	R	R		
Name	fcap2_en	fcap3_en	ipcap1offset	fcap1offset	rescap_en	rescap		

(no description)

Bits	Name	Description
7	fcap2_en	Enable/Disable additional 50fF capacitance path in the second integrators integrating capacitance path See Table 1-230.
6	fcap3_en	Enable/Disable additonal capacitance path in the third integrator's integrating capacitance path See Table 1-231.
5	ipcap1offset	Offset capacitance for the input sampling capacitance in the first stage integrator See Table 1-232.
4	fcap1offset	Offset Capacitance for the integrating capacitance in the first stage integrator See Table 1-229.
3	rescap_en	Enable/Disable Capacitance path meant for DFT (Design for Testability) of the resonator path See Table 1-233.
2:0	rescap[2:0]	Resonator Capacitor Trim 12 fF to 100 fF with 12 fF step

Table 1-229. Bit field encoding: FCAP1OFFSET_ENUM

Value	Name	Description
1'b0	FCAP1OFFSET_0	Don't add offset capacitance
1'b1	FCAP1OFFSET_1	Add offset capacitance of 3.4 pF

Table 1-230. Bit field encoding: FCAP2_EN_ENUM

Value	Name	Description
1'h0	FCAP2_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	FCAP2_EN_ENABLE	Enable the additonal 50fF capacitance path

Table 1-231. Bit field encoding: FCAP3_EN_ENUM

Value	Name	Description
1'h0	FCAP3_EN_DISABLE	Disable the additonal 100fF capacitance path
1'h1	FCAP3_EN_ENABLE	Enable the 100fF capacitance path

Table 1-232. Bit field encoding: IPCAP1OFFSET_ENUM

Value	Name	Description
1'b0	IPCAP1OFFSET_0	Don't add offset capacitance
1'b1	IPCAP1OFFSET_1	Add offset capacitance of 4.8 pF

1.3.347 DSM[0..0]_CR7 (continued)

Table 1-233. Bit field encoding: RESCAP_EN_ENUM

Value	Name	Description
1'h0	RESCAP_EN_DISABLE	Disable the DFT 12fF capacitance path
1'h1	RESCAP_EN_ENABLE	Enable the DFT 12fF capacitance path

1.3.348 DSM[0..0]_CR8

Delta Sigma Modulator Control Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR8: 0x40005888

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0000			
HW Access	R	R			R			
Name	ipcap2_en	ipcap2			fcap2			

(no description)

Bits	Name	Description
7	ipcap2_en	Enable/Disable additional 50fF capacitance path in the second integrator's input sampling path See Table 1-236.
6:4	ipcap2[2:0]	The second integrator's input sampling capacitance (0-350fF, 50fF step) See Table 1-235.
3:0	fcap2[3:0]	The second stage integrating capacitance (0-750fF, 50fF step) See Table 1-234.

Table 1-234. Bit field encoding: FCAP2_ENUM

Value	Name	Description
4'h0	FCAP2_0FEMPTO	0fF
4'h1	FCAP2_50FEMPTO	50fF
4'h2	FCAP2_100FEMPTO	100fF
4'h3	FCAP2_150FEMPTO	150fF
4'h4	FCAP2_200FEMPTO	200fF
4'h5	FCAP2_250FEMPTO	250fF
4'h6	FCAP2_300FEMPTO	300fF
4'h7	FCAP2_350FEMPTO	350fF
4'h8	FCAP2_400FEMPTO	400fF
4'h9	FCAP2_450FEMPTO	450fF
4'ha	FCAP2_500FEMPTO	500fF
4'hb	FCAP2_550FEMPTO	550fF
4'hc	FCAP2_600FEMPTO	600fF
4'hd	FCAP2_650FEMPTO	650fF
4'he	FCAP2_700FEMPTO	700fF
4'hf	FCAP2_750FEMPTO	750fF

Table 1-235. Bit field encoding: IPCAP2_ENUM

Value	Name	Description
3'h0	IPCAP2_0FEMPTO	0fF
3'h1	IPCAP2_50FEMPTO	50fF
3'h2	IPCAP2_100FEMPTO	100fF
3'h3	IPCAP2_150FEMPTO	150fF
3'h4	IPCAP2_200FEMPTO	200fF
3'h5	IPCAP2_250FEMPTO	250fF
3'h6	IPCAP2_300FEMPTO	300fF

1.3.348 DSM[0..0]_CR8 (continued)

Table 1-235. Bit field encoding: IPCAP2_ENUM

3'h7	IPCAP2_350FEMPTO	350fF

Table 1-236. Bit field encoding: IPCAP2_EN_ENUM

Value	Name	Description
1'h0	IPCAP2_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	IPCAP2_EN_ENABLE	Enable the additonal 50fF capacitance path

1.3.349 DSM[0..0]_CR9

Delta Sigma Modulator Control Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR9: 0x40005889

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0000			
HW Access	R	R			R			
Name	ipcap3_en	ipcap3			fcap3			

(no description)

Bits	Name	Description
7	ipcap3_en	Enable/Disable additional 50fF capacitance path in the third integrator's input sampling path See Table 1-239.
6:4	ipcap3[2:0]	The third integrator's input sampling capacitance (0-350fF in 50fF step) See Table 1-238.
3:0	fcap3[3:0]	The third stage integrating capacitance (0-750fF, 50fF step) See Table 1-237.

Table 1-237. Bit field encoding: FCAP3_ENUM

Value	Name	Description
4'h0	FCAP3_0FEMPTO	0fF
4'h1	FCAP3_50FEMPTO	50fF
4'h2	FCAP3_100FEMPTO	100fF
4'h3	FCAP3_150FEMPTO	150fF
4'h4	FCAP3_200FEMPTO	200fF
4'h5	FCAP3_250FEMPTO	250fF
4'h6	FCAP3_300FEMPTO	300fF
4'h7	FCAP3_350FEMPTO	350fF
4'h8	FCAP3_400FEMPTO	400fF
4'h9	FCAP3_450FEMPTO	450fF
4'ha	FCAP3_500FEMPTO	500fF
4'hb	FCAP3_550FEMPTO	550fF
4'hc	FCAP3_600FEMPTO	600fF
4'hd	FCAP3_650FEMPTO	650fF
4'he	FCAP3_700FEMPTO	700fF
4'hf	FCAP3_750FEMPTO	750fF

Table 1-238. Bit field encoding: IPCAP3_ENUM

Value	Name	Description
3'h0	IPCAP3_0FEMPTO	0fF
3'h1	IPCAP3_50FEMPTO	50fF
3'h2	IPCAP3_100FEMPTO	100fF
3'h3	IPCAP3_150FEMPTO	150fF
3'h4	IPCAP3_200FEMPTO	200fF
3'h5	IPCAP3_250FEMPTO	250fF
3'h6	IPCAP3_300FEMPTO	300fF

1.3.349 DSM[0..0]_CR9 (continued)

Table 1-238. Bit field encoding: IPCAP3_ENUM

3'h7	IPCAP3_350FEMPTO	350fF

Table 1-239. Bit field encoding: IPCAP3_EN_ENUM

Value	Name	Description
1'h0	IPCAP3_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	IPCAP3_EN_ENABLE	Enable the additonal 50fF capacitance path

1.3.350 DSM[0..0]_CR10

Delta Sigma Modulator Control Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR10: 0x4000588A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0	R/W:000		
HW Access	R	R			R	R		
Name	sumcap1_en	sumcap1			sumcap2_en	sumcap2		

(no description)

Bits	Name	Description
7	sumcap1_en	Enabling/Disabling the the additional 50fF capacitance path that lies between first integrator output and summer input (feed-forward) path See Table 1-241.
6:4	sumcap1[2:0]	The summer capacitance that lies on the feed-forward path from the first integrator output (0fF to 350fF in 50fF step) See Table 1-240.
3	sumcap2_en	Enabling/Disabling the additional 50fF capacitance path that lies between the second integrator output and summer input (feed-forward) path See Table 1-243.
2:0	sumcap2[2:0]	The summer capacitance that lies on the feed-forward path from the second integrator output (0fF to 350fF in 50fF step See Table 1-242.

Table 1-240. Bit field encoding: SUMCAP1_ENUM

Value	Name	Description
3'h0	SUMCAP1_0FEMPTO	0fF
3'h1	SUMCAP1_50FEMPTO	50fF
3'h2	SUMCAP1_100FEMPTO	100fF
3'h3	SUMCAP1_150FEMPTO	150fF
3'h4	SUMCAP1_200FEMPTO	200fF
3'h5	SUMCAP1_250FEMPTO	250fF
3'h6	SUMCAP1_300FEMPTO	300fF
3'h7	SUMCAP1_350FEMPTO	350fF

Table 1-241. Bit field encoding: SUMCAP1_EN_ENUM

Value	Name	Description

1.3.350 DSM[0..0]_CR10 (continued)

Table 1-241. Bit field encoding: SUMCAP1_EN_ENUM

1'h0	SUMCAP1_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	SUMCAP1_EN_ENABLE	Enable the additonal 50fF capacitance path

Table 1-242. Bit field encoding: SUMCAP2_ENUM

Value	Name	Description
3'h0	SUMCAP2_0FEMPTO	0fF
3'h1	SUMCAP2_50FEMPTO	50fF
3'h2	SUMCAP2_100FEMPTO	100fF
3'h3	SUMCAP2_150FEMPTO	150fF
3'h4	SUMCAP2_200FEMPTO	200fF
3'h5	SUMCAP2_250FEMPTO	250fF
3'h6	SUMCAP2_300FEMPTO	300fF
3'h7	SUMCAP2_350FEMPTO	350fF

Table 1-243. Bit field encoding: SUMCAP2_EN_ENUM

Value	Name	Description
1'h0	SUMCAP2_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	SUMCAP2_EN_ENABLE	Enable the additonal 50fF capacitance path

1.3.351 DSM[0..0]_CR11

Delta Sigma Modulator Control Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR11: 0x4000588B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0000			
HW Access	R	R			R			
Name	sumcap3_en	sumcap3			sumcapfb			

(no description)

Bits	Name	Description
7	sumcap3_en	Enabling/Disabling the additional 50fF path that lies between the third integrator output and summer input (feed-forward) path See Table 1-245.
6:4	sumcap3[2:0]	The summer capacitance that lies on the feed-forward path from the third integrator output (0fF to 350fF in 50fF step See Table 1-244.
3:0	sumcapfb[3:0]	The summer feedback capacitance (0fF to 750F in 50fF step) See Table 1-246.

Table 1-244. Bit field encoding: SUMCAP3_ENUM

Value	Name	Description
3'h0	SUMCAP3_0FEMPTO	0fF
3'h1	SUMCAP3_50FEMPTO	50fF
3'h2	SUMCAP3_100FEMPTO	100fF
3'h3	SUMCAP3_150FEMPTO	150fF
3'h4	SUMCAP3_200FEMPTO	200fF
3'h5	SUMCAP3_250FEMPTO	250fF
3'h6	SUMCAP3_300FEMPTO	300fF
3'h7	SUMCAP3_350FEMPTO	350fF

Table 1-245. Bit field encoding: SUMCAP3_EN_ENUM

Value	Name	Description
1'h0	SUMCAP3_EN_DISABLE	Disable the additional 50fF capacitance path
1'h1	SUMCAP3_EN_ENABLE	Enable the additonal 50fF capacitance path

1.3.351 DSM[0..0]_CR11 (continued)

Table 1-246. Bit field encoding: SUMCAPFB_ENUM

Value	Name	Description
4'h0	SUMCAPFB_0FEMPTO	0fF
4'h1	SUMCAPFB_50FEMPTO	50fF
4'h2	SUMCAPFB_100FEMPTO	100fF
4'h3	SUMCAPFB_150FEMPTO	150fF
4'h4	SUMCAPFB_200FEMPTO	200fF
4'h5	SUMCAPFB_250FEMPTO	250fF
4'h6	SUMCAPFB_300FEMPTO	300fF
4'h7	SUMCAPFB_350FEMPTO	350fF
4'h8	SUMCAPFB_400FEMPTO	400fF
4'h9	SUMCAPFB_450FEMPTO	450fF
4'ha	SUMCAPFB_500FEMPTO	500fF
4'hb	SUMCAPFB_550FEMPTO	550fF
4'hc	SUMCAPFB_600FEMPTO	600fF
4'hd	SUMCAPFB_650FEMPTO	650fF
4'he	SUMCAPFB_700FEMPTO	700fF
4'hf	SUMCAPFB_750FEMPTO	750fF

1.3.352 DSM[0..0]_CR12

Delta Sigma Modulator Control Register 12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR12: 0x4000588C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:00000				
HW Access	NA	R	R	R				
Name		sumcapfb_en	sumcapin_en	sumcapin				

(no description)

Bits	Name	Description
6	sumcapfb_en	Enabling/Disabling the DFT path that lies on the feedback path of the active summer See Table 1-247.
5	sumcapin_en	Enabling/Disabling the DFT path that lies between input of the sigma delta modulator and the summer input. See Table 1-249.
4:0	sumcapin[4:0]	The summer capacitance that lies on the path where the input signal is summed (50fF to 1.6pF in 50fF step) See Table 1-248.

Table 1-247. Bit field encoding: SUMCAPFB_EN_ENUM

Value	Name	Description
1'h0	SUMCAPFB_EN_DISABLE	Disable the DFT 50fF capacitance path
1'h1	SUMCAPFB_EN_ENABLE	Enable the DFT 50fF capacitance path

Table 1-248. Bit field encoding: SUMCAPIN_ENUM

Value	Name	Description
5'h00	SUMCAPIN_0FEMPTO	0fF
5'h01	SUMCAPIN_50FEMPTO	50fF
5'h02	SUMCAPIN_100FEMPTO	100fF
5'h03	SUMCAPIN_150FEMPTO	150fF
5'h04	SUMCAPIN_200FEMPTO	200fF
5'h05	SUMCAPIN_250FEMPTO	250fF
5'h06	SUMCAPIN_300FEMPTO	300fF
5'h07	SUMCAPIN_350FEMPTO	350fF
5'h08	SUMCAPIN_400FEMPTO	400fF

1.3.352 DSM[0..0]_CR12 (continued)

Table 1-248. Bit field encoding: SUMCAPIN_ENUM

5'h09	SUMCAPIN_450FEMPTO	450fF
5'h0a	SUMCAPIN_500FEMPTO	500fF
5'h0b	SUMCAPIN_550FEMPTO	550fF
5'h0c	SUMCAPIN_600FEMPTO	600fF
5'h0d	SUMCAPIN_650FEMPTO	650fF
5'h0e	SUMCAPIN_700FEMPTO	700fF
5'h0f	SUMCAPIN_750FEMPTO	750fF
5'h10	SUMCAPIN_800FEMPTO	800fF
5'h11	SUMCAPIN_850FEMPTO	850fF
5'h12	SUMCAPIN_900FEMPTO	900fF
5'h13	SUMCAPIN_950FEMPTO	950fF
5'h14	SUMCAPIN_1000FEMPTO	1000fF
5'h15	SUMCAPIN_1050FEMPTO	1050fF
5'h16	SUMCAPIN_1100FEMPTO	1100fF
5'h17	SUMCAPIN_1150FEMPTO	1150fF
5'h18	SUMCAPIN_1200FEMPTO	1200fF
5'h19	SUMCAPIN_1250FEMPTO	1250fF
5'h1a	SUMCAPIN_1300FEMPTO	1300fF
5'h1b	SUMCAPIN_1350FEMPTO	1350fF
5'h1c	SUMCAPIN_1400FEMPTO	1400fF
5'h1d	SUMCAPIN_1450FEMPTO	1450fF
5'h1e	SUMCAPIN_1500FEMPTO	1500fF
5'h1f	SUMCAPIN_1550FEMPTO	1550fF

Table 1-249. Bit field encoding: SUMCAPIN_EN_ENUM

Value	Name	Description
1'h0	SUMCAPIN_EN_DISABLE	Disable the DFT 50fF capacitance path
1'h1	SUMCAPIN_EN_ENABLE	Enable the DFT 50fF capacitance path

1.3.353 DSM[0..0]_CR13

Delta Sigma Modulator Control Register 13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR13: 0x4000588D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name								

(no description)

Bits	Name	Description
7:0	RSVD[7:0]	Reserved for refsel expansion

1.3.354 DSM[0..0]_CR14

Delta Sigma Modulator Control Register 14

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR14: 0x4000588E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				NA:0	R/W:000		
HW Access	R				NA	R		
Name	opamp1_bw					power1		

(no description)

Bits	Name	Description
7:4	opamp1_bw[3:0]	First Stage Opamp Bandwidth Control (Risk Mitigation not for User control). Table gives value for Modulator input bw[3:0] See Table 1-250.
2:0	power1[2:0]	First Stage Opamp Power level control See Table 1-251.

Table 1-250. Bit field encoding: OPAMP1_BW_ENUM

Value	Name	Description
4'h0	OPAMP1_BW_0	(default) | 0000
4'h1	OPAMP1_BW_1	(used with 1.5X power option) | 0001
4'h2	OPAMP1_BW_2	(used with 2X power option) | 0011
4'h3	OPAMP1_BW_3	(used with 2.5X power option | 0111
4'h4	OPAMP1_BW_4	(higher BW, 1.25X current | 1000
4'h5	OPAMP1_BW_5	(lower noise) | 1001
4'h6	OPAMP1_BW_6	NA
4'h7	OPAMP1_BW_7	NA
4'h8	OPAMP1_BW_8	NA
4'h9	OPAMP1_BW_9	NA
4'ha	OPAMP1_BW_A	NA
4'hb	OPAMP1_BW_B	NA
4'hc	OPAMP1_BW_C	NA
4'hd	OPAMP1_BW_D	NA
4'he	OPAMP1_BW_E	NA
4'hf	OPAMP1_BW_F	NA

Table 1-251. Bit field encoding: POWER1_ENUM

Value	Name	Description
3'h0	POWER1_0	Low (44uA)
3'h1	POWER1_1	Medium (123uA)
3'h2	POWER1_2	High (492uA)
3'h3	POWER1_3	1.5X (750uA)
3'h4	POWER1_4	2X (1mA)
3'h5	POWER1_5	C/2 @ 3MSPS (277uA)
3'h6	POWER1_6	C/4 @ 3MSPS (185uA)
3'h7	POWER1_7	2.5X (1.5mA)

1.3.355 DSM[0..0]_CR15

Delta Sigma Modulator Control Register 15

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR15: 0x4000588F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		NA:0	R/W:000		
HW Access	NA		R		NA	R		
Name			power_comp			power2_3		

(no description)

Bits	Name	Description
5:4	power_comp[1:0]	The power control for the quantizer block See Table 1-253.
2:0	power2_3[2:0]	The power control for the second and third integrator stages See Table 1-252.

Table 1-252. Bit field encoding: POWER2_3_ENUM

Value	Name	Description
3'h0	POWER2_3_LOW	LOW (4uA)
3'h1	POWER2_3_MEDIUM	MEDIUM (17uA)
3'h2	POWER2_3_HIGH	HIGH (68uA)
3'h3	POWER2_3_1P5X	1.5X (100uA)
3'h4	POWER2_3_2X	2X (135uA)
3'h5	POWER2_3_HIGH_5	HIGH (68uA)
3'h6	POWER2_3_HIGH_6	HIGH (68uA)
3'h7	POWER2_3_HIGH_7	HIGH (68uA)

Table 1-253. Bit field encoding: POWER_COMP_ENUM

Value	Name	Description
2'h0	POWER_COMP_VERYLOW	very low (2.2uA)
2'h1	POWER_COMP_NORMAL	Normal (8.6uA)
2'h2	POWER_COMP_6MHZ	6MHz (17uA)
2'h3	POWER_COMP_12MHZ	12MHz (35uA)

1.3.356 DSM[0..0]_CR16

Delta Sigma Modulator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR16: 0x40005890

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			R/W:0	R/W:000		
HW Access	NA	R			R	R		
Name		power_sum			en_cp	cp_pwrctl		

(no description)

Bits	Name	Description
6:4	power_sum[2:0]	The power control for the summer block See Table 1-255.
3	en_cp	Enable charge pump
2:0	cp_pwrctl[2:0]	Charge Pump Power Control Modes See Table 1-254.

Table 1-254. Bit field encoding: CP_PWRCTL_ENUM

Value	Name	Description
3'h0	CP_PWRCTL_TURBO	Charge pump operating in Turbo Power (560uA) mode
3'h1	CP_PWRCTL_2X	Charge pump operating in 6MHz (300uA) mode
3'h2	CP_PWRCTL_HIGH	Charge pump operating in High power (170uA) mode
3'h3	CP_PWRCTL_MEDIUM	Charge pump operating in Medium power (70uA) mode
3'h4	CP_PWRCTL_LOW	Charge pump operating in Low Power (30uA) mode
3'h5	CP_PWRCTL_5	Reserved
3'h6	CP_PWRCTL_6	Reserved
3'h7	CP_PWRCTL_7	Reserved

Table 1-255. Bit field encoding: POWER_SUM_ENUM

Value	Name	Description
3'h0	POWER_SUM_LOW	LOW (4uA)
3'h1	POWER_SUM_MEDIUM	MEDIUM (17uA)
3'h2	POWER_SUM_HIGH	HIGH (68uA)
3'h3	POWER_SUM_1P5X	1.5X (100uA)
3'h4	POWER_SUM_2X	2X (135uA)
3'h5	POWER_SUM_HIGH_5	HIGH (68uA)
3'h6	POWER_SUM_HIGH_6	HIGH (68uA)
3'h7	POWER_SUM_HIGH_7	HIGH (68uA)

1.3.357 DSM[0..0]_CR17

Delta Sigma Modulator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR17: 0x40005891

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:0	R/W:0
HW Access	R		R		R		R	R
Name	pwr_ctrl_vref_inn		pwr_ctrl_vcm		pwr_ctrl_vref		en_buf_vcm	en_buf_vref

(no description)

Bits	Name	Description
7:6	pwr_ctrl_vref_inn[1:0]	Power control modes for REFBUF1 (the reference buffer that connects ADC reference to the negative input MUX of the channel) See Table 1-260.
5:4	pwr_ctrl_vcm[1:0]	Power Control for the Voltage Common Mode Buffer for the Sigma Delta ADC See Table 1-258.
3:2	pwr_ctrl_vref[1:0]	Power Control for the Voltage Reference Buffer for the Sigma Delta ADC See Table 1-259.
1	en_buf_vcm	Enable/Disable control for ADC (Internal)Reference Buffer See Table 1-256.
0	en_buf_vref	Enable/Disable control for ADC (Internal)Reference Buffer See Table 1-257.

Table 1-256. Bit field encoding: EN_BUF_VCM_ENUM

Value	Name	Description
1'h0	EN_BUF_VCM_0	The ADC Output common mode (VCM) voltage buffer is powered down
1'h1	EN_BUF_VCM_1	The ADC Output common mode (VCM) voltage buffer is NOT powered down

Table 1-257. Bit field encoding: EN_BUF_VREF_ENUM

Value	Name	Description
1'h0	EN_BUF_VREF_0	The Internal Reference Voltage Buffer is powered down
1'h1	EN_BUF_VREF_1	The Internal Reference Voltage Buffer is NOT powered down

Table 1-258. Bit field encoding: PWR_CTRL_VCM_ENUM

Value	Name	Description
2'h0	PWR_CTRL_VCM_0	VCM Buffer is operating in Low Power (TBD uA) mode
2'h1	PWR_CTRL_VCM_1	VCM Buffer is operating in Medium Power (TBD uA) mode
2'h2	PWR_CTRL_VCM_2	VCM Buffer is operating in High Power (TBD uA) mode
2'h3	PWR_CTRL_VCM_3	VCM Buffer is operating in Turbo Power (TBD uA)mode

Table 1-259. Bit field encoding: PWR_CTRL_VREF_ENUM

Value	Name	Description
2'h0	PWR_CTRL_VREF_0	VREF Buffer is operating in Low Power (TBD uA) mode

1.3.357 DSM[0..0]_CR17 (continued)

Table 1-259. Bit field encoding: PWR_CTRL_VREF_ENUM

2'h1	PWR_CTRL_VREF_1	VREF Buffer is operating in Medium Power (TBD uA) mode
2'h2	PWR_CTRL_VREF_2	VREF Buffer is operating in High Power (TBD uA) mode
2'h3	PWR_CTRL_VREF_3	VREF Buffer is operating in Turbo Power (TBD uA)mode

Table 1-260. Bit field encoding: PWR_CTRL_VREF_INN_ENUM

Value	Name	Description
2'h0	PWR_CTRL_VREF_INN_LOW	VREF Buffer (Input mux path) is operating in Low Power (26uA) mode
2'h1	PWR_CTRL_VREF_INN_MEDIUM	VREF Buffer (Input mux path) is operating in Medium Power (32uA) mode
2'h2	PWR_CTRL_VREF_INN_HIGH	VREF Buffer (Input mux path) is operating in High Power (118uA) mode
2'h3	PWR_CTRL_VREF_INN_TURBO	VREF Buffer (Input mux path) is operating in Turbo Power (232uA) mode

1.3.358 DSM[0..0]_REF0

Delta Sigma Modulator Reference Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF0: 0x40005892

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R		R	R	R	R		
Name	vcmsel		vcm_res_div_en	vref_res_div_en	en_buf_vref_inn	refmux		

(no description)

Bits	Name	Description
7:6	vcmsel[1:0]	Output common mode selection for modulator See Table 1-262.
5	vcm_res_div_en	If enabled it allows the resitor divided value of (Vpwra/2) to a selectable voltage for the VCM Mux
4	vref_res_div_en	If enabled it allows the resistor divided value of (Vda/4) to a selectable voltage for the RefMux
3	en_buf_vref_inn	Enable/Disable control for ADC (internal) REFBUF1 Buffer; This buffers the ADC reference before being sent to INN Mux; See IROS DSM chapter
2:0	refmux[2:0]	Mux control that allows for selecting one among the various available internal reference values See Table 1-261.

Table 1-261. Bit field encoding: REFMUX_ENUM

Value	Name	Description
3'h0	REFMUX_0	No Selection made for VCM
3'h1	REFMUX_1	Unbuffered VCM is also the VREF of the DSM
3'h2	REFMUX_2	Vda/4 is selected as the reference for the DSM (Vda is the external voltage supply)
3'h3	REFMUX_3	VDAC0 output is the reference for the DSM
3'h4	REFMUX_4	internal precision bandgap reference of 1.024 (typ) is selected as the DSM reference
3'h5	REFMUX_5	internal precision bandgap reference of 1.2V (typ) is selected as the DSM reference
3'h6	REFMUX_6	N/A
3'h7	REFMUX_7	N/A

Table 1-262. Bit field encoding: VCMSEL_ENUM

Value	Name	Description
2'h0	VCMSEL_0	No selection is made for VCM
2'h1	VCMSEL_1	0.8V from bandgap trim buffer is being selected as VCM (output common mode) for the DSM opamps
2'h2	VCMSEL_2	0.7V from bandgap trim buffer is being selected as VCM (output common mode)
2'h3	VCMSEL_3	Vpwra/2 is being selected as VCM (output common mode) for the DSM opamps; NOTE: bit DSMn.REF0[4], vcm_res_div_en, should be enabled to make this selection

1.3.359 DSM[0..0]_REF1

Delta Sigma Modulator Reference Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF1: 0x40005893

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name								

(no description)

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.360 DSM[0..0]_REF2

Delta Sigma Modulator Reference Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF2: 0x40005894

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	s7_en	s6_en	s5_en	s4_en	s3_en	s2_en	s1_en	s0_en

(no description)

Bits	Name	Description
7	s7_en	If Set, closes the S7 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
6	s6_en	If Set, closes the S6 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
5	s5_en	If Set, closes the S5 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
4	s4_en	If Set, closes the S4 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
3	s3_en	If Set, closes the S3 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
2	s2_en	If Set, closes the S2 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
1	s1_en	If Set, closes the S1 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
0	s0_en	If Set, closes the S0 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel

1.3.361 DSM[0..0]_REF3

Delta Sigma Modulator Reference Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF3: 0x40005895

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Name			s13_en	s12_en	s11_en	s10_en	s9_en	s8_en

(no description)

Bits	Name	Description
5	s13_en	If Set, closes the S13 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
4	s12_en	If Set, closes the S12 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
3	s11_en	If Set, closes the S11 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
2	s10_en	If Set, closes the S10 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
1	s9_en	If Set, closes the S9 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
0	s8_en	If Set, closes the S8 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel

1.3.362 DSM[0..0]_DEM0

Delta Sigma Modulator Dynamic Element Matching Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_DEM0: 0x40005896

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				demtest_src	adc_test_en	en_dem	en_scrambler1	en_scrambler0

(no description)

Bits	Name	Description
4	demtest_src	Select demtest source See Table 1-264.
3	adc_test_en	Enable/Disable All test modes in Sigma Delta Channel See Table 1-263.
2	en_dem	Enable DEM See Table 1-265.
1	en_scrambler1	Enable Scrambler 1 See Table 1-267.
0	en_scrambler0	Enable Scrambler 0 See Table 1-266.

Table 1-263. Bit field encoding: ADC_TEST_EN_ENUM

Value	Name	Description
1'h0	ADC_TEST_EN_0	Disable all test modes for the sigma delta channel
1'h1	ADC_TEST_EN_1	Enable all test modes for the sigma delta channel

Table 1-264. Bit field encoding: DEMTEST_SRC_ENUM

Value	Name	Description
1'h0	DEMTEST_SRC_REG	ANAIF register source selected
1'h1	DEMTEST_SRC_UDB	UDB generated source selected

Table 1-265. Bit field encoding: EN_DEM_ENUM

Value	Name	Description
1'h0	EN_DEM_DISABLE	Disable DEM
1'h1	EN_DEM_ENABLE	Enable DEM

Table 1-266. Bit field encoding: EN_SCRAMBLER0_ENUM

Value	Name	Description
1'h0	EN_SCRAMBLER0_DISABLE	Disable Scrambler 0

1.3.362 DSM[0..0]_DEM0 (continued)

Table 1-266. Bit field encoding: EN_SCRAMBLER0_ENUM

1'h1	EN_SCRAMBLER0_ENABLE	Enable Scrambler 0

Table 1-267. Bit field encoding: EN_SCRAMBLER1_ENUM

Value	Name	Description
1'h0	EN_SCRAMBLER1_DISABLE	Disable Scrambler 1
1'h1	EN_SCRAMBLER1_ENABLE	Enable Scrambler 1

1.3.363 DSM[0..0]_DEM1

Delta Sigma Modulator Dynamic Element Matching Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_DEM1: 0x40005897

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	demtest							

(no description)

Bits	Name	Description
7:0	demtest[7:0]	Register control for the DAC unit elements inside the first integrator. This can be used when bit DSM.DEM0[3], adc_test_en, is set. If the adc_test_en is not set the the control logic inside the modulator determines how the DAC unit elements are controlled. This is meant for static testing purposes

1.3.364 DSM[0..0]_TST0

Delta Sigma Modulator Test Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_TST0: 0x40005898

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			R/W:0000			
HW Access	NA	R			R			
Name		dig_test_sel			refsel_ctrl			

(no description)

Bits	Name	Description
6:4	dig_test_sel[2:0]	To test various digital outputs to digital muxes (for DFT)
3:0	refsel_ctrl[3:0]	This is the 4-bit encoded value which selects one among the 15 important DFT observable points inside the DSM. 4'h0 (0000) through 4'ha (1010) selects between various tap points in the quantizer resistor ladder. 4'hb (1011) through 4'he (1110) selects special points inside the DSM See Table 1-268.

Table 1-268. Bit field encoding: REFSEL_CTRL_ENUM

Value	Name	Description
4'h0	REFSEL_CTRL_0	(9/32)*Vref
4'h1	REFSEL_CTRL_1	(11/32)*Vref
4'h2	REFSEL_CTRL_2	(12/32)*Vref
4'h3	REFSEL_CTRL_3	(13/32)*Vref
4'h4	REFSEL_CTRL_4	(15/32)*Vref
4'h5	REFSEL_CTRL_5	(16/32)*Vref
4'h6	REFSEL_CTRL_6	(17/32)*Vref
4'h7	REFSEL_CTRL_7	(19/32)*Vref
4'h8	REFSEL_CTRL_8	(20/32)*Vref
4'h9	REFSEL_CTRL_9	(21/32)*Vref
4'ha	REFSEL_CTRL_10	(23/32)*Vref
4'hb	REFSEL_CTRL_11	Selects VICM (Input Common Mode) applied to DSM to be available at Ref_out DFT point
4'hc	REFSEL_CTRL_12	Selects Vb0 (2nd and 3rd integrator Opamp Bias Voltage) inside the DSM to Ref_out DFT point
4'hd	REFSEL_CTRL_13	Selects VRCM (Half of applied Reference) inside the DSM to Ref_out DFT point
4'he	REFSEL_CTRL_14	Selects vbias0_int, an internal bias point from inside the DSM to Ref_out DFT point
4'hf	REFSEL_CTRL_15	Not a valid selection

1.3.365 DSM[0..0]_TST1

Delta Sigma Modulator Test Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_TST1: 0x40005899

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name								

(no description)

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.366 DSM[0..0]_BUF0

Delta Sigma Modulator Buffer Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF0: 0x4000589A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						rail_rail_en	bypass_p	enable_p

(no description)

Bits	Name	Description
2	rail_rail_en	Selects Rail-to-Rail Mode See Table 1-271.
1	bypass_p	Remove positive half of the buffer from signal path See Table 1-269.
0	enable_p	Buffer Positive Half Enable See Table 1-270.

Table 1-269. Bit field encoding: BYPASS_P_ENUM

Value	Name	Description
1'b0	BYPASS_P_0	The buffer in the positive half remains on the signal path (Refer Fig 33-2)
1'b1	BYPASS_P_1	bypass the buffer on the positive half of the signal path (Refer Fig 33-2)

Table 1-270. Bit field encoding: ENABLE_P_ENUM

Value	Name	Description
1'b0	ENABLE_P_0	power down buffer in positive half
1'b1	ENABLE_P_1	enable positive half of buffer

Table 1-271. Bit field encoding: RAIL_RAIL_EN_ENUM

Value	Name	Description
1'h0	RAIL_RAIL_EN_DISABLE	Level shifted mode
1'h1	RAIL_RAIL_EN_ENABLE	Rail-to-Rail mode

1.3.367 DSM[0..0]_BUF1

Delta Sigma Modulator Buffer Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF1: 0x4000589B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		R/W:0	R/W:0
HW Access	NA				R		R	R
Name					gain		bypass_n	enable_n

(no description)

Bits	Name	Description
3:2	gain[1:0]	Gain settings of 1,2,4,8 are supported
1	bypass_n	Remove negative half of the buffer from signal path See Table 1-272.
0	enable_n	Buffer Negative Half Enable See Table 1-273.

Table 1-272. Bit field encoding: BYPASS_N_ENUM

Value	Name	Description
1'b0	BYPASS_N_DISABLE_BYPASS	The buffer in the negative half remains on the signal path (Refer Fig 33-2)
1'b1	BYPASS_N_ENABLE_BYPASS	bypass the buffer on the negative half of the signal path (Refer Fig 33-2)

Table 1-273. Bit field encoding: ENABLE_N_ENUM

Value	Name	Description
1'b0	ENABLE_N_0	power down buffer in negative half
1'b1	ENABLE_P_1	enable negative half of buffer

1.3.368 DSM[0..0]_BUF2

Delta Sigma Modulator Buffer Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF2: 0x4000589C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							add_extra_rc	lowpower_en

(no description)

Bits	Name	Description
1	add_extra_rc	If enabled an additional RC is included at the output of the buffer differentially, to lower noise at the expense of settling else normal settling. See s8hizbuf BROS for more information
0	lowpower_en	Enables the lower power mode of operation. See s8hizbuf BROS for more information See Table 1-274.

Table 1-274. Bit field encoding: LOWPOWER_EN_ENUM

Value	Name	Description
1'h0	LOWPOWER_EN_0	TBD
1'h1	LOWPOWER_EN_1	TBD

1.3.369 DSM[0..0]_BUF3

Delta Sigma Modulator Buffer Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF3: 0x4000589D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					buf_chop_en	buf_fchop		

(no description)

Bits	Name	Description
3	buf_chop_en	Enable/ Disable Chopping of the input buffer (TYPE A or B as selected in DSM_BUF0 register) See Table 1-275.
2:0	buf_fchop[2:0]	Input Buffer Chopping frequency control See Table 1-276.

Table 1-275. Bit field encoding: BUF_CHOP_EN_ENUM

Value	Name	Description
1'b0	BUF_CHOP_EN_0	Disable Chopping of the input buffer (type is as determined by
1'b1	BUF_CHOP_EN_1	Enable Chopping of the input buffer

Table 1-276. Bit field encoding: BUF_FCHOP_ENUM

Value	Name	Description
3'h0	BUF_FCHOP_0	chopping frequency is fs/2
3'h1	BUF_FCHOP_1	chopping frequency is fs/4
3'h2	BUF_FCHOP_2	chopping frequency is fs/8
3'h3	BUF_FCHOP_3	chopping frequency is fs/16
3'h4	BUF_FCHOP_4	chopping frequency is fs/32
3'h5	BUF_FCHOP_5	chopping frequency is fs/64
3'h6	BUF_FCHOP_6	chopping frequency is fs/128
3'h7	BUF_FCHOP_7	chopping frequency is fs/256

1.3.370 DSM[0..0]_MISC

Delta Sigma Modulator Miscellaneous register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_MISC: 0x4000589E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								sel_iclk_cp

(no description)

Bits	Name	Description
0	sel_iclk_cp	Select Charge Pump Internal Clock See Table 1-277.

Table 1-277. Bit field encoding: SEL_ICLK_CP_ENUM

Value	Name	Description
1'b0	SEL_ICLK_CP_EXTERNAL	External (DSI) Charge Pump Clock selected
1'b1	SEL_ICLK_CP_INTERNAL	Internal Charge Pump Clock selected

1.3.371 DSM[0..0]_RSVD1

Delta Sigma Modulator RSVD 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_RSVD1: 0x4000589F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name								

(no description)

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.372 SAR[0..1]_CSR0

SAR status and control register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR0: 0x40005900 SAR1_CSR0: 0x40005908

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:0	NA:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R		R	NA	R	R	R	R
Name	icont		reset_soft		hiz	mx_sof	sof_mode	sof_bit

(no description)

Bits	Name	Description
7:6	icont[1:0]	current control See Table 1-278.
5	reset_soft	firmware reset (not autoclearing) - can be used to stop a conversion See Table 1-281.
3	hiz	Sample time HiZ See Table 1-279.
2	mx_sof	Start-of-Frame (sof) source selection See Table 1-280.
1	sof_mode	Start-of-Frame (sof) mode See Table 1-283.
0	sof_bit	Start-of-Frame (sof) register source; enable conversion; (NOTE: autoclearing upon receipt of eof_sync when sof_mode==edge-sensitive) See Table 1-282.

Table 1-278. Bit field encoding: ICONT_ENUM

Value	Name	Description
2'h0	ICONT_0	Full current
2'h1	ICONT_1	1/2 of maximum current
2'h2	ICONT_2	1/3 of maximum current
2'h3	ICONT_3	1/4 of maximum current

Table 1-279. Bit field encoding: SAR_HIZ_ENUM

Value	Name	Description
1'b0	SAR_HIZ_RETAIN	Retain DAC value at beginning of sampling
1'b1	SAR_HIZ_CLEAR	Clear DAC value at beginning of sampling

Table 1-280. Bit field encoding: SAR_MX_SOF_ENUM

Value	Name	Description
1'b0	SAR_MX_SOF_BIT	source: sof_bit
1'b1	SAR_MX_SOF_UDB	source: UDB

1.3.372 SAR[0..1]_CSR0 (continued)

Table 1-281. Bit field encoding: SAR_RESET_SOFT_ENUM

Value	Name	Description
1'b0	SAR_RESET_SOFT_NOTACTIVE	reset soft not active
1'b1	SAR_RESET_SOFT_ACTIVE	reset soft active

Table 1-282. Bit field encoding: SAR_SOF_BIT_ENUM

Value	Name	Description
1'b0	SAR_SOF_BIT_0	disable conversion
1'b1	SAR_SOF_BIT_1	Enable conversion

Table 1-283. Bit field encoding: SAR_SOF_MODE_ENUM

Value	Name	Description
1'b0	SAR_SOF_MODE_LEVEL	level-sensitive sof source
1'b1	SAR_SOF_MODE_EDGE	edge-sensitive sof source

1.3.373 SAR[0..1]_CSR1

SAR status and control register 1

Reset: Reset Signals Listed Below

Register : Address

SAR0_CSR1: 0x40005901 SAR1_CSR1: 0x40005909

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000			R/W:0	R/W:0	R/W:0	R/W:0	RC:0
HW Access	R			R	R	R	R	R/W
Name	muxref			swvp_src	swvn_src	irq_mode	irq_mask	eof

(no description)

Bits	Name	Description
7:5	muxref[2:0]	SAR reference mux control See Table 1-287.
4	swvp_src	SAR positive input routing control source See Table 1-289.
3	swvn_src	SAR negative input routing control source See Table 1-288.
2	irq_mode	interrupt mode See Table 1-286.
1	irq_mask	Enable interrupt request from eof See Table 1-285.
0	eof	End Of Frame - clear-on-read sticky bit See Table 1-284.

Reset Table

resetsignal	field(s)
System reset for retention flops [reset_all_retention]	irq_mask, irq_mode, swvn_src, swvp_src, muxref[2:0]
Domain reset for non-retention flops [reset_all_nonretention]	eof

Table 1-284. Bit field encoding: SAR_EOF_ENUM

Value	Name	Description
1'b0	SAR_EOF_0	data_out NOT new
1'b1	SAR_EOF_1	End-of-Frame; data_out new

1.3.373 SAR[0..1]_CSR1 (continued)

Table 1-285. Bit field encoding: SAR_IRQ_MASK_ENUM

Value	Name	Description
1'b0	SAR_IRQ_MASK_DIS	disabled
1'b1	SAR_IRQ_MASK_EN	enabled

Table 1-286. Bit field encoding: SAR_IRQ_MODE_ENUM

Value	Name	Description
1'b0	SAR_IRQ_MODE_LEVEL	level
1'b1	SAR_IRQ_MODE_EDGE	edge

Table 1-287. Bit field encoding: SAR_MUXREF_ENUM

Value	Name	Description
3'h0	SAR_MUXREF_0	Not Used
3'h1	SAR_MUXREF_1	Not Used
3'h2	SAR_MUXREF_2	vda/2
3'h3	SAR_MUXREF_3	vdac
3'h4	SAR_MUXREF_4	BG vref1
3'h5	SAR_MUXREF_5	BG vref2
3'h6	SAR_MUXREF_6	Not Used
3'h7	SAR_MUXREF_7	Not Used

Table 1-288. Bit field encoding: SAR_SWVN_SRC_ENUM

Value	Name	Description
1'b0	SAR_SWVN_SRC_REG	ANAIF SAR routing registers
1'b1	SAR_SWVN_SRC_UDB	UDB

Table 1-289. Bit field encoding: SAR_SWVP_SRC_ENUM

Value	Name	Description
1'b0	SAR_SWVP_SRC_REG	ANAIF SAR routing registers
1'b1	SAR_SWVP_SRC_UDB	UDB

1.3.374 SAR[0..1]_CSR2

SAR status and control register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR2: 0x40005902 SAR1_CSR2: 0x4000590A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:000			R/W:000		
HW Access	R		R			R		
Name	resolution		sample_width_msb			sample_width_lsb		

(no description)

Bits	Name	Description
7:6	resolution[1:0]	8b,10b,12b resolution selection (data_out is LSBit aligned (right-shifted) according to the resolution mode) See Table 1-290.
5:3	sample_width_msb[2:0]	Sample time down counter start value MSB
2:0	sample_width_lsb[2:0]	Sample time down counter start value LSB See Table 1-291.

Table 1-290. Bit field encoding: SAR_RESOLUTION_ENUM

Value	Name	Description
2'h0	SAR_RESOLUTION_12BIT_DEFAULT	12-bit conversion = data_out[11:0]
2'h1	SAR_RESOLUTION_8BIT	8-bit conversion = data_out[7:0] (data_out[11:8] = 4'b0)
2'h2	SAR_RESOLUTION_10BIT	10-bit conversion = data_out[9:0] (data_out[11:10] = 2'b0)
2'h3	SAR_RESOLUTION_12BIT_ALSO	12-bit conversion = data_out[11:0]

Table 1-291. Bit field encoding: SAR_SAMPLE_WIDTH_LSB_ENUM

Value	Name	Description
3'h0	SAR_SAMPLE_WIDTH_LSB_MIN	minimum sample time: +1 clock cycle
3'h7	SAR_SAMPLE_WIDTH_LSB_MAX	maximum sample time: +8 clock cycles

1.3.375 SAR[0..1]_CSR3

SAR status and control register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR3: 0x40005903 SAR1_CSR3: 0x4000590B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:00		R/W:00		R/W:0	R/W:0
HW Access	R	R	R		R		R	R
Name	en_cp	en_resvda	pwr_ctrl_vcm		pwr_ctrl_vref		en_buf_vcm	en_buf_vref

(no description)

Bits	Name	Description
7	en_cp	Enable SAR charge pump See Table 1-294.
6	en_resvda	Enable SAR vda resister ladder divider See Table 1-295.
5:4	pwr_ctrl_vcm[1:0]	SAR VCM reference power control See Table 1-296.
3:2	pwr_ctrl_vref[1:0]	SAR VREF reference power control See Table 1-297.
1	en_buf_vcm	Enable SAR VCM reference buffer See Table 1-292.
0	en_buf_vref	Enable SAR VREF reference buffer See Table 1-293.

Table 1-292. Bit field encoding: SAR_EN_BUF_VCM_ENUM

Value	Name	Description
1'b0	SAR_EN_BUF_VCM_DIS	disabled
1'b1	SAR_EN_BUF_VCM_EN	enabled

Table 1-293. Bit field encoding: SAR_EN_BUF_VREF_ENUM

Value	Name	Description
1'b0	SAR_EN_BUF_VREF_DIS	disabled
1'b1	SAR_EN_BUF_VREF_EN	enabled

Table 1-294. Bit field encoding: SAR_EN_CP_ENUM

Value	Name	Description
1'b0	SAR_EN_CP_DIS	disabled
1'b1	SAR_EN_CP_EN	enabled

1.3.375 SAR[0..1]_CSR3 (continued)

Table 1-295. Bit field encoding: SAR_EN_RESVDA_ENUM

Value	Name	Description
1'b0	SAR_EN_RESVDA_DIS	disabled
1'b1	SAR_EN_RESVDA_EN	enabled

Table 1-296. Bit field encoding: SAR_PWR_CTRL_VCM_ENUM

Value	Name	Description
2'h0	SAR_PWR_CTRL_VCM_0	Not used
2'h1	SAR_PWR_CTRL_VCM_1	Not used
2'h2	SAR_PWR_CTRL_VCM_2	Not used
2'h3	SAR_PWR_CTRL_VCM_3	Not used

Table 1-297. Bit field encoding: SAR_PWR_CTRL_VREF_ENUM

Value	Name	Description
2'h0	SAR_PWR_CTRL_VREF_0	Max power
2'h1	SAR_PWR_CTRL_VREF_1	divide by 2
2'h2	SAR_PWR_CTRL_VREF_2	divide by 3
2'h3	SAR_PWR_CTRL_VREF_3	divide by 4

1.3.376 SAR[0..1]_CSR4

SAR status and control register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR4: 0x40005904 SAR1_CSR4: 0x4000590C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R	R	R	R	R	R	R
Name		dft_outc_2	dft_outc_1	dft_outc_0	dft_inc_3	dft_inc_2	dft_inc_1	dft_inc_0

(no description)

Bits	Name	Description
6	dft_outc_2	DFT observe point enable See Table 1-299.
5	dft_outc_1	DFT observe point enable See Table 1-299.
4	dft_outc_0	DFT observe point enable See Table 1-299.
3	dft_inc_3	DFT control point enable See Table 1-298.
2	dft_inc_2	DFT control point enable See Table 1-298.
1	dft_inc_1	DFT control point enable See Table 1-298.
0	dft_inc_0	DFT control point enable See Table 1-298.

Table 1-298. Bit field encoding: SAR_DFT_INC_ENUM

Value	Name	Description
1'b0	SAR_DFT_INC_DISABLED	dft control point disabled
1'b1	SAR_DFT_INC_ENABLED	dft control point enabled

Table 1-299. Bit field encoding: SAR_DFT_OUTC_ENUM

Value	Name	Description
1'b0	SAR_DFT_OUTC_DISABLED	dft observe point disabled
1'b1	SAR_DFT_OUTC_ENABLED	dft observe point enabled

1.3.377 SAR[0..1]_CSR5

SAR status and control register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR5: 0x40005905 SAR1_CSR5: 0x4000590D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0000			
HW Access	R	R	R	R	R			
Name	overrun_det_en	dly_inc	dcen	en_csel_dft	sel_csel_dft			

(no description)

Bits	Name	Description
7	overrun_det_en	Enable data overrun detection See Table 1-303.
6	dly_inc	Control for delay circuits See Table 1-301.
5	dcen	Short AC coupling in comparator for DFT See Table 1-300.
4	en_csel_dft	Enable for sel_csel_dft See Table 1-302.
3:0	sel_csel_dft[3:0]	To use this test value set en_csel_dft See Table 1-304.

Table 1-300. Bit field encoding: SAR_DCEN_ENUM

Value	Name	Description
1'b0	SAR_DCEN_0	not shorted
1'b1	SAR_DCEN_1	shorted

Table 1-301. Bit field encoding: SAR_DLY_INC_ENUM

Value	Name	Description
1'b0	SAR_DLY_INC_0	low delay
1'b1	SAR_DLY_INC_1	high delay

Table 1-302. Bit field encoding: SAR_EN_CSEL_DFT_ENUM

Value	Name	Description
1'b0	SAR_EN_CSEL_DFT_DISABLED	Normal mode
1'b1	SAR_EN_CSEL_DFT_ENABLED	Test mode; sel_csel_dft[3:0] used

Table 1-303. Bit field encoding: SAR_OVERRUN_DET_EN_ENUM

Value	Name	Description

1.3.377 SAR[0..1]_CSR5 (continued)

Table 1-303. Bit field encoding: SAR_OVERRUN_DET_EN_ENUM

1'b0	SAR_OVERRUN_DET_EN_DIS	disabled
1'b1	SAR_OVERRUN_DET_EN_EN	enabled

Table 1-304. Bit field encoding: SAR_SEL_CSEL_DFT_ENUM

Value	Name	Description
4'h0	SAR_SEL_CSEL_DFT_MIN	min csel_dft
4'hf	SAR_SEL_CSEL_DFT_MAX	max csel_dft

1.3.378 SAR[0..1]_CSR6

SAR status and control register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR6: 0x40005906 SAR1_CSR6: 0x4000590E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

(no description)

Bits	Name	Description
7	s_7	Enable reference switch See Table 1-305.
6	s_6	Enable reference switch See Table 1-305.
5	s_5	Enable reference switch See Table 1-305.
4	s_4	Enable reference switch See Table 1-305.
3	s_3	Enable reference switch See Table 1-305.
2	s_2	Enable reference switch See Table 1-305.
1	s_1	Enable reference switch See Table 1-305.
0	s_0	Enable reference switch See Table 1-305.

Table 1-305. Bit field encoding: SAR_REF_S_ENUM

Value	Name	Description
1'b0	SAR_REF_S_DIS	disabled
1'b1	SAR_REF_S_EN	enabled

1.3.379 SAR[0..1]_CSR7

SAR status and control register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CSR7: 0x40005907 SAR1_CSR7: 0x4000590F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Name			s_13	s_12	s_11	s_10	s_9	s_8

(no description)

Bits	Name	Description
5	s_13	Enable reference switch See Table 1-306.
4	s_12	Enable reference switch See Table 1-306.
3	s_11	Enable reference switch See Table 1-306.
2	s_10	Enable reference switch See Table 1-306.
1	s_9	Enable reference switch See Table 1-306.
0	s_8	Enable reference switch See Table 1-306.

Table 1-306. Bit field encoding: SAR_REF_S_ENUM

Value	Name	Description
1'b0	SAR_REF_S_DIS	disabled
1'b1	SAR_REF_S_EN	enabled

1.3.380 SC0_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW0: 0x40005A00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vn_ag7	vn_ag6	vn_ag5	vn_ag4	vn_ag3	vn_ag2	vn_ag1	vn_ag0

(no description)

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-307.
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-307.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-307.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-307.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-307.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-307.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-307.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-307.

Table 1-307. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.381 SC0_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW2: 0x40005A02

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:0	R/W:0
HW Access	NA				R	R	NA	R
Name					vn_abus3	vn_abus2		vn_abus0

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-308.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-308.
0	vn_abus0	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-308.

Table 1-308. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.382 SC0_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW3: 0x40005A03

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:000			R/W:0	R/W:0
HW Access	NA		R	NA			R	R
Name			vp_vref				vn_vref	vn_amx

(no description)

Bits	Name	Description
5	vp_vref	Connect positive voltage input to Voltage Reference See Table 1-310.
1	vn_vref	Connect negative voltage input to Voltage Reference See Table 1-310.
0	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-309.

Table 1-309. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-310. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.383 SC0_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW4: 0x40005A04

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		vp_ag6		vp_ag4		vp_ag2		vp_ag0

(no description)

Bits	Name	Description
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-311.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-311.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-311.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-311.

Table 1-311. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.384 SC0_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW6: 0x40005A06

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								vp_abus0

(no description)

Bits	Name	Description
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-312.

Table 1-312. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.385 SC0_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW7: 0x40005A07

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:00	
HW Access	NA					R/W	NA	
Name						vn_vo		

(no description)

Bits	Name	Description
2	vn_vo	Connect negative voltage input to output of opposite SC See Table 1-313.

Table 1-313. Bit field encoding: VN_VO_ENUM

Value	Name	Description
1'b0	VN_VO_0	not connected
1'b1	VN_VO_1	Connect VN to VO of opposite SC

1.3.386 SC0_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW8: 0x40005A08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Name	vo_ag7		vo_ag5		vo_ag3		vo_ag1	

(no description)

Bits	Name	Description
7	vo_ag7	Connect voltage output to analog global of same side (see field instance name) See Table 1-314.
5	vo_ag5	Connect voltage output to analog global of same side (see field instance name) See Table 1-314.
3	vo_ag3	Connect voltage output to analog global of same side (see field instance name) See Table 1-314.
1	vo_ag1	Connect voltage output to analog global of same side (see field instance name) See Table 1-314.

Table 1-314. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.387 SC0_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW10: 0x40005A0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Name					vo_abus3		vo_abus1	

(no description)

Bits	Name	Description
3	vo_abus3	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-315.
1	vo_abus1	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-315.

Table 1-315. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.388 SC0_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CLK: 0x40005A0B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA		R/W	R	R	R		
Name			dyn_cntl_en	bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
5	dyn_cntl_en	Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-318.
4	bypass_sync	Bypass Synchronization See Table 1-316.
3	clk_en	Clock gating control See Table 1-317.
2:0	mx_clk[2:0]	Clock Selection See Table 1-319.

Table 1-316. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-317. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-318. Bit field encoding: DYN_CNTL_ENUM

Value	Name	Description
1'b0	DYN_CNTL_DIS	Dynamic Control Disabled
1'b1	DYN_CNTL_EN	Dynamic Control Enabled

Table 1-319. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.389 SC0_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_BST: 0x40005A0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					bst_clk_en	mx_bst_clk		

(no description)

Bits	Name	Description
3	bst_clk_en	Clock gating control See Table 1-320.
2:0	mx_bst_clk[2:0]	Clock Selection See Table 1-321.

Table 1-320. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-321. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.390 SC1_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW0: 0x40005A10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vn_ag7	vn_ag6	vn_ag5	vn_ag4	vn_ag3	vn_ag2	vn_ag1	vn_ag0

(no description)

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-322.
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-322.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-322.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-322.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-322.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-322.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-322.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-322.

Table 1-322. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.391 SC1_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW2: 0x40005A12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:0	R/W:0
HW Access	NA				R	R	NA	R
Name					vn_abus3	vn_abus2		vn_abus0

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-323.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-323.
0	vn_abus0	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-323.

Table 1-323. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.392 SC1_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW3: 0x40005A13

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:000			R/W:0	R/W:0
HW Access	NA		R	NA			R	R
Name			vp_vref				vn_vref	vn_amx

(no description)

Bits	Name	Description
5	vp_vref	Connect positive voltage input to Voltage Reference See Table 1-325.
1	vn_vref	Connect negative voltage input to Voltage Reference See Table 1-325.
0	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-324.

Table 1-324. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-325. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.393 SC1_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW4: 0x40005A14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		vp_ag6		vp_ag4		vp_ag2		vp_ag0

(no description)

Bits	Name	Description
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-326.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-326.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-326.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-326.

Table 1-326. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.394 SC1_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW6: 0x40005A16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								vp_abus0

(no description)

Bits	Name	Description
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-327.

Table 1-327. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.395 SC1_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW7: 0x40005A17

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:00	
HW Access	NA					R/W	NA	
Name						vn_vo		

(no description)

Bits	Name	Description
2	vn_vo	Connect negative voltage input to output of opposite SC See Table 1-328.

Table 1-328. Bit field encoding: VN_VO_ENUM

Value	Name	Description
1'b0	VN_VO_0	not connected
1'b1	VN_VO_1	Connect VN to VO of opposite SC

1.3.396 SC1_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW8: 0x40005A18

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Name	vo_ag7		vo_ag5		vo_ag3		vo_ag1	

(no description)

Bits	Name	Description
7	vo_ag7	Connect voltage output to analog global of same side (see field instance name) See Table 1-329.
5	vo_ag5	Connect voltage output to analog global of same side (see field instance name) See Table 1-329.
3	vo_ag3	Connect voltage output to analog global of same side (see field instance name) See Table 1-329.
1	vo_ag1	Connect voltage output to analog global of same side (see field instance name) See Table 1-329.

Table 1-329. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.397 SC1_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW10: 0x40005A1A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Name					vo_abus3		vo_abus1	

(no description)

Bits	Name	Description
3	vo_abus3	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-330.
1	vo_abus1	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-330.

Table 1-330. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.398 SC1_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_CLK: 0x40005A1B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA		R/W	R	R	R		
Name			dyn_cntl_en	bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
5	dyn_cntl_en	Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-333.
4	bypass_sync	Bypass Synchronization See Table 1-331.
3	clk_en	Clock gating control See Table 1-332.
2:0	mx_clk[2:0]	Clock Selection See Table 1-334.

Table 1-331. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-332. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-333. Bit field encoding: DYN_CNTL_ENUM

Value	Name	Description
1'b0	DYN_CNTL_DIS	Dynamic Control Disabled
1'b1	DYN_CNTL_EN	Dynamic Control Enabled

Table 1-334. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.399 SC1_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_BST: 0x40005A1C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					bst_clk_en	mx_bst_clk		

(no description)

Bits	Name	Description
3	bst_clk_en	Clock gating control See Table 1-335.
2:0	mx_bst_clk[2:0]	Clock Selection See Table 1-336.

Table 1-335. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-336. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.400 SC2_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW0: 0x40005A20

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vn_ag7	vn_ag6	vn_ag5	vn_ag4	vn_ag3	vn_ag2	vn_ag1	vn_ag0

(no description)

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-337.
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-337.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-337.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-337.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-337.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-337.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-337.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-337.

Table 1-337. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.401 SC2_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW2: 0x40005A22

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	NA:0
HW Access	NA				R	R	R	NA
Name					vn_abus3	vn_abus2	vn_abus1	

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-338.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-338.
1	vn_abus1	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-338.

Table 1-338. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.402 SC2_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW3: 0x40005A23

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:000			R/W:0	R/W:0
HW Access	NA		R	NA			R	R
Name			vp_vref				vn_vref	vn_amx

(no description)

Bits	Name	Description
5	vp_vref	Connect positive voltage input to Voltage Reference See Table 1-340.
1	vn_vref	Connect negative voltage input to Voltage Reference See Table 1-340.
0	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-339.

Table 1-339. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-340. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.403 SC2_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW4: 0x40005A24

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Name	vp_ag7		vp_ag5		vp_ag3		vp_ag1	

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-341.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-341.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-341.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-341.

Table 1-341. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.404 SC2_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW6: 0x40005A26

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	NA:0
HW Access	NA						R	NA
Name							vp_abus1	

(no description)

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-342.

Table 1-342. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.405 SC2_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW7: 0x40005A27

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:00	
HW Access	NA					R/W	NA	
Name						vn_vo		

(no description)

Bits	Name	Description
2	vn_vo	Connect negative voltage input to output of opposite SC See Table 1-343.

Table 1-343. Bit field encoding: VN_VO_ENUM

Value	Name	Description
1'b0	VN_VO_0	not connected
1'b1	VN_VO_1	Connect VN to VO of opposite SC

1.3.406 SC2_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW8: 0x40005A28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		vo_ag6		vo_ag4		vo_ag2		vo_ag0

(no description)

Bits	Name	Description
6	vo_ag6	Connect voltage output to analog global of same side (see field instance name) See Table 1-344.
4	vo_ag4	Connect voltage output to analog global of same side (see field instance name) See Table 1-344.
2	vo_ag2	Connect voltage output to analog global of same side (see field instance name) See Table 1-344.
0	vo_ag0	Connect voltage output to analog global of same side (see field instance name) See Table 1-344.

Table 1-344. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.407 SC2_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW10: 0x40005A2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Name						vo_abus2		vo_abus0

(no description)

Bits	Name	Description
2	vo_abus2	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-345.
0	vo_abus0	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-345.

Table 1-345. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.408 SC2_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_CLK: 0x40005A2B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA		R/W	R	R	R		
Name			dyn_cntl_en	bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
5	dyn_cntl_en	Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-348.
4	bypass_sync	Bypass Synchronization See Table 1-346.
3	clk_en	Clock gating control See Table 1-347.
2:0	mx_clk[2:0]	Clock Selection See Table 1-349.

Table 1-346. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-347. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-348. Bit field encoding: DYN_CNTL_ENUM

Value	Name	Description
1'b0	DYN_CNTL_DIS	Dynamic Control Disabled
1'b1	DYN_CNTL_EN	Dynamic Control Enabled

Table 1-349. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.409 SC2_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_BST: 0x40005A2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					bst_clk_en	mx_bst_clk		

(no description)

Bits	Name	Description
3	bst_clk_en	Clock gating control See Table 1-350.
2:0	mx_bst_clk[2:0]	Clock Selection See Table 1-351.

Table 1-350. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-351. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.410 SC3_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW0: 0x40005A30

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vn_ag7	vn_ag6	vn_ag5	vn_ag4	vn_ag3	vn_ag2	vn_ag1	vn_ag0

(no description)

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-352.
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-352.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-352.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-352.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-352.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-352.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-352.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-352.

Table 1-352. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.411 SC3_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW2: 0x40005A32

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	NA:0
HW Access	NA				R	R	R	NA
Name					vn_abus3	vn_abus2	vn_abus1	

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-353.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-353.
1	vn_abus1	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-353.

Table 1-353. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.412 SC3_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW3: 0x40005A33

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:000			R/W:0	R/W:0
HW Access	NA		R	NA			R	R
Name			vp_vref				vn_vref	vn_amx

(no description)

Bits	Name	Description
5	vp_vref	Connect positive voltage input to Voltage Reference See Table 1-355.
1	vn_vref	Connect negative voltage input to Voltage Reference See Table 1-355.
0	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-354.

Table 1-354. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-355. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.413 SC3_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW4: 0x40005A34

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Name	vp_ag7		vp_ag5		vp_ag3		vp_ag1	

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-356.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-356.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-356.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-356.

Table 1-356. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.414 SC3_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW6: 0x40005A36

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	NA:0
HW Access	NA						R	NA
Name							vp_abus1	

(no description)

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-357.

Table 1-357. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.415 SC3_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW7: 0x40005A37

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:00	
HW Access	NA					R/W	NA	
Name						vn_vo		

(no description)

Bits	Name	Description
2	vn_vo	Connect negative voltage input to output of opposite SC See Table 1-358.

Table 1-358. Bit field encoding: VN_VO_ENUM

Value	Name	Description
1'b0	VN_VO_0	not connected
1'b1	VN_VO_1	Connect VN to VO of opposite SC

1.3.416 SC3_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW8: 0x40005A38

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		vo_ag6		vo_ag4		vo_ag2		vo_ag0

(no description)

Bits	Name	Description
6	vo_ag6	Connect voltage output to analog global of same side (see field instance name) See Table 1-359.
4	vo_ag4	Connect voltage output to analog global of same side (see field instance name) See Table 1-359.
2	vo_ag2	Connect voltage output to analog global of same side (see field instance name) See Table 1-359.
0	vo_ag0	Connect voltage output to analog global of same side (see field instance name) See Table 1-359.

Table 1-359. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.417 SC3_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW10: 0x40005A3A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Name						vo_abus2		vo_abus0

(no description)

Bits	Name	Description
2	vo_abus2	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-360.
0	vo_abus0	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-360.

Table 1-360. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.418 SC3_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_CLK: 0x40005A3B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA		R/W	R	R	R		
Name			dyn_cntl_en	bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
5	dyn_cntl_en	Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-363.
4	bypass_sync	Bypass Synchronization See Table 1-361.
3	clk_en	Clock gating control See Table 1-362.
2:0	mx_clk[2:0]	Clock Selection See Table 1-364.

Table 1-361. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-362. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-363. Bit field encoding: DYN_CNTL_ENUM

Value	Name	Description
1'b0	DYN_CNTL_DIS	Dynamic Control Disabled
1'b1	DYN_CNTL_EN	Dynamic Control Enabled

Table 1-364. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.419 SC3_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_BST: 0x40005A3C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					bst_clk_en	mx_bst_clk		

(no description)

Bits	Name	Description
3	bst_clk_en	Clock gating control See Table 1-365.
2:0	mx_bst_clk[2:0]	Clock Selection See Table 1-366.

Table 1-365. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-366. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.420 DAC0_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW0: 0x40005A80

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							v_ag1	v_ag0

(no description)

Bits	Name	Description
1	v_ag1	Connect voltage output to analog global of same side (see field instance name) See Table 1-367.
0	v_ag0	Connect voltage output to analog global of same side (see field instance name) See Table 1-367.

Table 1-367. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.421 DAC0_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW2: 0x40005A82

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Name					v_abus3		v_abus1	

(no description)

Bits	Name	Description
3	v_abus3	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-368.
1	v_abus1	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-368.

Table 1-368. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.422 DAC0_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW3: 0x40005A83

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	NA:000			R/W:0
HW Access	R	NA		R	NA			R
Name	iout			i_amx				v_amx

(no description)

Bits	Name	Description
7	iout	Connect current output to pad See Table 1-370.
4	i_amx	Connect current output to Analog Mux Bus See Table 1-369.
0	v_amx	Connect voltage output to Analog Mux Bus See Table 1-369.

Table 1-369. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-370. Bit field encoding: IOUT_ENUM

Value	Name	Description
1'b0	IOUT_NC	not connected
1'b1	IOUT_CONNECT	Connect to pad (see routing diagram)

1.3.423 DAC0_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW4: 0x40005A84

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							i_ag1	i_ag0

(no description)

Bits	Name	Description
1	i_ag1	Connect current output to analog global of same side (see field instance name) See Table 1-371.
0	i_ag0	Connect current output to analog global of same side (see field instance name) See Table 1-371.

Table 1-371. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.424 DAC0_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_STROBE: 0x40005A87

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					strobe_en	mx_strobe		

(no description)

Bits	Name	Description
3	strobe_en	Strobe gating control (See mx_strobe==3'h0) See Table 1-373.
2:0	mx_strobe[2:0]	Strobe source selection See Table 1-372.

Table 1-372. Bit field encoding: MX_STROBE_ENUM

Value	Name	Description
3'h0	MX_STROBE_BUSWRITE	Select bus write strobe source (Enable gater regardless of strobe_en setting)
3'h1	MX_STROBE_UDB_SRC	Select UDB strobe source
3'h2	MX_STROBE_NC_2	NC
3'h3	MX_STROBE_NC_3	NC
3'h4	MX_STROBE_CLK_A0_DIG	Select clk_a0_dig
3'h5	MX_STROBE_CLK_A1_DIG	Select clk_a1_dig
3'h6	MX_STROBE_CLK_A2_DIG	Select clk_a2_dig
3'h7	MX_STROBE_CLK_A3_DIG	Select clk_a3_dig

Table 1-373. Bit field encoding: STROBE_EN_ENUM

Value	Name	Description
1'b0	STROBE_EN_0	disable strobe
1'b1	STROBE_EN_1	enable strobe

1.3.425 DAC1_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW0: 0x40005A88

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							v_ag1	v_ag0

(no description)

Bits	Name	Description
1	v_ag1	Connect voltage output to analog global of same side (see field instance name) See Table 1-374.
0	v_ag0	Connect voltage output to analog global of same side (see field instance name) See Table 1-374.

Table 1-374. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.426 DAC1_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW2: 0x40005A8A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Name					v_abus3		v_abus1	

(no description)

Bits	Name	Description
3	v_abus3	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-375.
1	v_abus1	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-375.

Table 1-375. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.427 DAC1_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW3: 0x40005A8B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	NA:000			R/W:0
HW Access	R	NA		R	NA			R
Name	iout			i_amx				v_amx

(no description)

Bits	Name	Description
7	iout	Connect current output to pad See Table 1-377.
4	i_amx	Connect current output to Analog Mux Bus See Table 1-376.
0	v_amx	Connect voltage output to Analog Mux Bus See Table 1-376.

Table 1-376. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-377. Bit field encoding: IOUT_ENUM

Value	Name	Description
1'b0	IOUT_NC	not connected
1'b1	IOUT_CONNECT	Connect to pad (see routing diagram)

1.3.428 DAC1_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW4: 0x40005A8C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							i_ag1	i_ag0

(no description)

Bits	Name	Description
1	i_ag1	Connect current output to analog global of same side (see field instance name) See Table 1-378.
0	i_ag0	Connect current output to analog global of same side (see field instance name) See Table 1-378.

Table 1-378. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.429 DAC1_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_STROBE: 0x40005A8F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					strobe_en	mx_strobe		

(no description)

Bits	Name	Description
3	strobe_en	Strobe gating control (See mx_strobe==3'h0) See Table 1-380.
2:0	mx_strobe[2:0]	Strobe source selection See Table 1-379.

Table 1-379. Bit field encoding: MX_STROBE_ENUM

Value	Name	Description
3'h0	MX_STROBE_BUSWRITE	Select bus write strobe source (Enable gater regardless of strobe_en setting)
3'h1	MX_STROBE_UDB_SRC	Select UDB strobe source
3'h2	MX_STROBE_NC_2	NC
3'h3	MX_STROBE_NC_3	NC
3'h4	MX_STROBE_CLK_A0_DIG	Select clk_a0_dig
3'h5	MX_STROBE_CLK_A1_DIG	Select clk_a1_dig
3'h6	MX_STROBE_CLK_A2_DIG	Select clk_a2_dig
3'h7	MX_STROBE_CLK_A3_DIG	Select clk_a3_dig

Table 1-380. Bit field encoding: STROBE_EN_ENUM

Value	Name	Description
1'b0	STROBE_EN_0	disable strobe
1'b1	STROBE_EN_1	enable strobe

1.3.430 DAC2_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW0: 0x40005A90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Name			v_ag5	v_ag4				

(no description)

Bits	Name	Description
5	v_ag5	Connect voltage output to analog global of same side (see field instance name) See Table 1-381.
4	v_ag4	Connect voltage output to analog global of same side (see field instance name) See Table 1-381.

Table 1-381. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.431 DAC2_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW2: 0x40005A92

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Name						v_abus2		v_abus0

(no description)

Bits	Name	Description
2	v_abus2	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-382.
0	v_abus0	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-382.

Table 1-382. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.432 DAC2_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW3: 0x40005A93

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	NA:000			R/W:0
HW Access	R	NA		R	NA			R
Name	iout			i_amx				v_amx

(no description)

Bits	Name	Description
7	iout	Connect current output to pad See Table 1-384.
4	i_amx	Connect current output to Analog Mux Bus See Table 1-383.
0	v_amx	Connect voltage output to Analog Mux Bus See Table 1-383.

Table 1-383. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-384. Bit field encoding: IOUT_ENUM

Value	Name	Description
1'b0	IOUT_NC	not connected
1'b1	IOUT_CONNECT	Connect to pad (see routing diagram)

1.3.433 DAC2_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW4: 0x40005A94

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Name			i_ag5	i_ag4				

(no description)

Bits	Name	Description
5	i_ag5	Connect current output to analog global of same side (see field instance name) See Table 1-385.
4	i_ag4	Connect current output to analog global of same side (see field instance name) See Table 1-385.

Table 1-385. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.434 DAC2_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_STROBE: 0x40005A97

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					strobe_en	mx_strobe		

(no description)

Bits	Name	Description
3	strobe_en	Strobe gating control (See mx_strobe==3'h0) See Table 1-387.
2:0	mx_strobe[2:0]	Strobe source selection See Table 1-386.

Table 1-386. Bit field encoding: MX_STROBE_ENUM

Value	Name	Description
3'h0	MX_STROBE_BUSWRITE	Select bus write strobe source (Enable gater regardless of strobe_en setting)
3'h1	MX_STROBE_UDB_SRC	Select UDB strobe source
3'h2	MX_STROBE_NC_2	NC
3'h3	MX_STROBE_NC_3	NC
3'h4	MX_STROBE_CLK_A0_DIG	Select clk_a0_dig
3'h5	MX_STROBE_CLK_A1_DIG	Select clk_a1_dig
3'h6	MX_STROBE_CLK_A2_DIG	Select clk_a2_dig
3'h7	MX_STROBE_CLK_A3_DIG	Select clk_a3_dig

Table 1-387. Bit field encoding: STROBE_EN_ENUM

Value	Name	Description
1'b0	STROBE_EN_0	disable strobe
1'b1	STROBE_EN_1	enable strobe

1.3.435 DAC3_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW0: 0x40005A98

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Name			v_ag5	v_ag4				

(no description)

Bits	Name	Description
5	v_ag5	Connect voltage output to analog global of same side (see field instance name) See Table 1-388.
4	v_ag4	Connect voltage output to analog global of same side (see field instance name) See Table 1-388.

Table 1-388. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.436 DAC3_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW2: 0x40005A9A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Name						v_abus2		v_abus0

(no description)

Bits	Name	Description
2	v_abus2	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-389.
0	v_abus0	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-389.

Table 1-389. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.437 DAC3_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW3: 0x40005A9B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	NA:000			R/W:0
HW Access	R	NA		R	NA			R
Name	iout			i_amx				v_amx

(no description)

Bits	Name	Description
7	iout	Connect current output to pad See Table 1-391.
4	i_amx	Connect current output to Analog Mux Bus See Table 1-390.
0	v_amx	Connect voltage output to Analog Mux Bus See Table 1-390.

Table 1-390. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-391. Bit field encoding: IOUT_ENUM

Value	Name	Description
1'b0	IOUT_NC	not connected
1'b1	IOUT_CONNECT	Connect to pad (see routing diagram)

1.3.438 DAC3_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW4: 0x40005A9C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Name			i_ag5	i_ag4				

(no description)

Bits	Name	Description
5	i_ag5	Connect current output to analog global of same side (see field instance name) See Table 1-392.
4	i_ag4	Connect current output to analog global of same side (see field instance name) See Table 1-392.

Table 1-392. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.439 DAC3_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_STROBE: 0x40005A9F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Name					strobe_en	mx_strobe		

(no description)

Bits	Name	Description
3	strobe_en	Strobe gating control (See mx_strobe==3'h0) See Table 1-394.
2:0	mx_strobe[2:0]	Strobe source selection See Table 1-393.

Table 1-393. Bit field encoding: MX_STROBE_ENUM

Value	Name	Description
3'h0	MX_STROBE_BUSWRITE	Select bus write strobe source (Enable gater regardless of strobe_en setting)
3'h1	MX_STROBE_UDB_SRC	Select UDB strobe source
3'h2	MX_STROBE_NC_2	NC
3'h3	MX_STROBE_NC_3	NC
3'h4	MX_STROBE_CLK_A0_DIG	Select clk_a0_dig
3'h5	MX_STROBE_CLK_A1_DIG	Select clk_a1_dig
3'h6	MX_STROBE_CLK_A2_DIG	Select clk_a2_dig
3'h7	MX_STROBE_CLK_A3_DIG	Select clk_a3_dig

Table 1-394. Bit field encoding: STROBE_EN_ENUM

Value	Name	Description
1'b0	STROBE_EN_0	disable strobe
1'b1	STROBE_EN_1	enable strobe

1.3.440 CMP0_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW0: 0x40005AC0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-395.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-395.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-395.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-395.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-395.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-395.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-395.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-395.

Table 1-395. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.441 CMP0_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW2: 0x40005AC2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							vp_abus1	vp_abus0

(no description)

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-396.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-396.

Table 1-396. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.442 CMP0_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW3: 0x40005AC3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:0
HW Access	NA	R	R	R	R	NA		R
Name		vn_vref1	vn_vref0	vn_amx	vp_refbuf			vp_amx

(no description)

Bits	Name	Description
6	vn_vref1	Connect negative voltage input to Voltage Reference 0 See Table 1-399.
5	vn_vref0	Connect negative voltage input to Voltage Reference 1 See Table 1-399.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-397.
3	vp_refbuf	Connect positive voltage input to CapSense reference buffer channel See Table 1-398.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-397.

Table 1-397. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-398. Bit field encoding: VP_REFBUF_ENUM

Value	Name	Description
1'b0	VP_REFBUF_ENABLED	disable
1'b1	VP_REFBUF_DISABLED	enable

Table 1-399. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.443 CMP0_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW4: 0x40005AC4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		vn_ag6		vn_ag4		vn_ag2		vn_ag0

(no description)

Bits	Name	Description
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-400.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-400.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-400.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-400.

Table 1-400. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.444 CMP0_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW6: 0x40005AC6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:00	
HW Access	NA				R	R	NA	
Name					vn_abus3	vn_abus2		

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-401.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-401.

Table 1-401. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.445 CMP0_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_CLK: 0x40005AC7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Name				bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-402.
3	clk_en	Clock gating control See Table 1-403.
2:0	mx_clk[2:0]	Clock Selection See Table 1-404.

Table 1-402. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-403. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-404. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.446 CMP1_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW0: 0x40005AC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-405.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-405.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-405.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-405.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-405.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-405.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-405.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-405.

Table 1-405. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.447 CMP1_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW2: 0x40005ACA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							vp_abus1	vp_abus0

(no description)

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-406.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-406.

Table 1-406. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.448 CMP1_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW3: 0x40005ACB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:0
HW Access	NA	R	R	R	R	NA		R
Name		vn_vref1	vn_vref0	vn_amx	vp_refbuf			vp_amx

(no description)

Bits	Name	Description
6	vn_vref1	Connect negative voltage input to Voltage Reference 0 See Table 1-409.
5	vn_vref0	Connect negative voltage input to Voltage Reference 1 See Table 1-409.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-407.
3	vp_refbuf	Connect positive voltage input to CapSense reference buffer channel See Table 1-408.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-407.

Table 1-407. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-408. Bit field encoding: VP_REFBUF_ENUM

Value	Name	Description
1'b0	VP_REFBUF_ENABLED	disable
1'b1	VP_REFBUF_DISABLED	enable

Table 1-409. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.449 CMP1_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW4: 0x40005ACC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		vn_ag6		vn_ag4		vn_ag2		vn_ag0

(no description)

Bits	Name	Description
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-410.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-410.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-410.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-410.

Table 1-410. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.450 CMP1_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW6: 0x40005ACE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:00	
HW Access	NA				R	R	NA	
Name					vn_abus3	vn_abus2		

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-411.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-411.

Table 1-411. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.451 CMP1_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_CLK: 0x40005ACF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Name				bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-412.
3	clk_en	Clock gating control See Table 1-413.
2:0	mx_clk[2:0]	Clock Selection See Table 1-414.

Table 1-412. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-413. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-414. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.452 CMP2_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW0: 0x40005AD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-415.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-415.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-415.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-415.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-415.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-415.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-415.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-415.

Table 1-415. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.453 CMP2_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW2: 0x40005AD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							vp_abus1	vp_abus0

(no description)

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-416.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-416.

Table 1-416. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.454 CMP2_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW3: 0x40005AD3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:0
HW Access	NA	R	R	R	R	NA		R
Name		vn_vref1	vn_vref0	vn_amx	vp_refbuf			vp_amx

(no description)

Bits	Name	Description
6	vn_vref1	Connect negative voltage input to Voltage Reference 0 See Table 1-419.
5	vn_vref0	Connect negative voltage input to Voltage Reference 1 See Table 1-419.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-417.
3	vp_refbuf	Connect positive voltage input to CapSense reference buffer channel See Table 1-418.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-417.

Table 1-417. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-418. Bit field encoding: VP_REFBUF_ENUM

Value	Name	Description
1'b0	VP_REFBUF_ENABLED	disable
1'b1	VP_REFBUF_DISABLED	enable

Table 1-419. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.455 CMP2_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW4: 0x40005AD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Name	vn_ag7		vn_ag5		vn_ag3		vn_ag1	

(no description)

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-420.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-420.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-420.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-420.

Table 1-420. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.456 CMP2_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW6: 0x40005AD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:00	
HW Access	NA				R	R	NA	
Name					vn_abus3	vn_abus2		

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-421.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-421.

Table 1-421. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.457 CMP2_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_CLK: 0x40005AD7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Name				bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-422.
3	clk_en	Clock gating control See Table 1-423.
2:0	mx_clk[2:0]	Clock Selection See Table 1-424.

Table 1-422. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-423. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-424. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.458 CMP3_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW0: 0x40005AD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-425.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-425.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-425.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-425.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-425.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-425.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-425.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-425.

Table 1-425. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.459 CMP3_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW2: 0x40005ADA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							vp_abus1	vp_abus0

(no description)

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-426.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-426.

Table 1-426. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.460 CMP3_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW3: 0x40005ADB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:0
HW Access	NA	R	R	R	R	NA		R
Name		vn_vref1	vn_vref0	vn_amx	vp_refbuf			vp_amx

(no description)

Bits	Name	Description
6	vn_vref1	Connect negative voltage input to Voltage Reference 0 See Table 1-429.
5	vn_vref0	Connect negative voltage input to Voltage Reference 1 See Table 1-429.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-427.
3	vp_refbuf	Connect positive voltage input to CapSense reference buffer channel See Table 1-428.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-427.

Table 1-427. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-428. Bit field encoding: VP_REFBUF_ENUM

Value	Name	Description
1'b0	VP_REFBUF_ENABLED	disable
1'b1	VP_REFBUF_DISABLED	enable

Table 1-429. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.461 CMP3_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW4: 0x40005ADC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Name	vn_ag7		vn_ag5		vn_ag3		vn_ag1	

(no description)

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-430.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-430.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-430.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-430.

Table 1-430. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.462 CMP3_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW6: 0x40005ADE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:00	
HW Access	NA				R	R	NA	
Name					vn_abus3	vn_abus2		

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-431.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-431.

Table 1-431. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.463 CMP3_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_CLK: 0x40005ADF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Name				bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-432.
3	clk_en	Clock gating control See Table 1-433.
2:0	mx_clk[2:0]	Clock Selection See Table 1-434.

Table 1-432. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-433. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-434. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.464 DSM0_SW0

Delta Sigma Modulator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW0: 0x40005B00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-435.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-435.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-435.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-435.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-435.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-435.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-435.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-435.

Table 1-435. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.465 DSM0_SW2

Delta Sigma Modulator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW2: 0x40005B02

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Name						vp_abus2		vp_abus0

(no description)

Bits	Name	Description
2	vp_abus2	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-436.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-436.

Table 1-436. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.466 DSM0_SW3

Delta Sigma Modulator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW3: 0x40005B03

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	NA:00	
HW Access	NA	R	R	R	NA	R	NA	
Name		vn_vssa	vn_vref	vn_amx		vp_vssa		

(no description)

Bits	Name	Description
6	vn_vssa	Connect negative voltage input to vssa See Table 1-439.
5	vn_vref	Connect negative voltage input to Voltage Reference See Table 1-438.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-437.
2	vp_vssa	Connect positive voltage input to vssa See Table 1-439.

Table 1-437. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-438. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

Table 1-439. Bit field encoding: VSSA_ENUM

Value	Name	Description
1'b0	VSSA_NC	not connected
1'b1	VSSA_CONNECTED	Connect to vssa

1.3.467 DSM0_SW4

Delta Sigma Modulator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW4: 0x40005B04

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Name	vn_ag7		vn_ag5		vn_ag3		vn_ag1	

(no description)

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-440.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-440.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-440.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-440.

Table 1-440. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.468 DSM0_SW6

Delta Sigma Modulator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW6: 0x40005B06

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Name					vn_abus3		vn_abus1	

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-441.
1	vn_abus1	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-441.

Table 1-441. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.469 DSM0_CLK

Delta Sigma Modulator Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CLK: 0x40005B07

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Name				bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-442.
3	clk_en	Clock gating control See Table 1-443.
2:0	mx_clk[2:0]	Clock Selection See Table 1-444.

Table 1-442. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-443. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-444. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

1.3.470 SAR0_SW0

SAR Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW0: 0x40005B20

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-445.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-445.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-445.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-445.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-445.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-445.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-445.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-445.

Table 1-445. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.471 SAR0_SW2

SAR Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW2: 0x40005B22

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Name						vp_abus2		vp_abus0

(no description)

Bits	Name	Description
2	vp_abus2	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-446.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-446.

Table 1-446. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.472 SAR0_SW3

SAR Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW3: 0x40005B23

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	NA:00	
HW Access	NA	R	R	R	NA	R	NA	
Name		vn_vssa	vn_vref	vn_amx		vp_vssa		

(no description)

Bits	Name	Description
6	vn_vssa	Connect negative voltage input to vssa See Table 1-449.
5	vn_vref	Connect negative voltage input to Voltage Reference See Table 1-448.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-447.
2	vp_vssa	Connect positive voltage input to vssa See Table 1-449.

Table 1-447. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-448. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

Table 1-449. Bit field encoding: VSSA_ENUM

Value	Name	Description
1'b0	VSSA_NC	not connected
1'b1	VSSA_CONNECTED	Connect to vssa

1.3.473 SAR0_SW4

SAR Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW4: 0x40005B24

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		vn_ag6		vn_ag4		vn_ag2		vn_ag0

(no description)

Bits	Name	Description
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-450.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-450.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-450.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-450.

Table 1-450. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.474 SAR0_SW6

SAR Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_SW6: 0x40005B26

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Name					vn_abus3		vn_abus1	

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-451.
1	vn_abus1	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-451.

Table 1-451. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.475 SAR0_CLK

SAR Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR0_CLK: 0x40005B27

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000			R/W:0	R/W:0	R/W:000		
HW Access	R			R	R	R		
Name	mx_pumpclk			bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
7:5	mx_pumpclk[2:0]	Pump Clock Selection See Table 1-455.
4	bypass_sync	Bypass Synchronization See Table 1-452.
3	clk_en	Clock gating control See Table 1-453.
2:0	mx_clk[2:0]	Clock Selection See Table 1-454.

Table 1-452. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-453. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-454. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

Table 1-455. Bit field encoding: MX_PUMPCLK_ENUM

Value	Name	Description
3'h0	MX_PUMPCLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_PUMPCLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_PUMPCLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_PUMPCLK_3	Select clk_a3 and clk_a3_dig

1.3.475 SAR0_CLK (continued)

Table 1-455. Bit field encoding: MX_PUMPCLK_ENUM

3'h4	MX_PUMPCLK_4	Select UDB generated clock

1.3.476 SAR1_SW0

SAR Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW0: 0x40005B28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

(no description)

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-456.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-456.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-456.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-456.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-456.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-456.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-456.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-456.

Table 1-456. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.477 SAR1_SW2

SAR Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW2: 0x40005B2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Name						vp_abus2		vp_abus0

(no description)

Bits	Name	Description
2	vp_abus2	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-457.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-457.

Table 1-457. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.478 SAR1_SW3

SAR Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW3: 0x40005B2B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	NA:00	
HW Access	NA	R	R	R	NA	R	NA	
Name		vn_vssa	vn_vref	vn_amx		vp_vssa		

(no description)

Bits	Name	Description
6	vn_vssa	Connect negative voltage input to vssa See Table 1-460.
5	vn_vref	Connect negative voltage input to Voltage Reference See Table 1-459.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-458.
2	vp_vssa	Connect positive voltage input to vssa See Table 1-460.

Table 1-458. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-459. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

Table 1-460. Bit field encoding: VSSA_ENUM

Value	Name	Description
1'b0	VSSA_NC	not connected
1'b1	VSSA_CONNECTED	Connect to vssa

1.3.479 SAR1_SW4

SAR Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW4: 0x40005B2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Name		vn_ag6		vn_ag4		vn_ag2		vn_ag0

(no description)

Bits	Name	Description
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-461.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-461.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-461.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-461.

Table 1-461. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.480 SAR1_SW6

SAR Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_SW6: 0x40005B2E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Name					vn_abus3		vn_abus1	

(no description)

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-462.
1	vn_abus1	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-462.

Table 1-462. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.481 SAR1_CLK

SAR Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SAR1_CLK: 0x40005B2F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000			R/W:0	R/W:0	R/W:000		
HW Access	R			R	R	R		
Name	mx_pumpclk			bypass_sync	clk_en	mx_clk		

(no description)

Bits	Name	Description
7:5	mx_pumpclk[2:0]	Pump Clock Selection See Table 1-466.
4	bypass_sync	Bypass Synchronization See Table 1-463.
3	clk_en	Clock gating control See Table 1-464.
2:0	mx_clk[2:0]	Clock Selection See Table 1-465.

Table 1-463. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-464. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-465. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

Table 1-466. Bit field encoding: MX_PUMPCLK_ENUM

Value	Name	Description
3'h0	MX_PUMPCLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_PUMPCLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_PUMPCLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_PUMPCLK_3	Select clk_a3 and clk_a3_dig

1.3.481 SAR1_CLK (continued)

Table 1-466. Bit field encoding: MX_PUMPCLK_ENUM

3'h4	MX_PUMPCLK_4	Select UDB generated clock

1.3.482 ABUF0_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF0_MX: 0x40005B40

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Name			mx_vn		mx_vp			

(no description)

Bits	Name	Description
5:4	mx_vn[1:0]	Mux Select VN See Table 1-467.
3:0	mx_vp[3:0]	Mux Select VP See Table 1-468.

Table 1-467. Bit field encoding: ABUF0_MX_VN_ENUM

Value	Name	Description
2'h0	ABUF0_MX_VN_DEFAULT	Not Connected (Default)
2'h1	ABUF0_MX_VN_AG4	Mux Selection AGL[4]
2'h2	ABUF0_MX_VN_AG6	Mux Selection AGL[6]

Table 1-468. Bit field encoding: ABUF0_MX_VP_ENUM

Value	Name	Description
4'h0	ABUF0_MX_VP_0	Not Connected (Default)
4'h1	ABUF0_MX_VP_AG4	Mux Selection: AGL[4]
4'h2	ABUF0_MX_VP_AG5	Mux Selection: AGL[5]
4'h3	ABUF0_MX_VP_AG6	Mux Selection: AGL[6]
4'h4	ABUF0_MX_VP_AG7	Mux Selection: AGL[7]
4'h5	ABUF0_MX_VP_ABUS0	Mux Selection: ABUSL[0]
4'h6	ABUF0_MX_VP_ABUS1	Mux Selection: ABUSL[1]
4'h7	ABUF0_MX_VP_ABUS2	Mux Selection: ABUSL[2]
4'h8	ABUF0_MX_VP_ABUS3	Mux Selection: ABUSL[3]
4'h9	ABUF0_MX_VP_VREF	Mux Selection: ABUF Voltage Reference
4'ha	ABUF0_MX_VP_H_A	Reserved (NC)
4'hb	ABUF0_MX_VP_H_B	Reserved (NC)
4'hc	ABUF0_MX_VP_H_C	Reserved (NC)
4'hd	ABUF0_MX_VP_H_D	Reserved (NC)
4'he	ABUF0_MX_VP_H_E	Reserved (NC)
4'hf	ABUF0_MX_VP_H_F	Reserved (NC)

1.3.483 ABUF0_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF0_SW: 0x40005B41

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						swinp	swinn	swfol

(no description)

Bits	Name	Description
2	swinp	Switch Enable Positive Input
1	swinn	Switch Enable Negative Input
0	swfol	Switch Enable Follow

1.3.484 ABUF1_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF1_MX: 0x40005B42

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Name			mx_vn		mx_vp			

(no description)

Bits	Name	Description
5:4	mx_vn[1:0]	Mux Select VN See Table 1-469.
3:0	mx_vp[3:0]	Mux Select VP See Table 1-470.

Table 1-469. Bit field encoding: ABUF1_MX_VN_ENUM

Value	Name	Description
2'h0	ABUF1_MX_VN_DEFAULT	Not Connected (Default)
2'h1	ABUF1_MX_VN_AG4	Mux Selection AGR[4]
2'h2	ABUF1_MX_VN_AG6	Mux Selection AGR[6]

Table 1-470. Bit field encoding: ABUF1_MX_VP_ENUM

Value	Name	Description
4'h0	ABUF1_MX_VP_0	Not Connected (Default)
4'h1	ABUF1_MX_VP_AG4	Mux Selection: AGR[4]
4'h2	ABUF1_MX_VP_AG5	Mux Selection: AGR[5]
4'h3	ABUF1_MX_VP_AG6	Mux Selection: AGR[6]
4'h4	ABUF1_MX_VP_AG7	Mux Selection: AGR[7]
4'h5	ABUF1_MX_VP_ABUS0	Mux Selection: ABUSR[0]
4'h6	ABUF1_MX_VP_ABUS1	Mux Selection: ABUSR[1]
4'h7	ABUF1_MX_VP_ABUS2	Mux Selection: ABUSR[2]
4'h8	ABUF1_MX_VP_ABUS3	Mux Selection: ABUSR[3]
4'h9	ABUF1_MX_VP_VREF	Mux Selection: ABUF Voltage Reference
4'ha	ABUF1_MX_VP_H_A	Reserved (NC)
4'hb	ABUF1_MX_VP_H_B	Reserved (NC)
4'hc	ABUF1_MX_VP_H_C	Reserved (NC)
4'hd	ABUF1_MX_VP_H_D	Reserved (NC)
4'he	ABUF1_MX_VP_H_E	Reserved (NC)
4'hf	ABUF1_MX_VP_H_F	Reserved (NC)

1.3.485 ABUF1_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF1_SW: 0x40005B43

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						swinp	swinn	swfol

(no description)

Bits	Name	Description
2	swinp	Switch Enable Positive Input
1	swinn	Switch Enable Negative Input
0	swfol	Switch Enable Follow

1.3.486 ABUF2_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF2_MX: 0x40005B44

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Name			mx_vn		mx_vp			

(no description)

Bits	Name	Description
5:4	mx_vn[1:0]	Mux Select VN See Table 1-471.
3:0	mx_vp[3:0]	Mux Select VP See Table 1-472.

Table 1-471. Bit field encoding: ABUF2_MX_VN_ENUM

Value	Name	Description
2'h0	ABUF2_MX_VN_DEFAULT	Not Connected (Default)
2'h1	ABUF2_MX_VN_AG5	Mux Selection AGL[5]
2'h2	ABUF2_MX_VN_AG7	Mux Selection AGL[7]

Table 1-472. Bit field encoding: ABUF2_MX_VP_ENUM

Value	Name	Description
4'h0	ABUF2_MX_VP_0	Not Connected (Default)
4'h1	ABUF2_MX_VP_AG4	Mux Selection: AGL[4]
4'h2	ABUF2_MX_VP_AG5	Mux Selection: AGL[5]
4'h3	ABUF2_MX_VP_AG6	Mux Selection: AGL[6]
4'h4	ABUF2_MX_VP_AG7	Mux Selection: AGL[7]
4'h5	ABUF2_MX_VP_ABUS0	Mux Selection: ABUSL[0]
4'h6	ABUF2_MX_VP_ABUS1	Mux Selection: ABUSL[1]
4'h7	ABUF2_MX_VP_ABUS2	Mux Selection: ABUSL[2]
4'h8	ABUF2_MX_VP_ABUS3	Mux Selection: ABUSL[3]
4'h9	ABUF2_MX_VP_VREF	Mux Selection: ABUF Voltage Reference
4'ha	ABUF2_MX_VP_H_A	Reserved (NC)
4'hb	ABUF2_MX_VP_H_B	Reserved (NC)
4'hc	ABUF2_MX_VP_H_C	Reserved (NC)
4'hd	ABUF2_MX_VP_H_D	Reserved (NC)
4'he	ABUF2_MX_VP_H_E	Reserved (NC)
4'hf	ABUF2_MX_VP_H_F	Reserved (NC)

1.3.487 ABUF2_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF2_SW: 0x40005B45

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						swinp	swinn	swfol

(no description)

Bits	Name	Description
2	swinp	Switch Enable Positive Input
1	swinn	Switch Enable Negative Input
0	swfol	Switch Enable Follow

1.3.488 ABUF3_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF3_MX: 0x40005B46

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Name			mx_vn		mx_vp			

(no description)

Bits	Name	Description
5:4	mx_vn[1:0]	Mux Select VN See Table 1-473.
3:0	mx_vp[3:0]	Mux Select VP See Table 1-474.

Table 1-473. Bit field encoding: ABUF3_MX_VN_ENUM

Value	Name	Description
2'h0	ABUF3_MX_VN_DEFAULT	Not Connected (Default)
2'h1	ABUF3_MX_VN_AG5	Mux Selection AGR[5]
2'h2	ABUF3_MX_VN_AG7	Mux Selection AGR[7]

Table 1-474. Bit field encoding: ABUF3_MX_VP_ENUM

Value	Name	Description
4'h0	ABUF3_MX_VP_0	Not Connected (Default)
4'h1	ABUF3_MX_VP_AG4	Mux Selection: AGR[4]
4'h2	ABUF3_MX_VP_AG5	Mux Selection: AGR[5]
4'h3	ABUF3_MX_VP_AG6	Mux Selection: AGR[6]
4'h4	ABUF3_MX_VP_AG7	Mux Selection: AGR[7]
4'h5	ABUF3_MX_VP_ABUS0	Mux Selection: ABUSR[0]
4'h6	ABUF3_MX_VP_ABUS1	Mux Selection: ABUSR[1]
4'h7	ABUF3_MX_VP_ABUS2	Mux Selection: ABUSR[2]
4'h8	ABUF3_MX_VP_ABUS3	Mux Selection: ABUSR[3]
4'h9	ABUF3_MX_VP_VREF	Mux Selection: ABUF Voltage Reference
4'ha	ABUF3_MX_VP_H_A	Reserved (NC)
4'hb	ABUF3_MX_VP_H_B	Reserved (NC)
4'hc	ABUF3_MX_VP_H_C	Reserved (NC)
4'hd	ABUF3_MX_VP_H_D	Reserved (NC)
4'he	ABUF3_MX_VP_H_E	Reserved (NC)
4'hf	ABUF3_MX_VP_H_F	Reserved (NC)

1.3.489 ABUF3_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ABUF3_SW: 0x40005B47

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						swinp	swinn	swfol

(no description)

Bits	Name	Description
2	swinp	Switch Enable Positive Input
1	swinn	Switch Enable Negative Input
0	swfol	Switch Enable Follow

1.3.490 LCDDAC_SW0

LCDDAC Switch Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW0: 0x40005B50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						sw0		

(no description)

Bits	Name	Description
2:0	sw0[2:0]	Switch Control for LCD_BIAS_BUS[0] See Table 1-475.

Table 1-475. Bit field encoding: LCDDAC_SW0_ENUM

Value	Name	Description
3'h0	LCDDAC_SW0_NC	NC
3'h1	LCDDAC_SW0_LCDDAC_V0	LCDDAC_V0 connected to LCD_BIAS_BUS[0]
3'h2	LCDDAC_SW0_ABUSR0	ABUSR[0] connected to LCD_BIAS_BUS[0]
3'h3	LCDDAC_SW0_3	LCDDAC_V0 and ABUSR[0] connected to LCD_BIAS_BUS[0]
3'h4	LCDDAC_SW0_ABUSR1	ABUSR[1] connected to LCD_BIAS_BUS[0]
3'h5	LCDDAC_SW0_5	LCDDAC_V0 and ABUSR[1] connected to LCD_BIAS_BUS[0]
3'h6	LCDDAC_SW0_6	ABUSR[0] and ABUSR[1] connected to LCD_BIAS_BUS[0]
3'h7	LCDDAC_SW0_7	LCDDAC_V0 and ABUSR[0] and ABUSR[1] connected to LCD_BIAS_BUS[0]

1.3.491 LCDDAC_SW1

LCDDAC Switch Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW1: 0x40005B51

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						sw1		

(no description)

Bits	Name	Description
2:0	sw1[2:0]	Switch Control for LCD_BIAS_BUS[1] See Table 1-476.

Table 1-476. Bit field encoding: LCDDAC_SW1_ENUM

Value	Name	Description
3'h0	LCDDAC_SW1_NC	NC
3'h1	LCDDAC_SW1_LCDDAC_V1	LCDDAC_V1 connected to LCD_BIAS_BUS[1]
3'h2	LCDDAC_SW1_ABUSL0	ABUSL[0] connected to LCD_BIAS_BUS[1]
3'h3	LCDDAC_SW1_3	LCDDAC_V1 and ABUSL[0] connected to LCD_BIAS_BUS[1]
3'h4	LCDDAC_SW1_ABUSL1	ABUSL[1] connected to LCD_BIAS_BUS[1]
3'h5	LCDDAC_SW1_5	LCDDAC_V1 and ABUSL[1] connected to LCD_BIAS_BUS[1]
3'h6	LCDDAC_SW1_6	ABUSL[0] and ABUSL[1] connected to LCD_BIAS_BUS[1]
3'h7	LCDDAC_SW1_7	LCDDAC_V1 and ABUSL[0] and ABUSL[1] connected to LCD_BIAS_BUS[1]

1.3.492 LCDDAC_SW2

LCDDAC Switch Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW2: 0x40005B52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						sw2		

(no description)

Bits	Name	Description
2:0	sw2[2:0]	Switch Control for LCD_BIAS_BUS[2] See Table 1-477.

Table 1-477. Bit field encoding: LCDDAC_SW2_ENUM

Value	Name	Description
3'h0	LCDDAC_SW2_NC	NC
3'h1	LCDDAC_SW2_LCDDAC_V2	LCDDAC_V2 connected to LCD_BIAS_BUS[2]
3'h2	LCDDAC_SW2_ABUSR2	ABUSR[2] connected to LCD_BIAS_BUS[2]
3'h3	LCDDAC_SW2_3	LCDDAC_V2 and ABUSR[2] connected to LCD_BIAS_BUS[2]
3'h4	LCDDAC_SW2_ABUSR3	ABUSR[3] connected to LCD_BIAS_BUS[2]
3'h5	LCDDAC_SW2_5	LCDDAC_V2 and ABUSR[3] connected to LCD_BIAS_BUS[2]
3'h6	LCDDAC_SW2_6	ABUSR[2] and ABUSR[3] connected to LCD_BIAS_BUS[2]
3'h7	LCDDAC_SW2_7	LCDDAC_V2 and ABUSR[2] and ABUSR[3] connected to LCD_BIAS_BUS[2]

1.3.493 LCDDAC_SW3

LCDDAC Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW3: 0x40005B53

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						sw3		

(no description)

Bits	Name	Description
2:0	sw3[2:0]	Switch Control for LCD_BIAS_BUS[3] See Table 1-478.

Table 1-478. Bit field encoding: LCDDAC_SW3_ENUM

Value	Name	Description
3'h0	LCDDAC_SW3_NC	NC
3'h1	LCDDAC_SW3_LCDDAC_V3	LCDDAC_V3 connected to LCD_BIAS_BUS[3]
3'h2	LCDDAC_SW3_ABUSL2	ABUSL[2] connected to LCD_BIAS_BUS[3]
3'h3	LCDDAC_SW3_3	LCDDAC_V3 and ABUSL[2] connected to LCD_BIAS_BUS[3]
3'h4	LCDDAC_SW3_ABUSL3	ABUSL[3] connected to LCD_BIAS_BUS[3]
3'h5	LCDDAC_SW3_5	LCDDAC_V3 and ABUSL[3] connected to LCD_BIAS_BUS[3]
3'h6	LCDDAC_SW3_6	ABUSL[2] and ABUSL[3] connected to LCD_BIAS_BUS[3]
3'h7	LCDDAC_SW3_7	LCDDAC_V3 and ABUSL[2] and ABUSL[3] connected to LCD_BIAS_BUS[3]

1.3.494 LCDDAC_SW4

LCDDAC Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW4: 0x40005B54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						sw4		

(no description)

Bits	Name	Description
2:0	sw4[2:0]	Switch Control for LCD_BIAS_BUS[4] See Table 1-479.

Table 1-479. Bit field encoding: LCDDAC_SW4_ENUM

Value	Name	Description
3'h0	LCDDAC_SW4_NC	NC
3'h1	LCDDAC_SW4_LCDDAC_V4	LCDDAC_V4 connected to LCD_BIAS_BUS[4]
3'h2	LCDDAC_SW4_AMUXBUSR	AMUXBUSR connected to LCD_BIAS_BUS[4]
3'h3	LCDDAC_SW4_3	LCDDAC_V4 and AMUXBUSR connected to LCD_BIAS_BUS[4]
3'h4	LCDDAC_SW4_AMUXBUSL	AMUXBUSL connected to LCD_BIAS_BUS[4]
3'h5	LCDDAC_SW4_5	LCDDAC_V4 and AMUXBUSL connected to LCD_BIAS_BUS[4]
3'h6	LCDDAC_SW4_6	AMUXBUSR and AMUXBUSL connected to LCD_BIAS_BUS[4]
3'h7	LCDDAC_SW4_7	LCDDAC_V4 and AMUXBUSR and AMUXBUSL connected to LCD_BIAS_BUS[4]

1.3.495 SC_MISC

Switched Cap Miscellaneous Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_MISC: 0x40005B56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:00		R/W:0	R/W:0
HW Access	NA		R	R	NA		R	R
Name			sc_pump_force	sc_pump_auto			diff_pga_1_3	diff_pga_0_2

(no description)

Bits	Name	Description
5	sc_pump_force	force pumping - if block enabled enable pump regardless of voltage state
4	sc_pump_auto	enable autopumping - if block enabled pump when low voltage detected
1	diff_pga_1_3	Switched Cap Pair Connect for Differential Amplifier Applications See Table 1-480.
0	diff_pga_0_2	Switched Cap Pair Connect for Differential Amplifier Applications See Table 1-480.

Table 1-480. Bit field encoding: SC_DIFF_PGA_ENUM

Value	Name	Description
1'h0	SC_DIFF_PGA_DISABLED	Differential PGA pair connect disabled
1'h1	SC_DIFF_PGA_ENABLED	Differential PGA pair connect enabled

1.3.496 BUS_SW0

Bus Switch Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW0: 0x40005B58

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	ag7	ag6	ag5	ag4	ag3	ag2	ag1	ag0

(no description)

Bits	Name	Description
7	ag7	Connect Left and Right Analog Globals See Table 1-488.
6	ag6	Connect Left and Right Analog Globals See Table 1-487.
5	ag5	Connect Left and Right Analog Globals See Table 1-486.
4	ag4	Connect Left and Right Analog Globals See Table 1-485.
3	ag3	Connect Left and Right Analog Globals See Table 1-484.
2	ag2	Connect Left and Right Analog Globals See Table 1-483.
1	ag1	Connect Left and Right Analog Globals See Table 1-482.
0	ag0	Connect Left and Right Analog Globals See Table 1-481.

Table 1-481. Bit field encoding: AG0_ENUM

Value	Name	Description
1'b0	AG0_NC	Disconnect AGL[0] and AGR[0]
1'b1	AG0_CONNECT	Connect AGL[0] and AGR[0]

Table 1-482. Bit field encoding: AG1_ENUM

Value	Name	Description
1'b0	AG1_NC	Disconnect AGL[1] and AGR[1]
1'b1	AG1_CONNECT	Connect AGL[1] and AGR[1]

Table 1-483. Bit field encoding: AG2_ENUM

Value	Name	Description

1.3.496 BUS_SW0 (continued)

Table 1-483. Bit field encoding: AG2_ENUM

1'b0	AG2_NC	Disconnect AGL[2] and AGR[2]
1'b1	AG2_CONNECT	Connect AGL[2] and AGR[2]

Table 1-484. Bit field encoding: AG3_ENUM

Value	Name	Description
1'b0	AG3_NC	Disconnect AGL[3] and AGR[3]
1'b1	AG3_CONNECT	Connect AGL[3] and AGR[3]

Table 1-485. Bit field encoding: AG4_ENUM

Value	Name	Description
1'b0	AG4_NC	Disconnect AGL[4] and AGR[4]
1'b1	AG4_CONNECT	Connect AGL[4] and AGR[4]

Table 1-486. Bit field encoding: AG5_ENUM

Value	Name	Description
1'b0	AG5_NC	Disconnect AGL[5] and AGR[5]
1'b1	AG5_CONNECT	Connect AGL[5] and AGR[5]

Table 1-487. Bit field encoding: AG6_ENUM

Value	Name	Description
1'b0	AG6_NC	Disconnect AGL[6] and AGR[6]
1'b1	AG6_CONNECT	Connect AGL[6] and AGR[6]

Table 1-488. Bit field encoding: AG7_ENUM

Value	Name	Description
1'b0	AG7_NC	Disconnect AGL[7] and AGR[7]
1'b1	AG7_CONNECT	Connect AGL[7] and AGR[7]

1.3.497 BUS_SW2

Bus Switch Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW2: 0x40005B5A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					abus3	abus2	abus1	abus0

(no description)

Bits	Name	Description
3	abus3	Connect Left and Right Analog (local) Buses See Table 1-492.
2	abus2	Connect Left and Right Analog (local) Buses See Table 1-491.
1	abus1	Connect Left and Right Analog (local) Buses See Table 1-490.
0	abus0	Connect Left and Right Analog (local) Buses See Table 1-489.

Table 1-489. Bit field encoding: ABUS0_ENUM

Value	Name	Description
1'b0	ABUS0_NC	Disconnect ABUSL[0] and ABUSR[0]
1'b1	ABUS0_CONNECT	Connect ABUSL[0] and ABUSR[0]

Table 1-490. Bit field encoding: ABUS1_ENUM

Value	Name	Description
1'b0	ABUS1_NC	Disconnect ABUSL[1] and ABUSR[1]
1'b1	ABUS1_CONNECT	Connect ABUSL[1] and ABUSR[1]

Table 1-491. Bit field encoding: ABUS2_ENUM

Value	Name	Description
1'b0	ABUS2_NC	Disconnect ABUSL[2] and ABUSR[2]
1'b1	ABUS2_CONNECT	Connect ABUSL[2] and ABUSR[2]

Table 1-492. Bit field encoding: ABUS3_ENUM

Value	Name	Description
1'b0	ABUS3_NC	Disconnect ABUSL[3] and ABUSR[3]
1'b1	ABUS3_CONNECT	Connect ABUSL[3] and ABUSR[3]

1.3.498 BUS_SW3

Bus Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW3: 0x40005B5B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								amx

(no description)

Bits	Name	Description
0	amx	Connect Left and Rigth Analog Mux Bus See Table 1-493.

Table 1-493. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	Disconnect AMXL and AMXR
1'b1	AMX_CONNECT	Connect AMXL and AMXR

1.3.499 DFT_CR0

DFT Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR0: 0x40005B5C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:000		
HW Access	R	R	R	R	NA	R		
Name	force_tp2	en_tp2	force_tp1	en_tp1		tvmon1_sel		

(no description)

Bits	Name	Description
7	force_tp2	test point 2 - force low. Not used in this release of this device.
6	en_tp2	test point 2 - enable level shifting from TP2 (test point 2) pad to analog global route AGL1.
5	force_tp1	test point 1 - force high. Not used in this release of this device.
4	en_tp1	test point 1 - enable level shifting from TP1 (test point 1) pad to analog global route AGL0.
2:0	tvmon1_sel[2:0]	Connect power net to tvmon1 test point (Also need to select tvmon1 for DFT mux input) See Table 1-494.

Table 1-494. Bit field encoding: TVMON1_SEL_ENUM

Value	Name	Description
3'h0	TVMON1_SEL_NC	tvmon1/1a test points not connected (Default)
3'h1	TVMON1_SEL_VSLEEP	tvmon1/1a test points connected to vsleep
3'h2	TVMON1_SEL_VPWRKA	tvmon1/1a test points connected to vpwrka
3'h3	TVMON1_SEL_VPWRI2C	tvmon1/1a test points connected to vpwri2c
3'h4	TVMON1_SEL_VPB	tvmon1/1a test points connected to vpb
3'h5	TVMON1_SEL_VPWRA	tvmon1/1a test points connected to vpwra
3'h6	TVMON1_SEL_VNWELL	tvmon1/1a test points connected to vnwell
3'h7	TVMON1_SEL_NC2	tvmon1/1a test points not connected

1.3.500 DFT_CR1

DFT Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR1: 0x40005B5D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						tvmon2_sel		

(no description)

Bits	Name	Description
2:0	tvmon2_sel[2:0]	Connect power net to tvmon2 test point (Also need to select tvmon1 for DFT mux input) See Table 1-495.

Table 1-495. Bit field encoding: TVMON2_SEL_ENUM

Value	Name	Description
3'h0	TVMON2_SEL_NC	tvmon2/2a test points not connected (Default)
3'h1	TVMON2_SEL_VNB	tvmon2/2a test points connected to vnb
3'h2	TVMON2_SEL_VREF	tvmon2/2a test points connected to bref_v800mV
3'h3	TVMON2_SEL_VPWRD	tvmon2/2a test points connected to Digital LDO output
3'h4	TVMON2_SEL_NPROT	tvmon2/2a test points connected to nprot
3'h5	TVMON2_SEL_BIASN	tvmon2/2a test points connected to biasn
3'h6	TVMON2_SEL_VSSA	tvmon2/2a test points connected to vssa
3'h7	TVMON2_SEL_NC2	tvmon2/2a test points not connected

1.3.501 DFT_CR2

DFT Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR2: 0x40005B5E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Name		dft_mx1				dft_mx0		

(no description)

Bits	Name	Description
6:4	dft_mx1[2:0]	Connect test signals to AGL<7> (Analog Global Left 7) See Table 1-497.
2:0	dft_mx0[2:0]	Connect test signals to AGL<4> (Analog Global Left 4) See Table 1-496.

Table 1-496. Bit field encoding: DFT_MX0_ENUM

Value	Name	Description
3'h0	DFT_MX0_NC	NC
3'h1	DFT_MX0_DAC0_TMUX_AGL4	Connect dac0_tmux to AGL<4>
3'h2	DFT_MX0_DSM0_SUMN_TST_AGL4	Connect dsm0_sumn_tst to AGL<4>
3'h3	DFT_MX0_DSM0_REFOUT_AGL4	Connect dsm0_refout to AGL<4>
3'h4	DFT_MX0_DSM0_TST_DIGOUT_AGL4	Connect dsm0_tst_digout to AGL<4>
3'h5	DFT_MX0_TS_DFT_AGL4	Connect ts_dft (SPC Temp Sensor) to AGL<4>
3'h6	DFT_MX0_FM_DFT_AGL4	Connect fm_dft (Flash Memory) to AGL<4>

Table 1-497. Bit field encoding: DFT_MX1_ENUM

Value	Name	Description
3'h0	DFT_MX1_NC	NC
3'h1	DFT_MX1_DAC2_TMUX_AGL7	Connect dac2_tmux to AGL<7>
3'h2	DFT_MX1_CMP_DFT_AGL7	Connect cmp_dft to AGL<7> (see also cmp_mxdft[1:0])
3'h3	DFT_MX1_TVMON1_AGL7	Connect pwrsys tvmon1 to AGL<7>
3'h4	DFT_MX1_TVMON2_AGL7	Connect pwrsys tvmon2 to AGL<7>
3'h5	DFT_MX1_DSM0_SUMP_TST_AGL7	Connect dsm0_sump_tst to AGL<7>
3'h6	DFT_MX1_BREF_ITEST_AGL7	Connect bref_itest to AGL<7>

1.3.502 DFT_CR3

DFT Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFT_CR3: 0x40005B5F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Name		dft_mx3				dft_mx2		

(no description)

Bits	Name	Description
6:4	dft_mx3[2:0]	Connect test signals to AGR<7> (Analog Global Right 7) See Table 1-499.
2:0	dft_mx2[2:0]	Connect test signals to AGR<4> (Analog Global Right 4) See Table 1-498.

Table 1-498. Bit field encoding: DFT_MX2_ENUM

Value	Name	Description
3'h0	DFT_MX2_NC	NC
3'h1	DFT_MX2_DAC3_TMUX_AGR4	Connect dacr1_tmux to AGR<4>
3'h2	DFT_MX2_BREF_ISRC7_AGR4	Connect bref_isrc7 to AGR<4>
3'h3	DFT_MX2_LCDDAC_DFT_AGR4	Connect lcddac_dft to AGR<4>
3'h4	DFT_MX2_S8XOSC_TPUMP_DFT_AGR4	Connect s8xosc_tpump_dft to AGR<4>
3'h5	DFT_MX2_TVMON1A	Connect pwrsys tvmon1a to AGR<4>
3'h6	DFT_MX2_TVMON2A	Connect pwrsys tvmon2a to AGR<4>

Table 1-499. Bit field encoding: DFT_MX3_ENUM

Value	Name	Description
3'h0	DFT_MX3_NC	NC
3'h1	DFT_MX3_DAC1_TMUX_AGR7	Connect dac1_tmux to AGR<7>
3'h2	DFT_MX3_S8XOSC_TESTOUT_DFT_AGR7	Connect s8xosc_testout_dft to AGR<7>
3'h3	DFT_MX3_BGREFS_TMUX_AGR7	Connect bgrefs_tmux to AGR<7>
3'h4	DFT_MX3_BG_TMUX_AGR7	Connect bg_tmux to AGR<7>
3'h5	DFT_MX3_X32_TST_AGR7	Connect x32_tst to AGR<7>
3'h6	DFT_MX3_PLL_VCTRLIO_AGR7	Connect pll_VctrlIO to AGR<7>

1.3.503 DAC[0..3]_D

DAC Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_D: 0x40005B80 DAC1_D: 0x40005B81 DAC2_D: 0x40005B82

DAC3_D: 0x40005B83

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data							

(no description)

Bits	Name	Description
7:0	data[7:0]	8 DAC Data bits

1.3.504 DSM[0..0]_OUT0

DSM Output Register 0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DSM0_OUT0: 0x40005B88

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	dout							

(no description)

Bits	Name	Description
7:0	dout[7:0]	DSM output

1.3.505 DSM[0..0]_OUT1

DSM Output Register 1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DSM0_OUT1: 0x40005B89

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R:0	R:0	R:0000			
HW Access	NA		W	W	W			
Name			ovdcause	ovdflag	dout2scomp			

(no description)

Bits	Name	Description
5	ovdcause	Overload Cause See Table 1-501.
4	ovdflag	Overload detected
3:0	dout2scomp[3:0]	DSM Output Register 1 See Table 1-500.

Table 1-500. Bit field encoding: DSM_DOUT2SCOMP_ENUM

Value	Name	Description
4'b0000	DSM_DOUT2SCOMP_0	NA (qlev=00); 0 (qlev=01); 0 (qlev=10)
4'b0001	DSM_DOUT2SCOMP_1	+1 (qlev=00); +1 (qlev=01); +1 (qlev=10)
4'b0010	DSM_DOUT2SCOMP_2	NA (qlev=00); NA (qlev=01); +2 (qlev=10)
4'b0011	DSM_DOUT2SCOMP_3	NA (qlev=00); NA (qlev=01); +3 (qlev=10)
4'b0100	DSM_DOUT2SCOMP_4	NA (qlev=00); NA (qlev=01); +4 (qlev=10)
4'b0101	DSM_DOUT2SCOMP_5	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'b0110	DSM_DOUT2SCOMP_6	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'b0111	DSM_DOUT2SCOMP_7	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'b1000	DSM_DOUT2SCOMP_8	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'b1001	DSM_DOUT2SCOMP_9	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'b1010	DSM_DOUT2SCOMP_10	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'b1011	DSM_DOUT2SCOMP_11	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'b1100	DSM_DOUT2SCOMP_12	NA (qlev=00); NA (qlev=01); -4 (qlev=10)
4'b1101	DSM_DOUT2SCOMP_13	NA (qlev=00); NA (qlev=01); -3 (qlev=10)
4'b1110	DSM_DOUT2SCOMP_14	NA (qlev=00); NA (qlev=01); -2 (qlev=10)
4'b1111	DSM_DOUT2SCOMP_15	-1 (qlev=00); -1 (qlev=01); -1 (qlev=10)

Table 1-501. Bit field encoding: OVDCAUSE_ENUM

Value	Name	Description
1'b0	OVDCAUSE_0	0s overload
1'b1	OVDCAUSE_1	1s overload

1.3.506 SC_SR

Switched Capacitor Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_SR: 0x40005B8C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				RC:0	RC:0	RC:0	RC:0
HW Access	NA				W	W	W	W
Name					sc3_modout	sc2_modout	sc1_modout	sc0_modout

(no description)

Bits	Name	Description
3	sc3_modout	Switched Cap block modulator output
2	sc2_modout	Switched Cap block modulator output
1	sc1_modout	Switched Cap block modulator output
0	sc0_modout	Switched Cap block modulator output

1.3.507 SC_MSK

SC IRQ Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_MSK: 0x40005B8D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					sc3_msk	sc2_msk	sc1_msk	sc0_msk

(no description)

Bits	Name	Description
3	sc3_msk	Enable SC IRQ See Table 1-502.
2	sc2_msk	Enable SC IRQ See Table 1-502.
1	sc1_msk	Enable SC IRQ See Table 1-502.
0	sc0_msk	Enable SC IRQ See Table 1-502.

Table 1-502. Bit field encoding: SC_MSK_ENUM

Value	Name	Description
1'b1	SC_MSK_ENABLE	enable SC IRQ
1'b0	SC_MSK_DISABLE	disable SC IRQ

1.3.508 LUT_SR

LUT Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

LUT_SR: 0x40005B8E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				RC:0	RC:0	RC:0	RC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					lut3_out	lut2_out	lut1_out	lut0_out

Clear-on-read sticky status register

Bits	Name	Description
3	lut3_out	LUT output
2	lut2_out	LUT output
1	lut1_out	LUT output
0	lut0_out	LUT output

1.3.509 LUT_MSK

LUT Interrupt ReQuest (IRQ) Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_MSK: 0x40005B8F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					lut3_msk	lut2_msk	lut1_msk	lut0_msk

(no description)

Bits	Name	Description
3	lut3_msk	Enable LUT IRQ See Table 1-503.
2	lut2_msk	Enable LUT IRQ See Table 1-503.
1	lut1_msk	Enable LUT IRQ See Table 1-503.
0	lut0_msk	Enable LUT IRQ See Table 1-503.

Table 1-503. Bit field encoding: LUT_MSK_ENUM

Value	Name	Description
1'b1	LUT_MSK_ENABLE	enable LUT IRQ
1'b0	LUT_MSK_DISABLE	disable LUT IRQ

1.3.510 CMP_WRK

Comparator output working register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CMP_WRK: 0x40005B90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:0	R:0	R:0	R:0
HW Access	NA				W	W	W	W
Name					cmp3_out	cmp2_out	cmp1_out	cmp0_out

(no description)

Bits	Name	Description
3	cmp3_out	Comparator Output
2	cmp2_out	Comparator Output
1	cmp1_out	Comparator Output
0	cmp0_out	Comparator Output

1.3.511 CMP_LTRI

Comparator LTRI working register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP_LTRI: 0x40005B91

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		NA:0	R/W:0
HW Access	NA				R		NA	R
Name					cmp_mxdft			ltri

(no description)

Bits	Name	Description
3:2	cmp_mxdft[1:0]	Comparator Test Point selection (Need to further select with DFT muxes) See Table 1-504.
0	ltri	Enables/latches the comparator output for transient time measurement purposes

Table 1-504. Bit field encoding: CMP_MXDFT_ENUM

Value	Name	Description
2'h0	CMP_MXDFT_0	cmp0_out_tr
2'h1	CMP_MXDFT_1	cmp1_out_tr
2'h2	CMP_MXDFT_2	cmp2_out_tr
2'h3	CMP_MXDFT_3	cmp3_out_tr

1.3.512 TFAULT_WRK0

Timing Fault Working Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TFAULT_WRK0: 0x40005B92

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	fine_taps_7_0							

(no description)

Bits	Name	Description
7:0	fine_taps_7_0[7:0]	Fine Taps 7:0 Capture

1.3.513 TFAULT_WRK1

Timing Fault Working Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TFAULT_WRK1: 0x40005B93

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	fine_taps_15_8							

(no description)

Bits	Name	Description
7:0	fine_taps_15_8[7:0]	Fine Taps 15:8 Capture

1.3.514 TFAULT_WRK2

Timing Fault Working Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TFAULT_WRK2: 0x40005B94

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:0000			
HW Access	NA				R/W			
Name					coarse_taps			

(no description)

Bits	Name	Description
3:0	coarse_taps[3:0]	Coarse Taps 3:0 Capture

1.3.515 TFAULT_WRK3

Timing Fault Working Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TFAULT_WRK3: 0x40005B95

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							W:0
HW Access	NA							R
Name								oneshot_trigger

(no description)

Bits	Name	Description
0	oneshot_trigger	oneshot trigger (Write-only)

1.3.516 SAR[0..1]_WRK0

SAR working register 0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SAR0_WRK0: 0x40005BA0 SAR1_WRK0: 0x40005BA2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	data_out_7_0							

(no description)

Bits	Name	Description
7:0	data_out_7_0[7:0]	data_out[7:0]

1.3.517 SAR[0..1]_WRK1

SAR register 1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SAR0_WRK1: 0x40005BA1 SAR1_WRK1: 0x40005BA3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0	NA:000			R:0000			
HW Access	R/W	NA			R/W			
Name	overrun_det				data_out_11_8			

(no description)

Bits	Name	Description
7	overrun_det	data overrun detection flag (read-to-clear sticky bit) is set when overrun_det_en is set and new data overwrote old data / old data not read (completely) See Table 1-505.
3:0	data_out_11_8[3:0]	data_out[11:8]

Table 1-505. Bit field encoding: SAR_OVERRUN_DET_ENUM

Value	Name	Description
1'b0	SAR_OVERRUN_DET_0	no data overrun has occurred
1'b1	SAR_OVERRUN_DET_1	data overrun has occurred - all bytes of the last data_out have not been read when new data was written

1.3.518 ANAIF_WRK_SARS_SOF

SAR Global Start-of-frame register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ANAIF_WRK_SARS_SOF: 0x40005BA8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							sof_bit_1	sof_bit_0

(no description)

Bits	Name	Description
1	sof_bit_1	Start-of-Frame (sof) register source; enable conversion; (NOTE: autoclearing upon receipt of eof_sync when sof_mode==edge-sensitive) See Table 1-506.
0	sof_bit_0	Start-of-Frame (sof) register source; enable conversion; (NOTE: autoclearing upon receipt of eof_sync when sof_mode==edge-sensitive) See Table 1-506.

Table 1-506. Bit field encoding: SAR_SOF_BIT_ENUM

Value	Name	Description
1'b0	SAR_SOF_BIT_0	disable conversion
1'b1	SAR_SOF_BIT_1	Enable conversion

1.3.519 USB_EP0_DR[0..7]

Control End point EP0 Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_EP0_DR0: 0x40006000	USB_EP0_DR1: 0x40006001
USB_EP0_DR2: 0x40006002	USB_EP0_DR3: 0x40006003
USB_EP0_DR4: 0x40006004	USB_EP0_DR5: 0x40006005
USB_EP0_DR6: 0x40006006	USB_EP0_DR7: 0x40006007

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_byte							

The Endpoint 0 Data Register (EP0_DR) is used to read and write data to the USB control endpoint. The EP0_DR register has a hardware-locking feature that prevents the CPU write when SETUP is active. The registers are locked as soon as the SETUP token is decoded and remain locked throughout the SETUP transaction and until the EP0_CR register have been read. This is to prevent over-writing new SETUP data before firmware knows it has arrived. All other endpoint data buffers do not have this locking feature. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_byte[7:0]	This register is shared for both transmit and receive. The count in the EP0_CNT register determines the number of bytes received or to be transferred.

1.3.520 USB_CR0

USB control 0 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_CR0: 0x40006008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Name	usb_enable	device_address						

The USB Control Register 0 (CR0) is used to set the PSoC3's USB address and enable the USB system resource. All bits in this register are reset to zero when a USB bus reset interrupt occurs. The IMO frequency should be set to 24MHz before USB is enabled. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	usb_enable	This bit enables the PSoC device to respond to USB traffic. 0 - USB disabled. 1 - USB enabled.
6:0	device_address[6:0]	These bits specify the USB device address to which the SIE will respond. This address must be set by firmware and is specified by the USB Host with a SET ADDRESS command during USB enumeration. This value must be programmed by firmware when assigned during enumeration. It is not set automatically by the hardware.

1.3.521 USB_CR1

USB control 1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_CR1: 0x40006009

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/WZC:0	R/W:0	R/W:0
HW Access	NA					W	R	R
Name						bus_activity	enable_lock	reg_enable

The USB Control Register 1 (CR1) is used to configure the internal regulator and the oscillator tuning capability. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
2	bus_activity	The Bus Activity bit is a stickybit that detects any non-idle USB event that has occurred on the USB bus. Once set to High by the SIE to indicate the bus activity this bit retains its logical High value until firmware clears it. Writing a '0' to this bit clears it; writing a '1' preserves its value. 0 No activity. 1 Non-idle activity (D+ = Low) was detected since the last time the bit was cleared. Sticky (individual bits)
1	enable_lock	This bit is set to turn on the automatic frequency locking of the internal oscillator to USB traffic. Unless an external clock is being provided this bit should remain set for proper USB operation. 0 Locking disabled. 1 Locking enabled.
0	reg_enable	This bit controls the operation of the internal USB regulator. For applications with PSoC supply voltages in the 5V range this bit is set high to enable the internal regulator. For device supply voltage in the 3.3V range this bit is cleared to connect the transceiver directly to the supply. 0- Pass-through mode. Use for Vdd = 3.3V range. 1- Regulating mode. Use for Vdd = 5V range.

1.3.522 USB_SIE_EP_INT_EN

USB SIE Data Endpoints Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP_INT_EN: 0x4000600A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	ep8_intr_en	ep7_intr_en	ep6_intr_en	ep5_intr_en	ep4_intr_en	ep3_intr_en	ep2_intr_en	ep1_intr_en

The USB SIE Data Endpoints Interrupt Enable Register (SIE_EP_INT_EN) is used to enable/ mask the Data Endpoint Interrupts This register is clocked with the AHB Bus Clock

Bits	Name	Description
7	ep8_intr_en	EP8 Interrupt Enable. 0: Do not raise EP8 Interrupt. 1: Raise EP8 Interrupt
6	ep7_intr_en	EP7 Interrupt Enable. 0: Do not raise EP7 Interrupt. 1: Raise EP7 Interrupt
5	ep6_intr_en	EP6 Interrupt Enable. 0: Do not raise EP6 Interrupt. 1: Raise EP6 Interrupt
4	ep5_intr_en	EP5 Interrupt Enable. 0: Do not raise EP5 Interrupt. 1: Raise EP5 Interrupt
3	ep4_intr_en	EP4 Interrupt Enable. 0: Do not raise EP4 Interrupt. 1: Raise EP4 Interrupt
2	ep3_intr_en	EP3 Interrupt Enable. 0: Do not raise EP3 Interrupt. 1: Raise EP3 Interrupt
1	ep2_intr_en	EP2 Interrupt Enable. 0: Do not raise EP2 Interrupt. 1: Raise EP2 Interrupt
0	ep1_intr_en	EP1 Interrupt Enable. 0: Do not raise EP1 Interrupt. 1: Raise EP1 Interrupt

1.3.523 USB_SIE_EP_INT_SR

SIE Data Endpoint Interrupt Status

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP_INT_SR: 0x4000600B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ep8_intr	ep7_intr	ep6_intr	ep5_intr	ep4_intr	ep3_intr	ep2_intr	ep1_intr

SIE Data Endpoint Status Register. This is an Interrupt Status Register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_intr	EP8 Interrupt Status. 0: EP8 Interrupt not raised. 1: EP8 Interrupt Present
6	ep7_intr	EP7 Interrupt Status. 0: EP7 Interrupt not raised. 1: EP7 Interrupt Present
5	ep6_intr	EP6 Interrupt Status. 0: EP6 Interrupt not raised. 1: EP6 Interrupt Present
4	ep5_intr	EP5 Interrupt Status. 0: EP5 Interrupt not raised. 1: EP5 Interrupt Present
3	ep4_intr	EP4 Interrupt Status. 0: EP4 Interrupt not raised. 1: EP4 Interrupt Present
2	ep3_intr	EP3 Interrupt Status. 0: EP3 Interrupt not raised. 1: EP3 Interrupt Present
1	ep2_intr	EP2 Interrupt Status. 0: EP2 Interrupt not raised. 1: EP2 Interrupt Present
0	ep1_intr	EP1 Interrupt Status. 0: EP1 Interrupt not raised. 1: EP1 Interrupt Present

1.3.524 USB_SIE_EP1_CNT0

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP1_CNT0: 0x4000600C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R	W	NA			R		
Name	data_toggle	data_valid				data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.525 USB_SIE_EP1_CNT1

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP1_CNT1: 0x4000600D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.526 USB_SIE_EP1_CR0

Propname	Non-control end-point's control Regis-ter

0x4000600eSystem reset for retention flops [reset_all_retention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.527 USB_USBIO_CR0

USBIO Control 0 Register

Reset: Reset Signals Listed Below

Register : Address

USB_USBIO_CR0: 0x40006010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	NA:0000				R:U
HW Access	R	R	R	NA				W
Name	ten	tse0	td					rd

The USB IO Control Register 0 (USBIO_CR0) is used for manually transmitting on the USB D+ and D- pins or reading the differential receiver. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	ten	USB Transmit Enable. This is used to manually transmit on the D+ and D- pins. Normally this bit should be cleared to allow the internal SIE to drive the pins. The most common reason for manually transmitting is to force a resume state on the bus. 0- Manual Transmission Off (TSE0 and TD have no effect). 1- Manual Transmission Enabled (TSE0 and TD determine the state of the D+ and Dpins).
6	tse0	Transmit Single-Ended Zero. SE0: both D+ and D- low. No effect if TEN=0. 0- Do not force SE0. 1- Force SE0 on D+ and D-.
5	td	Transmit Data. Transmit a USB J or K state on the USB bus. No effect if TEN=0 or TSE0=1. 0- Force USB K state (D+ is low D- is high). 1- Force USB J state (D+ is high D- is low)
0	rd	Received Data. This read only bit gives the state of the USB differential receiver. 0- D+ < D- or D+ = D- = 0.

Reset Table

resetsignal	field(s)
N/A	rd
System reset for retention flops [reset_all_retention]	td, tse0, ten

1.3.528 USB_USBIO_CR2

USBIO control 2 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_USBIO_CR2: 0x40006011

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	R	R	R	R	R	R	R	
Name	test_res	test_pkt	x_dec	x_inc	minc	mdec	trim	

The USB IO Control Register 2 (USBIO_CR2) is an internal register used for trimming the USBIO cell and for access to internal test modes. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	test_res	This bit is for testing the nonpass through suspend mode pull up. 0- No effect. 1- Apply resistor to the D+ pin.
6	test_pkt	This bit enables the device to transmit a packet in response to an internally generated IN packet. This bit has no affect unless the Test OK bit is set in the CR1 register. 0- No effect. 1- Generate one packet when set.
5	x_dec	This bit supplies the option to decrease the USB crossover voltage. 0- No effect. 1- Decrement crossover voltage.
4	x_inc	This bit supplies the option to increase the USB crossover voltage. 0- No effect. 1- Increment crossover voltage.
3	minc	When set this bit increases the USB edge matching ratio.
2	mdec	When set this bit decreases the USB edge matching ratio.
1:0	trim[1:0]	These two bits of trim are for the suspend mode resistor. 00- No effect. 01- Lower idle voltage. 10- Raise idle voltage. 11- Do not use.

1.3.529 USB_USBIO_CR1

USBIO control 1 Register

Reset: Reset Signals Listed Below

Register : Address

USB_USBIO_CR1: 0x40006012

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R:U	R:U
HW Access	R	R	R	R	R	R	W	W
Name	iomode	drive_mode	dpi	dmi	p2puen	usbpuen	dpo	dmo

The USB IO Control Register 1 (USBIO_CR1) is used to manually read or write the D+ and D- pins and to configure internal pull-up resistors on those pins. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	iomode	This bit allows the D+ and D- pins to be configured for either USB mode or bit banged modes. If this bit is set the DMI and DPI bits are used to drive the D- and D+ pins. 0- USB Mode. Drive Mode has no effect. 1- Drive Mode DMI and DPI determine state of the D+ and D- pins.
6	drive_mode	If the IOMode bit is set this bit configures the D- and D+ pins for either CMOS drive or open-drain drive. If IOMode is cleared this bit has no effect. In open drain mode 5 k? pull-up resistors can be connected internally with the PS2PUEN bit. 0- D+ and D- are in open drain mode. If the DPI or DMI bits are set high the corresponding D+ or D- pad will be high impedance. 1- D+ and D- are in CMOS drive mode. D+ follows DPI and D- follows DMI.
5	dpi	This bit is used to drive the D+ pin if IOMode=1. Refer to the Drive Mode bit for drive state of pad. 0- Drive D+ pad low. 1- Drive D+ pad high (unless Drive Mode=0).
4	dmi	This bit is used to drive the D- pin if IOMode=1. Refer to the Drive Mode bit for drive stateof pad. 0- Drive D- pad low. 1- Drive D- pad high (unless Drive Mode=0).
3	p2puen	This bit controls the connection of the two internal 5 k pull-up resistors to the D+ and D- pins. 0- No effect. 1- Apply 5K pull-ups between Vdd and both D+ and D- pads independent of the IO-Mode and Drive Mode bits.
2	usbpuen	This bit controls the connection of the internal 1.5 k pull up resistor on the D+ pin. 0- No effect. 1- Apply internal USB pull-up resistor to D+ pad.
1	dpo	This read only bit gives the state of the D+ pin.
0	dmo	This read only bit gives the state of the D- pin.

Reset Table

resetsignal	field(s)
N/A	dmo, dpo
System reset for retention flops [reset_all_retention]	usbpuen, p2puen, dmi, dpi, drive_mode, iomode

1.3.530 USB_SOF0

Start Of Frame Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SOF0: 0x40006018

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	frame_number							

The USB Start of Frame Registers (SOF0 and SOF1) provide access to the 11-bit SOF frame number. Start of frame packets are sent from the host every one ms. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	frame_number[7:0]	It has the lower 8 bits [7:0] of the SOF frame number.

1.3.531 USB_SOF1

Start Of Frame Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SOF1: 0x40006019

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R:000		
HW Access	NA					R/W		
Name						frame_number		

The USB Start of Frame Registers (SOF0 and SOF1) provide access to the 11-bit SOF frame number. Start of frame packets are sent from the host every one ms. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
2:0	frame_number[2:0]	It has the upper 3 bits [10:8] of the SOF frame number.

1.3.532 USB_SIE_EP2_CNT0

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP2_CNT0: 0x4000601C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R	W	NA			R		
Name	data_toggle	data_valid				data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.533 USB_SIE_EP2_CNT1

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP2_CNT1: 0x4000601D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.534 USB_SIE_EP2_CR0

Propname	Non-control end-point's control Regis-ter

0x4000601eSystem reset for retention flops [reset_all_retention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.535 USB_OSCLK_DR0

Oscillator lock data register 0

Reset: N/A

Register : Address

USB_OSCLK_DR0: 0x40006020

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	W							
Name	adder							

The Oscillator Lock Data Register 0 (OSCLK_DR0) is an internal register that may be used in the testing of the oscillator locking circuit. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	adder[7:0]	These bits return the lower 8 bits of the oscillator locking circuits adder output.

1.3.536 USB_OSCLK_DR1

Oscillator lock data register 1

Reset: N/A

Register : Address

USB_OSCLK_DR1: 0x40006021

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R:UUUUUUU						
HW Access	NA	W						
Name		adder						

The Oscillator Lock Data Register 1 (OSCLK_DR1) is an internal register that may be used in the testing of the oscillator locking circuit. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
6:0	adder[6:0]	These bits return the upper 7 bits of the oscillator locking circuits adder output.

1.3.537 USB_EP0_CR

Endpoint0 control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_EP0_CR: 0x40006028

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WC:0	R/WC:0	R/WC:0	R/WC:0	R/W:0000			
HW Access	W	W	W	W	R			
Name	setup_rcvd	in_rcvd	out_rcvd	acked_txn	mode			

The Endpoint Control Register (EP0_CR) is used to configure endpoint 0. Because both firmware and the SIE are allowed to write to the Endpoint 0 Control and Count registers the SIE provides an interlocking mechanism to prevent accidental overwriting of data. When the SIE writes to these registers they are locked and the processor cannot write to them until after reading the EP0_CR register. Writing to this register clears the upper four bits regardless of the value written. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	setup_rcvd	When set this bit indicates a valid SETUP packet was received and ACKed. This bit is forced HIGH from the start of the data packet phase of the SETUP transaction until the start of the ACK packet returned by the SIE. The CPU is prevented from clearing this bit during this interval. After this interval the bit will remain set until cleared by firmware. While this bit is set to '1' the CPU cannot write to the EP0_DRx registers. This prevents firmware from overwriting an incoming SETUP transaction before firmware has a chance to read the SETUP data. This bit is cleared by any non-locked writes to the register. Sticky (individual bits)
6	in_rcvd	When set this bit indicates a valid IN packet has been received. This bit is updated to '1' after the host acknowledges an IN data packet. When clear this bit indicates either no IN has been received or that the host did not acknowledge the IN data by sending ACK handshake. It is cleared by any non-locked writes to the register. Sticky (individual bits)
5	out_rcvd	When set this bit indicates a valid OUT packet has been received and ACKed. This bit is updated to '1' after the last received packet in an OUT transaction. When clear this bit indicates no OUT received. It is cleared by any non-locked writes to the register. Sticky (individual bits)
4	acked_txn	This bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with a ACK packet. This bit is cleared by any nonlocked writes to the register. Sticky (individual bits)
3:0	mode[3:0]	The mode bits control how the USB SIE responds to traffic and how the USB SIE will change the mode of that endpoint as a result of host packets to the endpoint.

1.3.538 USB_EP0_CNT

Endpoint0 count Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_EP0_CNT: 0x40006029

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:00		R/W:0000			
HW Access	R	W	NA		R			
Name	data_toggle	data_valid			byte_count			

The Endpoint 0 Count Register (EP0_CNT) is used to configure endpoint 0. Whenever the count updates from a SETUP or OUT transaction this register locks and can not be written by the CPU. Reading the EP0_CR register unlocks this register. This prevents firmware from overwriting a status update on incoming SETUP or OUT transactions before firmware has a chance to read the data. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit. For OUT or SETUP transactions the SIE hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit indicates whether there were errors in OUT or SETUP transactions. It is cleared to '0' if CRC bit stuff or PID errors have occurred. This bit does not update for some endpoint mode settings. This bit may be cleared by writing a zero to it when the register is not locked. 0- Error in data received. 1- No Errors Sticky (individual bits)
3:0	byte_count[3:0]	These bits indicate the number of data bytes in a transaction. For IN transactions firmware loads the count with the number of bytes to be transmitted to the host from the endpoint FIFO. Valid values are 0 to 8. For OUT or SETUP transactions the count is updated by hardware to the number of data bytes received plus two for the CRC bytes. Valid values are 2 to 10.

1.3.539 USB_SIE_EP3_CNT0

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP3_CNT0: 0x4000602C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R	W	NA			R		
Name	data_toggle	data_valid				data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.540 USB_SIE_EP3_CNT1

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP3_CNT1: 0x4000602D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.541 USB_SIE_EP3_CR0

Propname	Non-control end-point's control Regis-ter

0x4000602eSystem reset for retention flops [reset_all_retention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.542 USB_SIE_EP4_CNT0

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP4_CNT0: 0x4000603C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R	W	NA			R		
Name	data_toggle	data_valid				data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.543 USB_SIE_EP4_CNT1

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP4_CNT1: 0x4000603D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.544 USB_SIE_EP4_CR0

Propname	Non-control end-point's control Regis-ter

0x4000603eSystem reset for retention flops [reset_all_retention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.545 USB_SIE_EP5_CNT0

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP5_CNT0: 0x4000604C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R	W	NA			R		
Name	data_toggle	data_valid				data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.546 USB_SIE_EP5_CNT1

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP5_CNT1: 0x4000604D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.547 USB_SIE_EP5_CR0

Propname	Non-control end-point's control Regis-ter

0x4000604eSystem reset for retention flops [reset_all_retention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.548 USB_SIE_EP6_CNT0

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP6_CNT0: 0x4000605C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R	W	NA			R		
Name	data_toggle	data_valid				data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.549 USB_SIE_EP6_CNT1

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP6_CNT1: 0x4000605D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.550 USB_SIE_EP6_CR0

Propname	Non-control end-point's control Regis-ter

0x4000605eSystem reset for retention flops [reset_all_retention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.551 USB_SIE_EP7_CNT0

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP7_CNT0: 0x4000606C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R	W	NA			R		
Name	data_toggle	data_valid				data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.552 USB_SIE_EP7_CNT1

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP7_CNT1: 0x4000606D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.553 USB_SIE_EP7_CR0

Propname	Non-control end-point's control Regis-ter

0x4000606eSystem reset for retention flops [reset_all_retention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.554 USB_SIE_EP8_CNT0

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP8_CNT0: 0x4000607C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R	W	NA			R		
Name	data_toggle	data_valid				data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.555 USB_SIE_EP8_CNT1

Non-control endpoint count register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_SIE_EP8_CNT1: 0x4000607D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.556 USB_SIE_EP8_CR0

Propname	Non-control end-point's control Regis-ter

0x4000607eSystem reset for retention flops [reset_all_retention]Register : AddressThe Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

1.3.557 USB_ARB_EP1_CFG

Endpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP1_CFG: 0x40006080

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.558 USB_ARB_EP1_INT_EN

Endpoint Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP1_INT_EN: 0x40006081

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.559 USB_ARB_EP1_SR

Endpoint Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP1_SR: 0x40006082

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.560 USB_ARB_RW1_WA

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW1_WA: 0x40006084

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.561 USB_ARB_RW1_WA_MSB

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW1_WA_MSB: 0x40006085

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.562 USB_ARB_RW1_RA

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW1_RA: 0x40006086

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.563 USB_ARB_RW1_RA_MSB

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW1_RA_MSB: 0x40006087

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.564 USB_ARB_RW1_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW1_DR: 0x40006088

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.565 USB_BUF_SIZE

Dedicated Endpoint Buffer Size Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_BUF_SIZE: 0x4000608C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Name	out_buf				in_buf			

Dedicated buffer size for IN and OUT type Endpoints; Encoded power of 2 value; Eg: 1 => 2 bytes; 2 => 4 bytes; 9 => 512 bytes This register is clocked with AHB Bus Clock

Bits	Name	Description
7:4	out_buf[3:0]	Buffer size for OUT Endpoints.
3:0	in_buf[3:0]	Buffer size for IN Endpoints.

1.3.566 USB_EP_ACTIVE

Endpoint Active Indication Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_EP_ACTIVE: 0x4000608E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	ep8_act	ep7_act	ep6_act	ep5_act	ep4_act	ep3_act	ep2_act	ep1_act

Endpoint Active Register; Indicates if an Endpoint is active or not; Required to be programmed only in the case of Automatic Memory Management mode of operation. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_act	Endpoint 8 Active Indication. 0: Inactive. 1: Active
6	ep7_act	Endpoint 7 Active Indication. 0: Inactive. 1: Active
5	ep6_act	Endpoint 6 Active Indication. 0: Inactive. 1: Active
4	ep5_act	Endpoint 5 Active Indication. 0: Inactive. 1: Active
3	ep4_act	Endpoint 4 Active Indication. 0: Inactive. 1: Active
2	ep3_act	Endpoint 3 Active Indication. 0: Inactive. 1: Active
1	ep2_act	Endpoint 2 Active Indication. 0: Inactive. 1: Active
0	ep1_act	Endpoint 1 Active Indication. 0: Inactive. 1: Active

1.3.567 USB_EP_TYPE

Endpoint Type (IN/OUT) Indication

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_EP_TYPE: 0x4000608F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	ep8_typ	ep7_typ	ep6_typ	ep5_typ	ep4_typ	ep3_typ	ep2_typ	ep1_typ

Endpoint Type Register; Indicates the Endpoint Type as IN / OUT. Value is valid if EP_ACTIVE bit is set for the corresponding Endpoint. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_typ	Endpoint 8 Type Indication. 0: IN. 1: OUT
6	ep7_typ	Endpoint 7 Type Indication. 0: IN. 1: OUT
5	ep6_typ	Endpoint 6 Type Indication. 0: IN. 1: OUT
4	ep5_typ	Endpoint 5 Type Indication. 0: IN. 1: OUT
3	ep4_typ	Endpoint 4 Type Indication. 0: IN. 1: OUT
2	ep3_typ	Endpoint 3 Type Indication. 0: IN. 1: OUT
1	ep2_typ	Endpoint 2 Type Indication. 0: IN. 1: OUT
0	ep1_typ	Endpoint 1 Type Indication. 0: IN. 1: OUT

1.3.568 USB_ARB_EP2_CFG

Endpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP2_CFG: 0x40006090

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.569 USB_ARB_EP2_INT_EN

Endpoint Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP2_INT_EN: 0x40006091

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.570 USB_ARB_EP2_SR

Endpoint Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP2_SR: 0x40006092

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.571 USB_ARB_RW2_WA

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW2_WA: 0x40006094

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.572 USB_ARB_RW2_WA_MSB

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW2_WA_MSB: 0x40006095

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.573 USB_ARB_RW2_RA

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW2_RA: 0x40006096

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.574 USB_ARB_RW2_RA_MSB

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW2_RA_MSB: 0x40006097

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.575 USB_ARB_RW2_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW2_DR: 0x40006098

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.576 USB_ARB_CFG

Arbiter Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_CFG: 0x4000609C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:00		R/W:0	NA:0000			
HW Access	R	R		R	NA			
Name	cfg_cmp	dma_cfg		auto_mem				

Arbiter Configuration Register. For MODE I Operation: This register can be left in its default state. For MODE II and MODE III Operation: This register should be programmed. Cfg_cmp bit set to 0 during configuration of PFSUSB Registers. Cfg_cmp bit set to 1 once configuration is complete. This should then be held at 1 during functional mode. Similarly auto_mem and dma_cfg settings are static and should not be modified during block operation. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	cfg_cmp	Register Configuration Complete Indication. Posedge is detected on this bit. Hence a 0 to 1 transition is required. 0: Configuration in progress. 1: Configuration complete.
6:5	dma_cfg[1:0]	DMA Access Configuration. 00: No DMA. 01: Manual DMA. 10: Auto DMA and Manual DMA. 11: Reserved.
4	auto_mem	Auto / Manual Memory Configuration. 0: Manual Memory Config (CPU). 1: Auto Memory Configl

1.3.577 USB_USB_CLK_EN

USB Block Clock Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_USB_CLK_EN: 0x4000609D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								csr_clk_en

USB Block Clock Enable Register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	csr_clk_en	Clock Enable for Core Logic clocked by AHB bus clock

1.3.578 USB_ARB_INT_EN

Arbiter Interrupt Enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_INT_EN: 0x4000609E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	ep8_intr_en	ep7_intr_en	ep6_intr_en	ep5_intr_en	ep4_intr_en	ep3_intr_en	ep2_intr_en	ep1_intr_en

Arbiter Interrupt Enable Register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_intr_en	EP8 Interrupt Enable. 0: Do not raise EP8 Interrupt. 1: Raise EP8 Interrupt
6	ep7_intr_en	EP7 Interrupt Enable. 0: Do not raise EP7 Interrupt. 1: Raise EP7 Interrupt
5	ep6_intr_en	EP6 Interrupt Enable. 0: Do not raise EP6 Interrupt. 1: Raise EP6 Interrupt
4	ep5_intr_en	EP5 Interrupt Enable. 0: Do not raise EP5 Interrupt. 1: Raise EP5 Interrupt
3	ep4_intr_en	EP4 Interrupt Enable. 0: Do not raise EP4 Interrupt. 1: Raise EP4 Interrupt
2	ep3_intr_en	EP3 Interrupt Enable. 0: Do not raise EP3 Interrupt. 1: Raise EP3 Interrupt
1	ep2_intr_en	EP2 Interrupt Enable. 0: Do not raise EP2 Interrupt. 1: Raise EP2 Interrupt
0	ep1_intr_en	EP1 Interrupt Enable. 0: Do not raise EP1 Interrupt. 1: Raise EP1 Interrupt

1.3.579 USB_ARB_INT_SR

Arbiter Interrupt Status

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_INT_SR: 0x4000609F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ep8_intr	ep7_intr	ep6_intr	ep5_intr	ep4_intr	ep3_intr	ep2_intr	ep1_intr

Arbiter Status Register. This is an Interrupt Status Register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_intr	EP8 Interrupt Status. 0: EP8 Interrupt not raised. 1: EP8 Interrupt Present
6	ep7_intr	EP7 Interrupt Status. 0: EP7 Interrupt not raised. 1: EP7 Interrupt Present
5	ep6_intr	EP6 Interrupt Status. 0: EP6 Interrupt not raised. 1: EP6 Interrupt Present
4	ep5_intr	EP5 Interrupt Status. 0: EP5 Interrupt not raised. 1: EP5 Interrupt Present
3	ep4_intr	EP4 Interrupt Status. 0: EP4 Interrupt not raised. 1: EP4 Interrupt Present
2	ep3_intr	EP3 Interrupt Status. 0: EP3 Interrupt not raised. 1: EP3 Interrupt Present
1	ep2_intr	EP2 Interrupt Status. 0: EP2 Interrupt not raised. 1: EP2 Interrupt Present
0	ep1_intr	EP1 Interrupt Status. 0: EP1 Interrupt not raised. 1: EP1 Interrupt Present

1.3.580 USB_ARB_EP3_CFG

Endpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP3_CFG: 0x400060A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.581 USB_ARB_EP3_INT_EN

Endpoint Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP3_INT_EN: 0x400060A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.582 USB_ARB_EP3_SR

Endpoint Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP3_SR: 0x400060A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.583 USB_ARB_RW3_WA

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW3_WA: 0x400060A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.584 USB_ARB_RW3_WA_MSB

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW3_WA_MSB: 0x400060A5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.585 USB_ARB_RW3_RA

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW3_RA: 0x400060A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.586 USB_ARB_RW3_RA_MSB

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW3_RA_MSB: 0x400060A7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.587 USB_ARB_RW3_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW3_DR: 0x400060A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.588 USB_CWA

Common Area Write Address

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_CWA: 0x400060AC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	cwa							

Write Address Pointer for Common Area; LSB 8 bits of the 9 bit pointer are stored in this register. This register is only valid in Mode3 operation. Although it is R/W register for CPU, all intended updates are performed by the block and CPU can access the value for debug purposes. This register will indicate the Common Area location in memory. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	cwa[7:0]	Write Address for Common Area

1.3.589 USB_CWA_MSB

Common Area Write Address

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_CWA_MSB: 0x400060AD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								cwa_msb

Write Address Pointer for Common Area; MSB of the 9 bit pointer are stored in this register. This register is only valid in Mode3 operation. Although it is R/W register for CPU, all intended updates are performed by the block and CPU can access the value for debug purposes. This register will indicate the Common Area location in memory. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	cwa_msb	Write Address for Common Area

1.3.590 USB_ARB_EP4_CFG

Endpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP4_CFG: 0x400060B0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.591 USB_ARB_EP4_INT_EN

Endpoint Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP4_INT_EN: 0x400060B1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.592 USB_ARB_EP4_SR

Endpoint Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP4_SR: 0x400060B2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.593 USB_ARB_RW4_WA

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW4_WA: 0x400060B4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.594 USB_ARB_RW4_WA_MSB

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW4_WA_MSB: 0x400060B5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.595 USB_ARB_RW4_RA

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW4_RA: 0x400060B6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.596 USB_ARB_RW4_RA_MSB

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW4_RA_MSB: 0x400060B7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.597 USB_ARB_RW4_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW4_DR: 0x400060B8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.598 USB_DMA_THRES

DMA Burst / Threshold Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_DMA_THRES: 0x400060BC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	dma_ths							

It contains 8 LSB bits of DMA Threshold Register This register is only valid in Mode3 operation. This register should be programmed to the same value as the DMA Burst Count programmed in the corresponding Channel Basic Config Register in PHUB. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dma_ths[7:0]	8 Lsb bits of 9 bit DMA Threshold count.

1.3.599 USB_DMA_THRES_MSB

DMA Burst / Threshold Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_DMA_THRES_MSB: 0x400060BD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								dma_ths_msb

It contains the MSB bit of DMA Threshold Register This register is clocked with AHB Bus Clock

Bits	Name	Description
0	dma_ths_msb	Msb bit of 9 bit DMA Threshold count.

1.3.600 USB_ARB_EP5_CFG

Endpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP5_CFG: 0x400060C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.601 USB_ARB_EP5_INT_EN

Endpoint Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP5_INT_EN: 0x400060C1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.602 USB_ARB_EP5_SR

Endpoint Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP5_SR: 0x400060C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.603 USB_ARB_RW5_WA

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW5_WA: 0x400060C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.604 USB_ARB_RW5_WA_MSB

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW5_WA_MSB: 0x400060C5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.605 USB_ARB_RW5_RA

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW5_RA: 0x400060C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.606 USB_ARB_RW5_RA_MSB

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW5_RA_MSB: 0x400060C7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.607 USB_ARB_RW5_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW5_DR: 0x400060C8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.608 USB_BUS_RST_CNT

Bus Reset Count Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_BUS_RST_CNT: 0x400060CC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:10	
HW Access	NA						R	
Name							bus_rst_cnt	

Bus Reset Count register ; For USB bus reset length This register is clocked with AHB Bus Clock

Bits	Name	Description
1:0	bus_rst_cnt[1:0]	Bus Reset Count Length

1.3.609 USB_ARB_EP6_CFG

Endpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP6_CFG: 0x400060D0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.610 USB_ARB_EP6_INT_EN

Endpoint Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP6_INT_EN: 0x400060D1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.611 USB_ARB_EP6_SR

Endpoint Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP6_SR: 0x400060D2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.612 USB_ARB_RW6_WA

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW6_WA: 0x400060D4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.613 USB_ARB_RW6_WA_MSB

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW6_WA_MSB: 0x400060D5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.614 USB_ARB_RW6_RA

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW6_RA: 0x400060D6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.615 USB_ARB_RW6_RA_MSB

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW6_RA_MSB: 0x400060D7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.616 USB_ARB_RW6_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW6_DR: 0x400060D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.617 USB_ARB_EP7_CFG

Endpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP7_CFG: 0x400060E0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.618 USB_ARB_EP7_INT_EN

Endpoint Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP7_INT_EN: 0x400060E1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.619 USB_ARB_EP7_SR

Endpoint Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP7_SR: 0x400060E2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.620 USB_ARB_RW7_WA

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW7_WA: 0x400060E4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.621 USB_ARB_RW7_WA_MSB

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW7_WA_MSB: 0x400060E5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.622 USB_ARB_RW7_RA

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW7_RA: 0x400060E6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.623 USB_ARB_RW7_RA_MSB

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW7_RA_MSB: 0x400060E7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.624 USB_ARB_RW7_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW7_DR: 0x400060E8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.625 USB_ARB_EP8_CFG

Endpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP8_CFG: 0x400060F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.626 USB_ARB_EP8_INT_EN

Endpoint Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP8_INT_EN: 0x400060F1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.627 USB_ARB_EP8_SR

Endpoint Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_EP8_SR: 0x400060F2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.628 USB_ARB_RW8_WA

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW8_WA: 0x400060F4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.629 USB_ARB_RW8_WA_MSB

Endpoint Write Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW8_WA_MSB: 0x400060F5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.630 USB_ARB_RW8_RA

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW8_RA: 0x400060F6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.631 USB_ARB_RW8_RA_MSB

Endpoint Read Address value

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_ARB_RW8_RA_MSB: 0x400060F7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.632 USB_ARB_RW8_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW8_DR: 0x400060F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.633 B[0..3]_UDB00_A0

UDB00_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A0: 0x40006400

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.634 B[0..3]_UDB01_A0

UDB01_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A0: 0x40006401

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.635 B[0..3]_UDB02_A0

UDB02_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A0: 0x40006402

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.636 B[0..3]_UDB03_A0

UDB03_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A0: 0x40006403

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.637 B[0..3]_UDB04_A0

UDB04_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A0: 0x40006404 B1_UDB04_A0: 0x40006504

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.638 B[0..3]_UDB05_A0

UDB05_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A0: 0x40006405 B1_UDB05_A0: 0x40006505

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.639 B[0..3]_UDB06_A0

UDB06_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A0: 0x40006406 B1_UDB06_A0: 0x40006506

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.640 B[0..3]_UDB07_A0

UDB07_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A0: 0x40006407 B1_UDB07_A0: 0x40006507

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.641 B[0..3]_UDB08_A0

UDB08_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A0: 0x40006408 B1_UDB08_A0: 0x40006508

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.642 B[0..3]_UDB09_A0

UDB09_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A0: 0x40006409 B1_UDB09_A0: 0x40006509

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.643 B[0..3]_UDB10_A0

UDB10_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A0: 0x4000640A B1_UDB10_A0: 0x4000650A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.644 B[0..3]_UDB11_A0

UDB11_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A0: 0x4000640B B1_UDB11_A0: 0x4000650B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.645 B[0..3]_UDB12_A0

UDB12_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A0: 0x4000640C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.646 B[0..3]_UDB13_A0

UDB13_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A0: 0x4000640D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.647 B[0..3]_UDB14_A0

UDB14_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A0: 0x4000640E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.648 B[0..3]_UDB15_A0

UDB15_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A0: 0x4000640F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.649 B[0..3]_UDB00_A1

UDB00_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A1: 0x40006410

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.650 B[0..3]_UDB01_A1

UDB01_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A1: 0x40006411

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.651 B[0..3]_UDB02_A1

UDB02_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A1: 0x40006412

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.652 B[0..3]_UDB03_A1

UDB03_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A1: 0x40006413

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.653 B[0..3]_UDB04_A1

UDB04_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A1: 0x40006414 B1_UDB04_A1: 0x40006514

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.654 B[0..3]_UDB05_A1

UDB05_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A1: 0x40006415 B1_UDB05_A1: 0x40006515

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.655 B[0..3]_UDB06_A1

UDB06_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A1: 0x40006416 B1_UDB06_A1: 0x40006516

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.656 B[0..3]_UDB07_A1

UDB07_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A1: 0x40006417 B1_UDB07_A1: 0x40006517

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.657 B[0..3]_UDB08_A1

UDB08_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A1: 0x40006418 B1_UDB08_A1: 0x40006518

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.658 B[0..3]_UDB09_A1

UDB09_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A1: 0x40006419 B1_UDB09_A1: 0x40006519

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.659 B[0..3]_UDB10_A1

UDB10_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A1: 0x4000641A B1_UDB10_A1: 0x4000651A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.660 B[0..3]_UDB11_A1

UDB11_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A1: 0x4000641B B1_UDB11_A1: 0x4000651B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.661 B[0..3]_UDB12_A1

UDB12_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A1: 0x4000641C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.662 B[0..3]_UDB13_A1

UDB13_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A1: 0x4000641D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.663 B[0..3]_UDB14_A1

UDB14_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A1: 0x4000641E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.664 B[0..3]_UDB15_A1

UDB15_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A1: 0x4000641F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.665 B[0..3]_UDB00_D0

UDB00_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_D0: 0x40006420

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.666 B[0..3]_UDB01_D0

UDB01_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_D0: 0x40006421

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.667 B[0..3]_UDB02_D0

UDB02_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_D0: 0x40006422

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.668 B[0..3]_UDB03_D0

UDB03_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_D0: 0x40006423

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.669 B[0..3]_UDB04_D0

UDB04_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_D0: 0x40006424 B1_UDB04_D0: 0x40006524

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.670 B[0..3]_UDB05_D0

UDB05_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_D0: 0x40006425 B1_UDB05_D0: 0x40006525

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.671 B[0..3]_UDB06_D0

UDB06_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_D0: 0x40006426 B1_UDB06_D0: 0x40006526

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.672 B[0..3]_UDB07_D0

UDB07_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_D0: 0x40006427 B1_UDB07_D0: 0x40006527

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.673 B[0..3]_UDB08_D0

UDB08_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_D0: 0x40006428 B1_UDB08_D0: 0x40006528

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.674 B[0..3]_UDB09_D0

UDB09_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_D0: 0x40006429 B1_UDB09_D0: 0x40006529

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.675 B[0..3]_UDB10_D0

UDB10_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_D0: 0x4000642A B1_UDB10_D0: 0x4000652A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.676 B[0..3]_UDB11_D0

UDB11_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_D0: 0x4000642B B1_UDB11_D0: 0x4000652B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.677 B[0..3]_UDB12_D0

UDB12_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_D0: 0x4000642C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.678 B[0..3]_UDB13_D0

UDB13_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_D0: 0x4000642D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.679 B[0..3]_UDB14_D0

UDB14_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_D0: 0x4000642E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.680 B[0..3]_UDB15_D0

UDB15_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_D0: 0x4000642F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.681 B[0..3]_UDB00_D1

UDB00_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_D1: 0x40006430

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.682 B[0..3]_UDB01_D1

UDB01_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_D1: 0x40006431

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.683 B[0..3]_UDB02_D1

UDB02_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_D1: 0x40006432

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.684 B[0..3]_UDB03_D1

UDB03_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_D1: 0x40006433

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.685 B[0..3]_UDB04_D1

UDB04_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_D1: 0x40006434 B1_UDB04_D1: 0x40006534

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.686 B[0..3]_UDB05_D1

UDB05_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_D1: 0x40006435 B1_UDB05_D1: 0x40006535

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.687 B[0..3]_UDB06_D1

UDB06_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_D1: 0x40006436 B1_UDB06_D1: 0x40006536

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.688 B[0..3]_UDB07_D1

UDB07_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_D1: 0x40006437 B1_UDB07_D1: 0x40006537

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.689 B[0..3]_UDB08_D1

UDB08_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_D1: 0x40006438 B1_UDB08_D1: 0x40006538

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.690 B[0..3]_UDB09_D1

UDB09_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_D1: 0x40006439 B1_UDB09_D1: 0x40006539

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.691 B[0..3]_UDB10_D1

UDB10_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_D1: 0x4000643A B1_UDB10_D1: 0x4000653A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.692 B[0..3]_UDB11_D1

UDB11_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_D1: 0x4000643B B1_UDB11_D1: 0x4000653B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.693 B[0..3]_UDB12_D1

UDB12_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_D1: 0x4000643C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.694 B[0..3]_UDB13_D1

UDB13_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_D1: 0x4000643D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.695 B[0..3]_UDB14_D1

UDB14_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_D1: 0x4000643E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.696 B[0..3]_UDB15_D1

UDB15_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_D1: 0x4000643F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.697 B[0..3]_UDB00_F0

UDB00_F0

Reset: N/A

Register : Address

B0_UDB00_F0: 0x40006440

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.698 B[0..3]_UDB01_F0

UDB01_F0

Reset: N/A

Register : Address

B0_UDB01_F0: 0x40006441

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.699 B[0..3]_UDB02_F0

UDB02_F0

Reset: N/A

Register : Address

B0_UDB02_F0: 0x40006442

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.700 B[0..3]_UDB03_F0

UDB03_F0

Reset: N/A

Register : Address

B0_UDB03_F0: 0x40006443

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.701 B[0..3]_UDB04_F0

UDB04_F0

Reset: N/A

Register : Address

B0_UDB04_F0: 0x40006444 B1_UDB04_F0: 0x40006544

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.702 B[0..3]_UDB05_F0

UDB05_F0

Reset: N/A

Register : Address

B0_UDB05_F0: 0x40006445 B1_UDB05_F0: 0x40006545

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.703 B[0..3]_UDB06_F0

UDB06_F0

Reset: N/A

Register : Address

B0_UDB06_F0: 0x40006446 B1_UDB06_F0: 0x40006546

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.704 B[0..3]_UDB07_F0

UDB07_F0

Reset: N/A

Register : Address

B0_UDB07_F0: 0x40006447 B1_UDB07_F0: 0x40006547

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.705 B[0..3]_UDB08_F0

UDB08_F0

Reset: N/A

Register : Address

B0_UDB08_F0: 0x40006448 B1_UDB08_F0: 0x40006548

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.706 B[0..3]_UDB09_F0

UDB09_F0

Reset: N/A

Register : Address

B0_UDB09_F0: 0x40006449 B1_UDB09_F0: 0x40006549

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.707 B[0..3]_UDB10_F0

UDB10_F0

Reset: N/A

Register : Address

B0_UDB10_F0: 0x4000644A B1_UDB10_F0: 0x4000654A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.708 B[0..3]_UDB11_F0

UDB11_F0

Reset: N/A

Register : Address

B0_UDB11_F0: 0x4000644B B1_UDB11_F0: 0x4000654B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.709 B[0..3]_UDB12_F0

UDB12_F0

Reset: N/A

Register : Address

B0_UDB12_F0: 0x4000644C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.710 B[0..3]_UDB13_F0

UDB13_F0

Reset: N/A

Register : Address

B0_UDB13_F0: 0x4000644D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.711 B[0..3]_UDB14_F0

UDB14_F0

Reset: N/A

Register : Address

B0_UDB14_F0: 0x4000644E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.712 B[0..3]_UDB15_F0

UDB15_F0

Reset: N/A

Register : Address

B0_UDB15_F0: 0x4000644F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.713 B[0..3]_UDB00_F1

UDB00_F1

Reset: N/A

Register : Address

B0_UDB00_F1: 0x40006450

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.714 B[0..3]_UDB01_F1

UDB01_F1

Reset: N/A

Register : Address

B0_UDB01_F1: 0x40006451

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.715 B[0..3]_UDB02_F1

UDB02_F1

Reset: N/A

Register : Address

B0_UDB02_F1: 0x40006452

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.716 B[0..3]_UDB03_F1

UDB03_F1

Reset: N/A

Register : Address

B0_UDB03_F1: 0x40006453

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.717 B[0..3]_UDB04_F1

UDB04_F1

Reset: N/A

Register : Address

B0_UDB04_F1: 0x40006454 B1_UDB04_F1: 0x40006554

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.718 B[0..3]_UDB05_F1

UDB05_F1

Reset: N/A

Register : Address

B0_UDB05_F1: 0x40006455 B1_UDB05_F1: 0x40006555

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.719 B[0..3]_UDB06_F1

UDB06_F1

Reset: N/A

Register : Address

B0_UDB06_F1: 0x40006456 B1_UDB06_F1: 0x40006556

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.720 B[0..3]_UDB07_F1

UDB07_F1

Reset: N/A

Register : Address

B0_UDB07_F1: 0x40006457 B1_UDB07_F1: 0x40006557

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.721 B[0..3]_UDB08_F1

UDB08_F1

Reset: N/A

Register : Address

B0_UDB08_F1: 0x40006458 B1_UDB08_F1: 0x40006558

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.722 B[0..3]_UDB09_F1

UDB09_F1

Reset: N/A

Register : Address

B0_UDB09_F1: 0x40006459 B1_UDB09_F1: 0x40006559

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.723 B[0..3]_UDB10_F1

UDB10_F1

Reset: N/A

Register : Address

B0_UDB10_F1: 0x4000645A B1_UDB10_F1: 0x4000655A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.724 B[0..3]_UDB11_F1

UDB11_F1

Reset: N/A

Register : Address

B0_UDB11_F1: 0x4000645B B1_UDB11_F1: 0x4000655B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.725 B[0..3]_UDB12_F1

UDB12_F1

Reset: N/A

Register : Address

B0_UDB12_F1: 0x4000645C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.726 B[0..3]_UDB13_F1

UDB13_F1

Reset: N/A

Register : Address

B0_UDB13_F1: 0x4000645D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.727 B[0..3]_UDB14_F1

UDB14_F1

Reset: N/A

Register : Address

B0_UDB14_F1: 0x4000645E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.728 B[0..3]_UDB15_F1

UDB15_F1

Reset: N/A

Register : Address

B0_UDB15_F1: 0x4000645F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.729 B[0..3]_UDB00_ST

UDB00_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_ST: 0x40006460

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.730 B[0..3]_UDB01_ST

UDB01_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_ST: 0x40006461

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.731 B[0..3]_UDB02_ST

UDB02_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_ST: 0x40006462

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.732 B[0..3]_UDB03_ST

UDB03_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_ST: 0x40006463

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.733 B[0..3]_UDB04_ST

UDB04_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_ST: 0x40006464 B1_UDB04_ST: 0x40006564

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.734 B[0..3]_UDB05_ST

UDB05_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_ST: 0x40006465 B1_UDB05_ST: 0x40006565

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.735 B[0..3]_UDB06_ST

UDB06_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_ST: 0x40006466 B1_UDB06_ST: 0x40006566

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.736 B[0..3]_UDB07_ST

UDB07_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_ST: 0x40006467 B1_UDB07_ST: 0x40006567

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.737 B[0..3]_UDB08_ST

UDB08_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_ST: 0x40006468 B1_UDB08_ST: 0x40006568

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.738 B[0..3]_UDB09_ST

UDB09_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_ST: 0x40006469 B1_UDB09_ST: 0x40006569

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.739 B[0..3]_UDB10_ST

UDB10_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_ST: 0x4000646A B1_UDB10_ST: 0x4000656A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.740 B[0..3]_UDB11_ST

UDB11_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_ST: 0x4000646B B1_UDB11_ST: 0x4000656B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.741 B[0..3]_UDB12_ST

UDB12_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_ST: 0x4000646C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.742 B[0..3]_UDB13_ST

UDB13_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_ST: 0x4000646D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.743 B[0..3]_UDB14_ST

UDB14_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_ST: 0x4000646E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.744 B[0..3]_UDB15_ST

UDB15_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_ST: 0x4000646F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.745 B[0..3]_UDB00_CTL

UDB00_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_CTL: 0x40006470

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.746 B[0..3]_UDB01_CTL

UDB01_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_CTL: 0x40006471

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.747 B[0..3]_UDB02_CTL

UDB02_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_CTL: 0x40006472

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.748 B[0..3]_UDB03_CTL

UDB03_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_CTL: 0x40006473

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.749 B[0..3]_UDB04_CTL

UDB04_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_CTL: 0x40006474 B1_UDB04_CTL: 0x40006574

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.750 B[0..3]_UDB05_CTL

UDB05_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_CTL: 0x40006475 B1_UDB05_CTL: 0x40006575

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.751 B[0..3]_UDB06_CTL

UDB06_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_CTL: 0x40006476 B1_UDB06_CTL: 0x40006576

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.752 B[0..3]_UDB07_CTL

UDB07_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_CTL: 0x40006477 B1_UDB07_CTL: 0x40006577

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.753 B[0..3]_UDB08_CTL

UDB08_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_CTL: 0x40006478 B1_UDB08_CTL: 0x40006578

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.754 B[0..3]_UDB09_CTL

UDB09_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_CTL: 0x40006479 B1_UDB09_CTL: 0x40006579

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.755 B[0..3]_UDB10_CTL

UDB10_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_CTL: 0x4000647A B1_UDB10_CTL: 0x4000657A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.756 B[0..3]_UDB11_CTL

UDB11_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_CTL: 0x4000647B B1_UDB11_CTL: 0x4000657B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.757 B[0..3]_UDB12_CTL

UDB12_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_CTL: 0x4000647C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.758 B[0..3]_UDB13_CTL

UDB13_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_CTL: 0x4000647D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.759 B[0..3]_UDB14_CTL

UDB14_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_CTL: 0x4000647E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.760 B[0..3]_UDB15_CTL

UDB15_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_CTL: 0x4000647F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.761 B[0..3]_UDB00_MSK

UDB00_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_MSK: 0x40006480

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.762 B[0..3]_UDB01_MSK

UDB01_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_MSK: 0x40006481

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.763 B[0..3]_UDB02_MSK

UDB02_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_MSK: 0x40006482

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.764 B[0..3]_UDB03_MSK

UDB03_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_MSK: 0x40006483

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.765 B[0..3]_UDB04_MSK

UDB04_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_MSK: 0x40006484 B1_UDB04_MSK: 0x40006584

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.766 B[0..3]_UDB05_MSK

UDB05_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_MSK: 0x40006485 B1_UDB05_MSK: 0x40006585

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.767 B[0..3]_UDB06_MSK

UDB06_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_MSK: 0x40006486 B1_UDB06_MSK: 0x40006586

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.768 B[0..3]_UDB07_MSK

UDB07_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_MSK: 0x40006487 B1_UDB07_MSK: 0x40006587

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.769 B[0..3]_UDB08_MSK

UDB08_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_MSK: 0x40006488 B1_UDB08_MSK: 0x40006588

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.770 B[0..3]_UDB09_MSK

UDB09_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_MSK: 0x40006489 B1_UDB09_MSK: 0x40006589

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.771 B[0..3]_UDB10_MSK

UDB10_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_MSK: 0x4000648A B1_UDB10_MSK: 0x4000658A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.772 B[0..3]_UDB11_MSK

UDB11_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_MSK: 0x4000648B B1_UDB11_MSK: 0x4000658B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.773 B[0..3]_UDB12_MSK

UDB12_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_MSK: 0x4000648C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.774 B[0..3]_UDB13_MSK

UDB13_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_MSK: 0x4000648D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.775 B[0..3]_UDB14_MSK

UDB14_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_MSK: 0x4000648E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.776 B[0..3]_UDB15_MSK

UDB15_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_MSK: 0x4000648F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.777 B[0..3]_UDB00_ACTL

UDB00_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_ACTL: 0x40006490

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-507.
4	INT_EN	(no description) See Table 1-510.
3	FIFO1_LVL	FIFO level See Table 1-509.
2	FIFO0_LVL	FIFO level See Table 1-509.
1	FIFO1_CLR	FIFO clear See Table 1-508.
0	FIFO0_CLR	FIFO clear See Table 1-508.

Table 1-507. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-508. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-509. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-510. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.777 B[0..3]_UDB00_ACTL (continued)

Table 1-510. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.778 B[0..3]_UDB01_ACTL

UDB01_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_ACTL: 0x40006491

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-511.
4	INT_EN	(no description) See Table 1-514.
3	FIFO1_LVL	FIFO level See Table 1-513.
2	FIFO0_LVL	FIFO level See Table 1-513.
1	FIFO1_CLR	FIFO clear See Table 1-512.
0	FIFO0_CLR	FIFO clear See Table 1-512.

Table 1-511. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-512. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-513. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-514. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.778 B[0..3]_UDB01_ACTL (continued)

Table 1-514. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.779 B[0..3]_UDB02_ACTL

UDB02_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_ACTL: 0x40006492

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-515.
4	INT_EN	(no description) See Table 1-518.
3	FIFO1_LVL	FIFO level See Table 1-517.
2	FIFO0_LVL	FIFO level See Table 1-517.
1	FIFO1_CLR	FIFO clear See Table 1-516.
0	FIFO0_CLR	FIFO clear See Table 1-516.

Table 1-515. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-516. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-517. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-518. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.779 B[0..3]_UDB02_ACTL (continued)

Table 1-518. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.780 B[0..3]_UDB03_ACTL

UDB03_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_ACTL: 0x40006493

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-519.
4	INT_EN	(no description) See Table 1-522.
3	FIFO1_LVL	FIFO level See Table 1-521.
2	FIFO0_LVL	FIFO level See Table 1-521.
1	FIFO1_CLR	FIFO clear See Table 1-520.
0	FIFO0_CLR	FIFO clear See Table 1-520.

Table 1-519. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-520. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-521. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-522. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.780 B[0..3]_UDB03_ACTL (continued)

Table 1-522. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.781 B[0..3]_UDB04_ACTL

UDB04_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_ACTL: 0x40006494 B1_UDB04_ACTL: 0x40006594

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-523.
4	INT_EN	(no description) See Table 1-526.
3	FIFO1_LVL	FIFO level See Table 1-525.
2	FIFO0_LVL	FIFO level See Table 1-525.
1	FIFO1_CLR	FIFO clear See Table 1-524.
0	FIFO0_CLR	FIFO clear See Table 1-524.

Table 1-523. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-524. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-525. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-526. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.781 B[0..3]_UDB04_ACTL (continued)

Table 1-526. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.782 B[0..3]_UDB05_ACTL

UDB05_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_ACTL: 0x40006495 B1_UDB05_ACTL: 0x40006595

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-527.
4	INT_EN	(no description) See Table 1-530.
3	FIFO1_LVL	FIFO level See Table 1-529.
2	FIFO0_LVL	FIFO level See Table 1-529.
1	FIFO1_CLR	FIFO clear See Table 1-528.
0	FIFO0_CLR	FIFO clear See Table 1-528.

Table 1-527. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-528. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-529. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-530. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.782 B[0..3]_UDB05_ACTL (continued)

Table 1-530. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.783 B[0..3]_UDB06_ACTL

UDB06_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_ACTL: 0x40006496 B1_UDB06_ACTL: 0x40006596

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-531.
4	INT_EN	(no description) See Table 1-534.
3	FIFO1_LVL	FIFO level See Table 1-533.
2	FIFO0_LVL	FIFO level See Table 1-533.
1	FIFO1_CLR	FIFO clear See Table 1-532.
0	FIFO0_CLR	FIFO clear See Table 1-532.

Table 1-531. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-532. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-533. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-534. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.783 B[0..3]_UDB06_ACTL (continued)

Table 1-534. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.784 B[0..3]_UDB07_ACTL

UDB07_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_ACTL: 0x40006497 B1_UDB07_ACTL: 0x40006597

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-535.
4	INT_EN	(no description) See Table 1-538.
3	FIFO1_LVL	FIFO level See Table 1-537.
2	FIFO0_LVL	FIFO level See Table 1-537.
1	FIFO1_CLR	FIFO clear See Table 1-536.
0	FIFO0_CLR	FIFO clear See Table 1-536.

Table 1-535. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-536. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-537. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-538. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.784 B[0..3]_UDB07_ACTL (continued)

Table 1-538. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.785 B[0..3]_UDB08_ACTL

UDB08_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_ACTL: 0x40006498 B1_UDB08_ACTL: 0x40006598

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-539.
4	INT_EN	(no description) See Table 1-542.
3	FIFO1_LVL	FIFO level See Table 1-541.
2	FIFO0_LVL	FIFO level See Table 1-541.
1	FIFO1_CLR	FIFO clear See Table 1-540.
0	FIFO0_CLR	FIFO clear See Table 1-540.

Table 1-539. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-540. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-541. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-542. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.785 B[0..3]_UDB08_ACTL (continued)

Table 1-542. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.786 B[0..3]_UDB09_ACTL

UDB09_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_ACTL: 0x40006499 B1_UDB09_ACTL: 0x40006599

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-543.
4	INT_EN	(no description) See Table 1-546.
3	FIFO1_LVL	FIFO level See Table 1-545.
2	FIFO0_LVL	FIFO level See Table 1-545.
1	FIFO1_CLR	FIFO clear See Table 1-544.
0	FIFO0_CLR	FIFO clear See Table 1-544.

Table 1-543. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-544. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-545. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-546. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.786 B[0..3]_UDB09_ACTL (continued)

Table 1-546. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.787 B[0..3]_UDB10_ACTL

UDB10_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_ACTL: 0x4000649A B1_UDB10_ACTL: 0x4000659A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-547.
4	INT_EN	(no description) See Table 1-550.
3	FIFO1_LVL	FIFO level See Table 1-549.
2	FIFO0_LVL	FIFO level See Table 1-549.
1	FIFO1_CLR	FIFO clear See Table 1-548.
0	FIFO0_CLR	FIFO clear See Table 1-548.

Table 1-547. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-548. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-549. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-550. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.787 B[0..3]_UDB10_ACTL (continued)

Table 1-550. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.788 B[0..3]_UDB11_ACTL

UDB11_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_ACTL: 0x4000649B B1_UDB11_ACTL: 0x4000659B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-551.
4	INT_EN	(no description) See Table 1-554.
3	FIFO1_LVL	FIFO level See Table 1-553.
2	FIFO0_LVL	FIFO level See Table 1-553.
1	FIFO1_CLR	FIFO clear See Table 1-552.
0	FIFO0_CLR	FIFO clear See Table 1-552.

Table 1-551. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-552. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-553. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-554. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.788 B[0..3]_UDB11_ACTL (continued)

Table 1-554. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.789 B[0..3]_UDB12_ACTL

UDB12_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_ACTL: 0x4000649C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-555.
4	INT_EN	(no description) See Table 1-558.
3	FIFO1_LVL	FIFO level See Table 1-557.
2	FIFO0_LVL	FIFO level See Table 1-557.
1	FIFO1_CLR	FIFO clear See Table 1-556.
0	FIFO0_CLR	FIFO clear See Table 1-556.

Table 1-555. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-556. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-557. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-558. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.789 B[0..3]_UDB12_ACTL (continued)

Table 1-558. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.790 B[0..3]_UDB13_ACTL

UDB13_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_ACTL: 0x4000649D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-559.
4	INT_EN	(no description) See Table 1-562.
3	FIFO1_LVL	FIFO level See Table 1-561.
2	FIFO0_LVL	FIFO level See Table 1-561.
1	FIFO1_CLR	FIFO clear See Table 1-560.
0	FIFO0_CLR	FIFO clear See Table 1-560.

Table 1-559. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-560. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-561. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-562. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.790 B[0..3]_UDB13_ACTL (continued)

Table 1-562. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.791 B[0..3]_UDB14_ACTL

UDB14_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_ACTL: 0x4000649E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-563.
4	INT_EN	(no description) See Table 1-566.
3	FIFO1_LVL	FIFO level See Table 1-565.
2	FIFO0_LVL	FIFO level See Table 1-565.
1	FIFO1_CLR	FIFO clear See Table 1-564.
0	FIFO0_CLR	FIFO clear See Table 1-564.

Table 1-563. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-564. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-565. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-566. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.791 B[0..3]_UDB14_ACTL (continued)

Table 1-566. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.792 B[0..3]_UDB15_ACTL

UDB15_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_ACTL: 0x4000649F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-567.
4	INT_EN	(no description) See Table 1-570.
3	FIFO1_LVL	FIFO level See Table 1-569.
2	FIFO0_LVL	FIFO level See Table 1-569.
1	FIFO1_CLR	FIFO clear See Table 1-568.
0	FIFO0_CLR	FIFO clear See Table 1-568.

Table 1-567. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-568. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-569. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-570. Bit field encoding: E_INT_EN

Value	Name	Description

1.3.792 B[0..3]_UDB15_ACTL (continued)

Table 1-570. Bit field encoding: E_INT_EN

1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.793 B[0..3]_UDB00_MC

UDB00_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_MC: 0x400064A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.794 B[0..3]_UDB01_MC

UDB01_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_MC: 0x400064A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.795 B[0..3]_UDB02_MC

UDB02_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_MC: 0x400064A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.796 B[0..3]_UDB03_MC

UDB03_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_MC: 0x400064A3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.797 B[0..3]_UDB04_MC

UDB04_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_MC: 0x400064A4 B1_UDB04_MC: 0x400065A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.798 B[0..3]_UDB05_MC

UDB05_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_MC: 0x400064A5 B1_UDB05_MC: 0x400065A5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.799 B[0..3]_UDB06_MC

UDB06_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_MC: 0x400064A6 B1_UDB06_MC: 0x400065A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.800 B[0..3]_UDB07_MC

UDB07_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_MC: 0x400064A7 B1_UDB07_MC: 0x400065A7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.801 B[0..3]_UDB08_MC

UDB08_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_MC: 0x400064A8 B1_UDB08_MC: 0x400065A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.802 B[0..3]_UDB09_MC

UDB09_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_MC: 0x400064A9 B1_UDB09_MC: 0x400065A9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.803 B[0..3]_UDB10_MC

UDB10_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_MC: 0x400064AA B1_UDB10_MC: 0x400065AA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.804 B[0..3]_UDB11_MC

UDB11_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_MC: 0x400064AB B1_UDB11_MC: 0x400065AB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.805 B[0..3]_UDB12_MC

UDB12_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_MC: 0x400064AC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.806 B[0..3]_UDB13_MC

UDB13_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_MC: 0x400064AD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.807 B[0..3]_UDB14_MC

UDB14_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_MC: 0x400064AE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.808 B[0..3]_UDB15_MC

UDB15_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_MC: 0x400064AF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.809 B[0..3]_UDB00_01_A0

UDB00_01_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_A0: 0x40006800

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.810 B[0..3]_UDB01_02_A0

UDB01_02_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_A0: 0x40006802

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.811 B[0..3]_UDB02_03_A0

UDB02_03_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_A0: 0x40006804

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.812 B[0..3]_UDB03_04_A0

UDB03_04_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_A0: 0x40006806

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.813 B[0..3]_UDB04_05_A0

UDB04_05_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_A0: 0x40006808 B1_UDB04_05_A0: 0x40006A08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.814 B[0..3]_UDB05_06_A0

UDB05_06_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_A0: 0x4000680A B1_UDB05_06_A0: 0x40006A0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.815 B[0..3]_UDB06_07_A0

UDB06_07_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_A0: 0x4000680C B1_UDB06_07_A0: 0x40006A0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.816 B[0..3]_UDB07_08_A0

UDB07_08_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_A0: 0x4000680E B1_UDB07_08_A0: 0x40006A0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.817 B[0..3]_UDB08_09_A0

UDB08_09_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_A0: 0x40006810 B1_UDB08_09_A0: 0x40006A10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.818 B[0..3]_UDB09_10_A0

UDB09_10_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_A0: 0x40006812 B1_UDB09_10_A0: 0x40006A12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.819 B[0..3]_UDB10_11_A0

UDB10_11_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_A0: 0x40006814 B1_UDB10_11_A0: 0x40006A14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.820 B[0..3]_UDB11_12_A0

UDB11_12_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_A0: 0x40006816 B1_UDB11_12_A0: 0x40006A16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.821 B[0..3]_UDB12_13_A0

UDB12_13_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_A0: 0x40006818

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.822 B[0..3]_UDB13_14_A0

UDB13_14_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_A0: 0x4000681A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.823 B[0..3]_UDB14_15_A0

UDB14_15_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_A0: 0x4000681C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.824 B[0..3]_UDB00_01_A1

UDB00_01_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_A1: 0x40006820

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.825 B[0..3]_UDB01_02_A1

UDB01_02_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_A1: 0x40006822

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.826 B[0..3]_UDB02_03_A1

UDB02_03_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_A1: 0x40006824

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.827 B[0..3]_UDB03_04_A1

UDB03_04_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_A1: 0x40006826

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.828 B[0..3]_UDB04_05_A1

UDB04_05_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_A1: 0x40006828 B1_UDB04_05_A1: 0x40006A28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.829 B[0..3]_UDB05_06_A1

UDB05_06_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_A1: 0x4000682A B1_UDB05_06_A1: 0x40006A2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.830 B[0..3]_UDB06_07_A1

UDB06_07_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_A1: 0x4000682C B1_UDB06_07_A1: 0x40006A2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.831 B[0..3]_UDB07_08_A1

UDB07_08_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_A1: 0x4000682E B1_UDB07_08_A1: 0x40006A2E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.832 B[0..3]_UDB08_09_A1

UDB08_09_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_A1: 0x40006830 B1_UDB08_09_A1: 0x40006A30

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.833 B[0..3]_UDB09_10_A1

UDB09_10_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_A1: 0x40006832 B1_UDB09_10_A1: 0x40006A32

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.834 B[0..3]_UDB10_11_A1

UDB10_11_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_A1: 0x40006834 B1_UDB10_11_A1: 0x40006A34

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.835 B[0..3]_UDB11_12_A1

UDB11_12_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_A1: 0x40006836 B1_UDB11_12_A1: 0x40006A36

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.836 B[0..3]_UDB12_13_A1

UDB12_13_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_A1: 0x40006838

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.837 B[0..3]_UDB13_14_A1

UDB13_14_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_A1: 0x4000683A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.838 B[0..3]_UDB14_15_A1

UDB14_15_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_A1: 0x4000683C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.839 B[0..3]_UDB00_01_D0

UDB00_01_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_D0: 0x40006840

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.840 B[0..3]_UDB01_02_D0

UDB01_02_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_D0: 0x40006842

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.841 B[0..3]_UDB02_03_D0

UDB02_03_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_D0: 0x40006844

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.842 B[0..3]_UDB03_04_D0

UDB03_04_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_D0: 0x40006846

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.843 B[0..3]_UDB04_05_D0

UDB04_05_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_D0: 0x40006848 B1_UDB04_05_D0: 0x40006A48

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.844 B[0..3]_UDB05_06_D0

UDB05_06_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_D0: 0x4000684A B1_UDB05_06_D0: 0x40006A4A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.845 B[0..3]_UDB06_07_D0

UDB06_07_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_D0: 0x4000684C B1_UDB06_07_D0: 0x40006A4C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.846 B[0..3]_UDB07_08_D0

UDB07_08_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_D0: 0x4000684E B1_UDB07_08_D0: 0x40006A4E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.847 B[0..3]_UDB08_09_D0

UDB08_09_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_D0: 0x40006850 B1_UDB08_09_D0: 0x40006A50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.848 B[0..3]_UDB09_10_D0

UDB09_10_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_D0: 0x40006852 B1_UDB09_10_D0: 0x40006A52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.849 B[0..3]_UDB10_11_D0

UDB10_11_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_D0: 0x40006854 B1_UDB10_11_D0: 0x40006A54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.850 B[0..3]_UDB11_12_D0

UDB11_12_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_D0: 0x40006856 B1_UDB11_12_D0: 0x40006A56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.851 B[0..3]_UDB12_13_D0

UDB12_13_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_D0: 0x40006858

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.852 B[0..3]_UDB13_14_D0

UDB13_14_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_D0: 0x4000685A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.853 B[0..3]_UDB14_15_D0

UDB14_15_D0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_D0: 0x4000685C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.854 B[0..3]_UDB00_01_D1

UDB00_01_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_D1: 0x40006860

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.855 B[0..3]_UDB01_02_D1

UDB01_02_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_D1: 0x40006862

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.856 B[0..3]_UDB02_03_D1

UDB02_03_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_D1: 0x40006864

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.857 B[0..3]_UDB03_04_D1

UDB03_04_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_D1: 0x40006866

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.858 B[0..3]_UDB04_05_D1

UDB04_05_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_D1: 0x40006868 B1_UDB04_05_D1: 0x40006A68

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.859 B[0..3]_UDB05_06_D1

UDB05_06_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_D1: 0x4000686A B1_UDB05_06_D1: 0x40006A6A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.860 B[0..3]_UDB06_07_D1

UDB06_07_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_D1: 0x4000686C B1_UDB06_07_D1: 0x40006A6C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.861 B[0..3]_UDB07_08_D1

UDB07_08_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_D1: 0x4000686E B1_UDB07_08_D1: 0x40006A6E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.862 B[0..3]_UDB08_09_D1

UDB08_09_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_D1: 0x40006870 B1_UDB08_09_D1: 0x40006A70

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.863 B[0..3]_UDB09_10_D1

UDB09_10_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_D1: 0x40006872 B1_UDB09_10_D1: 0x40006A72

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.864 B[0..3]_UDB10_11_D1

UDB10_11_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_D1: 0x40006874 B1_UDB10_11_D1: 0x40006A74

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.865 B[0..3]_UDB11_12_D1

UDB11_12_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_D1: 0x40006876 B1_UDB11_12_D1: 0x40006A76

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.866 B[0..3]_UDB12_13_D1

UDB12_13_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_D1: 0x40006878

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.867 B[0..3]_UDB13_14_D1

UDB13_14_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_D1: 0x4000687A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.868 B[0..3]_UDB14_15_D1

UDB14_15_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_D1: 0x4000687C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.869 B[0..3]_UDB00_01_F0

UDB00_01_F0

Reset: N/A

Register : Address

B0_UDB00_01_F0: 0x40006880

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.870 B[0..3]_UDB01_02_F0

UDB01_02_F0

Reset: N/A

Register : Address

B0_UDB01_02_F0: 0x40006882

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.871 B[0..3]_UDB02_03_F0

UDB02_03_F0

Reset: N/A

Register : Address

B0_UDB02_03_F0: 0x40006884

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.872 B[0..3]_UDB03_04_F0

UDB03_04_F0

Reset: N/A

Register : Address

B0_UDB03_04_F0: 0x40006886

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.873 B[0..3]_UDB04_05_F0

UDB04_05_F0

Reset: N/A

Register : Address

B0_UDB04_05_F0: 0x40006888 B1_UDB04_05_F0: 0x40006A88

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.874 B[0..3]_UDB05_06_F0

UDB05_06_F0

Reset: N/A

Register : Address

B0_UDB05_06_F0: 0x4000688A B1_UDB05_06_F0: 0x40006A8A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.875 B[0..3]_UDB06_07_F0

UDB06_07_F0

Reset: N/A

Register : Address

B0_UDB06_07_F0: 0x4000688C B1_UDB06_07_F0: 0x40006A8C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.876 B[0..3]_UDB07_08_F0

UDB07_08_F0

Reset: N/A

Register : Address

B0_UDB07_08_F0: 0x4000688E B1_UDB07_08_F0: 0x40006A8E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.877 B[0..3]_UDB08_09_F0

UDB08_09_F0

Reset: N/A

Register : Address

B0_UDB08_09_F0: 0x40006890 B1_UDB08_09_F0: 0x40006A90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.878 B[0..3]_UDB09_10_F0

UDB09_10_F0

Reset: N/A

Register : Address

B0_UDB09_10_F0: 0x40006892 B1_UDB09_10_F0: 0x40006A92

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.879 B[0..3]_UDB10_11_F0

UDB10_11_F0

Reset: N/A

Register : Address

B0_UDB10_11_F0: 0x40006894 B1_UDB10_11_F0: 0x40006A94

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.880 B[0..3]_UDB11_12_F0

UDB11_12_F0

Reset: N/A

Register : Address

B0_UDB11_12_F0: 0x40006896 B1_UDB11_12_F0: 0x40006A96

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.881 B[0..3]_UDB12_13_F0

UDB12_13_F0

Reset: N/A

Register : Address

B0_UDB12_13_F0: 0x40006898

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.882 B[0..3]_UDB13_14_F0

UDB13_14_F0

Reset: N/A

Register : Address

B0_UDB13_14_F0: 0x4000689A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.883 B[0..3]_UDB14_15_F0

UDB14_15_F0

Reset: N/A

Register : Address

B0_UDB14_15_F0: 0x4000689C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.884 B[0..3]_UDB00_01_F1

UDB00_01_F1

Reset: N/A

Register : Address

B0_UDB00_01_F1: 0x400068A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.885 B[0..3]_UDB01_02_F1

UDB01_02_F1

Reset: N/A

Register : Address

B0_UDB01_02_F1: 0x400068A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.886 B[0..3]_UDB02_03_F1

UDB02_03_F1

Reset: N/A

Register : Address

B0_UDB02_03_F1: 0x400068A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.887 B[0..3]_UDB03_04_F1

UDB03_04_F1

Reset: N/A

Register : Address

B0_UDB03_04_F1: 0x400068A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.888 B[0..3]_UDB04_05_F1

UDB04_05_F1

Reset: N/A

Register : Address

B0_UDB04_05_F1: 0x400068A8 B1_UDB04_05_F1: 0x40006AA8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.889 B[0..3]_UDB05_06_F1

UDB05_06_F1

Reset: N/A

Register : Address

B0_UDB05_06_F1: 0x400068AA B1_UDB05_06_F1: 0x40006AAA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.890 B[0..3]_UDB06_07_F1

UDB06_07_F1

Reset: N/A

Register : Address

B0_UDB06_07_F1: 0x400068AC B1_UDB06_07_F1: 0x40006AAC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.891 B[0..3]_UDB07_08_F1

UDB07_08_F1

Reset: N/A

Register : Address

B0_UDB07_08_F1: 0x400068AE B1_UDB07_08_F1: 0x40006AAE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.892 B[0..3]_UDB08_09_F1

UDB08_09_F1

Reset: N/A

Register : Address

B0_UDB08_09_F1: 0x400068B0 B1_UDB08_09_F1: 0x40006AB0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.893 B[0..3]_UDB09_10_F1

UDB09_10_F1

Reset: N/A

Register : Address

B0_UDB09_10_F1: 0x400068B2 B1_UDB09_10_F1: 0x40006AB2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.894 B[0..3]_UDB10_11_F1

UDB10_11_F1

Reset: N/A

Register : Address

B0_UDB10_11_F1: 0x400068B4 B1_UDB10_11_F1: 0x40006AB4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.895 B[0..3]_UDB11_12_F1

UDB11_12_F1

Reset: N/A

Register : Address

B0_UDB11_12_F1: 0x400068B6 B1_UDB11_12_F1: 0x40006AB6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.896 B[0..3]_UDB12_13_F1

UDB12_13_F1

Reset: N/A

Register : Address

B0_UDB12_13_F1: 0x400068B8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.897 B[0..3]_UDB13_14_F1

UDB13_14_F1

Reset: N/A

Register : Address

B0_UDB13_14_F1: 0x400068BA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.898 B[0..3]_UDB14_15_F1

UDB14_15_F1

Reset: N/A

Register : Address

B0_UDB14_15_F1: 0x400068BC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.899 B[0..3]_UDB00_01_ST

UDB00_01_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_ST: 0x400068C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.900 B[0..3]_UDB01_02_ST

UDB01_02_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_ST: 0x400068C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.901 B[0..3]_UDB02_03_ST

UDB02_03_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_ST: 0x400068C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.902 B[0..3]_UDB03_04_ST

UDB03_04_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_ST: 0x400068C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.903 B[0..3]_UDB04_05_ST

UDB04_05_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_ST: 0x400068C8 B1_UDB04_05_ST: 0x40006AC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.904 B[0..3]_UDB05_06_ST

UDB05_06_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_ST: 0x400068CA B1_UDB05_06_ST: 0x40006ACA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.905 B[0..3]_UDB06_07_ST

UDB06_07_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_ST: 0x400068CC B1_UDB06_07_ST: 0x40006ACC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.906 B[0..3]_UDB07_08_ST

UDB07_08_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_ST: 0x400068CE B1_UDB07_08_ST: 0x40006ACE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.907 B[0..3]_UDB08_09_ST

UDB08_09_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_ST: 0x400068D0 B1_UDB08_09_ST: 0x40006AD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.908 B[0..3]_UDB09_10_ST

UDB09_10_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_ST: 0x400068D2 B1_UDB09_10_ST: 0x40006AD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.909 B[0..3]_UDB10_11_ST

UDB10_11_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_ST: 0x400068D4 B1_UDB10_11_ST: 0x40006AD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.910 B[0..3]_UDB11_12_ST

UDB11_12_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_ST: 0x400068D6 B1_UDB11_12_ST: 0x40006AD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.911 B[0..3]_UDB12_13_ST

UDB12_13_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_ST: 0x400068D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.912 B[0..3]_UDB13_14_ST

UDB13_14_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_ST: 0x400068DA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.913 B[0..3]_UDB14_15_ST

UDB14_15_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_ST: 0x400068DC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.914 B[0..3]_UDB00_01_CTL

UDB00_01_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_CTL: 0x400068E0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.915 B[0..3]_UDB01_02_CTL

UDB01_02_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_CTL: 0x400068E2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.916 B[0..3]_UDB02_03_CTL

UDB02_03_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_CTL: 0x400068E4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.917 B[0..3]_UDB03_04_CTL

UDB03_04_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_CTL: 0x400068E6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.918 B[0..3]_UDB04_05_CTL

UDB04_05_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_CTL: 0x400068E8 B1_UDB04_05_CTL: 0x40006AE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.919 B[0..3]_UDB05_06_CTL

UDB05_06_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_CTL: 0x400068EA B1_UDB05_06_CTL: 0x40006AEA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.920 B[0..3]_UDB06_07_CTL

UDB06_07_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_CTL: 0x400068EC B1_UDB06_07_CTL: 0x40006AEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.921 B[0..3]_UDB07_08_CTL

UDB07_08_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_CTL: 0x400068EE B1_UDB07_08_CTL: 0x40006AEE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.922 B[0..3]_UDB08_09_CTL

UDB08_09_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_CTL: 0x400068F0 B1_UDB08_09_CTL: 0x40006AF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.923 B[0..3]_UDB09_10_CTL

UDB09_10_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_CTL: 0x400068F2 B1_UDB09_10_CTL: 0x40006AF2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.924 B[0..3]_UDB10_11_CTL

UDB10_11_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_CTL: 0x400068F4 B1_UDB10_11_CTL: 0x40006AF4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.925 B[0..3]_UDB11_12_CTL

UDB11_12_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_CTL: 0x400068F6 B1_UDB11_12_CTL: 0x40006AF6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.926 B[0..3]_UDB12_13_CTL

UDB12_13_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_CTL: 0x400068F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.927 B[0..3]_UDB13_14_CTL

UDB13_14_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_CTL: 0x400068FA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.928 B[0..3]_UDB14_15_CTL

UDB14_15_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_CTL: 0x400068FC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.929 B[0..3]_UDB00_01_MSK

UDB00_01_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_MSK: 0x40006900

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.930 B[0..3]_UDB01_02_MSK

UDB01_02_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_MSK: 0x40006902

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.931 B[0..3]_UDB02_03_MSK

UDB02_03_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_MSK: 0x40006904

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.932 B[0..3]_UDB03_04_MSK

UDB03_04_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_MSK: 0x40006906

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.933 B[0..3]_UDB04_05_MSK

UDB04_05_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_MSK: 0x40006908 B1_UDB04_05_MSK: 0x40006B08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.934 B[0..3]_UDB05_06_MSK

UDB05_06_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_MSK: 0x4000690A B1_UDB05_06_MSK: 0x40006B0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.935 B[0..3]_UDB06_07_MSK

UDB06_07_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_MSK: 0x4000690C B1_UDB06_07_MSK: 0x40006B0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.936 B[0..3]_UDB07_08_MSK

UDB07_08_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_MSK: 0x4000690E B1_UDB07_08_MSK: 0x40006B0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.937 B[0..3]_UDB08_09_MSK

UDB08_09_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_MSK: 0x40006910 B1_UDB08_09_MSK: 0x40006B10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.938 B[0..3]_UDB09_10_MSK

UDB09_10_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_MSK: 0x40006912 B1_UDB09_10_MSK: 0x40006B12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.939 B[0..3]_UDB10_11_MSK

UDB10_11_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_MSK: 0x40006914 B1_UDB10_11_MSK: 0x40006B14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.940 B[0..3]_UDB11_12_MSK

UDB11_12_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_MSK: 0x40006916 B1_UDB11_12_MSK: 0x40006B16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.941 B[0..3]_UDB12_13_MSK

UDB12_13_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_MSK: 0x40006918

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.942 B[0..3]_UDB13_14_MSK

UDB13_14_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_MSK: 0x4000691A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.943 B[0..3]_UDB14_15_MSK

UDB14_15_MSK

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_MSK: 0x4000691C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.944 B[0..3]_UDB00_01_ACTL

UDB00_01_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_ACTL: 0x40006920

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-571.
12	INT_EN_MS	(no description) See Table 1-574.
11	FIFO1_LVL_MS	FIFO level See Table 1-573.
10	FIFO0_LVL_MS	FIFO level See Table 1-573.
9	FIFO1_CLR_MS	FIFO clear See Table 1-572.
8	FIFO0_CLR_MS	FIFO clear See Table 1-572.
5	CNT_START_LS	FIFO0 clear See Table 1-571.
4	INT_EN_LS	(no description) See Table 1-574.
3	FIFO1_LVL_LS	FIFO level See Table 1-573.

1.3.944 B[0..3]_UDB00_01_ACTL (continued)

2	FIFO0_LVL_LS	FIFO level See Table 1-573.
1	FIFO1_CLR_LS	FIFO clear See Table 1-572.
0	FIFO0_CLR_LS	FIFO clear See Table 1-572.

Table 1-571. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-572. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-573. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-574. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.945 B[0..3]_UDB01_02_ACTL

UDB01_02_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_ACTL: 0x40006922

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-575.
12	INT_EN_MS	(no description) See Table 1-578.
11	FIFO1_LVL_MS	FIFO level See Table 1-577.
10	FIFO0_LVL_MS	FIFO level See Table 1-577.
9	FIFO1_CLR_MS	FIFO clear See Table 1-576.
8	FIFO0_CLR_MS	FIFO clear See Table 1-576.
5	CNT_START_LS	FIFO0 clear See Table 1-575.
4	INT_EN_LS	(no description) See Table 1-578.
3	FIFO1_LVL_LS	FIFO level See Table 1-577.

1.3.945 B[0..3]_UDB01_02_ACTL (continued)

2	FIFO0_LVL_LS	FIFO level See Table 1-577.
1	FIFO1_CLR_LS	FIFO clear See Table 1-576.
0	FIFO0_CLR_LS	FIFO clear See Table 1-576.

Table 1-575. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-576. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-577. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-578. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.946 B[0..3]_UDB02_03_ACTL

UDB02_03_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_ACTL: 0x40006924

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-579.
12	INT_EN_MS	(no description) See Table 1-582.
11	FIFO1_LVL_MS	FIFO level See Table 1-581.
10	FIFO0_LVL_MS	FIFO level See Table 1-581.
9	FIFO1_CLR_MS	FIFO clear See Table 1-580.
8	FIFO0_CLR_MS	FIFO clear See Table 1-580.
5	CNT_START_LS	FIFO0 clear See Table 1-579.
4	INT_EN_LS	(no description) See Table 1-582.
3	FIFO1_LVL_LS	FIFO level See Table 1-581.

1.3.946 B[0..3]_UDB02_03_ACTL (continued)

2	FIFO0_LVL_LS	FIFO level See Table 1-581.
1	FIFO1_CLR_LS	FIFO clear See Table 1-580.
0	FIFO0_CLR_LS	FIFO clear See Table 1-580.

Table 1-579. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-580. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-581. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-582. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.947 B[0..3]_UDB03_04_ACTL

UDB03_04_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_ACTL: 0x40006926

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-583.
12	INT_EN_MS	(no description) See Table 1-586.
11	FIFO1_LVL_MS	FIFO level See Table 1-585.
10	FIFO0_LVL_MS	FIFO level See Table 1-585.
9	FIFO1_CLR_MS	FIFO clear See Table 1-584.
8	FIFO0_CLR_MS	FIFO clear See Table 1-584.
5	CNT_START_LS	FIFO0 clear See Table 1-583.
4	INT_EN_LS	(no description) See Table 1-586.
3	FIFO1_LVL_LS	FIFO level See Table 1-585.

1.3.947 B[0..3]_UDB03_04_ACTL (continued)

2	FIFO0_LVL_LS	FIFO level See Table 1-585.
1	FIFO1_CLR_LS	FIFO clear See Table 1-584.
0	FIFO0_CLR_LS	FIFO clear See Table 1-584.

Table 1-583. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-584. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-585. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-586. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.948 B[0..3]_UDB04_05_ACTL

UDB04_05_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_ACTL: 0x40006928

B1_UDB04_05_ACTL: 0x40006B28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-587.
12	INT_EN_MS	(no description) See Table 1-590.
11	FIFO1_LVL_MS	FIFO level See Table 1-589.
10	FIFO0_LVL_MS	FIFO level See Table 1-589.
9	FIFO1_CLR_MS	FIFO clear See Table 1-588.
8	FIFO0_CLR_MS	FIFO clear See Table 1-588.
5	CNT_START_LS	FIFO0 clear See Table 1-587.
4	INT_EN_LS	(no description) See Table 1-590.

1.3.948 B[0..3]_UDB04_05_ACTL (continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-589.
2	FIFO0_LVL_LS	FIFO level See Table 1-589.
1	FIFO1_CLR_LS	FIFO clear See Table 1-588.
0	FIFO0_CLR_LS	FIFO clear See Table 1-588.

Table 1-587. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-588. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-589. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-590. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.949 B[0..3]_UDB05_06_ACTL

UDB05_06_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_ACTL: 0x4000692A

B1_UDB05_06_ACTL: 0x40006B2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-591.
12	INT_EN_MS	(no description) See Table 1-594.
11	FIFO1_LVL_MS	FIFO level See Table 1-593.
10	FIFO0_LVL_MS	FIFO level See Table 1-593.
9	FIFO1_CLR_MS	FIFO clear See Table 1-592.
8	FIFO0_CLR_MS	FIFO clear See Table 1-592.
5	CNT_START_LS	FIFO0 clear See Table 1-591.
4	INT_EN_LS	(no description) See Table 1-594.

1.3.949 B[0..3]_UDB05_06_ACTL (continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-593.
2	FIFO0_LVL_LS	FIFO level See Table 1-593.
1	FIFO1_CLR_LS	FIFO clear See Table 1-592.
0	FIFO0_CLR_LS	FIFO clear See Table 1-592.

Table 1-591. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-592. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-593. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-594. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.950 B[0..3]_UDB06_07_ACTL

UDB06_07_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_ACTL: 0x4000692C

B1_UDB06_07_ACTL: 0x40006B2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-595.
12	INT_EN_MS	(no description) See Table 1-598.
11	FIFO1_LVL_MS	FIFO level See Table 1-597.
10	FIFO0_LVL_MS	FIFO level See Table 1-597.
9	FIFO1_CLR_MS	FIFO clear See Table 1-596.
8	FIFO0_CLR_MS	FIFO clear See Table 1-596.
5	CNT_START_LS	FIFO0 clear See Table 1-595.
4	INT_EN_LS	(no description) See Table 1-598.

1.3.950 B[0..3]_UDB06_07_ACTL (continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-597.
2	FIFO0_LVL_LS	FIFO level See Table 1-597.
1	FIFO1_CLR_LS	FIFO clear See Table 1-596.
0	FIFO0_CLR_LS	FIFO clear See Table 1-596.

Table 1-595. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-596. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-597. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-598. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.951 B[0..3]_UDB07_08_ACTL

UDB07_08_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_ACTL: 0x4000692E

B1_UDB07_08_ACTL: 0x40006B2E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-599.
12	INT_EN_MS	(no description) See Table 1-602.
11	FIFO1_LVL_MS	FIFO level See Table 1-601.
10	FIFO0_LVL_MS	FIFO level See Table 1-601.
9	FIFO1_CLR_MS	FIFO clear See Table 1-600.
8	FIFO0_CLR_MS	FIFO clear See Table 1-600.
5	CNT_START_LS	FIFO0 clear See Table 1-599.
4	INT_EN_LS	(no description) See Table 1-602.

1.3.951 B[0..3]_UDB07_08_ACTL (continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-601.
2	FIFO0_LVL_LS	FIFO level See Table 1-601.
1	FIFO1_CLR_LS	FIFO clear See Table 1-600.
0	FIFO0_CLR_LS	FIFO clear See Table 1-600.

Table 1-599. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-600. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-601. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-602. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.952 B[0..3]_UDB08_09_ACTL

UDB08_09_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_ACTL: 0x40006930

B1_UDB08_09_ACTL: 0x40006B30

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-603.
12	INT_EN_MS	(no description) See Table 1-606.
11	FIFO1_LVL_MS	FIFO level See Table 1-605.
10	FIFO0_LVL_MS	FIFO level See Table 1-605.
9	FIFO1_CLR_MS	FIFO clear See Table 1-604.
8	FIFO0_CLR_MS	FIFO clear See Table 1-604.
5	CNT_START_LS	FIFO0 clear See Table 1-603.
4	INT_EN_LS	(no description) See Table 1-606.

1.3.952 B[0..3]_UDB08_09_ACTL (continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-605.
2	FIFO0_LVL_LS	FIFO level See Table 1-605.
1	FIFO1_CLR_LS	FIFO clear See Table 1-604.
0	FIFO0_CLR_LS	FIFO clear See Table 1-604.

Table 1-603. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-604. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-605. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-606. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.953 B[0..3]_UDB09_10_ACTL

UDB09_10_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_ACTL: 0x40006932

B1_UDB09_10_ACTL: 0x40006B32

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-607.
12	INT_EN_MS	(no description) See Table 1-610.
11	FIFO1_LVL_MS	FIFO level See Table 1-609.
10	FIFO0_LVL_MS	FIFO level See Table 1-609.
9	FIFO1_CLR_MS	FIFO clear See Table 1-608.
8	FIFO0_CLR_MS	FIFO clear See Table 1-608.
5	CNT_START_LS	FIFO0 clear See Table 1-607.
4	INT_EN_LS	(no description) See Table 1-610.

1.3.953 B[0..3]_UDB09_10_ACTL (continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-609.
2	FIFO0_LVL_LS	FIFO level See Table 1-609.
1	FIFO1_CLR_LS	FIFO clear See Table 1-608.
0	FIFO0_CLR_LS	FIFO clear See Table 1-608.

Table 1-607. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-608. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-609. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-610. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.954 B[0..3]_UDB10_11_ACTL

UDB10_11_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_ACTL: 0x40006934

B1_UDB10_11_ACTL: 0x40006B34

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-611.
12	INT_EN_MS	(no description) See Table 1-614.
11	FIFO1_LVL_MS	FIFO level See Table 1-613.
10	FIFO0_LVL_MS	FIFO level See Table 1-613.
9	FIFO1_CLR_MS	FIFO clear See Table 1-612.
8	FIFO0_CLR_MS	FIFO clear See Table 1-612.
5	CNT_START_LS	FIFO0 clear See Table 1-611.
4	INT_EN_LS	(no description) See Table 1-614.

1.3.954 B[0..3]_UDB10_11_ACTL (continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-613.
2	FIFO0_LVL_LS	FIFO level See Table 1-613.
1	FIFO1_CLR_LS	FIFO clear See Table 1-612.
0	FIFO0_CLR_LS	FIFO clear See Table 1-612.

Table 1-611. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-612. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-613. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-614. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.955 B[0..3]_UDB11_12_ACTL

UDB11_12_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_ACTL: 0x40006936

B1_UDB11_12_ACTL: 0x40006B36

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-615.
12	INT_EN_MS	(no description) See Table 1-618.
11	FIFO1_LVL_MS	FIFO level See Table 1-617.
10	FIFO0_LVL_MS	FIFO level See Table 1-617.
9	FIFO1_CLR_MS	FIFO clear See Table 1-616.
8	FIFO0_CLR_MS	FIFO clear See Table 1-616.
5	CNT_START_LS	FIFO0 clear See Table 1-615.
4	INT_EN_LS	(no description) See Table 1-618.

1.3.955 B[0..3]_UDB11_12_ACTL (continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-617.
2	FIFO0_LVL_LS	FIFO level See Table 1-617.
1	FIFO1_CLR_LS	FIFO clear See Table 1-616.
0	FIFO0_CLR_LS	FIFO clear See Table 1-616.

Table 1-615. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-616. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-617. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-618. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.956 B[0..3]_UDB12_13_ACTL

UDB12_13_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_ACTL: 0x40006938

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-619.
12	INT_EN_MS	(no description) See Table 1-622.
11	FIFO1_LVL_MS	FIFO level See Table 1-621.
10	FIFO0_LVL_MS	FIFO level See Table 1-621.
9	FIFO1_CLR_MS	FIFO clear See Table 1-620.
8	FIFO0_CLR_MS	FIFO clear See Table 1-620.
5	CNT_START_LS	FIFO0 clear See Table 1-619.
4	INT_EN_LS	(no description) See Table 1-622.
3	FIFO1_LVL_LS	FIFO level See Table 1-621.

1.3.956 B[0..3]_UDB12_13_ACTL (continued)

2	FIFO0_LVL_LS	FIFO level See Table 1-621.
1	FIFO1_CLR_LS	FIFO clear See Table 1-620.
0	FIFO0_CLR_LS	FIFO clear See Table 1-620.

Table 1-619. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-620. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-621. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-622. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.957 B[0..3]_UDB13_14_ACTL

UDB13_14_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_ACTL: 0x4000693A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-623.
12	INT_EN_MS	(no description) See Table 1-626.
11	FIFO1_LVL_MS	FIFO level See Table 1-625.
10	FIFO0_LVL_MS	FIFO level See Table 1-625.
9	FIFO1_CLR_MS	FIFO clear See Table 1-624.
8	FIFO0_CLR_MS	FIFO clear See Table 1-624.
5	CNT_START_LS	FIFO0 clear See Table 1-623.
4	INT_EN_LS	(no description) See Table 1-626.
3	FIFO1_LVL_LS	FIFO level See Table 1-625.

1.3.957 B[0..3]_UDB13_14_ACTL (continued)

2	FIFO0_LVL_LS	FIFO level See Table 1-625.
1	FIFO1_CLR_LS	FIFO clear See Table 1-624.
0	FIFO0_CLR_LS	FIFO clear See Table 1-624.

Table 1-623. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-624. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-625. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-626. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.958 B[0..3]_UDB14_15_ACTL

UDB14_15_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_ACTL: 0x4000693C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-627.
12	INT_EN_MS	(no description) See Table 1-630.
11	FIFO1_LVL_MS	FIFO level See Table 1-629.
10	FIFO0_LVL_MS	FIFO level See Table 1-629.
9	FIFO1_CLR_MS	FIFO clear See Table 1-628.
8	FIFO0_CLR_MS	FIFO clear See Table 1-628.
5	CNT_START_LS	FIFO0 clear See Table 1-627.
4	INT_EN_LS	(no description) See Table 1-630.
3	FIFO1_LVL_LS	FIFO level See Table 1-629.

1.3.958 B[0..3]_UDB14_15_ACTL (continued)

2	FIFO0_LVL_LS	FIFO level See Table 1-629.
1	FIFO1_CLR_LS	FIFO clear See Table 1-628.
0	FIFO0_CLR_LS	FIFO clear See Table 1-628.

Table 1-627. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-628. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-629. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-630. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.959 B[0..3]_UDB00_01_MC

UDB00_01_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_MC: 0x40006940

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.960 B[0..3]_UDB01_02_MC

UDB01_02_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_MC: 0x40006942

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.961 B[0..3]_UDB02_03_MC

UDB02_03_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_MC: 0x40006944

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.962 B[0..3]_UDB03_04_MC

UDB03_04_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_MC: 0x40006946

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.963 B[0..3]_UDB04_05_MC

UDB04_05_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_MC: 0x40006948 B1_UDB04_05_MC: 0x40006B48

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.964 B[0..3]_UDB05_06_MC

UDB05_06_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_MC: 0x4000694A B1_UDB05_06_MC: 0x40006B4A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.965 B[0..3]_UDB06_07_MC

UDB06_07_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_MC: 0x4000694C B1_UDB06_07_MC: 0x40006B4C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.966 B[0..3]_UDB07_08_MC

UDB07_08_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_MC: 0x4000694E B1_UDB07_08_MC: 0x40006B4E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.967 B[0..3]_UDB08_09_MC

UDB08_09_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_MC: 0x40006950 B1_UDB08_09_MC: 0x40006B50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.968 B[0..3]_UDB09_10_MC

UDB09_10_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_MC: 0x40006952 B1_UDB09_10_MC: 0x40006B52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.969 B[0..3]_UDB10_11_MC

UDB10_11_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_MC: 0x40006954 B1_UDB10_11_MC: 0x40006B54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.970 B[0..3]_UDB11_12_MC

UDB11_12_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_MC: 0x40006956 B1_UDB11_12_MC: 0x40006B56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.971 B[0..3]_UDB12_13_MC

UDB12_13_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_MC: 0x40006958

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.972 B[0..3]_UDB13_14_MC

UDB13_14_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_MC: 0x4000695A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.973 B[0..3]_UDB14_15_MC

UDB14_15_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_MC: 0x4000695C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.974 B[0..3]_UDB00_A0_A1

UDB00_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A0_A1: 0x40006800

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.975 B[0..3]_UDB01_A0_A1

UDB01_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A0_A1: 0x40006802

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.976 B[0..3]_UDB02_A0_A1

UDB02_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A0_A1: 0x40006804

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.977 B[0..3]_UDB03_A0_A1

UDB03_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A0_A1: 0x40006806

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.978 B[0..3]_UDB04_A0_A1

UDB04_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A0_A1: 0x40006808 B1_UDB04_A0_A1: 0x40006A08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.979 B[0..3]_UDB05_A0_A1

UDB05_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A0_A1: 0x4000680A B1_UDB05_A0_A1: 0x40006A0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.980 B[0..3]_UDB06_A0_A1

UDB06_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A0_A1: 0x4000680C B1_UDB06_A0_A1: 0x40006A0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.981 B[0..3]_UDB07_A0_A1

UDB07_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A0_A1: 0x4000680E B1_UDB07_A0_A1: 0x40006A0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.982 B[0..3]_UDB08_A0_A1

UDB08_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A0_A1: 0x40006810 B1_UDB08_A0_A1: 0x40006A10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.983 B[0..3]_UDB09_A0_A1

UDB09_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A0_A1: 0x40006812 B1_UDB09_A0_A1: 0x40006A12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.984 B[0..3]_UDB10_A0_A1

UDB10_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A0_A1: 0x40006814 B1_UDB10_A0_A1: 0x40006A14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.985 B[0..3]_UDB11_A0_A1

UDB11_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A0_A1: 0x40006816 B1_UDB11_A0_A1: 0x40006A16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.986 B[0..3]_UDB12_A0_A1

UDB12_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A0_A1: 0x40006818

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.987 B[0..3]_UDB13_A0_A1

UDB13_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A0_A1: 0x4000681A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.988 B[0..3]_UDB14_A0_A1

UDB14_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A0_A1: 0x4000681C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.989 B[0..3]_UDB15_A0_A1

UDB15_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A0_A1: 0x4000681E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.990 B[0..3]_UDB00_D0_D1

UDB00_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_D0_D1: 0x40006840

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.991 B[0..3]_UDB01_D0_D1

UDB01_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_D0_D1: 0x40006842

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.992 B[0..3]_UDB02_D0_D1

UDB02_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_D0_D1: 0x40006844

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.993 B[0..3]_UDB03_D0_D1

UDB03_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_D0_D1: 0x40006846

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.994 B[0..3]_UDB04_D0_D1

UDB04_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_D0_D1: 0x40006848 B1_UDB04_D0_D1: 0x40006A48

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.995 B[0..3]_UDB05_D0_D1

UDB05_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_D0_D1: 0x4000684A B1_UDB05_D0_D1: 0x40006A4A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.996 B[0..3]_UDB06_D0_D1

UDB06_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_D0_D1: 0x4000684C B1_UDB06_D0_D1: 0x40006A4C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.997 B[0..3]_UDB07_D0_D1

UDB07_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_D0_D1: 0x4000684E B1_UDB07_D0_D1: 0x40006A4E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.998 B[0..3]_UDB08_D0_D1

UDB08_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_D0_D1: 0x40006850 B1_UDB08_D0_D1: 0x40006A50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.999 B[0..3]_UDB09_D0_D1

UDB09_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_D0_D1: 0x40006852 B1_UDB09_D0_D1: 0x40006A52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1000 B[0..3]_UDB10_D0_D1

UDB10_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_D0_D1: 0x40006854 B1_UDB10_D0_D1: 0x40006A54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1001 B[0..3]_UDB11_D0_D1

UDB11_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_D0_D1: 0x40006856 B1_UDB11_D0_D1: 0x40006A56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1002 B[0..3]_UDB12_D0_D1

UDB12_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_D0_D1: 0x40006858

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1003 B[0..3]_UDB13_D0_D1

UDB13_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_D0_D1: 0x4000685A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1004 B[0..3]_UDB14_D0_D1

UDB14_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_D0_D1: 0x4000685C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1005 B[0..3]_UDB15_D0_D1

UDB15_D0_D1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_D0_D1: 0x4000685E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1006 B[0..3]_UDB00_F0_F1

UDB00_F0_F1

Reset: N/A

Register : Address

B0_UDB00_F0_F1: 0x40006880

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1007 B[0..3]_UDB01_F0_F1

UDB01_F0_F1

Reset: N/A

Register : Address

B0_UDB01_F0_F1: 0x40006882

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1008 B[0..3]_UDB02_F0_F1

UDB02_F0_F1

Reset: N/A

Register : Address

B0_UDB02_F0_F1: 0x40006884

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1009 B[0..3]_UDB03_F0_F1

UDB03_F0_F1

Reset: N/A

Register : Address

B0_UDB03_F0_F1: 0x40006886

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1010 B[0..3]_UDB04_F0_F1

UDB04_F0_F1

Reset: N/A

Register : Address

B0_UDB04_F0_F1: 0x40006888 B1_UDB04_F0_F1: 0x40006A88

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1011 B[0..3]_UDB05_F0_F1

UDB05_F0_F1

Reset: N/A

Register : Address

B0_UDB05_F0_F1: 0x4000688A B1_UDB05_F0_F1: 0x40006A8A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1012 B[0..3]_UDB06_F0_F1

UDB06_F0_F1

Reset: N/A

Register : Address

B0_UDB06_F0_F1: 0x4000688C B1_UDB06_F0_F1: 0x40006A8C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1013 B[0..3]_UDB07_F0_F1

UDB07_F0_F1

Reset: N/A

Register : Address

B0_UDB07_F0_F1: 0x4000688E B1_UDB07_F0_F1: 0x40006A8E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1014 B[0..3]_UDB08_F0_F1

UDB08_F0_F1

Reset: N/A

Register : Address

B0_UDB08_F0_F1: 0x40006890 B1_UDB08_F0_F1: 0x40006A90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1015 B[0..3]_UDB09_F0_F1

UDB09_F0_F1

Reset: N/A

Register : Address

B0_UDB09_F0_F1: 0x40006892 B1_UDB09_F0_F1: 0x40006A92

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1016 B[0..3]_UDB10_F0_F1

UDB10_F0_F1

Reset: N/A

Register : Address

B0_UDB10_F0_F1: 0x40006894 B1_UDB10_F0_F1: 0x40006A94

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1017 B[0..3]_UDB11_F0_F1

UDB11_F0_F1

Reset: N/A

Register : Address

B0_UDB11_F0_F1: 0x40006896 B1_UDB11_F0_F1: 0x40006A96

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1018 B[0..3]_UDB12_F0_F1

UDB12_F0_F1

Reset: N/A

Register : Address

B0_UDB12_F0_F1: 0x40006898

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1019 B[0..3]_UDB13_F0_F1

UDB13_F0_F1

Reset: N/A

Register : Address

B0_UDB13_F0_F1: 0x4000689A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1020 B[0..3]_UDB14_F0_F1

UDB14_F0_F1

Reset: N/A

Register : Address

B0_UDB14_F0_F1: 0x4000689C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1021 B[0..3]_UDB15_F0_F1

UDB15_F0_F1

Reset: N/A

Register : Address

B0_UDB15_F0_F1: 0x4000689E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1022 B[0..3]_UDB00_ST_CTL

UDB00_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_ST_CTL: 0x400068C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1023 B[0..3]_UDB01_ST_CTL

UDB01_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_ST_CTL: 0x400068C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1024 B[0..3]_UDB02_ST_CTL

UDB02_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_ST_CTL: 0x400068C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1025 B[0..3]_UDB03_ST_CTL

UDB03_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_ST_CTL: 0x400068C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1026 B[0..3]_UDB04_ST_CTL

UDB04_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_ST_CTL: 0x400068C8 B1_UDB04_ST_CTL: 0x40006AC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1027 B[0..3]_UDB05_ST_CTL

UDB05_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_ST_CTL: 0x400068CA B1_UDB05_ST_CTL: 0x40006ACA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1028 B[0..3]_UDB06_ST_CTL

UDB06_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_ST_CTL: 0x400068CC B1_UDB06_ST_CTL: 0x40006ACC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1029 B[0..3]_UDB07_ST_CTL

UDB07_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_ST_CTL: 0x400068CE B1_UDB07_ST_CTL: 0x40006ACE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1030 B[0..3]_UDB08_ST_CTL

UDB08_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_ST_CTL: 0x400068D0 B1_UDB08_ST_CTL: 0x40006AD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1031 B[0..3]_UDB09_ST_CTL

UDB09_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_ST_CTL: 0x400068D2 B1_UDB09_ST_CTL: 0x40006AD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1032 B[0..3]_UDB10_ST_CTL

UDB10_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_ST_CTL: 0x400068D4 B1_UDB10_ST_CTL: 0x40006AD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1033 B[0..3]_UDB11_ST_CTL

UDB11_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_ST_CTL: 0x400068D6 B1_UDB11_ST_CTL: 0x40006AD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1034 B[0..3]_UDB12_ST_CTL

UDB12_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_ST_CTL: 0x400068D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1035 B[0..3]_UDB13_ST_CTL

UDB13_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_ST_CTL: 0x400068DA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1036 B[0..3]_UDB14_ST_CTL

UDB14_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_ST_CTL: 0x400068DC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1037 B[0..3]_UDB15_ST_CTL

UDB15_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_ST_CTL: 0x400068DE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1038 B[0..3]_UDB00_MSK_ACTL

UDB00_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_MSK_ACTL: 0x40006900

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-631.
12	INT_EN	(no description) See Table 1-634.
11	FIFO1_LVL	FIFO level See Table 1-633.
10	FIFO0_LVL	FIFO level See Table 1-633.
9	FIFO1_CLR	FIFO clear See Table 1-632.
8	FIFO0_CLR	FIFO clear See Table 1-632.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-631. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-632. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

1.3.1038 B[0..3]_UDB00_MSK_ACTL (continued)

Table 1-633. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-634. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1039 B[0..3]_UDB01_MSK_ACTL

UDB01_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_MSK_ACTL: 0x40006902

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-635.
12	INT_EN	(no description) See Table 1-638.
11	FIFO1_LVL	FIFO level See Table 1-637.
10	FIFO0_LVL	FIFO level See Table 1-637.
9	FIFO1_CLR	FIFO clear See Table 1-636.
8	FIFO0_CLR	FIFO clear See Table 1-636.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-635. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-636. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

1.3.1039 B[0..3]_UDB01_MSK_ACTL (continued)

Table 1-637. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-638. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1040 B[0..3]_UDB02_MSK_ACTL

UDB02_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_MSK_ACTL: 0x40006904

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-639.
12	INT_EN	(no description) See Table 1-642.
11	FIFO1_LVL	FIFO level See Table 1-641.
10	FIFO0_LVL	FIFO level See Table 1-641.
9	FIFO1_CLR	FIFO clear See Table 1-640.
8	FIFO0_CLR	FIFO clear See Table 1-640.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-639. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-640. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

1.3.1040 B[0..3]_UDB02_MSK_ACTL (continued)

Table 1-641. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-642. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1041 B[0..3]_UDB03_MSK_ACTL

UDB03_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_MSK_ACTL: 0x40006906

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-643.
12	INT_EN	(no description) See Table 1-646.
11	FIFO1_LVL	FIFO level See Table 1-645.
10	FIFO0_LVL	FIFO level See Table 1-645.
9	FIFO1_CLR	FIFO clear See Table 1-644.
8	FIFO0_CLR	FIFO clear See Table 1-644.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-643. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-644. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

1.3.1041 B[0..3]_UDB03_MSK_ACTL (continued)

Table 1-645. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-646. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1042 B[0..3]_UDB04_MSK_ACTL

UDB04_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_MSK_ACTL: 0x40006908

B1_UDB04_MSK_ACTL: 0x40006B08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-647.
12	INT_EN	(no description) See Table 1-650.
11	FIFO1_LVL	FIFO level See Table 1-649.
10	FIFO0_LVL	FIFO level See Table 1-649.
9	FIFO1_CLR	FIFO clear See Table 1-648.
8	FIFO0_CLR	FIFO clear See Table 1-648.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-647. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-648. Bit field encoding: E_FIFO_CLR

Value	Name	Description

1.3.1042 B[0..3]_UDB04_MSK_ACTL (continued)

Table 1-648. Bit field encoding: E_FIFO_CLR

1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-649. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-650. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1043 B[0..3]_UDB05_MSK_ACTL

UDB05_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_MSK_ACTL: 0x4000690A

B1_UDB05_MSK_ACTL: 0x40006B0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-651.
12	INT_EN	(no description) See Table 1-654.
11	FIFO1_LVL	FIFO level See Table 1-653.
10	FIFO0_LVL	FIFO level See Table 1-653.
9	FIFO1_CLR	FIFO clear See Table 1-652.
8	FIFO0_CLR	FIFO clear See Table 1-652.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-651. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-652. Bit field encoding: E_FIFO_CLR

Value	Name	Description

1.3.1043 B[0..3]_UDB05_MSK_ACTL (continued)

Table 1-652. Bit field encoding: E_FIFO_CLR

1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-653. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-654. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1044 B[0..3]_UDB06_MSK_ACTL

UDB06_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_MSK_ACTL: 0x4000690C

B1_UDB06_MSK_ACTL: 0x40006B0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-655.
12	INT_EN	(no description) See Table 1-658.
11	FIFO1_LVL	FIFO level See Table 1-657.
10	FIFO0_LVL	FIFO level See Table 1-657.
9	FIFO1_CLR	FIFO clear See Table 1-656.
8	FIFO0_CLR	FIFO clear See Table 1-656.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-655. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-656. Bit field encoding: E_FIFO_CLR

Value	Name	Description

1.3.1044 B[0..3]_UDB06_MSK_ACTL (continued)

Table 1-656. Bit field encoding: E_FIFO_CLR

1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-657. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-658. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1045 B[0..3]_UDB07_MSK_ACTL

UDB07_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_MSK_ACTL: 0x4000690E

B1_UDB07_MSK_ACTL: 0x40006B0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-659.
12	INT_EN	(no description) See Table 1-662.
11	FIFO1_LVL	FIFO level See Table 1-661.
10	FIFO0_LVL	FIFO level See Table 1-661.
9	FIFO1_CLR	FIFO clear See Table 1-660.
8	FIFO0_CLR	FIFO clear See Table 1-660.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-659. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-660. Bit field encoding: E_FIFO_CLR

Value	Name	Description

1.3.1045 B[0..3]_UDB07_MSK_ACTL (continued)

Table 1-660. Bit field encoding: E_FIFO_CLR

1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-661. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-662. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1046 B[0..3]_UDB08_MSK_ACTL

UDB08_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_MSK_ACTL: 0x40006910

B1_UDB08_MSK_ACTL: 0x40006B10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-663.
12	INT_EN	(no description) See Table 1-666.
11	FIFO1_LVL	FIFO level See Table 1-665.
10	FIFO0_LVL	FIFO level See Table 1-665.
9	FIFO1_CLR	FIFO clear See Table 1-664.
8	FIFO0_CLR	FIFO clear See Table 1-664.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-663. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-664. Bit field encoding: E_FIFO_CLR

Value	Name	Description

1.3.1046 B[0..3]_UDB08_MSK_ACTL (continued)

Table 1-664. Bit field encoding: E_FIFO_CLR

1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-665. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-666. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1047 B[0..3]_UDB09_MSK_ACTL

UDB09_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_MSK_ACTL: 0x40006912

B1_UDB09_MSK_ACTL: 0x40006B12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-667.
12	INT_EN	(no description) See Table 1-670.
11	FIFO1_LVL	FIFO level See Table 1-669.
10	FIFO0_LVL	FIFO level See Table 1-669.
9	FIFO1_CLR	FIFO clear See Table 1-668.
8	FIFO0_CLR	FIFO clear See Table 1-668.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-667. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-668. Bit field encoding: E_FIFO_CLR

Value	Name	Description

1.3.1047 B[0..3]_UDB09_MSK_ACTL (continued)

Table 1-668. Bit field encoding: E_FIFO_CLR

1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-669. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-670. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1048 B[0..3]_UDB10_MSK_ACTL

UDB10_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_MSK_ACTL: 0x40006914

B1_UDB10_MSK_ACTL: 0x40006B14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-671.
12	INT_EN	(no description) See Table 1-674.
11	FIFO1_LVL	FIFO level See Table 1-673.
10	FIFO0_LVL	FIFO level See Table 1-673.
9	FIFO1_CLR	FIFO clear See Table 1-672.
8	FIFO0_CLR	FIFO clear See Table 1-672.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-671. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-672. Bit field encoding: E_FIFO_CLR

Value	Name	Description

1.3.1048 B[0..3]_UDB10_MSK_ACTL (continued)

Table 1-672. Bit field encoding: E_FIFO_CLR

1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-673. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-674. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1049 B[0..3]_UDB11_MSK_ACTL

UDB11_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_MSK_ACTL: 0x40006916

B1_UDB11_MSK_ACTL: 0x40006B16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-675.
12	INT_EN	(no description) See Table 1-678.
11	FIFO1_LVL	FIFO level See Table 1-677.
10	FIFO0_LVL	FIFO level See Table 1-677.
9	FIFO1_CLR	FIFO clear See Table 1-676.
8	FIFO0_CLR	FIFO clear See Table 1-676.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-675. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-676. Bit field encoding: E_FIFO_CLR

Value	Name	Description

1.3.1049 B[0..3]_UDB11_MSK_ACTL (continued)

Table 1-676. Bit field encoding: E_FIFO_CLR

1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-677. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-678. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1050 B[0..3]_UDB12_MSK_ACTL

UDB12_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_MSK_ACTL: 0x40006918

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-679.
12	INT_EN	(no description) See Table 1-682.
11	FIFO1_LVL	FIFO level See Table 1-681.
10	FIFO0_LVL	FIFO level See Table 1-681.
9	FIFO1_CLR	FIFO clear See Table 1-680.
8	FIFO0_CLR	FIFO clear See Table 1-680.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-679. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-680. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

1.3.1050 B[0..3]_UDB12_MSK_ACTL (continued)

Table 1-681. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-682. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1051 B[0..3]_UDB13_MSK_ACTL

UDB13_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_MSK_ACTL: 0x4000691A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-683.
12	INT_EN	(no description) See Table 1-686.
11	FIFO1_LVL	FIFO level See Table 1-685.
10	FIFO0_LVL	FIFO level See Table 1-685.
9	FIFO1_CLR	FIFO clear See Table 1-684.
8	FIFO0_CLR	FIFO clear See Table 1-684.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-683. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-684. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

1.3.1051 B[0..3]_UDB13_MSK_ACTL (continued)

Table 1-685. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-686. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1052 B[0..3]_UDB14_MSK_ACTL

UDB14_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_MSK_ACTL: 0x4000691C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-687.
12	INT_EN	(no description) See Table 1-690.
11	FIFO1_LVL	FIFO level See Table 1-689.
10	FIFO0_LVL	FIFO level See Table 1-689.
9	FIFO1_CLR	FIFO clear See Table 1-688.
8	FIFO0_CLR	FIFO clear See Table 1-688.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-687. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-688. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

1.3.1052 B[0..3]_UDB14_MSK_ACTL (continued)

Table 1-689. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-690. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1053 B[0..3]_UDB15_MSK_ACTL

UDB15_MSK_ACTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_MSK_ACTL: 0x4000691E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Name		MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Name			CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-691.
12	INT_EN	(no description) See Table 1-694.
11	FIFO1_LVL	FIFO level See Table 1-693.
10	FIFO0_LVL	FIFO level See Table 1-693.
9	FIFO1_CLR	FIFO clear See Table 1-692.
8	FIFO0_CLR	FIFO clear See Table 1-692.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-691. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-692. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

1.3.1053 B[0..3]_UDB15_MSK_ACTL (continued)

Table 1-693. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-694. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1054 B[0..3]_UDB00_MC_00

UDB00_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_MC_00: 0x40006940

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1055 B[0..3]_UDB01_MC_00

UDB01_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_MC_00: 0x40006942

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1056 B[0..3]_UDB02_MC_00

UDB02_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_MC_00: 0x40006944

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1057 B[0..3]_UDB03_MC_00

UDB03_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_MC_00: 0x40006946

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1058 B[0..3]_UDB04_MC_00

UDB04_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_MC_00: 0x40006948 B1_UDB04_MC_00: 0x40006B48

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1059 B[0..3]_UDB05_MC_00

UDB05_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_MC_00: 0x4000694A B1_UDB05_MC_00: 0x40006B4A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1060 B[0..3]_UDB06_MC_00

UDB06_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_MC_00: 0x4000694C B1_UDB06_MC_00: 0x40006B4C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1061 B[0..3]_UDB07_MC_00

UDB07_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_MC_00: 0x4000694E B1_UDB07_MC_00: 0x40006B4E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1062 B[0..3]_UDB08_MC_00

UDB08_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_MC_00: 0x40006950 B1_UDB08_MC_00: 0x40006B50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1063 B[0..3]_UDB09_MC_00

UDB09_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_MC_00: 0x40006952 B1_UDB09_MC_00: 0x40006B52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1064 B[0..3]_UDB10_MC_00

UDB10_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_MC_00: 0x40006954 B1_UDB10_MC_00: 0x40006B54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1065 B[0..3]_UDB11_MC_00

UDB11_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_MC_00: 0x40006956 B1_UDB11_MC_00: 0x40006B56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1066 B[0..3]_UDB12_MC_00

UDB12_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_MC_00: 0x40006958

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1067 B[0..3]_UDB13_MC_00

UDB13_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_MC_00: 0x4000695A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1068 B[0..3]_UDB14_MC_00

UDB14_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_MC_00: 0x4000695C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1069 B[0..3]_UDB15_MC_00

UDB15_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_MC_00: 0x4000695E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1070 PHUB_CFG

PHUB Configuration

Reset: Reset Signals Listed Below

Register : Address

PHUB_CFG: 0x40007000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1111111							R/W:0
HW Access	R							R
Name	spk_cpu_pri							cpu_clkdif

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:11111111							
HW Access	R							
Name	spk_cpu_pri							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Name	simple_pri	pri_int_en						

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:U	R/W:UUUU				R/W:111		
HW Access	NA	R				R		
Name		prune_clock_dly				bus_timeout		

This is the general configuration register for the PHUB

Bits	Name	Description
30:27	prune_clock_dly[3:0]	Specifies the amount of delay of prune_clock with respect to clock. The actual delay amount for each setting is determined by an external block that implements the actual delay. The reset value for this field is determined by the PHUB_PRUNE_CLOCK_DLY_RESET_VAL `define.
26:24	bus_timeout[2:0]	Specifies the number of wait states (!HREADY responses by an accessed peripheral) PHUB will allow before timing out the AHB transaction. On a bus timeout PHUB will act as if it received a positive HREADY from the peripheral then move onto the next natural transaction as it would normally. The BUS_TIMEOUT bit of the ERR register will be set upon detecting the timeout. See Table 1-695.
23	simple_pri	0: Grant allocation fairness algorithm enabled 1: Grant allocation fairness algorithm disabled; simple priority utilized

1.3.1070 PHUB_CFG (continued)

22:16	pri_int_en[6:0]	0: Priority can not interrupt lower priority channels 1: Priority can interrupt lower priority channels Bits 22:16 correspond to priorities 6:0. Priority 7 is the lowest priority and thus can not interrupt yet lower priorities and therefore there is no bit for it.
15:1	spk_cpu_pri[14:0]	0: DMA priority spoke 1: CPU priority spoke Bits 15:1 correspond to spokes 15:1 respectively. SPK0 is not accessible by the CPU and thus no bit exists for it. The number of valid SPKxx_CPU_PRI bits is determined by the cfg_num_of_spk[4:0] input to PHUB; non-configured bits are hardwired to 0.
0	cpu_clkdif	0: CPU_CLOCK_EN assumed tied to 1; Performance Mode 1: CPU_CLOCK_EN assumed to modulate; Mixed Frequency Mode

Reset Table

resetsignal	field(s)
N/A	prune_clock_dly[3:0]
System reset for retention flops [reset_all_retention]	cpu_clkdif, spk_cpu_pri[14:0], pri_int_en[6:0], simple_pri, bus_timeout[2:0]

Table 1-695. Bit field encoding: BUS_TIMEOUT_ENUM

Value	Name	Description
3'b000	Timeout_0	Disable bus timeout detection
3'b001	Timeout_1	1 wait state
3'b010	Timeout_2	2 wait states
3'b011	Timeout_3	4 wait states
3'b100	Timeout_4	8 wait states
3'b101	Timeout_5	16 wait states
3'b110	Timeout_6	32 wait states
3'b111	Timeout_7	64 wait states (default)

1.3.1071 PHUB_ERR

PHUB Error Detection

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_ERR: 0x40007004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:UUUU				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R	R	R	R
Name					periph_err	unpop_acc	bus_timeout	boot_dma_fail

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

PHUB detects the following errors: 1. Bus Timeout 2. Unpopulated address access 3. Peripheral AHB ERROR response If the error was detected as a result of a CPU access then PHUB will send an AHB ERROR response to the CPU. If the error was detected as a result of either a CPU or DMA access then PHUB will set the corresponding bit in the following ERR register.

Bits	Name	Description
3	periph_err	Set to 1 when a peripheral responds to a bus transaction with an AHB ERROR response. Cleared by writing a 1.
2	unpop_acc	Set to 1 when an access is attempted to an address that does not decode to any spoke HSEL. Cleared by writing a 1.
1	bus_timeout	Set to 1 when a bus timeout occurs. Cleared by writing a 1. Timeout values are determined by the BUS_TIMEOUT field in the PHUBCFG register.
0	boot_dma_fail	Set to 1 if boot DMA fails. Cleared by writing a 1.

1.3.1072 PHUB_ERR_ADR

PHUB Error Address

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_ERR_ADR: 0x40007008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name	err_adr							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R							
Name	err_adr							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R							
Name	err_adr							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R							
Name	err_adr							

Contains the address that caused an error to trigger

Bits	Name	Description
31:0	err_adr[31:0]	Contains the value of the address that caused the error (limited to the BUS_TIMEOUT, UNPOP_ACC and PERIPH_ERR errors). If there are a succession of errors that occur before the CPU is able to clear the ERR register to all zeros, ERR_ADR will latch the address of the first error only.

1.3.1073 PHUB_CH[0..23]_BASIC_CFG

Channel Basic Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_CH0_BASIC_CFG: 0x40007010
PHUB_CH1_BASIC_CFG: 0x40007020
PHUB_CH2_BASIC_CFG: 0x40007030
PHUB_CH3_BASIC_CFG: 0x40007040
PHUB_CH4_BASIC_CFG: 0x40007050
PHUB_CH5_BASIC_CFG: 0x40007060
PHUB_CH6_BASIC_CFG: 0x40007070
PHUB_CH7_BASIC_CFG: 0x40007080
PHUB_CH8_BASIC_CFG: 0x40007090
PHUB_CH9_BASIC_CFG: 0x400070A0
PHUB_CH10_BASIC_CFG: 0x400070B0
PHUB_CH11_BASIC_CFG: 0x400070C0
PHUB_CH12_BASIC_CFG: 0x400070D0
PHUB_CH13_BASIC_CFG: 0x400070E0
PHUB_CH14_BASIC_CFG: 0x400070F0
PHUB_CH15_BASIC_CFG: 0x40007100
PHUB_CH16_BASIC_CFG: 0x40007110
PHUB_CH17_BASIC_CFG: 0x40007120
PHUB_CH18_BASIC_CFG: 0x40007130
PHUB_CH19_BASIC_CFG: 0x40007140
PHUB_CH20_BASIC_CFG: 0x40007150
PHUB_CH21_BASIC_CFG: 0x40007160
PHUB_CH22_BASIC_CFG: 0x40007170
PHUB_CH23_BASIC_CFG: 0x40007180

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:UU		R/W:0	R/W:0	R/W:000			R/W:0
HW Access	NA		R	R	R			R
Name			work_sep	rr_en	pri			en

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

1.3.1073 PHUB_CH[0..23]_BASIC_CFG (continued)

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Each channel will have the following basic configuration stored in gates inside PHUB.

Bits	Name	Description
5	work_sep	If a TD requires multiple bursts DMAC must remember where it left off between bursts while allowing interleaving other channels' bus access. It can either store the intermediate TD states on top of the current CHn_ORIG_TD0/1 of the TD chain, OR it can store it separately in a working area called CHn_SEP_TD0/1. The latter allows the original TD chain to be preserved. 0: Store the intermediate and final TD states on top of the original TD chain. Intermediate state storage allows the CPU to gauge progress of a particular TD. Final state storage allows the CPU to 'walk the chain' later and see what the final completion state of each TD was. 1: Store the intermediate TD states separately in CHn_SEP_TD0/1 to preserve the original TD chain. Intermediate state storage allows the CPU to gauge progress of a particular TD. Note the final state of each TD is not stored anywhere in this case. CHn_SEP_TD0/1 is stored in TDMEM and the address is: {00, CH_NUM[5:0], 000} WORK_SEP is only valid if the cfg_en_work_sep input to PHUB is true; otherwise WORK_SEP is hardwired to zero.
4	rr_en	Round-Robin enable RR_EN is only valid if the cfg_ch_recent_cnt_size[2:0] input to PHUB is not zero; otherwise RR_EN is hardwired to zero.
3:1	pri[2:0]	Channel priority; see DMA Arbiter section for description of channel priorities
0	en	0: Channel is disabled from accepting requests. This is the default state of the channel and allows the channel to be fully configured before enabling. This can also be used to stall a chain. If TD_ACTIVE=0 then clearing this bit will prevent any further DMA requests from being accepted by the channel until ENABLE is set again. If TD_ACTIVE=1 then DMAC will allow the current burst to finish naturally. Then when DMAC returns to the IDLE state it will prevent any further DMA requests from being accepted by the channel until ENABLE is set again. 1: channel is enabled and will accept DMA requests for it

1.3.1074 PHUB_CH[0..23]_ACTION

Channel Action

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_CH0_ACTION: 0x40007014	PHUB_CH1_ACTION: 0x40007024
PHUB_CH2_ACTION: 0x40007034	PHUB_CH3_ACTION: 0x40007044
PHUB_CH4_ACTION: 0x40007054	PHUB_CH5_ACTION: 0x40007064
PHUB_CH6_ACTION: 0x40007074	PHUB_CH7_ACTION: 0x40007084
PHUB_CH8_ACTION: 0x40007094	PHUB_CH9_ACTION: 0x400070A4
PHUB_CH10_ACTION: 0x400070B4	PHUB_CH11_ACTION: 0x400070C4
PHUB_CH12_ACTION: 0x400070D4	PHUB_CH13_ACTION: 0x400070E4
PHUB_CH14_ACTION: 0x400070F4	PHUB_CH15_ACTION: 0x40007104
PHUB_CH16_ACTION: 0x40007114	PHUB_CH17_ACTION: 0x40007124
PHUB_CH18_ACTION: 0x40007134	PHUB_CH19_ACTION: 0x40007144
PHUB_CH20_ACTION: 0x40007154	PHUB_CH21_ACTION: 0x40007164
PHUB_CH22_ACTION: 0x40007174	PHUB_CH23_ACTION: 0x40007184

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:UUUUU					R/WOSET:0	R/WOSET:0	R/WOSET:0
HW Access	NA					R	R	R
Name						cpu_term_chain	cpu_term_td	cpu_req

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Each channel will have the following action register associated with it:

Bits	Name	Description

1.3.1074 PHUB_CH[0..23]_ACTION (continued)

2	cpu_term_chain	Setting this bit causes the TD chain to terminate and the channel's ENABLE and CHAIN_ACTIVE bits to clear. If TD_ACTIVE=0 setting this bit will effectively create a request for the channel. When the request wins the DMAC will do some housekeeping associated with terminating a chain which includes clearing the channel's ENABLE, CHAIN_ACTIVE and CPU_TERM_CHAIN bits. If TD_ACTIVE=1 then DMAC will terminate the current burst as soon as any outstanding AHB requests are completed. The channel's ENABLE, CHAIN_ACTIVE and CPU_TERM_CHAIN bits will be cleared when the DMAC returns to the IDLE state.
1	cpu_term_td	Setting this bit causes the current TD to terminate regardless of the status of the XFRCNT associated with the TD. If TD_ACTIVE=0 the CPU_TERM_TD bit will just wait in the background. When the channel is eventually requested and serviced by DMAC the data burst will be preempted and the TD will complete just as if XFRCNT had expired. When the DMAC FSM returns to the IDLE state it will clear the CPU_TERM_TD bit. If TD_ACTIVE=1 then DMAC will terminate the current burst as soon as any outstanding AHB requests are completed. The TD will them complete just as if XFRCNT had expired. When the DMAC FSM returns to the IDLE state it will clear the CPU_TERM_TD bit.
0	cpu_req	Setting this bit creates a direct DMA request for the channel. If TD_ACTIVE=0 CPU_REQ will remain set until the request wins arbitration and is accepted by DMAC. This bit is cleared upon triggering the DMAC FSM from the IDLE state. If TD_ACTIVE=1 CPU_REQ will remain set and will apply to the next burst for the channel. The bit will essentially be ignored by DMAC and will be left alone so that it can trigger the next burst for the channel.

1.3.1075 PHUB_CH[0..23]_BASIC_STATUS

Channel Basic Status Register

Reset: Reset Signals Listed Below

Register : Address

PHUB_CH0_BASIC_STATUS: 0x40007018
PHUB_CH1_BASIC_STATUS: 0x40007028
PHUB_CH2_BASIC_STATUS: 0x40007038
PHUB_CH3_BASIC_STATUS: 0x40007048
PHUB_CH4_BASIC_STATUS: 0x40007058
PHUB_CH5_BASIC_STATUS: 0x40007068
PHUB_CH6_BASIC_STATUS: 0x40007078
PHUB_CH7_BASIC_STATUS: 0x40007088
PHUB_CH8_BASIC_STATUS: 0x40007098
PHUB_CH9_BASIC_STATUS: 0x400070A8
PHUB_CH10_BASIC_STATUS: 0x400070B8
PHUB_CH11_BASIC_STATUS: 0x400070C8
PHUB_CH12_BASIC_STATUS: 0x400070D8
PHUB_CH13_BASIC_STATUS: 0x400070E8
PHUB_CH14_BASIC_STATUS: 0x400070F8
PHUB_CH15_BASIC_STATUS: 0x40007108
PHUB_CH16_BASIC_STATUS: 0x40007118
PHUB_CH17_BASIC_STATUS: 0x40007128
PHUB_CH18_BASIC_STATUS: 0x40007138
PHUB_CH19_BASIC_STATUS: 0x40007148
PHUB_CH20_BASIC_STATUS: 0x40007158
PHUB_CH21_BASIC_STATUS: 0x40007168
PHUB_CH22_BASIC_STATUS: 0x40007178
PHUB_CH23_BASIC_STATUS: 0x40007188

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:1111				NA:UU		R:0	R:0
HW Access	R				NA		R	R
Name	rr_cnt						td_active	chain_active

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:U	R/W:UUUUUUU						
HW Access	NA	R						

1.3.1075 PHUB_CH[0..23]_BASIC_STATUS (continued)

Name		td_ptr

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Name								

Each channel will have the following status information stored in gates inside PHUB

Bits	Name	Description
14:8	td_ptr[6:0]	Address pointer to the current CHn_ORIG_TD0/1 in the chain. The CPU initializes this to the location of the first TD in the chain before enabling the channel. DMAC updates TD_PTR with NEXT_TD when it completes the current TD. This gives status to the CPU of how far along the chain is and where it is. The CHn_ORIG_TD0/1 chain is stored in TDMEM and DMAC accesses the current TD at: {TD_PTR[7:0], 000} The number of valid TD_PTR bits is determined by the cfg_ch_td_ptr_size[3:0] input to PHUB; non-configured bits are hardwired to 0. br] TD_PTR resets to the same value as the channel number.
7:4	rr_cnt[3:0]	Current state of the channel's Round-Robin counter. The lower the value the more recently the channel has won a DMA grant with zero meaning it won the last grant. 0: RR_CNT will be frozen on the terminal count (all ones) and therefore it will look as if the channel has never received a DMA grant which will give it an advantage over channels that do support Round-Robin. Put another way, when RR_EN=0 the channel is not subject to Round-Robin rules. 1: RR_CNT will reset each time the channel wins a DMA grant. It will increment each time any other channel wins a DMA grant. It will stop incrementing when it hits the terminal count (all ones). The number of valid RR_CNT bits is determined by the cfg_ch_recent_cnt_size[2:0] input to PHUB; non-configured bits are hardwired to 0.
1	td_active	0: channel is not currently being serviced by DMAC 1: channel is currently being serviced by DMAC
0	chain_active	0: TD chain is inactive; either no DMA requests have triggered a new chain or the previous chain has completed. 1: TD chain has been triggered by a DMA request

Reset Table

resetsignal	field(s)
N/A	td_ptr[6:0]

1.3.1075 PHUB_CH[0..23]_BASIC_STATUS (continued)

Reset Table

System reset for retention flops [reset_all_retention]	chain_active, td_active, rr_cnt[3:0]

1.3.1076 PHUB_CFGMEM[0..23]_CFG0

PHUB Channel Configuration Register 0

Reset: N/A

Register : Address

PHUB_CFGMEM0_CFG0: 0x40007600
PHUB_CFGMEM1_CFG0: 0x40007608
PHUB_CFGMEM2_CFG0: 0x40007610
PHUB_CFGMEM3_CFG0: 0x40007618
PHUB_CFGMEM4_CFG0: 0x40007620
PHUB_CFGMEM5_CFG0: 0x40007628
PHUB_CFGMEM6_CFG0: 0x40007630
PHUB_CFGMEM7_CFG0: 0x40007638
PHUB_CFGMEM8_CFG0: 0x40007640
PHUB_CFGMEM9_CFG0: 0x40007648
PHUB_CFGMEM10_CFG0: 0x40007650
PHUB_CFGMEM11_CFG0: 0x40007658
PHUB_CFGMEM12_CFG0: 0x40007660
PHUB_CFGMEM13_CFG0: 0x40007668
PHUB_CFGMEM14_CFG0: 0x40007670
PHUB_CFGMEM15_CFG0: 0x40007678
PHUB_CFGMEM16_CFG0: 0x40007680
PHUB_CFGMEM17_CFG0: 0x40007688
PHUB_CFGMEM18_CFG0: 0x40007690
PHUB_CFGMEM19_CFG0: 0x40007698
PHUB_CFGMEM20_CFG0: 0x400076A0
PHUB_CFGMEM21_CFG0: 0x400076A8
PHUB_CFGMEM22_CFG0: 0x400076B0
PHUB_CFGMEM23_CFG0: 0x400076B8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:UUUUUUU						
HW Access	R	R						
Name	req_per_burst	burstcnt						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			

1.3.1076 PHUB_CFGMEM[0..23]_CFG0 (continued)

Name	termout1_sel	termout0_sel

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUU				R/W:UUUU			
HW Access	NA				R			
Name					termin_sel			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUU							NA:U
HW Access	R							NA
Name	burstcount_remain							

Each channel will have some configuration information stored in RAM, and this configuration information is called CHn_CFG0/1. CHn_CFG0/1 are stored in CFGMEM at {CH_NUM[5:0], 000}. Chn_CFG0/1 are described in detail below.

Bits	Name	Description
31:25	burstcount_remain[6:0]	These bits are reserved for use by the DMAC in storing the intermediate state of BURSTCNT in the event that the channel is interrupted mid-burst by a higher priority channel. These bits need to be preserved by SW only if the channel is active and interrupt-able. Otherwise SW can over-write these bits without concern, for instance when initially setting up the configuration for the channel.
19:16	termin_sel[3:0]	Selects 1 of the 16 TERMIN[15:0] inputs to PHUB for use in terminating a TD. Any active high strobe on the TERMIN signal will be positive edge detected and will cause the TD to terminate if TERMIN_EN is set in the TD. The TD will complete just as if XFRCNT expired.
15:12	termout1_sel[3:0]	Selects 1 of the 16 TERMOUT1[15:0] outputs from PHUB to be toggled upon completion of the current TD if TERMOUT1_EN is set in the TD. Because the frequency of the receiving logic for the TERMOUT1 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT1 signal and interpret either as the completion of the current TD.
11:8	termout0_sel[3:0]	Selects 1 of the 16 TERMOUT0[15:0] outputs from PHUB to be toggled upon completion of the current TD if TERMOUT0_EN is set in the TD. Because the frequency of the receiving logic for the TERMOUT0 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT0 signal and interpret either as the completion of the current TD.
7	req_per_burst	0: A DMA request is required to activate each TD in the chain. If the TD requires multiple bursts to complete then all subsequent bursts after the first burst will be automatically requested and carried out. DMAC will set the AUTO_BURST_WHOLE_TD request after completing each burst except the last. 1: A DMA request is required to activate each TD in the chain. If the TD requires multiple bursts to complete then all subsequent bursts after the first burst must also be individually requested.
6:0	burstcnt[6:0]	The data block moved by a TD can be broken up into small bursts. BURSTCNT[6:0] specifies the length of the small burst from 1 to 127 bytes. If BURSTCNT=0 this means do not break the data block into small bursts and instead burst the whole XFRCNT in one burst. The number of valid BURSTCNT bits is determined by the cfg_burstcnt_size[2:0] input to PHUB; non-configured bits are ignored by the DMAC.

1.3.1077 PHUB_CFGMEM[0..23]_CFG1

PHUB Channel Configuration Register 1

Reset: N/A

Register : Address

PHUB_CFGMEM0_CFG1: 0x40007604
PHUB_CFGMEM1_CFG1: 0x4000760C
PHUB_CFGMEM2_CFG1: 0x40007614
PHUB_CFGMEM3_CFG1: 0x4000761C
PHUB_CFGMEM4_CFG1: 0x40007624
PHUB_CFGMEM5_CFG1: 0x4000762C
PHUB_CFGMEM6_CFG1: 0x40007634
PHUB_CFGMEM7_CFG1: 0x4000763C
PHUB_CFGMEM8_CFG1: 0x40007644
PHUB_CFGMEM9_CFG1: 0x4000764C
PHUB_CFGMEM10_CFG1: 0x40007654
PHUB_CFGMEM11_CFG1: 0x4000765C
PHUB_CFGMEM12_CFG1: 0x40007664
PHUB_CFGMEM13_CFG1: 0x4000766C
PHUB_CFGMEM14_CFG1: 0x40007674
PHUB_CFGMEM15_CFG1: 0x4000767C
PHUB_CFGMEM16_CFG1: 0x40007684
PHUB_CFGMEM17_CFG1: 0x4000768C
PHUB_CFGMEM18_CFG1: 0x40007694
PHUB_CFGMEM19_CFG1: 0x4000769C
PHUB_CFGMEM20_CFG1: 0x400076A4
PHUB_CFGMEM21_CFG1: 0x400076AC
PHUB_CFGMEM22_CFG1: 0x400076B4
PHUB_CFGMEM23_CFG1: 0x400076BC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	src_base_adr							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	src_base_adr							

1.3.1077 PHUB_CFGMEM[0..23]_CFG1 (continued)

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	dst_base_adr							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	dst_base_adr							

Each channel will have some configuration information stored in RAM, and this configuration information is called CHn_CFG0/1. CHn_CFG0/1 are stored in CFGMEM at {CH_NUM[5:0], 000}. Chn_CFG0/1 are described in detail below.

Bits	Name	Description
31:16	dst_base_adr[15:0]	Base address used for the destination address. Concatenates with DST_ADR[15:0] from the TD to form the full address.
15:0	src_base_adr[15:0]	Base address used for the source address. Concatenates with SRC_ADR[15:0] from the TD to form the full source address.

1.3.1078 PHUB_TDMEM[0..127]_ORIG_TD0

PHUB Original Transaction Descriptor 0

Reset: N/A

Register : Address

PHUB_TDMEM0_ORIG_TD0: 0x40007800
PHUB_TDMEM1_ORIG_TD0: 0x40007808
PHUB_TDMEM2_ORIG_TD0: 0x40007810
PHUB_TDMEM3_ORIG_TD0: 0x40007818
PHUB_TDMEM4_ORIG_TD0: 0x40007820
PHUB_TDMEM5_ORIG_TD0: 0x40007828
PHUB_TDMEM6_ORIG_TD0: 0x40007830
PHUB_TDMEM7_ORIG_TD0: 0x40007838
PHUB_TDMEM8_ORIG_TD0: 0x40007840
PHUB_TDMEM9_ORIG_TD0: 0x40007848
PHUB_TDMEM10_ORIG_TD0: 0x40007850
PHUB_TDMEM11_ORIG_TD0: 0x40007858
PHUB_TDMEM12_ORIG_TD0: 0x40007860
PHUB_TDMEM13_ORIG_TD0: 0x40007868
PHUB_TDMEM14_ORIG_TD0: 0x40007870
PHUB_TDMEM15_ORIG_TD0: 0x40007878
PHUB_TDMEM16_ORIG_TD0: 0x40007880
PHUB_TDMEM17_ORIG_TD0: 0x40007888
PHUB_TDMEM18_ORIG_TD0: 0x40007890
PHUB_TDMEM19_ORIG_TD0: 0x40007898
PHUB_TDMEM20_ORIG_TD0: 0x400078A0
PHUB_TDMEM21_ORIG_TD0: 0x400078A8
PHUB_TDMEM22_ORIG_TD0: 0x400078B0
PHUB_TDMEM23_ORIG_TD0: 0x400078B8
PHUB_TDMEM24_ORIG_TD0: 0x400078C0
PHUB_TDMEM25_ORIG_TD0: 0x400078C8
PHUB_TDMEM26_ORIG_TD0: 0x400078D0
PHUB_TDMEM27_ORIG_TD0: 0x400078D8
PHUB_TDMEM28_ORIG_TD0: 0x400078E0
PHUB_TDMEM29_ORIG_TD0: 0x400078E8
PHUB_TDMEM30_ORIG_TD0: 0x400078F0
PHUB_TDMEM31_ORIG_TD0: 0x400078F8

1.3.1078 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

Register : Address

PHUB_TDMEM32_ORIG_TD0: 0x40007900
PHUB_TDMEM33_ORIG_TD0: 0x40007908
PHUB_TDMEM34_ORIG_TD0: 0x40007910
PHUB_TDMEM35_ORIG_TD0: 0x40007918
PHUB_TDMEM36_ORIG_TD0: 0x40007920
PHUB_TDMEM37_ORIG_TD0: 0x40007928
PHUB_TDMEM38_ORIG_TD0: 0x40007930
PHUB_TDMEM39_ORIG_TD0: 0x40007938
PHUB_TDMEM40_ORIG_TD0: 0x40007940
PHUB_TDMEM41_ORIG_TD0: 0x40007948
PHUB_TDMEM42_ORIG_TD0: 0x40007950
PHUB_TDMEM43_ORIG_TD0: 0x40007958
PHUB_TDMEM44_ORIG_TD0: 0x40007960
PHUB_TDMEM45_ORIG_TD0: 0x40007968
PHUB_TDMEM46_ORIG_TD0: 0x40007970
PHUB_TDMEM47_ORIG_TD0: 0x40007978
PHUB_TDMEM48_ORIG_TD0: 0x40007980
PHUB_TDMEM49_ORIG_TD0: 0x40007988
PHUB_TDMEM50_ORIG_TD0: 0x40007990
PHUB_TDMEM51_ORIG_TD0: 0x40007998
PHUB_TDMEM52_ORIG_TD0: 0x400079A0
PHUB_TDMEM53_ORIG_TD0: 0x400079A8
PHUB_TDMEM54_ORIG_TD0: 0x400079B0
PHUB_TDMEM55_ORIG_TD0: 0x400079B8
PHUB_TDMEM56_ORIG_TD0: 0x400079C0
PHUB_TDMEM57_ORIG_TD0: 0x400079C8
PHUB_TDMEM58_ORIG_TD0: 0x400079D0
PHUB_TDMEM59_ORIG_TD0: 0x400079D8
PHUB_TDMEM60_ORIG_TD0: 0x400079E0
PHUB_TDMEM61_ORIG_TD0: 0x400079E8
PHUB_TDMEM62_ORIG_TD0: 0x400079F0
PHUB_TDMEM63_ORIG_TD0: 0x400079F8
PHUB_TDMEM64_ORIG_TD0: 0x40007A00
PHUB_TDMEM65_ORIG_TD0: 0x40007A08
PHUB_TDMEM66_ORIG_TD0: 0x40007A10
PHUB_TDMEM67_ORIG_TD0: 0x40007A18

1.3.1078 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

Register : Address

PHUB_TDMEM68_ORIG_TD0: 0x40007A20
PHUB_TDMEM69_ORIG_TD0: 0x40007A28
PHUB_TDMEM70_ORIG_TD0: 0x40007A30
PHUB_TDMEM71_ORIG_TD0: 0x40007A38
PHUB_TDMEM72_ORIG_TD0: 0x40007A40
PHUB_TDMEM73_ORIG_TD0: 0x40007A48
PHUB_TDMEM74_ORIG_TD0: 0x40007A50
PHUB_TDMEM75_ORIG_TD0: 0x40007A58
PHUB_TDMEM76_ORIG_TD0: 0x40007A60
PHUB_TDMEM77_ORIG_TD0: 0x40007A68
PHUB_TDMEM78_ORIG_TD0: 0x40007A70
PHUB_TDMEM79_ORIG_TD0: 0x40007A78
PHUB_TDMEM80_ORIG_TD0: 0x40007A80
PHUB_TDMEM81_ORIG_TD0: 0x40007A88
PHUB_TDMEM82_ORIG_TD0: 0x40007A90
PHUB_TDMEM83_ORIG_TD0: 0x40007A98
PHUB_TDMEM84_ORIG_TD0: 0x40007AA0
PHUB_TDMEM85_ORIG_TD0: 0x40007AA8
PHUB_TDMEM86_ORIG_TD0: 0x40007AB0
PHUB_TDMEM87_ORIG_TD0: 0x40007AB8
PHUB_TDMEM88_ORIG_TD0: 0x40007AC0
PHUB_TDMEM89_ORIG_TD0: 0x40007AC8
PHUB_TDMEM90_ORIG_TD0: 0x40007AD0
PHUB_TDMEM91_ORIG_TD0: 0x40007AD8
PHUB_TDMEM92_ORIG_TD0: 0x40007AE0
PHUB_TDMEM93_ORIG_TD0: 0x40007AE8
PHUB_TDMEM94_ORIG_TD0: 0x40007AF0
PHUB_TDMEM95_ORIG_TD0: 0x40007AF8
PHUB_TDMEM96_ORIG_TD0: 0x40007B00
PHUB_TDMEM97_ORIG_TD0: 0x40007B08
PHUB_TDMEM98_ORIG_TD0: 0x40007B10
PHUB_TDMEM99_ORIG_TD0: 0x40007B18
PHUB_TDMEM100_ORIG_TD0: 0x40007B20
PHUB_TDMEM101_ORIG_TD0: 0x40007B28
PHUB_TDMEM102_ORIG_TD0: 0x40007B30
PHUB_TDMEM103_ORIG_TD0: 0x40007B38

1.3.1078 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

Register : Address

PHUB_TDMEM104_ORIG_TD0: 0x40007B40
PHUB_TDMEM105_ORIG_TD0: 0x40007B48
PHUB_TDMEM106_ORIG_TD0: 0x40007B50
PHUB_TDMEM107_ORIG_TD0: 0x40007B58
PHUB_TDMEM108_ORIG_TD0: 0x40007B60
PHUB_TDMEM109_ORIG_TD0: 0x40007B68
PHUB_TDMEM110_ORIG_TD0: 0x40007B70
PHUB_TDMEM111_ORIG_TD0: 0x40007B78
PHUB_TDMEM112_ORIG_TD0: 0x40007B80
PHUB_TDMEM113_ORIG_TD0: 0x40007B88
PHUB_TDMEM114_ORIG_TD0: 0x40007B90
PHUB_TDMEM115_ORIG_TD0: 0x40007B98
PHUB_TDMEM116_ORIG_TD0: 0x40007BA0
PHUB_TDMEM117_ORIG_TD0: 0x40007BA8
PHUB_TDMEM118_ORIG_TD0: 0x40007BB0
PHUB_TDMEM119_ORIG_TD0: 0x40007BB8
PHUB_TDMEM120_ORIG_TD0: 0x40007BC0
PHUB_TDMEM121_ORIG_TD0: 0x40007BC8
PHUB_TDMEM122_ORIG_TD0: 0x40007BD0
PHUB_TDMEM123_ORIG_TD0: 0x40007BD8
PHUB_TDMEM124_ORIG_TD0: 0x40007BE0
PHUB_TDMEM125_ORIG_TD0: 0x40007BE8
PHUB_TDMEM126_ORIG_TD0: 0x40007BF0
PHUB_TDMEM127_ORIG_TD0: 0x40007BF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	xfrcnt							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUU				R/W:UUUU			
HW Access	NA				R			
Name					xfrcnt			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							

1.3.1078 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

HW Access	R
Name	next_td_ptr

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	swap_en	swap_size	auto_exec_next	termin_en	termout1_en	termout0_en	inc_dst_adr	inc_src_adr

Each channel will have a TD chain (as short as one TD in length) that provides instructions to the DMAC for carrying out a DMA sequence for the channel. This is described in greater detail in the 'TD Chains' section to follow. The TD chain is comprised of one or more CHn_ORIG_TD0/1 TDs. DMAC accesses the CHn_ORIG_TD0/1 chain from TDMEM and the address in TDMEM of the current TD in the chain is {TD_PTR[7:0], 000}. TD_PTR for the first TD in a chain is initialized by the CPU. As the chain progresses through TDs the TD_PTR will be automatically updated by DMAC to reflect the current TD being accessed in the chain. CHn_ORIG_TD0/1 are described in detail below.

Bits	Name	Description
31	swap_en	0: Do not perform endian swap 1: Perform endian swap. BURSTCNT and XFRCNT must be an integer multiple of SWAP_SIZE.
30	swap_size	Only valid if SWAP_EN=1. 0: Swap size = 2 bytes, meaning every 2 bytes are endian swapped during the DMA transfer. 1: Swap size = 4 bytes, meaning every 4 bytes are endian swapped during the DMA transfer.
29	auto_exec_next	0: The next TD in the chain requires a CPU_REQ or peripheral request in order to trigger 1: The next TD in the chain will trigger automatically when the current TD completes. The DMAC will create an AUTO_EXEC_NEXT_TD request for the channel when it completes the current TD.
28	termin_en	0: Do not terminate this TD based on a TERMIN signal. 1: Terminate this TD if a positive edge on the TERMIN signal selected by TERMIN_SEL is detected. Any ongoing burst will terminate as soon as any outstanding AHB requests have been completed. The TD will then complete just as if XFRCNT expired. TBD: describe when TERMIN signal can activate, when it gets considered (TD_ACTIVE 0/1) and when it gets cleared.
27	termout1_en	0: Do not toggle a TERMOUT1 signal when this TD completes 1: When this TD completes the TERMOUT1 signal selected by TERMOUT1_SEL will toggle. Because the frequency of the receiving logic for the TERMOUT1 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT1 signal and interpret either as the completion of the current TD.
26	termout0_en	0: Do not toggle a TERMOUT0 signal when the TD completes 1: When this TD completes the TERMOUT0 signal selected by TERMOUT0_SEL will toggle. Because the frequency of the receiving logic for the TERMOUT0 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT0 signal and interpret either as the completion of the current TD.

1.3.1078 PHUB_TDMEM[0..127]_ORIG_TD0 (continued)

25	inc_dst_adr	0: Freeze DST_ADR throughout the burst 1: Increment DST_ADR according to the size of each data transaction in the burst
24	inc_src_adr	0: Freeze SRC_ADR throughout the burst 1: Increment SRC_ADR according to the size of each data transaction in the burst
23:16	next_td_ptr[7:0]	Specifies the next TD to be executed in the chain when this TD completes. When this TD completes the value of NEXT_TD_PTR is copied into the TD_PTR status register to allow the CPU to see where in the chain the channel is. If NEXT_TD_PTR=0xFF then this is the last TD in the chain. When the last TD in a chain completes DMAC will clear CHANNEL_EN and CHAIN_ACTIVE.
11:0	xfrcnt[11:0]	Transfer count in bytes from 1 to 4KB-1, or indefinite transfer count if set to 0. 1. Setting XFRCNT to 0: This means transfer count is not used to terminate the TD. An indefinite amount of data can be transferred in this mode. The TD must be terminated either by TERMIN, CPU_TERM_TD or CPU_TERM_CHAIN. Data movement is broken into bursts according to BURSTCNT. Note in the special case where both XFRCNT and BURSTCNT are 0 data will be transferred indefinitely and without interruption. 2. Setting XFRCNT to non-0: This means the XFRCNT is used to determine how much data will be transferred (1 to 4KB-1). If BURSTCNT=0 then DMAC will transfer the entire XFRCNT worth of data in one burst. If BURSTCNT is not 0 and BURSTCNT represents a value that is greater than or equal to XFRCNT then DMAC will transfer the entire XFRCNT worth of data in one burst. If BURSTCNT is not 0 and BURSTCNT represents a value that is less than XFRCNT then DMAC will break the data movement into multiple bursts as dictated by BURSTCNT. See the description for the REQ_PER_BURST bit for how subsequent bursts are triggered. At any point the TD can terminate before exhausting the XFRCNT due to TERMIN, CPU_TERM_TD or CPU_TERM_CHAIN. When DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update the XFRCNT to reflect the newly decremented value based on the number of bytes that were transferred in the burst. The number of valid XFRCNT bits is determined by the cfg_xfrcnt_size[4:0] input to PHUB; non-configured bits are ignored by the DMAC.

1.3.1079 PHUB_TDMEM[0..127]_ORIG_TD1

PHUB Original Transaction Descriptor 0

Reset: N/A

Register : Address

PHUB_TDMEM0_ORIG_TD1: 0x40007804
PHUB_TDMEM1_ORIG_TD1: 0x4000780C
PHUB_TDMEM2_ORIG_TD1: 0x40007814
PHUB_TDMEM3_ORIG_TD1: 0x4000781C
PHUB_TDMEM4_ORIG_TD1: 0x40007824
PHUB_TDMEM5_ORIG_TD1: 0x4000782C
PHUB_TDMEM6_ORIG_TD1: 0x40007834
PHUB_TDMEM7_ORIG_TD1: 0x4000783C
PHUB_TDMEM8_ORIG_TD1: 0x40007844
PHUB_TDMEM9_ORIG_TD1: 0x4000784C
PHUB_TDMEM10_ORIG_TD1: 0x40007854
PHUB_TDMEM11_ORIG_TD1: 0x4000785C
PHUB_TDMEM12_ORIG_TD1: 0x40007864
PHUB_TDMEM13_ORIG_TD1: 0x4000786C
PHUB_TDMEM14_ORIG_TD1: 0x40007874
PHUB_TDMEM15_ORIG_TD1: 0x4000787C
PHUB_TDMEM16_ORIG_TD1: 0x40007884
PHUB_TDMEM17_ORIG_TD1: 0x4000788C
PHUB_TDMEM18_ORIG_TD1: 0x40007894
PHUB_TDMEM19_ORIG_TD1: 0x4000789C
PHUB_TDMEM20_ORIG_TD1: 0x400078A4
PHUB_TDMEM21_ORIG_TD1: 0x400078AC
PHUB_TDMEM22_ORIG_TD1: 0x400078B4
PHUB_TDMEM23_ORIG_TD1: 0x400078BC
PHUB_TDMEM24_ORIG_TD1: 0x400078C4
PHUB_TDMEM25_ORIG_TD1: 0x400078CC
PHUB_TDMEM26_ORIG_TD1: 0x400078D4
PHUB_TDMEM27_ORIG_TD1: 0x400078DC
PHUB_TDMEM28_ORIG_TD1: 0x400078E4
PHUB_TDMEM29_ORIG_TD1: 0x400078EC
PHUB_TDMEM30_ORIG_TD1: 0x400078F4
PHUB_TDMEM31_ORIG_TD1: 0x400078FC

1.3.1079 PHUB_TDMEM[0..127]_ORIG_TD1 (continued)

Register : Address

PHUB_TDMEM32_ORIG_TD1: 0x40007904
PHUB_TDMEM33_ORIG_TD1: 0x4000790C
PHUB_TDMEM34_ORIG_TD1: 0x40007914
PHUB_TDMEM35_ORIG_TD1: 0x4000791C
PHUB_TDMEM36_ORIG_TD1: 0x40007924
PHUB_TDMEM37_ORIG_TD1: 0x4000792C
PHUB_TDMEM38_ORIG_TD1: 0x40007934
PHUB_TDMEM39_ORIG_TD1: 0x4000793C
PHUB_TDMEM40_ORIG_TD1: 0x40007944
PHUB_TDMEM41_ORIG_TD1: 0x4000794C
PHUB_TDMEM42_ORIG_TD1: 0x40007954
PHUB_TDMEM43_ORIG_TD1: 0x4000795C
PHUB_TDMEM44_ORIG_TD1: 0x40007964
PHUB_TDMEM45_ORIG_TD1: 0x4000796C
PHUB_TDMEM46_ORIG_TD1: 0x40007974
PHUB_TDMEM47_ORIG_TD1: 0x4000797C
PHUB_TDMEM48_ORIG_TD1: 0x40007984
PHUB_TDMEM49_ORIG_TD1: 0x4000798C
PHUB_TDMEM50_ORIG_TD1: 0x40007994
PHUB_TDMEM51_ORIG_TD1: 0x4000799C
PHUB_TDMEM52_ORIG_TD1: 0x400079A4
PHUB_TDMEM53_ORIG_TD1: 0x400079AC
PHUB_TDMEM54_ORIG_TD1: 0x400079B4
PHUB_TDMEM55_ORIG_TD1: 0x400079BC
PHUB_TDMEM56_ORIG_TD1: 0x400079C4
PHUB_TDMEM57_ORIG_TD1: 0x400079CC
PHUB_TDMEM58_ORIG_TD1: 0x400079D4
PHUB_TDMEM59_ORIG_TD1: 0x400079DC
PHUB_TDMEM60_ORIG_TD1: 0x400079E4
PHUB_TDMEM61_ORIG_TD1: 0x400079EC
PHUB_TDMEM62_ORIG_TD1: 0x400079F4
PHUB_TDMEM63_ORIG_TD1: 0x400079FC
PHUB_TDMEM64_ORIG_TD1: 0x40007A04
PHUB_TDMEM65_ORIG_TD1: 0x40007A0C
PHUB_TDMEM66_ORIG_TD1: 0x40007A14
PHUB_TDMEM67_ORIG_TD1: 0x40007A1C

1.3.1079 PHUB_TDMEM[0..127]_ORIG_TD1 (continued)

Register : Address

PHUB_TDMEM68_ORIG_TD1: 0x40007A24
PHUB_TDMEM69_ORIG_TD1: 0x40007A2C
PHUB_TDMEM70_ORIG_TD1: 0x40007A34
PHUB_TDMEM71_ORIG_TD1: 0x40007A3C
PHUB_TDMEM72_ORIG_TD1: 0x40007A44
PHUB_TDMEM73_ORIG_TD1: 0x40007A4C
PHUB_TDMEM74_ORIG_TD1: 0x40007A54
PHUB_TDMEM75_ORIG_TD1: 0x40007A5C
PHUB_TDMEM76_ORIG_TD1: 0x40007A64
PHUB_TDMEM77_ORIG_TD1: 0x40007A6C
PHUB_TDMEM78_ORIG_TD1: 0x40007A74
PHUB_TDMEM79_ORIG_TD1: 0x40007A7C
PHUB_TDMEM80_ORIG_TD1: 0x40007A84
PHUB_TDMEM81_ORIG_TD1: 0x40007A8C
PHUB_TDMEM82_ORIG_TD1: 0x40007A94
PHUB_TDMEM83_ORIG_TD1: 0x40007A9C
PHUB_TDMEM84_ORIG_TD1: 0x40007AA4
PHUB_TDMEM85_ORIG_TD1: 0x40007AAC
PHUB_TDMEM86_ORIG_TD1: 0x40007AB4
PHUB_TDMEM87_ORIG_TD1: 0x40007ABC
PHUB_TDMEM88_ORIG_TD1: 0x40007AC4
PHUB_TDMEM89_ORIG_TD1: 0x40007ACC
PHUB_TDMEM90_ORIG_TD1: 0x40007AD4
PHUB_TDMEM91_ORIG_TD1: 0x40007ADC
PHUB_TDMEM92_ORIG_TD1: 0x40007AE4
PHUB_TDMEM93_ORIG_TD1: 0x40007AEC
PHUB_TDMEM94_ORIG_TD1: 0x40007AF4
PHUB_TDMEM95_ORIG_TD1: 0x40007AFC
PHUB_TDMEM96_ORIG_TD1: 0x40007B04
PHUB_TDMEM97_ORIG_TD1: 0x40007B0C
PHUB_TDMEM98_ORIG_TD1: 0x40007B14
PHUB_TDMEM99_ORIG_TD1: 0x40007B1C
PHUB_TDMEM100_ORIG_TD1: 0x40007B24
PHUB_TDMEM101_ORIG_TD1: 0x40007B2C
PHUB_TDMEM102_ORIG_TD1: 0x40007B34
PHUB_TDMEM103_ORIG_TD1: 0x40007B3C

1.3.1079 PHUB_TDMEM[0..127]_ORIG_TD1 (continued)

Register : Address

PHUB_TDMEM104_ORIG_TD1: 0x40007B44
PHUB_TDMEM105_ORIG_TD1: 0x40007B4C
PHUB_TDMEM106_ORIG_TD1: 0x40007B54
PHUB_TDMEM107_ORIG_TD1: 0x40007B5C
PHUB_TDMEM108_ORIG_TD1: 0x40007B64
PHUB_TDMEM109_ORIG_TD1: 0x40007B6C
PHUB_TDMEM110_ORIG_TD1: 0x40007B74
PHUB_TDMEM111_ORIG_TD1: 0x40007B7C
PHUB_TDMEM112_ORIG_TD1: 0x40007B84
PHUB_TDMEM113_ORIG_TD1: 0x40007B8C
PHUB_TDMEM114_ORIG_TD1: 0x40007B94
PHUB_TDMEM115_ORIG_TD1: 0x40007B9C
PHUB_TDMEM116_ORIG_TD1: 0x40007BA4
PHUB_TDMEM117_ORIG_TD1: 0x40007BAC
PHUB_TDMEM118_ORIG_TD1: 0x40007BB4
PHUB_TDMEM119_ORIG_TD1: 0x40007BBC
PHUB_TDMEM120_ORIG_TD1: 0x40007BC4
PHUB_TDMEM121_ORIG_TD1: 0x40007BCC
PHUB_TDMEM122_ORIG_TD1: 0x40007BD4
PHUB_TDMEM123_ORIG_TD1: 0x40007BDC
PHUB_TDMEM124_ORIG_TD1: 0x40007BE4
PHUB_TDMEM125_ORIG_TD1: 0x40007BEC
PHUB_TDMEM126_ORIG_TD1: 0x40007BF4
PHUB_TDMEM127_ORIG_TD1: 0x40007BFC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	src_adr							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	src_adr							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							

1.3.1079 PHUB_TDMEM[0..127]_ORIG_TD1 (continued)

HW Access	R
Name	dst_adr

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	dst_adr							

Each channel will have a TD chain (as short as one TD in length) that provides instructions to the DMAC for carrying out a DMA sequence for the channel. This is described in greater detail in the 'TD Chains' section to follow. The TD chain is comprised of one or more CHn_ORIG_TD0/1 TDs. DMAC accesses the CHn_ORIG_TD0/1 chain from TDMEM and the address in TDMEM of the current TD in the chain is {TD_PTR[7:0], 000}. TD_PTR for the first TD in a chain is initialized by the CPU. As the chain progresses through TDs the TD_PTR will be automatically updated by DMAC to reflect the current TD being accessed in the chain. CHn_ORIG_TD0/1 are described in detail below.

Bits	Name	Description
31:16	dst_adr[15:0]	Specifies the lower portion of the full destination address by concatenating with DST_BASE_ADR from CHn_CFG1. Can be incremented or not depending on the setting of INC_DST_ADR. Only DST_ADR will increment; DST_BASE_ADR will remain static. Therefore, separate TDs should be used to cross 64KB address boundaries. If INC_DST_ADR=1 then when DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update DST_ADR to reflect the newly incremented value based on the number of bytes that were transferred to the destination during the burst.
15:0	src_adr[15:0]	Specifies the lower portion of the full source address by concatenating with SRC_BASE_ADR from CHn_CFG1. Can be incremented or not depending on the setting of INC_SRC_ADR. Only SRC_ADR will increment; SRC_BASE_ADR will remain static. Therefore, separate TDs should be used to cross 64KB address boundaries. If INC_SRC_ADR=1 then when DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update SRC_ADR to reflect the newly incremented value based on the number of bytes that were transferred from the source during the burst.

1.3.1080 CAN[0..0]_CSR_INT_SR

INT_SR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAN0_CSR_INT_SR: 0x4000A000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	NA:00	
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	NA	
Name	form_err	ack_err	stuff_err	bit_err	ovr_load	arb_loss		

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA			R/W	R/W	R/W	R/W	R/W
Name				rx_msg	tx_msg	rx_msg_loss	bus_off	crc_err

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The interrupt status register stores internal interrupt events. Once a bit is set it remains set until it is cleared by writing a '1' to it. The interrupt enable register has no effect on the interrupt status register. A pending interrupt occurs when the flag is set to '1'. To acknowledge an interrupt, set the flag to '1'

Bits	Name	Description
12	rx_msg	Msg Recieved
11	tx_msg	Tx msg Sent
10	rx_msg_loss	Rx msg loss Interrupt
9	bus_off	Bus Off State
8	crc_err	CRC Error Interrupt
7	form_err	Form Error Interrupt
6	ack_err	Ack Error Interrupt
5	stuff_err	Stuff Error Interrupt
4	bit_err	Bit Error Interrupt

1.3.1080 CAN[0..0]_CSR_INT_SR (continued)

3	ovr_load	Overload Interrupt
2	arb_loss	Arbitration Loss

1.3.1081 CAN[0..0]_CSR_INT_EN

INT_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAN0_CSR_INT_EN: 0x4000A004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0
HW Access	R	R	R	R	R	R	NA	R
Name	form_err	ack_err	stuff_err	bit_err	ovr_load	arb_loss		int_ebl

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				rx_msg	tx_msg	rx_msg_loss	bus_off	crc_err

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

A particular interrupt source is enabled by setting its respective flag to 1

Bits	Name	Description
12	rx_msg	Msg Recived
11	tx_msg	Tx Msg sent Interrupt
10	rx_msg_loss	Rx Msg Loss Interrupt Enable
9	bus_off	Busoff State Interrupt Enable
8	crc_err	CRC Error Interrupt Enable
7	form_err	Form Error Interrupt Enable
6	ack_err	Ack Error Interrupt Enable
5	stuff_err	Stuff Error Interrupt Enable
4	bit_err	Bit Error Interrupt Enable
3	ovr_load	Overload Interrupt Enable
2	arb_loss	Arbitration Loss Interrupt Enable

1.3.1081 CAN[0..0]_CSR_INT_EN (continued)

0	int_ebl	Global Interrupt enable Flag

1.3.1082 CAN[0..0]_CSR_BUF_SR

BUF_SR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAN0_CSR_BUF_SR: 0x4000A008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	rx_msg7	rx_msg6	rx_msg5	rx_msg4	rx_msg3	rx_msg2	rx_msg1	rx_msg0

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	rx_msg15	rx_msg14	rx_msg13	rx_msg12	rx_msg11	rx_msg10	rx_msg9	rx_msg8

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	tx_msg7	tx_msg6	tx_msg5	tx_msg4	tx_msg3	tx_msg2	tx_msg1	tx_msg0

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

These status indicators bundle the respective flags from all RxMessage and TxMessage buffers. Note All flags are read only. To acknowledge a MsgAv flag, the CPU must write to the respective RxMessage buffer.

Bits	Name	Description
23	tx_msg7	Tx req Pending for Tx Msg7
22	tx_msg6	Tx req Pending for Tx Msg6
21	tx_msg5	Tx req Pending for Tx Msg5
20	tx_msg4	Tx req Pending for Tx Msg4
19	tx_msg3	Tx req Pending for Tx Msg3
18	tx_msg2	Tx req Pending for Tx Msg2
17	tx_msg1	Tx req Pending for Tx Msg1
16	tx_msg0	Tx req Pending for Tx Msg0
15	rx_msg15	Rx Msg15 Available
14	rx_msg14	Rx Msg14 Available
13	rx_msg13	Rx Msg13 Available

1.3.1082 CAN[0..0]_CSR_BUF_SR (continued)

12	rx_msg12	Rx Msg12 Available
11	rx_msg11	Rx Msg11 Available
10	rx_msg10	Rx Msg10 Available
9	rx_msg9	Rx Msg9 Available
8	rx_msg8	Rx Msg8 Available
7	rx_msg7	Rx Msg7 Available
6	rx_msg6	Rx Msg6 Available
5	rx_msg5	Rx Msg5 Available
4	rx_msg4	Rx Msg4 Available
3	rx_msg3	Rx Msg3 Available
2	rx_msg2	Rx Msg2 Available
1	rx_msg1	Rx Msg1 Available
0	rx_msg0	Rx Msg0 Available

1.3.1083 CAN[0..0]_CSR_ERR_SR

ERR_SR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAN0_CSR_ERR_SR: 0x4000A00C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	tx_err_cnt							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	rx_err_cnt							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000				R:0	R:0	R:00	
HW Access	NA				R/W	R/W	R/W	
Name					rxgte96	txgte96	err_state	

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Status indicators are provided to report the CAN controller error state, receive error count, and transmit error count. Special flags report error counter values equal to or in excess of 96 errors are available to indicate heavily disturbed bus situations. The transmitter error counter according to the CAN standard. When it is greater than 255 Decomal, it is fixed at 255 Decimal.

Bits	Name	Description
19	rxgte96	Rx Error Count is greater or equal to 96 Decimal
18	txgte96	Tx Error Count is greater or equal to 96 Decimal
17:16	err_state[1:0]	Error State of CAN node, 00 error active, 01 error passive, 1x bus off
15:8	rx_err_cnt[7:0]	Rx error Count. When in bus-off state,this counter is used to count 128 groups of 11 recessive bits
7:0	tx_err_cnt[7:0]	Tx error Count

1.3.1084 CAN[0..0]_CSR_CMD

CMD

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAN0_CSR_CMD: 0x4000A010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	R/W:0
HW Access	NA				R	NA	R	R/W
Name					sram_test		listen	run_stop

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The CAN can be used in different operating mode,by disabling transmitting data,it is possible to use the CAN in listen only mode,enabling feature such as automatic bit rate detection,SRAM Test Mode

Bits	Name	Description
3	sram_test	SRAM test Mode. 0 Normal operation, 1 Enable SRAM test mode
1	listen	Listen only mode. 0 Active, 1 CAN listen only
0	run_stop	Run/Stop mode. 0 Sets the CAN controller to stop mode. Returns '1' when stopped, 1 Sets the CAN controller to run mode. Returns '1' when running

1.3.1085 CAN[0..0]_CSR_CFG

CFG

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAN0_CSR_CFG: 0x4000A014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000			R/W:0	R/W:00		R/W:0	R/W:0
HW Access	R			R	R		R	R
Name	cfg_tseg2			auto_rst	cfg_sjw		sampling_mode	edge_mode

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/W:0	R/W:0000			
HW Access	NA			R	R			
Name				cfg_arbiter	cfg_tseg1			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	cfg_bitrate							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R						
Name		cfg_bitrate						

CAN module has to be configured prior to use,this register define the effective CAN data rate,CAN data synchronization,message buffer arbitration

Bits	Name	Description
30:16	cfg_bitrate[14:0]	CAN configuration Bit rate. 0 equals 1 clock cycle, 1 equals 2 clock cycles, ..., 32767 equals 32768 clock cycles
12	cfg_arbiter	Tx buffer Arbiter. 0 Round robin arbitration, 1 Fixed priority arbitration
11:8	cfg_tseg1[3:0]	Length of time segment1
7:5	cfg_tseg2[2:0]	Length of time segment2
4	auto_rst	auto_restart. 0 After bus-off, the CAN must be restarted 'by hand'. This is the recommended setting, 1 After bus-off, the CAN is restarting automatically after 128 groups of 11 recessive bits
3:2	cfg_sjw[1:0]	Synchronization Jump Width
1	sampling_mode	CAN bus Bit sampling. 0 One sampling point is used in the receiver path, 1 Three sampling points with majority decision are used

1.3.1085 CAN[0..0]_CSR_CFG (continued)

0	edge_mode	CAN bus synchronization logic. 0 Edge from 'R' to 'D' is used for synchronization, 1 Both edges are used

1.3.1086 CAN[0..0]_TX[0..7]_CMD

TXCMD

Reset: N/A

Register : Address

CAN0_TX0_CMD: 0x4000A020
CAN0_TX1_CMD: 0x4000A030
CAN0_TX2_CMD: 0x4000A040
CAN0_TX3_CMD: 0x4000A050
CAN0_TX4_CMD: 0x4000A060
CAN0_TX5_CMD: 0x4000A070
CAN0_TX6_CMD: 0x4000A080
CAN0_TX7_CMD: 0x4000A090

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:U	R:U	R:U	R:U
HW Access	NA				R/W	R/W	R/W	R/W
Name					wpn1	txint_ebl	txabort	txreq

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	RSVD0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:UUUU			
HW Access	R/W	R/W	R	R	R			
Name	wpn2	RSVD1	rtr	ide	dlc			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	RSVD2							

This is the Interrupt Enable bit. 0 interrupt disabled. 1 interrupt enables, successful message transmission sets the TxMsg flag in the Interrupt Controller.

Bits	Name	Description
31:24	RSVD2[7:0]	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
23	Write Protect Bit (wpn2) {wpn2}	This Write Protect bit does not have a register within the RTL. It functions as a control input.Hence neither does it have a known reset value, nor can software read back a written value. The 0 or 1 Readback value for the bit comes as a Read to that register results in Memory data being sent out in that bit position, hence resulting in an unpredictable read value, completely independent of the written value.
22	RSVD1	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
21	rtr	RTR Remote bit. 0 Standard message, 1 RTR message
20	ide	Extended identifier. 0 Standard format message, 1 Extended format message

1.3.1086 CAN[0..0]_TX[0..7]_CMD (continued)

19:16	dlc[3:0]	Data Length of the Tx Msg. Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0 Message has 0 data byte, data[63:0] is not used, 1 Message has 1 data byte, data[63:56] is used, ..., 8 Message has 8 data bytes, data [63:0] is used, 9-15 Message has 8 data bytes
15:8	RSVD0[7:0]	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
3	wpn1	WPN Write protect not Flag. 0 Bit[2] remains unchanged, 1 Bit[2] is modified, default. This bit is always zero for readback
2	txint_ebl	Transmit Interrupt Enable. 0 Interrupt disabled, 1 Interrupt enabled, succesful message transmission setst the TxMsg flag in the interrupt controller
1	txabort	Transmit Abort Request. 0 idle, 1 Requests removal of a pending message. The message is removed the next time an arbitration loss happened. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time
0	txreq	Transmit Request. For Write: 0 Idle, 1 Message Transmit request. For Read: 0 TxReq completed, 1 TxReq pending

1.3.1087 CAN[0..0]_TX[0..7]_ID

TXID

Reset: N/A

Register : Address

CAN0_TX0_ID: 0x4000A024
CAN0_TX1_ID: 0x4000A034
CAN0_TX2_ID: 0x4000A044
CAN0_TX3_ID: 0x4000A054
CAN0_TX4_ID: 0x4000A064
CAN0_TX5_ID: 0x4000A074
CAN0_TX6_ID: 0x4000A084
CAN0_TX7_ID: 0x4000A094

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUU					NA:000		
HW Access	R					NA		
Name	id							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

CAN Tx Msg Identifier

Bits	Name	Description
31:3	id[28:0]	Tx Msg Indentifier

1.3.1088 CAN[0..0]_TX[0..7]_DH

TXDH

Reset: N/A

Register : Address

CAN0_TX0_DH: 0x4000A028
CAN0_TX1_DH: 0x4000A038
CAN0_TX2_DH: 0x4000A048
CAN0_TX3_DH: 0x4000A058
CAN0_TX4_DH: 0x4000A068
CAN0_TX5_DH: 0x4000A078
CAN0_TX6_DH: 0x4000A088
CAN0_TX7_DH: 0x4000A098

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_high							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_high							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_high							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_high							

CAN Tx Msg Upper Data Bytes

Bits	Name	Description
31:0	data_high[31:0]	Upper Date Bytes

1.3.1089 CAN[0..0]_TX[0..7]_DL

TXDL

Reset: N/A

Register : Address

CAN0_TX0_DL: 0x4000A02C
CAN0_TX1_DL: 0x4000A03C
CAN0_TX2_DL: 0x4000A04C
CAN0_TX3_DL: 0x4000A05C
CAN0_TX4_DL: 0x4000A06C
CAN0_TX5_DL: 0x4000A07C
CAN0_TX6_DL: 0x4000A08C
CAN0_TX7_DL: 0x4000A09C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_low							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_low							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_low							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_low							

CAN Tx Msg Lower Data Bytes

Bits	Name	Description
31:0	data_low[31:0]	Lower Data Bytes

1.3.1090 CAN[0..0]_RX[0..15]_CMD

RXCMD

Reset: N/A

Register : Address

CAN0_RX0_CMD: 0x4000A0A0	CAN0_RX1_CMD: 0x4000A0C0
CAN0_RX2_CMD: 0x4000A0E0	CAN0_RX3_CMD: 0x4000A100
CAN0_RX4_CMD: 0x4000A120	CAN0_RX5_CMD: 0x4000A140
CAN0_RX6_CMD: 0x4000A160	CAN0_RX7_CMD: 0x4000A180
CAN0_RX8_CMD: 0x4000A1A0	CAN0_RX9_CMD: 0x4000A1C0
CAN0_RX10_CMD: 0x4000A1E0	CAN0_RX11_CMD: 0x4000A200
CAN0_RX12_CMD: 0x4000A220	CAN0_RX13_CMD: 0x4000A240
CAN0_RX14_CMD: 0x4000A260	CAN0_RX15_CMD: 0x4000A280

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	wpnl	lk_flg	rx_int_ebl	rtr_rply	buf_ebl	rtr_abort	rtr_rpy_pnd	msg_av

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	RSVD0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:UUUU			
HW Access	R/W	R/W	R	R	R			
Name	wpnh	RSVD1	rtr	ide	dlc			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	RSVD2							

Rx Msg Control register have recieve interrupt enable,buffer enable,link flag,identifier

Bits	Name	Description
31:24	RSVD2[7:0]	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
23	Write Protect Bit (wpnh) {wpnh}	This Write Protect bit does not have a register within the RTL. It functions as a control input.Hence neither does it have a known reset value, nor can software read back a written value. The 0 or 1 Readback value for the bit comes as a Read to that register results in Memory data being sent out in that bit position, hence resulting in an unpredictable read value, completely independent of the written value.

1.3.1090 CAN[0..0]_RX[0..15]_CMD (continued)

22	RSVD1	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
21	rtr	RTR Remote Bit.0 This is a regular message, 1 This is an RTR message
20	ide	Extended Identifier Bit. 0 This is a standard format message, 1 This is an extended format message
19:16	dlc[3:0]	Data Length Code. 0 Message has 0 data bytes, data[63:0] is not valid, 1 Message has 1 data byte, data[63:56] is valid, ..., 8 Message has 8 data bytes, data [63:0] is valid, 9-15 Message has 8 data bytes
15:8	RSVD0[7:0]	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
7	wpnl	WPNL Write Protect Not Low flag. 0 Bits[6:3] remain unchanged, 1 Bits[6:3] are modified, default. The bit is always zero for readback
6	lk_flg	Link Flag used to link the Rx Buffer. 0 This buffer is not linked to the next, 1 This biffer is linked with the next buffer
5	rx_int_ebl	Recieve Interrupt Enable. 0 Interrupt generation is disabled, 1 Interrupt generation is enabled
4	rtr_rply	Automatic RTR Message Handling. 0 Automatic RTR message handling disabled, 1 Automatic RTR message handling enabled
3	buf_ebl	Buffer Enable. 0 Buffer is disabled, 1 Buffer is enabled
2	rtr_abort	RTR Abort Request. 0 Idle, 1 Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time.
1	rtr_rpy_pnd	RTR Reply request Pending. 0 No RTR reply request pending, 1 RTR reply request pending
0	msg_av	Message Available. For Read: 0 No new message available, 1 New message available. For Write: 0 Idle, 1 Acknowledges receipt of new message

1.3.1091 CAN[0..0]_RX[0..15]_ID

RXID

Reset: N/A

Register : Address

CAN0_RX0_ID: 0x4000A0A4	CAN0_RX1_ID: 0x4000A0C4
CAN0_RX2_ID: 0x4000A0E4	CAN0_RX3_ID: 0x4000A104
CAN0_RX4_ID: 0x4000A124	CAN0_RX5_ID: 0x4000A144
CAN0_RX6_ID: 0x4000A164	CAN0_RX7_ID: 0x4000A184
CAN0_RX8_ID: 0x4000A1A4	CAN0_RX9_ID: 0x4000A1C4
CAN0_RX10_ID: 0x4000A1E4	CAN0_RX11_ID: 0x4000A204
CAN0_RX12_ID: 0x4000A224	CAN0_RX13_ID: 0x4000A244
CAN0_RX14_ID: 0x4000A264	CAN0_RX15_ID: 0x4000A284

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUU					R/W:UUU		
HW Access	R					R		
Name	id					zeroes		

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

The register contains Rx Msg Identifier

Bits	Name	Description
31:3	id[28:0]	Rx Msg Identifier
2:0	zeroes[2:0]	zeros

1.3.1092 CAN[0..0]_RX[0..15]_DH

RXDH

Reset: N/A

Register : Address

CAN0_RX0_DH: 0x4000A0A8	CAN0_RX1_DH: 0x4000A0C8
CAN0_RX2_DH: 0x4000A0E8	CAN0_RX3_DH: 0x4000A108
CAN0_RX4_DH: 0x4000A128	CAN0_RX5_DH: 0x4000A148
CAN0_RX6_DH: 0x4000A168	CAN0_RX7_DH: 0x4000A188
CAN0_RX8_DH: 0x4000A1A8	CAN0_RX9_DH: 0x4000A1C8
CAN0_RX10_DH: 0x4000A1E8	CAN0_RX11_DH: 0x4000A208
CAN0_RX12_DH: 0x4000A228	CAN0_RX13_DH: 0x4000A248
CAN0_RX14_DH: 0x4000A268	CAN0_RX15_DH: 0x4000A288

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_high							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_high							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_high							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_high							

The register contains the Upper Data Bytes

Bits	Name	Description
31:0	data_high[31:0]	Upper Data bytes

1.3.1093 CAN[0..0]_RX[0..15]_DL

RXDL

Reset: N/A

Register : Address

CAN0_RX0_DL: 0x4000A0AC	CAN0_RX1_DL: 0x4000A0CC
CAN0_RX2_DL: 0x4000A0EC	CAN0_RX3_DL: 0x4000A10C
CAN0_RX4_DL: 0x4000A12C	CAN0_RX5_DL: 0x4000A14C
CAN0_RX6_DL: 0x4000A16C	CAN0_RX7_DL: 0x4000A18C
CAN0_RX8_DL: 0x4000A1AC	CAN0_RX9_DL: 0x4000A1CC
CAN0_RX10_DL: 0x4000A1EC	CAN0_RX11_DL: 0x4000A20C
CAN0_RX12_DL: 0x4000A22C	CAN0_RX13_DL: 0x4000A24C
CAN0_RX14_DL: 0x4000A26C	CAN0_RX15_DL: 0x4000A28C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data							

The Register Contains the Lower data bytes

Bits	Name	Description
31:0	data[31:0]	Lower Data bytes

1.3.1094 CAN[0..0]_RX[0..15]_AMR

RXAMR

Reset: N/A

Register : Address

CAN0_RX0_AMR: 0x4000A0B0	CAN0_RX1_AMR: 0x4000A0D0
CAN0_RX2_AMR: 0x4000A0F0	CAN0_RX3_AMR: 0x4000A110
CAN0_RX4_AMR: 0x4000A130	CAN0_RX5_AMR: 0x4000A150
CAN0_RX6_AMR: 0x4000A170	CAN0_RX7_AMR: 0x4000A190
CAN0_RX8_AMR: 0x4000A1B0	CAN0_RX9_AMR: 0x4000A1D0
CAN0_RX10_AMR: 0x4000A1F0	CAN0_RX11_AMR: 0x4000A210
CAN0_RX12_AMR: 0x4000A230	CAN0_RX13_AMR: 0x4000A250
CAN0_RX14_AMR: 0x4000A270	CAN0_RX15_AMR: 0x4000A290

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUU					R/W:U	R/W:U	NA:0
HW Access	R					R	R	NA
Name	id					ide	rtr	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

The Register contains the Acceptance mask value

Bits	Name	Description
31:3	id[28:0]	Identifier
2	ide	Extended Identifier
1	rtr	RTR Bit

1.3.1095 CAN[0..0]_RX[0..15]_ACR

RXACR

Reset: N/A

Register : Address

CAN0_RX0_ACR: 0x4000A0B4	CAN0_RX1_ACR: 0x4000A0D4
CAN0_RX2_ACR: 0x4000A0F4	CAN0_RX3_ACR: 0x4000A114
CAN0_RX4_ACR: 0x4000A134	CAN0_RX5_ACR: 0x4000A154
CAN0_RX6_ACR: 0x4000A174	CAN0_RX7_ACR: 0x4000A194
CAN0_RX8_ACR: 0x4000A1B4	CAN0_RX9_ACR: 0x4000A1D4
CAN0_RX10_ACR: 0x4000A1F4	CAN0_RX11_ACR: 0x4000A214
CAN0_RX12_ACR: 0x4000A234	CAN0_RX13_ACR: 0x4000A254
CAN0_RX14_ACR: 0x4000A274	CAN0_RX15_ACR: 0x4000A294

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUU					R/W:U	R/W:U	NA:0
HW Access	R					R	R	NA
Name	id					ide	rtr	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	id							

The Register contains the Acceptance Code value

Bits	Name	Description
31:3	id[28:0]	Identifier
2	ide	Extended Identifier
1	rtr	RTR Bit

1.3.1096 CAN[0..0]_RX[0..15]_AMRD

RXAMRD

Reset: N/A

Register : Address

CAN0_RX0_AMRD: 0x4000A0B8	CAN0_RX1_AMRD: 0x4000A0D8
CAN0_RX2_AMRD: 0x4000A0F8	CAN0_RX3_AMRD: 0x4000A118
CAN0_RX4_AMRD: 0x4000A138	CAN0_RX5_AMRD: 0x4000A158
CAN0_RX6_AMRD: 0x4000A178	CAN0_RX7_AMRD: 0x4000A198
CAN0_RX8_AMRD: 0x4000A1B8	CAN0_RX9_AMRD: 0x4000A1D8
CAN0_RX10_AMRD: 0x4000A1F8	CAN0_RX11_AMRD: 0x4000A218
CAN0_RX12_AMRD: 0x4000A238	CAN0_RX13_AMRD: 0x4000A258
CAN0_RX14_AMRD: 0x4000A278	CAN0_RX15_AMRD: 0x4000A298

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_lsb							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_lsb							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The register conatins the Acceptance mask data

Bits	Name	Description
15:0	data_lsb[15:0]	Upper 2 Bytes of Data

1.3.1097 CAN[0..0]_RX[0..15]_ACRD

RXACRD

Reset: N/A

Register : Address

CAN0_RX0_ACRD: 0x4000A0BC	CAN0_RX1_ACRD: 0x4000A0DC
CAN0_RX2_ACRD: 0x4000A0FC	CAN0_RX3_ACRD: 0x4000A11C
CAN0_RX4_ACRD: 0x4000A13C	CAN0_RX5_ACRD: 0x4000A15C
CAN0_RX6_ACRD: 0x4000A17C	CAN0_RX7_ACRD: 0x4000A19C
CAN0_RX8_ACRD: 0x4000A1BC	CAN0_RX9_ACRD: 0x4000A1DC
CAN0_RX10_ACRD: 0x4000A1FC	CAN0_RX11_ACRD: 0x4000A21C
CAN0_RX12_ACRD: 0x4000A23C	CAN0_RX13_ACRD: 0x4000A25C
CAN0_RX14_ACRD: 0x4000A27C	CAN0_RX15_ACRD: 0x4000A29C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_lsb							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	data_lsb							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The register conatins the Acceptance code data

Bits	Name	Description
15:0	data_lsb[15:0]	Upper 2 Bytes of Data

1.3.1098 DFB[0..0]_DPA_SRAM_DATA[0..127]

Data RAM A

Reset: N/A

Register : Address

DFB_DPA_SRAM_DATA: 0x4000C000-0x4000C1FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Data Storage SRAM

Bits	Name	Description
23:0	sramdata[23:0]	(no description)

1.3.1099 DFB[0..0]_DPB_SRAM_DATA[0..127]

DFB Data RAM B

Reset: N/A

Register : Address

DFB_DPB_SRAM_DATA: 0x4000C200-0x4000C3FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Data Storage SRAM

Bits	Name	Description
23:0	sramdata[23:0]	(no description)

1.3.1100 DFB[0..0]_CSA_SRAM_DATA[0..63]

DFB Control Store A

Reset: N/A

Register : Address

DFB_CSA_SRAM_DATA: 0x4000C400-0x4000C4FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Control Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.1101 DFB[0..0]_CSB_SRAM_DATA[0..63]

DFB Control Store B

Reset: N/A

Register : Address

DFB_CSB_SRAM_DATA: 0x4000C500-0x4000C5FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Control Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.1102 DFB[0..0]_FSM_SRAM_DATA[0..63]

DFB Code Store B

Reset: N/A

Register : Address

DFB_FSM_SRAM_DATA: 0x4000C600-0x4000C6FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Code Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.1103 DFB[0..0]_ACU_SRAM_DATA[0..15]

DFB Address Store

Reset: N/A

Register : Address

DFB_ACU_SRAM_DATA: 0x4000C700-0x4000C73F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:UUUUUU					
HW Access	NA		R/W					
Name			sramdata					

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Address Storage SRAM

Bits	Name	Description
13:0	sramdata[13:0]	(no description)

1.3.1104 DFB[0..0]_CR

DFB Command Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_CR: 0x4000C780

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						CORECLK_DISABLE	ADDR6	RUN

This register enables/disables DFB operation and sets FSM memory bank. Also, the internal core clock gater is controlled. A read of this register produces the last value written to this register.

Bits	Name	Description
2	CORECLK_DISABLE	This bit controls the clock gating of the Core clock. See Table 1-697.
1	ADDR6	This bit is address bit 6 of the FSM RAM. See Table 1-696.
0	RUN	DFB operation enable / disable. See Table 1-698.

Table 1-696. Bit field encoding: addr6_enum

Value	Name	Description
1'b1	ADDR6_HIGH	ADDR6 is High
1'b0	ADDR6_LOW	ADDR6 is Low

Table 1-697. Bit field encoding: coreclk_disable_enum

Value	Name	Description
1'b1	CORECLK_DISABLE_HIGH	Core Clock is Disabled (gated)
1'b0	CORECLK_DISABLE_LOW	Core Clock is Enabled

Table 1-698. Bit field encoding: run_bit_enum

Value	Name	Description
1'b1	RUN_EN	DFB is enabled to operate.
1'b0	RUN_DIS	DFB operation is halted.

1.3.1105 DFB[0..0]_SR

DFB Status Register

Reset: Reset Signals Listed Below

Register : Address

DFB0_SR: 0x4000C784

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R:U	R:U	R:U
HW Access	W	W	W	W	W	W	W	W
Name	INTR_SEM 2	INTR_SEM 1	INTR_SEM 0	INTR_HOL DB	INTR_HOL DA	RND_MOD E	SAT_MODE	RAM_SEL

This register provides status of the current operating state of the DFB.

Bits	Name	Description
7	INTR_SEM2	Indicates a pending Semaphore 2 interrupt See Table 1-703.
6	INTR_SEM1	Indicates a pending Semaphore 1 interrupt See Table 1-702.
5	INTR_SEM0	Indicates a pending Semaphore 0 interrupt See Table 1-701.
4	INTR_HOLDB	Indicates a pending Hold B interrupt See Table 1-700.
3	INTR_HOLDA	Indicates a pending Hold A interrupt See Table 1-699.
2	RND_MODE	Indicates the state of the Round flag in the Datapath Unit. See Table 1-705.
1	SAT_MODE	Indicates the state of the Saturation flag in the ALU. See Table 1-706.
0	RAM_SEL	This bit indicates which Control Store memory is in use, RAM A or RAM B. See Table 1-704.

Reset Table

resetsignal	field(s)
N/A	RAM_SEL, SAT_MODE, RND_MODE

1.3.1105 DFB[0..0]_SR (continued)

Reset Table

Domain reset for non-retention flops [reset_all_nonretention]	INTR_HOLDA, INTR_HOLDB, INTR_SEM0, INTR_SEM1, INTR_SEM2

Table 1-699. Bit field encoding: intr_holda_enum

Value	Name	Description
1'b0	HOLDA_OFF	Indicates no pending Holding A Register Interrupt.
1'b1	HOLDA_ON	Indicates a pending Holding A Register Interrupt.

Table 1-700. Bit field encoding: intr_holdb_enum

Value	Name	Description
1'b0	HOLDB_OFF	Indicates no pending Holding B Register Interrupt.
1'b1	HOLDB_ON	Indicates a pending Holding B Register Interrupt.

Table 1-701. Bit field encoding: intr_sem0_enum

Value	Name	Description
1'b0	SEM0_OFF	Indicates no pending Semaphore 0 Interrupt.
1'b1	SEM0_ON	Indicates a pending Semaphore 0 Interrupt.

Table 1-702. Bit field encoding: intr_sem1_enum

Value	Name	Description
1'b0	SEM1_OFF	Indicates no pending Semaphore 1 Interrupt.
1'b1	SEM1_ON	Indicates a pending Semaphore 1 Interrupt.

Table 1-703. Bit field encoding: intr_sem2_enum

Value	Name	Description
1'b0	SEM2_OFF	Indicates no pending Semaphore 2 Interrupt.
1'b1	SEM2_ON	Indicates a pending Semaphore 2 Interrupt.

Table 1-704. Bit field encoding: ram_select_bit_enum

Value	Name	Description
1'b0	RAMSEL_LOW	Control Store memory A is in use.
1'b1	RAMSEL_HIGH	Control Store memory B is in use.

Table 1-705. Bit field encoding: rnd_mode_enum

Value	Name	Description
1'b0	RND_OFF	Indicates Round Mode is off.
1'b1	RND_ON	Indicates Round Mode is on.

Table 1-706. Bit field encoding: sat_mode_enum

Value	Name	Description
1'b0	SAT_OFF	Indicates Saturation mode is off.
1'b1	SAT_ON	Indicates Saturation mode is on.

1.3.1106 DFB[0..0]_RAM_EN

DFB RAM Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_RAM_EN: 0x4000C788

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R		R	R	R	R	R	R
Name	RAMWR_ADDRING		DPB_EN	DPA_EN	ACU_EN	CSB_EN	CSA_EN	FSM_EN

This register controls the DFB memory enables. These bits are tied directly to the enable pins of the RAMs in this block and should be used by System SW to power-down RAMs not in use. A read of this register produces the last value written to this register.

Bits	Name	Description
7:6	RAMWR_ADDRING[1:0]	These two bits control the write addressing of the 4 largest RAMs embedded in the DFB (CS-A, CS-B, Data-A, Data-B). The setting of these bits allows overlaid writes to occur to these memories when it is desired to fill them with like data. This feature is primarily intended to enhance SW BIST test time but may also have functional uses as well like filling both CS RAMs concurrently as they typically hold identical data. Setting these bits to 01, for example, configures the HW to write to both CS-A and CS-B for any write to the address space of either CS-A or CS-B. Reads are not affected by these bits. See Table 1-708.
5	DPB_EN	Datapath RAM B RAM enable / disable. See Table 1-707.
4	DPA_EN	Datapath RAM A RAM enable / disable. See Table 1-707.
3	ACU_EN	ACU RAM RAM enable / disable. See Table 1-707.
2	CSB_EN	Control Store RAM B RAM enable / disable. See Table 1-707.
1	CSA_EN	Control Store RAM A RAM enable / disable. See Table 1-707.
0	FSM_EN	FSM RAM RAM enable / disable. See Table 1-707.

Table 1-707. Bit field encoding: ram_enable_bit_enum

Value	Name	Description
1'b1	RAM_EN	RAM is enabled.
1'b0	RAM_DIS	RAM is disabled.

Table 1-708. Bit field encoding: ram_write_addressing_bits_enum

Value	Name	Description

1.3.1106 DFB[0..0]_RAM_EN (continued)

Table 1-708. Bit field encoding: ram_write_addressing_bits_enum

2'b00	NO_OVERLAY	No overlay mapping.
2'b11	OVERLAY_CS_A_CS_B	Overlay CS A with CS B.
2'b10	OVERLAY_DATA_A_DATA_B	Overlay Data A with Data B.
2'b11	OVERLAY_CS_AB_DATA_AB	Overlay CS A/B with Data A with DATA B.

1.3.1107 DFB[0..0]_RAM_DIR

DFB RAM Direction Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_RAM_DIR: 0x4000C78C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1
HW Access	NA	R	R	R	R	R	R	R
Name		SNP_DABLE	DPB_DIR	DPA_DIR	ACU_DIR	CSB_DIR	CSA_DIR	FSM_DIR

This register controls the DFB memory direction. These bits control if each RAM of this block is embedded to the DFB function or mapped in the system address space on the AHB bus. Mapping to the bus facilitates SW BIST, Configuration filling, and Block Mode transfers. A read to this register returns what was last written. When programming code into the CSA/B and FSM RAMs the RAM_DIR bits should be set and unset together.

Bits	Name	Description
6	SNP_DABLE	RAM Read Address Snoop Disable See Table 1-710.
5	DPB_DIR	Datapath RAM B RAM Direction. See Table 1-709.
4	DPA_DIR	Datapath RAM A RAM Direction. See Table 1-709.
3	ACU_DIR	ACU RAM RAM Direction. See Table 1-709.
2	CSB_DIR	Control Store RAM B RAM Direction. See Table 1-709.
1	CSA_DIR	Control Store RAM A RAM Direction. See Table 1-709.
0	FSM_DIR	FSM RAM RAM Direction. See Table 1-709.

Table 1-709. Bit field encoding: ram_direction_bit_enum

Value	Name	Description
1'b1	RAM_AHB	System Bus
1'b0	RAM_DFB	DFB

Table 1-710. Bit field encoding: snoop_disable_bit_enum

Value	Name	Description
1'b1	SNP_DISABLE	Disabled
1'b0	SNP_ENABLE	Enabled

1.3.1108 DFB[0..0]_SEMA

DFB Semaphore Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_SEMA: 0x4000C790

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Name		SEMA_MASK				SEMA		

This register controls the DFB Semaphore register. These bits are used to pass semaphores between the DFB Controller and the System SW. Their definition is user defined. A read to this register returns what was last written by either System SW or the DFB Controller.

Bits	Name	Description
6:4	SEMA_MASK[2:0]	Semaphore Mask Bits for use by System and DFB Controller SW.
2:0	SEMA[2:0]	Semaphore Bits for use by System and DFB Controller SW.

1.3.1109 DFB[0..0]_DSI_CTRL

DFB Global Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DSI_CTRL: 0x4000C794

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		R/W:00	
HW Access	NA				R		R	
Name					GBL2_OUT		GBL1_OUT	

This register controls what internal signals are mapped to the primary output global signals. A read of this register produces the last value written to this register.

Bits	Name	Description
3:2	GBL2_OUT[1:0]	These bits are used to control what internal signals are mapped to the primary output signal global02. See Table 1-712.
1:0	GBL1_OUT[1:0]	These bits are used to control what internal signals are mapped to the primary output signal global01. See Table 1-711.

Table 1-711. Bit field encoding: global_output_1_encoding_bits_enum

Value	Name	Description
2'b00	DFB_RUN	DFB RUN Bit
2'b01	SEM0	Semaphore Bit 0.
2'b10	SEM1	Semaphore Bit 1.
2'b11	DFB_INTR	DFB Interrupt Bit.

Table 1-712. Bit field encoding: global_output_2_encoding_bits_enum

Value	Name	Description
2'b00	SEM2	Semaphore Bit 2.
2'b01	DPSIGN	DP Sign.
2'b10	DPTHREASH	DP Threashold.
2'b11	DPEQ	DP EQ.

1.3.1110 DFB[0..0]_INT_CTRL

DFB Interrupt Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_INT_CTRL: 0x4000C798

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				SEMA2_EN	SEMA1_EN	SEMA0_EN	HOLDB_EN	HOLDA_EN

This register allows control of what events generate an interrupt. Each of the events enabled by the bits in this register are ORed together to produce the dfb_intr signal. A read to this register returns what was last written.

Bits	Name	Description
4	SEMA2_EN	Interrupt mask to Semaphore register 2. See Table 1-714.
3	SEMA1_EN	Interrupt mask to Semaphore register 1. See Table 1-714.
2	SEMA0_EN	Interrupt mask to Semaphore register 0. See Table 1-714.
1	HOLDB_EN	Interrupt mask to enable holding register B. See Table 1-713.
0	HOLDA_EN	Interrupt mask to enable holding register A. See Table 1-713.

Table 1-713. Bit field encoding: enable_holding_reg_bit_enum

Value	Name	Description
1'b1	ENABLE_HOLDING_IRQ_EN	Interrupt is generated each time new valid data is written inot the output Holding register.
1'b0	ENABLE_HOLDING_IRQ_DIS	Holding register interrupt masked.

Table 1-714. Bit field encoding: enable_semaphore_bit_enum

Value	Name	Description
1'b1	ENABLE_SEMAPHORE_IRQ_EN	Interrupt is generated each time a 1 is written to the semaphore register.
1'b0	ENABLE_SEMAPHORE_IRQ_DIS	Semaphore register interrupt masked.

1.3.1111 DFB[0..0]_DMA_CTRL

DFB DMAREQ Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DMA_CTRL: 0x4000C79C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		R/W:00	
HW Access	NA				R		R	
Name					DMAREQ2		DMAREQ1	

This register allows control of what events generate DMAREQ events. Each field allows the user to configure what event drives each of the two DMAREQ primary output signals. A read to this register returns what was last written. When a semaphore is programmed to be a DMAREQ, the HW makes it a 1-cycle pulse by clearing writes of 1's after one clock. If a Holding register is selected, the DMAREQ is level sensed and stays asserted until the Holding register is read.

Bits	Name	Description
3:2	DMAREQ2[1:0]	The value in these two bits selects which event drives dma_req2. See Table 1-716.
1:0	DMAREQ1[1:0]	The value in these two bits selects which event drives dma_req1. See Table 1-715.

Table 1-715. Bit field encoding: dma_req_1_source_bits_enum

Value	Name	Description
2'b00	DMAREQ1_DISABLED	Disabled
2'b01	DMAREQ1_HOLDING_REG_A	New data in Holding Register A.
2'b10	DMAREQ1_SEMAPHORE_0	Semaphore 0.
2'b11	DMAREQ1_SEMAPHORE_1	Semaphore 1.

Table 1-716. Bit field encoding: dma_req_2_source_bits_enum

Value	Name	Description
2'b00	DMAREQ2_DISABLED	Disabled
2'b01	DMAREQ2_HOLDING_REG_B	New data in Holding Register B.
2'b10	DMAREQ2_SEMAPHORE_0	Semaphore 0.
2'b11	DMAREQ2_SEMAPHORE_1	Semaphore 1.

1.3.1112 DFB[0..0]_STAGEA

DFB Low Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEA: 0x4000C7A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	STGA_LOW							

This register is the low byte of the Streaming input Staging Register Port A. A read to this register returns what was last written.

Bits	Name	Description
7:0	STGA_LOW[7:0]	A write to this register sets the low byte of the input Staging Register for Port A.

1.3.1113 DFB[0..0]_STAGEAM

DFB Middle Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEAM: 0x4000C7A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	STGA_MID							

This register is the middle byte of the Streaming input Staging Register Port A. A read to this register returns what was last written.

Bits	Name	Description
7:0	STGA_MID[7:0]	A write to this register sets the middle byte of the input Staging Register for Port A.

1.3.1114 DFB[0..0]_STAGEAH

DFB High Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEAH: 0x4000C7A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	STGA_HIGH							

This register is the high byte of the Streaming input Staging Register Port A. A read to this register returns what was last written.

Bits	Name	Description
7:0	STGA_HIGH[7:0]	A write to this register sets the high byte of the input Staging Register for Port A.

1.3.1115 DFB[0..0]_STAGEB

DFB Low Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEB: 0x4000C7A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	STGB_LOW							

This register is the low byte of the Streaming input Staging Register Port B. A read to this register returns what was last written.

Bits	Name	Description
7:0	STGB_LOW[7:0]	A write to this register sets the low byte of the input Staging Register for Port B.

1.3.1116 DFB[0..0]_STAGEBM

DFB Middle Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEBM: 0x4000C7A5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	STGB_MID							

This register is the middle byte of the Streaming input Staging Register Port B. A read to this register returns what was last written.

Bits	Name	Description
7:0	STGB_MID[7:0]	A write to this register sets the middle byte of the input Staging Register for Port B.

1.3.1117 DFB[0..0]_STAGEBH

DFB High Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEBH: 0x4000C7A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	STGB_HIGH							

This register is the high byte of the Streaming input Staging Register Port B. A read to this register returns what was last written.

Bits	Name	Description
7:0	STGB_HIGH[7:0]	A write to this register sets the high byte of the input Staging Register for Port B.

1.3.1118 DFB[0..0]_HOLDA

DFB Low Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDA: 0x4000C7A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	HOLDA_LOW							

This register is the low byte of the output Holding Register Port A. A read of this register returns the last result generated by the DFB.

Bits	Name	Description
7:0	HOLDA_LOW[7:0]	Low byte of the output Holding Register, Port A.

1.3.1119 DFB[0..0]_HOLDAM

DFB Middle Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAM: 0x4000C7A9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	HOLDA_MID							

This register is the middle byte of the output Holding Register Port A. A read of this register returns the last result generated by the DFB.

Bits	Name	Description
7:0	HOLDA_MID[7:0]	Middle byte of the output Holding Register, Port A.

1.3.1120 DFB[0..0]_HOLDAH

DFB High Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAH: 0x4000C7AA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	HOLDA_HIGH							

This register is the high byte of the output Holding Register Port A. A read of this register returns the last result generated by the DFB.

Bits	Name	Description
7:0	HOLDA_HIGH[7:0]	High byte of the output Holding Register, Port A.

1.3.1121 DFB[0..0]_HOLDAS

DFB Holding Register A Sign Extension

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAS: 0x4000C7AB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	HOLDA_SIGNEXT							

This register is read-only and always contains 0x0 if read as a byte and contains the sign extension of the value in HOLDA if HOLDA is read as a word or HOLDAH is read as 16-bits.

Bits	Name	Description
7:0	HOLDA_SIGNEXT[7:0]	Output Holding Register Sign Extension, Port A.

1.3.1122 DFB[0..0]_HOLDB

DFB Low Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDB: 0x4000C7AC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	HOLDB_LOW							

This register is the low byte of the output Holding Register Port B. A read of this register returns the last result generated by the DFB.

Bits	Name	Description
7:0	HOLDB_LOW[7:0]	Low byte of the output Holding Register, Port B.

1.3.1123 DFB[0..0]_HOLDBM

DFB Middle Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBM: 0x4000C7AD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	HOLDB_MID							

This register is the middle byte of the output Holding Register Port B. A read of this register returns the last result generated by the DFB.

Bits	Name	Description
7:0	HOLDB_MID[7:0]	Middle byte of the output Holding Register, Port B.

1.3.1124 DFB[0..0]_HOLDBH

DFB High Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBH: 0x4000C7AE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	HOLDB_HIGH							

This register is the high byte of the output Holding Register Port B. A read of this register returns the last result generated by the DFB.

Bits	Name	Description
7:0	HOLDB_HIGH[7:0]	High byte of the output Holding Register, Port B.

1.3.1125 DFB[0..0]_HOLDBS

DFB Holding Register B Sign Extension

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBS: 0x4000C7AF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Name	HOLDB_SIGNEXT							

This register is read-only and always contains 0x0 if read as a byte and contains the sign extension of the value in HOLDB if HOLDB is read as a word or HOLDBH is read as 16-bits.

Bits	Name	Description
7:0	HOLDB_SIGNEXT[7:0]	Output Holding Register Sign Extension, Port B.

1.3.1126 DFB[0..0]_COHER

DFB Coherency Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_COHER: 0x4000C7B0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:10		R/W:10		R/W:10		R/W:10	
HW Access	R		R		R		R	
Name	holdb_key		holda_key		stgb_key		stga_key	

The 4 2-bit fields of this register are used to select which of the 3 bytes of each of the STAGEA, STAGEB, HOLDA and HOLDB will be used as the Key Coherency Byte.

Bits	Name	Description
7:6	holdb_key[1:0]	Sets the Key Coherency Byte of the Holding B register See Table 1-718.
5:4	holda_key[1:0]	Sets the Key Coherency Byte of the Holding A register See Table 1-717.
3:2	stgb_key[1:0]	Sets the Key Coherency Byte of the Staging B register See Table 1-720.
1:0	stga_key[1:0]	Sets the Key Coherency Byte of the Staging A register See Table 1-719.

Table 1-717. Bit field encoding: holda_key_enum

Value	Name	Description
2'b00	HOLDA_KEY_LOW	Key Byte is low byte.
2'b01	HOLDA_KEY_MID	Key Byte is med byte.
2'b10	HOLDA_KEY_HIGH	Key Byte is high byte.

Table 1-718. Bit field encoding: holdb_key_enum

Value	Name	Description
2'b00	HOLDB_KEY_LOW	Key Byte is low byte.
2'b01	HOLDB_KEY_MID	Key Byte is med byte.
2'b10	HOLDB_KEY_HIGH	Key Byte is high byte.

Table 1-719. Bit field encoding: stga_key_enum

Value	Name	Description
2'b00	STGA_KEY_LOW	Key Byte is low byte.
2'b01	STGA_KEY_MID	Key Byte is med byte.
2'b10	STGA_KEY_HIGH	Key Byte is high byte.

Table 1-720. Bit field encoding: stgb_key_enum

Value	Name	Description
2'b00	STGB_KEY_LOW	Key Byte is low byte.
2'b01	STGB_KEY_MID	Key Byte is med byte.
2'b10	STGB_KEY_HIGH	Key Byte is high byte.

1.3.1127 DFB[0..0]_DALIGN

DFB Data Alignment Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DALIGN: 0x4000C7B4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					holdb_dalign	holda_dalign	stgb_dalign	stga_dalign

The 4 bits of this register are used to select data alignment of the 4 registers STAGEA, STAGEB, HOLDA and HOLDB. If the bit is set high the STAGE registers will shift left on writes and the HOLD registers will shift right on reads, both by 8-bits.

Bits	Name	Description
3	holdb_dalign	Shifts the read right by a byte. See Table 1-722.
2	holda_dalign	Shifts the read right by a byte. See Table 1-721.
1	stgb_dalign	Shifts the write left by a byte. See Table 1-724.
0	stga_dalign	Shifts the write left by a byte. See Table 1-723.

Table 1-721. Bit field encoding: holda_dalign_enum

Value	Name	Description
1'b0	HOLDA_DALIGN_LOW	Reads normally.
1'b1	HOLDA_DALIGN_HIGH	Reads shifted right by 8-bits.

Table 1-722. Bit field encoding: holdb_dalign_enum

Value	Name	Description
1'b0	HOLDB_DALIGN_LOW	Reads normally.
1'b1	HOLDB_DALIGN_HIGH	Reads shifted right by 8-bits.

Table 1-723. Bit field encoding: stga_dalign_enum

Value	Name	Description
1'b0	STGA_DALIGN_LOW	Writes normally.
1'b1	STGA_DALIGN_HIGH	Writes shifted left by 8-bits.

Table 1-724. Bit field encoding: stgb_dalign_enum

Value	Name	Description
1'b0	STGB_DALIGN_LOW	Writes normally.
1'b1	STGB_DALIGN_HIGH	Writes shifted left by 8-bits.

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11]

PLD_IT

Reset: N/A

Register : Address

B0_P0_U0_PLD_IT0: 0x40010000
B0_P0_U0_PLD_IT1: 0x40010004
B0_P0_U0_PLD_IT2: 0x40010008
B0_P0_U0_PLD_IT3: 0x4001000C
B0_P0_U0_PLD_IT4: 0x40010010
B0_P0_U0_PLD_IT5: 0x40010014
B0_P0_U0_PLD_IT6: 0x40010018
B0_P0_U0_PLD_IT7: 0x4001001C
B0_P0_U0_PLD_IT8: 0x40010020
B0_P0_U0_PLD_IT9: 0x40010024
B0_P0_U0_PLD_IT10: 0x40010028
B0_P0_U0_PLD_IT11: 0x4001002C
B0_P0_U1_PLD_IT0: 0x40010080
B0_P0_U1_PLD_IT1: 0x40010084
B0_P0_U1_PLD_IT2: 0x40010088
B0_P0_U1_PLD_IT3: 0x4001008C
B0_P0_U1_PLD_IT4: 0x40010090
B0_P0_U1_PLD_IT5: 0x40010094
B0_P0_U1_PLD_IT6: 0x40010098
B0_P0_U1_PLD_IT7: 0x4001009C
B0_P0_U1_PLD_IT8: 0x400100A0
B0_P0_U1_PLD_IT9: 0x400100A4
B0_P0_U1_PLD_IT10: 0x400100A8
B0_P0_U1_PLD_IT11: 0x400100AC
B0_P1_U0_PLD_IT0: 0x40010200
B0_P1_U0_PLD_IT1: 0x40010204
B0_P1_U0_PLD_IT2: 0x40010208
B0_P1_U0_PLD_IT3: 0x4001020C
B0_P1_U0_PLD_IT4: 0x40010210
B0_P1_U0_PLD_IT5: 0x40010214
B0_P1_U0_PLD_IT6: 0x40010218
B0_P1_U0_PLD_IT7: 0x4001021C

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P1_U0_PLD_IT8: 0x40010220

B0_P1_U0_PLD_IT9: 0x40010224

B0_P1_U0_PLD_IT10: 0x40010228

B0_P1_U0_PLD_IT11: 0x4001022C

B0_P1_U1_PLD_IT0: 0x40010280

B0_P1_U1_PLD_IT1: 0x40010284

B0_P1_U1_PLD_IT2: 0x40010288

B0_P1_U1_PLD_IT3: 0x4001028C

B0_P1_U1_PLD_IT4: 0x40010290

B0_P1_U1_PLD_IT5: 0x40010294

B0_P1_U1_PLD_IT6: 0x40010298

B0_P1_U1_PLD_IT7: 0x4001029C

B0_P1_U1_PLD_IT8: 0x400102A0

B0_P1_U1_PLD_IT9: 0x400102A4

B0_P1_U1_PLD_IT10: 0x400102A8

B0_P1_U1_PLD_IT11: 0x400102AC

B0_P2_U0_PLD_IT0: 0x40010400

B0_P2_U0_PLD_IT1: 0x40010404

B0_P2_U0_PLD_IT2: 0x40010408

B0_P2_U0_PLD_IT3: 0x4001040C

B0_P2_U0_PLD_IT4: 0x40010410

B0_P2_U0_PLD_IT5: 0x40010414

B0_P2_U0_PLD_IT6: 0x40010418

B0_P2_U0_PLD_IT7: 0x4001041C

B0_P2_U0_PLD_IT8: 0x40010420

B0_P2_U0_PLD_IT9: 0x40010424

B0_P2_U0_PLD_IT10: 0x40010428

B0_P2_U0_PLD_IT11: 0x4001042C

B0_P2_U1_PLD_IT0: 0x40010480

B0_P2_U1_PLD_IT1: 0x40010484

B0_P2_U1_PLD_IT2: 0x40010488

B0_P2_U1_PLD_IT3: 0x4001048C

B0_P2_U1_PLD_IT4: 0x40010490

B0_P2_U1_PLD_IT5: 0x40010494

B0_P2_U1_PLD_IT6: 0x40010498

B0_P2_U1_PLD_IT7: 0x4001049C

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P2_U1_PLD_IT8: 0x400104A0

B0_P2_U1_PLD_IT9: 0x400104A4

B0_P2_U1_PLD_IT10: 0x400104A8

B0_P2_U1_PLD_IT11: 0x400104AC

B0_P3_U0_PLD_IT0: 0x40010600

B0_P3_U0_PLD_IT1: 0x40010604

B0_P3_U0_PLD_IT2: 0x40010608

B0_P3_U0_PLD_IT3: 0x4001060C

B0_P3_U0_PLD_IT4: 0x40010610

B0_P3_U0_PLD_IT5: 0x40010614

B0_P3_U0_PLD_IT6: 0x40010618

B0_P3_U0_PLD_IT7: 0x4001061C

B0_P3_U0_PLD_IT8: 0x40010620

B0_P3_U0_PLD_IT9: 0x40010624

B0_P3_U0_PLD_IT10: 0x40010628

B0_P3_U0_PLD_IT11: 0x4001062C

B0_P3_U1_PLD_IT0: 0x40010680

B0_P3_U1_PLD_IT1: 0x40010684

B0_P3_U1_PLD_IT2: 0x40010688

B0_P3_U1_PLD_IT3: 0x4001068C

B0_P3_U1_PLD_IT4: 0x40010690

B0_P3_U1_PLD_IT5: 0x40010694

B0_P3_U1_PLD_IT6: 0x40010698

B0_P3_U1_PLD_IT7: 0x4001069C

B0_P3_U1_PLD_IT8: 0x400106A0

B0_P3_U1_PLD_IT9: 0x400106A4

B0_P3_U1_PLD_IT10: 0x400106A8

B0_P3_U1_PLD_IT11: 0x400106AC

B0_P4_U0_PLD_IT0: 0x40010800

B0_P4_U0_PLD_IT1: 0x40010804

B0_P4_U0_PLD_IT2: 0x40010808

B0_P4_U0_PLD_IT3: 0x4001080C

B0_P4_U0_PLD_IT4: 0x40010810

B0_P4_U0_PLD_IT5: 0x40010814

B0_P4_U0_PLD_IT6: 0x40010818

B0_P4_U0_PLD_IT7: 0x4001081C

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P4_U0_PLD_IT8: 0x40010820

B0_P4_U0_PLD_IT9: 0x40010824

B0_P4_U0_PLD_IT10: 0x40010828

B0_P4_U0_PLD_IT11: 0x4001082C

B0_P4_U1_PLD_IT0: 0x40010880

B0_P4_U1_PLD_IT1: 0x40010884

B0_P4_U1_PLD_IT2: 0x40010888

B0_P4_U1_PLD_IT3: 0x4001088C

B0_P4_U1_PLD_IT4: 0x40010890

B0_P4_U1_PLD_IT5: 0x40010894

B0_P4_U1_PLD_IT6: 0x40010898

B0_P4_U1_PLD_IT7: 0x4001089C

B0_P4_U1_PLD_IT8: 0x400108A0

B0_P4_U1_PLD_IT9: 0x400108A4

B0_P4_U1_PLD_IT10: 0x400108A8

B0_P4_U1_PLD_IT11: 0x400108AC

B0_P5_U0_PLD_IT0: 0x40010A00

B0_P5_U0_PLD_IT1: 0x40010A04

B0_P5_U0_PLD_IT2: 0x40010A08

B0_P5_U0_PLD_IT3: 0x40010A0C

B0_P5_U0_PLD_IT4: 0x40010A10

B0_P5_U0_PLD_IT5: 0x40010A14

B0_P5_U0_PLD_IT6: 0x40010A18

B0_P5_U0_PLD_IT7: 0x40010A1C

B0_P5_U0_PLD_IT8: 0x40010A20

B0_P5_U0_PLD_IT9: 0x40010A24

B0_P5_U0_PLD_IT10: 0x40010A28

B0_P5_U0_PLD_IT11: 0x40010A2C

B0_P5_U1_PLD_IT0: 0x40010A80

B0_P5_U1_PLD_IT1: 0x40010A84

B0_P5_U1_PLD_IT2: 0x40010A88

B0_P5_U1_PLD_IT3: 0x40010A8C

B0_P5_U1_PLD_IT4: 0x40010A90

B0_P5_U1_PLD_IT5: 0x40010A94

B0_P5_U1_PLD_IT6: 0x40010A98

B0_P5_U1_PLD_IT7: 0x40010A9C

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P5_U1_PLD_IT8: 0x40010AA0

B0_P5_U1_PLD_IT9: 0x40010AA4

B0_P5_U1_PLD_IT10: 0x40010AA8

B0_P5_U1_PLD_IT11: 0x40010AAC

B0_P6_U0_PLD_IT0: 0x40010C00

B0_P6_U0_PLD_IT1: 0x40010C04

B0_P6_U0_PLD_IT2: 0x40010C08

B0_P6_U0_PLD_IT3: 0x40010C0C

B0_P6_U0_PLD_IT4: 0x40010C10

B0_P6_U0_PLD_IT5: 0x40010C14

B0_P6_U0_PLD_IT6: 0x40010C18

B0_P6_U0_PLD_IT7: 0x40010C1C

B0_P6_U0_PLD_IT8: 0x40010C20

B0_P6_U0_PLD_IT9: 0x40010C24

B0_P6_U0_PLD_IT10: 0x40010C28

B0_P6_U0_PLD_IT11: 0x40010C2C

B0_P6_U1_PLD_IT0: 0x40010C80

B0_P6_U1_PLD_IT1: 0x40010C84

B0_P6_U1_PLD_IT2: 0x40010C88

B0_P6_U1_PLD_IT3: 0x40010C8C

B0_P6_U1_PLD_IT4: 0x40010C90

B0_P6_U1_PLD_IT5: 0x40010C94

B0_P6_U1_PLD_IT6: 0x40010C98

B0_P6_U1_PLD_IT7: 0x40010C9C

B0_P6_U1_PLD_IT8: 0x40010CA0

B0_P6_U1_PLD_IT9: 0x40010CA4

B0_P6_U1_PLD_IT10: 0x40010CA8

B0_P6_U1_PLD_IT11: 0x40010CAC

B0_P7_U0_PLD_IT0: 0x40010E00

B0_P7_U0_PLD_IT1: 0x40010E04

B0_P7_U0_PLD_IT2: 0x40010E08

B0_P7_U0_PLD_IT3: 0x40010E0C

B0_P7_U0_PLD_IT4: 0x40010E10

B0_P7_U0_PLD_IT5: 0x40010E14

B0_P7_U0_PLD_IT6: 0x40010E18

B0_P7_U0_PLD_IT7: 0x40010E1C

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B0_P7_U0_PLD_IT8: 0x40010E20

B0_P7_U0_PLD_IT9: 0x40010E24

B0_P7_U0_PLD_IT10: 0x40010E28

B0_P7_U0_PLD_IT11: 0x40010E2C

B0_P7_U1_PLD_IT0: 0x40010E80

B0_P7_U1_PLD_IT1: 0x40010E84

B0_P7_U1_PLD_IT2: 0x40010E88

B0_P7_U1_PLD_IT3: 0x40010E8C

B0_P7_U1_PLD_IT4: 0x40010E90

B0_P7_U1_PLD_IT5: 0x40010E94

B0_P7_U1_PLD_IT6: 0x40010E98

B0_P7_U1_PLD_IT7: 0x40010E9C

B0_P7_U1_PLD_IT8: 0x40010EA0

B0_P7_U1_PLD_IT9: 0x40010EA4

B0_P7_U1_PLD_IT10: 0x40010EA8

B0_P7_U1_PLD_IT11: 0x40010EAC

B1_P2_U0_PLD_IT0: 0x40011400

B1_P2_U0_PLD_IT1: 0x40011404

B1_P2_U0_PLD_IT2: 0x40011408

B1_P2_U0_PLD_IT3: 0x4001140C

B1_P2_U0_PLD_IT4: 0x40011410

B1_P2_U0_PLD_IT5: 0x40011414

B1_P2_U0_PLD_IT6: 0x40011418

B1_P2_U0_PLD_IT7: 0x4001141C

B1_P2_U0_PLD_IT8: 0x40011420

B1_P2_U0_PLD_IT9: 0x40011424

B1_P2_U0_PLD_IT10: 0x40011428

B1_P2_U0_PLD_IT11: 0x4001142C

B1_P2_U1_PLD_IT0: 0x40011480

B1_P2_U1_PLD_IT1: 0x40011484

B1_P2_U1_PLD_IT2: 0x40011488

B1_P2_U1_PLD_IT3: 0x4001148C

B1_P2_U1_PLD_IT4: 0x40011490

B1_P2_U1_PLD_IT5: 0x40011494

B1_P2_U1_PLD_IT6: 0x40011498

B1_P2_U1_PLD_IT7: 0x4001149C

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B1_P2_U1_PLD_IT8: 0x400114A0

B1_P2_U1_PLD_IT9: 0x400114A4

B1_P2_U1_PLD_IT10: 0x400114A8

B1_P2_U1_PLD_IT11: 0x400114AC

B1_P3_U0_PLD_IT0: 0x40011600

B1_P3_U0_PLD_IT1: 0x40011604

B1_P3_U0_PLD_IT2: 0x40011608

B1_P3_U0_PLD_IT3: 0x4001160C

B1_P3_U0_PLD_IT4: 0x40011610

B1_P3_U0_PLD_IT5: 0x40011614

B1_P3_U0_PLD_IT6: 0x40011618

B1_P3_U0_PLD_IT7: 0x4001161C

B1_P3_U0_PLD_IT8: 0x40011620

B1_P3_U0_PLD_IT9: 0x40011624

B1_P3_U0_PLD_IT10: 0x40011628

B1_P3_U0_PLD_IT11: 0x4001162C

B1_P3_U1_PLD_IT0: 0x40011680

B1_P3_U1_PLD_IT1: 0x40011684

B1_P3_U1_PLD_IT2: 0x40011688

B1_P3_U1_PLD_IT3: 0x4001168C

B1_P3_U1_PLD_IT4: 0x40011690

B1_P3_U1_PLD_IT5: 0x40011694

B1_P3_U1_PLD_IT6: 0x40011698

B1_P3_U1_PLD_IT7: 0x4001169C

B1_P3_U1_PLD_IT8: 0x400116A0

B1_P3_U1_PLD_IT9: 0x400116A4

B1_P3_U1_PLD_IT10: 0x400116A8

B1_P3_U1_PLD_IT11: 0x400116AC

B1_P4_U0_PLD_IT0: 0x40011800

B1_P4_U0_PLD_IT1: 0x40011804

B1_P4_U0_PLD_IT2: 0x40011808

B1_P4_U0_PLD_IT3: 0x4001180C

B1_P4_U0_PLD_IT4: 0x40011810

B1_P4_U0_PLD_IT5: 0x40011814

B1_P4_U0_PLD_IT6: 0x40011818

B1_P4_U0_PLD_IT7: 0x4001181C

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B1_P4_U0_PLD_IT8: 0x40011820

B1_P4_U0_PLD_IT9: 0x40011824

B1_P4_U0_PLD_IT10: 0x40011828

B1_P4_U0_PLD_IT11: 0x4001182C

B1_P4_U1_PLD_IT0: 0x40011880

B1_P4_U1_PLD_IT1: 0x40011884

B1_P4_U1_PLD_IT2: 0x40011888

B1_P4_U1_PLD_IT3: 0x4001188C

B1_P4_U1_PLD_IT4: 0x40011890

B1_P4_U1_PLD_IT5: 0x40011894

B1_P4_U1_PLD_IT6: 0x40011898

B1_P4_U1_PLD_IT7: 0x4001189C

B1_P4_U1_PLD_IT8: 0x400118A0

B1_P4_U1_PLD_IT9: 0x400118A4

B1_P4_U1_PLD_IT10: 0x400118A8

B1_P4_U1_PLD_IT11: 0x400118AC

B1_P5_U0_PLD_IT0: 0x40011A00

B1_P5_U0_PLD_IT1: 0x40011A04

B1_P5_U0_PLD_IT2: 0x40011A08

B1_P5_U0_PLD_IT3: 0x40011A0C

B1_P5_U0_PLD_IT4: 0x40011A10

B1_P5_U0_PLD_IT5: 0x40011A14

B1_P5_U0_PLD_IT6: 0x40011A18

B1_P5_U0_PLD_IT7: 0x40011A1C

B1_P5_U0_PLD_IT8: 0x40011A20

B1_P5_U0_PLD_IT9: 0x40011A24

B1_P5_U0_PLD_IT10: 0x40011A28

B1_P5_U0_PLD_IT11: 0x40011A2C

B1_P5_U1_PLD_IT0: 0x40011A80

B1_P5_U1_PLD_IT1: 0x40011A84

B1_P5_U1_PLD_IT2: 0x40011A88

B1_P5_U1_PLD_IT3: 0x40011A8C

B1_P5_U1_PLD_IT4: 0x40011A90

B1_P5_U1_PLD_IT5: 0x40011A94

B1_P5_U1_PLD_IT6: 0x40011A98

B1_P5_U1_PLD_IT7: 0x40011A9C

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

Register : Address

B1_P5_U1_PLD_IT8: 0x40011AA0

B1_P5_U1_PLD_IT9: 0x40011AA4

B1_P5_U1_PLD_IT10: 0x40011AA8

B1_P5_U1_PLD_IT11: 0x40011AAC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Complement input term byte

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term.
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term.
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term.
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term.
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term.
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term.
25	PLD1_ITxT_1	True input term. Bit position corresponds to product term.
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term.
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term.

1.3.1128 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11] (continued)

22	PLD0_ITxT_6	True input term. Bit position corresponds to product term.
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term.
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term.
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term.
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term.
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term.
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term.
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term
3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term

1.3.1129 B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3]

PLD_ORT

Reset: N/A

Register : Address

B0_P0_U0_PLD_ORT0: 0x40010030
B0_P0_U0_PLD_ORT1: 0x40010032
B0_P0_U0_PLD_ORT2: 0x40010034
B0_P0_U0_PLD_ORT3: 0x40010036
B0_P0_U1_PLD_ORT0: 0x400100B0
B0_P0_U1_PLD_ORT1: 0x400100B2
B0_P0_U1_PLD_ORT2: 0x400100B4
B0_P0_U1_PLD_ORT3: 0x400100B6
B0_P1_U0_PLD_ORT0: 0x40010230
B0_P1_U0_PLD_ORT1: 0x40010232
B0_P1_U0_PLD_ORT2: 0x40010234
B0_P1_U0_PLD_ORT3: 0x40010236
B0_P1_U1_PLD_ORT0: 0x400102B0
B0_P1_U1_PLD_ORT1: 0x400102B2
B0_P1_U1_PLD_ORT2: 0x400102B4
B0_P1_U1_PLD_ORT3: 0x400102B6
B0_P2_U0_PLD_ORT0: 0x40010430
B0_P2_U0_PLD_ORT1: 0x40010432
B0_P2_U0_PLD_ORT2: 0x40010434
B0_P2_U0_PLD_ORT3: 0x40010436
B0_P2_U1_PLD_ORT0: 0x400104B0
B0_P2_U1_PLD_ORT1: 0x400104B2
B0_P2_U1_PLD_ORT2: 0x400104B4
B0_P2_U1_PLD_ORT3: 0x400104B6
B0_P3_U0_PLD_ORT0: 0x40010630
B0_P3_U0_PLD_ORT1: 0x40010632
B0_P3_U0_PLD_ORT2: 0x40010634
B0_P3_U0_PLD_ORT3: 0x40010636
B0_P3_U1_PLD_ORT0: 0x400106B0
B0_P3_U1_PLD_ORT1: 0x400106B2
B0_P3_U1_PLD_ORT2: 0x400106B4
B0_P3_U1_PLD_ORT3: 0x400106B6

1.3.1129 B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3] (continued)

Register : Address

B0_P4_U0_PLD_ORT0: 0x40010830

B0_P4_U0_PLD_ORT1: 0x40010832

B0_P4_U0_PLD_ORT2: 0x40010834

B0_P4_U0_PLD_ORT3: 0x40010836

B0_P4_U1_PLD_ORT0: 0x400108B0

B0_P4_U1_PLD_ORT1: 0x400108B2

B0_P4_U1_PLD_ORT2: 0x400108B4

B0_P4_U1_PLD_ORT3: 0x400108B6

B0_P5_U0_PLD_ORT0: 0x40010A30

B0_P5_U0_PLD_ORT1: 0x40010A32

B0_P5_U0_PLD_ORT2: 0x40010A34

B0_P5_U0_PLD_ORT3: 0x40010A36

B0_P5_U1_PLD_ORT0: 0x40010AB0

B0_P5_U1_PLD_ORT1: 0x40010AB2

B0_P5_U1_PLD_ORT2: 0x40010AB4

B0_P5_U1_PLD_ORT3: 0x40010AB6

B0_P6_U0_PLD_ORT0: 0x40010C30

B0_P6_U0_PLD_ORT1: 0x40010C32

B0_P6_U0_PLD_ORT2: 0x40010C34

B0_P6_U0_PLD_ORT3: 0x40010C36

B0_P6_U1_PLD_ORT0: 0x40010CB0

B0_P6_U1_PLD_ORT1: 0x40010CB2

B0_P6_U1_PLD_ORT2: 0x40010CB4

B0_P6_U1_PLD_ORT3: 0x40010CB6

B0_P7_U0_PLD_ORT0: 0x40010E30

B0_P7_U0_PLD_ORT1: 0x40010E32

B0_P7_U0_PLD_ORT2: 0x40010E34

B0_P7_U0_PLD_ORT3: 0x40010E36

B0_P7_U1_PLD_ORT0: 0x40010EB0

B0_P7_U1_PLD_ORT1: 0x40010EB2

B0_P7_U1_PLD_ORT2: 0x40010EB4

B0_P7_U1_PLD_ORT3: 0x40010EB6

B1_P2_U0_PLD_ORT0: 0x40011430

B1_P2_U0_PLD_ORT1: 0x40011432

B1_P2_U0_PLD_ORT2: 0x40011434

B1_P2_U0_PLD_ORT3: 0x40011436

1.3.1129 B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3] (continued)

Register : Address

B1_P2_U1_PLD_ORT0: 0x400114B0

B1_P2_U1_PLD_ORT1: 0x400114B2

B1_P2_U1_PLD_ORT2: 0x400114B4

B1_P2_U1_PLD_ORT3: 0x400114B6

B1_P3_U0_PLD_ORT0: 0x40011630

B1_P3_U0_PLD_ORT1: 0x40011632

B1_P3_U0_PLD_ORT2: 0x40011634

B1_P3_U0_PLD_ORT3: 0x40011636

B1_P3_U1_PLD_ORT0: 0x400116B0

B1_P3_U1_PLD_ORT1: 0x400116B2

B1_P3_U1_PLD_ORT2: 0x400116B4

B1_P3_U1_PLD_ORT3: 0x400116B6

B1_P4_U0_PLD_ORT0: 0x40011830

B1_P4_U0_PLD_ORT1: 0x40011832

B1_P4_U0_PLD_ORT2: 0x40011834

B1_P4_U0_PLD_ORT3: 0x40011836

B1_P4_U1_PLD_ORT0: 0x400118B0

B1_P4_U1_PLD_ORT1: 0x400118B2

B1_P4_U1_PLD_ORT2: 0x400118B4

B1_P4_U1_PLD_ORT3: 0x400118B6

B1_P5_U0_PLD_ORT0: 0x40011A30

B1_P5_U0_PLD_ORT1: 0x40011A32

B1_P5_U0_PLD_ORT2: 0x40011A34

B1_P5_U0_PLD_ORT3: 0x40011A36

B1_P5_U1_PLD_ORT0: 0x40011AB0

B1_P5_U1_PLD_ORT1: 0x40011AB2

B1_P5_U1_PLD_ORT2: 0x40011AB4

B1_P5_U1_PLD_ORT3: 0x40011AB6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT _PTx_7	PLD0_ORT _PTx_6	PLD0_ORT _PTx_5	PLD0_ORT _PTx_4	PLD0_ORT _PTx_3	PLD0_ORT _PTx_2	PLD0_ORT _PTx_1	PLD0_ORT _PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U

1.3.1129 B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3] (continued)

HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT _PTx_7	PLD1_ORT _PTx_6	PLD1_ORT _PTx_5	PLD1_ORT _PTx_4	PLD1_ORT _PTx_3	PLD1_ORT _PTx_2	PLD1_ORT _PTx_1	PLD1_ORT _PTx_0

OR term byte

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term.
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term.
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term.
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term.
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term.
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term.
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term.
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term.
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term.
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term.
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term.
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term.
3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term.
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term.
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term.
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term.

1.3.1130 B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST

MC_CFG_CEN_CONST

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_CEN_CONST: 0x40010038
B0_P0_U1_MC_CFG_CEN_CONST: 0x400100B8
B0_P1_U0_MC_CFG_CEN_CONST: 0x40010238
B0_P1_U1_MC_CFG_CEN_CONST: 0x400102B8
B0_P2_U0_MC_CFG_CEN_CONST: 0x40010438
B0_P2_U1_MC_CFG_CEN_CONST: 0x400104B8
B0_P3_U0_MC_CFG_CEN_CONST: 0x40010638
B0_P3_U1_MC_CFG_CEN_CONST: 0x400106B8
B0_P4_U0_MC_CFG_CEN_CONST: 0x40010838
B0_P4_U1_MC_CFG_CEN_CONST: 0x400108B8
B0_P5_U0_MC_CFG_CEN_CONST: 0x40010A38
B0_P5_U1_MC_CFG_CEN_CONST: 0x40010AB8
B0_P6_U0_MC_CFG_CEN_CONST: 0x40010C38
B0_P6_U1_MC_CFG_CEN_CONST: 0x40010CB8
B0_P7_U0_MC_CFG_CEN_CONST: 0x40010E38
B0_P7_U1_MC_CFG_CEN_CONST: 0x40010EB8
B1_P2_U0_MC_CFG_CEN_CONST: 0x40011438
B1_P2_U1_MC_CFG_CEN_CONST: 0x400114B8
B1_P3_U0_MC_CFG_CEN_CONST: 0x40011638
B1_P3_U1_MC_CFG_CEN_CONST: 0x400116B8
B1_P4_U0_MC_CFG_CEN_CONST: 0x40011838
B1_P4_U1_MC_CFG_CEN_CONST: 0x400118B8
B1_P5_U0_MC_CFG_CEN_CONST: 0x40011A38
B1_P5_U1_MC_CFG_CEN_CONST: 0x40011AB8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R

1.3.1130 B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST (continued)

Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Macrocell configuration for Carry Enable and Constant

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant See Table 1-726.
14	PLD1_MC3_CEN	Carry enable See Table 1-725.
13	PLD1_MC2_DFF_C	DFF Constant See Table 1-726.
12	PLD1_MC2_CEN	Carry enable See Table 1-725.
11	PLD1_MC1_DFF_C	DFF Constant See Table 1-726.
10	PLD1_MC1_CEN	Carry enable See Table 1-725.
9	PLD1_MC0_DFF_C	DFF Constant See Table 1-726.
8	PLD1_MC0_CEN	Carry enable See Table 1-725.
7	PLD0_MC3_DFF_C	DFF Constant See Table 1-726.
6	PLD0_MC3_CEN	Carry enable See Table 1-725.
5	PLD0_MC2_DFF_C	DFF Constant See Table 1-726.
4	PLD0_MC2_CEN	Carry enable See Table 1-725.
3	PLD0_MC1_DFF_C	DFF Constant See Table 1-726.
2	PLD0_MC1_CEN	Carry enable See Table 1-725.
1	PLD0_MC0_DFF_C	DFF Constant See Table 1-726.

1.3.1130 B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST (continued)

0	PLD0_MC0_CEN	Carry enable See Table 1-725.

Table 1-725. Bit field encoding: CEN_ENUM

Value	Name	Description
1'b0	DISABLE	Disabled
1'b1	ENABLE	Enabled

Table 1-726. Bit field encoding: DFF_ENUM

Value	Name	Description
1'b0	TRUE	DFF non-inverted
1'b1	INVERTED	DFF inverted

1.3.1131 B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB

MC_CFG_XORFB

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_XORFB: 0x4001003A

B0_P0_U1_MC_CFG_XORFB: 0x400100BA

B0_P1_U0_MC_CFG_XORFB: 0x4001023A

B0_P1_U1_MC_CFG_XORFB: 0x400102BA

B0_P2_U0_MC_CFG_XORFB: 0x4001043A

B0_P2_U1_MC_CFG_XORFB: 0x400104BA

B0_P3_U0_MC_CFG_XORFB: 0x4001063A

B0_P3_U1_MC_CFG_XORFB: 0x400106BA

B0_P4_U0_MC_CFG_XORFB: 0x4001083A

B0_P4_U1_MC_CFG_XORFB: 0x400108BA

B0_P5_U0_MC_CFG_XORFB: 0x40010A3A

B0_P5_U1_MC_CFG_XORFB: 0x40010ABA

B0_P6_U0_MC_CFG_XORFB: 0x40010C3A

B0_P6_U1_MC_CFG_XORFB: 0x40010CBA

B0_P7_U0_MC_CFG_XORFB: 0x40010E3A

B0_P7_U1_MC_CFG_XORFB: 0x40010EBA

B1_P2_U0_MC_CFG_XORFB: 0x4001143A

B1_P2_U1_MC_CFG_XORFB: 0x400114BA

B1_P3_U0_MC_CFG_XORFB: 0x4001163A

B1_P3_U1_MC_CFG_XORFB: 0x400116BA

B1_P4_U0_MC_CFG_XORFB: 0x4001183A

B1_P4_U1_MC_CFG_XORFB: 0x400118BA

B1_P5_U0_MC_CFG_XORFB: 0x40011A3A

B1_P5_U1_MC_CFG_XORFB: 0x40011ABA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UU		R/W:UU		R/W:UU		R/W:UU	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB		PLD0_MC2_XORFB		PLD0_MC1_XORFB		PLD0_MC0_XORFB	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UU		R/W:UU		R/W:UU		R/W:UU	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB		PLD1_MC2_XORFB		PLD1_MC1_XORFB		PLD1_MC0_XORFB	

1.3.1131 B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB (continued)

Macrocell configuration for XOR feedback

Bits	Name	Description
15:14	PLD1_MC3_XORFB[1:0]	XOR feedback See Table 1-727.
13:12	PLD1_MC2_XORFB[1:0]	XOR feedback See Table 1-727.
11:10	PLD1_MC1_XORFB[1:0]	XOR feedback See Table 1-727.
9:8	PLD1_MC0_XORFB[1:0]	XOR feedback See Table 1-727.
7:6	PLD0_MC3_XORFB[1:0]	XOR feedback See Table 1-727.
5:4	PLD0_MC2_XORFB[1:0]	XOR feedback See Table 1-727.
3:2	PLD0_MC1_XORFB[1:0]	XOR feedback See Table 1-727.
1:0	PLD0_MC0_XORFB[1:0]	XOR feedback See Table 1-727.

Table 1-727. Bit field encoding: XORFB_ENUM

Value	Name	Description
2'b00	DFF	DFF
2'b01	CARRY	Carry
2'b10	TFF_H	TFF on high
2'b11	TFF_L	TFF on low

1.3.1132 B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET

MC_CFG_SET_RESET

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_SET_RESET: 0x4001003C

B0_P0_U1_MC_CFG_SET_RESET: 0x400100BC

B0_P1_U0_MC_CFG_SET_RESET: 0x4001023C

B0_P1_U1_MC_CFG_SET_RESET: 0x400102BC

B0_P2_U0_MC_CFG_SET_RESET: 0x4001043C

B0_P2_U1_MC_CFG_SET_RESET: 0x400104BC

B0_P3_U0_MC_CFG_SET_RESET: 0x4001063C

B0_P3_U1_MC_CFG_SET_RESET: 0x400106BC

B0_P4_U0_MC_CFG_SET_RESET: 0x4001083C

B0_P4_U1_MC_CFG_SET_RESET: 0x400108BC

B0_P5_U0_MC_CFG_SET_RESET: 0x40010A3C

B0_P5_U1_MC_CFG_SET_RESET: 0x40010ABC

B0_P6_U0_MC_CFG_SET_RESET: 0x40010C3C

B0_P6_U1_MC_CFG_SET_RESET: 0x40010CBC

B0_P7_U0_MC_CFG_SET_RESET: 0x40010E3C

B0_P7_U1_MC_CFG_SET_RESET: 0x40010EBC

B1_P2_U0_MC_CFG_SET_RESET: 0x4001143C

B1_P2_U1_MC_CFG_SET_RESET: 0x400114BC

B1_P3_U0_MC_CFG_SET_RESET: 0x4001163C

B1_P3_U1_MC_CFG_SET_RESET: 0x400116BC

B1_P4_U0_MC_CFG_SET_RESET: 0x4001183C

B1_P4_U1_MC_CFG_SET_RESET: 0x400118BC

B1_P5_U0_MC_CFG_SET_RESET: 0x40011A3C

B1_P5_U1_MC_CFG_SET_RESET: 0x40011ABC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U

1.3.1132 B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET (continued)

HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Macrocell configuration for set and reset

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable See Table 1-728.
14	PLD1_MC3_SET_SEL	Set select enable See Table 1-729.
13	PLD1_MC2_RESET_SEL	Reset select enable See Table 1-728.
12	PLD1_MC2_SET_SEL	Set select enable See Table 1-729.
11	PLD1_MC1_RESET_SEL	Reset select enable See Table 1-728.
10	PLD1_MC1_SET_SEL	Set select enable See Table 1-729.
9	PLD1_MC0_RESET_SEL	Reset select enable See Table 1-728.
8	PLD1_MC0_SET_SEL	Set select enable See Table 1-729.
7	PLD0_MC3_RESET_SEL	Reset select enable See Table 1-728.
6	PLD0_MC3_SET_SEL	Set select enable See Table 1-729.
5	PLD0_MC2_RESET_SEL	Reset select enable See Table 1-728.
4	PLD0_MC2_SET_SEL	Set select enable See Table 1-729.
3	PLD0_MC1_RESET_SEL	Reset select enable See Table 1-728.
2	PLD0_MC1_SET_SEL	Set select enable See Table 1-729.
1	PLD0_MC0_RESET_SEL	Reset select enable See Table 1-728.

1.3.1132 B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET (continued)

0	PLD0_MC0_SET_SEL	Set select enable See Table 1-729.

Table 1-728. Bit field encoding: RESET_SEL_ENUM

Value	Name	Description
1'b0	DISABLE	Reset not used
1'b1	ENABLE	Reset enabled

Table 1-729. Bit field encoding: SET_SEL_ENUM

Value	Name	Description
1'b0	DISABLE	Set not used
1'b1	ENABLE	Set reset enabled

1.3.1133 B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS

MC_CFG_BYPASS

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_BYPASS: 0x4001003E
B0_P0_U1_MC_CFG_BYPASS: 0x400100BE
B0_P1_U0_MC_CFG_BYPASS: 0x4001023E
B0_P1_U1_MC_CFG_BYPASS: 0x400102BE
B0_P2_U0_MC_CFG_BYPASS: 0x4001043E
B0_P2_U1_MC_CFG_BYPASS: 0x400104BE
B0_P3_U0_MC_CFG_BYPASS: 0x4001063E
B0_P3_U1_MC_CFG_BYPASS: 0x400106BE
B0_P4_U0_MC_CFG_BYPASS: 0x4001083E
B0_P4_U1_MC_CFG_BYPASS: 0x400108BE
B0_P5_U0_MC_CFG_BYPASS: 0x40010A3E
B0_P5_U1_MC_CFG_BYPASS: 0x40010ABE
B0_P6_U0_MC_CFG_BYPASS: 0x40010C3E
B0_P6_U1_MC_CFG_BYPASS: 0x40010CBE
B0_P7_U0_MC_CFG_BYPASS: 0x40010E3E
B0_P7_U1_MC_CFG_BYPASS: 0x40010EBE
B1_P2_U0_MC_CFG_BYPASS: 0x4001143E
B1_P2_U1_MC_CFG_BYPASS: 0x400114BE
B1_P3_U0_MC_CFG_BYPASS: 0x4001163E
B1_P3_U1_MC_CFG_BYPASS: 0x400116BE
B1_P4_U0_MC_CFG_BYPASS: 0x4001183E
B1_P4_U1_MC_CFG_BYPASS: 0x400118BE
B1_P5_U0_MC_CFG_BYPASS: 0x40011A3E
B1_P5_U1_MC_CFG_BYPASS: 0x40011ABE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:U	NA:0	R/W:U	NA:0	R/W:U	NA:0	R/W:U
HW Access	NA	R	NA	R	NA	R	NA	R
Name		PLD0_MC3_BYPASS		PLD0_MC2_BYPASS		PLD0_MC1_BYPASS		PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:U	NA:0	R/W:U	NA:0	R/W:U	NA:0	R/W:U
HW Access	NA	R	NA	R	NA	R	NA	R

1.3.1133 B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS (continued)

Name		PLD1_MC3 _BYPASS		PLD1_MC2 _BYPASS		PLD1_MC1 _BYPASS		PLD1_MC0 _BYPASS

Macrocell configuration for bypass

Bits	Name	Description
14	PLD1_MC3_BYPASS	Bypass selection See Table 1-730.
12	PLD1_MC2_BYPASS	Bypass selection See Table 1-730.
10	PLD1_MC1_BYPASS	Bypass selection See Table 1-730.
8	PLD1_MC0_BYPASS	Bypass selection See Table 1-730.
6	PLD0_MC3_BYPASS	Bypass selection See Table 1-730.
4	PLD0_MC2_BYPASS	Bypass selection See Table 1-730.
2	PLD0_MC1_BYPASS	Bypass selection See Table 1-730.
0	PLD0_MC0_BYPASS	Bypass selection See Table 1-730.

Table 1-730. Bit field encoding: BYPASS_ENUM

Value	Name	Description
1'b0	REGISTER	Registered output
1'b1	COMBINATIONAL	Combinational output

1.3.1134 B[0..3]_P[0..7]_U[0..1]_CFG0

CFG0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG0: 0x40010040	B0_P0_U1_CFG0: 0x400100C0
B0_P1_U0_CFG0: 0x40010240	B0_P1_U1_CFG0: 0x400102C0
B0_P2_U0_CFG0: 0x40010440	B0_P2_U1_CFG0: 0x400104C0
B0_P3_U0_CFG0: 0x40010640	B0_P3_U1_CFG0: 0x400106C0
B0_P4_U0_CFG0: 0x40010840	B0_P4_U1_CFG0: 0x400108C0
B0_P5_U0_CFG0: 0x40010A40	B0_P5_U1_CFG0: 0x40010AC0
B0_P6_U0_CFG0: 0x40010C40	B0_P6_U1_CFG0: 0x40010CC0
B0_P7_U0_CFG0: 0x40010E40	B0_P7_U1_CFG0: 0x40010EC0
B1_P2_U0_CFG0: 0x40011440	B1_P2_U1_CFG0: 0x400114C0
B1_P3_U0_CFG0: 0x40011640	B1_P3_U1_CFG0: 0x400116C0
B1_P4_U0_CFG0: 0x40011840	B1_P4_U1_CFG0: 0x400118C0
B1_P5_U0_CFG0: 0x40011A40	B1_P5_U1_CFG0: 0x40011AC0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Name		RAD1				RAD0		

Datapath Input Selection - RAD1 RAD0

Bits	Name	Description
6:4	RAD1[2:0]	Datapath Permutable Input Mux See Table 1-731.
2:0	RAD0[2:0]	Datapath Permutable Input Mux See Table 1-731.

Table 1-731. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1135 B[0..3]_P[0..7]_U[0..1]_CFG1

CFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG1: 0x40010041	B0_P0_U1_CFG1: 0x400100C1
B0_P1_U0_CFG1: 0x40010241	B0_P1_U1_CFG1: 0x400102C1
B0_P2_U0_CFG1: 0x40010441	B0_P2_U1_CFG1: 0x400104C1
B0_P3_U0_CFG1: 0x40010641	B0_P3_U1_CFG1: 0x400106C1
B0_P4_U0_CFG1: 0x40010841	B0_P4_U1_CFG1: 0x400108C1
B0_P5_U0_CFG1: 0x40010A41	B0_P5_U1_CFG1: 0x40010AC1
B0_P6_U0_CFG1: 0x40010C41	B0_P6_U1_CFG1: 0x40010CC1
B0_P7_U0_CFG1: 0x40010E41	B0_P7_U1_CFG1: 0x40010EC1
B1_P2_U0_CFG1: 0x40011441	B1_P2_U1_CFG1: 0x400114C1
B1_P3_U0_CFG1: 0x40011641	B1_P3_U1_CFG1: 0x400116C1
B1_P4_U0_CFG1: 0x40011841	B1_P4_U1_CFG1: 0x400118C1
B1_P5_U0_CFG1: 0x40011A41	B1_P5_U1_CFG1: 0x40011AC1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						RAD2		

Datapath Input Selection - RAD2

Bits	Name	Description
2:0	RAD2[2:0]	Datapath Permutable Input Mux See Table 1-732.

Table 1-732. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1136 B[0..3]_P[0..7]_U[0..1]_CFG2

CFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG2: 0x40010042	B0_P0_U1_CFG2: 0x400100C2
B0_P1_U0_CFG2: 0x40010242	B0_P1_U1_CFG2: 0x400102C2
B0_P2_U0_CFG2: 0x40010442	B0_P2_U1_CFG2: 0x400104C2
B0_P3_U0_CFG2: 0x40010642	B0_P3_U1_CFG2: 0x400106C2
B0_P4_U0_CFG2: 0x40010842	B0_P4_U1_CFG2: 0x400108C2
B0_P5_U0_CFG2: 0x40010A42	B0_P5_U1_CFG2: 0x40010AC2
B0_P6_U0_CFG2: 0x40010C42	B0_P6_U1_CFG2: 0x40010CC2
B0_P7_U0_CFG2: 0x40010E42	B0_P7_U1_CFG2: 0x40010EC2
B1_P2_U0_CFG2: 0x40011442	B1_P2_U1_CFG2: 0x400114C2
B1_P3_U0_CFG2: 0x40011642	B1_P3_U1_CFG2: 0x400116C2
B1_P4_U0_CFG2: 0x40011842	B1_P4_U1_CFG2: 0x400118C2
B1_P5_U0_CFG2: 0x40011A42	B1_P5_U1_CFG2: 0x40011AC2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Name		F1_LD				F0_LD		

Datapath Input Selection - F1_LD F0_LD

Bits	Name	Description
6:4	F1_LD[2:0]	Datapath Permutable Input Mux See Table 1-733.
2:0	F0_LD[2:0]	Datapath Permutable Input Mux See Table 1-733.

Table 1-733. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1137 B[0..3]_P[0..7]_U[0..1]_CFG3

CFG3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG3: 0x40010043	B0_P0_U1_CFG3: 0x400100C3
B0_P1_U0_CFG3: 0x40010243	B0_P1_U1_CFG3: 0x400102C3
B0_P2_U0_CFG3: 0x40010443	B0_P2_U1_CFG3: 0x400104C3
B0_P3_U0_CFG3: 0x40010643	B0_P3_U1_CFG3: 0x400106C3
B0_P4_U0_CFG3: 0x40010843	B0_P4_U1_CFG3: 0x400108C3
B0_P5_U0_CFG3: 0x40010A43	B0_P5_U1_CFG3: 0x40010AC3
B0_P6_U0_CFG3: 0x40010C43	B0_P6_U1_CFG3: 0x40010CC3
B0_P7_U0_CFG3: 0x40010E43	B0_P7_U1_CFG3: 0x40010EC3
B1_P2_U0_CFG3: 0x40011443	B1_P2_U1_CFG3: 0x400114C3
B1_P3_U0_CFG3: 0x40011643	B1_P3_U1_CFG3: 0x400116C3
B1_P4_U0_CFG3: 0x40011843	B1_P4_U1_CFG3: 0x400118C3
B1_P5_U0_CFG3: 0x40011A43	B1_P5_U1_CFG3: 0x40011AC3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Name		D1_LD				D0_LD		

Datapath Input Selection - D1_LD D0_LD

Bits	Name	Description
6:4	D1_LD[2:0]	Datapath Permutable Input Mux See Table 1-734.
2:0	D0_LD[2:0]	Datapath Permutable Input Mux See Table 1-734.

Table 1-734. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1138 B[0..3]_P[0..7]_U[0..1]_CFG4

CFG4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG4: 0x40010044	B0_P0_U1_CFG4: 0x400100C4
B0_P1_U0_CFG4: 0x40010244	B0_P1_U1_CFG4: 0x400102C4
B0_P2_U0_CFG4: 0x40010444	B0_P2_U1_CFG4: 0x400104C4
B0_P3_U0_CFG4: 0x40010644	B0_P3_U1_CFG4: 0x400106C4
B0_P4_U0_CFG4: 0x40010844	B0_P4_U1_CFG4: 0x400108C4
B0_P5_U0_CFG4: 0x40010A44	B0_P5_U1_CFG4: 0x40010AC4
B0_P6_U0_CFG4: 0x40010C44	B0_P6_U1_CFG4: 0x40010CC4
B0_P7_U0_CFG4: 0x40010E44	B0_P7_U1_CFG4: 0x40010EC4
B1_P2_U0_CFG4: 0x40011444	B1_P2_U1_CFG4: 0x400114C4
B1_P3_U0_CFG4: 0x40011644	B1_P3_U1_CFG4: 0x400116C4
B1_P4_U0_CFG4: 0x40011844	B1_P4_U1_CFG4: 0x400118C4
B1_P5_U0_CFG4: 0x40011A44	B1_P5_U1_CFG4: 0x40011AC4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Name		CI_MUX				SI_MUX		

Datapath Input Selection - CI_MUX SI_MUX

Bits	Name	Description
6:4	CI_MUX[2:0]	Datapath Permutable Input Mux See Table 1-735.
2:0	SI_MUX[2:0]	Datapath Permutable Input Mux See Table 1-735.

Table 1-735. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1139 B[0..3]_P[0..7]_U[0..1]_CFG5

CFG5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG5: 0x40010045	B0_P0_U1_CFG5: 0x400100C5
B0_P1_U0_CFG5: 0x40010245	B0_P1_U1_CFG5: 0x400102C5
B0_P2_U0_CFG5: 0x40010445	B0_P2_U1_CFG5: 0x400104C5
B0_P3_U0_CFG5: 0x40010645	B0_P3_U1_CFG5: 0x400106C5
B0_P4_U0_CFG5: 0x40010845	B0_P4_U1_CFG5: 0x400108C5
B0_P5_U0_CFG5: 0x40010A45	B0_P5_U1_CFG5: 0x40010AC5
B0_P6_U0_CFG5: 0x40010C45	B0_P6_U1_CFG5: 0x40010CC5
B0_P7_U0_CFG5: 0x40010E45	B0_P7_U1_CFG5: 0x40010EC5
B1_P2_U0_CFG5: 0x40011445	B1_P2_U1_CFG5: 0x400114C5
B1_P3_U0_CFG5: 0x40011645	B1_P3_U1_CFG5: 0x400116C5
B1_P4_U0_CFG5: 0x40011845	B1_P4_U1_CFG5: 0x400118C5
B1_P5_U0_CFG5: 0x40011A45	B1_P5_U1_CFG5: 0x40011AC5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Name	OUT1				OUT0			

Datapath Output Selection - OUT1 OUT0

Bits	Name	Description
7:4	OUT1[3:0]	Datapath Permutable Ouput Mux See Table 1-736.
3:0	OUT0[3:0]	Datapath Permutable Ouput Mux See Table 1-736.

Table 1-736. Bit field encoding: DP_OUTPUT_MUX_ENUM

Value	Name	Description
4'b0000	CE0	Comparator 0 equal
4'b0001	CL0	Comparator 0 less than
4'b0010	Z0	Accumulator 0 zero detect
4'b0011	FF0	Accumulator 0 ones detect
4'b0100	CE1	Comparator 1 equal
4'b0101	CL1	Comparator 1 less than
4'b0110	Z1	Accumulator 1 zero detect
4'b0111	FF1	Accumulator 1 ones detect
4'b1000	OV_MSB	Overflow of MSB
4'b1001	CO_MSB	Carry out of MSB
4'b1010	CMSBO	CRC MSB
4'b1011	SO	Shift out

1.3.1139 B[0..3]_P[0..7]_U[0..1]_CFG5 (continued)

Table 1-736. Bit field encoding: DP_OUTPUT_MUX_ENUM

4'b1100	F0_BUS_STAT	FIFO 0 bus status defined by direction and level
4'b1101	F0_BLK_STAT	FIFO 0 block status defined by direction
4'b1110	F1_BUS_STAT	FIFO 1 bus status defined by direction and level
4'b1111	F1_BLK_STAT	FIFO 1 block status defined by direction

1.3.1140 B[0..3]_P[0..7]_U[0..1]_CFG6

CFG6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG6: 0x40010046	B0_P0_U1_CFG6: 0x400100C6
B0_P1_U0_CFG6: 0x40010246	B0_P1_U1_CFG6: 0x400102C6
B0_P2_U0_CFG6: 0x40010446	B0_P2_U1_CFG6: 0x400104C6
B0_P3_U0_CFG6: 0x40010646	B0_P3_U1_CFG6: 0x400106C6
B0_P4_U0_CFG6: 0x40010846	B0_P4_U1_CFG6: 0x400108C6
B0_P5_U0_CFG6: 0x40010A46	B0_P5_U1_CFG6: 0x40010AC6
B0_P6_U0_CFG6: 0x40010C46	B0_P6_U1_CFG6: 0x40010CC6
B0_P7_U0_CFG6: 0x40010E46	B0_P7_U1_CFG6: 0x40010EC6
B1_P2_U0_CFG6: 0x40011446	B1_P2_U1_CFG6: 0x400114C6
B1_P3_U0_CFG6: 0x40011646	B1_P3_U1_CFG6: 0x400116C6
B1_P4_U0_CFG6: 0x40011846	B1_P4_U1_CFG6: 0x400118C6
B1_P5_U0_CFG6: 0x40011A46	B1_P5_U1_CFG6: 0x40011AC6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Name	OUT3				OUT2			

Datapath Output Selection - OUT3 OUT2

Bits	Name	Description
7:4	OUT3[3:0]	Datapath Permutable Ouput Mux See Table 1-737.
3:0	OUT2[3:0]	Datapath Permutable Ouput Mux See Table 1-737.

Table 1-737. Bit field encoding: DP_OUTPUT_MUX_ENUM

Value	Name	Description
4'b0000	CE0	Comparator 0 equal
4'b0001	CL0	Comparator 0 less than
4'b0010	Z0	Accumulator 0 zero detect
4'b0011	FF0	Accumulator 0 ones detect
4'b0100	CE1	Comparator 1 equal
4'b0101	CL1	Comparator 1 less than
4'b0110	Z1	Accumulator 1 zero detect
4'b0111	FF1	Accumulator 1 ones detect
4'b1000	OV_MSB	Overflow of MSB
4'b1001	CO_MSB	Carry out of MSB
4'b1010	CMSBO	CRC MSB
4'b1011	SO	Shift out

1.3.1140 B[0..3]_P[0..7]_U[0..1]_CFG6 (continued)

Table 1-737. Bit field encoding: DP_OUTPUT_MUX_ENUM

4'b1100	F0_BUS_STAT	FIFO 0 bus status defined by direction and level
4'b1101	F0_BLK_STAT	FIFO 0 block status defined by direction
4'b1110	F1_BUS_STAT	FIFO 1 bus status defined by direction and level
4'b1111	F1_BLK_STAT	FIFO 1 block status defined by direction

1.3.1141 B[0..3]_P[0..7]_U[0..1]_CFG7

CFG7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG7: 0x40010047	B0_P0_U1_CFG7: 0x400100C7
B0_P1_U0_CFG7: 0x40010247	B0_P1_U1_CFG7: 0x400102C7
B0_P2_U0_CFG7: 0x40010447	B0_P2_U1_CFG7: 0x400104C7
B0_P3_U0_CFG7: 0x40010647	B0_P3_U1_CFG7: 0x400106C7
B0_P4_U0_CFG7: 0x40010847	B0_P4_U1_CFG7: 0x400108C7
B0_P5_U0_CFG7: 0x40010A47	B0_P5_U1_CFG7: 0x40010AC7
B0_P6_U0_CFG7: 0x40010C47	B0_P6_U1_CFG7: 0x40010CC7
B0_P7_U0_CFG7: 0x40010E47	B0_P7_U1_CFG7: 0x40010EC7
B1_P2_U0_CFG7: 0x40011447	B1_P2_U1_CFG7: 0x400114C7
B1_P3_U0_CFG7: 0x40011647	B1_P3_U1_CFG7: 0x400116C7
B1_P4_U0_CFG7: 0x40011847	B1_P4_U1_CFG7: 0x400118C7
B1_P5_U0_CFG7: 0x40011A47	B1_P5_U1_CFG7: 0x40011AC7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Name	OUT5				OUT4			

Datapath Output Selection - OUT5 OUT4

Bits	Name	Description
7:4	OUT5[3:0]	Datapath Permutable Ouput Mux See Table 1-738.
3:0	OUT4[3:0]	Datapath Permutable Ouput Mux See Table 1-738.

Table 1-738. Bit field encoding: DP_OUTPUT_MUX_ENUM

Value	Name	Description
4'b0000	CE0	Comparator 0 equal
4'b0001	CL0	Comparator 0 less than
4'b0010	Z0	Accumulator 0 zero detect
4'b0011	FF0	Accumulator 0 ones detect
4'b0100	CE1	Comparator 1 equal
4'b0101	CL1	Comparator 1 less than
4'b0110	Z1	Accumulator 1 zero detect
4'b0111	FF1	Accumulator 1 ones detect
4'b1000	OV_MSB	Overflow of MSB
4'b1001	CO_MSB	Carry out of MSB
4'b1010	CMSBO	CRC MSB
4'b1011	SO	Shift out

1.3.1141 B[0..3]_P[0..7]_U[0..1]_CFG7 (continued)

Table 1-738. Bit field encoding: DP_OUTPUT_MUX_ENUM

4'b1100	F0_BUS_STAT	FIFO 0 bus status defined by direction and level
4'b1101	F0_BLK_STAT	FIFO 0 block status defined by direction
4'b1110	F1_BUS_STAT	FIFO 1 bus status defined by direction and level
4'b1111	F1_BLK_STAT	FIFO 1 block status defined by direction

1.3.1142 B[0..3]_P[0..7]_U[0..1]_CFG8

CFG8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG8: 0x40010048	B0_P0_U1_CFG8: 0x400100C8
B0_P1_U0_CFG8: 0x40010248	B0_P1_U1_CFG8: 0x400102C8
B0_P2_U0_CFG8: 0x40010448	B0_P2_U1_CFG8: 0x400104C8
B0_P3_U0_CFG8: 0x40010648	B0_P3_U1_CFG8: 0x400106C8
B0_P4_U0_CFG8: 0x40010848	B0_P4_U1_CFG8: 0x400108C8
B0_P5_U0_CFG8: 0x40010A48	B0_P5_U1_CFG8: 0x40010AC8
B0_P6_U0_CFG8: 0x40010C48	B0_P6_U1_CFG8: 0x40010CC8
B0_P7_U0_CFG8: 0x40010E48	B0_P7_U1_CFG8: 0x40010EC8
B1_P2_U0_CFG8: 0x40011448	B1_P2_U1_CFG8: 0x400114C8
B1_P3_U0_CFG8: 0x40011648	B1_P3_U1_CFG8: 0x400116C8
B1_P4_U0_CFG8: 0x40011848	B1_P4_U1_CFG8: 0x400118C8
B1_P5_U0_CFG8: 0x40011A48	B1_P5_U1_CFG8: 0x40011AC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Name			OUT_SYNC					

Datapath Output Synchronization

Bits	Name	Description
5:0	OUT_SYNC[5:0]	Output Synchronization field

1.3.1143 B[0..3]_P[0..7]_U[0..1]_CFG9

CFG9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG9: 0x40010049	B0_P0_U1_CFG9: 0x400100C9
B0_P1_U0_CFG9: 0x40010249	B0_P1_U1_CFG9: 0x400102C9
B0_P2_U0_CFG9: 0x40010449	B0_P2_U1_CFG9: 0x400104C9
B0_P3_U0_CFG9: 0x40010649	B0_P3_U1_CFG9: 0x400106C9
B0_P4_U0_CFG9: 0x40010849	B0_P4_U1_CFG9: 0x400108C9
B0_P5_U0_CFG9: 0x40010A49	B0_P5_U1_CFG9: 0x40010AC9
B0_P6_U0_CFG9: 0x40010C49	B0_P6_U1_CFG9: 0x40010CC9
B0_P7_U0_CFG9: 0x40010E49	B0_P7_U1_CFG9: 0x40010EC9
B1_P2_U0_CFG9: 0x40011449	B1_P2_U1_CFG9: 0x400114C9
B1_P3_U0_CFG9: 0x40011649	B1_P3_U1_CFG9: 0x400116C9
B1_P4_U0_CFG9: 0x40011849	B1_P4_U1_CFG9: 0x400118C9
B1_P5_U0_CFG9: 0x40011A49	B1_P5_U1_CFG9: 0x40011AC9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	AMASK							

ALU Mask

Bits	Name	Description
7:0	AMASK[7:0]	Datapath Mask

1.3.1144 B[0..3]_P[0..7]_U[0..1]_CFG10

CFG10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG10: 0x4001004A	B0_P0_U1_CFG10: 0x400100CA
B0_P1_U0_CFG10: 0x4001024A	B0_P1_U1_CFG10: 0x400102CA
B0_P2_U0_CFG10: 0x4001044A	B0_P2_U1_CFG10: 0x400104CA
B0_P3_U0_CFG10: 0x4001064A	B0_P3_U1_CFG10: 0x400106CA
B0_P4_U0_CFG10: 0x4001084A	B0_P4_U1_CFG10: 0x400108CA
B0_P5_U0_CFG10: 0x40010A4A	B0_P5_U1_CFG10: 0x40010ACA
B0_P6_U0_CFG10: 0x40010C4A	B0_P6_U1_CFG10: 0x40010CCA
B0_P7_U0_CFG10: 0x40010E4A	B0_P7_U1_CFG10: 0x40010ECA
B1_P2_U0_CFG10: 0x4001144A	B1_P2_U1_CFG10: 0x400114CA
B1_P3_U0_CFG10: 0x4001164A	B1_P3_U1_CFG10: 0x400116CA
B1_P4_U0_CFG10: 0x4001184A	B1_P4_U1_CFG10: 0x400118CA
B1_P5_U0_CFG10: 0x40011A4A	B1_P5_U1_CFG10: 0x40011ACA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CMASK0							

Compare 0 Mask

Bits	Name	Description
7:0	CMASK0[7:0]	Datapath Mask

1.3.1145 B[0..3]_P[0..7]_U[0..1]_CFG11

CFG11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG11: 0x4001004B	B0_P0_U1_CFG11: 0x400100CB
B0_P1_U0_CFG11: 0x4001024B	B0_P1_U1_CFG11: 0x400102CB
B0_P2_U0_CFG11: 0x4001044B	B0_P2_U1_CFG11: 0x400104CB
B0_P3_U0_CFG11: 0x4001064B	B0_P3_U1_CFG11: 0x400106CB
B0_P4_U0_CFG11: 0x4001084B	B0_P4_U1_CFG11: 0x400108CB
B0_P5_U0_CFG11: 0x40010A4B	B0_P5_U1_CFG11: 0x40010ACB
B0_P6_U0_CFG11: 0x40010C4B	B0_P6_U1_CFG11: 0x40010CCB
B0_P7_U0_CFG11: 0x40010E4B	B0_P7_U1_CFG11: 0x40010ECB
B1_P2_U0_CFG11: 0x4001144B	B1_P2_U1_CFG11: 0x400114CB
B1_P3_U0_CFG11: 0x4001164B	B1_P3_U1_CFG11: 0x400116CB
B1_P4_U0_CFG11: 0x4001184B	B1_P4_U1_CFG11: 0x400118CB
B1_P5_U0_CFG11: 0x40011A4B	B1_P5_U1_CFG11: 0x40011ACB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	CMASK1							

Compare 1 Mask

Bits	Name	Description
7:0	CMASK1[7:0]	Datapath Mask

1.3.1146 B[0..3]_P[0..7]_U[0..1]_CFG12

CFG12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG12: 0x4001004C	B0_P0_U1_CFG12: 0x400100CC
B0_P1_U0_CFG12: 0x4001024C	B0_P1_U1_CFG12: 0x400102CC
B0_P2_U0_CFG12: 0x4001044C	B0_P2_U1_CFG12: 0x400104CC
B0_P3_U0_CFG12: 0x4001064C	B0_P3_U1_CFG12: 0x400106CC
B0_P4_U0_CFG12: 0x4001084C	B0_P4_U1_CFG12: 0x400108CC
B0_P5_U0_CFG12: 0x40010A4C	B0_P5_U1_CFG12: 0x40010ACC
B0_P6_U0_CFG12: 0x40010C4C	B0_P6_U1_CFG12: 0x40010CCC
B0_P7_U0_CFG12: 0x40010E4C	B0_P7_U1_CFG12: 0x40010ECC
B1_P2_U0_CFG12: 0x4001144C	B1_P2_U1_CFG12: 0x400114CC
B1_P3_U0_CFG12: 0x4001164C	B1_P3_U1_CFG12: 0x400116CC
B1_P4_U0_CFG12: 0x4001184C	B1_P4_U1_CFG12: 0x400118CC
B1_P5_U0_CFG12: 0x40011A4C	B1_P5_U1_CFG12: 0x40011ACC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB		SI_SELA	

Datapath Static Configuration - masks and shift in

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable See Table 1-740.
6	CMASK0_EN	Datapath mask enable See Table 1-740.
5	AMASK_EN	Datapath mask enable See Table 1-740.
4	DEF_SI	Datapath default shift value See Table 1-739.
3:2	SI_SELB[1:0]	Datapath shift in source select See Table 1-741.
1:0	SI_SELA[1:0]	Datapath shift in source select See Table 1-741.

1.3.1146 B[0..3]_P[0..7]_U[0..1]_CFG12 (continued)

Table 1-739. Bit field encoding: DEF_SHIFT_ENUM

Value	Name	Description
1'b0	DEFAULT_0	Default shift is 0
1'b1	DEFAULT_1	Default shift is 1

Table 1-740. Bit field encoding: MASK_ENABLE_ENUM

Value	Name	Description
1'b0	DISABLE	Masking disabled
1'b1	ENABLE	Masking enabled

Table 1-741. Bit field encoding: SI_SEL_ENUM

Value	Name	Description
2'b00	DEFAULT	Default value specified in default shift field
2'b01	REGISTERED	Shift in is the shift out registered from previous cycle
2'b10	ROUTE	Shift in is selected from datapath routing input
2'b11	CHAIN	Shift in is chained from the previous datapath

1.3.1147 B[0..3]_P[0..7]_U[0..1]_CFG13

CFG13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG13: 0x4001004D	B0_P0_U1_CFG13: 0x400100CD
B0_P1_U0_CFG13: 0x4001024D	B0_P1_U1_CFG13: 0x400102CD
B0_P2_U0_CFG13: 0x4001044D	B0_P2_U1_CFG13: 0x400104CD
B0_P3_U0_CFG13: 0x4001064D	B0_P3_U1_CFG13: 0x400106CD
B0_P4_U0_CFG13: 0x4001084D	B0_P4_U1_CFG13: 0x400108CD
B0_P5_U0_CFG13: 0x40010A4D	B0_P5_U1_CFG13: 0x40010ACD
B0_P6_U0_CFG13: 0x40010C4D	B0_P6_U1_CFG13: 0x40010CCD
B0_P7_U0_CFG13: 0x40010E4D	B0_P7_U1_CFG13: 0x40010ECD
B1_P2_U0_CFG13: 0x4001144D	B1_P2_U1_CFG13: 0x400114CD
B1_P3_U0_CFG13: 0x4001164D	B1_P3_U1_CFG13: 0x400116CD
B1_P4_U0_CFG13: 0x4001184D	B1_P4_U1_CFG13: 0x400118CD
B1_P5_U0_CFG13: 0x40011A4D	B1_P5_U1_CFG13: 0x40011ACD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Name	CMP_SELB		CMP_SELA		CI_SELB		CI_SELA	

Datapath Static Configuration - Carry in and compares

Bits	Name	Description
7:6	CMP_SELB[1:0]	Datapath compare select See Table 1-743.
5:4	CMP_SELA[1:0]	Datapath compare select See Table 1-743.
3:2	CI_SELB[1:0]	Datapath carry in source select See Table 1-742.
1:0	CI_SELA[1:0]	Datapath carry in source select See Table 1-742.

Table 1-742. Bit field encoding: CI_SEL_ENUM

Value	Name	Description
2'b00	DEFAULT	Default arithmetic mode
2'b01	REGISTERED	Carry in is the carry out registered from previous cycle
2'b10	ROUTE	Carry in is selected from datapath routing input
2'b11	CHAIN	Carry in is chained from the previous datapath

1.3.1147 B[0..3]_P[0..7]_U[0..1]_CFG13 (continued)

Table 1-743. Bit field encoding: CMP_SEL_ENUM

Value	Name	Description
2'b00	A1_D1	Compare A1 to D1
2'b01	A1_A0	Compare A1 to A0
2'b10	A0_D1	Compare A0 to D1
2'b11	A0_A0	Compare A0 to A0

1.3.1148 B[0..3]_P[0..7]_U[0..1]_CFG14

CFG14

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG14: 0x4001004E	B0_P0_U1_CFG14: 0x400100CE
B0_P1_U0_CFG14: 0x4001024E	B0_P1_U1_CFG14: 0x400102CE
B0_P2_U0_CFG14: 0x4001044E	B0_P2_U1_CFG14: 0x400104CE
B0_P3_U0_CFG14: 0x4001064E	B0_P3_U1_CFG14: 0x400106CE
B0_P4_U0_CFG14: 0x4001084E	B0_P4_U1_CFG14: 0x400108CE
B0_P5_U0_CFG14: 0x40010A4E	B0_P5_U1_CFG14: 0x40010ACE
B0_P6_U0_CFG14: 0x40010C4E	B0_P6_U1_CFG14: 0x40010CCE
B0_P7_U0_CFG14: 0x40010E4E	B0_P7_U1_CFG14: 0x40010ECE
B1_P2_U0_CFG14: 0x4001144E	B1_P2_U1_CFG14: 0x400114CE
B1_P3_U0_CFG14: 0x4001164E	B1_P3_U1_CFG14: 0x400116CE
B1_P4_U0_CFG14: 0x4001184E	B1_P4_U1_CFG14: 0x400118CE
B1_P5_U0_CFG14: 0x40011A4E	B1_P5_U1_CFG14: 0x40011ACE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Datapath Static Configuration - chaining and MSB

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable See Table 1-747.
6:4	MSB_SEL[2:0]	Datapath MSB Selection See Table 1-748.
3	CHAIN_CMSB	Datapath CRC MSB chaining enable See Table 1-744.
2	CHAIN_FB	Datapath CRC feedback chaining enable See Table 1-746.
1	CHAIN1	Datapath condition chaining enable See Table 1-745.
0	CHAIN0	Datapath condition chaining enable See Table 1-745.

1.3.1148 B[0..3]_P[0..7]_U[0..1]_CFG14 (continued)

Table 1-744. Bit field encoding: CHAIN_CMSB_ENUM

Value	Name	Description
1'b0	DISABLE	CRC MSB is not chained
1'b1	ENABLE	CRC MSB is chained from the next (MSB) datapath

Table 1-745. Bit field encoding: CHAIN_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Conditions are not chained
1'b1	ENABLE	Conditions are chained from the previous (LSB) datapath

Table 1-746. Bit field encoding: CHAIN_FB_ENUM

Value	Name	Description
1'b0	DISABLE	CRC feedback is not chained
1'b1	ENABLE	CRC feedback is chained from the previous (LSB) datapath

Table 1-747. Bit field encoding: MSB_EN_ENUM

Value	Name	Description
1'b0	DISABLE	MSB selection is disabled, MSB is bit 7
1'b1	ENABLE	MSB selection is controlled by MSB_SEL

Table 1-748. Bit field encoding: MSB_SEL_ENUM

Value	Name	Description
3'b000	BIT0	MSB is bit 0
3'b001	BIT1	MSB is bit 1
3'b010	BIT2	MSB is bit 2
3'b011	BIT3	MSB is bit 3
3'b100	BIT4	MSB is bit 4
3'b101	BIT5	MSB is bit 5
3'b110	BIT6	MSB is bit 6
3'b111	BIT7	MSB is bit 7 - equivalent to MSB EN = 0

1.3.1149 B[0..3]_P[0..7]_U[0..1]_CFG15

CFG15

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG15: 0x4001004F	B0_P0_U1_CFG15: 0x400100CF
B0_P1_U0_CFG15: 0x4001024F	B0_P1_U1_CFG15: 0x400102CF
B0_P2_U0_CFG15: 0x4001044F	B0_P2_U1_CFG15: 0x400104CF
B0_P3_U0_CFG15: 0x4001064F	B0_P3_U1_CFG15: 0x400106CF
B0_P4_U0_CFG15: 0x4001084F	B0_P4_U1_CFG15: 0x400108CF
B0_P5_U0_CFG15: 0x40010A4F	B0_P5_U1_CFG15: 0x40010ACF
B0_P6_U0_CFG15: 0x40010C4F	B0_P6_U1_CFG15: 0x40010CCF
B0_P7_U0_CFG15: 0x40010E4F	B0_P7_U1_CFG15: 0x40010ECF
B1_P2_U0_CFG15: 0x4001144F	B1_P2_U1_CFG15: 0x400114CF
B1_P3_U0_CFG15: 0x4001164F	B1_P3_U1_CFG15: 0x400116CF
B1_P4_U0_CFG15: 0x4001184F	B1_P4_U1_CFG15: 0x400118CF
B1_P5_U0_CFG15: 0x40011A4F	B1_P5_U1_CFG15: 0x40011ACF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	NC1	NC0	F1_INSEL		F0_INSEL	

Datapath Static Configuration - FIFOs, shift out, parallel input

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection See Table 1-750.
6	SHIFT_SEL	Datapath shift out selection See Table 1-751.
5	NC1	Spare register bit
4	NC0	Spare register bit
3:2	F1_INSEL[1:0]	Datapath FIFO Configuration See Table 1-749.
1:0	F0_INSEL[1:0]	Datapath FIFO Configuration See Table 1-749.

Table 1-749. Bit field encoding: FIFO_CFG_ENUM

Value	Name	Description
2'b00	INPUT	Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator

1.3.1149 B[0..3]_P[0..7]_U[0..1]_CFG15 (continued)

Table 1-749. Bit field encoding: FIFO_CFG_ENUM

2'b01	OUTPUT_A0	Output Mode: Write source is A0, read destination is the system bus
2'b10	OUTPUT_A1	Output Mode: Write source is A1, read destination is the system bus
2'b11	OUTPUT_ALU	Output Mode: Write source is the ALU output, read destination is the system bus

Table 1-750. Bit field encoding: PI_SEL_ENUM

Value	Name	Description
1'b0	NORMAL	Normal operation, ALU source is from accumulator selection
1'b1	PARALLEL	ALU source A input is from the parallel data input

Table 1-751. Bit field encoding: SHIFT_SEL_ENUM

Value	Name	Description
1'b0	SOL_MSB	Routed shift out is shift out left (sol_msb)
1'b1	SOR	Routed shift out is shift out right (sor)

1.3.1150 B[0..3]_P[0..7]_U[0..1]_CFG16

CFG16

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG16: 0x40010050	B0_P0_U1_CFG16: 0x400100D0
B0_P1_U0_CFG16: 0x40010250	B0_P1_U1_CFG16: 0x400102D0
B0_P2_U0_CFG16: 0x40010450	B0_P2_U1_CFG16: 0x400104D0
B0_P3_U0_CFG16: 0x40010650	B0_P3_U1_CFG16: 0x400106D0
B0_P4_U0_CFG16: 0x40010850	B0_P4_U1_CFG16: 0x400108D0
B0_P5_U0_CFG16: 0x40010A50	B0_P5_U1_CFG16: 0x40010AD0
B0_P6_U0_CFG16: 0x40010C50	B0_P6_U1_CFG16: 0x40010CD0
B0_P7_U0_CFG16: 0x40010E50	B0_P7_U1_CFG16: 0x40010ED0
B1_P2_U0_CFG16: 0x40011450	B1_P2_U1_CFG16: 0x400114D0
B1_P3_U0_CFG16: 0x40011650	B1_P3_U1_CFG16: 0x400116D0
B1_P4_U0_CFG16: 0x40011850	B1_P4_U1_CFG16: 0x400118D0
B1_P5_U0_CFG16: 0x40011A50	B1_P5_U1_CFG16: 0x40011AD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Datapath Static Configuration

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. See Table 1-755.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. See Table 1-755.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. See Table 1-757.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are captured. Captured data may be read immediately from the FIFO. Only applies to FIFOs configured in output mode. See Table 1-754.

1.3.1150 B[0..3]_P[0..7]_U[0..1]_CFG16 (continued)

3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode See Table 1-756.
2	FIFO_ASYNC	Asynchronous FIFO clocking support See Table 1-753.
1	EXT_CRCPRS	External CRC/PRS mode See Table 1-752.
0	WRK16_CONCAT	Datapath register access mode See Table 1-758.

Table 1-752. Bit field encoding: EXT_CRCPRS_ENUM

Value	Name	Description
1'b0	INTERNAL	Internal CRC/PRS routing
1'b1	EXTERNAL	External CRC/PRS routing

Table 1-753. Bit field encoding: FIFO_ASYNC_ENUM

Value	Name	Description
1'b0	DISABLED	FIFO clocks are synchronous
1'b1	ENABLED	FIFO clocks are asynchronous

Table 1-754. Bit field encoding: FIFO_CAP_ENUM

Value	Name	Description
1'b0	DISABLED	FIFO capture is disabled.
1'b1	ENABLED	FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.

Table 1-755. Bit field encoding: FIFO_CK_INV

Value	Name	Description
1'b0	NORMAL	FIFO clock is the same polarity as the Datapath clock.
1'b1	INVERTED	FIFO clock is inverted with respect to the Datapath clock.

Table 1-756. Bit field encoding: FIFO_EDGE_ENUM

Value	Name	Description
1'b0	LEVEL	FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge.
1'b1	EDGE	FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be detected.

Table 1-757. Bit field encoding: FIFO_FAST_ENUM

Value	Name	Description
1'b0	DISABLED	FIFO is clocked with selected Datapath clock.
1'b1	ENABLED	FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.

Table 1-758. Bit field encoding: WRK16_SEL_ENUM

Value	Name	Description
1'b0	DEFAULT	16-bit default access mode: selects registers in two consecutive UDBs in chaining order
1'b1	CONCATENATE	16-bit concat access mode: selects concatenated registers in a single UDB

1.3.1151 B[0..3]_P[0..7]_U[0..1]_CFG20

CFG20

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG20: 0x40010054	B0_P0_U1_CFG20: 0x400100D4
B0_P1_U0_CFG20: 0x40010254	B0_P1_U1_CFG20: 0x400102D4
B0_P2_U0_CFG20: 0x40010454	B0_P2_U1_CFG20: 0x400104D4
B0_P3_U0_CFG20: 0x40010654	B0_P3_U1_CFG20: 0x400106D4
B0_P4_U0_CFG20: 0x40010854	B0_P4_U1_CFG20: 0x400108D4
B0_P5_U0_CFG20: 0x40010A54	B0_P5_U1_CFG20: 0x40010AD4
B0_P6_U0_CFG20: 0x40010C54	B0_P6_U1_CFG20: 0x40010CD4
B0_P7_U0_CFG20: 0x40010E54	B0_P7_U1_CFG20: 0x40010ED4
B1_P2_U0_CFG20: 0x40011454	B1_P2_U1_CFG20: 0x400114D4
B1_P3_U0_CFG20: 0x40011654	B1_P3_U1_CFG20: 0x400116D4
B1_P4_U0_CFG20: 0x40011854	B1_P4_U1_CFG20: 0x400118D4
B1_P5_U0_CFG20: 0x40011A54	B1_P5_U1_CFG20: 0x40011AD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	STAT_MD							

Status input mode selection

Bits	Name	Description
7:0	STAT_MD[7:0]	Mode selection for each bit of the status register

1.3.1152 B[0..3]_P[0..7]_U[0..1]_CFG21

CFG21

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG21: 0x40010055	B0_P0_U1_CFG21: 0x400100D5
B0_P1_U0_CFG21: 0x40010255	B0_P1_U1_CFG21: 0x400102D5
B0_P2_U0_CFG21: 0x40010455	B0_P2_U1_CFG21: 0x400104D5
B0_P3_U0_CFG21: 0x40010655	B0_P3_U1_CFG21: 0x400106D5
B0_P4_U0_CFG21: 0x40010855	B0_P4_U1_CFG21: 0x400108D5
B0_P5_U0_CFG21: 0x40010A55	B0_P5_U1_CFG21: 0x40010AD5
B0_P6_U0_CFG21: 0x40010C55	B0_P6_U1_CFG21: 0x40010CD5
B0_P7_U0_CFG21: 0x40010E55	B0_P7_U1_CFG21: 0x40010ED5
B1_P2_U0_CFG21: 0x40011455	B1_P2_U1_CFG21: 0x400114D5
B1_P3_U0_CFG21: 0x40011655	B1_P3_U1_CFG21: 0x400116D5
B1_P4_U0_CFG21: 0x40011855	B1_P4_U1_CFG21: 0x400118D5
B1_P5_U0_CFG21: 0x40011A55	B1_P5_U1_CFG21: 0x40011AD5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							NC1	NC0

Spare register bits

Bits	Name	Description
1	NC1	Spare register bit
0	NC0	Spare register bit

1.3.1153 B[0..3]_P[0..7]_U[0..1]_CFG22

CFG22

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG22: 0x40010056	B0_P0_U1_CFG22: 0x400100D6
B0_P1_U0_CFG22: 0x40010256	B0_P1_U1_CFG22: 0x400102D6
B0_P2_U0_CFG22: 0x40010456	B0_P2_U1_CFG22: 0x400104D6
B0_P3_U0_CFG22: 0x40010656	B0_P3_U1_CFG22: 0x400106D6
B0_P4_U0_CFG22: 0x40010856	B0_P4_U1_CFG22: 0x400108D6
B0_P5_U0_CFG22: 0x40010A56	B0_P5_U1_CFG22: 0x40010AD6
B0_P6_U0_CFG22: 0x40010C56	B0_P6_U1_CFG22: 0x40010CD6
B0_P7_U0_CFG22: 0x40010E56	B0_P7_U1_CFG22: 0x40010ED6
B1_P2_U0_CFG22: 0x40011456	B1_P2_U1_CFG22: 0x400114D6
B1_P3_U0_CFG22: 0x40011656	B1_P3_U1_CFG22: 0x400116D6
B1_P4_U0_CFG22: 0x40011856	B1_P4_U1_CFG22: 0x400118D6
B1_P5_U0_CFG22: 0x40011A56	B1_P5_U1_CFG22: 0x40011AD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:00	
HW Access	NA				R	R	R	
Name					SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL	

Status Output Control

Bits	Name	Description
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module See Table 1-761.
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 See Table 1-760.
1:0	SC_OUT_CTL[1:0]	Selects the output source for the Status and Control routing connections See Table 1-759.

Table 1-759. Bit field encoding: OUT_CTL_ENUM

Value	Name	Description
2'b00	CONTROL	Control out, 8-bits of control are driven to the routing connections
2'b01	PARALLEL	Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections
2'b10	COUNTER	Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections
2'b11	RESERVED	Reserved

1.3.1153 B[0..3]_P[0..7]_U[0..1]_CFG22 (continued)

Table 1-760. Bit field encoding: SC_INT_MD_ENUM

Value	Name	Description
1'b0	NORMAL	Normal Mode - Routing connection sc_io[3] is a normal input to the status register
1'b1	INT_MODE	Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output

Table 1-761. Bit field encoding: SC_SYNC_MD_ENUM

Value	Name	Description
1'b0	NORMAL	Normal Mode - Status register operation
1'b1	SYNC_MODE	Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs

1.3.1154 B[0..3]_P[0..7]_U[0..1]_CFG23

CFG23

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG23: 0x40010057	B0_P0_U1_CFG23: 0x400100D7
B0_P1_U0_CFG23: 0x40010257	B0_P1_U1_CFG23: 0x400102D7
B0_P2_U0_CFG23: 0x40010457	B0_P2_U1_CFG23: 0x400104D7
B0_P3_U0_CFG23: 0x40010657	B0_P3_U1_CFG23: 0x400106D7
B0_P4_U0_CFG23: 0x40010857	B0_P4_U1_CFG23: 0x400108D7
B0_P5_U0_CFG23: 0x40010A57	B0_P5_U1_CFG23: 0x40010AD7
B0_P6_U0_CFG23: 0x40010C57	B0_P6_U1_CFG23: 0x40010CD7
B0_P7_U0_CFG23: 0x40010E57	B0_P7_U1_CFG23: 0x40010ED7
B1_P2_U0_CFG23: 0x40011457	B1_P2_U1_CFG23: 0x400114D7
B1_P3_U0_CFG23: 0x40011657	B1_P3_U1_CFG23: 0x400116D7
B1_P4_U0_CFG23: 0x40011857	B1_P4_U1_CFG23: 0x400118D7
B1_P5_U0_CFG23: 0x40011A57	B1_P5_U1_CFG23: 0x40011AD7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	NA		R	R	R		R	
Name			ROUTE_EN	ROUTE_LD	CNT_EN_SEL		CNT_LD_SEL	

Counter Routing Control

Bits	Name	Description
5	ROUTE_EN	Configure the counter enable signal for routing input See Table 1-764.
4	ROUTE_LD	Configure the counter load signal for routing input See Table 1-765.
3:2	CNT_EN_SEL[1:0]	Selects the routing inputs for the counter enable signal See Table 1-762.
1:0	CNT_LD_SEL[1:0]	Selects the routing inputs for the counter load signal See Table 1-763.

Table 1-762. Bit field encoding: SC_CNT_EN_ENUM

Value	Name	Description
2'b00	SC_IN4	sc_in[4]
2'b01	SC_IN5	sc_in[5]
2'b10	SC_IN6	sc_in[6]
2'b11	SC_IO	sc_io, (SC_IO_CTL must be set to Input Mode)

1.3.1154 B[0..3]_P[0..7]_U[0..1]_CFG23 (continued)

Table 1-763. Bit field encoding: SC_CNT_LD_ENUM

Value	Name	Description
2'b00	SC_IN0	sc_in[0]
2'b01	SC_IN1	sc_in[1]
2'b10	SC_IN2	sc_in[2]
2'b11	SC_IN3	sc_in[3]

Table 1-764. Bit field encoding: SC_ROUTE_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register)
1'b1	ROUTED	Routed EN signal is used, CNT START must be set

Table 1-765. Bit field encoding: SC_ROUTE_LD_ENUM

Value	Name	Description
1'b0	DISABLE	Routed LD signal is not used
1'b1	ROUTED	Routed LD signal is used

1.3.1155 B[0..3]_P[0..7]_U[0..1]_CFG24

CFG24

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG24: 0x40010058	B0_P0_U1_CFG24: 0x400100D8
B0_P1_U0_CFG24: 0x40010258	B0_P1_U1_CFG24: 0x400102D8
B0_P2_U0_CFG24: 0x40010458	B0_P2_U1_CFG24: 0x400104D8
B0_P3_U0_CFG24: 0x40010658	B0_P3_U1_CFG24: 0x400106D8
B0_P4_U0_CFG24: 0x40010858	B0_P4_U1_CFG24: 0x400108D8
B0_P5_U0_CFG24: 0x40010A58	B0_P5_U1_CFG24: 0x40010AD8
B0_P6_U0_CFG24: 0x40010C58	B0_P6_U1_CFG24: 0x40010CD8
B0_P7_U0_CFG24: 0x40010E58	B0_P7_U1_CFG24: 0x40010ED8
B1_P2_U0_CFG24: 0x40011458	B1_P2_U1_CFG24: 0x400114D8
B1_P3_U0_CFG24: 0x40011658	B1_P3_U1_CFG24: 0x400116D8
B1_P4_U0_CFG24: 0x40011858	B1_P4_U1_CFG24: 0x400118D8
B1_P5_U0_CFG24: 0x40011A58	B1_P5_U1_CFG24: 0x40011AD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	NA	R	R	R	R		R	
Name		RC_FRES	RC_INV	RC_EN_INV	RC_EN_MODE		RC_EN_SEL	

PLD0 Clock Enable Selection Register

Bits	Name	Description
6	RC_FRES	Block firmware reset. When this bit is set, the embedded state of the associated block is reset See Table 1-769.
5	RC_INV	Inverted clock selection See Table 1-770.
4	RC_EN_INV	Inverted enable selection See Table 1-766.
3:2	RC_EN_MODE[1:0]	Select operating mode See Table 1-767.
1:0	RC_EN_SEL[1:0]	Select channel route for enable control See Table 1-768.

Table 1-766. Bit field encoding: RC_EN_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted

1.3.1155 B[0..3]_P[0..7]_U[0..1]_CFG24 (continued)

Table 1-766. Bit field encoding: RC_EN_INV_ENUM

1'b1	INVERTED	Inverted

Table 1-767. Bit field encoding: RC_EN_MODE_ENUM

Value	Name	Description
2'b00	OFF	Always off
2'b01	ON	Always on
2'b10	POSEDGE	Positive edge
2'b11	LEVEL	Level sensitive

Table 1-768. Bit field encoding: RC_EN_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-769. Bit field encoding: RC_FRES_ENUM

Value	Name	Description
1'b0	Normal	Block is not held in reset.
1'b1	Reset	Block is held reset.

Table 1-770. Bit field encoding: RC_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

1.3.1156 B[0..3]_P[0..7]_U[0..1]_CFG25

CFG25

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG25: 0x40010059	B0_P0_U1_CFG25: 0x400100D9
B0_P1_U0_CFG25: 0x40010259	B0_P1_U1_CFG25: 0x400102D9
B0_P2_U0_CFG25: 0x40010459	B0_P2_U1_CFG25: 0x400104D9
B0_P3_U0_CFG25: 0x40010659	B0_P3_U1_CFG25: 0x400106D9
B0_P4_U0_CFG25: 0x40010859	B0_P4_U1_CFG25: 0x400108D9
B0_P5_U0_CFG25: 0x40010A59	B0_P5_U1_CFG25: 0x40010AD9
B0_P6_U0_CFG25: 0x40010C59	B0_P6_U1_CFG25: 0x40010CD9
B0_P7_U0_CFG25: 0x40010E59	B0_P7_U1_CFG25: 0x40010ED9
B1_P2_U0_CFG25: 0x40011459	B1_P2_U1_CFG25: 0x400114D9
B1_P3_U0_CFG25: 0x40011659	B1_P3_U1_CFG25: 0x400116D9
B1_P4_U0_CFG25: 0x40011859	B1_P4_U1_CFG25: 0x400118D9
B1_P5_U0_CFG25: 0x40011A59	B1_P5_U1_CFG25: 0x40011AD9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	NA	R	R	R	R		R	
Name		RC_FRES	RC_INV	RC_EN_INV	RC_EN_MODE		RC_EN_SEL	

PLD1 Clock Enable Selection Register

Bits	Name	Description
6	RC_FRES	Block firmware reset. When this bit is set, the embedded state of the associated block is reset See Table 1-774.
5	RC_INV	Inverted clock selection See Table 1-775.
4	RC_EN_INV	Inverted enable selection See Table 1-771.
3:2	RC_EN_MODE[1:0]	Select operating mode See Table 1-772.
1:0	RC_EN_SEL[1:0]	Select channel route for enable control See Table 1-773.

Table 1-771. Bit field encoding: RC_EN_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted

1.3.1156 B[0..3]_P[0..7]_U[0..1]_CFG25 (continued)

Table 1-771. Bit field encoding: RC_EN_INV_ENUM

1'b1	INVERTED	Inverted

Table 1-772. Bit field encoding: RC_EN_MODE_ENUM

Value	Name	Description
2'b00	OFF	Always off
2'b01	ON	Always on
2'b10	POSEDGE	Positive edge
2'b11	LEVEL	Level sensitive

Table 1-773. Bit field encoding: RC_EN_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-774. Bit field encoding: RC_FRES_ENUM

Value	Name	Description
1'b0	Normal	Block is not held in reset.
1'b1	Reset	Block is held reset.

Table 1-775. Bit field encoding: RC_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

1.3.1157 B[0..3]_P[0..7]_U[0..1]_CFG26

CFG26

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG26: 0x4001005A	B0_P0_U1_CFG26: 0x400100DA
B0_P1_U0_CFG26: 0x4001025A	B0_P1_U1_CFG26: 0x400102DA
B0_P2_U0_CFG26: 0x4001045A	B0_P2_U1_CFG26: 0x400104DA
B0_P3_U0_CFG26: 0x4001065A	B0_P3_U1_CFG26: 0x400106DA
B0_P4_U0_CFG26: 0x4001085A	B0_P4_U1_CFG26: 0x400108DA
B0_P5_U0_CFG26: 0x40010A5A	B0_P5_U1_CFG26: 0x40010ADA
B0_P6_U0_CFG26: 0x40010C5A	B0_P6_U1_CFG26: 0x40010CDA
B0_P7_U0_CFG26: 0x40010E5A	B0_P7_U1_CFG26: 0x40010EDA
B1_P2_U0_CFG26: 0x4001145A	B1_P2_U1_CFG26: 0x400114DA
B1_P3_U0_CFG26: 0x4001165A	B1_P3_U1_CFG26: 0x400116DA
B1_P4_U0_CFG26: 0x4001185A	B1_P4_U1_CFG26: 0x400118DA
B1_P5_U0_CFG26: 0x40011A5A	B1_P5_U1_CFG26: 0x40011ADA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	NA	R	R	R	R		R	
Name		RC_FRES	RC_INV	RC_EN_INV	RC_EN_MODE		RC_EN_SEL	

Datapath Clock Enable Selection Register

Bits	Name	Description
6	RC_FRES	Block firmware reset. When this bit is set, the embedded state of the associated block is reset See Table 1-779.
5	RC_INV	Inverted clock selection See Table 1-780.
4	RC_EN_INV	Inverted enable selection See Table 1-776.
3:2	RC_EN_MODE[1:0]	Select operating mode See Table 1-777.
1:0	RC_EN_SEL[1:0]	Select channel route for enable control See Table 1-778.

Table 1-776. Bit field encoding: RC_EN_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted

1.3.1157 B[0..3]_P[0..7]_U[0..1]_CFG26 (continued)

Table 1-776. Bit field encoding: RC_EN_INV_ENUM

1'b1	INVERTED	Inverted

Table 1-777. Bit field encoding: RC_EN_MODE_ENUM

Value	Name	Description
2'b00	OFF	Always off
2'b01	ON	Always on
2'b10	POSEDGE	Positive edge
2'b11	LEVEL	Level sensitive

Table 1-778. Bit field encoding: RC_EN_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-779. Bit field encoding: RC_FRES_ENUM

Value	Name	Description
1'b0	Normal	Block is not held in reset.
1'b1	Reset	Block is held reset.

Table 1-780. Bit field encoding: RC_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

1.3.1158 B[0..3]_P[0..7]_U[0..1]_CFG27

CFG27

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG27: 0x4001005B	B0_P0_U1_CFG27: 0x400100DB
B0_P1_U0_CFG27: 0x4001025B	B0_P1_U1_CFG27: 0x400102DB
B0_P2_U0_CFG27: 0x4001045B	B0_P2_U1_CFG27: 0x400104DB
B0_P3_U0_CFG27: 0x4001065B	B0_P3_U1_CFG27: 0x400106DB
B0_P4_U0_CFG27: 0x4001085B	B0_P4_U1_CFG27: 0x400108DB
B0_P5_U0_CFG27: 0x40010A5B	B0_P5_U1_CFG27: 0x40010ADB
B0_P6_U0_CFG27: 0x40010C5B	B0_P6_U1_CFG27: 0x40010CDB
B0_P7_U0_CFG27: 0x40010E5B	B0_P7_U1_CFG27: 0x40010EDB
B1_P2_U0_CFG27: 0x4001145B	B1_P2_U1_CFG27: 0x400114DB
B1_P3_U0_CFG27: 0x4001165B	B1_P3_U1_CFG27: 0x400116DB
B1_P4_U0_CFG27: 0x4001185B	B1_P4_U1_CFG27: 0x400118DB
B1_P5_U0_CFG27: 0x40011A5B	B1_P5_U1_CFG27: 0x40011ADB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	NA	R	R	R	R		R	
Name		RC_FRES	RC_INV	RC_EN_INV	RC_EN_MODE		RC_EN_SEL	

Status and Control Clock Enable Selection Register

Bits	Name	Description
6	RC_FRES	Block firmware reset. When this bit is set, the embedded state of the associated block is reset See Table 1-784.
5	RC_INV	Inverted clock selection See Table 1-785.
4	RC_EN_INV	Inverted enable selection See Table 1-781.
3:2	RC_EN_MODE[1:0]	Select operating mode See Table 1-782.
1:0	RC_EN_SEL[1:0]	Select channel route for enable control See Table 1-783.

Table 1-781. Bit field encoding: RC_EN_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted

1.3.1158 B[0..3]_P[0..7]_U[0..1]_CFG27 (continued)

Table 1-781. Bit field encoding: RC_EN_INV_ENUM

1'b1	INVERTED	Inverted

Table 1-782. Bit field encoding: RC_EN_MODE_ENUM

Value	Name	Description
2'b00	OFF	Always off
2'b01	ON	Always on
2'b10	POSEDGE	Positive edge
2'b11	LEVEL	Level sensitive

Table 1-783. Bit field encoding: RC_EN_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-784. Bit field encoding: RC_FRES_ENUM

Value	Name	Description
1'b0	Normal	Block is not held in reset.
1'b1	Reset	Block is held reset.

Table 1-785. Bit field encoding: RC_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

1.3.1159 B[0..3]_P[0..7]_U[0..1]_CFG28

CFG28

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG28: 0x4001005C	B0_P0_U1_CFG28: 0x400100DC
B0_P1_U0_CFG28: 0x4001025C	B0_P1_U1_CFG28: 0x400102DC
B0_P2_U0_CFG28: 0x4001045C	B0_P2_U1_CFG28: 0x400104DC
B0_P3_U0_CFG28: 0x4001065C	B0_P3_U1_CFG28: 0x400106DC
B0_P4_U0_CFG28: 0x4001085C	B0_P4_U1_CFG28: 0x400108DC
B0_P5_U0_CFG28: 0x40010A5C	B0_P5_U1_CFG28: 0x40010ADC
B0_P6_U0_CFG28: 0x40010C5C	B0_P6_U1_CFG28: 0x40010CDC
B0_P7_U0_CFG28: 0x40010E5C	B0_P7_U1_CFG28: 0x40010EDC
B1_P2_U0_CFG28: 0x4001145C	B1_P2_U1_CFG28: 0x400114DC
B1_P3_U0_CFG28: 0x4001165C	B1_P3_U1_CFG28: 0x400116DC
B1_P4_U0_CFG28: 0x4001185C	B1_P4_U1_CFG28: 0x400118DC
B1_P5_U0_CFG28: 0x40011A5C	B1_P5_U1_CFG28: 0x40011ADC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Name	PLD1_CK_SEL				PLD0_CK_SEL			

Clock Selection, PLD1 and PLD0

Bits	Name	Description
7:4	PLD1_CK_SEL[3:0]	Clock selection registers See Table 1-786.
3:0	PLD0_CK_SEL[3:0]	Clock selection registers See Table 1-786.

Table 1-786. Bit field encoding: RC_CK_SEL_ENUM

Value	Name	Description
4'b0000	GCLK0	gclk[0]
4'b0001	GCLK1	gclk[1]
4'b0010	GCLK2	gclk[2]
4'b0011	GCLK3	gclk[3]
4'b0100	GCLK4	gclk[4]
4'b0101	GCLK5	gclk[5]
4'b0110	GCLK6	gclk[6]
4'b0111	GCLK7	gclk[7]
4'b1000	EXT_CLK	ext_clk
4'b1001	SYSCLK	sysclk

1.3.1160 B[0..3]_P[0..7]_U[0..1]_CFG29

CFG29

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG29: 0x4001005D	B0_P0_U1_CFG29: 0x400100DD
B0_P1_U0_CFG29: 0x4001025D	B0_P1_U1_CFG29: 0x400102DD
B0_P2_U0_CFG29: 0x4001045D	B0_P2_U1_CFG29: 0x400104DD
B0_P3_U0_CFG29: 0x4001065D	B0_P3_U1_CFG29: 0x400106DD
B0_P4_U0_CFG29: 0x4001085D	B0_P4_U1_CFG29: 0x400108DD
B0_P5_U0_CFG29: 0x40010A5D	B0_P5_U1_CFG29: 0x40010ADD
B0_P6_U0_CFG29: 0x40010C5D	B0_P6_U1_CFG29: 0x40010CDD
B0_P7_U0_CFG29: 0x40010E5D	B0_P7_U1_CFG29: 0x40010EDD
B1_P2_U0_CFG29: 0x4001145D	B1_P2_U1_CFG29: 0x400114DD
B1_P3_U0_CFG29: 0x4001165D	B1_P3_U1_CFG29: 0x400116DD
B1_P4_U0_CFG29: 0x4001185D	B1_P4_U1_CFG29: 0x400118DD
B1_P5_U0_CFG29: 0x40011A5D	B1_P5_U1_CFG29: 0x40011ADD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Name	SC_CK_SEL				DP_CK_SEL			

Clock Selection, Datapath, Status and Control

Bits	Name	Description
7:4	SC_CK_SEL[3:0]	Clock selection registers See Table 1-787.
3:0	DP_CK_SEL[3:0]	Clock selection registers See Table 1-787.

Table 1-787. Bit field encoding: RC_CK_SEL_ENUM

Value	Name	Description
4'b0000	GCLK0	gclk[0]
4'b0001	GCLK1	gclk[1]
4'b0010	GCLK2	gclk[2]
4'b0011	GCLK3	gclk[3]
4'b0100	GCLK4	gclk[4]
4'b0101	GCLK5	gclk[5]
4'b0110	GCLK6	gclk[6]
4'b0111	GCLK7	gclk[7]
4'b1000	EXT_CLK	ext_clk
4'b1001	SYSCLK	sysclk

1.3.1161 B[0..3]_P[0..7]_U[0..1]_CFG30

CFG30

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG30: 0x4001005E	B0_P0_U1_CFG30: 0x400100DE
B0_P1_U0_CFG30: 0x4001025E	B0_P1_U1_CFG30: 0x400102DE
B0_P2_U0_CFG30: 0x4001045E	B0_P2_U1_CFG30: 0x400104DE
B0_P3_U0_CFG30: 0x4001065E	B0_P3_U1_CFG30: 0x400106DE
B0_P4_U0_CFG30: 0x4001085E	B0_P4_U1_CFG30: 0x400108DE
B0_P5_U0_CFG30: 0x40010A5E	B0_P5_U1_CFG30: 0x40010ADE
B0_P6_U0_CFG30: 0x40010C5E	B0_P6_U1_CFG30: 0x40010CDE
B0_P7_U0_CFG30: 0x40010E5E	B0_P7_U1_CFG30: 0x40010EDE
B1_P2_U0_CFG30: 0x4001145E	B1_P2_U1_CFG30: 0x400114DE
B1_P3_U0_CFG30: 0x4001165E	B1_P3_U1_CFG30: 0x400116DE
B1_P4_U0_CFG30: 0x4001185E	B1_P4_U1_CFG30: 0x400118DE
B1_P5_U0_CFG30: 0x40011A5E	B1_P5_U1_CFG30: 0x40011ADE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	NA			R	R	R	R	
Name				GUDB_WR	EN_RES_CNT	RES_POL	RES_SEL	

Reset Selection Register

Bits	Name	Description
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. See Table 1-789.
3	EN_RES_CNT	Enable routed reset to counter/control register See Table 1-788.
2	RES_POL	Select polarity of the routed reset control See Table 1-790.
1:0	RES_SEL[1:0]	Select routing input for routed reset control See Table 1-791.

Table 1-788. Bit field encoding: RC_EN_RES_CNT

Value	Name	Description
1'b0	DISABLE	Routed reset is not applied to counter/control register
1'b1	ENABLE	Routed reset is applied to the counter/control register

1.3.1161 B[0..3]_P[0..7]_U[0..1]_CFG30 (continued)

Table 1-789. Bit field encoding: RC_GUDB_WR

Value	Name	Description
1'b0	DISABLE	Global UDB configuration/working register write is disabled
1'b1	ENABLE	Global UDB configuration/working register write is enabled

Table 1-790. Bit field encoding: RC_RES_POL_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

Table 1-791. Bit field encoding: RC_RES_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

1.3.1162 B[0..3]_P[0..7]_U[0..1]_CFG31

CFG31

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG31: 0x4001005F	B0_P0_U1_CFG31: 0x400100DF
B0_P1_U0_CFG31: 0x4001025F	B0_P1_U1_CFG31: 0x400102DF
B0_P2_U0_CFG31: 0x4001045F	B0_P2_U1_CFG31: 0x400104DF
B0_P3_U0_CFG31: 0x4001065F	B0_P3_U1_CFG31: 0x400106DF
B0_P4_U0_CFG31: 0x4001085F	B0_P4_U1_CFG31: 0x400108DF
B0_P5_U0_CFG31: 0x40010A5F	B0_P5_U1_CFG31: 0x40010ADF
B0_P6_U0_CFG31: 0x40010C5F	B0_P6_U1_CFG31: 0x40010CDF
B0_P7_U0_CFG31: 0x40010E5F	B0_P7_U1_CFG31: 0x40010EDF
B1_P2_U0_CFG31: 0x4001145F	B1_P2_U1_CFG31: 0x400114DF
B1_P3_U0_CFG31: 0x4001165F	B1_P3_U1_CFG31: 0x400116DF
B1_P4_U0_CFG31: 0x4001185F	B1_P4_U1_CFG31: 0x400118DF
B1_P5_U0_CFG31: 0x40011A5F	B1_P5_U1_CFG31: 0x40011ADF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		NA:00		R/W:0	R/W:0
HW Access	NA		R		NA		R	R
Name			EXT_CK_SEL				EXT_SYNC	NC0

Reset and Clock Input Enable

Bits	Name	Description
5:4	EXT_CK_SEL[1:0]	External clock selection See Table 1-792.
1	EXT_SYNC	Enable synchronization of selected external clock See Table 1-793.
0	NC0	Spare register bit

Table 1-792. Bit field encoding: RC_EXT_CK_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-793. Bit field encoding: RC_EXT_SYNC

Value	Name	Description
1'b0	DISABLE	Selected external clock input is not synchronized
1'b1	ENABLE	Selected external clock input is synchronized

1.3.1163 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7]

DCFG

Reset: N/A

Register : Address

B0_P0_U0_DCFG0: 0x40010060	B0_P0_U0_DCFG1: 0x40010062
B0_P0_U0_DCFG2: 0x40010064	B0_P0_U0_DCFG3: 0x40010066
B0_P0_U0_DCFG4: 0x40010068	B0_P0_U0_DCFG5: 0x4001006A
B0_P0_U0_DCFG6: 0x4001006C	B0_P0_U0_DCFG7: 0x4001006E
B0_P0_U1_DCFG0: 0x400100E0	B0_P0_U1_DCFG1: 0x400100E2
B0_P0_U1_DCFG2: 0x400100E4	B0_P0_U1_DCFG3: 0x400100E6
B0_P0_U1_DCFG4: 0x400100E8	B0_P0_U1_DCFG5: 0x400100EA
B0_P0_U1_DCFG6: 0x400100EC	B0_P0_U1_DCFG7: 0x400100EE
B0_P1_U0_DCFG0: 0x40010260	B0_P1_U0_DCFG1: 0x40010262
B0_P1_U0_DCFG2: 0x40010264	B0_P1_U0_DCFG3: 0x40010266
B0_P1_U0_DCFG4: 0x40010268	B0_P1_U0_DCFG5: 0x4001026A
B0_P1_U0_DCFG6: 0x4001026C	B0_P1_U0_DCFG7: 0x4001026E
B0_P1_U1_DCFG0: 0x400102E0	B0_P1_U1_DCFG1: 0x400102E2
B0_P1_U1_DCFG2: 0x400102E4	B0_P1_U1_DCFG3: 0x400102E6
B0_P1_U1_DCFG4: 0x400102E8	B0_P1_U1_DCFG5: 0x400102EA
B0_P1_U1_DCFG6: 0x400102EC	B0_P1_U1_DCFG7: 0x400102EE
B0_P2_U0_DCFG0: 0x40010460	B0_P2_U0_DCFG1: 0x40010462
B0_P2_U0_DCFG2: 0x40010464	B0_P2_U0_DCFG3: 0x40010466
B0_P2_U0_DCFG4: 0x40010468	B0_P2_U0_DCFG5: 0x4001046A
B0_P2_U0_DCFG6: 0x4001046C	B0_P2_U0_DCFG7: 0x4001046E
B0_P2_U1_DCFG0: 0x400104E0	B0_P2_U1_DCFG1: 0x400104E2
B0_P2_U1_DCFG2: 0x400104E4	B0_P2_U1_DCFG3: 0x400104E6
B0_P2_U1_DCFG4: 0x400104E8	B0_P2_U1_DCFG5: 0x400104EA
B0_P2_U1_DCFG6: 0x400104EC	B0_P2_U1_DCFG7: 0x400104EE
B0_P3_U0_DCFG0: 0x40010660	B0_P3_U0_DCFG1: 0x40010662
B0_P3_U0_DCFG2: 0x40010664	B0_P3_U0_DCFG3: 0x40010666
B0_P3_U0_DCFG4: 0x40010668	B0_P3_U0_DCFG5: 0x4001066A
B0_P3_U0_DCFG6: 0x4001066C	B0_P3_U0_DCFG7: 0x4001066E
B0_P3_U1_DCFG0: 0x400106E0	B0_P3_U1_DCFG1: 0x400106E2
B0_P3_U1_DCFG2: 0x400106E4	B0_P3_U1_DCFG3: 0x400106E6
B0_P3_U1_DCFG4: 0x400106E8	B0_P3_U1_DCFG5: 0x400106EA
B0_P3_U1_DCFG6: 0x400106EC	B0_P3_U1_DCFG7: 0x400106EE

1.3.1163 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] (continued)

Register : Address

B0_P4_U0_DCFG0: 0x40010860
B0_P4_U0_DCFG1: 0x40010862
B0_P4_U0_DCFG2: 0x40010864
B0_P4_U0_DCFG3: 0x40010866
B0_P4_U0_DCFG4: 0x40010868
B0_P4_U0_DCFG5: 0x4001086A
B0_P4_U0_DCFG6: 0x4001086C
B0_P4_U0_DCFG7: 0x4001086E
B0_P4_U1_DCFG0: 0x400108E0
B0_P4_U1_DCFG1: 0x400108E2
B0_P4_U1_DCFG2: 0x400108E4
B0_P4_U1_DCFG3: 0x400108E6
B0_P4_U1_DCFG4: 0x400108E8
B0_P4_U1_DCFG5: 0x400108EA
B0_P4_U1_DCFG6: 0x400108EC
B0_P4_U1_DCFG7: 0x400108EE
B0_P5_U0_DCFG0: 0x40010A60
B0_P5_U0_DCFG1: 0x40010A62
B0_P5_U0_DCFG2: 0x40010A64
B0_P5_U0_DCFG3: 0x40010A66
B0_P5_U0_DCFG4: 0x40010A68
B0_P5_U0_DCFG5: 0x40010A6A
B0_P5_U0_DCFG6: 0x40010A6C
B0_P5_U0_DCFG7: 0x40010A6E
B0_P5_U1_DCFG0: 0x40010AE0
B0_P5_U1_DCFG1: 0x40010AE2
B0_P5_U1_DCFG2: 0x40010AE4
B0_P5_U1_DCFG3: 0x40010AE6
B0_P5_U1_DCFG4: 0x40010AE8
B0_P5_U1_DCFG5: 0x40010AEA
B0_P5_U1_DCFG6: 0x40010AEC
B0_P5_U1_DCFG7: 0x40010AEE
B0_P6_U0_DCFG0: 0x40010C60
B0_P6_U0_DCFG1: 0x40010C62
B0_P6_U0_DCFG2: 0x40010C64
B0_P6_U0_DCFG3: 0x40010C66
B0_P6_U0_DCFG4: 0x40010C68
B0_P6_U0_DCFG5: 0x40010C6A
B0_P6_U0_DCFG6: 0x40010C6C
B0_P6_U0_DCFG7: 0x40010C6E
B0_P6_U1_DCFG0: 0x40010CE0
B0_P6_U1_DCFG1: 0x40010CE2
B0_P6_U1_DCFG2: 0x40010CE4
B0_P6_U1_DCFG3: 0x40010CE6
B0_P6_U1_DCFG4: 0x40010CE8
B0_P6_U1_DCFG5: 0x40010CEA
B0_P6_U1_DCFG6: 0x40010CEC
B0_P6_U1_DCFG7: 0x40010CEE
B0_P7_U0_DCFG0: 0x40010E60
B0_P7_U0_DCFG1: 0x40010E62
B0_P7_U0_DCFG2: 0x40010E64
B0_P7_U0_DCFG3: 0x40010E66
B0_P7_U0_DCFG4: 0x40010E68
B0_P7_U0_DCFG5: 0x40010E6A
B0_P7_U0_DCFG6: 0x40010E6C
B0_P7_U0_DCFG7: 0x40010E6E
B0_P7_U1_DCFG0: 0x40010EE0
B0_P7_U1_DCFG1: 0x40010EE2
B0_P7_U1_DCFG2: 0x40010EE4
B0_P7_U1_DCFG3: 0x40010EE6
B0_P7_U1_DCFG4: 0x40010EE8
B0_P7_U1_DCFG5: 0x40010EEA
B0_P7_U1_DCFG6: 0x40010EEC
B0_P7_U1_DCFG7: 0x40010EEE
B1_P2_U0_DCFG0: 0x40011460
B1_P2_U0_DCFG1: 0x40011462
B1_P2_U0_DCFG2: 0x40011464
B1_P2_U0_DCFG3: 0x40011466
B1_P2_U0_DCFG4: 0x40011468
B1_P2_U0_DCFG5: 0x4001146A
B1_P2_U0_DCFG6: 0x4001146C
B1_P2_U0_DCFG7: 0x4001146E

1.3.1163 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] (continued)

Register : Address

B1_P2_U1_DCFG0: 0x400114E0
B1_P2_U1_DCFG1: 0x400114E2
B1_P2_U1_DCFG2: 0x400114E4
B1_P2_U1_DCFG3: 0x400114E6
B1_P2_U1_DCFG4: 0x400114E8
B1_P2_U1_DCFG5: 0x400114EA
B1_P2_U1_DCFG6: 0x400114EC
B1_P2_U1_DCFG7: 0x400114EE
B1_P3_U0_DCFG0: 0x40011660
B1_P3_U0_DCFG1: 0x40011662
B1_P3_U0_DCFG2: 0x40011664
B1_P3_U0_DCFG3: 0x40011666
B1_P3_U0_DCFG4: 0x40011668
B1_P3_U0_DCFG5: 0x4001166A
B1_P3_U0_DCFG6: 0x4001166C
B1_P3_U0_DCFG7: 0x4001166E
B1_P3_U1_DCFG0: 0x400116E0
B1_P3_U1_DCFG1: 0x400116E2
B1_P3_U1_DCFG2: 0x400116E4
B1_P3_U1_DCFG3: 0x400116E6
B1_P3_U1_DCFG4: 0x400116E8
B1_P3_U1_DCFG5: 0x400116EA
B1_P3_U1_DCFG6: 0x400116EC
B1_P3_U1_DCFG7: 0x400116EE
B1_P4_U0_DCFG0: 0x40011860
B1_P4_U0_DCFG1: 0x40011862
B1_P4_U0_DCFG2: 0x40011864
B1_P4_U0_DCFG3: 0x40011866
B1_P4_U0_DCFG4: 0x40011868
B1_P4_U0_DCFG5: 0x4001186A
B1_P4_U0_DCFG6: 0x4001186C
B1_P4_U0_DCFG7: 0x4001186E
B1_P4_U1_DCFG0: 0x400118E0
B1_P4_U1_DCFG1: 0x400118E2
B1_P4_U1_DCFG2: 0x400118E4
B1_P4_U1_DCFG3: 0x400118E6
B1_P4_U1_DCFG4: 0x400118E8
B1_P4_U1_DCFG5: 0x400118EA
B1_P4_U1_DCFG6: 0x400118EC
B1_P4_U1_DCFG7: 0x400118EE
B1_P5_U0_DCFG0: 0x40011A60
B1_P5_U0_DCFG1: 0x40011A62
B1_P5_U0_DCFG2: 0x40011A64
B1_P5_U0_DCFG3: 0x40011A66
B1_P5_U0_DCFG4: 0x40011A68
B1_P5_U0_DCFG5: 0x40011A6A
B1_P5_U0_DCFG6: 0x40011A6C
B1_P5_U0_DCFG7: 0x40011A6E
B1_P5_U1_DCFG0: 0x40011AE0
B1_P5_U1_DCFG1: 0x40011AE2
B1_P5_U1_DCFG2: 0x40011AE4
B1_P5_U1_DCFG3: 0x40011AE6
B1_P5_U1_DCFG4: 0x40011AE8
B1_P5_U1_DCFG5: 0x40011AEA
B1_P5_U1_DCFG6: 0x40011AEC
B1_P5_U1_DCFG7: 0x40011AEE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UU		R/W:UU		R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC		A1_WR_SRC		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUU			R/W:U	R/W:UU		R/W:UU	
HW Access	R			R	R		R	

1.3.1163 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] (continued)

Name	FUNC	SRC_A	SRC_B	SHIFT

Dynamic Configuration RAM

Bits	Name	Description
15:13	FUNC[2:0]	Dynamic ALU function selection See Table 1-799.
12	SRC_A	Dynamic ALU source A selection See Table 1-802.
11:10	SRC_B[1:0]	Dynamic ALU source B selection See Table 1-803.
9:8	SHIFT[1:0]	Dynamic shift selection See Table 1-800.
7:6	A0_WR_SRC[1:0]	Dynamic A0 write srouce selection See Table 1-794.
5:4	A1_WR_SRC[1:0]	Dynamic A1 write srouce selection See Table 1-795.
3	CFB_EN	Dynamic CRC feedback selection See Table 1-796.
2	CI_SEL	Dynamic carry in selection See Table 1-797.
1	SI_SEL	Dynamic shift in selection See Table 1-801.
0	CMP_SEL	Dynamic compare selection See Table 1-798.

Table 1-794. Bit field encoding: A0_WR_SRC_ENUM

Value	Name	Description
2'b00	NOWRITE	no value written to A0
2'b01	ALU	ALU output written to A0
2'b10	D0	D0 value written to A0
2'b11	F0	F0 value written to A0

Table 1-795. Bit field encoding: A1_WR_SRC_ENUM

Value	Name	Description
2'b00	NOWRITE	no value written to A1
2'b01	ALU	ALU output written to A1
2'b10	D1	D1 value written to A1
2'b11	F1	F1 value written to A1

Table 1-796. Bit field encoding: CFB_EN_ENUM

Value	Name	Description
1'b0	DISABLE	CRC feedback disabled
1'b1	ENABLE	CRC feedback enabled

1.3.1163 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7] (continued)

Table 1-797. Bit field encoding: CI_SEL_ENUM

Value	Name	Description
1'b0	CFG_A	Configuration A
1'b1	CFG_B	Configuration B

Table 1-798. Bit field encoding: CMP_SEL_ENUM

Value	Name	Description
1'b0	CFG_A	Configuration A
1'b1	CFG_B	Configuration B

Table 1-799. Bit field encoding: FUNC_ENUM

Value	Name	Description
3'b000	PASS	Pass
3'b001	INC_A	Increment source A
3'b010	DEC_A	Decrement source A
3'b011	ADD	Add
3'b100	SUB	Subtract
3'b101	XOR	Bitwise XOR
3'b110	AND	Bitwise AND
3'b111	OR	Bitwise OR

Table 1-800. Bit field encoding: SHIFT_ENUM

Value	Name	Description
2'b00	NOSHIFT	No shift
2'b01	LEFT	Left shift
2'b10	RIGHT	Right shift
2'b11	SWAP	Nibble swap

Table 1-801. Bit field encoding: SI_SEL_ENUM

Value	Name	Description
1'b0	CFG_A	Configuration A
1'b1	CFG_B	Configuration B

Table 1-802. Bit field encoding: SRC_A_ENUM

Value	Name	Description
1'b0	A0	ALU source A is A0
1'b1	A1	ALU source A is A1

Table 1-803. Bit field encoding: SRC_B_ENUM

Value	Name	Description
2'b00	D0	ALU source B is D0
2'b01	D1	ALU source B is D1
2'b10	A0	ALU source B is A0
2'b11	A1	ALU source B is A1

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127]

HC

Reset: N/A

Register : Address

B0_P0_ROUTE_HC0: 0x40010100	B0_P0_ROUTE_HC1: 0x40010101
B0_P0_ROUTE_HC2: 0x40010102	B0_P0_ROUTE_HC3: 0x40010103
B0_P0_ROUTE_HC4: 0x40010104	B0_P0_ROUTE_HC5: 0x40010105
B0_P0_ROUTE_HC6: 0x40010106	B0_P0_ROUTE_HC7: 0x40010107
B0_P0_ROUTE_HC8: 0x40010108	B0_P0_ROUTE_HC9: 0x40010109
B0_P0_ROUTE_HC10: 0x4001010A	B0_P0_ROUTE_HC11: 0x4001010B
B0_P0_ROUTE_HC12: 0x4001010C	B0_P0_ROUTE_HC13: 0x4001010D
B0_P0_ROUTE_HC14: 0x4001010E	B0_P0_ROUTE_HC15: 0x4001010F
B0_P0_ROUTE_HC16: 0x40010110	B0_P0_ROUTE_HC17: 0x40010111
B0_P0_ROUTE_HC18: 0x40010112	B0_P0_ROUTE_HC19: 0x40010113
B0_P0_ROUTE_HC20: 0x40010114	B0_P0_ROUTE_HC21: 0x40010115
B0_P0_ROUTE_HC22: 0x40010116	B0_P0_ROUTE_HC23: 0x40010117
B0_P0_ROUTE_HC24: 0x40010118	B0_P0_ROUTE_HC25: 0x40010119
B0_P0_ROUTE_HC26: 0x4001011A	B0_P0_ROUTE_HC27: 0x4001011B
B0_P0_ROUTE_HC28: 0x4001011C	B0_P0_ROUTE_HC29: 0x4001011D
B0_P0_ROUTE_HC30: 0x4001011E	B0_P0_ROUTE_HC31: 0x4001011F
B0_P0_ROUTE_HC32: 0x40010120	B0_P0_ROUTE_HC33: 0x40010121
B0_P0_ROUTE_HC34: 0x40010122	B0_P0_ROUTE_HC35: 0x40010123
B0_P0_ROUTE_HC36: 0x40010124	B0_P0_ROUTE_HC37: 0x40010125
B0_P0_ROUTE_HC38: 0x40010126	B0_P0_ROUTE_HC39: 0x40010127
B0_P0_ROUTE_HC40: 0x40010128	B0_P0_ROUTE_HC41: 0x40010129
B0_P0_ROUTE_HC42: 0x4001012A	B0_P0_ROUTE_HC43: 0x4001012B
B0_P0_ROUTE_HC44: 0x4001012C	B0_P0_ROUTE_HC45: 0x4001012D
B0_P0_ROUTE_HC46: 0x4001012E	B0_P0_ROUTE_HC47: 0x4001012F
B0_P0_ROUTE_HC48: 0x40010130	B0_P0_ROUTE_HC49: 0x40010131
B0_P0_ROUTE_HC50: 0x40010132	B0_P0_ROUTE_HC51: 0x40010133
B0_P0_ROUTE_HC52: 0x40010134	B0_P0_ROUTE_HC53: 0x40010135
B0_P0_ROUTE_HC54: 0x40010136	B0_P0_ROUTE_HC55: 0x40010137
B0_P0_ROUTE_HC56: 0x40010138	B0_P0_ROUTE_HC57: 0x40010139
B0_P0_ROUTE_HC58: 0x4001013A	B0_P0_ROUTE_HC59: 0x4001013B
B0_P0_ROUTE_HC60: 0x4001013C	B0_P0_ROUTE_HC61: 0x4001013D
B0_P0_ROUTE_HC62: 0x4001013E	B0_P0_ROUTE_HC63: 0x4001013F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P0_ROUTE_HC64: 0x40010140
B0_P0_ROUTE_HC65: 0x40010141
B0_P0_ROUTE_HC66: 0x40010142
B0_P0_ROUTE_HC67: 0x40010143
B0_P0_ROUTE_HC68: 0x40010144
B0_P0_ROUTE_HC69: 0x40010145
B0_P0_ROUTE_HC70: 0x40010146
B0_P0_ROUTE_HC71: 0x40010147
B0_P0_ROUTE_HC72: 0x40010148
B0_P0_ROUTE_HC73: 0x40010149
B0_P0_ROUTE_HC74: 0x4001014A
B0_P0_ROUTE_HC75: 0x4001014B
B0_P0_ROUTE_HC76: 0x4001014C
B0_P0_ROUTE_HC77: 0x4001014D
B0_P0_ROUTE_HC78: 0x4001014E
B0_P0_ROUTE_HC79: 0x4001014F
B0_P0_ROUTE_HC80: 0x40010150
B0_P0_ROUTE_HC81: 0x40010151
B0_P0_ROUTE_HC82: 0x40010152
B0_P0_ROUTE_HC83: 0x40010153
B0_P0_ROUTE_HC84: 0x40010154
B0_P0_ROUTE_HC85: 0x40010155
B0_P0_ROUTE_HC86: 0x40010156
B0_P0_ROUTE_HC87: 0x40010157
B0_P0_ROUTE_HC88: 0x40010158
B0_P0_ROUTE_HC89: 0x40010159
B0_P0_ROUTE_HC90: 0x4001015A
B0_P0_ROUTE_HC91: 0x4001015B
B0_P0_ROUTE_HC92: 0x4001015C
B0_P0_ROUTE_HC93: 0x4001015D
B0_P0_ROUTE_HC94: 0x4001015E
B0_P0_ROUTE_HC95: 0x4001015F
B0_P0_ROUTE_HC96: 0x40010160
B0_P0_ROUTE_HC97: 0x40010161
B0_P0_ROUTE_HC98: 0x40010162
B0_P0_ROUTE_HC99: 0x40010163
B0_P0_ROUTE_HC100: 0x40010164
B0_P0_ROUTE_HC101: 0x40010165
B0_P0_ROUTE_HC102: 0x40010166
B0_P0_ROUTE_HC103: 0x40010167
B0_P0_ROUTE_HC104: 0x40010168
B0_P0_ROUTE_HC105: 0x40010169
B0_P0_ROUTE_HC106: 0x4001016A
B0_P0_ROUTE_HC107: 0x4001016B
B0_P0_ROUTE_HC108: 0x4001016C
B0_P0_ROUTE_HC109: 0x4001016D
B0_P0_ROUTE_HC110: 0x4001016E
B0_P0_ROUTE_HC111: 0x4001016F
B0_P0_ROUTE_HC112: 0x40010170
B0_P0_ROUTE_HC113: 0x40010171
B0_P0_ROUTE_HC114: 0x40010172
B0_P0_ROUTE_HC115: 0x40010173
B0_P0_ROUTE_HC116: 0x40010174
B0_P0_ROUTE_HC117: 0x40010175
B0_P0_ROUTE_HC118: 0x40010176
B0_P0_ROUTE_HC119: 0x40010177
B0_P0_ROUTE_HC120: 0x40010178
B0_P0_ROUTE_HC121: 0x40010179
B0_P0_ROUTE_HC122: 0x4001017A
B0_P0_ROUTE_HC123: 0x4001017B
B0_P0_ROUTE_HC124: 0x4001017C
B0_P0_ROUTE_HC125: 0x4001017D
B0_P0_ROUTE_HC126: 0x4001017E
B0_P0_ROUTE_HC127: 0x4001017F
B0_P1_ROUTE_HC0: 0x40010300
B0_P1_ROUTE_HC1: 0x40010301
B0_P1_ROUTE_HC2: 0x40010302
B0_P1_ROUTE_HC3: 0x40010303
B0_P1_ROUTE_HC4: 0x40010304
B0_P1_ROUTE_HC5: 0x40010305
B0_P1_ROUTE_HC6: 0x40010306
B0_P1_ROUTE_HC7: 0x40010307

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P1_ROUTE_HC8: 0x40010308
B0_P1_ROUTE_HC9: 0x40010309
B0_P1_ROUTE_HC10: 0x4001030A
B0_P1_ROUTE_HC11: 0x4001030B
B0_P1_ROUTE_HC12: 0x4001030C
B0_P1_ROUTE_HC13: 0x4001030D
B0_P1_ROUTE_HC14: 0x4001030E
B0_P1_ROUTE_HC15: 0x4001030F
B0_P1_ROUTE_HC16: 0x40010310
B0_P1_ROUTE_HC17: 0x40010311
B0_P1_ROUTE_HC18: 0x40010312
B0_P1_ROUTE_HC19: 0x40010313
B0_P1_ROUTE_HC20: 0x40010314
B0_P1_ROUTE_HC21: 0x40010315
B0_P1_ROUTE_HC22: 0x40010316
B0_P1_ROUTE_HC23: 0x40010317
B0_P1_ROUTE_HC24: 0x40010318
B0_P1_ROUTE_HC25: 0x40010319
B0_P1_ROUTE_HC26: 0x4001031A
B0_P1_ROUTE_HC27: 0x4001031B
B0_P1_ROUTE_HC28: 0x4001031C
B0_P1_ROUTE_HC29: 0x4001031D
B0_P1_ROUTE_HC30: 0x4001031E
B0_P1_ROUTE_HC31: 0x4001031F
B0_P1_ROUTE_HC32: 0x40010320
B0_P1_ROUTE_HC33: 0x40010321
B0_P1_ROUTE_HC34: 0x40010322
B0_P1_ROUTE_HC35: 0x40010323
B0_P1_ROUTE_HC36: 0x40010324
B0_P1_ROUTE_HC37: 0x40010325
B0_P1_ROUTE_HC38: 0x40010326
B0_P1_ROUTE_HC39: 0x40010327
B0_P1_ROUTE_HC40: 0x40010328
B0_P1_ROUTE_HC41: 0x40010329
B0_P1_ROUTE_HC42: 0x4001032A
B0_P1_ROUTE_HC43: 0x4001032B
B0_P1_ROUTE_HC44: 0x4001032C
B0_P1_ROUTE_HC45: 0x4001032D
B0_P1_ROUTE_HC46: 0x4001032E
B0_P1_ROUTE_HC47: 0x4001032F
B0_P1_ROUTE_HC48: 0x40010330
B0_P1_ROUTE_HC49: 0x40010331
B0_P1_ROUTE_HC50: 0x40010332
B0_P1_ROUTE_HC51: 0x40010333
B0_P1_ROUTE_HC52: 0x40010334
B0_P1_ROUTE_HC53: 0x40010335
B0_P1_ROUTE_HC54: 0x40010336
B0_P1_ROUTE_HC55: 0x40010337
B0_P1_ROUTE_HC56: 0x40010338
B0_P1_ROUTE_HC57: 0x40010339
B0_P1_ROUTE_HC58: 0x4001033A
B0_P1_ROUTE_HC59: 0x4001033B
B0_P1_ROUTE_HC60: 0x4001033C
B0_P1_ROUTE_HC61: 0x4001033D
B0_P1_ROUTE_HC62: 0x4001033E
B0_P1_ROUTE_HC63: 0x4001033F
B0_P1_ROUTE_HC64: 0x40010340
B0_P1_ROUTE_HC65: 0x40010341
B0_P1_ROUTE_HC66: 0x40010342
B0_P1_ROUTE_HC67: 0x40010343
B0_P1_ROUTE_HC68: 0x40010344
B0_P1_ROUTE_HC69: 0x40010345
B0_P1_ROUTE_HC70: 0x40010346
B0_P1_ROUTE_HC71: 0x40010347
B0_P1_ROUTE_HC72: 0x40010348
B0_P1_ROUTE_HC73: 0x40010349
B0_P1_ROUTE_HC74: 0x4001034A
B0_P1_ROUTE_HC75: 0x4001034B
B0_P1_ROUTE_HC76: 0x4001034C
B0_P1_ROUTE_HC77: 0x4001034D
B0_P1_ROUTE_HC78: 0x4001034E
B0_P1_ROUTE_HC79: 0x4001034F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P1_ROUTE_HC80: 0x40010350
B0_P1_ROUTE_HC81: 0x40010351
B0_P1_ROUTE_HC82: 0x40010352
B0_P1_ROUTE_HC83: 0x40010353
B0_P1_ROUTE_HC84: 0x40010354
B0_P1_ROUTE_HC85: 0x40010355
B0_P1_ROUTE_HC86: 0x40010356
B0_P1_ROUTE_HC87: 0x40010357
B0_P1_ROUTE_HC88: 0x40010358
B0_P1_ROUTE_HC89: 0x40010359
B0_P1_ROUTE_HC90: 0x4001035A
B0_P1_ROUTE_HC91: 0x4001035B
B0_P1_ROUTE_HC92: 0x4001035C
B0_P1_ROUTE_HC93: 0x4001035D
B0_P1_ROUTE_HC94: 0x4001035E
B0_P1_ROUTE_HC95: 0x4001035F
B0_P1_ROUTE_HC96: 0x40010360
B0_P1_ROUTE_HC97: 0x40010361
B0_P1_ROUTE_HC98: 0x40010362
B0_P1_ROUTE_HC99: 0x40010363
B0_P1_ROUTE_HC100: 0x40010364
B0_P1_ROUTE_HC101: 0x40010365
B0_P1_ROUTE_HC102: 0x40010366
B0_P1_ROUTE_HC103: 0x40010367
B0_P1_ROUTE_HC104: 0x40010368
B0_P1_ROUTE_HC105: 0x40010369
B0_P1_ROUTE_HC106: 0x4001036A
B0_P1_ROUTE_HC107: 0x4001036B
B0_P1_ROUTE_HC108: 0x4001036C
B0_P1_ROUTE_HC109: 0x4001036D
B0_P1_ROUTE_HC110: 0x4001036E
B0_P1_ROUTE_HC111: 0x4001036F
B0_P1_ROUTE_HC112: 0x40010370
B0_P1_ROUTE_HC113: 0x40010371
B0_P1_ROUTE_HC114: 0x40010372
B0_P1_ROUTE_HC115: 0x40010373
B0_P1_ROUTE_HC116: 0x40010374
B0_P1_ROUTE_HC117: 0x40010375
B0_P1_ROUTE_HC118: 0x40010376
B0_P1_ROUTE_HC119: 0x40010377
B0_P1_ROUTE_HC120: 0x40010378
B0_P1_ROUTE_HC121: 0x40010379
B0_P1_ROUTE_HC122: 0x4001037A
B0_P1_ROUTE_HC123: 0x4001037B
B0_P1_ROUTE_HC124: 0x4001037C
B0_P1_ROUTE_HC125: 0x4001037D
B0_P1_ROUTE_HC126: 0x4001037E
B0_P1_ROUTE_HC127: 0x4001037F
B0_P2_ROUTE_HC0: 0x40010500
B0_P2_ROUTE_HC1: 0x40010501
B0_P2_ROUTE_HC2: 0x40010502
B0_P2_ROUTE_HC3: 0x40010503
B0_P2_ROUTE_HC4: 0x40010504
B0_P2_ROUTE_HC5: 0x40010505
B0_P2_ROUTE_HC6: 0x40010506
B0_P2_ROUTE_HC7: 0x40010507
B0_P2_ROUTE_HC8: 0x40010508
B0_P2_ROUTE_HC9: 0x40010509
B0_P2_ROUTE_HC10: 0x4001050A
B0_P2_ROUTE_HC11: 0x4001050B
B0_P2_ROUTE_HC12: 0x4001050C
B0_P2_ROUTE_HC13: 0x4001050D
B0_P2_ROUTE_HC14: 0x4001050E
B0_P2_ROUTE_HC15: 0x4001050F
B0_P2_ROUTE_HC16: 0x40010510
B0_P2_ROUTE_HC17: 0x40010511
B0_P2_ROUTE_HC18: 0x40010512
B0_P2_ROUTE_HC19: 0x40010513
B0_P2_ROUTE_HC20: 0x40010514
B0_P2_ROUTE_HC21: 0x40010515
B0_P2_ROUTE_HC22: 0x40010516
B0_P2_ROUTE_HC23: 0x40010517

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P2_ROUTE_HC24: 0x40010518
B0_P2_ROUTE_HC25: 0x40010519
B0_P2_ROUTE_HC26: 0x4001051A
B0_P2_ROUTE_HC27: 0x4001051B
B0_P2_ROUTE_HC28: 0x4001051C
B0_P2_ROUTE_HC29: 0x4001051D
B0_P2_ROUTE_HC30: 0x4001051E
B0_P2_ROUTE_HC31: 0x4001051F
B0_P2_ROUTE_HC32: 0x40010520
B0_P2_ROUTE_HC33: 0x40010521
B0_P2_ROUTE_HC34: 0x40010522
B0_P2_ROUTE_HC35: 0x40010523
B0_P2_ROUTE_HC36: 0x40010524
B0_P2_ROUTE_HC37: 0x40010525
B0_P2_ROUTE_HC38: 0x40010526
B0_P2_ROUTE_HC39: 0x40010527
B0_P2_ROUTE_HC40: 0x40010528
B0_P2_ROUTE_HC41: 0x40010529
B0_P2_ROUTE_HC42: 0x4001052A
B0_P2_ROUTE_HC43: 0x4001052B
B0_P2_ROUTE_HC44: 0x4001052C
B0_P2_ROUTE_HC45: 0x4001052D
B0_P2_ROUTE_HC46: 0x4001052E
B0_P2_ROUTE_HC47: 0x4001052F
B0_P2_ROUTE_HC48: 0x40010530
B0_P2_ROUTE_HC49: 0x40010531
B0_P2_ROUTE_HC50: 0x40010532
B0_P2_ROUTE_HC51: 0x40010533
B0_P2_ROUTE_HC52: 0x40010534
B0_P2_ROUTE_HC53: 0x40010535
B0_P2_ROUTE_HC54: 0x40010536
B0_P2_ROUTE_HC55: 0x40010537
B0_P2_ROUTE_HC56: 0x40010538
B0_P2_ROUTE_HC57: 0x40010539
B0_P2_ROUTE_HC58: 0x4001053A
B0_P2_ROUTE_HC59: 0x4001053B
B0_P2_ROUTE_HC60: 0x4001053C
B0_P2_ROUTE_HC61: 0x4001053D
B0_P2_ROUTE_HC62: 0x4001053E
B0_P2_ROUTE_HC63: 0x4001053F
B0_P2_ROUTE_HC64: 0x40010540
B0_P2_ROUTE_HC65: 0x40010541
B0_P2_ROUTE_HC66: 0x40010542
B0_P2_ROUTE_HC67: 0x40010543
B0_P2_ROUTE_HC68: 0x40010544
B0_P2_ROUTE_HC69: 0x40010545
B0_P2_ROUTE_HC70: 0x40010546
B0_P2_ROUTE_HC71: 0x40010547
B0_P2_ROUTE_HC72: 0x40010548
B0_P2_ROUTE_HC73: 0x40010549
B0_P2_ROUTE_HC74: 0x4001054A
B0_P2_ROUTE_HC75: 0x4001054B
B0_P2_ROUTE_HC76: 0x4001054C
B0_P2_ROUTE_HC77: 0x4001054D
B0_P2_ROUTE_HC78: 0x4001054E
B0_P2_ROUTE_HC79: 0x4001054F
B0_P2_ROUTE_HC80: 0x40010550
B0_P2_ROUTE_HC81: 0x40010551
B0_P2_ROUTE_HC82: 0x40010552
B0_P2_ROUTE_HC83: 0x40010553
B0_P2_ROUTE_HC84: 0x40010554
B0_P2_ROUTE_HC85: 0x40010555
B0_P2_ROUTE_HC86: 0x40010556
B0_P2_ROUTE_HC87: 0x40010557
B0_P2_ROUTE_HC88: 0x40010558
B0_P2_ROUTE_HC89: 0x40010559
B0_P2_ROUTE_HC90: 0x4001055A
B0_P2_ROUTE_HC91: 0x4001055B
B0_P2_ROUTE_HC92: 0x4001055C
B0_P2_ROUTE_HC93: 0x4001055D
B0_P2_ROUTE_HC94: 0x4001055E
B0_P2_ROUTE_HC95: 0x4001055F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P2_ROUTE_HC96: 0x40010560
B0_P2_ROUTE_HC97: 0x40010561
B0_P2_ROUTE_HC98: 0x40010562
B0_P2_ROUTE_HC99: 0x40010563
B0_P2_ROUTE_HC100: 0x40010564
B0_P2_ROUTE_HC101: 0x40010565
B0_P2_ROUTE_HC102: 0x40010566
B0_P2_ROUTE_HC103: 0x40010567
B0_P2_ROUTE_HC104: 0x40010568
B0_P2_ROUTE_HC105: 0x40010569
B0_P2_ROUTE_HC106: 0x4001056A
B0_P2_ROUTE_HC107: 0x4001056B
B0_P2_ROUTE_HC108: 0x4001056C
B0_P2_ROUTE_HC109: 0x4001056D
B0_P2_ROUTE_HC110: 0x4001056E
B0_P2_ROUTE_HC111: 0x4001056F
B0_P2_ROUTE_HC112: 0x40010570
B0_P2_ROUTE_HC113: 0x40010571
B0_P2_ROUTE_HC114: 0x40010572
B0_P2_ROUTE_HC115: 0x40010573
B0_P2_ROUTE_HC116: 0x40010574
B0_P2_ROUTE_HC117: 0x40010575
B0_P2_ROUTE_HC118: 0x40010576
B0_P2_ROUTE_HC119: 0x40010577
B0_P2_ROUTE_HC120: 0x40010578
B0_P2_ROUTE_HC121: 0x40010579
B0_P2_ROUTE_HC122: 0x4001057A
B0_P2_ROUTE_HC123: 0x4001057B
B0_P2_ROUTE_HC124: 0x4001057C
B0_P2_ROUTE_HC125: 0x4001057D
B0_P2_ROUTE_HC126: 0x4001057E
B0_P2_ROUTE_HC127: 0x4001057F
B0_P3_ROUTE_HC0: 0x40010700
B0_P3_ROUTE_HC1: 0x40010701
B0_P3_ROUTE_HC2: 0x40010702
B0_P3_ROUTE_HC3: 0x40010703
B0_P3_ROUTE_HC4: 0x40010704
B0_P3_ROUTE_HC5: 0x40010705
B0_P3_ROUTE_HC6: 0x40010706
B0_P3_ROUTE_HC7: 0x40010707
B0_P3_ROUTE_HC8: 0x40010708
B0_P3_ROUTE_HC9: 0x40010709
B0_P3_ROUTE_HC10: 0x4001070A
B0_P3_ROUTE_HC11: 0x4001070B
B0_P3_ROUTE_HC12: 0x4001070C
B0_P3_ROUTE_HC13: 0x4001070D
B0_P3_ROUTE_HC14: 0x4001070E
B0_P3_ROUTE_HC15: 0x4001070F
B0_P3_ROUTE_HC16: 0x40010710
B0_P3_ROUTE_HC17: 0x40010711
B0_P3_ROUTE_HC18: 0x40010712
B0_P3_ROUTE_HC19: 0x40010713
B0_P3_ROUTE_HC20: 0x40010714
B0_P3_ROUTE_HC21: 0x40010715
B0_P3_ROUTE_HC22: 0x40010716
B0_P3_ROUTE_HC23: 0x40010717
B0_P3_ROUTE_HC24: 0x40010718
B0_P3_ROUTE_HC25: 0x40010719
B0_P3_ROUTE_HC26: 0x4001071A
B0_P3_ROUTE_HC27: 0x4001071B
B0_P3_ROUTE_HC28: 0x4001071C
B0_P3_ROUTE_HC29: 0x4001071D
B0_P3_ROUTE_HC30: 0x4001071E
B0_P3_ROUTE_HC31: 0x4001071F
B0_P3_ROUTE_HC32: 0x40010720
B0_P3_ROUTE_HC33: 0x40010721
B0_P3_ROUTE_HC34: 0x40010722
B0_P3_ROUTE_HC35: 0x40010723
B0_P3_ROUTE_HC36: 0x40010724
B0_P3_ROUTE_HC37: 0x40010725
B0_P3_ROUTE_HC38: 0x40010726
B0_P3_ROUTE_HC39: 0x40010727

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P3_ROUTE_HC40: 0x40010728
B0_P3_ROUTE_HC41: 0x40010729
B0_P3_ROUTE_HC42: 0x4001072A
B0_P3_ROUTE_HC43: 0x4001072B
B0_P3_ROUTE_HC44: 0x4001072C
B0_P3_ROUTE_HC45: 0x4001072D
B0_P3_ROUTE_HC46: 0x4001072E
B0_P3_ROUTE_HC47: 0x4001072F
B0_P3_ROUTE_HC48: 0x40010730
B0_P3_ROUTE_HC49: 0x40010731
B0_P3_ROUTE_HC50: 0x40010732
B0_P3_ROUTE_HC51: 0x40010733
B0_P3_ROUTE_HC52: 0x40010734
B0_P3_ROUTE_HC53: 0x40010735
B0_P3_ROUTE_HC54: 0x40010736
B0_P3_ROUTE_HC55: 0x40010737
B0_P3_ROUTE_HC56: 0x40010738
B0_P3_ROUTE_HC57: 0x40010739
B0_P3_ROUTE_HC58: 0x4001073A
B0_P3_ROUTE_HC59: 0x4001073B
B0_P3_ROUTE_HC60: 0x4001073C
B0_P3_ROUTE_HC61: 0x4001073D
B0_P3_ROUTE_HC62: 0x4001073E
B0_P3_ROUTE_HC63: 0x4001073F
B0_P3_ROUTE_HC64: 0x40010740
B0_P3_ROUTE_HC65: 0x40010741
B0_P3_ROUTE_HC66: 0x40010742
B0_P3_ROUTE_HC67: 0x40010743
B0_P3_ROUTE_HC68: 0x40010744
B0_P3_ROUTE_HC69: 0x40010745
B0_P3_ROUTE_HC70: 0x40010746
B0_P3_ROUTE_HC71: 0x40010747
B0_P3_ROUTE_HC72: 0x40010748
B0_P3_ROUTE_HC73: 0x40010749
B0_P3_ROUTE_HC74: 0x4001074A
B0_P3_ROUTE_HC75: 0x4001074B
B0_P3_ROUTE_HC76: 0x4001074C
B0_P3_ROUTE_HC77: 0x4001074D
B0_P3_ROUTE_HC78: 0x4001074E
B0_P3_ROUTE_HC79: 0x4001074F
B0_P3_ROUTE_HC80: 0x40010750
B0_P3_ROUTE_HC81: 0x40010751
B0_P3_ROUTE_HC82: 0x40010752
B0_P3_ROUTE_HC83: 0x40010753
B0_P3_ROUTE_HC84: 0x40010754
B0_P3_ROUTE_HC85: 0x40010755
B0_P3_ROUTE_HC86: 0x40010756
B0_P3_ROUTE_HC87: 0x40010757
B0_P3_ROUTE_HC88: 0x40010758
B0_P3_ROUTE_HC89: 0x40010759
B0_P3_ROUTE_HC90: 0x4001075A
B0_P3_ROUTE_HC91: 0x4001075B
B0_P3_ROUTE_HC92: 0x4001075C
B0_P3_ROUTE_HC93: 0x4001075D
B0_P3_ROUTE_HC94: 0x4001075E
B0_P3_ROUTE_HC95: 0x4001075F
B0_P3_ROUTE_HC96: 0x40010760
B0_P3_ROUTE_HC97: 0x40010761
B0_P3_ROUTE_HC98: 0x40010762
B0_P3_ROUTE_HC99: 0x40010763
B0_P3_ROUTE_HC100: 0x40010764
B0_P3_ROUTE_HC101: 0x40010765
B0_P3_ROUTE_HC102: 0x40010766
B0_P3_ROUTE_HC103: 0x40010767
B0_P3_ROUTE_HC104: 0x40010768
B0_P3_ROUTE_HC105: 0x40010769
B0_P3_ROUTE_HC106: 0x4001076A
B0_P3_ROUTE_HC107: 0x4001076B
B0_P3_ROUTE_HC108: 0x4001076C
B0_P3_ROUTE_HC109: 0x4001076D
B0_P3_ROUTE_HC110: 0x4001076E
B0_P3_ROUTE_HC111: 0x4001076F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P3_ROUTE_HC112: 0x40010770
B0_P3_ROUTE_HC113: 0x40010771
B0_P3_ROUTE_HC114: 0x40010772
B0_P3_ROUTE_HC115: 0x40010773
B0_P3_ROUTE_HC116: 0x40010774
B0_P3_ROUTE_HC117: 0x40010775
B0_P3_ROUTE_HC118: 0x40010776
B0_P3_ROUTE_HC119: 0x40010777
B0_P3_ROUTE_HC120: 0x40010778
B0_P3_ROUTE_HC121: 0x40010779
B0_P3_ROUTE_HC122: 0x4001077A
B0_P3_ROUTE_HC123: 0x4001077B
B0_P3_ROUTE_HC124: 0x4001077C
B0_P3_ROUTE_HC125: 0x4001077D
B0_P3_ROUTE_HC126: 0x4001077E
B0_P3_ROUTE_HC127: 0x4001077F
B0_P4_ROUTE_HC0: 0x40010900
B0_P4_ROUTE_HC1: 0x40010901
B0_P4_ROUTE_HC2: 0x40010902
B0_P4_ROUTE_HC3: 0x40010903
B0_P4_ROUTE_HC4: 0x40010904
B0_P4_ROUTE_HC5: 0x40010905
B0_P4_ROUTE_HC6: 0x40010906
B0_P4_ROUTE_HC7: 0x40010907
B0_P4_ROUTE_HC8: 0x40010908
B0_P4_ROUTE_HC9: 0x40010909
B0_P4_ROUTE_HC10: 0x4001090A
B0_P4_ROUTE_HC11: 0x4001090B
B0_P4_ROUTE_HC12: 0x4001090C
B0_P4_ROUTE_HC13: 0x4001090D
B0_P4_ROUTE_HC14: 0x4001090E
B0_P4_ROUTE_HC15: 0x4001090F
B0_P4_ROUTE_HC16: 0x40010910
B0_P4_ROUTE_HC17: 0x40010911
B0_P4_ROUTE_HC18: 0x40010912
B0_P4_ROUTE_HC19: 0x40010913
B0_P4_ROUTE_HC20: 0x40010914
B0_P4_ROUTE_HC21: 0x40010915
B0_P4_ROUTE_HC22: 0x40010916
B0_P4_ROUTE_HC23: 0x40010917
B0_P4_ROUTE_HC24: 0x40010918
B0_P4_ROUTE_HC25: 0x40010919
B0_P4_ROUTE_HC26: 0x4001091A
B0_P4_ROUTE_HC27: 0x4001091B
B0_P4_ROUTE_HC28: 0x4001091C
B0_P4_ROUTE_HC29: 0x4001091D
B0_P4_ROUTE_HC30: 0x4001091E
B0_P4_ROUTE_HC31: 0x4001091F
B0_P4_ROUTE_HC32: 0x40010920
B0_P4_ROUTE_HC33: 0x40010921
B0_P4_ROUTE_HC34: 0x40010922
B0_P4_ROUTE_HC35: 0x40010923
B0_P4_ROUTE_HC36: 0x40010924
B0_P4_ROUTE_HC37: 0x40010925
B0_P4_ROUTE_HC38: 0x40010926
B0_P4_ROUTE_HC39: 0x40010927
B0_P4_ROUTE_HC40: 0x40010928
B0_P4_ROUTE_HC41: 0x40010929
B0_P4_ROUTE_HC42: 0x4001092A
B0_P4_ROUTE_HC43: 0x4001092B
B0_P4_ROUTE_HC44: 0x4001092C
B0_P4_ROUTE_HC45: 0x4001092D
B0_P4_ROUTE_HC46: 0x4001092E
B0_P4_ROUTE_HC47: 0x4001092F
B0_P4_ROUTE_HC48: 0x40010930
B0_P4_ROUTE_HC49: 0x40010931
B0_P4_ROUTE_HC50: 0x40010932
B0_P4_ROUTE_HC51: 0x40010933
B0_P4_ROUTE_HC52: 0x40010934
B0_P4_ROUTE_HC53: 0x40010935
B0_P4_ROUTE_HC54: 0x40010936
B0_P4_ROUTE_HC55: 0x40010937

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P4_ROUTE_HC56: 0x40010938
B0_P4_ROUTE_HC57: 0x40010939
B0_P4_ROUTE_HC58: 0x4001093A
B0_P4_ROUTE_HC59: 0x4001093B
B0_P4_ROUTE_HC60: 0x4001093C
B0_P4_ROUTE_HC61: 0x4001093D
B0_P4_ROUTE_HC62: 0x4001093E
B0_P4_ROUTE_HC63: 0x4001093F
B0_P4_ROUTE_HC64: 0x40010940
B0_P4_ROUTE_HC65: 0x40010941
B0_P4_ROUTE_HC66: 0x40010942
B0_P4_ROUTE_HC67: 0x40010943
B0_P4_ROUTE_HC68: 0x40010944
B0_P4_ROUTE_HC69: 0x40010945
B0_P4_ROUTE_HC70: 0x40010946
B0_P4_ROUTE_HC71: 0x40010947
B0_P4_ROUTE_HC72: 0x40010948
B0_P4_ROUTE_HC73: 0x40010949
B0_P4_ROUTE_HC74: 0x4001094A
B0_P4_ROUTE_HC75: 0x4001094B
B0_P4_ROUTE_HC76: 0x4001094C
B0_P4_ROUTE_HC77: 0x4001094D
B0_P4_ROUTE_HC78: 0x4001094E
B0_P4_ROUTE_HC79: 0x4001094F
B0_P4_ROUTE_HC80: 0x40010950
B0_P4_ROUTE_HC81: 0x40010951
B0_P4_ROUTE_HC82: 0x40010952
B0_P4_ROUTE_HC83: 0x40010953
B0_P4_ROUTE_HC84: 0x40010954
B0_P4_ROUTE_HC85: 0x40010955
B0_P4_ROUTE_HC86: 0x40010956
B0_P4_ROUTE_HC87: 0x40010957
B0_P4_ROUTE_HC88: 0x40010958
B0_P4_ROUTE_HC89: 0x40010959
B0_P4_ROUTE_HC90: 0x4001095A
B0_P4_ROUTE_HC91: 0x4001095B
B0_P4_ROUTE_HC92: 0x4001095C
B0_P4_ROUTE_HC93: 0x4001095D
B0_P4_ROUTE_HC94: 0x4001095E
B0_P4_ROUTE_HC95: 0x4001095F
B0_P4_ROUTE_HC96: 0x40010960
B0_P4_ROUTE_HC97: 0x40010961
B0_P4_ROUTE_HC98: 0x40010962
B0_P4_ROUTE_HC99: 0x40010963
B0_P4_ROUTE_HC100: 0x40010964
B0_P4_ROUTE_HC101: 0x40010965
B0_P4_ROUTE_HC102: 0x40010966
B0_P4_ROUTE_HC103: 0x40010967
B0_P4_ROUTE_HC104: 0x40010968
B0_P4_ROUTE_HC105: 0x40010969
B0_P4_ROUTE_HC106: 0x4001096A
B0_P4_ROUTE_HC107: 0x4001096B
B0_P4_ROUTE_HC108: 0x4001096C
B0_P4_ROUTE_HC109: 0x4001096D
B0_P4_ROUTE_HC110: 0x4001096E
B0_P4_ROUTE_HC111: 0x4001096F
B0_P4_ROUTE_HC112: 0x40010970
B0_P4_ROUTE_HC113: 0x40010971
B0_P4_ROUTE_HC114: 0x40010972
B0_P4_ROUTE_HC115: 0x40010973
B0_P4_ROUTE_HC116: 0x40010974
B0_P4_ROUTE_HC117: 0x40010975
B0_P4_ROUTE_HC118: 0x40010976
B0_P4_ROUTE_HC119: 0x40010977
B0_P4_ROUTE_HC120: 0x40010978
B0_P4_ROUTE_HC121: 0x40010979
B0_P4_ROUTE_HC122: 0x4001097A
B0_P4_ROUTE_HC123: 0x4001097B
B0_P4_ROUTE_HC124: 0x4001097C
B0_P4_ROUTE_HC125: 0x4001097D
B0_P4_ROUTE_HC126: 0x4001097E
B0_P4_ROUTE_HC127: 0x4001097F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P5_ROUTE_HC0: 0x40010B00
B0_P5_ROUTE_HC1: 0x40010B01
B0_P5_ROUTE_HC2: 0x40010B02
B0_P5_ROUTE_HC3: 0x40010B03
B0_P5_ROUTE_HC4: 0x40010B04
B0_P5_ROUTE_HC5: 0x40010B05
B0_P5_ROUTE_HC6: 0x40010B06
B0_P5_ROUTE_HC7: 0x40010B07
B0_P5_ROUTE_HC8: 0x40010B08
B0_P5_ROUTE_HC9: 0x40010B09
B0_P5_ROUTE_HC10: 0x40010B0A
B0_P5_ROUTE_HC11: 0x40010B0B
B0_P5_ROUTE_HC12: 0x40010B0C
B0_P5_ROUTE_HC13: 0x40010B0D
B0_P5_ROUTE_HC14: 0x40010B0E
B0_P5_ROUTE_HC15: 0x40010B0F
B0_P5_ROUTE_HC16: 0x40010B10
B0_P5_ROUTE_HC17: 0x40010B11
B0_P5_ROUTE_HC18: 0x40010B12
B0_P5_ROUTE_HC19: 0x40010B13
B0_P5_ROUTE_HC20: 0x40010B14
B0_P5_ROUTE_HC21: 0x40010B15
B0_P5_ROUTE_HC22: 0x40010B16
B0_P5_ROUTE_HC23: 0x40010B17
B0_P5_ROUTE_HC24: 0x40010B18
B0_P5_ROUTE_HC25: 0x40010B19
B0_P5_ROUTE_HC26: 0x40010B1A
B0_P5_ROUTE_HC27: 0x40010B1B
B0_P5_ROUTE_HC28: 0x40010B1C
B0_P5_ROUTE_HC29: 0x40010B1D
B0_P5_ROUTE_HC30: 0x40010B1E
B0_P5_ROUTE_HC31: 0x40010B1F
B0_P5_ROUTE_HC32: 0x40010B20
B0_P5_ROUTE_HC33: 0x40010B21
B0_P5_ROUTE_HC34: 0x40010B22
B0_P5_ROUTE_HC35: 0x40010B23
B0_P5_ROUTE_HC36: 0x40010B24
B0_P5_ROUTE_HC37: 0x40010B25
B0_P5_ROUTE_HC38: 0x40010B26
B0_P5_ROUTE_HC39: 0x40010B27
B0_P5_ROUTE_HC40: 0x40010B28
B0_P5_ROUTE_HC41: 0x40010B29
B0_P5_ROUTE_HC42: 0x40010B2A
B0_P5_ROUTE_HC43: 0x40010B2B
B0_P5_ROUTE_HC44: 0x40010B2C
B0_P5_ROUTE_HC45: 0x40010B2D
B0_P5_ROUTE_HC46: 0x40010B2E
B0_P5_ROUTE_HC47: 0x40010B2F
B0_P5_ROUTE_HC48: 0x40010B30
B0_P5_ROUTE_HC49: 0x40010B31
B0_P5_ROUTE_HC50: 0x40010B32
B0_P5_ROUTE_HC51: 0x40010B33
B0_P5_ROUTE_HC52: 0x40010B34
B0_P5_ROUTE_HC53: 0x40010B35
B0_P5_ROUTE_HC54: 0x40010B36
B0_P5_ROUTE_HC55: 0x40010B37
B0_P5_ROUTE_HC56: 0x40010B38
B0_P5_ROUTE_HC57: 0x40010B39
B0_P5_ROUTE_HC58: 0x40010B3A
B0_P5_ROUTE_HC59: 0x40010B3B
B0_P5_ROUTE_HC60: 0x40010B3C
B0_P5_ROUTE_HC61: 0x40010B3D
B0_P5_ROUTE_HC62: 0x40010B3E
B0_P5_ROUTE_HC63: 0x40010B3F
B0_P5_ROUTE_HC64: 0x40010B40
B0_P5_ROUTE_HC65: 0x40010B41
B0_P5_ROUTE_HC66: 0x40010B42
B0_P5_ROUTE_HC67: 0x40010B43
B0_P5_ROUTE_HC68: 0x40010B44
B0_P5_ROUTE_HC69: 0x40010B45
B0_P5_ROUTE_HC70: 0x40010B46
B0_P5_ROUTE_HC71: 0x40010B47

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P5_ROUTE_HC72: 0x40010B48
B0_P5_ROUTE_HC73: 0x40010B49
B0_P5_ROUTE_HC74: 0x40010B4A
B0_P5_ROUTE_HC75: 0x40010B4B
B0_P5_ROUTE_HC76: 0x40010B4C
B0_P5_ROUTE_HC77: 0x40010B4D
B0_P5_ROUTE_HC78: 0x40010B4E
B0_P5_ROUTE_HC79: 0x40010B4F
B0_P5_ROUTE_HC80: 0x40010B50
B0_P5_ROUTE_HC81: 0x40010B51
B0_P5_ROUTE_HC82: 0x40010B52
B0_P5_ROUTE_HC83: 0x40010B53
B0_P5_ROUTE_HC84: 0x40010B54
B0_P5_ROUTE_HC85: 0x40010B55
B0_P5_ROUTE_HC86: 0x40010B56
B0_P5_ROUTE_HC87: 0x40010B57
B0_P5_ROUTE_HC88: 0x40010B58
B0_P5_ROUTE_HC89: 0x40010B59
B0_P5_ROUTE_HC90: 0x40010B5A
B0_P5_ROUTE_HC91: 0x40010B5B
B0_P5_ROUTE_HC92: 0x40010B5C
B0_P5_ROUTE_HC93: 0x40010B5D
B0_P5_ROUTE_HC94: 0x40010B5E
B0_P5_ROUTE_HC95: 0x40010B5F
B0_P5_ROUTE_HC96: 0x40010B60
B0_P5_ROUTE_HC97: 0x40010B61
B0_P5_ROUTE_HC98: 0x40010B62
B0_P5_ROUTE_HC99: 0x40010B63
B0_P5_ROUTE_HC100: 0x40010B64
B0_P5_ROUTE_HC101: 0x40010B65
B0_P5_ROUTE_HC102: 0x40010B66
B0_P5_ROUTE_HC103: 0x40010B67
B0_P5_ROUTE_HC104: 0x40010B68
B0_P5_ROUTE_HC105: 0x40010B69
B0_P5_ROUTE_HC106: 0x40010B6A
B0_P5_ROUTE_HC107: 0x40010B6B
B0_P5_ROUTE_HC108: 0x40010B6C
B0_P5_ROUTE_HC109: 0x40010B6D
B0_P5_ROUTE_HC110: 0x40010B6E
B0_P5_ROUTE_HC111: 0x40010B6F
B0_P5_ROUTE_HC112: 0x40010B70
B0_P5_ROUTE_HC113: 0x40010B71
B0_P5_ROUTE_HC114: 0x40010B72
B0_P5_ROUTE_HC115: 0x40010B73
B0_P5_ROUTE_HC116: 0x40010B74
B0_P5_ROUTE_HC117: 0x40010B75
B0_P5_ROUTE_HC118: 0x40010B76
B0_P5_ROUTE_HC119: 0x40010B77
B0_P5_ROUTE_HC120: 0x40010B78
B0_P5_ROUTE_HC121: 0x40010B79
B0_P5_ROUTE_HC122: 0x40010B7A
B0_P5_ROUTE_HC123: 0x40010B7B
B0_P5_ROUTE_HC124: 0x40010B7C
B0_P5_ROUTE_HC125: 0x40010B7D
B0_P5_ROUTE_HC126: 0x40010B7E
B0_P5_ROUTE_HC127: 0x40010B7F
B0_P6_ROUTE_HC0: 0x40010D00
B0_P6_ROUTE_HC1: 0x40010D01
B0_P6_ROUTE_HC2: 0x40010D02
B0_P6_ROUTE_HC3: 0x40010D03
B0_P6_ROUTE_HC4: 0x40010D04
B0_P6_ROUTE_HC5: 0x40010D05
B0_P6_ROUTE_HC6: 0x40010D06
B0_P6_ROUTE_HC7: 0x40010D07
B0_P6_ROUTE_HC8: 0x40010D08
B0_P6_ROUTE_HC9: 0x40010D09
B0_P6_ROUTE_HC10: 0x40010D0A
B0_P6_ROUTE_HC11: 0x40010D0B
B0_P6_ROUTE_HC12: 0x40010D0C
B0_P6_ROUTE_HC13: 0x40010D0D
B0_P6_ROUTE_HC14: 0x40010D0E
B0_P6_ROUTE_HC15: 0x40010D0F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P6_ROUTE_HC16: 0x40010D10
B0_P6_ROUTE_HC17: 0x40010D11
B0_P6_ROUTE_HC18: 0x40010D12
B0_P6_ROUTE_HC19: 0x40010D13
B0_P6_ROUTE_HC20: 0x40010D14
B0_P6_ROUTE_HC21: 0x40010D15
B0_P6_ROUTE_HC22: 0x40010D16
B0_P6_ROUTE_HC23: 0x40010D17
B0_P6_ROUTE_HC24: 0x40010D18
B0_P6_ROUTE_HC25: 0x40010D19
B0_P6_ROUTE_HC26: 0x40010D1A
B0_P6_ROUTE_HC27: 0x40010D1B
B0_P6_ROUTE_HC28: 0x40010D1C
B0_P6_ROUTE_HC29: 0x40010D1D
B0_P6_ROUTE_HC30: 0x40010D1E
B0_P6_ROUTE_HC31: 0x40010D1F
B0_P6_ROUTE_HC32: 0x40010D20
B0_P6_ROUTE_HC33: 0x40010D21
B0_P6_ROUTE_HC34: 0x40010D22
B0_P6_ROUTE_HC35: 0x40010D23
B0_P6_ROUTE_HC36: 0x40010D24
B0_P6_ROUTE_HC37: 0x40010D25
B0_P6_ROUTE_HC38: 0x40010D26
B0_P6_ROUTE_HC39: 0x40010D27
B0_P6_ROUTE_HC40: 0x40010D28
B0_P6_ROUTE_HC41: 0x40010D29
B0_P6_ROUTE_HC42: 0x40010D2A
B0_P6_ROUTE_HC43: 0x40010D2B
B0_P6_ROUTE_HC44: 0x40010D2C
B0_P6_ROUTE_HC45: 0x40010D2D
B0_P6_ROUTE_HC46: 0x40010D2E
B0_P6_ROUTE_HC47: 0x40010D2F
B0_P6_ROUTE_HC48: 0x40010D30
B0_P6_ROUTE_HC49: 0x40010D31
B0_P6_ROUTE_HC50: 0x40010D32
B0_P6_ROUTE_HC51: 0x40010D33
B0_P6_ROUTE_HC52: 0x40010D34
B0_P6_ROUTE_HC53: 0x40010D35
B0_P6_ROUTE_HC54: 0x40010D36
B0_P6_ROUTE_HC55: 0x40010D37
B0_P6_ROUTE_HC56: 0x40010D38
B0_P6_ROUTE_HC57: 0x40010D39
B0_P6_ROUTE_HC58: 0x40010D3A
B0_P6_ROUTE_HC59: 0x40010D3B
B0_P6_ROUTE_HC60: 0x40010D3C
B0_P6_ROUTE_HC61: 0x40010D3D
B0_P6_ROUTE_HC62: 0x40010D3E
B0_P6_ROUTE_HC63: 0x40010D3F
B0_P6_ROUTE_HC64: 0x40010D40
B0_P6_ROUTE_HC65: 0x40010D41
B0_P6_ROUTE_HC66: 0x40010D42
B0_P6_ROUTE_HC67: 0x40010D43
B0_P6_ROUTE_HC68: 0x40010D44
B0_P6_ROUTE_HC69: 0x40010D45
B0_P6_ROUTE_HC70: 0x40010D46
B0_P6_ROUTE_HC71: 0x40010D47
B0_P6_ROUTE_HC72: 0x40010D48
B0_P6_ROUTE_HC73: 0x40010D49
B0_P6_ROUTE_HC74: 0x40010D4A
B0_P6_ROUTE_HC75: 0x40010D4B
B0_P6_ROUTE_HC76: 0x40010D4C
B0_P6_ROUTE_HC77: 0x40010D4D
B0_P6_ROUTE_HC78: 0x40010D4E
B0_P6_ROUTE_HC79: 0x40010D4F
B0_P6_ROUTE_HC80: 0x40010D50
B0_P6_ROUTE_HC81: 0x40010D51
B0_P6_ROUTE_HC82: 0x40010D52
B0_P6_ROUTE_HC83: 0x40010D53
B0_P6_ROUTE_HC84: 0x40010D54
B0_P6_ROUTE_HC85: 0x40010D55
B0_P6_ROUTE_HC86: 0x40010D56
B0_P6_ROUTE_HC87: 0x40010D57

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P6_ROUTE_HC88: 0x40010D58
B0_P6_ROUTE_HC89: 0x40010D59
B0_P6_ROUTE_HC90: 0x40010D5A
B0_P6_ROUTE_HC91: 0x40010D5B
B0_P6_ROUTE_HC92: 0x40010D5C
B0_P6_ROUTE_HC93: 0x40010D5D
B0_P6_ROUTE_HC94: 0x40010D5E
B0_P6_ROUTE_HC95: 0x40010D5F
B0_P6_ROUTE_HC96: 0x40010D60
B0_P6_ROUTE_HC97: 0x40010D61
B0_P6_ROUTE_HC98: 0x40010D62
B0_P6_ROUTE_HC99: 0x40010D63
B0_P6_ROUTE_HC100: 0x40010D64
B0_P6_ROUTE_HC101: 0x40010D65
B0_P6_ROUTE_HC102: 0x40010D66
B0_P6_ROUTE_HC103: 0x40010D67
B0_P6_ROUTE_HC104: 0x40010D68
B0_P6_ROUTE_HC105: 0x40010D69
B0_P6_ROUTE_HC106: 0x40010D6A
B0_P6_ROUTE_HC107: 0x40010D6B
B0_P6_ROUTE_HC108: 0x40010D6C
B0_P6_ROUTE_HC109: 0x40010D6D
B0_P6_ROUTE_HC110: 0x40010D6E
B0_P6_ROUTE_HC111: 0x40010D6F
B0_P6_ROUTE_HC112: 0x40010D70
B0_P6_ROUTE_HC113: 0x40010D71
B0_P6_ROUTE_HC114: 0x40010D72
B0_P6_ROUTE_HC115: 0x40010D73
B0_P6_ROUTE_HC116: 0x40010D74
B0_P6_ROUTE_HC117: 0x40010D75
B0_P6_ROUTE_HC118: 0x40010D76
B0_P6_ROUTE_HC119: 0x40010D77
B0_P6_ROUTE_HC120: 0x40010D78
B0_P6_ROUTE_HC121: 0x40010D79
B0_P6_ROUTE_HC122: 0x40010D7A
B0_P6_ROUTE_HC123: 0x40010D7B
B0_P6_ROUTE_HC124: 0x40010D7C
B0_P6_ROUTE_HC125: 0x40010D7D
B0_P6_ROUTE_HC126: 0x40010D7E
B0_P6_ROUTE_HC127: 0x40010D7F
B0_P7_ROUTE_HC0: 0x40010F00
B0_P7_ROUTE_HC1: 0x40010F01
B0_P7_ROUTE_HC2: 0x40010F02
B0_P7_ROUTE_HC3: 0x40010F03
B0_P7_ROUTE_HC4: 0x40010F04
B0_P7_ROUTE_HC5: 0x40010F05
B0_P7_ROUTE_HC6: 0x40010F06
B0_P7_ROUTE_HC7: 0x40010F07
B0_P7_ROUTE_HC8: 0x40010F08
B0_P7_ROUTE_HC9: 0x40010F09
B0_P7_ROUTE_HC10: 0x40010F0A
B0_P7_ROUTE_HC11: 0x40010F0B
B0_P7_ROUTE_HC12: 0x40010F0C
B0_P7_ROUTE_HC13: 0x40010F0D
B0_P7_ROUTE_HC14: 0x40010F0E
B0_P7_ROUTE_HC15: 0x40010F0F
B0_P7_ROUTE_HC16: 0x40010F10
B0_P7_ROUTE_HC17: 0x40010F11
B0_P7_ROUTE_HC18: 0x40010F12
B0_P7_ROUTE_HC19: 0x40010F13
B0_P7_ROUTE_HC20: 0x40010F14
B0_P7_ROUTE_HC21: 0x40010F15
B0_P7_ROUTE_HC22: 0x40010F16
B0_P7_ROUTE_HC23: 0x40010F17
B0_P7_ROUTE_HC24: 0x40010F18
B0_P7_ROUTE_HC25: 0x40010F19
B0_P7_ROUTE_HC26: 0x40010F1A
B0_P7_ROUTE_HC27: 0x40010F1B
B0_P7_ROUTE_HC28: 0x40010F1C
B0_P7_ROUTE_HC29: 0x40010F1D
B0_P7_ROUTE_HC30: 0x40010F1E
B0_P7_ROUTE_HC31: 0x40010F1F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P7_ROUTE_HC32: 0x40010F20
B0_P7_ROUTE_HC33: 0x40010F21
B0_P7_ROUTE_HC34: 0x40010F22
B0_P7_ROUTE_HC35: 0x40010F23
B0_P7_ROUTE_HC36: 0x40010F24
B0_P7_ROUTE_HC37: 0x40010F25
B0_P7_ROUTE_HC38: 0x40010F26
B0_P7_ROUTE_HC39: 0x40010F27
B0_P7_ROUTE_HC40: 0x40010F28
B0_P7_ROUTE_HC41: 0x40010F29
B0_P7_ROUTE_HC42: 0x40010F2A
B0_P7_ROUTE_HC43: 0x40010F2B
B0_P7_ROUTE_HC44: 0x40010F2C
B0_P7_ROUTE_HC45: 0x40010F2D
B0_P7_ROUTE_HC46: 0x40010F2E
B0_P7_ROUTE_HC47: 0x40010F2F
B0_P7_ROUTE_HC48: 0x40010F30
B0_P7_ROUTE_HC49: 0x40010F31
B0_P7_ROUTE_HC50: 0x40010F32
B0_P7_ROUTE_HC51: 0x40010F33
B0_P7_ROUTE_HC52: 0x40010F34
B0_P7_ROUTE_HC53: 0x40010F35
B0_P7_ROUTE_HC54: 0x40010F36
B0_P7_ROUTE_HC55: 0x40010F37
B0_P7_ROUTE_HC56: 0x40010F38
B0_P7_ROUTE_HC57: 0x40010F39
B0_P7_ROUTE_HC58: 0x40010F3A
B0_P7_ROUTE_HC59: 0x40010F3B
B0_P7_ROUTE_HC60: 0x40010F3C
B0_P7_ROUTE_HC61: 0x40010F3D
B0_P7_ROUTE_HC62: 0x40010F3E
B0_P7_ROUTE_HC63: 0x40010F3F
B0_P7_ROUTE_HC64: 0x40010F40
B0_P7_ROUTE_HC65: 0x40010F41
B0_P7_ROUTE_HC66: 0x40010F42
B0_P7_ROUTE_HC67: 0x40010F43
B0_P7_ROUTE_HC68: 0x40010F44
B0_P7_ROUTE_HC69: 0x40010F45
B0_P7_ROUTE_HC70: 0x40010F46
B0_P7_ROUTE_HC71: 0x40010F47
B0_P7_ROUTE_HC72: 0x40010F48
B0_P7_ROUTE_HC73: 0x40010F49
B0_P7_ROUTE_HC74: 0x40010F4A
B0_P7_ROUTE_HC75: 0x40010F4B
B0_P7_ROUTE_HC76: 0x40010F4C
B0_P7_ROUTE_HC77: 0x40010F4D
B0_P7_ROUTE_HC78: 0x40010F4E
B0_P7_ROUTE_HC79: 0x40010F4F
B0_P7_ROUTE_HC80: 0x40010F50
B0_P7_ROUTE_HC81: 0x40010F51
B0_P7_ROUTE_HC82: 0x40010F52
B0_P7_ROUTE_HC83: 0x40010F53
B0_P7_ROUTE_HC84: 0x40010F54
B0_P7_ROUTE_HC85: 0x40010F55
B0_P7_ROUTE_HC86: 0x40010F56
B0_P7_ROUTE_HC87: 0x40010F57
B0_P7_ROUTE_HC88: 0x40010F58
B0_P7_ROUTE_HC89: 0x40010F59
B0_P7_ROUTE_HC90: 0x40010F5A
B0_P7_ROUTE_HC91: 0x40010F5B
B0_P7_ROUTE_HC92: 0x40010F5C
B0_P7_ROUTE_HC93: 0x40010F5D
B0_P7_ROUTE_HC94: 0x40010F5E
B0_P7_ROUTE_HC95: 0x40010F5F
B0_P7_ROUTE_HC96: 0x40010F60
B0_P7_ROUTE_HC97: 0x40010F61
B0_P7_ROUTE_HC98: 0x40010F62
B0_P7_ROUTE_HC99: 0x40010F63
B0_P7_ROUTE_HC100: 0x40010F64
B0_P7_ROUTE_HC101: 0x40010F65
B0_P7_ROUTE_HC102: 0x40010F66
B0_P7_ROUTE_HC103: 0x40010F67

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B0_P7_ROUTE_HC104: 0x40010F68
B0_P7_ROUTE_HC105: 0x40010F69
B0_P7_ROUTE_HC106: 0x40010F6A
B0_P7_ROUTE_HC107: 0x40010F6B
B0_P7_ROUTE_HC108: 0x40010F6C
B0_P7_ROUTE_HC109: 0x40010F6D
B0_P7_ROUTE_HC110: 0x40010F6E
B0_P7_ROUTE_HC111: 0x40010F6F
B0_P7_ROUTE_HC112: 0x40010F70
B0_P7_ROUTE_HC113: 0x40010F71
B0_P7_ROUTE_HC114: 0x40010F72
B0_P7_ROUTE_HC115: 0x40010F73
B0_P7_ROUTE_HC116: 0x40010F74
B0_P7_ROUTE_HC117: 0x40010F75
B0_P7_ROUTE_HC118: 0x40010F76
B0_P7_ROUTE_HC119: 0x40010F77
B0_P7_ROUTE_HC120: 0x40010F78
B0_P7_ROUTE_HC121: 0x40010F79
B0_P7_ROUTE_HC122: 0x40010F7A
B0_P7_ROUTE_HC123: 0x40010F7B
B0_P7_ROUTE_HC124: 0x40010F7C
B0_P7_ROUTE_HC125: 0x40010F7D
B0_P7_ROUTE_HC126: 0x40010F7E
B0_P7_ROUTE_HC127: 0x40010F7F
B1_P2_ROUTE_HC0: 0x40011500
B1_P2_ROUTE_HC1: 0x40011501
B1_P2_ROUTE_HC2: 0x40011502
B1_P2_ROUTE_HC3: 0x40011503
B1_P2_ROUTE_HC4: 0x40011504
B1_P2_ROUTE_HC5: 0x40011505
B1_P2_ROUTE_HC6: 0x40011506
B1_P2_ROUTE_HC7: 0x40011507
B1_P2_ROUTE_HC8: 0x40011508
B1_P2_ROUTE_HC9: 0x40011509
B1_P2_ROUTE_HC10: 0x4001150A
B1_P2_ROUTE_HC11: 0x4001150B
B1_P2_ROUTE_HC12: 0x4001150C
B1_P2_ROUTE_HC13: 0x4001150D
B1_P2_ROUTE_HC14: 0x4001150E
B1_P2_ROUTE_HC15: 0x4001150F
B1_P2_ROUTE_HC16: 0x40011510
B1_P2_ROUTE_HC17: 0x40011511
B1_P2_ROUTE_HC18: 0x40011512
B1_P2_ROUTE_HC19: 0x40011513
B1_P2_ROUTE_HC20: 0x40011514
B1_P2_ROUTE_HC21: 0x40011515
B1_P2_ROUTE_HC22: 0x40011516
B1_P2_ROUTE_HC23: 0x40011517
B1_P2_ROUTE_HC24: 0x40011518
B1_P2_ROUTE_HC25: 0x40011519
B1_P2_ROUTE_HC26: 0x4001151A
B1_P2_ROUTE_HC27: 0x4001151B
B1_P2_ROUTE_HC28: 0x4001151C
B1_P2_ROUTE_HC29: 0x4001151D
B1_P2_ROUTE_HC30: 0x4001151E
B1_P2_ROUTE_HC31: 0x4001151F
B1_P2_ROUTE_HC32: 0x40011520
B1_P2_ROUTE_HC33: 0x40011521
B1_P2_ROUTE_HC34: 0x40011522
B1_P2_ROUTE_HC35: 0x40011523
B1_P2_ROUTE_HC36: 0x40011524
B1_P2_ROUTE_HC37: 0x40011525
B1_P2_ROUTE_HC38: 0x40011526
B1_P2_ROUTE_HC39: 0x40011527
B1_P2_ROUTE_HC40: 0x40011528
B1_P2_ROUTE_HC41: 0x40011529
B1_P2_ROUTE_HC42: 0x4001152A
B1_P2_ROUTE_HC43: 0x4001152B
B1_P2_ROUTE_HC44: 0x4001152C
B1_P2_ROUTE_HC45: 0x4001152D
B1_P2_ROUTE_HC46: 0x4001152E
B1_P2_ROUTE_HC47: 0x4001152F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B1_P2_ROUTE_HC48: 0x40011530
B1_P2_ROUTE_HC49: 0x40011531
B1_P2_ROUTE_HC50: 0x40011532
B1_P2_ROUTE_HC51: 0x40011533
B1_P2_ROUTE_HC52: 0x40011534
B1_P2_ROUTE_HC53: 0x40011535
B1_P2_ROUTE_HC54: 0x40011536
B1_P2_ROUTE_HC55: 0x40011537
B1_P2_ROUTE_HC56: 0x40011538
B1_P2_ROUTE_HC57: 0x40011539
B1_P2_ROUTE_HC58: 0x4001153A
B1_P2_ROUTE_HC59: 0x4001153B
B1_P2_ROUTE_HC60: 0x4001153C
B1_P2_ROUTE_HC61: 0x4001153D
B1_P2_ROUTE_HC62: 0x4001153E
B1_P2_ROUTE_HC63: 0x4001153F
B1_P2_ROUTE_HC64: 0x40011540
B1_P2_ROUTE_HC65: 0x40011541
B1_P2_ROUTE_HC66: 0x40011542
B1_P2_ROUTE_HC67: 0x40011543
B1_P2_ROUTE_HC68: 0x40011544
B1_P2_ROUTE_HC69: 0x40011545
B1_P2_ROUTE_HC70: 0x40011546
B1_P2_ROUTE_HC71: 0x40011547
B1_P2_ROUTE_HC72: 0x40011548
B1_P2_ROUTE_HC73: 0x40011549
B1_P2_ROUTE_HC74: 0x4001154A
B1_P2_ROUTE_HC75: 0x4001154B
B1_P2_ROUTE_HC76: 0x4001154C
B1_P2_ROUTE_HC77: 0x4001154D
B1_P2_ROUTE_HC78: 0x4001154E
B1_P2_ROUTE_HC79: 0x4001154F
B1_P2_ROUTE_HC80: 0x40011550
B1_P2_ROUTE_HC81: 0x40011551
B1_P2_ROUTE_HC82: 0x40011552
B1_P2_ROUTE_HC83: 0x40011553
B1_P2_ROUTE_HC84: 0x40011554
B1_P2_ROUTE_HC85: 0x40011555
B1_P2_ROUTE_HC86: 0x40011556
B1_P2_ROUTE_HC87: 0x40011557
B1_P2_ROUTE_HC88: 0x40011558
B1_P2_ROUTE_HC89: 0x40011559
B1_P2_ROUTE_HC90: 0x4001155A
B1_P2_ROUTE_HC91: 0x4001155B
B1_P2_ROUTE_HC92: 0x4001155C
B1_P2_ROUTE_HC93: 0x4001155D
B1_P2_ROUTE_HC94: 0x4001155E
B1_P2_ROUTE_HC95: 0x4001155F
B1_P2_ROUTE_HC96: 0x40011560
B1_P2_ROUTE_HC97: 0x40011561
B1_P2_ROUTE_HC98: 0x40011562
B1_P2_ROUTE_HC99: 0x40011563
B1_P2_ROUTE_HC100: 0x40011564
B1_P2_ROUTE_HC101: 0x40011565
B1_P2_ROUTE_HC102: 0x40011566
B1_P2_ROUTE_HC103: 0x40011567
B1_P2_ROUTE_HC104: 0x40011568
B1_P2_ROUTE_HC105: 0x40011569
B1_P2_ROUTE_HC106: 0x4001156A
B1_P2_ROUTE_HC107: 0x4001156B
B1_P2_ROUTE_HC108: 0x4001156C
B1_P2_ROUTE_HC109: 0x4001156D
B1_P2_ROUTE_HC110: 0x4001156E
B1_P2_ROUTE_HC111: 0x4001156F
B1_P2_ROUTE_HC112: 0x40011570
B1_P2_ROUTE_HC113: 0x40011571
B1_P2_ROUTE_HC114: 0x40011572
B1_P2_ROUTE_HC115: 0x40011573
B1_P2_ROUTE_HC116: 0x40011574
B1_P2_ROUTE_HC117: 0x40011575
B1_P2_ROUTE_HC118: 0x40011576
B1_P2_ROUTE_HC119: 0x40011577

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B1_P2_ROUTE_HC120: 0x40011578
B1_P2_ROUTE_HC121: 0x40011579
B1_P2_ROUTE_HC122: 0x4001157A
B1_P2_ROUTE_HC123: 0x4001157B
B1_P2_ROUTE_HC124: 0x4001157C
B1_P2_ROUTE_HC125: 0x4001157D
B1_P2_ROUTE_HC126: 0x4001157E
B1_P2_ROUTE_HC127: 0x4001157F
B1_P3_ROUTE_HC0: 0x40011700
B1_P3_ROUTE_HC1: 0x40011701
B1_P3_ROUTE_HC2: 0x40011702
B1_P3_ROUTE_HC3: 0x40011703
B1_P3_ROUTE_HC4: 0x40011704
B1_P3_ROUTE_HC5: 0x40011705
B1_P3_ROUTE_HC6: 0x40011706
B1_P3_ROUTE_HC7: 0x40011707
B1_P3_ROUTE_HC8: 0x40011708
B1_P3_ROUTE_HC9: 0x40011709
B1_P3_ROUTE_HC10: 0x4001170A
B1_P3_ROUTE_HC11: 0x4001170B
B1_P3_ROUTE_HC12: 0x4001170C
B1_P3_ROUTE_HC13: 0x4001170D
B1_P3_ROUTE_HC14: 0x4001170E
B1_P3_ROUTE_HC15: 0x4001170F
B1_P3_ROUTE_HC16: 0x40011710
B1_P3_ROUTE_HC17: 0x40011711
B1_P3_ROUTE_HC18: 0x40011712
B1_P3_ROUTE_HC19: 0x40011713
B1_P3_ROUTE_HC20: 0x40011714
B1_P3_ROUTE_HC21: 0x40011715
B1_P3_ROUTE_HC22: 0x40011716
B1_P3_ROUTE_HC23: 0x40011717
B1_P3_ROUTE_HC24: 0x40011718
B1_P3_ROUTE_HC25: 0x40011719
B1_P3_ROUTE_HC26: 0x4001171A
B1_P3_ROUTE_HC27: 0x4001171B
B1_P3_ROUTE_HC28: 0x4001171C
B1_P3_ROUTE_HC29: 0x4001171D
B1_P3_ROUTE_HC30: 0x4001171E
B1_P3_ROUTE_HC31: 0x4001171F
B1_P3_ROUTE_HC32: 0x40011720
B1_P3_ROUTE_HC33: 0x40011721
B1_P3_ROUTE_HC34: 0x40011722
B1_P3_ROUTE_HC35: 0x40011723
B1_P3_ROUTE_HC36: 0x40011724
B1_P3_ROUTE_HC37: 0x40011725
B1_P3_ROUTE_HC38: 0x40011726
B1_P3_ROUTE_HC39: 0x40011727
B1_P3_ROUTE_HC40: 0x40011728
B1_P3_ROUTE_HC41: 0x40011729
B1_P3_ROUTE_HC42: 0x4001172A
B1_P3_ROUTE_HC43: 0x4001172B
B1_P3_ROUTE_HC44: 0x4001172C
B1_P3_ROUTE_HC45: 0x4001172D
B1_P3_ROUTE_HC46: 0x4001172E
B1_P3_ROUTE_HC47: 0x4001172F
B1_P3_ROUTE_HC48: 0x40011730
B1_P3_ROUTE_HC49: 0x40011731
B1_P3_ROUTE_HC50: 0x40011732
B1_P3_ROUTE_HC51: 0x40011733
B1_P3_ROUTE_HC52: 0x40011734
B1_P3_ROUTE_HC53: 0x40011735
B1_P3_ROUTE_HC54: 0x40011736
B1_P3_ROUTE_HC55: 0x40011737
B1_P3_ROUTE_HC56: 0x40011738
B1_P3_ROUTE_HC57: 0x40011739
B1_P3_ROUTE_HC58: 0x4001173A
B1_P3_ROUTE_HC59: 0x4001173B
B1_P3_ROUTE_HC60: 0x4001173C
B1_P3_ROUTE_HC61: 0x4001173D
B1_P3_ROUTE_HC62: 0x4001173E
B1_P3_ROUTE_HC63: 0x4001173F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B1_P3_ROUTE_HC64: 0x40011740
B1_P3_ROUTE_HC65: 0x40011741
B1_P3_ROUTE_HC66: 0x40011742
B1_P3_ROUTE_HC67: 0x40011743
B1_P3_ROUTE_HC68: 0x40011744
B1_P3_ROUTE_HC69: 0x40011745
B1_P3_ROUTE_HC70: 0x40011746
B1_P3_ROUTE_HC71: 0x40011747
B1_P3_ROUTE_HC72: 0x40011748
B1_P3_ROUTE_HC73: 0x40011749
B1_P3_ROUTE_HC74: 0x4001174A
B1_P3_ROUTE_HC75: 0x4001174B
B1_P3_ROUTE_HC76: 0x4001174C
B1_P3_ROUTE_HC77: 0x4001174D
B1_P3_ROUTE_HC78: 0x4001174E
B1_P3_ROUTE_HC79: 0x4001174F
B1_P3_ROUTE_HC80: 0x40011750
B1_P3_ROUTE_HC81: 0x40011751
B1_P3_ROUTE_HC82: 0x40011752
B1_P3_ROUTE_HC83: 0x40011753
B1_P3_ROUTE_HC84: 0x40011754
B1_P3_ROUTE_HC85: 0x40011755
B1_P3_ROUTE_HC86: 0x40011756
B1_P3_ROUTE_HC87: 0x40011757
B1_P3_ROUTE_HC88: 0x40011758
B1_P3_ROUTE_HC89: 0x40011759
B1_P3_ROUTE_HC90: 0x4001175A
B1_P3_ROUTE_HC91: 0x4001175B
B1_P3_ROUTE_HC92: 0x4001175C
B1_P3_ROUTE_HC93: 0x4001175D
B1_P3_ROUTE_HC94: 0x4001175E
B1_P3_ROUTE_HC95: 0x4001175F
B1_P3_ROUTE_HC96: 0x40011760
B1_P3_ROUTE_HC97: 0x40011761
B1_P3_ROUTE_HC98: 0x40011762
B1_P3_ROUTE_HC99: 0x40011763
B1_P3_ROUTE_HC100: 0x40011764
B1_P3_ROUTE_HC101: 0x40011765
B1_P3_ROUTE_HC102: 0x40011766
B1_P3_ROUTE_HC103: 0x40011767
B1_P3_ROUTE_HC104: 0x40011768
B1_P3_ROUTE_HC105: 0x40011769
B1_P3_ROUTE_HC106: 0x4001176A
B1_P3_ROUTE_HC107: 0x4001176B
B1_P3_ROUTE_HC108: 0x4001176C
B1_P3_ROUTE_HC109: 0x4001176D
B1_P3_ROUTE_HC110: 0x4001176E
B1_P3_ROUTE_HC111: 0x4001176F
B1_P3_ROUTE_HC112: 0x40011770
B1_P3_ROUTE_HC113: 0x40011771
B1_P3_ROUTE_HC114: 0x40011772
B1_P3_ROUTE_HC115: 0x40011773
B1_P3_ROUTE_HC116: 0x40011774
B1_P3_ROUTE_HC117: 0x40011775
B1_P3_ROUTE_HC118: 0x40011776
B1_P3_ROUTE_HC119: 0x40011777
B1_P3_ROUTE_HC120: 0x40011778
B1_P3_ROUTE_HC121: 0x40011779
B1_P3_ROUTE_HC122: 0x4001177A
B1_P3_ROUTE_HC123: 0x4001177B
B1_P3_ROUTE_HC124: 0x4001177C
B1_P3_ROUTE_HC125: 0x4001177D
B1_P3_ROUTE_HC126: 0x4001177E
B1_P3_ROUTE_HC127: 0x4001177F
B1_P4_ROUTE_HC0: 0x40011900
B1_P4_ROUTE_HC1: 0x40011901
B1_P4_ROUTE_HC2: 0x40011902
B1_P4_ROUTE_HC3: 0x40011903
B1_P4_ROUTE_HC4: 0x40011904
B1_P4_ROUTE_HC5: 0x40011905
B1_P4_ROUTE_HC6: 0x40011906
B1_P4_ROUTE_HC7: 0x40011907

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B1_P4_ROUTE_HC8: 0x40011908
B1_P4_ROUTE_HC9: 0x40011909
B1_P4_ROUTE_HC10: 0x4001190A
B1_P4_ROUTE_HC11: 0x4001190B
B1_P4_ROUTE_HC12: 0x4001190C
B1_P4_ROUTE_HC13: 0x4001190D
B1_P4_ROUTE_HC14: 0x4001190E
B1_P4_ROUTE_HC15: 0x4001190F
B1_P4_ROUTE_HC16: 0x40011910
B1_P4_ROUTE_HC17: 0x40011911
B1_P4_ROUTE_HC18: 0x40011912
B1_P4_ROUTE_HC19: 0x40011913
B1_P4_ROUTE_HC20: 0x40011914
B1_P4_ROUTE_HC21: 0x40011915
B1_P4_ROUTE_HC22: 0x40011916
B1_P4_ROUTE_HC23: 0x40011917
B1_P4_ROUTE_HC24: 0x40011918
B1_P4_ROUTE_HC25: 0x40011919
B1_P4_ROUTE_HC26: 0x4001191A
B1_P4_ROUTE_HC27: 0x4001191B
B1_P4_ROUTE_HC28: 0x4001191C
B1_P4_ROUTE_HC29: 0x4001191D
B1_P4_ROUTE_HC30: 0x4001191E
B1_P4_ROUTE_HC31: 0x4001191F
B1_P4_ROUTE_HC32: 0x40011920
B1_P4_ROUTE_HC33: 0x40011921
B1_P4_ROUTE_HC34: 0x40011922
B1_P4_ROUTE_HC35: 0x40011923
B1_P4_ROUTE_HC36: 0x40011924
B1_P4_ROUTE_HC37: 0x40011925
B1_P4_ROUTE_HC38: 0x40011926
B1_P4_ROUTE_HC39: 0x40011927
B1_P4_ROUTE_HC40: 0x40011928
B1_P4_ROUTE_HC41: 0x40011929
B1_P4_ROUTE_HC42: 0x4001192A
B1_P4_ROUTE_HC43: 0x4001192B
B1_P4_ROUTE_HC44: 0x4001192C
B1_P4_ROUTE_HC45: 0x4001192D
B1_P4_ROUTE_HC46: 0x4001192E
B1_P4_ROUTE_HC47: 0x4001192F
B1_P4_ROUTE_HC48: 0x40011930
B1_P4_ROUTE_HC49: 0x40011931
B1_P4_ROUTE_HC50: 0x40011932
B1_P4_ROUTE_HC51: 0x40011933
B1_P4_ROUTE_HC52: 0x40011934
B1_P4_ROUTE_HC53: 0x40011935
B1_P4_ROUTE_HC54: 0x40011936
B1_P4_ROUTE_HC55: 0x40011937
B1_P4_ROUTE_HC56: 0x40011938
B1_P4_ROUTE_HC57: 0x40011939
B1_P4_ROUTE_HC58: 0x4001193A
B1_P4_ROUTE_HC59: 0x4001193B
B1_P4_ROUTE_HC60: 0x4001193C
B1_P4_ROUTE_HC61: 0x4001193D
B1_P4_ROUTE_HC62: 0x4001193E
B1_P4_ROUTE_HC63: 0x4001193F
B1_P4_ROUTE_HC64: 0x40011940
B1_P4_ROUTE_HC65: 0x40011941
B1_P4_ROUTE_HC66: 0x40011942
B1_P4_ROUTE_HC67: 0x40011943
B1_P4_ROUTE_HC68: 0x40011944
B1_P4_ROUTE_HC69: 0x40011945
B1_P4_ROUTE_HC70: 0x40011946
B1_P4_ROUTE_HC71: 0x40011947
B1_P4_ROUTE_HC72: 0x40011948
B1_P4_ROUTE_HC73: 0x40011949
B1_P4_ROUTE_HC74: 0x4001194A
B1_P4_ROUTE_HC75: 0x4001194B
B1_P4_ROUTE_HC76: 0x4001194C
B1_P4_ROUTE_HC77: 0x4001194D
B1_P4_ROUTE_HC78: 0x4001194E
B1_P4_ROUTE_HC79: 0x4001194F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B1_P4_ROUTE_HC80: 0x40011950
B1_P4_ROUTE_HC81: 0x40011951
B1_P4_ROUTE_HC82: 0x40011952
B1_P4_ROUTE_HC83: 0x40011953
B1_P4_ROUTE_HC84: 0x40011954
B1_P4_ROUTE_HC85: 0x40011955
B1_P4_ROUTE_HC86: 0x40011956
B1_P4_ROUTE_HC87: 0x40011957
B1_P4_ROUTE_HC88: 0x40011958
B1_P4_ROUTE_HC89: 0x40011959
B1_P4_ROUTE_HC90: 0x4001195A
B1_P4_ROUTE_HC91: 0x4001195B
B1_P4_ROUTE_HC92: 0x4001195C
B1_P4_ROUTE_HC93: 0x4001195D
B1_P4_ROUTE_HC94: 0x4001195E
B1_P4_ROUTE_HC95: 0x4001195F
B1_P4_ROUTE_HC96: 0x40011960
B1_P4_ROUTE_HC97: 0x40011961
B1_P4_ROUTE_HC98: 0x40011962
B1_P4_ROUTE_HC99: 0x40011963
B1_P4_ROUTE_HC100: 0x40011964
B1_P4_ROUTE_HC101: 0x40011965
B1_P4_ROUTE_HC102: 0x40011966
B1_P4_ROUTE_HC103: 0x40011967
B1_P4_ROUTE_HC104: 0x40011968
B1_P4_ROUTE_HC105: 0x40011969
B1_P4_ROUTE_HC106: 0x4001196A
B1_P4_ROUTE_HC107: 0x4001196B
B1_P4_ROUTE_HC108: 0x4001196C
B1_P4_ROUTE_HC109: 0x4001196D
B1_P4_ROUTE_HC110: 0x4001196E
B1_P4_ROUTE_HC111: 0x4001196F
B1_P4_ROUTE_HC112: 0x40011970
B1_P4_ROUTE_HC113: 0x40011971
B1_P4_ROUTE_HC114: 0x40011972
B1_P4_ROUTE_HC115: 0x40011973
B1_P4_ROUTE_HC116: 0x40011974
B1_P4_ROUTE_HC117: 0x40011975
B1_P4_ROUTE_HC118: 0x40011976
B1_P4_ROUTE_HC119: 0x40011977
B1_P4_ROUTE_HC120: 0x40011978
B1_P4_ROUTE_HC121: 0x40011979
B1_P4_ROUTE_HC122: 0x4001197A
B1_P4_ROUTE_HC123: 0x4001197B
B1_P4_ROUTE_HC124: 0x4001197C
B1_P4_ROUTE_HC125: 0x4001197D
B1_P4_ROUTE_HC126: 0x4001197E
B1_P4_ROUTE_HC127: 0x4001197F
B1_P5_ROUTE_HC0: 0x40011B00
B1_P5_ROUTE_HC1: 0x40011B01
B1_P5_ROUTE_HC2: 0x40011B02
B1_P5_ROUTE_HC3: 0x40011B03
B1_P5_ROUTE_HC4: 0x40011B04
B1_P5_ROUTE_HC5: 0x40011B05
B1_P5_ROUTE_HC6: 0x40011B06
B1_P5_ROUTE_HC7: 0x40011B07
B1_P5_ROUTE_HC8: 0x40011B08
B1_P5_ROUTE_HC9: 0x40011B09
B1_P5_ROUTE_HC10: 0x40011B0A
B1_P5_ROUTE_HC11: 0x40011B0B
B1_P5_ROUTE_HC12: 0x40011B0C
B1_P5_ROUTE_HC13: 0x40011B0D
B1_P5_ROUTE_HC14: 0x40011B0E
B1_P5_ROUTE_HC15: 0x40011B0F
B1_P5_ROUTE_HC16: 0x40011B10
B1_P5_ROUTE_HC17: 0x40011B11
B1_P5_ROUTE_HC18: 0x40011B12
B1_P5_ROUTE_HC19: 0x40011B13
B1_P5_ROUTE_HC20: 0x40011B14
B1_P5_ROUTE_HC21: 0x40011B15
B1_P5_ROUTE_HC22: 0x40011B16
B1_P5_ROUTE_HC23: 0x40011B17

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B1_P5_ROUTE_HC24: 0x40011B18
B1_P5_ROUTE_HC25: 0x40011B19
B1_P5_ROUTE_HC26: 0x40011B1A
B1_P5_ROUTE_HC27: 0x40011B1B
B1_P5_ROUTE_HC28: 0x40011B1C
B1_P5_ROUTE_HC29: 0x40011B1D
B1_P5_ROUTE_HC30: 0x40011B1E
B1_P5_ROUTE_HC31: 0x40011B1F
B1_P5_ROUTE_HC32: 0x40011B20
B1_P5_ROUTE_HC33: 0x40011B21
B1_P5_ROUTE_HC34: 0x40011B22
B1_P5_ROUTE_HC35: 0x40011B23
B1_P5_ROUTE_HC36: 0x40011B24
B1_P5_ROUTE_HC37: 0x40011B25
B1_P5_ROUTE_HC38: 0x40011B26
B1_P5_ROUTE_HC39: 0x40011B27
B1_P5_ROUTE_HC40: 0x40011B28
B1_P5_ROUTE_HC41: 0x40011B29
B1_P5_ROUTE_HC42: 0x40011B2A
B1_P5_ROUTE_HC43: 0x40011B2B
B1_P5_ROUTE_HC44: 0x40011B2C
B1_P5_ROUTE_HC45: 0x40011B2D
B1_P5_ROUTE_HC46: 0x40011B2E
B1_P5_ROUTE_HC47: 0x40011B2F
B1_P5_ROUTE_HC48: 0x40011B30
B1_P5_ROUTE_HC49: 0x40011B31
B1_P5_ROUTE_HC50: 0x40011B32
B1_P5_ROUTE_HC51: 0x40011B33
B1_P5_ROUTE_HC52: 0x40011B34
B1_P5_ROUTE_HC53: 0x40011B35
B1_P5_ROUTE_HC54: 0x40011B36
B1_P5_ROUTE_HC55: 0x40011B37
B1_P5_ROUTE_HC56: 0x40011B38
B1_P5_ROUTE_HC57: 0x40011B39
B1_P5_ROUTE_HC58: 0x40011B3A
B1_P5_ROUTE_HC59: 0x40011B3B
B1_P5_ROUTE_HC60: 0x40011B3C
B1_P5_ROUTE_HC61: 0x40011B3D
B1_P5_ROUTE_HC62: 0x40011B3E
B1_P5_ROUTE_HC63: 0x40011B3F
B1_P5_ROUTE_HC64: 0x40011B40
B1_P5_ROUTE_HC65: 0x40011B41
B1_P5_ROUTE_HC66: 0x40011B42
B1_P5_ROUTE_HC67: 0x40011B43
B1_P5_ROUTE_HC68: 0x40011B44
B1_P5_ROUTE_HC69: 0x40011B45
B1_P5_ROUTE_HC70: 0x40011B46
B1_P5_ROUTE_HC71: 0x40011B47
B1_P5_ROUTE_HC72: 0x40011B48
B1_P5_ROUTE_HC73: 0x40011B49
B1_P5_ROUTE_HC74: 0x40011B4A
B1_P5_ROUTE_HC75: 0x40011B4B
B1_P5_ROUTE_HC76: 0x40011B4C
B1_P5_ROUTE_HC77: 0x40011B4D
B1_P5_ROUTE_HC78: 0x40011B4E
B1_P5_ROUTE_HC79: 0x40011B4F
B1_P5_ROUTE_HC80: 0x40011B50
B1_P5_ROUTE_HC81: 0x40011B51
B1_P5_ROUTE_HC82: 0x40011B52
B1_P5_ROUTE_HC83: 0x40011B53
B1_P5_ROUTE_HC84: 0x40011B54
B1_P5_ROUTE_HC85: 0x40011B55
B1_P5_ROUTE_HC86: 0x40011B56
B1_P5_ROUTE_HC87: 0x40011B57
B1_P5_ROUTE_HC88: 0x40011B58
B1_P5_ROUTE_HC89: 0x40011B59
B1_P5_ROUTE_HC90: 0x40011B5A
B1_P5_ROUTE_HC91: 0x40011B5B
B1_P5_ROUTE_HC92: 0x40011B5C
B1_P5_ROUTE_HC93: 0x40011B5D
B1_P5_ROUTE_HC94: 0x40011B5E
B1_P5_ROUTE_HC95: 0x40011B5F

1.3.1164 B[0..3]_P[0..7]_ROUTE_HC[0..127] (continued)

Register : Address

B1_P5_ROUTE_HC96: 0x40011B60
B1_P5_ROUTE_HC97: 0x40011B61
B1_P5_ROUTE_HC98: 0x40011B62
B1_P5_ROUTE_HC99: 0x40011B63
B1_P5_ROUTE_HC100: 0x40011B64
B1_P5_ROUTE_HC101: 0x40011B65
B1_P5_ROUTE_HC102: 0x40011B66
B1_P5_ROUTE_HC103: 0x40011B67
B1_P5_ROUTE_HC104: 0x40011B68
B1_P5_ROUTE_HC105: 0x40011B69
B1_P5_ROUTE_HC106: 0x40011B6A
B1_P5_ROUTE_HC107: 0x40011B6B
B1_P5_ROUTE_HC108: 0x40011B6C
B1_P5_ROUTE_HC109: 0x40011B6D
B1_P5_ROUTE_HC110: 0x40011B6E
B1_P5_ROUTE_HC111: 0x40011B6F
B1_P5_ROUTE_HC112: 0x40011B70
B1_P5_ROUTE_HC113: 0x40011B71
B1_P5_ROUTE_HC114: 0x40011B72
B1_P5_ROUTE_HC115: 0x40011B73
B1_P5_ROUTE_HC116: 0x40011B74
B1_P5_ROUTE_HC117: 0x40011B75
B1_P5_ROUTE_HC118: 0x40011B76
B1_P5_ROUTE_HC119: 0x40011B77
B1_P5_ROUTE_HC120: 0x40011B78
B1_P5_ROUTE_HC121: 0x40011B79
B1_P5_ROUTE_HC122: 0x40011B7A
B1_P5_ROUTE_HC123: 0x40011B7B
B1_P5_ROUTE_HC124: 0x40011B7C
B1_P5_ROUTE_HC125: 0x40011B7D
B1_P5_ROUTE_HC126: 0x40011B7E
B1_P5_ROUTE_HC127: 0x40011B7F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	hc_byte							

UDB Channel HC Tile Configuration

Bits	Name	Description
7:0	hc_byte[7:0]	RAM configuration bytes for channel

1.3.1165 B[0..3]_P[0..7]_ROUTE_HV_L[0..15]

HV_L

Reset: N/A

Register : Address

B0_P0_ROUTE_HV_L0: 0x40010180

B0_P0_ROUTE_HV_L1: 0x40010181

B0_P0_ROUTE_HV_L2: 0x40010182

B0_P0_ROUTE_HV_L3: 0x40010183

B0_P0_ROUTE_HV_L4: 0x40010184

B0_P0_ROUTE_HV_L5: 0x40010185

B0_P0_ROUTE_HV_L6: 0x40010186

B0_P0_ROUTE_HV_L7: 0x40010187

B0_P0_ROUTE_HV_L8: 0x40010188

B0_P0_ROUTE_HV_L9: 0x40010189

B0_P0_ROUTE_HV_L10: 0x4001018A

B0_P0_ROUTE_HV_L11: 0x4001018B

B0_P0_ROUTE_HV_L12: 0x4001018C

B0_P0_ROUTE_HV_L13: 0x4001018D

B0_P0_ROUTE_HV_L14: 0x4001018E

B0_P0_ROUTE_HV_L15: 0x4001018F

B0_P1_ROUTE_HV_L0: 0x40010380

B0_P1_ROUTE_HV_L1: 0x40010381

B0_P1_ROUTE_HV_L2: 0x40010382

B0_P1_ROUTE_HV_L3: 0x40010383

B0_P1_ROUTE_HV_L4: 0x40010384

B0_P1_ROUTE_HV_L5: 0x40010385

B0_P1_ROUTE_HV_L6: 0x40010386

B0_P1_ROUTE_HV_L7: 0x40010387

B0_P1_ROUTE_HV_L8: 0x40010388

B0_P1_ROUTE_HV_L9: 0x40010389

B0_P1_ROUTE_HV_L10: 0x4001038A

B0_P1_ROUTE_HV_L11: 0x4001038B

B0_P1_ROUTE_HV_L12: 0x4001038C

B0_P1_ROUTE_HV_L13: 0x4001038D

B0_P1_ROUTE_HV_L14: 0x4001038E

B0_P1_ROUTE_HV_L15: 0x4001038F

1.3.1165 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B0_P2_ROUTE_HV_L0: 0x40010580

B0_P2_ROUTE_HV_L1: 0x40010581

B0_P2_ROUTE_HV_L2: 0x40010582

B0_P2_ROUTE_HV_L3: 0x40010583

B0_P2_ROUTE_HV_L4: 0x40010584

B0_P2_ROUTE_HV_L5: 0x40010585

B0_P2_ROUTE_HV_L6: 0x40010586

B0_P2_ROUTE_HV_L7: 0x40010587

B0_P2_ROUTE_HV_L8: 0x40010588

B0_P2_ROUTE_HV_L9: 0x40010589

B0_P2_ROUTE_HV_L10: 0x4001058A

B0_P2_ROUTE_HV_L11: 0x4001058B

B0_P2_ROUTE_HV_L12: 0x4001058C

B0_P2_ROUTE_HV_L13: 0x4001058D

B0_P2_ROUTE_HV_L14: 0x4001058E

B0_P2_ROUTE_HV_L15: 0x4001058F

B0_P3_ROUTE_HV_L0: 0x40010780

B0_P3_ROUTE_HV_L1: 0x40010781

B0_P3_ROUTE_HV_L2: 0x40010782

B0_P3_ROUTE_HV_L3: 0x40010783

B0_P3_ROUTE_HV_L4: 0x40010784

B0_P3_ROUTE_HV_L5: 0x40010785

B0_P3_ROUTE_HV_L6: 0x40010786

B0_P3_ROUTE_HV_L7: 0x40010787

B0_P3_ROUTE_HV_L8: 0x40010788

B0_P3_ROUTE_HV_L9: 0x40010789

B0_P3_ROUTE_HV_L10: 0x4001078A

B0_P3_ROUTE_HV_L11: 0x4001078B

B0_P3_ROUTE_HV_L12: 0x4001078C

B0_P3_ROUTE_HV_L13: 0x4001078D

B0_P3_ROUTE_HV_L14: 0x4001078E

B0_P3_ROUTE_HV_L15: 0x4001078F

B0_P4_ROUTE_HV_L0: 0x40010980

B0_P4_ROUTE_HV_L1: 0x40010981

B0_P4_ROUTE_HV_L2: 0x40010982

B0_P4_ROUTE_HV_L3: 0x40010983

1.3.1165 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B0_P4_ROUTE_HV_L4: 0x40010984

B0_P4_ROUTE_HV_L5: 0x40010985

B0_P4_ROUTE_HV_L6: 0x40010986

B0_P4_ROUTE_HV_L7: 0x40010987

B0_P4_ROUTE_HV_L8: 0x40010988

B0_P4_ROUTE_HV_L9: 0x40010989

B0_P4_ROUTE_HV_L10: 0x4001098A

B0_P4_ROUTE_HV_L11: 0x4001098B

B0_P4_ROUTE_HV_L12: 0x4001098C

B0_P4_ROUTE_HV_L13: 0x4001098D

B0_P4_ROUTE_HV_L14: 0x4001098E

B0_P4_ROUTE_HV_L15: 0x4001098F

B0_P5_ROUTE_HV_L0: 0x40010B80

B0_P5_ROUTE_HV_L1: 0x40010B81

B0_P5_ROUTE_HV_L2: 0x40010B82

B0_P5_ROUTE_HV_L3: 0x40010B83

B0_P5_ROUTE_HV_L4: 0x40010B84

B0_P5_ROUTE_HV_L5: 0x40010B85

B0_P5_ROUTE_HV_L6: 0x40010B86

B0_P5_ROUTE_HV_L7: 0x40010B87

B0_P5_ROUTE_HV_L8: 0x40010B88

B0_P5_ROUTE_HV_L9: 0x40010B89

B0_P5_ROUTE_HV_L10: 0x40010B8A

B0_P5_ROUTE_HV_L11: 0x40010B8B

B0_P5_ROUTE_HV_L12: 0x40010B8C

B0_P5_ROUTE_HV_L13: 0x40010B8D

B0_P5_ROUTE_HV_L14: 0x40010B8E

B0_P5_ROUTE_HV_L15: 0x40010B8F

B0_P6_ROUTE_HV_L0: 0x40010D80

B0_P6_ROUTE_HV_L1: 0x40010D81

B0_P6_ROUTE_HV_L2: 0x40010D82

B0_P6_ROUTE_HV_L3: 0x40010D83

B0_P6_ROUTE_HV_L4: 0x40010D84

B0_P6_ROUTE_HV_L5: 0x40010D85

B0_P6_ROUTE_HV_L6: 0x40010D86

B0_P6_ROUTE_HV_L7: 0x40010D87

1.3.1165 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B0_P6_ROUTE_HV_L8: 0x40010D88

B0_P6_ROUTE_HV_L9: 0x40010D89

B0_P6_ROUTE_HV_L10: 0x40010D8A

B0_P6_ROUTE_HV_L11: 0x40010D8B

B0_P6_ROUTE_HV_L12: 0x40010D8C

B0_P6_ROUTE_HV_L13: 0x40010D8D

B0_P6_ROUTE_HV_L14: 0x40010D8E

B0_P6_ROUTE_HV_L15: 0x40010D8F

B0_P7_ROUTE_HV_L0: 0x40010F80

B0_P7_ROUTE_HV_L1: 0x40010F81

B0_P7_ROUTE_HV_L2: 0x40010F82

B0_P7_ROUTE_HV_L3: 0x40010F83

B0_P7_ROUTE_HV_L4: 0x40010F84

B0_P7_ROUTE_HV_L5: 0x40010F85

B0_P7_ROUTE_HV_L6: 0x40010F86

B0_P7_ROUTE_HV_L7: 0x40010F87

B0_P7_ROUTE_HV_L8: 0x40010F88

B0_P7_ROUTE_HV_L9: 0x40010F89

B0_P7_ROUTE_HV_L10: 0x40010F8A

B0_P7_ROUTE_HV_L11: 0x40010F8B

B0_P7_ROUTE_HV_L12: 0x40010F8C

B0_P7_ROUTE_HV_L13: 0x40010F8D

B0_P7_ROUTE_HV_L14: 0x40010F8E

B0_P7_ROUTE_HV_L15: 0x40010F8F

B1_P2_ROUTE_HV_L0: 0x40011580

B1_P2_ROUTE_HV_L1: 0x40011581

B1_P2_ROUTE_HV_L2: 0x40011582

B1_P2_ROUTE_HV_L3: 0x40011583

B1_P2_ROUTE_HV_L4: 0x40011584

B1_P2_ROUTE_HV_L5: 0x40011585

B1_P2_ROUTE_HV_L6: 0x40011586

B1_P2_ROUTE_HV_L7: 0x40011587

B1_P2_ROUTE_HV_L8: 0x40011588

B1_P2_ROUTE_HV_L9: 0x40011589

B1_P2_ROUTE_HV_L10: 0x4001158A

B1_P2_ROUTE_HV_L11: 0x4001158B

1.3.1165 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B1_P2_ROUTE_HV_L12: 0x4001158C

B1_P2_ROUTE_HV_L13: 0x4001158D

B1_P2_ROUTE_HV_L14: 0x4001158E

B1_P2_ROUTE_HV_L15: 0x4001158F

B1_P3_ROUTE_HV_L0: 0x40011780

B1_P3_ROUTE_HV_L1: 0x40011781

B1_P3_ROUTE_HV_L2: 0x40011782

B1_P3_ROUTE_HV_L3: 0x40011783

B1_P3_ROUTE_HV_L4: 0x40011784

B1_P3_ROUTE_HV_L5: 0x40011785

B1_P3_ROUTE_HV_L6: 0x40011786

B1_P3_ROUTE_HV_L7: 0x40011787

B1_P3_ROUTE_HV_L8: 0x40011788

B1_P3_ROUTE_HV_L9: 0x40011789

B1_P3_ROUTE_HV_L10: 0x4001178A

B1_P3_ROUTE_HV_L11: 0x4001178B

B1_P3_ROUTE_HV_L12: 0x4001178C

B1_P3_ROUTE_HV_L13: 0x4001178D

B1_P3_ROUTE_HV_L14: 0x4001178E

B1_P3_ROUTE_HV_L15: 0x4001178F

B1_P4_ROUTE_HV_L0: 0x40011980

B1_P4_ROUTE_HV_L1: 0x40011981

B1_P4_ROUTE_HV_L2: 0x40011982

B1_P4_ROUTE_HV_L3: 0x40011983

B1_P4_ROUTE_HV_L4: 0x40011984

B1_P4_ROUTE_HV_L5: 0x40011985

B1_P4_ROUTE_HV_L6: 0x40011986

B1_P4_ROUTE_HV_L7: 0x40011987

B1_P4_ROUTE_HV_L8: 0x40011988

B1_P4_ROUTE_HV_L9: 0x40011989

B1_P4_ROUTE_HV_L10: 0x4001198A

B1_P4_ROUTE_HV_L11: 0x4001198B

B1_P4_ROUTE_HV_L12: 0x4001198C

B1_P4_ROUTE_HV_L13: 0x4001198D

B1_P4_ROUTE_HV_L14: 0x4001198E

B1_P4_ROUTE_HV_L15: 0x4001198F

1.3.1165 B[0..3]_P[0..7]_ROUTE_HV_L[0..15] (continued)

Register : Address

B1_P5_ROUTE_HV_L0: 0x40011B80

B1_P5_ROUTE_HV_L1: 0x40011B81

B1_P5_ROUTE_HV_L2: 0x40011B82

B1_P5_ROUTE_HV_L3: 0x40011B83

B1_P5_ROUTE_HV_L4: 0x40011B84

B1_P5_ROUTE_HV_L5: 0x40011B85

B1_P5_ROUTE_HV_L6: 0x40011B86

B1_P5_ROUTE_HV_L7: 0x40011B87

B1_P5_ROUTE_HV_L8: 0x40011B88

B1_P5_ROUTE_HV_L9: 0x40011B89

B1_P5_ROUTE_HV_L10: 0x40011B8A

B1_P5_ROUTE_HV_L11: 0x40011B8B

B1_P5_ROUTE_HV_L12: 0x40011B8C

B1_P5_ROUTE_HV_L13: 0x40011B8D

B1_P5_ROUTE_HV_L14: 0x40011B8E

B1_P5_ROUTE_HV_L15: 0x40011B8F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	hv_byte							

UDB Channel HV Tile Configuration

Bits	Name	Description
7:0	hv_byte[7:0]	RAM configuration bytes for channel

1.3.1166 B[0..3]_P[0..7]_ROUTE_HS[0..23]

HS

Reset: N/A

Register : Address

B0_P0_ROUTE_HS0: 0x40010190	B0_P0_ROUTE_HS1: 0x40010191
B0_P0_ROUTE_HS2: 0x40010192	B0_P0_ROUTE_HS3: 0x40010193
B0_P0_ROUTE_HS4: 0x40010194	B0_P0_ROUTE_HS5: 0x40010195
B0_P0_ROUTE_HS6: 0x40010196	B0_P0_ROUTE_HS7: 0x40010197
B0_P0_ROUTE_HS8: 0x40010198	B0_P0_ROUTE_HS9: 0x40010199
B0_P0_ROUTE_HS10: 0x4001019A	B0_P0_ROUTE_HS11: 0x4001019B
B0_P0_ROUTE_HS12: 0x4001019C	B0_P0_ROUTE_HS13: 0x4001019D
B0_P0_ROUTE_HS14: 0x4001019E	B0_P0_ROUTE_HS15: 0x4001019F
B0_P0_ROUTE_HS16: 0x400101A0	B0_P0_ROUTE_HS17: 0x400101A1
B0_P0_ROUTE_HS18: 0x400101A2	B0_P0_ROUTE_HS19: 0x400101A3
B0_P0_ROUTE_HS20: 0x400101A4	B0_P0_ROUTE_HS21: 0x400101A5
B0_P0_ROUTE_HS22: 0x400101A6	B0_P0_ROUTE_HS23: 0x400101A7
B0_P1_ROUTE_HS0: 0x40010390	B0_P1_ROUTE_HS1: 0x40010391
B0_P1_ROUTE_HS2: 0x40010392	B0_P1_ROUTE_HS3: 0x40010393
B0_P1_ROUTE_HS4: 0x40010394	B0_P1_ROUTE_HS5: 0x40010395
B0_P1_ROUTE_HS6: 0x40010396	B0_P1_ROUTE_HS7: 0x40010397
B0_P1_ROUTE_HS8: 0x40010398	B0_P1_ROUTE_HS9: 0x40010399
B0_P1_ROUTE_HS10: 0x4001039A	B0_P1_ROUTE_HS11: 0x4001039B
B0_P1_ROUTE_HS12: 0x4001039C	B0_P1_ROUTE_HS13: 0x4001039D
B0_P1_ROUTE_HS14: 0x4001039E	B0_P1_ROUTE_HS15: 0x4001039F
B0_P1_ROUTE_HS16: 0x400103A0	B0_P1_ROUTE_HS17: 0x400103A1
B0_P1_ROUTE_HS18: 0x400103A2	B0_P1_ROUTE_HS19: 0x400103A3
B0_P1_ROUTE_HS20: 0x400103A4	B0_P1_ROUTE_HS21: 0x400103A5
B0_P1_ROUTE_HS22: 0x400103A6	B0_P1_ROUTE_HS23: 0x400103A7
B0_P2_ROUTE_HS0: 0x40010590	B0_P2_ROUTE_HS1: 0x40010591
B0_P2_ROUTE_HS2: 0x40010592	B0_P2_ROUTE_HS3: 0x40010593
B0_P2_ROUTE_HS4: 0x40010594	B0_P2_ROUTE_HS5: 0x40010595
B0_P2_ROUTE_HS6: 0x40010596	B0_P2_ROUTE_HS7: 0x40010597
B0_P2_ROUTE_HS8: 0x40010598	B0_P2_ROUTE_HS9: 0x40010599
B0_P2_ROUTE_HS10: 0x4001059A	B0_P2_ROUTE_HS11: 0x4001059B
B0_P2_ROUTE_HS12: 0x4001059C	B0_P2_ROUTE_HS13: 0x4001059D
B0_P2_ROUTE_HS14: 0x4001059E	B0_P2_ROUTE_HS15: 0x4001059F

1.3.1166 B[0..3]_P[0..7]_ROUTE_HS[0..23] (continued)

Register : Address

B0_P2_ROUTE_HS16: 0x400105A0
B0_P2_ROUTE_HS17: 0x400105A1
B0_P2_ROUTE_HS18: 0x400105A2
B0_P2_ROUTE_HS19: 0x400105A3
B0_P2_ROUTE_HS20: 0x400105A4
B0_P2_ROUTE_HS21: 0x400105A5
B0_P2_ROUTE_HS22: 0x400105A6
B0_P2_ROUTE_HS23: 0x400105A7
B0_P3_ROUTE_HS0: 0x40010790
B0_P3_ROUTE_HS1: 0x40010791
B0_P3_ROUTE_HS2: 0x40010792
B0_P3_ROUTE_HS3: 0x40010793
B0_P3_ROUTE_HS4: 0x40010794
B0_P3_ROUTE_HS5: 0x40010795
B0_P3_ROUTE_HS6: 0x40010796
B0_P3_ROUTE_HS7: 0x40010797
B0_P3_ROUTE_HS8: 0x40010798
B0_P3_ROUTE_HS9: 0x40010799
B0_P3_ROUTE_HS10: 0x4001079A
B0_P3_ROUTE_HS11: 0x4001079B
B0_P3_ROUTE_HS12: 0x4001079C
B0_P3_ROUTE_HS13: 0x4001079D
B0_P3_ROUTE_HS14: 0x4001079E
B0_P3_ROUTE_HS15: 0x4001079F
B0_P3_ROUTE_HS16: 0x400107A0
B0_P3_ROUTE_HS17: 0x400107A1
B0_P3_ROUTE_HS18: 0x400107A2
B0_P3_ROUTE_HS19: 0x400107A3
B0_P3_ROUTE_HS20: 0x400107A4
B0_P3_ROUTE_HS21: 0x400107A5
B0_P3_ROUTE_HS22: 0x400107A6
B0_P3_ROUTE_HS23: 0x400107A7
B0_P4_ROUTE_HS0: 0x40010990
B0_P4_ROUTE_HS1: 0x40010991
B0_P4_ROUTE_HS2: 0x40010992
B0_P4_ROUTE_HS3: 0x40010993
B0_P4_ROUTE_HS4: 0x40010994
B0_P4_ROUTE_HS5: 0x40010995
B0_P4_ROUTE_HS6: 0x40010996
B0_P4_ROUTE_HS7: 0x40010997
B0_P4_ROUTE_HS8: 0x40010998
B0_P4_ROUTE_HS9: 0x40010999
B0_P4_ROUTE_HS10: 0x4001099A
B0_P4_ROUTE_HS11: 0x4001099B
B0_P4_ROUTE_HS12: 0x4001099C
B0_P4_ROUTE_HS13: 0x4001099D
B0_P4_ROUTE_HS14: 0x4001099E
B0_P4_ROUTE_HS15: 0x4001099F
B0_P4_ROUTE_HS16: 0x400109A0
B0_P4_ROUTE_HS17: 0x400109A1
B0_P4_ROUTE_HS18: 0x400109A2
B0_P4_ROUTE_HS19: 0x400109A3
B0_P4_ROUTE_HS20: 0x400109A4
B0_P4_ROUTE_HS21: 0x400109A5
B0_P4_ROUTE_HS22: 0x400109A6
B0_P4_ROUTE_HS23: 0x400109A7
B0_P5_ROUTE_HS0: 0x40010B90
B0_P5_ROUTE_HS1: 0x40010B91
B0_P5_ROUTE_HS2: 0x40010B92
B0_P5_ROUTE_HS3: 0x40010B93
B0_P5_ROUTE_HS4: 0x40010B94
B0_P5_ROUTE_HS5: 0x40010B95
B0_P5_ROUTE_HS6: 0x40010B96
B0_P5_ROUTE_HS7: 0x40010B97
B0_P5_ROUTE_HS8: 0x40010B98
B0_P5_ROUTE_HS9: 0x40010B99
B0_P5_ROUTE_HS10: 0x40010B9A
B0_P5_ROUTE_HS11: 0x40010B9B
B0_P5_ROUTE_HS12: 0x40010B9C
B0_P5_ROUTE_HS13: 0x40010B9D
B0_P5_ROUTE_HS14: 0x40010B9E
B0_P5_ROUTE_HS15: 0x40010B9F

1.3.1166 B[0..3]_P[0..7]_ROUTE_HS[0..23] (continued)

Register : Address

B0_P5_ROUTE_HS16: 0x40010BA0
B0_P5_ROUTE_HS17: 0x40010BA1
B0_P5_ROUTE_HS18: 0x40010BA2
B0_P5_ROUTE_HS19: 0x40010BA3
B0_P5_ROUTE_HS20: 0x40010BA4
B0_P5_ROUTE_HS21: 0x40010BA5
B0_P5_ROUTE_HS22: 0x40010BA6
B0_P5_ROUTE_HS23: 0x40010BA7
B0_P6_ROUTE_HS0: 0x40010D90
B0_P6_ROUTE_HS1: 0x40010D91
B0_P6_ROUTE_HS2: 0x40010D92
B0_P6_ROUTE_HS3: 0x40010D93
B0_P6_ROUTE_HS4: 0x40010D94
B0_P6_ROUTE_HS5: 0x40010D95
B0_P6_ROUTE_HS6: 0x40010D96
B0_P6_ROUTE_HS7: 0x40010D97
B0_P6_ROUTE_HS8: 0x40010D98
B0_P6_ROUTE_HS9: 0x40010D99
B0_P6_ROUTE_HS10: 0x40010D9A
B0_P6_ROUTE_HS11: 0x40010D9B
B0_P6_ROUTE_HS12: 0x40010D9C
B0_P6_ROUTE_HS13: 0x40010D9D
B0_P6_ROUTE_HS14: 0x40010D9E
B0_P6_ROUTE_HS15: 0x40010D9F
B0_P6_ROUTE_HS16: 0x40010DA0
B0_P6_ROUTE_HS17: 0x40010DA1
B0_P6_ROUTE_HS18: 0x40010DA2
B0_P6_ROUTE_HS19: 0x40010DA3
B0_P6_ROUTE_HS20: 0x40010DA4
B0_P6_ROUTE_HS21: 0x40010DA5
B0_P6_ROUTE_HS22: 0x40010DA6
B0_P6_ROUTE_HS23: 0x40010DA7
B0_P7_ROUTE_HS0: 0x40010F90
B0_P7_ROUTE_HS1: 0x40010F91
B0_P7_ROUTE_HS2: 0x40010F92
B0_P7_ROUTE_HS3: 0x40010F93
B0_P7_ROUTE_HS4: 0x40010F94
B0_P7_ROUTE_HS5: 0x40010F95
B0_P7_ROUTE_HS6: 0x40010F96
B0_P7_ROUTE_HS7: 0x40010F97
B0_P7_ROUTE_HS8: 0x40010F98
B0_P7_ROUTE_HS9: 0x40010F99
B0_P7_ROUTE_HS10: 0x40010F9A
B0_P7_ROUTE_HS11: 0x40010F9B
B0_P7_ROUTE_HS12: 0x40010F9C
B0_P7_ROUTE_HS13: 0x40010F9D
B0_P7_ROUTE_HS14: 0x40010F9E
B0_P7_ROUTE_HS15: 0x40010F9F
B0_P7_ROUTE_HS16: 0x40010FA0
B0_P7_ROUTE_HS17: 0x40010FA1
B0_P7_ROUTE_HS18: 0x40010FA2
B0_P7_ROUTE_HS19: 0x40010FA3
B0_P7_ROUTE_HS20: 0x40010FA4
B0_P7_ROUTE_HS21: 0x40010FA5
B0_P7_ROUTE_HS22: 0x40010FA6
B0_P7_ROUTE_HS23: 0x40010FA7
B1_P2_ROUTE_HS0: 0x40011590
B1_P2_ROUTE_HS1: 0x40011591
B1_P2_ROUTE_HS2: 0x40011592
B1_P2_ROUTE_HS3: 0x40011593
B1_P2_ROUTE_HS4: 0x40011594
B1_P2_ROUTE_HS5: 0x40011595
B1_P2_ROUTE_HS6: 0x40011596
B1_P2_ROUTE_HS7: 0x40011597
B1_P2_ROUTE_HS8: 0x40011598
B1_P2_ROUTE_HS9: 0x40011599
B1_P2_ROUTE_HS10: 0x4001159A
B1_P2_ROUTE_HS11: 0x4001159B
B1_P2_ROUTE_HS12: 0x4001159C
B1_P2_ROUTE_HS13: 0x4001159D
B1_P2_ROUTE_HS14: 0x4001159E
B1_P2_ROUTE_HS15: 0x4001159F

1.3.1166 B[0..3]_P[0..7]_ROUTE_HS[0..23] (continued)

Register : Address

B1_P2_ROUTE_HS16: 0x400115A0
B1_P2_ROUTE_HS17: 0x400115A1
B1_P2_ROUTE_HS18: 0x400115A2
B1_P2_ROUTE_HS19: 0x400115A3
B1_P2_ROUTE_HS20: 0x400115A4
B1_P2_ROUTE_HS21: 0x400115A5
B1_P2_ROUTE_HS22: 0x400115A6
B1_P2_ROUTE_HS23: 0x400115A7
B1_P3_ROUTE_HS0: 0x40011790
B1_P3_ROUTE_HS1: 0x40011791
B1_P3_ROUTE_HS2: 0x40011792
B1_P3_ROUTE_HS3: 0x40011793
B1_P3_ROUTE_HS4: 0x40011794
B1_P3_ROUTE_HS5: 0x40011795
B1_P3_ROUTE_HS6: 0x40011796
B1_P3_ROUTE_HS7: 0x40011797
B1_P3_ROUTE_HS8: 0x40011798
B1_P3_ROUTE_HS9: 0x40011799
B1_P3_ROUTE_HS10: 0x4001179A
B1_P3_ROUTE_HS11: 0x4001179B
B1_P3_ROUTE_HS12: 0x4001179C
B1_P3_ROUTE_HS13: 0x4001179D
B1_P3_ROUTE_HS14: 0x4001179E
B1_P3_ROUTE_HS15: 0x4001179F
B1_P3_ROUTE_HS16: 0x400117A0
B1_P3_ROUTE_HS17: 0x400117A1
B1_P3_ROUTE_HS18: 0x400117A2
B1_P3_ROUTE_HS19: 0x400117A3
B1_P3_ROUTE_HS20: 0x400117A4
B1_P3_ROUTE_HS21: 0x400117A5
B1_P3_ROUTE_HS22: 0x400117A6
B1_P3_ROUTE_HS23: 0x400117A7
B1_P4_ROUTE_HS0: 0x40011990
B1_P4_ROUTE_HS1: 0x40011991
B1_P4_ROUTE_HS2: 0x40011992
B1_P4_ROUTE_HS3: 0x40011993
B1_P4_ROUTE_HS4: 0x40011994
B1_P4_ROUTE_HS5: 0x40011995
B1_P4_ROUTE_HS6: 0x40011996
B1_P4_ROUTE_HS7: 0x40011997
B1_P4_ROUTE_HS8: 0x40011998
B1_P4_ROUTE_HS9: 0x40011999
B1_P4_ROUTE_HS10: 0x4001199A
B1_P4_ROUTE_HS11: 0x4001199B
B1_P4_ROUTE_HS12: 0x4001199C
B1_P4_ROUTE_HS13: 0x4001199D
B1_P4_ROUTE_HS14: 0x4001199E
B1_P4_ROUTE_HS15: 0x4001199F
B1_P4_ROUTE_HS16: 0x400119A0
B1_P4_ROUTE_HS17: 0x400119A1
B1_P4_ROUTE_HS18: 0x400119A2
B1_P4_ROUTE_HS19: 0x400119A3
B1_P4_ROUTE_HS20: 0x400119A4
B1_P4_ROUTE_HS21: 0x400119A5
B1_P4_ROUTE_HS22: 0x400119A6
B1_P4_ROUTE_HS23: 0x400119A7
B1_P5_ROUTE_HS0: 0x40011B90
B1_P5_ROUTE_HS1: 0x40011B91
B1_P5_ROUTE_HS2: 0x40011B92
B1_P5_ROUTE_HS3: 0x40011B93
B1_P5_ROUTE_HS4: 0x40011B94
B1_P5_ROUTE_HS5: 0x40011B95
B1_P5_ROUTE_HS6: 0x40011B96
B1_P5_ROUTE_HS7: 0x40011B97
B1_P5_ROUTE_HS8: 0x40011B98
B1_P5_ROUTE_HS9: 0x40011B99
B1_P5_ROUTE_HS10: 0x40011B9A
B1_P5_ROUTE_HS11: 0x40011B9B
B1_P5_ROUTE_HS12: 0x40011B9C
B1_P5_ROUTE_HS13: 0x40011B9D
B1_P5_ROUTE_HS14: 0x40011B9E
B1_P5_ROUTE_HS15: 0x40011B9F

1.3.1166 B[0..3]_P[0..7]_ROUTE_HS[0..23] (continued)

Register : Address

B1_P5_ROUTE_HS16: 0x40011BA0
B1_P5_ROUTE_HS17: 0x40011BA1
B1_P5_ROUTE_HS18: 0x40011BA2
B1_P5_ROUTE_HS19: 0x40011BA3
B1_P5_ROUTE_HS20: 0x40011BA4
B1_P5_ROUTE_HS21: 0x40011BA5
B1_P5_ROUTE_HS22: 0x40011BA6
B1_P5_ROUTE_HS23: 0x40011BA7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	hs_byte							

UDB Channel HS Tile Configuration

Bits	Name	Description
7:0	hs_byte[7:0]	RAM configuration bytes for channel

1.3.1167 B[0..3]_P[0..7]_ROUTE_HV_R[0..15]

HV_R

Reset: N/A

Register : Address

B0_P0_ROUTE_HV_R0: 0x400101A8
B0_P0_ROUTE_HV_R1: 0x400101A9
B0_P0_ROUTE_HV_R2: 0x400101AA
B0_P0_ROUTE_HV_R3: 0x400101AB
B0_P0_ROUTE_HV_R4: 0x400101AC
B0_P0_ROUTE_HV_R5: 0x400101AD
B0_P0_ROUTE_HV_R6: 0x400101AE
B0_P0_ROUTE_HV_R7: 0x400101AF
B0_P0_ROUTE_HV_R8: 0x400101B0
B0_P0_ROUTE_HV_R9: 0x400101B1
B0_P0_ROUTE_HV_R10: 0x400101B2
B0_P0_ROUTE_HV_R11: 0x400101B3
B0_P0_ROUTE_HV_R12: 0x400101B4
B0_P0_ROUTE_HV_R13: 0x400101B5
B0_P0_ROUTE_HV_R14: 0x400101B6
B0_P0_ROUTE_HV_R15: 0x400101B7
B0_P1_ROUTE_HV_R0: 0x400103A8
B0_P1_ROUTE_HV_R1: 0x400103A9
B0_P1_ROUTE_HV_R2: 0x400103AA
B0_P1_ROUTE_HV_R3: 0x400103AB
B0_P1_ROUTE_HV_R4: 0x400103AC
B0_P1_ROUTE_HV_R5: 0x400103AD
B0_P1_ROUTE_HV_R6: 0x400103AE
B0_P1_ROUTE_HV_R7: 0x400103AF
B0_P1_ROUTE_HV_R8: 0x400103B0
B0_P1_ROUTE_HV_R9: 0x400103B1
B0_P1_ROUTE_HV_R10: 0x400103B2
B0_P1_ROUTE_HV_R11: 0x400103B3
B0_P1_ROUTE_HV_R12: 0x400103B4
B0_P1_ROUTE_HV_R13: 0x400103B5
B0_P1_ROUTE_HV_R14: 0x400103B6
B0_P1_ROUTE_HV_R15: 0x400103B7

1.3.1167 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B0_P2_ROUTE_HV_R0: 0x400105A8

B0_P2_ROUTE_HV_R1: 0x400105A9

B0_P2_ROUTE_HV_R2: 0x400105AA

B0_P2_ROUTE_HV_R3: 0x400105AB

B0_P2_ROUTE_HV_R4: 0x400105AC

B0_P2_ROUTE_HV_R5: 0x400105AD

B0_P2_ROUTE_HV_R6: 0x400105AE

B0_P2_ROUTE_HV_R7: 0x400105AF

B0_P2_ROUTE_HV_R8: 0x400105B0

B0_P2_ROUTE_HV_R9: 0x400105B1

B0_P2_ROUTE_HV_R10: 0x400105B2

B0_P2_ROUTE_HV_R11: 0x400105B3

B0_P2_ROUTE_HV_R12: 0x400105B4

B0_P2_ROUTE_HV_R13: 0x400105B5

B0_P2_ROUTE_HV_R14: 0x400105B6

B0_P2_ROUTE_HV_R15: 0x400105B7

B0_P3_ROUTE_HV_R0: 0x400107A8

B0_P3_ROUTE_HV_R1: 0x400107A9

B0_P3_ROUTE_HV_R2: 0x400107AA

B0_P3_ROUTE_HV_R3: 0x400107AB

B0_P3_ROUTE_HV_R4: 0x400107AC

B0_P3_ROUTE_HV_R5: 0x400107AD

B0_P3_ROUTE_HV_R6: 0x400107AE

B0_P3_ROUTE_HV_R7: 0x400107AF

B0_P3_ROUTE_HV_R8: 0x400107B0

B0_P3_ROUTE_HV_R9: 0x400107B1

B0_P3_ROUTE_HV_R10: 0x400107B2

B0_P3_ROUTE_HV_R11: 0x400107B3

B0_P3_ROUTE_HV_R12: 0x400107B4

B0_P3_ROUTE_HV_R13: 0x400107B5

B0_P3_ROUTE_HV_R14: 0x400107B6

B0_P3_ROUTE_HV_R15: 0x400107B7

B0_P4_ROUTE_HV_R0: 0x400109A8

B0_P4_ROUTE_HV_R1: 0x400109A9

B0_P4_ROUTE_HV_R2: 0x400109AA

B0_P4_ROUTE_HV_R3: 0x400109AB

1.3.1167 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B0_P4_ROUTE_HV_R4: 0x400109AC

B0_P4_ROUTE_HV_R5: 0x400109AD

B0_P4_ROUTE_HV_R6: 0x400109AE

B0_P4_ROUTE_HV_R7: 0x400109AF

B0_P4_ROUTE_HV_R8: 0x400109B0

B0_P4_ROUTE_HV_R9: 0x400109B1

B0_P4_ROUTE_HV_R10: 0x400109B2

B0_P4_ROUTE_HV_R11: 0x400109B3

B0_P4_ROUTE_HV_R12: 0x400109B4

B0_P4_ROUTE_HV_R13: 0x400109B5

B0_P4_ROUTE_HV_R14: 0x400109B6

B0_P4_ROUTE_HV_R15: 0x400109B7

B0_P5_ROUTE_HV_R0: 0x40010BA8

B0_P5_ROUTE_HV_R1: 0x40010BA9

B0_P5_ROUTE_HV_R2: 0x40010BAA

B0_P5_ROUTE_HV_R3: 0x40010BAB

B0_P5_ROUTE_HV_R4: 0x40010BAC

B0_P5_ROUTE_HV_R5: 0x40010BAD

B0_P5_ROUTE_HV_R6: 0x40010BAE

B0_P5_ROUTE_HV_R7: 0x40010BAF

B0_P5_ROUTE_HV_R8: 0x40010BB0

B0_P5_ROUTE_HV_R9: 0x40010BB1

B0_P5_ROUTE_HV_R10: 0x40010BB2

B0_P5_ROUTE_HV_R11: 0x40010BB3

B0_P5_ROUTE_HV_R12: 0x40010BB4

B0_P5_ROUTE_HV_R13: 0x40010BB5

B0_P5_ROUTE_HV_R14: 0x40010BB6

B0_P5_ROUTE_HV_R15: 0x40010BB7

B0_P6_ROUTE_HV_R0: 0x40010DA8

B0_P6_ROUTE_HV_R1: 0x40010DA9

B0_P6_ROUTE_HV_R2: 0x40010DAA

B0_P6_ROUTE_HV_R3: 0x40010DAB

B0_P6_ROUTE_HV_R4: 0x40010DAC

B0_P6_ROUTE_HV_R5: 0x40010DAD

B0_P6_ROUTE_HV_R6: 0x40010DAE

B0_P6_ROUTE_HV_R7: 0x40010DAF

1.3.1167 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B0_P6_ROUTE_HV_R8: 0x40010DB0

B0_P6_ROUTE_HV_R9: 0x40010DB1

B0_P6_ROUTE_HV_R10: 0x40010DB2

B0_P6_ROUTE_HV_R11: 0x40010DB3

B0_P6_ROUTE_HV_R12: 0x40010DB4

B0_P6_ROUTE_HV_R13: 0x40010DB5

B0_P6_ROUTE_HV_R14: 0x40010DB6

B0_P6_ROUTE_HV_R15: 0x40010DB7

B0_P7_ROUTE_HV_R0: 0x40010FA8

B0_P7_ROUTE_HV_R1: 0x40010FA9

B0_P7_ROUTE_HV_R2: 0x40010FAA

B0_P7_ROUTE_HV_R3: 0x40010FAB

B0_P7_ROUTE_HV_R4: 0x40010FAC

B0_P7_ROUTE_HV_R5: 0x40010FAD

B0_P7_ROUTE_HV_R6: 0x40010FAE

B0_P7_ROUTE_HV_R7: 0x40010FAF

B0_P7_ROUTE_HV_R8: 0x40010FB0

B0_P7_ROUTE_HV_R9: 0x40010FB1

B0_P7_ROUTE_HV_R10: 0x40010FB2

B0_P7_ROUTE_HV_R11: 0x40010FB3

B0_P7_ROUTE_HV_R12: 0x40010FB4

B0_P7_ROUTE_HV_R13: 0x40010FB5

B0_P7_ROUTE_HV_R14: 0x40010FB6

B0_P7_ROUTE_HV_R15: 0x40010FB7

B1_P2_ROUTE_HV_R0: 0x400115A8

B1_P2_ROUTE_HV_R1: 0x400115A9

B1_P2_ROUTE_HV_R2: 0x400115AA

B1_P2_ROUTE_HV_R3: 0x400115AB

B1_P2_ROUTE_HV_R4: 0x400115AC

B1_P2_ROUTE_HV_R5: 0x400115AD

B1_P2_ROUTE_HV_R6: 0x400115AE

B1_P2_ROUTE_HV_R7: 0x400115AF

B1_P2_ROUTE_HV_R8: 0x400115B0

B1_P2_ROUTE_HV_R9: 0x400115B1

B1_P2_ROUTE_HV_R10: 0x400115B2

B1_P2_ROUTE_HV_R11: 0x400115B3

1.3.1167 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B1_P2_ROUTE_HV_R12: 0x400115B4

B1_P2_ROUTE_HV_R13: 0x400115B5

B1_P2_ROUTE_HV_R14: 0x400115B6

B1_P2_ROUTE_HV_R15: 0x400115B7

B1_P3_ROUTE_HV_R0: 0x400117A8

B1_P3_ROUTE_HV_R1: 0x400117A9

B1_P3_ROUTE_HV_R2: 0x400117AA

B1_P3_ROUTE_HV_R3: 0x400117AB

B1_P3_ROUTE_HV_R4: 0x400117AC

B1_P3_ROUTE_HV_R5: 0x400117AD

B1_P3_ROUTE_HV_R6: 0x400117AE

B1_P3_ROUTE_HV_R7: 0x400117AF

B1_P3_ROUTE_HV_R8: 0x400117B0

B1_P3_ROUTE_HV_R9: 0x400117B1

B1_P3_ROUTE_HV_R10: 0x400117B2

B1_P3_ROUTE_HV_R11: 0x400117B3

B1_P3_ROUTE_HV_R12: 0x400117B4

B1_P3_ROUTE_HV_R13: 0x400117B5

B1_P3_ROUTE_HV_R14: 0x400117B6

B1_P3_ROUTE_HV_R15: 0x400117B7

B1_P4_ROUTE_HV_R0: 0x400119A8

B1_P4_ROUTE_HV_R1: 0x400119A9

B1_P4_ROUTE_HV_R2: 0x400119AA

B1_P4_ROUTE_HV_R3: 0x400119AB

B1_P4_ROUTE_HV_R4: 0x400119AC

B1_P4_ROUTE_HV_R5: 0x400119AD

B1_P4_ROUTE_HV_R6: 0x400119AE

B1_P4_ROUTE_HV_R7: 0x400119AF

B1_P4_ROUTE_HV_R8: 0x400119B0

B1_P4_ROUTE_HV_R9: 0x400119B1

B1_P4_ROUTE_HV_R10: 0x400119B2

B1_P4_ROUTE_HV_R11: 0x400119B3

B1_P4_ROUTE_HV_R12: 0x400119B4

B1_P4_ROUTE_HV_R13: 0x400119B5

B1_P4_ROUTE_HV_R14: 0x400119B6

B1_P4_ROUTE_HV_R15: 0x400119B7

1.3.1167 B[0..3]_P[0..7]_ROUTE_HV_R[0..15] (continued)

Register : Address

B1_P5_ROUTE_HV_R0: 0x40011BA8

B1_P5_ROUTE_HV_R1: 0x40011BA9

B1_P5_ROUTE_HV_R2: 0x40011BAA

B1_P5_ROUTE_HV_R3: 0x40011BAB

B1_P5_ROUTE_HV_R4: 0x40011BAC

B1_P5_ROUTE_HV_R5: 0x40011BAD

B1_P5_ROUTE_HV_R6: 0x40011BAE

B1_P5_ROUTE_HV_R7: 0x40011BAF

B1_P5_ROUTE_HV_R8: 0x40011BB0

B1_P5_ROUTE_HV_R9: 0x40011BB1

B1_P5_ROUTE_HV_R10: 0x40011BB2

B1_P5_ROUTE_HV_R11: 0x40011BB3

B1_P5_ROUTE_HV_R12: 0x40011BB4

B1_P5_ROUTE_HV_R13: 0x40011BB5

B1_P5_ROUTE_HV_R14: 0x40011BB6

B1_P5_ROUTE_HV_R15: 0x40011BB7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	hv_byte							

UDB Channel HV Tile Configuration

Bits	Name	Description
7:0	hv_byte[7:0]	RAM configuration bytes for channel

1.3.1168 B[0..3]_P[0..7]_ROUTE_PLD0IN0

PLD0IN0

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN0: 0x400101C0

B0_P1_ROUTE_PLD0IN0: 0x400103C0

B0_P2_ROUTE_PLD0IN0: 0x400105C0

B0_P3_ROUTE_PLD0IN0: 0x400107C0

B0_P4_ROUTE_PLD0IN0: 0x400109C0

B0_P5_ROUTE_PLD0IN0: 0x40010BC0

B0_P6_ROUTE_PLD0IN0: 0x40010DC0

B0_P7_ROUTE_PLD0IN0: 0x40010FC0

B1_P2_ROUTE_PLD0IN0: 0x400115C0

B1_P3_ROUTE_PLD0IN0: 0x400117C0

B1_P4_ROUTE_PLD0IN0: 0x400119C0

B1_P5_ROUTE_PLD0IN0: 0x40011BC0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1169 B[0..3]_P[0..7]_ROUTE_PLD0IN1

PLD0IN1

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN1: 0x400101C2

B0_P1_ROUTE_PLD0IN1: 0x400103C2

B0_P2_ROUTE_PLD0IN1: 0x400105C2

B0_P3_ROUTE_PLD0IN1: 0x400107C2

B0_P4_ROUTE_PLD0IN1: 0x400109C2

B0_P5_ROUTE_PLD0IN1: 0x40010BC2

B0_P6_ROUTE_PLD0IN1: 0x40010DC2

B0_P7_ROUTE_PLD0IN1: 0x40010FC2

B1_P2_ROUTE_PLD0IN1: 0x400115C2

B1_P3_ROUTE_PLD0IN1: 0x400117C2

B1_P4_ROUTE_PLD0IN1: 0x400119C2

B1_P5_ROUTE_PLD0IN1: 0x40011BC2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1170 B[0..3]_P[0..7]_ROUTE_PLD0IN2

PLD0IN2

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN2: 0x400101C4

B0_P1_ROUTE_PLD0IN2: 0x400103C4

B0_P2_ROUTE_PLD0IN2: 0x400105C4

B0_P3_ROUTE_PLD0IN2: 0x400107C4

B0_P4_ROUTE_PLD0IN2: 0x400109C4

B0_P5_ROUTE_PLD0IN2: 0x40010BC4

B0_P6_ROUTE_PLD0IN2: 0x40010DC4

B0_P7_ROUTE_PLD0IN2: 0x40010FC4

B1_P2_ROUTE_PLD0IN2: 0x400115C4

B1_P3_ROUTE_PLD0IN2: 0x400117C4

B1_P4_ROUTE_PLD0IN2: 0x400119C4

B1_P5_ROUTE_PLD0IN2: 0x40011BC4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1171 B[0..3]_P[0..7]_ROUTE_PLD1IN0

PLD1IN0

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN0: 0x400101CA

B0_P1_ROUTE_PLD1IN0: 0x400103CA

B0_P2_ROUTE_PLD1IN0: 0x400105CA

B0_P3_ROUTE_PLD1IN0: 0x400107CA

B0_P4_ROUTE_PLD1IN0: 0x400109CA

B0_P5_ROUTE_PLD1IN0: 0x40010BCA

B0_P6_ROUTE_PLD1IN0: 0x40010DCA

B0_P7_ROUTE_PLD1IN0: 0x40010FCA

B1_P2_ROUTE_PLD1IN0: 0x400115CA

B1_P3_ROUTE_PLD1IN0: 0x400117CA

B1_P4_ROUTE_PLD1IN0: 0x400119CA

B1_P5_ROUTE_PLD1IN0: 0x40011BCA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1172 B[0..3]_P[0..7]_ROUTE_PLD1IN1

PLD1IN1

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN1: 0x400101CC

B0_P1_ROUTE_PLD1IN1: 0x400103CC

B0_P2_ROUTE_PLD1IN1: 0x400105CC

B0_P3_ROUTE_PLD1IN1: 0x400107CC

B0_P4_ROUTE_PLD1IN1: 0x400109CC

B0_P5_ROUTE_PLD1IN1: 0x40010BCC

B0_P6_ROUTE_PLD1IN1: 0x40010DCC

B0_P7_ROUTE_PLD1IN1: 0x40010FCC

B1_P2_ROUTE_PLD1IN1: 0x400115CC

B1_P3_ROUTE_PLD1IN1: 0x400117CC

B1_P4_ROUTE_PLD1IN1: 0x400119CC

B1_P5_ROUTE_PLD1IN1: 0x40011BCC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1173 B[0..3]_P[0..7]_ROUTE_PLD1IN2

PLD1IN2

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN2: 0x400101CE

B0_P1_ROUTE_PLD1IN2: 0x400103CE

B0_P2_ROUTE_PLD1IN2: 0x400105CE

B0_P3_ROUTE_PLD1IN2: 0x400107CE

B0_P4_ROUTE_PLD1IN2: 0x400109CE

B0_P5_ROUTE_PLD1IN2: 0x40010BCE

B0_P6_ROUTE_PLD1IN2: 0x40010DCE

B0_P7_ROUTE_PLD1IN2: 0x40010FCE

B1_P2_ROUTE_PLD1IN2: 0x400115CE

B1_P3_ROUTE_PLD1IN2: 0x400117CE

B1_P4_ROUTE_PLD1IN2: 0x400119CE

B1_P5_ROUTE_PLD1IN2: 0x40011BCE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1174 B[0..3]_P[0..7]_ROUTE_DPIN0

DPIN0

Reset: N/A

Register : Address

B0_P0_ROUTE_DPIN0: 0x400101D0

B0_P1_ROUTE_DPIN0: 0x400103D0

B0_P2_ROUTE_DPIN0: 0x400105D0

B0_P3_ROUTE_DPIN0: 0x400107D0

B0_P4_ROUTE_DPIN0: 0x400109D0

B0_P5_ROUTE_DPIN0: 0x40010BD0

B0_P6_ROUTE_DPIN0: 0x40010DD0

B0_P7_ROUTE_DPIN0: 0x40010FD0

B1_P2_ROUTE_DPIN0: 0x400115D0

B1_P3_ROUTE_DPIN0: 0x400117D0

B1_P4_ROUTE_DPIN0: 0x400119D0

B1_P5_ROUTE_DPIN0: 0x40011BD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1175 B[0..3]_P[0..7]_ROUTE_DPIN1

DPIN1

Reset: N/A

Register : Address

B0_P0_ROUTE_DPIN1: 0x400101D2

B0_P1_ROUTE_DPIN1: 0x400103D2

B0_P2_ROUTE_DPIN1: 0x400105D2

B0_P3_ROUTE_DPIN1: 0x400107D2

B0_P4_ROUTE_DPIN1: 0x400109D2

B0_P5_ROUTE_DPIN1: 0x40010BD2

B0_P6_ROUTE_DPIN1: 0x40010DD2

B0_P7_ROUTE_DPIN1: 0x40010FD2

B1_P2_ROUTE_DPIN1: 0x400115D2

B1_P3_ROUTE_DPIN1: 0x400117D2

B1_P4_ROUTE_DPIN1: 0x400119D2

B1_P5_ROUTE_DPIN1: 0x40011BD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:UU		R/W:UU		NA:00	
HW Access	NA		R		R		NA	
Name			pi_bot		pi_top			

UDB Channel PI Tile Configuration (half populated)

Bits	Name	Description
5:4	pi_bot[1:0]	RAM configuration bits (2) for BOTTOM UDB port interface configuration
3:2	pi_top[1:0]	RAM configuration bits (2) for TOP UDB port interface configuration

1.3.1176 B[0..3]_P[0..7]_ROUTE_SCIN

SCIN

Reset: N/A

Register : Address

B0_P0_ROUTE_SCIN: 0x400101D6

B0_P1_ROUTE_SCIN: 0x400103D6

B0_P2_ROUTE_SCIN: 0x400105D6

B0_P3_ROUTE_SCIN: 0x400107D6

B0_P4_ROUTE_SCIN: 0x400109D6

B0_P5_ROUTE_SCIN: 0x40010BD6

B0_P6_ROUTE_SCIN: 0x40010DD6

B0_P7_ROUTE_SCIN: 0x40010FD6

B1_P2_ROUTE_SCIN: 0x400115D6

B1_P3_ROUTE_SCIN: 0x400117D6

B1_P4_ROUTE_SCIN: 0x400119D6

B1_P5_ROUTE_SCIN: 0x40011BD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1177 B[0..3]_P[0..7]_ROUTE_SCIOIN

SCIOIN

Reset: N/A

Register : Address

B0_P0_ROUTE_SCIOIN: 0x400101D8

B0_P1_ROUTE_SCIOIN: 0x400103D8

B0_P2_ROUTE_SCIOIN: 0x400105D8

B0_P3_ROUTE_SCIOIN: 0x400107D8

B0_P4_ROUTE_SCIOIN: 0x400109D8

B0_P5_ROUTE_SCIOIN: 0x40010BD8

B0_P6_ROUTE_SCIOIN: 0x40010DD8

B0_P7_ROUTE_SCIOIN: 0x40010FD8

B1_P2_ROUTE_SCIOIN: 0x400115D8

B1_P3_ROUTE_SCIOIN: 0x400117D8

B1_P4_ROUTE_SCIOIN: 0x400119D8

B1_P5_ROUTE_SCIOIN: 0x40011BD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1178 B[0..3]_P[0..7]_ROUTE_RCIN

RCIN

Reset: N/A

Register : Address

B0_P0_ROUTE_RCIN: 0x400101DE

B0_P1_ROUTE_RCIN: 0x400103DE

B0_P2_ROUTE_RCIN: 0x400105DE

B0_P3_ROUTE_RCIN: 0x400107DE

B0_P4_ROUTE_RCIN: 0x400109DE

B0_P5_ROUTE_RCIN: 0x40010BDE

B0_P6_ROUTE_RCIN: 0x40010DDE

B0_P7_ROUTE_RCIN: 0x40010FDE

B1_P2_ROUTE_RCIN: 0x400115DE

B1_P3_ROUTE_RCIN: 0x400117DE

B1_P4_ROUTE_RCIN: 0x400119DE

B1_P5_ROUTE_RCIN: 0x40011BDE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1179 B[0..3]_P[0..7]_ROUTE_VS0

VS0

Reset: N/A

Register : Address

B0_P0_ROUTE_VS0: 0x400101E0	B0_P1_ROUTE_VS0: 0x400103E0
B0_P2_ROUTE_VS0: 0x400105E0	B0_P3_ROUTE_VS0: 0x400107E0
B0_P4_ROUTE_VS0: 0x400109E0	B0_P5_ROUTE_VS0: 0x40010BE0
B0_P6_ROUTE_VS0: 0x40010DE0	B0_P7_ROUTE_VS0: 0x40010FE0
B1_P2_ROUTE_VS0: 0x400115E0	B1_P3_ROUTE_VS0: 0x400117E0
B1_P4_ROUTE_VS0: 0x400119E0	B1_P5_ROUTE_VS0: 0x40011BE0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1180 B[0..3]_P[0..7]_ROUTE_VS1

VS1

Reset: N/A

Register : Address

B0_P0_ROUTE_VS1: 0x400101E2
B0_P1_ROUTE_VS1: 0x400103E2
B0_P2_ROUTE_VS1: 0x400105E2
B0_P3_ROUTE_VS1: 0x400107E2
B0_P4_ROUTE_VS1: 0x400109E2
B0_P5_ROUTE_VS1: 0x40010BE2
B0_P6_ROUTE_VS1: 0x40010DE2
B0_P7_ROUTE_VS1: 0x40010FE2
B1_P2_ROUTE_VS1: 0x400115E2
B1_P3_ROUTE_VS1: 0x400117E2
B1_P4_ROUTE_VS1: 0x400119E2
B1_P5_ROUTE_VS1: 0x40011BE2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1181 B[0..3]_P[0..7]_ROUTE_VS2

VS2

Reset: N/A

Register : Address

B0_P0_ROUTE_VS2: 0x400101E4	B0_P1_ROUTE_VS2: 0x400103E4
B0_P2_ROUTE_VS2: 0x400105E4	B0_P3_ROUTE_VS2: 0x400107E4
B0_P4_ROUTE_VS2: 0x400109E4	B0_P5_ROUTE_VS2: 0x40010BE4
B0_P6_ROUTE_VS2: 0x40010DE4	B0_P7_ROUTE_VS2: 0x40010FE4
B1_P2_ROUTE_VS2: 0x400115E4	B1_P3_ROUTE_VS2: 0x400117E4
B1_P4_ROUTE_VS2: 0x400119E4	B1_P5_ROUTE_VS2: 0x40011BE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1182 B[0..3]_P[0..7]_ROUTE_VS3

VS3

Reset: N/A

Register : Address

B0_P0_ROUTE_VS3: 0x400101E6
B0_P1_ROUTE_VS3: 0x400103E6
B0_P2_ROUTE_VS3: 0x400105E6
B0_P3_ROUTE_VS3: 0x400107E6
B0_P4_ROUTE_VS3: 0x400109E6
B0_P5_ROUTE_VS3: 0x40010BE6
B0_P6_ROUTE_VS3: 0x40010DE6
B0_P7_ROUTE_VS3: 0x40010FE6
B1_P2_ROUTE_VS3: 0x400115E6
B1_P3_ROUTE_VS3: 0x400117E6
B1_P4_ROUTE_VS3: 0x400119E6
B1_P5_ROUTE_VS3: 0x40011BE6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1183 B[0..3]_P[0..7]_ROUTE_VS4

VS4

Reset: N/A

Register : Address

B0_P0_ROUTE_VS4: 0x400101E8	B0_P1_ROUTE_VS4: 0x400103E8
B0_P2_ROUTE_VS4: 0x400105E8	B0_P3_ROUTE_VS4: 0x400107E8
B0_P4_ROUTE_VS4: 0x400109E8	B0_P5_ROUTE_VS4: 0x40010BE8
B0_P6_ROUTE_VS4: 0x40010DE8	B0_P7_ROUTE_VS4: 0x40010FE8
B1_P2_ROUTE_VS4: 0x400115E8	B1_P3_ROUTE_VS4: 0x400117E8
B1_P4_ROUTE_VS4: 0x400119E8	B1_P5_ROUTE_VS4: 0x40011BE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1184 B[0..3]_P[0..7]_ROUTE_VS5

VS5

Reset: N/A

Register : Address

B0_P0_ROUTE_VS5: 0x400101EA
B0_P1_ROUTE_VS5: 0x400103EA
B0_P2_ROUTE_VS5: 0x400105EA
B0_P3_ROUTE_VS5: 0x400107EA
B0_P4_ROUTE_VS5: 0x400109EA
B0_P5_ROUTE_VS5: 0x40010BEA
B0_P6_ROUTE_VS5: 0x40010DEA
B0_P7_ROUTE_VS5: 0x40010FEA
B1_P2_ROUTE_VS5: 0x400115EA
B1_P3_ROUTE_VS5: 0x400117EA
B1_P4_ROUTE_VS5: 0x400119EA
B1_P5_ROUTE_VS5: 0x40011BEA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1185 B[0..3]_P[0..7]_ROUTE_VS6

VS6

Reset: N/A

Register : Address

B0_P0_ROUTE_VS6: 0x400101EC	B0_P1_ROUTE_VS6: 0x400103EC
B0_P2_ROUTE_VS6: 0x400105EC	B0_P3_ROUTE_VS6: 0x400107EC
B0_P4_ROUTE_VS6: 0x400109EC	B0_P5_ROUTE_VS6: 0x40010BEC
B0_P6_ROUTE_VS6: 0x40010DEC	B0_P7_ROUTE_VS6: 0x40010FEC
B1_P2_ROUTE_VS6: 0x400115EC	B1_P3_ROUTE_VS6: 0x400117EC
B1_P4_ROUTE_VS6: 0x400119EC	B1_P5_ROUTE_VS6: 0x40011BEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1186 B[0..3]_P[0..7]_ROUTE_VS7

VS7

Reset: N/A

Register : Address

B0_P0_ROUTE_VS7: 0x400101EE
B0_P1_ROUTE_VS7: 0x400103EE
B0_P2_ROUTE_VS7: 0x400105EE
B0_P3_ROUTE_VS7: 0x400107EE
B0_P4_ROUTE_VS7: 0x400109EE
B0_P5_ROUTE_VS7: 0x40010BEE
B0_P6_ROUTE_VS7: 0x40010DEE
B0_P7_ROUTE_VS7: 0x40010FEE
B1_P2_ROUTE_VS7: 0x400115EE
B1_P3_ROUTE_VS7: 0x400117EE
B1_P4_ROUTE_VS7: 0x400119EE
B1_P5_ROUTE_VS7: 0x40011BEE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1187 DSI[0..15]_HC[0..127]

HC

Reset: N/A

Register : Address

DSI0_HC0: 0x40014000	DSI0_HC1: 0x40014001
DSI0_HC2: 0x40014002	DSI0_HC3: 0x40014003
DSI0_HC4: 0x40014004	DSI0_HC5: 0x40014005
DSI0_HC6: 0x40014006	DSI0_HC7: 0x40014007
DSI0_HC8: 0x40014008	DSI0_HC9: 0x40014009
DSI0_HC10: 0x4001400A	DSI0_HC11: 0x4001400B
DSI0_HC12: 0x4001400C	DSI0_HC13: 0x4001400D
DSI0_HC14: 0x4001400E	DSI0_HC15: 0x4001400F
DSI0_HC16: 0x40014010	DSI0_HC17: 0x40014011
DSI0_HC18: 0x40014012	DSI0_HC19: 0x40014013
DSI0_HC20: 0x40014014	DSI0_HC21: 0x40014015
DSI0_HC22: 0x40014016	DSI0_HC23: 0x40014017
DSI0_HC24: 0x40014018	DSI0_HC25: 0x40014019
DSI0_HC26: 0x4001401A	DSI0_HC27: 0x4001401B
DSI0_HC28: 0x4001401C	DSI0_HC29: 0x4001401D
DSI0_HC30: 0x4001401E	DSI0_HC31: 0x4001401F
DSI0_HC32: 0x40014020	DSI0_HC33: 0x40014021
DSI0_HC34: 0x40014022	DSI0_HC35: 0x40014023
DSI0_HC36: 0x40014024	DSI0_HC37: 0x40014025
DSI0_HC38: 0x40014026	DSI0_HC39: 0x40014027
DSI0_HC40: 0x40014028	DSI0_HC41: 0x40014029
DSI0_HC42: 0x4001402A	DSI0_HC43: 0x4001402B
DSI0_HC44: 0x4001402C	DSI0_HC45: 0x4001402D
DSI0_HC46: 0x4001402E	DSI0_HC47: 0x4001402F
DSI0_HC48: 0x40014030	DSI0_HC49: 0x40014031
DSI0_HC50: 0x40014032	DSI0_HC51: 0x40014033
DSI0_HC52: 0x40014034	DSI0_HC53: 0x40014035
DSI0_HC54: 0x40014036	DSI0_HC55: 0x40014037
DSI0_HC56: 0x40014038	DSI0_HC57: 0x40014039
DSI0_HC58: 0x4001403A	DSI0_HC59: 0x4001403B
DSI0_HC60: 0x4001403C	DSI0_HC61: 0x4001403D
DSI0_HC62: 0x4001403E	DSI0_HC63: 0x4001403F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI0_HC64: 0x40014040
DSI0_HC65: 0x40014041
DSI0_HC66: 0x40014042
DSI0_HC67: 0x40014043
DSI0_HC68: 0x40014044
DSI0_HC69: 0x40014045
DSI0_HC70: 0x40014046
DSI0_HC71: 0x40014047
DSI0_HC72: 0x40014048
DSI0_HC73: 0x40014049
DSI0_HC74: 0x4001404A
DSI0_HC75: 0x4001404B
DSI0_HC76: 0x4001404C
DSI0_HC77: 0x4001404D
DSI0_HC78: 0x4001404E
DSI0_HC79: 0x4001404F
DSI0_HC80: 0x40014050
DSI0_HC81: 0x40014051
DSI0_HC82: 0x40014052
DSI0_HC83: 0x40014053
DSI0_HC84: 0x40014054
DSI0_HC85: 0x40014055
DSI0_HC86: 0x40014056
DSI0_HC87: 0x40014057
DSI0_HC88: 0x40014058
DSI0_HC89: 0x40014059
DSI0_HC90: 0x4001405A
DSI0_HC91: 0x4001405B
DSI0_HC92: 0x4001405C
DSI0_HC93: 0x4001405D
DSI0_HC94: 0x4001405E
DSI0_HC95: 0x4001405F
DSI0_HC96: 0x40014060
DSI0_HC97: 0x40014061
DSI0_HC98: 0x40014062
DSI0_HC99: 0x40014063
DSI0_HC100: 0x40014064
DSI0_HC101: 0x40014065
DSI0_HC102: 0x40014066
DSI0_HC103: 0x40014067
DSI0_HC104: 0x40014068
DSI0_HC105: 0x40014069
DSI0_HC106: 0x4001406A
DSI0_HC107: 0x4001406B
DSI0_HC108: 0x4001406C
DSI0_HC109: 0x4001406D
DSI0_HC110: 0x4001406E
DSI0_HC111: 0x4001406F
DSI0_HC112: 0x40014070
DSI0_HC113: 0x40014071
DSI0_HC114: 0x40014072
DSI0_HC115: 0x40014073
DSI0_HC116: 0x40014074
DSI0_HC117: 0x40014075
DSI0_HC118: 0x40014076
DSI0_HC119: 0x40014077
DSI0_HC120: 0x40014078
DSI0_HC121: 0x40014079
DSI0_HC122: 0x4001407A
DSI0_HC123: 0x4001407B
DSI0_HC124: 0x4001407C
DSI0_HC125: 0x4001407D
DSI0_HC126: 0x4001407E
DSI0_HC127: 0x4001407F
DSI1_HC0: 0x40014100
DSI1_HC1: 0x40014101
DSI1_HC2: 0x40014102
DSI1_HC3: 0x40014103
DSI1_HC4: 0x40014104
DSI1_HC5: 0x40014105
DSI1_HC6: 0x40014106
DSI1_HC7: 0x40014107

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI1_HC8: 0x40014108	DSI1_HC9: 0x40014109
DSI1_HC10: 0x4001410A	DSI1_HC11: 0x4001410B
DSI1_HC12: 0x4001410C	DSI1_HC13: 0x4001410D
DSI1_HC14: 0x4001410E	DSI1_HC15: 0x4001410F
DSI1_HC16: 0x40014110	DSI1_HC17: 0x40014111
DSI1_HC18: 0x40014112	DSI1_HC19: 0x40014113
DSI1_HC20: 0x40014114	DSI1_HC21: 0x40014115
DSI1_HC22: 0x40014116	DSI1_HC23: 0x40014117
DSI1_HC24: 0x40014118	DSI1_HC25: 0x40014119
DSI1_HC26: 0x4001411A	DSI1_HC27: 0x4001411B
DSI1_HC28: 0x4001411C	DSI1_HC29: 0x4001411D
DSI1_HC30: 0x4001411E	DSI1_HC31: 0x4001411F
DSI1_HC32: 0x40014120	DSI1_HC33: 0x40014121
DSI1_HC34: 0x40014122	DSI1_HC35: 0x40014123
DSI1_HC36: 0x40014124	DSI1_HC37: 0x40014125
DSI1_HC38: 0x40014126	DSI1_HC39: 0x40014127
DSI1_HC40: 0x40014128	DSI1_HC41: 0x40014129
DSI1_HC42: 0x4001412A	DSI1_HC43: 0x4001412B
DSI1_HC44: 0x4001412C	DSI1_HC45: 0x4001412D
DSI1_HC46: 0x4001412E	DSI1_HC47: 0x4001412F
DSI1_HC48: 0x40014130	DSI1_HC49: 0x40014131
DSI1_HC50: 0x40014132	DSI1_HC51: 0x40014133
DSI1_HC52: 0x40014134	DSI1_HC53: 0x40014135
DSI1_HC54: 0x40014136	DSI1_HC55: 0x40014137
DSI1_HC56: 0x40014138	DSI1_HC57: 0x40014139
DSI1_HC58: 0x4001413A	DSI1_HC59: 0x4001413B
DSI1_HC60: 0x4001413C	DSI1_HC61: 0x4001413D
DSI1_HC62: 0x4001413E	DSI1_HC63: 0x4001413F
DSI1_HC64: 0x40014140	DSI1_HC65: 0x40014141
DSI1_HC66: 0x40014142	DSI1_HC67: 0x40014143
DSI1_HC68: 0x40014144	DSI1_HC69: 0x40014145
DSI1_HC70: 0x40014146	DSI1_HC71: 0x40014147
DSI1_HC72: 0x40014148	DSI1_HC73: 0x40014149
DSI1_HC74: 0x4001414A	DSI1_HC75: 0x4001414B
DSI1_HC76: 0x4001414C	DSI1_HC77: 0x4001414D
DSI1_HC78: 0x4001414E	DSI1_HC79: 0x4001414F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI1_HC80: 0x40014150	DSI1_HC81: 0x40014151
DSI1_HC82: 0x40014152	DSI1_HC83: 0x40014153
DSI1_HC84: 0x40014154	DSI1_HC85: 0x40014155
DSI1_HC86: 0x40014156	DSI1_HC87: 0x40014157
DSI1_HC88: 0x40014158	DSI1_HC89: 0x40014159
DSI1_HC90: 0x4001415A	DSI1_HC91: 0x4001415B
DSI1_HC92: 0x4001415C	DSI1_HC93: 0x4001415D
DSI1_HC94: 0x4001415E	DSI1_HC95: 0x4001415F
DSI1_HC96: 0x40014160	DSI1_HC97: 0x40014161
DSI1_HC98: 0x40014162	DSI1_HC99: 0x40014163
DSI1_HC100: 0x40014164	DSI1_HC101: 0x40014165
DSI1_HC102: 0x40014166	DSI1_HC103: 0x40014167
DSI1_HC104: 0x40014168	DSI1_HC105: 0x40014169
DSI1_HC106: 0x4001416A	DSI1_HC107: 0x4001416B
DSI1_HC108: 0x4001416C	DSI1_HC109: 0x4001416D
DSI1_HC110: 0x4001416E	DSI1_HC111: 0x4001416F
DSI1_HC112: 0x40014170	DSI1_HC113: 0x40014171
DSI1_HC114: 0x40014172	DSI1_HC115: 0x40014173
DSI1_HC116: 0x40014174	DSI1_HC117: 0x40014175
DSI1_HC118: 0x40014176	DSI1_HC119: 0x40014177
DSI1_HC120: 0x40014178	DSI1_HC121: 0x40014179
DSI1_HC122: 0x4001417A	DSI1_HC123: 0x4001417B
DSI1_HC124: 0x4001417C	DSI1_HC125: 0x4001417D
DSI1_HC126: 0x4001417E	DSI1_HC127: 0x4001417F
DSI2_HC0: 0x40014200	DSI2_HC1: 0x40014201
DSI2_HC2: 0x40014202	DSI2_HC3: 0x40014203
DSI2_HC4: 0x40014204	DSI2_HC5: 0x40014205
DSI2_HC6: 0x40014206	DSI2_HC7: 0x40014207
DSI2_HC8: 0x40014208	DSI2_HC9: 0x40014209
DSI2_HC10: 0x4001420A	DSI2_HC11: 0x4001420B
DSI2_HC12: 0x4001420C	DSI2_HC13: 0x4001420D
DSI2_HC14: 0x4001420E	DSI2_HC15: 0x4001420F
DSI2_HC16: 0x40014210	DSI2_HC17: 0x40014211
DSI2_HC18: 0x40014212	DSI2_HC19: 0x40014213
DSI2_HC20: 0x40014214	DSI2_HC21: 0x40014215
DSI2_HC22: 0x40014216	DSI2_HC23: 0x40014217

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI2_HC24: 0x40014218	DSI2_HC25: 0x40014219
DSI2_HC26: 0x4001421A	DSI2_HC27: 0x4001421B
DSI2_HC28: 0x4001421C	DSI2_HC29: 0x4001421D
DSI2_HC30: 0x4001421E	DSI2_HC31: 0x4001421F
DSI2_HC32: 0x40014220	DSI2_HC33: 0x40014221
DSI2_HC34: 0x40014222	DSI2_HC35: 0x40014223
DSI2_HC36: 0x40014224	DSI2_HC37: 0x40014225
DSI2_HC38: 0x40014226	DSI2_HC39: 0x40014227
DSI2_HC40: 0x40014228	DSI2_HC41: 0x40014229
DSI2_HC42: 0x4001422A	DSI2_HC43: 0x4001422B
DSI2_HC44: 0x4001422C	DSI2_HC45: 0x4001422D
DSI2_HC46: 0x4001422E	DSI2_HC47: 0x4001422F
DSI2_HC48: 0x40014230	DSI2_HC49: 0x40014231
DSI2_HC50: 0x40014232	DSI2_HC51: 0x40014233
DSI2_HC52: 0x40014234	DSI2_HC53: 0x40014235
DSI2_HC54: 0x40014236	DSI2_HC55: 0x40014237
DSI2_HC56: 0x40014238	DSI2_HC57: 0x40014239
DSI2_HC58: 0x4001423A	DSI2_HC59: 0x4001423B
DSI2_HC60: 0x4001423C	DSI2_HC61: 0x4001423D
DSI2_HC62: 0x4001423E	DSI2_HC63: 0x4001423F
DSI2_HC64: 0x40014240	DSI2_HC65: 0x40014241
DSI2_HC66: 0x40014242	DSI2_HC67: 0x40014243
DSI2_HC68: 0x40014244	DSI2_HC69: 0x40014245
DSI2_HC70: 0x40014246	DSI2_HC71: 0x40014247
DSI2_HC72: 0x40014248	DSI2_HC73: 0x40014249
DSI2_HC74: 0x4001424A	DSI2_HC75: 0x4001424B
DSI2_HC76: 0x4001424C	DSI2_HC77: 0x4001424D
DSI2_HC78: 0x4001424E	DSI2_HC79: 0x4001424F
DSI2_HC80: 0x40014250	DSI2_HC81: 0x40014251
DSI2_HC82: 0x40014252	DSI2_HC83: 0x40014253
DSI2_HC84: 0x40014254	DSI2_HC85: 0x40014255
DSI2_HC86: 0x40014256	DSI2_HC87: 0x40014257
DSI2_HC88: 0x40014258	DSI2_HC89: 0x40014259
DSI2_HC90: 0x4001425A	DSI2_HC91: 0x4001425B
DSI2_HC92: 0x4001425C	DSI2_HC93: 0x4001425D
DSI2_HC94: 0x4001425E	DSI2_HC95: 0x4001425F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI2_HC96: 0x40014260
DSI2_HC97: 0x40014261
DSI2_HC98: 0x40014262
DSI2_HC99: 0x40014263
DSI2_HC100: 0x40014264
DSI2_HC101: 0x40014265
DSI2_HC102: 0x40014266
DSI2_HC103: 0x40014267
DSI2_HC104: 0x40014268
DSI2_HC105: 0x40014269
DSI2_HC106: 0x4001426A
DSI2_HC107: 0x4001426B
DSI2_HC108: 0x4001426C
DSI2_HC109: 0x4001426D
DSI2_HC110: 0x4001426E
DSI2_HC111: 0x4001426F
DSI2_HC112: 0x40014270
DSI2_HC113: 0x40014271
DSI2_HC114: 0x40014272
DSI2_HC115: 0x40014273
DSI2_HC116: 0x40014274
DSI2_HC117: 0x40014275
DSI2_HC118: 0x40014276
DSI2_HC119: 0x40014277
DSI2_HC120: 0x40014278
DSI2_HC121: 0x40014279
DSI2_HC122: 0x4001427A
DSI2_HC123: 0x4001427B
DSI2_HC124: 0x4001427C
DSI2_HC125: 0x4001427D
DSI2_HC126: 0x4001427E
DSI2_HC127: 0x4001427F
DSI3_HC0: 0x40014300
DSI3_HC1: 0x40014301
DSI3_HC2: 0x40014302
DSI3_HC3: 0x40014303
DSI3_HC4: 0x40014304
DSI3_HC5: 0x40014305
DSI3_HC6: 0x40014306
DSI3_HC7: 0x40014307
DSI3_HC8: 0x40014308
DSI3_HC9: 0x40014309
DSI3_HC10: 0x4001430A
DSI3_HC11: 0x4001430B
DSI3_HC12: 0x4001430C
DSI3_HC13: 0x4001430D
DSI3_HC14: 0x4001430E
DSI3_HC15: 0x4001430F
DSI3_HC16: 0x40014310
DSI3_HC17: 0x40014311
DSI3_HC18: 0x40014312
DSI3_HC19: 0x40014313
DSI3_HC20: 0x40014314
DSI3_HC21: 0x40014315
DSI3_HC22: 0x40014316
DSI3_HC23: 0x40014317
DSI3_HC24: 0x40014318
DSI3_HC25: 0x40014319
DSI3_HC26: 0x4001431A
DSI3_HC27: 0x4001431B
DSI3_HC28: 0x4001431C
DSI3_HC29: 0x4001431D
DSI3_HC30: 0x4001431E
DSI3_HC31: 0x4001431F
DSI3_HC32: 0x40014320
DSI3_HC33: 0x40014321
DSI3_HC34: 0x40014322
DSI3_HC35: 0x40014323
DSI3_HC36: 0x40014324
DSI3_HC37: 0x40014325
DSI3_HC38: 0x40014326
DSI3_HC39: 0x40014327

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI3_HC40: 0x40014328
DSI3_HC41: 0x40014329
DSI3_HC42: 0x4001432A
DSI3_HC43: 0x4001432B
DSI3_HC44: 0x4001432C
DSI3_HC45: 0x4001432D
DSI3_HC46: 0x4001432E
DSI3_HC47: 0x4001432F
DSI3_HC48: 0x40014330
DSI3_HC49: 0x40014331
DSI3_HC50: 0x40014332
DSI3_HC51: 0x40014333
DSI3_HC52: 0x40014334
DSI3_HC53: 0x40014335
DSI3_HC54: 0x40014336
DSI3_HC55: 0x40014337
DSI3_HC56: 0x40014338
DSI3_HC57: 0x40014339
DSI3_HC58: 0x4001433A
DSI3_HC59: 0x4001433B
DSI3_HC60: 0x4001433C
DSI3_HC61: 0x4001433D
DSI3_HC62: 0x4001433E
DSI3_HC63: 0x4001433F
DSI3_HC64: 0x40014340
DSI3_HC65: 0x40014341
DSI3_HC66: 0x40014342
DSI3_HC67: 0x40014343
DSI3_HC68: 0x40014344
DSI3_HC69: 0x40014345
DSI3_HC70: 0x40014346
DSI3_HC71: 0x40014347
DSI3_HC72: 0x40014348
DSI3_HC73: 0x40014349
DSI3_HC74: 0x4001434A
DSI3_HC75: 0x4001434B
DSI3_HC76: 0x4001434C
DSI3_HC77: 0x4001434D
DSI3_HC78: 0x4001434E
DSI3_HC79: 0x4001434F
DSI3_HC80: 0x40014350
DSI3_HC81: 0x40014351
DSI3_HC82: 0x40014352
DSI3_HC83: 0x40014353
DSI3_HC84: 0x40014354
DSI3_HC85: 0x40014355
DSI3_HC86: 0x40014356
DSI3_HC87: 0x40014357
DSI3_HC88: 0x40014358
DSI3_HC89: 0x40014359
DSI3_HC90: 0x4001435A
DSI3_HC91: 0x4001435B
DSI3_HC92: 0x4001435C
DSI3_HC93: 0x4001435D
DSI3_HC94: 0x4001435E
DSI3_HC95: 0x4001435F
DSI3_HC96: 0x40014360
DSI3_HC97: 0x40014361
DSI3_HC98: 0x40014362
DSI3_HC99: 0x40014363
DSI3_HC100: 0x40014364
DSI3_HC101: 0x40014365
DSI3_HC102: 0x40014366
DSI3_HC103: 0x40014367
DSI3_HC104: 0x40014368
DSI3_HC105: 0x40014369
DSI3_HC106: 0x4001436A
DSI3_HC107: 0x4001436B
DSI3_HC108: 0x4001436C
DSI3_HC109: 0x4001436D
DSI3_HC110: 0x4001436E
DSI3_HC111: 0x4001436F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI3_HC112: 0x40014370	DSI3_HC113: 0x40014371
DSI3_HC114: 0x40014372	DSI3_HC115: 0x40014373
DSI3_HC116: 0x40014374	DSI3_HC117: 0x40014375
DSI3_HC118: 0x40014376	DSI3_HC119: 0x40014377
DSI3_HC120: 0x40014378	DSI3_HC121: 0x40014379
DSI3_HC122: 0x4001437A	DSI3_HC123: 0x4001437B
DSI3_HC124: 0x4001437C	DSI3_HC125: 0x4001437D
DSI3_HC126: 0x4001437E	DSI3_HC127: 0x4001437F
DSI4_HC0: 0x40014400	DSI4_HC1: 0x40014401
DSI4_HC2: 0x40014402	DSI4_HC3: 0x40014403
DSI4_HC4: 0x40014404	DSI4_HC5: 0x40014405
DSI4_HC6: 0x40014406	DSI4_HC7: 0x40014407
DSI4_HC8: 0x40014408	DSI4_HC9: 0x40014409
DSI4_HC10: 0x4001440A	DSI4_HC11: 0x4001440B
DSI4_HC12: 0x4001440C	DSI4_HC13: 0x4001440D
DSI4_HC14: 0x4001440E	DSI4_HC15: 0x4001440F
DSI4_HC16: 0x40014410	DSI4_HC17: 0x40014411
DSI4_HC18: 0x40014412	DSI4_HC19: 0x40014413
DSI4_HC20: 0x40014414	DSI4_HC21: 0x40014415
DSI4_HC22: 0x40014416	DSI4_HC23: 0x40014417
DSI4_HC24: 0x40014418	DSI4_HC25: 0x40014419
DSI4_HC26: 0x4001441A	DSI4_HC27: 0x4001441B
DSI4_HC28: 0x4001441C	DSI4_HC29: 0x4001441D
DSI4_HC30: 0x4001441E	DSI4_HC31: 0x4001441F
DSI4_HC32: 0x40014420	DSI4_HC33: 0x40014421
DSI4_HC34: 0x40014422	DSI4_HC35: 0x40014423
DSI4_HC36: 0x40014424	DSI4_HC37: 0x40014425
DSI4_HC38: 0x40014426	DSI4_HC39: 0x40014427
DSI4_HC40: 0x40014428	DSI4_HC41: 0x40014429
DSI4_HC42: 0x4001442A	DSI4_HC43: 0x4001442B
DSI4_HC44: 0x4001442C	DSI4_HC45: 0x4001442D
DSI4_HC46: 0x4001442E	DSI4_HC47: 0x4001442F
DSI4_HC48: 0x40014430	DSI4_HC49: 0x40014431
DSI4_HC50: 0x40014432	DSI4_HC51: 0x40014433
DSI4_HC52: 0x40014434	DSI4_HC53: 0x40014435
DSI4_HC54: 0x40014436	DSI4_HC55: 0x40014437

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI4_HC56: 0x40014438	DSI4_HC57: 0x40014439
DSI4_HC58: 0x4001443A	DSI4_HC59: 0x4001443B
DSI4_HC60: 0x4001443C	DSI4_HC61: 0x4001443D
DSI4_HC62: 0x4001443E	DSI4_HC63: 0x4001443F
DSI4_HC64: 0x40014440	DSI4_HC65: 0x40014441
DSI4_HC66: 0x40014442	DSI4_HC67: 0x40014443
DSI4_HC68: 0x40014444	DSI4_HC69: 0x40014445
DSI4_HC70: 0x40014446	DSI4_HC71: 0x40014447
DSI4_HC72: 0x40014448	DSI4_HC73: 0x40014449
DSI4_HC74: 0x4001444A	DSI4_HC75: 0x4001444B
DSI4_HC76: 0x4001444C	DSI4_HC77: 0x4001444D
DSI4_HC78: 0x4001444E	DSI4_HC79: 0x4001444F
DSI4_HC80: 0x40014450	DSI4_HC81: 0x40014451
DSI4_HC82: 0x40014452	DSI4_HC83: 0x40014453
DSI4_HC84: 0x40014454	DSI4_HC85: 0x40014455
DSI4_HC86: 0x40014456	DSI4_HC87: 0x40014457
DSI4_HC88: 0x40014458	DSI4_HC89: 0x40014459
DSI4_HC90: 0x4001445A	DSI4_HC91: 0x4001445B
DSI4_HC92: 0x4001445C	DSI4_HC93: 0x4001445D
DSI4_HC94: 0x4001445E	DSI4_HC95: 0x4001445F
DSI4_HC96: 0x40014460	DSI4_HC97: 0x40014461
DSI4_HC98: 0x40014462	DSI4_HC99: 0x40014463
DSI4_HC100: 0x40014464	DSI4_HC101: 0x40014465
DSI4_HC102: 0x40014466	DSI4_HC103: 0x40014467
DSI4_HC104: 0x40014468	DSI4_HC105: 0x40014469
DSI4_HC106: 0x4001446A	DSI4_HC107: 0x4001446B
DSI4_HC108: 0x4001446C	DSI4_HC109: 0x4001446D
DSI4_HC110: 0x4001446E	DSI4_HC111: 0x4001446F
DSI4_HC112: 0x40014470	DSI4_HC113: 0x40014471
DSI4_HC114: 0x40014472	DSI4_HC115: 0x40014473
DSI4_HC116: 0x40014474	DSI4_HC117: 0x40014475
DSI4_HC118: 0x40014476	DSI4_HC119: 0x40014477
DSI4_HC120: 0x40014478	DSI4_HC121: 0x40014479
DSI4_HC122: 0x4001447A	DSI4_HC123: 0x4001447B
DSI4_HC124: 0x4001447C	DSI4_HC125: 0x4001447D
DSI4_HC126: 0x4001447E	DSI4_HC127: 0x4001447F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI5_HC0: 0x40014500	DSI5_HC1: 0x40014501
DSI5_HC2: 0x40014502	DSI5_HC3: 0x40014503
DSI5_HC4: 0x40014504	DSI5_HC5: 0x40014505
DSI5_HC6: 0x40014506	DSI5_HC7: 0x40014507
DSI5_HC8: 0x40014508	DSI5_HC9: 0x40014509
DSI5_HC10: 0x4001450A	DSI5_HC11: 0x4001450B
DSI5_HC12: 0x4001450C	DSI5_HC13: 0x4001450D
DSI5_HC14: 0x4001450E	DSI5_HC15: 0x4001450F
DSI5_HC16: 0x40014510	DSI5_HC17: 0x40014511
DSI5_HC18: 0x40014512	DSI5_HC19: 0x40014513
DSI5_HC20: 0x40014514	DSI5_HC21: 0x40014515
DSI5_HC22: 0x40014516	DSI5_HC23: 0x40014517
DSI5_HC24: 0x40014518	DSI5_HC25: 0x40014519
DSI5_HC26: 0x4001451A	DSI5_HC27: 0x4001451B
DSI5_HC28: 0x4001451C	DSI5_HC29: 0x4001451D
DSI5_HC30: 0x4001451E	DSI5_HC31: 0x4001451F
DSI5_HC32: 0x40014520	DSI5_HC33: 0x40014521
DSI5_HC34: 0x40014522	DSI5_HC35: 0x40014523
DSI5_HC36: 0x40014524	DSI5_HC37: 0x40014525
DSI5_HC38: 0x40014526	DSI5_HC39: 0x40014527
DSI5_HC40: 0x40014528	DSI5_HC41: 0x40014529
DSI5_HC42: 0x4001452A	DSI5_HC43: 0x4001452B
DSI5_HC44: 0x4001452C	DSI5_HC45: 0x4001452D
DSI5_HC46: 0x4001452E	DSI5_HC47: 0x4001452F
DSI5_HC48: 0x40014530	DSI5_HC49: 0x40014531
DSI5_HC50: 0x40014532	DSI5_HC51: 0x40014533
DSI5_HC52: 0x40014534	DSI5_HC53: 0x40014535
DSI5_HC54: 0x40014536	DSI5_HC55: 0x40014537
DSI5_HC56: 0x40014538	DSI5_HC57: 0x40014539
DSI5_HC58: 0x4001453A	DSI5_HC59: 0x4001453B
DSI5_HC60: 0x4001453C	DSI5_HC61: 0x4001453D
DSI5_HC62: 0x4001453E	DSI5_HC63: 0x4001453F
DSI5_HC64: 0x40014540	DSI5_HC65: 0x40014541
DSI5_HC66: 0x40014542	DSI5_HC67: 0x40014543
DSI5_HC68: 0x40014544	DSI5_HC69: 0x40014545
DSI5_HC70: 0x40014546	DSI5_HC71: 0x40014547

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI5_HC72: 0x40014548
DSI5_HC73: 0x40014549
DSI5_HC74: 0x4001454A
DSI5_HC75: 0x4001454B
DSI5_HC76: 0x4001454C
DSI5_HC77: 0x4001454D
DSI5_HC78: 0x4001454E
DSI5_HC79: 0x4001454F
DSI5_HC80: 0x40014550
DSI5_HC81: 0x40014551
DSI5_HC82: 0x40014552
DSI5_HC83: 0x40014553
DSI5_HC84: 0x40014554
DSI5_HC85: 0x40014555
DSI5_HC86: 0x40014556
DSI5_HC87: 0x40014557
DSI5_HC88: 0x40014558
DSI5_HC89: 0x40014559
DSI5_HC90: 0x4001455A
DSI5_HC91: 0x4001455B
DSI5_HC92: 0x4001455C
DSI5_HC93: 0x4001455D
DSI5_HC94: 0x4001455E
DSI5_HC95: 0x4001455F
DSI5_HC96: 0x40014560
DSI5_HC97: 0x40014561
DSI5_HC98: 0x40014562
DSI5_HC99: 0x40014563
DSI5_HC100: 0x40014564
DSI5_HC101: 0x40014565
DSI5_HC102: 0x40014566
DSI5_HC103: 0x40014567
DSI5_HC104: 0x40014568
DSI5_HC105: 0x40014569
DSI5_HC106: 0x4001456A
DSI5_HC107: 0x4001456B
DSI5_HC108: 0x4001456C
DSI5_HC109: 0x4001456D
DSI5_HC110: 0x4001456E
DSI5_HC111: 0x4001456F
DSI5_HC112: 0x40014570
DSI5_HC113: 0x40014571
DSI5_HC114: 0x40014572
DSI5_HC115: 0x40014573
DSI5_HC116: 0x40014574
DSI5_HC117: 0x40014575
DSI5_HC118: 0x40014576
DSI5_HC119: 0x40014577
DSI5_HC120: 0x40014578
DSI5_HC121: 0x40014579
DSI5_HC122: 0x4001457A
DSI5_HC123: 0x4001457B
DSI5_HC124: 0x4001457C
DSI5_HC125: 0x4001457D
DSI5_HC126: 0x4001457E
DSI5_HC127: 0x4001457F
DSI6_HC0: 0x40014600
DSI6_HC1: 0x40014601
DSI6_HC2: 0x40014602
DSI6_HC3: 0x40014603
DSI6_HC4: 0x40014604
DSI6_HC5: 0x40014605
DSI6_HC6: 0x40014606
DSI6_HC7: 0x40014607
DSI6_HC8: 0x40014608
DSI6_HC9: 0x40014609
DSI6_HC10: 0x4001460A
DSI6_HC11: 0x4001460B
DSI6_HC12: 0x4001460C
DSI6_HC13: 0x4001460D
DSI6_HC14: 0x4001460E
DSI6_HC15: 0x4001460F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI6_HC16: 0x40014610	DSI6_HC17: 0x40014611
DSI6_HC18: 0x40014612	DSI6_HC19: 0x40014613
DSI6_HC20: 0x40014614	DSI6_HC21: 0x40014615
DSI6_HC22: 0x40014616	DSI6_HC23: 0x40014617
DSI6_HC24: 0x40014618	DSI6_HC25: 0x40014619
DSI6_HC26: 0x4001461A	DSI6_HC27: 0x4001461B
DSI6_HC28: 0x4001461C	DSI6_HC29: 0x4001461D
DSI6_HC30: 0x4001461E	DSI6_HC31: 0x4001461F
DSI6_HC32: 0x40014620	DSI6_HC33: 0x40014621
DSI6_HC34: 0x40014622	DSI6_HC35: 0x40014623
DSI6_HC36: 0x40014624	DSI6_HC37: 0x40014625
DSI6_HC38: 0x40014626	DSI6_HC39: 0x40014627
DSI6_HC40: 0x40014628	DSI6_HC41: 0x40014629
DSI6_HC42: 0x4001462A	DSI6_HC43: 0x4001462B
DSI6_HC44: 0x4001462C	DSI6_HC45: 0x4001462D
DSI6_HC46: 0x4001462E	DSI6_HC47: 0x4001462F
DSI6_HC48: 0x40014630	DSI6_HC49: 0x40014631
DSI6_HC50: 0x40014632	DSI6_HC51: 0x40014633
DSI6_HC52: 0x40014634	DSI6_HC53: 0x40014635
DSI6_HC54: 0x40014636	DSI6_HC55: 0x40014637
DSI6_HC56: 0x40014638	DSI6_HC57: 0x40014639
DSI6_HC58: 0x4001463A	DSI6_HC59: 0x4001463B
DSI6_HC60: 0x4001463C	DSI6_HC61: 0x4001463D
DSI6_HC62: 0x4001463E	DSI6_HC63: 0x4001463F
DSI6_HC64: 0x40014640	DSI6_HC65: 0x40014641
DSI6_HC66: 0x40014642	DSI6_HC67: 0x40014643
DSI6_HC68: 0x40014644	DSI6_HC69: 0x40014645
DSI6_HC70: 0x40014646	DSI6_HC71: 0x40014647
DSI6_HC72: 0x40014648	DSI6_HC73: 0x40014649
DSI6_HC74: 0x4001464A	DSI6_HC75: 0x4001464B
DSI6_HC76: 0x4001464C	DSI6_HC77: 0x4001464D
DSI6_HC78: 0x4001464E	DSI6_HC79: 0x4001464F
DSI6_HC80: 0x40014650	DSI6_HC81: 0x40014651
DSI6_HC82: 0x40014652	DSI6_HC83: 0x40014653
DSI6_HC84: 0x40014654	DSI6_HC85: 0x40014655
DSI6_HC86: 0x40014656	DSI6_HC87: 0x40014657

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI6_HC88: 0x40014658
DSI6_HC89: 0x40014659
DSI6_HC90: 0x4001465A
DSI6_HC91: 0x4001465B
DSI6_HC92: 0x4001465C
DSI6_HC93: 0x4001465D
DSI6_HC94: 0x4001465E
DSI6_HC95: 0x4001465F
DSI6_HC96: 0x40014660
DSI6_HC97: 0x40014661
DSI6_HC98: 0x40014662
DSI6_HC99: 0x40014663
DSI6_HC100: 0x40014664
DSI6_HC101: 0x40014665
DSI6_HC102: 0x40014666
DSI6_HC103: 0x40014667
DSI6_HC104: 0x40014668
DSI6_HC105: 0x40014669
DSI6_HC106: 0x4001466A
DSI6_HC107: 0x4001466B
DSI6_HC108: 0x4001466C
DSI6_HC109: 0x4001466D
DSI6_HC110: 0x4001466E
DSI6_HC111: 0x4001466F
DSI6_HC112: 0x40014670
DSI6_HC113: 0x40014671
DSI6_HC114: 0x40014672
DSI6_HC115: 0x40014673
DSI6_HC116: 0x40014674
DSI6_HC117: 0x40014675
DSI6_HC118: 0x40014676
DSI6_HC119: 0x40014677
DSI6_HC120: 0x40014678
DSI6_HC121: 0x40014679
DSI6_HC122: 0x4001467A
DSI6_HC123: 0x4001467B
DSI6_HC124: 0x4001467C
DSI6_HC125: 0x4001467D
DSI6_HC126: 0x4001467E
DSI6_HC127: 0x4001467F
DSI7_HC0: 0x40014700
DSI7_HC1: 0x40014701
DSI7_HC2: 0x40014702
DSI7_HC3: 0x40014703
DSI7_HC4: 0x40014704
DSI7_HC5: 0x40014705
DSI7_HC6: 0x40014706
DSI7_HC7: 0x40014707
DSI7_HC8: 0x40014708
DSI7_HC9: 0x40014709
DSI7_HC10: 0x4001470A
DSI7_HC11: 0x4001470B
DSI7_HC12: 0x4001470C
DSI7_HC13: 0x4001470D
DSI7_HC14: 0x4001470E
DSI7_HC15: 0x4001470F
DSI7_HC16: 0x40014710
DSI7_HC17: 0x40014711
DSI7_HC18: 0x40014712
DSI7_HC19: 0x40014713
DSI7_HC20: 0x40014714
DSI7_HC21: 0x40014715
DSI7_HC22: 0x40014716
DSI7_HC23: 0x40014717
DSI7_HC24: 0x40014718
DSI7_HC25: 0x40014719
DSI7_HC26: 0x4001471A
DSI7_HC27: 0x4001471B
DSI7_HC28: 0x4001471C
DSI7_HC29: 0x4001471D
DSI7_HC30: 0x4001471E
DSI7_HC31: 0x4001471F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI7_HC32: 0x40014720	DSI7_HC33: 0x40014721
DSI7_HC34: 0x40014722	DSI7_HC35: 0x40014723
DSI7_HC36: 0x40014724	DSI7_HC37: 0x40014725
DSI7_HC38: 0x40014726	DSI7_HC39: 0x40014727
DSI7_HC40: 0x40014728	DSI7_HC41: 0x40014729
DSI7_HC42: 0x4001472A	DSI7_HC43: 0x4001472B
DSI7_HC44: 0x4001472C	DSI7_HC45: 0x4001472D
DSI7_HC46: 0x4001472E	DSI7_HC47: 0x4001472F
DSI7_HC48: 0x40014730	DSI7_HC49: 0x40014731
DSI7_HC50: 0x40014732	DSI7_HC51: 0x40014733
DSI7_HC52: 0x40014734	DSI7_HC53: 0x40014735
DSI7_HC54: 0x40014736	DSI7_HC55: 0x40014737
DSI7_HC56: 0x40014738	DSI7_HC57: 0x40014739
DSI7_HC58: 0x4001473A	DSI7_HC59: 0x4001473B
DSI7_HC60: 0x4001473C	DSI7_HC61: 0x4001473D
DSI7_HC62: 0x4001473E	DSI7_HC63: 0x4001473F
DSI7_HC64: 0x40014740	DSI7_HC65: 0x40014741
DSI7_HC66: 0x40014742	DSI7_HC67: 0x40014743
DSI7_HC68: 0x40014744	DSI7_HC69: 0x40014745
DSI7_HC70: 0x40014746	DSI7_HC71: 0x40014747
DSI7_HC72: 0x40014748	DSI7_HC73: 0x40014749
DSI7_HC74: 0x4001474A	DSI7_HC75: 0x4001474B
DSI7_HC76: 0x4001474C	DSI7_HC77: 0x4001474D
DSI7_HC78: 0x4001474E	DSI7_HC79: 0x4001474F
DSI7_HC80: 0x40014750	DSI7_HC81: 0x40014751
DSI7_HC82: 0x40014752	DSI7_HC83: 0x40014753
DSI7_HC84: 0x40014754	DSI7_HC85: 0x40014755
DSI7_HC86: 0x40014756	DSI7_HC87: 0x40014757
DSI7_HC88: 0x40014758	DSI7_HC89: 0x40014759
DSI7_HC90: 0x4001475A	DSI7_HC91: 0x4001475B
DSI7_HC92: 0x4001475C	DSI7_HC93: 0x4001475D
DSI7_HC94: 0x4001475E	DSI7_HC95: 0x4001475F
DSI7_HC96: 0x40014760	DSI7_HC97: 0x40014761
DSI7_HC98: 0x40014762	DSI7_HC99: 0x40014763
DSI7_HC100: 0x40014764	DSI7_HC101: 0x40014765
DSI7_HC102: 0x40014766	DSI7_HC103: 0x40014767

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI7_HC104: 0x40014768
DSI7_HC105: 0x40014769
DSI7_HC106: 0x4001476A
DSI7_HC107: 0x4001476B
DSI7_HC108: 0x4001476C
DSI7_HC109: 0x4001476D
DSI7_HC110: 0x4001476E
DSI7_HC111: 0x4001476F
DSI7_HC112: 0x40014770
DSI7_HC113: 0x40014771
DSI7_HC114: 0x40014772
DSI7_HC115: 0x40014773
DSI7_HC116: 0x40014774
DSI7_HC117: 0x40014775
DSI7_HC118: 0x40014776
DSI7_HC119: 0x40014777
DSI7_HC120: 0x40014778
DSI7_HC121: 0x40014779
DSI7_HC122: 0x4001477A
DSI7_HC123: 0x4001477B
DSI7_HC124: 0x4001477C
DSI7_HC125: 0x4001477D
DSI7_HC126: 0x4001477E
DSI7_HC127: 0x4001477F
DSI8_HC0: 0x40014800
DSI8_HC1: 0x40014801
DSI8_HC2: 0x40014802
DSI8_HC3: 0x40014803
DSI8_HC4: 0x40014804
DSI8_HC5: 0x40014805
DSI8_HC6: 0x40014806
DSI8_HC7: 0x40014807
DSI8_HC8: 0x40014808
DSI8_HC9: 0x40014809
DSI8_HC10: 0x4001480A
DSI8_HC11: 0x4001480B
DSI8_HC12: 0x4001480C
DSI8_HC13: 0x4001480D
DSI8_HC14: 0x4001480E
DSI8_HC15: 0x4001480F
DSI8_HC16: 0x40014810
DSI8_HC17: 0x40014811
DSI8_HC18: 0x40014812
DSI8_HC19: 0x40014813
DSI8_HC20: 0x40014814
DSI8_HC21: 0x40014815
DSI8_HC22: 0x40014816
DSI8_HC23: 0x40014817
DSI8_HC24: 0x40014818
DSI8_HC25: 0x40014819
DSI8_HC26: 0x4001481A
DSI8_HC27: 0x4001481B
DSI8_HC28: 0x4001481C
DSI8_HC29: 0x4001481D
DSI8_HC30: 0x4001481E
DSI8_HC31: 0x4001481F
DSI8_HC32: 0x40014820
DSI8_HC33: 0x40014821
DSI8_HC34: 0x40014822
DSI8_HC35: 0x40014823
DSI8_HC36: 0x40014824
DSI8_HC37: 0x40014825
DSI8_HC38: 0x40014826
DSI8_HC39: 0x40014827
DSI8_HC40: 0x40014828
DSI8_HC41: 0x40014829
DSI8_HC42: 0x4001482A
DSI8_HC43: 0x4001482B
DSI8_HC44: 0x4001482C
DSI8_HC45: 0x4001482D
DSI8_HC46: 0x4001482E
DSI8_HC47: 0x4001482F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI8_HC48: 0x40014830
DSI8_HC49: 0x40014831
DSI8_HC50: 0x40014832
DSI8_HC51: 0x40014833
DSI8_HC52: 0x40014834
DSI8_HC53: 0x40014835
DSI8_HC54: 0x40014836
DSI8_HC55: 0x40014837
DSI8_HC56: 0x40014838
DSI8_HC57: 0x40014839
DSI8_HC58: 0x4001483A
DSI8_HC59: 0x4001483B
DSI8_HC60: 0x4001483C
DSI8_HC61: 0x4001483D
DSI8_HC62: 0x4001483E
DSI8_HC63: 0x4001483F
DSI8_HC64: 0x40014840
DSI8_HC65: 0x40014841
DSI8_HC66: 0x40014842
DSI8_HC67: 0x40014843
DSI8_HC68: 0x40014844
DSI8_HC69: 0x40014845
DSI8_HC70: 0x40014846
DSI8_HC71: 0x40014847
DSI8_HC72: 0x40014848
DSI8_HC73: 0x40014849
DSI8_HC74: 0x4001484A
DSI8_HC75: 0x4001484B
DSI8_HC76: 0x4001484C
DSI8_HC77: 0x4001484D
DSI8_HC78: 0x4001484E
DSI8_HC79: 0x4001484F
DSI8_HC80: 0x40014850
DSI8_HC81: 0x40014851
DSI8_HC82: 0x40014852
DSI8_HC83: 0x40014853
DSI8_HC84: 0x40014854
DSI8_HC85: 0x40014855
DSI8_HC86: 0x40014856
DSI8_HC87: 0x40014857
DSI8_HC88: 0x40014858
DSI8_HC89: 0x40014859
DSI8_HC90: 0x4001485A
DSI8_HC91: 0x4001485B
DSI8_HC92: 0x4001485C
DSI8_HC93: 0x4001485D
DSI8_HC94: 0x4001485E
DSI8_HC95: 0x4001485F
DSI8_HC96: 0x40014860
DSI8_HC97: 0x40014861
DSI8_HC98: 0x40014862
DSI8_HC99: 0x40014863
DSI8_HC100: 0x40014864
DSI8_HC101: 0x40014865
DSI8_HC102: 0x40014866
DSI8_HC103: 0x40014867
DSI8_HC104: 0x40014868
DSI8_HC105: 0x40014869
DSI8_HC106: 0x4001486A
DSI8_HC107: 0x4001486B
DSI8_HC108: 0x4001486C
DSI8_HC109: 0x4001486D
DSI8_HC110: 0x4001486E
DSI8_HC111: 0x4001486F
DSI8_HC112: 0x40014870
DSI8_HC113: 0x40014871
DSI8_HC114: 0x40014872
DSI8_HC115: 0x40014873
DSI8_HC116: 0x40014874
DSI8_HC117: 0x40014875
DSI8_HC118: 0x40014876
DSI8_HC119: 0x40014877

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI8_HC120: 0x40014878
DSI8_HC121: 0x40014879
DSI8_HC122: 0x4001487A
DSI8_HC123: 0x4001487B
DSI8_HC124: 0x4001487C
DSI8_HC125: 0x4001487D
DSI8_HC126: 0x4001487E
DSI8_HC127: 0x4001487F
DSI9_HC0: 0x40014900
DSI9_HC1: 0x40014901
DSI9_HC2: 0x40014902
DSI9_HC3: 0x40014903
DSI9_HC4: 0x40014904
DSI9_HC5: 0x40014905
DSI9_HC6: 0x40014906
DSI9_HC7: 0x40014907
DSI9_HC8: 0x40014908
DSI9_HC9: 0x40014909
DSI9_HC10: 0x4001490A
DSI9_HC11: 0x4001490B
DSI9_HC12: 0x4001490C
DSI9_HC13: 0x4001490D
DSI9_HC14: 0x4001490E
DSI9_HC15: 0x4001490F
DSI9_HC16: 0x40014910
DSI9_HC17: 0x40014911
DSI9_HC18: 0x40014912
DSI9_HC19: 0x40014913
DSI9_HC20: 0x40014914
DSI9_HC21: 0x40014915
DSI9_HC22: 0x40014916
DSI9_HC23: 0x40014917
DSI9_HC24: 0x40014918
DSI9_HC25: 0x40014919
DSI9_HC26: 0x4001491A
DSI9_HC27: 0x4001491B
DSI9_HC28: 0x4001491C
DSI9_HC29: 0x4001491D
DSI9_HC30: 0x4001491E
DSI9_HC31: 0x4001491F
DSI9_HC32: 0x40014920
DSI9_HC33: 0x40014921
DSI9_HC34: 0x40014922
DSI9_HC35: 0x40014923
DSI9_HC36: 0x40014924
DSI9_HC37: 0x40014925
DSI9_HC38: 0x40014926
DSI9_HC39: 0x40014927
DSI9_HC40: 0x40014928
DSI9_HC41: 0x40014929
DSI9_HC42: 0x4001492A
DSI9_HC43: 0x4001492B
DSI9_HC44: 0x4001492C
DSI9_HC45: 0x4001492D
DSI9_HC46: 0x4001492E
DSI9_HC47: 0x4001492F
DSI9_HC48: 0x40014930
DSI9_HC49: 0x40014931
DSI9_HC50: 0x40014932
DSI9_HC51: 0x40014933
DSI9_HC52: 0x40014934
DSI9_HC53: 0x40014935
DSI9_HC54: 0x40014936
DSI9_HC55: 0x40014937
DSI9_HC56: 0x40014938
DSI9_HC57: 0x40014939
DSI9_HC58: 0x4001493A
DSI9_HC59: 0x4001493B
DSI9_HC60: 0x4001493C
DSI9_HC61: 0x4001493D
DSI9_HC62: 0x4001493E
DSI9_HC63: 0x4001493F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI9_HC64: 0x40014940	DSI9_HC65: 0x40014941
DSI9_HC66: 0x40014942	DSI9_HC67: 0x40014943
DSI9_HC68: 0x40014944	DSI9_HC69: 0x40014945
DSI9_HC70: 0x40014946	DSI9_HC71: 0x40014947
DSI9_HC72: 0x40014948	DSI9_HC73: 0x40014949
DSI9_HC74: 0x4001494A	DSI9_HC75: 0x4001494B
DSI9_HC76: 0x4001494C	DSI9_HC77: 0x4001494D
DSI9_HC78: 0x4001494E	DSI9_HC79: 0x4001494F
DSI9_HC80: 0x40014950	DSI9_HC81: 0x40014951
DSI9_HC82: 0x40014952	DSI9_HC83: 0x40014953
DSI9_HC84: 0x40014954	DSI9_HC85: 0x40014955
DSI9_HC86: 0x40014956	DSI9_HC87: 0x40014957
DSI9_HC88: 0x40014958	DSI9_HC89: 0x40014959
DSI9_HC90: 0x4001495A	DSI9_HC91: 0x4001495B
DSI9_HC92: 0x4001495C	DSI9_HC93: 0x4001495D
DSI9_HC94: 0x4001495E	DSI9_HC95: 0x4001495F
DSI9_HC96: 0x40014960	DSI9_HC97: 0x40014961
DSI9_HC98: 0x40014962	DSI9_HC99: 0x40014963
DSI9_HC100: 0x40014964	DSI9_HC101: 0x40014965
DSI9_HC102: 0x40014966	DSI9_HC103: 0x40014967
DSI9_HC104: 0x40014968	DSI9_HC105: 0x40014969
DSI9_HC106: 0x4001496A	DSI9_HC107: 0x4001496B
DSI9_HC108: 0x4001496C	DSI9_HC109: 0x4001496D
DSI9_HC110: 0x4001496E	DSI9_HC111: 0x4001496F
DSI9_HC112: 0x40014970	DSI9_HC113: 0x40014971
DSI9_HC114: 0x40014972	DSI9_HC115: 0x40014973
DSI9_HC116: 0x40014974	DSI9_HC117: 0x40014975
DSI9_HC118: 0x40014976	DSI9_HC119: 0x40014977
DSI9_HC120: 0x40014978	DSI9_HC121: 0x40014979
DSI9_HC122: 0x4001497A	DSI9_HC123: 0x4001497B
DSI9_HC124: 0x4001497C	DSI9_HC125: 0x4001497D
DSI9_HC126: 0x4001497E	DSI9_HC127: 0x4001497F
DSI12_HC0: 0x40014C00	DSI12_HC1: 0x40014C01
DSI12_HC2: 0x40014C02	DSI12_HC3: 0x40014C03
DSI12_HC4: 0x40014C04	DSI12_HC5: 0x40014C05
DSI12_HC6: 0x40014C06	DSI12_HC7: 0x40014C07

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI12_HC8: 0x40014C08	DSI12_HC9: 0x40014C09
DSI12_HC10: 0x40014C0A	DSI12_HC11: 0x40014C0B
DSI12_HC12: 0x40014C0C	DSI12_HC13: 0x40014C0D
DSI12_HC14: 0x40014C0E	DSI12_HC15: 0x40014C0F
DSI12_HC16: 0x40014C10	DSI12_HC17: 0x40014C11
DSI12_HC18: 0x40014C12	DSI12_HC19: 0x40014C13
DSI12_HC20: 0x40014C14	DSI12_HC21: 0x40014C15
DSI12_HC22: 0x40014C16	DSI12_HC23: 0x40014C17
DSI12_HC24: 0x40014C18	DSI12_HC25: 0x40014C19
DSI12_HC26: 0x40014C1A	DSI12_HC27: 0x40014C1B
DSI12_HC28: 0x40014C1C	DSI12_HC29: 0x40014C1D
DSI12_HC30: 0x40014C1E	DSI12_HC31: 0x40014C1F
DSI12_HC32: 0x40014C20	DSI12_HC33: 0x40014C21
DSI12_HC34: 0x40014C22	DSI12_HC35: 0x40014C23
DSI12_HC36: 0x40014C24	DSI12_HC37: 0x40014C25
DSI12_HC38: 0x40014C26	DSI12_HC39: 0x40014C27
DSI12_HC40: 0x40014C28	DSI12_HC41: 0x40014C29
DSI12_HC42: 0x40014C2A	DSI12_HC43: 0x40014C2B
DSI12_HC44: 0x40014C2C	DSI12_HC45: 0x40014C2D
DSI12_HC46: 0x40014C2E	DSI12_HC47: 0x40014C2F
DSI12_HC48: 0x40014C30	DSI12_HC49: 0x40014C31
DSI12_HC50: 0x40014C32	DSI12_HC51: 0x40014C33
DSI12_HC52: 0x40014C34	DSI12_HC53: 0x40014C35
DSI12_HC54: 0x40014C36	DSI12_HC55: 0x40014C37
DSI12_HC56: 0x40014C38	DSI12_HC57: 0x40014C39
DSI12_HC58: 0x40014C3A	DSI12_HC59: 0x40014C3B
DSI12_HC60: 0x40014C3C	DSI12_HC61: 0x40014C3D
DSI12_HC62: 0x40014C3E	DSI12_HC63: 0x40014C3F
DSI12_HC64: 0x40014C40	DSI12_HC65: 0x40014C41
DSI12_HC66: 0x40014C42	DSI12_HC67: 0x40014C43
DSI12_HC68: 0x40014C44	DSI12_HC69: 0x40014C45
DSI12_HC70: 0x40014C46	DSI12_HC71: 0x40014C47
DSI12_HC72: 0x40014C48	DSI12_HC73: 0x40014C49
DSI12_HC74: 0x40014C4A	DSI12_HC75: 0x40014C4B
DSI12_HC76: 0x40014C4C	DSI12_HC77: 0x40014C4D
DSI12_HC78: 0x40014C4E	DSI12_HC79: 0x40014C4F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI12_HC80: 0x40014C50
DSI12_HC81: 0x40014C51
DSI12_HC82: 0x40014C52
DSI12_HC83: 0x40014C53
DSI12_HC84: 0x40014C54
DSI12_HC85: 0x40014C55
DSI12_HC86: 0x40014C56
DSI12_HC87: 0x40014C57
DSI12_HC88: 0x40014C58
DSI12_HC89: 0x40014C59
DSI12_HC90: 0x40014C5A
DSI12_HC91: 0x40014C5B
DSI12_HC92: 0x40014C5C
DSI12_HC93: 0x40014C5D
DSI12_HC94: 0x40014C5E
DSI12_HC95: 0x40014C5F
DSI12_HC96: 0x40014C60
DSI12_HC97: 0x40014C61
DSI12_HC98: 0x40014C62
DSI12_HC99: 0x40014C63
DSI12_HC100: 0x40014C64
DSI12_HC101: 0x40014C65
DSI12_HC102: 0x40014C66
DSI12_HC103: 0x40014C67
DSI12_HC104: 0x40014C68
DSI12_HC105: 0x40014C69
DSI12_HC106: 0x40014C6A
DSI12_HC107: 0x40014C6B
DSI12_HC108: 0x40014C6C
DSI12_HC109: 0x40014C6D
DSI12_HC110: 0x40014C6E
DSI12_HC111: 0x40014C6F
DSI12_HC112: 0x40014C70
DSI12_HC113: 0x40014C71
DSI12_HC114: 0x40014C72
DSI12_HC115: 0x40014C73
DSI12_HC116: 0x40014C74
DSI12_HC117: 0x40014C75
DSI12_HC118: 0x40014C76
DSI12_HC119: 0x40014C77
DSI12_HC120: 0x40014C78
DSI12_HC121: 0x40014C79
DSI12_HC122: 0x40014C7A
DSI12_HC123: 0x40014C7B
DSI12_HC124: 0x40014C7C
DSI12_HC125: 0x40014C7D
DSI12_HC126: 0x40014C7E
DSI12_HC127: 0x40014C7F
DSI13_HC0: 0x40014D00
DSI13_HC1: 0x40014D01
DSI13_HC2: 0x40014D02
DSI13_HC3: 0x40014D03
DSI13_HC4: 0x40014D04
DSI13_HC5: 0x40014D05
DSI13_HC6: 0x40014D06
DSI13_HC7: 0x40014D07
DSI13_HC8: 0x40014D08
DSI13_HC9: 0x40014D09
DSI13_HC10: 0x40014D0A
DSI13_HC11: 0x40014D0B
DSI13_HC12: 0x40014D0C
DSI13_HC13: 0x40014D0D
DSI13_HC14: 0x40014D0E
DSI13_HC15: 0x40014D0F
DSI13_HC16: 0x40014D10
DSI13_HC17: 0x40014D11
DSI13_HC18: 0x40014D12
DSI13_HC19: 0x40014D13
DSI13_HC20: 0x40014D14
DSI13_HC21: 0x40014D15
DSI13_HC22: 0x40014D16
DSI13_HC23: 0x40014D17

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI13_HC24: 0x40014D18	DSI13_HC25: 0x40014D19
DSI13_HC26: 0x40014D1A	DSI13_HC27: 0x40014D1B
DSI13_HC28: 0x40014D1C	DSI13_HC29: 0x40014D1D
DSI13_HC30: 0x40014D1E	DSI13_HC31: 0x40014D1F
DSI13_HC32: 0x40014D20	DSI13_HC33: 0x40014D21
DSI13_HC34: 0x40014D22	DSI13_HC35: 0x40014D23
DSI13_HC36: 0x40014D24	DSI13_HC37: 0x40014D25
DSI13_HC38: 0x40014D26	DSI13_HC39: 0x40014D27
DSI13_HC40: 0x40014D28	DSI13_HC41: 0x40014D29
DSI13_HC42: 0x40014D2A	DSI13_HC43: 0x40014D2B
DSI13_HC44: 0x40014D2C	DSI13_HC45: 0x40014D2D
DSI13_HC46: 0x40014D2E	DSI13_HC47: 0x40014D2F
DSI13_HC48: 0x40014D30	DSI13_HC49: 0x40014D31
DSI13_HC50: 0x40014D32	DSI13_HC51: 0x40014D33
DSI13_HC52: 0x40014D34	DSI13_HC53: 0x40014D35
DSI13_HC54: 0x40014D36	DSI13_HC55: 0x40014D37
DSI13_HC56: 0x40014D38	DSI13_HC57: 0x40014D39
DSI13_HC58: 0x40014D3A	DSI13_HC59: 0x40014D3B
DSI13_HC60: 0x40014D3C	DSI13_HC61: 0x40014D3D
DSI13_HC62: 0x40014D3E	DSI13_HC63: 0x40014D3F
DSI13_HC64: 0x40014D40	DSI13_HC65: 0x40014D41
DSI13_HC66: 0x40014D42	DSI13_HC67: 0x40014D43
DSI13_HC68: 0x40014D44	DSI13_HC69: 0x40014D45
DSI13_HC70: 0x40014D46	DSI13_HC71: 0x40014D47
DSI13_HC72: 0x40014D48	DSI13_HC73: 0x40014D49
DSI13_HC74: 0x40014D4A	DSI13_HC75: 0x40014D4B
DSI13_HC76: 0x40014D4C	DSI13_HC77: 0x40014D4D
DSI13_HC78: 0x40014D4E	DSI13_HC79: 0x40014D4F
DSI13_HC80: 0x40014D50	DSI13_HC81: 0x40014D51
DSI13_HC82: 0x40014D52	DSI13_HC83: 0x40014D53
DSI13_HC84: 0x40014D54	DSI13_HC85: 0x40014D55
DSI13_HC86: 0x40014D56	DSI13_HC87: 0x40014D57
DSI13_HC88: 0x40014D58	DSI13_HC89: 0x40014D59
DSI13_HC90: 0x40014D5A	DSI13_HC91: 0x40014D5B
DSI13_HC92: 0x40014D5C	DSI13_HC93: 0x40014D5D
DSI13_HC94: 0x40014D5E	DSI13_HC95: 0x40014D5F

1.3.1187 DSI[0..15]_HC[0..127] (continued)

Register : Address

DSI13_HC96: 0x40014D60	DSI13_HC97: 0x40014D61
DSI13_HC98: 0x40014D62	DSI13_HC99: 0x40014D63
DSI13_HC100: 0x40014D64	DSI13_HC101: 0x40014D65
DSI13_HC102: 0x40014D66	DSI13_HC103: 0x40014D67
DSI13_HC104: 0x40014D68	DSI13_HC105: 0x40014D69
DSI13_HC106: 0x40014D6A	DSI13_HC107: 0x40014D6B
DSI13_HC108: 0x40014D6C	DSI13_HC109: 0x40014D6D
DSI13_HC110: 0x40014D6E	DSI13_HC111: 0x40014D6F
DSI13_HC112: 0x40014D70	DSI13_HC113: 0x40014D71
DSI13_HC114: 0x40014D72	DSI13_HC115: 0x40014D73
DSI13_HC116: 0x40014D74	DSI13_HC117: 0x40014D75
DSI13_HC118: 0x40014D76	DSI13_HC119: 0x40014D77
DSI13_HC120: 0x40014D78	DSI13_HC121: 0x40014D79
DSI13_HC122: 0x40014D7A	DSI13_HC123: 0x40014D7B
DSI13_HC124: 0x40014D7C	DSI13_HC125: 0x40014D7D
DSI13_HC126: 0x40014D7E	DSI13_HC127: 0x40014D7F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	hc_byte							

DSI HC Tile Configuration

Bits	Name	Description
7:0	hc_byte[7:0]	RAM configuration for DSI channel bytes

1.3.1188 DSI[0..15]_HV_L[0..15]

HV_L

Reset: N/A

Register : Address

DSI0_HV_L0: 0x40014080	DSI0_HV_L1: 0x40014081
DSI0_HV_L2: 0x40014082	DSI0_HV_L3: 0x40014083
DSI0_HV_L4: 0x40014084	DSI0_HV_L5: 0x40014085
DSI0_HV_L6: 0x40014086	DSI0_HV_L7: 0x40014087
DSI0_HV_L8: 0x40014088	DSI0_HV_L9: 0x40014089
DSI0_HV_L10: 0x4001408A	DSI0_HV_L11: 0x4001408B
DSI0_HV_L12: 0x4001408C	DSI0_HV_L13: 0x4001408D
DSI0_HV_L14: 0x4001408E	DSI0_HV_L15: 0x4001408F
DSI1_HV_L0: 0x40014180	DSI1_HV_L1: 0x40014181
DSI1_HV_L2: 0x40014182	DSI1_HV_L3: 0x40014183
DSI1_HV_L4: 0x40014184	DSI1_HV_L5: 0x40014185
DSI1_HV_L6: 0x40014186	DSI1_HV_L7: 0x40014187
DSI1_HV_L8: 0x40014188	DSI1_HV_L9: 0x40014189
DSI1_HV_L10: 0x4001418A	DSI1_HV_L11: 0x4001418B
DSI1_HV_L12: 0x4001418C	DSI1_HV_L13: 0x4001418D
DSI1_HV_L14: 0x4001418E	DSI1_HV_L15: 0x4001418F
DSI2_HV_L0: 0x40014280	DSI2_HV_L1: 0x40014281
DSI2_HV_L2: 0x40014282	DSI2_HV_L3: 0x40014283
DSI2_HV_L4: 0x40014284	DSI2_HV_L5: 0x40014285
DSI2_HV_L6: 0x40014286	DSI2_HV_L7: 0x40014287
DSI2_HV_L8: 0x40014288	DSI2_HV_L9: 0x40014289
DSI2_HV_L10: 0x4001428A	DSI2_HV_L11: 0x4001428B
DSI2_HV_L12: 0x4001428C	DSI2_HV_L13: 0x4001428D
DSI2_HV_L14: 0x4001428E	DSI2_HV_L15: 0x4001428F
DSI3_HV_L0: 0x40014380	DSI3_HV_L1: 0x40014381
DSI3_HV_L2: 0x40014382	DSI3_HV_L3: 0x40014383
DSI3_HV_L4: 0x40014384	DSI3_HV_L5: 0x40014385
DSI3_HV_L6: 0x40014386	DSI3_HV_L7: 0x40014387
DSI3_HV_L8: 0x40014388	DSI3_HV_L9: 0x40014389
DSI3_HV_L10: 0x4001438A	DSI3_HV_L11: 0x4001438B
DSI3_HV_L12: 0x4001438C	DSI3_HV_L13: 0x4001438D
DSI3_HV_L14: 0x4001438E	DSI3_HV_L15: 0x4001438F

1.3.1188 DSI[0..15]_HV_L[0..15] (continued)

Register : Address

DSI4_HV_L0: 0x40014480	DSI4_HV_L1: 0x40014481
DSI4_HV_L2: 0x40014482	DSI4_HV_L3: 0x40014483
DSI4_HV_L4: 0x40014484	DSI4_HV_L5: 0x40014485
DSI4_HV_L6: 0x40014486	DSI4_HV_L7: 0x40014487
DSI4_HV_L8: 0x40014488	DSI4_HV_L9: 0x40014489
DSI4_HV_L10: 0x4001448A	DSI4_HV_L11: 0x4001448B
DSI4_HV_L12: 0x4001448C	DSI4_HV_L13: 0x4001448D
DSI4_HV_L14: 0x4001448E	DSI4_HV_L15: 0x4001448F
DSI5_HV_L0: 0x40014580	DSI5_HV_L1: 0x40014581
DSI5_HV_L2: 0x40014582	DSI5_HV_L3: 0x40014583
DSI5_HV_L4: 0x40014584	DSI5_HV_L5: 0x40014585
DSI5_HV_L6: 0x40014586	DSI5_HV_L7: 0x40014587
DSI5_HV_L8: 0x40014588	DSI5_HV_L9: 0x40014589
DSI5_HV_L10: 0x4001458A	DSI5_HV_L11: 0x4001458B
DSI5_HV_L12: 0x4001458C	DSI5_HV_L13: 0x4001458D
DSI5_HV_L14: 0x4001458E	DSI5_HV_L15: 0x4001458F
DSI6_HV_L0: 0x40014680	DSI6_HV_L1: 0x40014681
DSI6_HV_L2: 0x40014682	DSI6_HV_L3: 0x40014683
DSI6_HV_L4: 0x40014684	DSI6_HV_L5: 0x40014685
DSI6_HV_L6: 0x40014686	DSI6_HV_L7: 0x40014687
DSI6_HV_L8: 0x40014688	DSI6_HV_L9: 0x40014689
DSI6_HV_L10: 0x4001468A	DSI6_HV_L11: 0x4001468B
DSI6_HV_L12: 0x4001468C	DSI6_HV_L13: 0x4001468D
DSI6_HV_L14: 0x4001468E	DSI6_HV_L15: 0x4001468F
DSI7_HV_L0: 0x40014780	DSI7_HV_L1: 0x40014781
DSI7_HV_L2: 0x40014782	DSI7_HV_L3: 0x40014783
DSI7_HV_L4: 0x40014784	DSI7_HV_L5: 0x40014785
DSI7_HV_L6: 0x40014786	DSI7_HV_L7: 0x40014787
DSI7_HV_L8: 0x40014788	DSI7_HV_L9: 0x40014789
DSI7_HV_L10: 0x4001478A	DSI7_HV_L11: 0x4001478B
DSI7_HV_L12: 0x4001478C	DSI7_HV_L13: 0x4001478D
DSI7_HV_L14: 0x4001478E	DSI7_HV_L15: 0x4001478F
DSI8_HV_L0: 0x40014880	DSI8_HV_L1: 0x40014881
DSI8_HV_L2: 0x40014882	DSI8_HV_L3: 0x40014883
DSI8_HV_L4: 0x40014884	DSI8_HV_L5: 0x40014885
DSI8_HV_L6: 0x40014886	DSI8_HV_L7: 0x40014887

1.3.1188 DSI[0..15]_HV_L[0..15] (continued)

Register : Address

DSI8_HV_L8: 0x40014888	DSI8_HV_L9: 0x40014889
DSI8_HV_L10: 0x4001488A	DSI8_HV_L11: 0x4001488B
DSI8_HV_L12: 0x4001488C	DSI8_HV_L13: 0x4001488D
DSI8_HV_L14: 0x4001488E	DSI8_HV_L15: 0x4001488F
DSI9_HV_L0: 0x40014980	DSI9_HV_L1: 0x40014981
DSI9_HV_L2: 0x40014982	DSI9_HV_L3: 0x40014983
DSI9_HV_L4: 0x40014984	DSI9_HV_L5: 0x40014985
DSI9_HV_L6: 0x40014986	DSI9_HV_L7: 0x40014987
DSI9_HV_L8: 0x40014988	DSI9_HV_L9: 0x40014989
DSI9_HV_L10: 0x4001498A	DSI9_HV_L11: 0x4001498B
DSI9_HV_L12: 0x4001498C	DSI9_HV_L13: 0x4001498D
DSI9_HV_L14: 0x4001498E	DSI9_HV_L15: 0x4001498F
DSI12_HV_L0: 0x40014C80	DSI12_HV_L1: 0x40014C81
DSI12_HV_L2: 0x40014C82	DSI12_HV_L3: 0x40014C83
DSI12_HV_L4: 0x40014C84	DSI12_HV_L5: 0x40014C85
DSI12_HV_L6: 0x40014C86	DSI12_HV_L7: 0x40014C87
DSI12_HV_L8: 0x40014C88	DSI12_HV_L9: 0x40014C89
DSI12_HV_L10: 0x40014C8A	DSI12_HV_L11: 0x40014C8B
DSI12_HV_L12: 0x40014C8C	DSI12_HV_L13: 0x40014C8D
DSI12_HV_L14: 0x40014C8E	DSI12_HV_L15: 0x40014C8F
DSI13_HV_L0: 0x40014D80	DSI13_HV_L1: 0x40014D81
DSI13_HV_L2: 0x40014D82	DSI13_HV_L3: 0x40014D83
DSI13_HV_L4: 0x40014D84	DSI13_HV_L5: 0x40014D85
DSI13_HV_L6: 0x40014D86	DSI13_HV_L7: 0x40014D87
DSI13_HV_L8: 0x40014D88	DSI13_HV_L9: 0x40014D89
DSI13_HV_L10: 0x40014D8A	DSI13_HV_L11: 0x40014D8B
DSI13_HV_L12: 0x40014D8C	DSI13_HV_L13: 0x40014D8D
DSI13_HV_L14: 0x40014D8E	DSI13_HV_L15: 0x40014D8F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	hv_byte							

DSI HV Tile Configuration

Bits	Name	Description
7:0	hv_byte[7:0]	RAM configuration for DSI channel bytes

1.3.1189 DSI[0..15]_HS[0..23]

HS

Reset: N/A

Register : Address

DSI0_HS0: 0x40014090	DSI0_HS1: 0x40014091
DSI0_HS2: 0x40014092	DSI0_HS3: 0x40014093
DSI0_HS4: 0x40014094	DSI0_HS5: 0x40014095
DSI0_HS6: 0x40014096	DSI0_HS7: 0x40014097
DSI0_HS8: 0x40014098	DSI0_HS9: 0x40014099
DSI0_HS10: 0x4001409A	DSI0_HS11: 0x4001409B
DSI0_HS12: 0x4001409C	DSI0_HS13: 0x4001409D
DSI0_HS14: 0x4001409E	DSI0_HS15: 0x4001409F
DSI0_HS16: 0x400140A0	DSI0_HS17: 0x400140A1
DSI0_HS18: 0x400140A2	DSI0_HS19: 0x400140A3
DSI0_HS20: 0x400140A4	DSI0_HS21: 0x400140A5
DSI0_HS22: 0x400140A6	DSI0_HS23: 0x400140A7
DSI1_HS0: 0x40014190	DSI1_HS1: 0x40014191
DSI1_HS2: 0x40014192	DSI1_HS3: 0x40014193
DSI1_HS4: 0x40014194	DSI1_HS5: 0x40014195
DSI1_HS6: 0x40014196	DSI1_HS7: 0x40014197
DSI1_HS8: 0x40014198	DSI1_HS9: 0x40014199
DSI1_HS10: 0x4001419A	DSI1_HS11: 0x4001419B
DSI1_HS12: 0x4001419C	DSI1_HS13: 0x4001419D
DSI1_HS14: 0x4001419E	DSI1_HS15: 0x4001419F
DSI1_HS16: 0x400141A0	DSI1_HS17: 0x400141A1
DSI1_HS18: 0x400141A2	DSI1_HS19: 0x400141A3
DSI1_HS20: 0x400141A4	DSI1_HS21: 0x400141A5
DSI1_HS22: 0x400141A6	DSI1_HS23: 0x400141A7
DSI2_HS0: 0x40014290	DSI2_HS1: 0x40014291
DSI2_HS2: 0x40014292	DSI2_HS3: 0x40014293
DSI2_HS4: 0x40014294	DSI2_HS5: 0x40014295
DSI2_HS6: 0x40014296	DSI2_HS7: 0x40014297
DSI2_HS8: 0x40014298	DSI2_HS9: 0x40014299
DSI2_HS10: 0x4001429A	DSI2_HS11: 0x4001429B
DSI2_HS12: 0x4001429C	DSI2_HS13: 0x4001429D
DSI2_HS14: 0x4001429E	DSI2_HS15: 0x4001429F

1.3.1189 DSI[0..15]_HS[0..23] (continued)

Register : Address

DSI2_HS16: 0x400142A0
DSI2_HS17: 0x400142A1
DSI2_HS18: 0x400142A2
DSI2_HS19: 0x400142A3
DSI2_HS20: 0x400142A4
DSI2_HS21: 0x400142A5
DSI2_HS22: 0x400142A6
DSI2_HS23: 0x400142A7
DSI3_HS0: 0x40014390
DSI3_HS1: 0x40014391
DSI3_HS2: 0x40014392
DSI3_HS3: 0x40014393
DSI3_HS4: 0x40014394
DSI3_HS5: 0x40014395
DSI3_HS6: 0x40014396
DSI3_HS7: 0x40014397
DSI3_HS8: 0x40014398
DSI3_HS9: 0x40014399
DSI3_HS10: 0x4001439A
DSI3_HS11: 0x4001439B
DSI3_HS12: 0x4001439C
DSI3_HS13: 0x4001439D
DSI3_HS14: 0x4001439E
DSI3_HS15: 0x4001439F
DSI3_HS16: 0x400143A0
DSI3_HS17: 0x400143A1
DSI3_HS18: 0x400143A2
DSI3_HS19: 0x400143A3
DSI3_HS20: 0x400143A4
DSI3_HS21: 0x400143A5
DSI3_HS22: 0x400143A6
DSI3_HS23: 0x400143A7
DSI4_HS0: 0x40014490
DSI4_HS1: 0x40014491
DSI4_HS2: 0x40014492
DSI4_HS3: 0x40014493
DSI4_HS4: 0x40014494
DSI4_HS5: 0x40014495
DSI4_HS6: 0x40014496
DSI4_HS7: 0x40014497
DSI4_HS8: 0x40014498
DSI4_HS9: 0x40014499
DSI4_HS10: 0x4001449A
DSI4_HS11: 0x4001449B
DSI4_HS12: 0x4001449C
DSI4_HS13: 0x4001449D
DSI4_HS14: 0x4001449E
DSI4_HS15: 0x4001449F
DSI4_HS16: 0x400144A0
DSI4_HS17: 0x400144A1
DSI4_HS18: 0x400144A2
DSI4_HS19: 0x400144A3
DSI4_HS20: 0x400144A4
DSI4_HS21: 0x400144A5
DSI4_HS22: 0x400144A6
DSI4_HS23: 0x400144A7
DSI5_HS0: 0x40014590
DSI5_HS1: 0x40014591
DSI5_HS2: 0x40014592
DSI5_HS3: 0x40014593
DSI5_HS4: 0x40014594
DSI5_HS5: 0x40014595
DSI5_HS6: 0x40014596
DSI5_HS7: 0x40014597
DSI5_HS8: 0x40014598
DSI5_HS9: 0x40014599
DSI5_HS10: 0x4001459A
DSI5_HS11: 0x4001459B
DSI5_HS12: 0x4001459C
DSI5_HS13: 0x4001459D
DSI5_HS14: 0x4001459E
DSI5_HS15: 0x4001459F

1.3.1189 DSI[0..15]_HS[0..23] (continued)

Register : Address

DSI5_HS16: 0x400145A0	DSI5_HS17: 0x400145A1
DSI5_HS18: 0x400145A2	DSI5_HS19: 0x400145A3
DSI5_HS20: 0x400145A4	DSI5_HS21: 0x400145A5
DSI5_HS22: 0x400145A6	DSI5_HS23: 0x400145A7
DSI6_HS0: 0x40014690	DSI6_HS1: 0x40014691
DSI6_HS2: 0x40014692	DSI6_HS3: 0x40014693
DSI6_HS4: 0x40014694	DSI6_HS5: 0x40014695
DSI6_HS6: 0x40014696	DSI6_HS7: 0x40014697
DSI6_HS8: 0x40014698	DSI6_HS9: 0x40014699
DSI6_HS10: 0x4001469A	DSI6_HS11: 0x4001469B
DSI6_HS12: 0x4001469C	DSI6_HS13: 0x4001469D
DSI6_HS14: 0x4001469E	DSI6_HS15: 0x4001469F
DSI6_HS16: 0x400146A0	DSI6_HS17: 0x400146A1
DSI6_HS18: 0x400146A2	DSI6_HS19: 0x400146A3
DSI6_HS20: 0x400146A4	DSI6_HS21: 0x400146A5
DSI6_HS22: 0x400146A6	DSI6_HS23: 0x400146A7
DSI7_HS0: 0x40014790	DSI7_HS1: 0x40014791
DSI7_HS2: 0x40014792	DSI7_HS3: 0x40014793
DSI7_HS4: 0x40014794	DSI7_HS5: 0x40014795
DSI7_HS6: 0x40014796	DSI7_HS7: 0x40014797
DSI7_HS8: 0x40014798	DSI7_HS9: 0x40014799
DSI7_HS10: 0x4001479A	DSI7_HS11: 0x4001479B
DSI7_HS12: 0x4001479C	DSI7_HS13: 0x4001479D
DSI7_HS14: 0x4001479E	DSI7_HS15: 0x4001479F
DSI7_HS16: 0x400147A0	DSI7_HS17: 0x400147A1
DSI7_HS18: 0x400147A2	DSI7_HS19: 0x400147A3
DSI7_HS20: 0x400147A4	DSI7_HS21: 0x400147A5
DSI7_HS22: 0x400147A6	DSI7_HS23: 0x400147A7
DSI8_HS0: 0x40014890	DSI8_HS1: 0x40014891
DSI8_HS2: 0x40014892	DSI8_HS3: 0x40014893
DSI8_HS4: 0x40014894	DSI8_HS5: 0x40014895
DSI8_HS6: 0x40014896	DSI8_HS7: 0x40014897
DSI8_HS8: 0x40014898	DSI8_HS9: 0x40014899
DSI8_HS10: 0x4001489A	DSI8_HS11: 0x4001489B
DSI8_HS12: 0x4001489C	DSI8_HS13: 0x4001489D
DSI8_HS14: 0x4001489E	DSI8_HS15: 0x4001489F

1.3.1189 DSI[0..15]_HS[0..23] (continued)

Register : Address

DSI8_HS16: 0x400148A0
DSI8_HS17: 0x400148A1
DSI8_HS18: 0x400148A2
DSI8_HS19: 0x400148A3
DSI8_HS20: 0x400148A4
DSI8_HS21: 0x400148A5
DSI8_HS22: 0x400148A6
DSI8_HS23: 0x400148A7
DSI9_HS0: 0x40014990
DSI9_HS1: 0x40014991
DSI9_HS2: 0x40014992
DSI9_HS3: 0x40014993
DSI9_HS4: 0x40014994
DSI9_HS5: 0x40014995
DSI9_HS6: 0x40014996
DSI9_HS7: 0x40014997
DSI9_HS8: 0x40014998
DSI9_HS9: 0x40014999
DSI9_HS10: 0x4001499A
DSI9_HS11: 0x4001499B
DSI9_HS12: 0x4001499C
DSI9_HS13: 0x4001499D
DSI9_HS14: 0x4001499E
DSI9_HS15: 0x4001499F
DSI9_HS16: 0x400149A0
DSI9_HS17: 0x400149A1
DSI9_HS18: 0x400149A2
DSI9_HS19: 0x400149A3
DSI9_HS20: 0x400149A4
DSI9_HS21: 0x400149A5
DSI9_HS22: 0x400149A6
DSI9_HS23: 0x400149A7
DSI12_HS0: 0x40014C90
DSI12_HS1: 0x40014C91
DSI12_HS2: 0x40014C92
DSI12_HS3: 0x40014C93
DSI12_HS4: 0x40014C94
DSI12_HS5: 0x40014C95
DSI12_HS6: 0x40014C96
DSI12_HS7: 0x40014C97
DSI12_HS8: 0x40014C98
DSI12_HS9: 0x40014C99
DSI12_HS10: 0x40014C9A
DSI12_HS11: 0x40014C9B
DSI12_HS12: 0x40014C9C
DSI12_HS13: 0x40014C9D
DSI12_HS14: 0x40014C9E
DSI12_HS15: 0x40014C9F
DSI12_HS16: 0x40014CA0
DSI12_HS17: 0x40014CA1
DSI12_HS18: 0x40014CA2
DSI12_HS19: 0x40014CA3
DSI12_HS20: 0x40014CA4
DSI12_HS21: 0x40014CA5
DSI12_HS22: 0x40014CA6
DSI12_HS23: 0x40014CA7
DSI13_HS0: 0x40014D90
DSI13_HS1: 0x40014D91
DSI13_HS2: 0x40014D92
DSI13_HS3: 0x40014D93
DSI13_HS4: 0x40014D94
DSI13_HS5: 0x40014D95
DSI13_HS6: 0x40014D96
DSI13_HS7: 0x40014D97
DSI13_HS8: 0x40014D98
DSI13_HS9: 0x40014D99
DSI13_HS10: 0x40014D9A
DSI13_HS11: 0x40014D9B
DSI13_HS12: 0x40014D9C
DSI13_HS13: 0x40014D9D
DSI13_HS14: 0x40014D9E
DSI13_HS15: 0x40014D9F

1.3.1189 DSI[0..15]_HS[0..23] (continued)

Register : Address

DSI13_HS16: 0x40014DA0	DSI13_HS17: 0x40014DA1
DSI13_HS18: 0x40014DA2	DSI13_HS19: 0x40014DA3
DSI13_HS20: 0x40014DA4	DSI13_HS21: 0x40014DA5
DSI13_HS22: 0x40014DA6	DSI13_HS23: 0x40014DA7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	hs_byte							

DSI HS Tile Configuration

Bits	Name	Description
7:0	hs_byte[7:0]	RAM configuration for DSI channel bytes

1.3.1190 DSI[0..15]_HV_R[0..15]

HV_R

Reset: N/A

Register : Address

DSI0_HV_R0: 0x400140A8	DSI0_HV_R1: 0x400140A9
DSI0_HV_R2: 0x400140AA	DSI0_HV_R3: 0x400140AB
DSI0_HV_R4: 0x400140AC	DSI0_HV_R5: 0x400140AD
DSI0_HV_R6: 0x400140AE	DSI0_HV_R7: 0x400140AF
DSI0_HV_R8: 0x400140B0	DSI0_HV_R9: 0x400140B1
DSI0_HV_R10: 0x400140B2	DSI0_HV_R11: 0x400140B3
DSI0_HV_R12: 0x400140B4	DSI0_HV_R13: 0x400140B5
DSI0_HV_R14: 0x400140B6	DSI0_HV_R15: 0x400140B7
DSI1_HV_R0: 0x400141A8	DSI1_HV_R1: 0x400141A9
DSI1_HV_R2: 0x400141AA	DSI1_HV_R3: 0x400141AB
DSI1_HV_R4: 0x400141AC	DSI1_HV_R5: 0x400141AD
DSI1_HV_R6: 0x400141AE	DSI1_HV_R7: 0x400141AF
DSI1_HV_R8: 0x400141B0	DSI1_HV_R9: 0x400141B1
DSI1_HV_R10: 0x400141B2	DSI1_HV_R11: 0x400141B3
DSI1_HV_R12: 0x400141B4	DSI1_HV_R13: 0x400141B5
DSI1_HV_R14: 0x400141B6	DSI1_HV_R15: 0x400141B7
DSI2_HV_R0: 0x400142A8	DSI2_HV_R1: 0x400142A9
DSI2_HV_R2: 0x400142AA	DSI2_HV_R3: 0x400142AB
DSI2_HV_R4: 0x400142AC	DSI2_HV_R5: 0x400142AD
DSI2_HV_R6: 0x400142AE	DSI2_HV_R7: 0x400142AF
DSI2_HV_R8: 0x400142B0	DSI2_HV_R9: 0x400142B1
DSI2_HV_R10: 0x400142B2	DSI2_HV_R11: 0x400142B3
DSI2_HV_R12: 0x400142B4	DSI2_HV_R13: 0x400142B5
DSI2_HV_R14: 0x400142B6	DSI2_HV_R15: 0x400142B7
DSI3_HV_R0: 0x400143A8	DSI3_HV_R1: 0x400143A9
DSI3_HV_R2: 0x400143AA	DSI3_HV_R3: 0x400143AB
DSI3_HV_R4: 0x400143AC	DSI3_HV_R5: 0x400143AD
DSI3_HV_R6: 0x400143AE	DSI3_HV_R7: 0x400143AF
DSI3_HV_R8: 0x400143B0	DSI3_HV_R9: 0x400143B1
DSI3_HV_R10: 0x400143B2	DSI3_HV_R11: 0x400143B3
DSI3_HV_R12: 0x400143B4	DSI3_HV_R13: 0x400143B5
DSI3_HV_R14: 0x400143B6	DSI3_HV_R15: 0x400143B7

1.3.1190 DSI[0..15]_HV_R[0..15] (continued)

Register : Address

DSI4_HV_R0: 0x400144A8	DSI4_HV_R1: 0x400144A9
DSI4_HV_R2: 0x400144AA	DSI4_HV_R3: 0x400144AB
DSI4_HV_R4: 0x400144AC	DSI4_HV_R5: 0x400144AD
DSI4_HV_R6: 0x400144AE	DSI4_HV_R7: 0x400144AF
DSI4_HV_R8: 0x400144B0	DSI4_HV_R9: 0x400144B1
DSI4_HV_R10: 0x400144B2	DSI4_HV_R11: 0x400144B3
DSI4_HV_R12: 0x400144B4	DSI4_HV_R13: 0x400144B5
DSI4_HV_R14: 0x400144B6	DSI4_HV_R15: 0x400144B7
DSI5_HV_R0: 0x400145A8	DSI5_HV_R1: 0x400145A9
DSI5_HV_R2: 0x400145AA	DSI5_HV_R3: 0x400145AB
DSI5_HV_R4: 0x400145AC	DSI5_HV_R5: 0x400145AD
DSI5_HV_R6: 0x400145AE	DSI5_HV_R7: 0x400145AF
DSI5_HV_R8: 0x400145B0	DSI5_HV_R9: 0x400145B1
DSI5_HV_R10: 0x400145B2	DSI5_HV_R11: 0x400145B3
DSI5_HV_R12: 0x400145B4	DSI5_HV_R13: 0x400145B5
DSI5_HV_R14: 0x400145B6	DSI5_HV_R15: 0x400145B7
DSI6_HV_R0: 0x400146A8	DSI6_HV_R1: 0x400146A9
DSI6_HV_R2: 0x400146AA	DSI6_HV_R3: 0x400146AB
DSI6_HV_R4: 0x400146AC	DSI6_HV_R5: 0x400146AD
DSI6_HV_R6: 0x400146AE	DSI6_HV_R7: 0x400146AF
DSI6_HV_R8: 0x400146B0	DSI6_HV_R9: 0x400146B1
DSI6_HV_R10: 0x400146B2	DSI6_HV_R11: 0x400146B3
DSI6_HV_R12: 0x400146B4	DSI6_HV_R13: 0x400146B5
DSI6_HV_R14: 0x400146B6	DSI6_HV_R15: 0x400146B7
DSI7_HV_R0: 0x400147A8	DSI7_HV_R1: 0x400147A9
DSI7_HV_R2: 0x400147AA	DSI7_HV_R3: 0x400147AB
DSI7_HV_R4: 0x400147AC	DSI7_HV_R5: 0x400147AD
DSI7_HV_R6: 0x400147AE	DSI7_HV_R7: 0x400147AF
DSI7_HV_R8: 0x400147B0	DSI7_HV_R9: 0x400147B1
DSI7_HV_R10: 0x400147B2	DSI7_HV_R11: 0x400147B3
DSI7_HV_R12: 0x400147B4	DSI7_HV_R13: 0x400147B5
DSI7_HV_R14: 0x400147B6	DSI7_HV_R15: 0x400147B7
DSI8_HV_R0: 0x400148A8	DSI8_HV_R1: 0x400148A9
DSI8_HV_R2: 0x400148AA	DSI8_HV_R3: 0x400148AB
DSI8_HV_R4: 0x400148AC	DSI8_HV_R5: 0x400148AD
DSI8_HV_R6: 0x400148AE	DSI8_HV_R7: 0x400148AF

1.3.1190 DSI[0..15]_HV_R[0..15] (continued)

Register : Address

DSI8_HV_R8: 0x400148B0
DSI8_HV_R9: 0x400148B1
DSI8_HV_R10: 0x400148B2
DSI8_HV_R11: 0x400148B3
DSI8_HV_R12: 0x400148B4
DSI8_HV_R13: 0x400148B5
DSI8_HV_R14: 0x400148B6
DSI8_HV_R15: 0x400148B7
DSI9_HV_R0: 0x400149A8
DSI9_HV_R1: 0x400149A9
DSI9_HV_R2: 0x400149AA
DSI9_HV_R3: 0x400149AB
DSI9_HV_R4: 0x400149AC
DSI9_HV_R5: 0x400149AD
DSI9_HV_R6: 0x400149AE
DSI9_HV_R7: 0x400149AF
DSI9_HV_R8: 0x400149B0
DSI9_HV_R9: 0x400149B1
DSI9_HV_R10: 0x400149B2
DSI9_HV_R11: 0x400149B3
DSI9_HV_R12: 0x400149B4
DSI9_HV_R13: 0x400149B5
DSI9_HV_R14: 0x400149B6
DSI9_HV_R15: 0x400149B7
DSI12_HV_R0: 0x40014CA8
DSI12_HV_R1: 0x40014CA9
DSI12_HV_R2: 0x40014CAA
DSI12_HV_R3: 0x40014CAB
DSI12_HV_R4: 0x40014CAC
DSI12_HV_R5: 0x40014CAD
DSI12_HV_R6: 0x40014CAE
DSI12_HV_R7: 0x40014CAF
DSI12_HV_R8: 0x40014CB0
DSI12_HV_R9: 0x40014CB1
DSI12_HV_R10: 0x40014CB2
DSI12_HV_R11: 0x40014CB3
DSI12_HV_R12: 0x40014CB4
DSI12_HV_R13: 0x40014CB5
DSI12_HV_R14: 0x40014CB6
DSI12_HV_R15: 0x40014CB7
DSI13_HV_R0: 0x40014DA8
DSI13_HV_R1: 0x40014DA9
DSI13_HV_R2: 0x40014DAA
DSI13_HV_R3: 0x40014DAB
DSI13_HV_R4: 0x40014DAC
DSI13_HV_R5: 0x40014DAD
DSI13_HV_R6: 0x40014DAE
DSI13_HV_R7: 0x40014DAF
DSI13_HV_R8: 0x40014DB0
DSI13_HV_R9: 0x40014DB1
DSI13_HV_R10: 0x40014DB2
DSI13_HV_R11: 0x40014DB3
DSI13_HV_R12: 0x40014DB4
DSI13_HV_R13: 0x40014DB5
DSI13_HV_R14: 0x40014DB6
DSI13_HV_R15: 0x40014DB7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	hv_byte							

DSI HV Tile Configuration

Bits	Name	Description
7:0	hv_byte[7:0]	RAM configuration for DSI channel bytes

1.3.1191 DSI[0..15]_DSIINP0

DSIINP0

Reset: N/A

Register : Address

DSI0_DSIINP0: 0x400140C0
DSI1_DSIINP0: 0x400141C0
DSI2_DSIINP0: 0x400142C0
DSI3_DSIINP0: 0x400143C0
DSI4_DSIINP0: 0x400144C0
DSI5_DSIINP0: 0x400145C0
DSI6_DSIINP0: 0x400146C0
DSI7_DSIINP0: 0x400147C0
DSI8_DSIINP0: 0x400148C0
DSI9_DSIINP0: 0x400149C0
DSI12_DSIINP0: 0x40014CC0
DSI13_DSIINP0: 0x40014DC0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1192 DSI[0..15]_DSIINP1

DSIINP1

Reset: N/A

Register : Address

DSI0_DSIINP1: 0x400140C2	DSI1_DSIINP1: 0x400141C2
DSI2_DSIINP1: 0x400142C2	DSI3_DSIINP1: 0x400143C2
DSI4_DSIINP1: 0x400144C2	DSI5_DSIINP1: 0x400145C2
DSI6_DSIINP1: 0x400146C2	DSI7_DSIINP1: 0x400147C2
DSI8_DSIINP1: 0x400148C2	DSI9_DSIINP1: 0x400149C2
DSI12_DSIINP1: 0x40014CC2	DSI13_DSIINP1: 0x40014DC2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1193 DSI[0..15]_DSIINP2

DSIINP2

Reset: N/A

Register : Address

DSI0_DSIINP2: 0x400140C4
DSI1_DSIINP2: 0x400141C4
DSI2_DSIINP2: 0x400142C4
DSI3_DSIINP2: 0x400143C4
DSI4_DSIINP2: 0x400144C4
DSI5_DSIINP2: 0x400145C4
DSI6_DSIINP2: 0x400146C4
DSI7_DSIINP2: 0x400147C4
DSI8_DSIINP2: 0x400148C4
DSI9_DSIINP2: 0x400149C4
DSI12_DSIINP2: 0x40014CC4
DSI13_DSIINP2: 0x40014DC4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1194 DSI[0..15]_DSIINP3

DSIINP3

Reset: N/A

Register : Address

DSI0_DSIINP3: 0x400140C6	DSI1_DSIINP3: 0x400141C6
DSI2_DSIINP3: 0x400142C6	DSI3_DSIINP3: 0x400143C6
DSI4_DSIINP3: 0x400144C6	DSI5_DSIINP3: 0x400145C6
DSI6_DSIINP3: 0x400146C6	DSI7_DSIINP3: 0x400147C6
DSI8_DSIINP3: 0x400148C6	DSI9_DSIINP3: 0x400149C6
DSI12_DSIINP3: 0x40014CC6	DSI13_DSIINP3: 0x40014DC6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1195 DSI[0..15]_DSIINP4

DSIINP4

Reset: N/A

Register : Address

DSI0_DSIINP4: 0x400140C8
DSI1_DSIINP4: 0x400141C8
DSI2_DSIINP4: 0x400142C8
DSI3_DSIINP4: 0x400143C8
DSI4_DSIINP4: 0x400144C8
DSI5_DSIINP4: 0x400145C8
DSI6_DSIINP4: 0x400146C8
DSI7_DSIINP4: 0x400147C8
DSI8_DSIINP4: 0x400148C8
DSI9_DSIINP4: 0x400149C8
DSI12_DSIINP4: 0x40014CC8
DSI13_DSIINP4: 0x40014DC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1196 DSI[0..15]_DSIINP5

DSIINP5

Reset: N/A

Register : Address

DSI0_DSIINP5: 0x400140CA	DSI1_DSIINP5: 0x400141CA
DSI2_DSIINP5: 0x400142CA	DSI3_DSIINP5: 0x400143CA
DSI4_DSIINP5: 0x400144CA	DSI5_DSIINP5: 0x400145CA
DSI6_DSIINP5: 0x400146CA	DSI7_DSIINP5: 0x400147CA
DSI8_DSIINP5: 0x400148CA	DSI9_DSIINP5: 0x400149CA
DSI12_DSIINP5: 0x40014CCA	DSI13_DSIINP5: 0x40014DCA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1197 DSI[0..15]_DSIOUTP0

DSIOUTP0

Reset: N/A

Register : Address

DSI0_DSIOUTP0: 0x400140CC	DSI1_DSIOUTP0: 0x400141CC
DSI2_DSIOUTP0: 0x400142CC	DSI3_DSIOUTP0: 0x400143CC
DSI4_DSIOUTP0: 0x400144CC	DSI5_DSIOUTP0: 0x400145CC
DSI6_DSIOUTP0: 0x400146CC	DSI7_DSIOUTP0: 0x400147CC
DSI8_DSIOUTP0: 0x400148CC	DSI9_DSIOUTP0: 0x400149CC
DSI12_DSIOUTP0: 0x40014CCC	DSI13_DSIOUTP0: 0x40014DCC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1198 DSI[0..15]_DSIOUTP1

DSIOUTP1

Reset: N/A

Register : Address

DSI0_DSIOUTP1: 0x400140CE	DSI1_DSIOUTP1: 0x400141CE
DSI2_DSIOUTP1: 0x400142CE	DSI3_DSIOUTP1: 0x400143CE
DSI4_DSIOUTP1: 0x400144CE	DSI5_DSIOUTP1: 0x400145CE
DSI6_DSIOUTP1: 0x400146CE	DSI7_DSIOUTP1: 0x400147CE
DSI8_DSIOUTP1: 0x400148CE	DSI9_DSIOUTP1: 0x400149CE
DSI12_DSIOUTP1: 0x40014CCE	DSI13_DSIOUTP1: 0x40014DCE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1199 DSI[0..15]_DSIOUTP2

DSIOUTP2

Reset: N/A

Register : Address

DSI0_DSIOUTP2: 0x400140D0	DSI1_DSIOUTP2: 0x400141D0
DSI2_DSIOUTP2: 0x400142D0	DSI3_DSIOUTP2: 0x400143D0
DSI4_DSIOUTP2: 0x400144D0	DSI5_DSIOUTP2: 0x400145D0
DSI6_DSIOUTP2: 0x400146D0	DSI7_DSIOUTP2: 0x400147D0
DSI8_DSIOUTP2: 0x400148D0	DSI9_DSIOUTP2: 0x400149D0
DSI12_DSIOUTP2: 0x40014CD0	DSI13_DSIOUTP2: 0x40014DD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1200 DSI[0..15]_DSIOUTP3

DSIOUTP3

Reset: N/A

Register : Address

DSI0_DSIOUTP3: 0x400140D2
DSI1_DSIOUTP3: 0x400141D2
DSI2_DSIOUTP3: 0x400142D2
DSI3_DSIOUTP3: 0x400143D2
DSI4_DSIOUTP3: 0x400144D2
DSI5_DSIOUTP3: 0x400145D2
DSI6_DSIOUTP3: 0x400146D2
DSI7_DSIOUTP3: 0x400147D2
DSI8_DSIOUTP3: 0x400148D2
DSI9_DSIOUTP3: 0x400149D2
DSI12_DSIOUTP3: 0x40014CD2
DSI13_DSIOUTP3: 0x40014DD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1201 DSI[0..15]_DSIOUTT0

DSIOUTT0

Reset: N/A

Register : Address

DSI0_DSIOUTT0: 0x400140D4
DSI1_DSIOUTT0: 0x400141D4
DSI2_DSIOUTT0: 0x400142D4
DSI3_DSIOUTT0: 0x400143D4
DSI4_DSIOUTT0: 0x400144D4
DSI5_DSIOUTT0: 0x400145D4
DSI6_DSIOUTT0: 0x400146D4
DSI7_DSIOUTT0: 0x400147D4
DSI8_DSIOUTT0: 0x400148D4
DSI9_DSIOUTT0: 0x400149D4
DSI12_DSIOUTT0: 0x40014CD4
DSI13_DSIOUTT0: 0x40014DD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1202 DSI[0..15]_DSIOUTT1

DSIOUTT1

Reset: N/A

Register : Address

DSI0_DSIOUTT1: 0x400140D6	DSI1_DSIOUTT1: 0x400141D6
DSI2_DSIOUTT1: 0x400142D6	DSI3_DSIOUTT1: 0x400143D6
DSI4_DSIOUTT1: 0x400144D6	DSI5_DSIOUTT1: 0x400145D6
DSI6_DSIOUTT1: 0x400146D6	DSI7_DSIOUTT1: 0x400147D6
DSI8_DSIOUTT1: 0x400148D6	DSI9_DSIOUTT1: 0x400149D6
DSI12_DSIOUTT1: 0x40014CD6	DSI13_DSIOUTT1: 0x40014DD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1203 DSI[0..15]_DSIOUTT2

DSIOUTT2

Reset: N/A

Register : Address

DSI0_DSIOUTT2: 0x400140D8
DSI1_DSIOUTT2: 0x400141D8
DSI2_DSIOUTT2: 0x400142D8
DSI3_DSIOUTT2: 0x400143D8
DSI4_DSIOUTT2: 0x400144D8
DSI5_DSIOUTT2: 0x400145D8
DSI6_DSIOUTT2: 0x400146D8
DSI7_DSIOUTT2: 0x400147D8
DSI8_DSIOUTT2: 0x400148D8
DSI9_DSIOUTT2: 0x400149D8
DSI12_DSIOUTT2: 0x40014CD8
DSI13_DSIOUTT2: 0x40014DD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1204 DSI[0..15]_DSIOUTT3

DSIOUTT3

Reset: N/A

Register : Address

DSI0_DSIOUTT3: 0x400140DA	DSI1_DSIOUTT3: 0x400141DA
DSI2_DSIOUTT3: 0x400142DA	DSI3_DSIOUTT3: 0x400143DA
DSI4_DSIOUTT3: 0x400144DA	DSI5_DSIOUTT3: 0x400145DA
DSI6_DSIOUTT3: 0x400146DA	DSI7_DSIOUTT3: 0x400147DA
DSI8_DSIOUTT3: 0x400148DA	DSI9_DSIOUTT3: 0x400149DA
DSI12_DSIOUTT3: 0x40014CDA	DSI13_DSIOUTT3: 0x40014DDA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1205 DSI[0..15]_DSIOUTT4

DSIOUTT4

Reset: N/A

Register : Address

DSI0_DSIOUTT4: 0x400140DC
DSI1_DSIOUTT4: 0x400141DC
DSI2_DSIOUTT4: 0x400142DC
DSI3_DSIOUTT4: 0x400143DC
DSI4_DSIOUTT4: 0x400144DC
DSI5_DSIOUTT4: 0x400145DC
DSI6_DSIOUTT4: 0x400146DC
DSI7_DSIOUTT4: 0x400147DC
DSI8_DSIOUTT4: 0x400148DC
DSI9_DSIOUTT4: 0x400149DC
DSI12_DSIOUTT4: 0x40014CDC
DSI13_DSIOUTT4: 0x40014DDC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1206 DSI[0..15]_DSIOUTT5

DSIOUTT5

Reset: N/A

Register : Address

DSI0_DSIOUTT5: 0x400140DE	DSI1_DSIOUTT5: 0x400141DE
DSI2_DSIOUTT5: 0x400142DE	DSI3_DSIOUTT5: 0x400143DE
DSI4_DSIOUTT5: 0x400144DE	DSI5_DSIOUTT5: 0x400145DE
DSI6_DSIOUTT5: 0x400146DE	DSI7_DSIOUTT5: 0x400147DE
DSI8_DSIOUTT5: 0x400148DE	DSI9_DSIOUTT5: 0x400149DE
DSI12_DSIOUTT5: 0x40014CDE	DSI13_DSIOUTT5: 0x40014DDE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1207 DSI[0..15]_VS0

VS0

Reset: N/A

Register : Address

DSI0_VS0: 0x400140E0	DSI1_VS0: 0x400141E0
DSI2_VS0: 0x400142E0	DSI3_VS0: 0x400143E0
DSI4_VS0: 0x400144E0	DSI5_VS0: 0x400145E0
DSI6_VS0: 0x400146E0	DSI7_VS0: 0x400147E0
DSI8_VS0: 0x400148E0	DSI9_VS0: 0x400149E0
DSI12_VS0: 0x40014CE0	DSI13_VS0: 0x40014DE0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1208 DSI[0..15]_VS1

VS1

Reset: N/A

Register : Address

DSI0_VS1: 0x400140E2	DSI1_VS1: 0x400141E2
DSI2_VS1: 0x400142E2	DSI3_VS1: 0x400143E2
DSI4_VS1: 0x400144E2	DSI5_VS1: 0x400145E2
DSI6_VS1: 0x400146E2	DSI7_VS1: 0x400147E2
DSI8_VS1: 0x400148E2	DSI9_VS1: 0x400149E2
DSI12_VS1: 0x40014CE2	DSI13_VS1: 0x40014DE2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1209 DSI[0..15]_VS2

VS2

Reset: N/A

Register : Address

DSI0_VS2: 0x400140E4	DSI1_VS2: 0x400141E4
DSI2_VS2: 0x400142E4	DSI3_VS2: 0x400143E4
DSI4_VS2: 0x400144E4	DSI5_VS2: 0x400145E4
DSI6_VS2: 0x400146E4	DSI7_VS2: 0x400147E4
DSI8_VS2: 0x400148E4	DSI9_VS2: 0x400149E4
DSI12_VS2: 0x40014CE4	DSI13_VS2: 0x40014DE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1210 DSI[0..15]_VS3

VS3

Reset: N/A

Register : Address

DSI0_VS3: 0x400140E6	DSI1_VS3: 0x400141E6
DSI2_VS3: 0x400142E6	DSI3_VS3: 0x400143E6
DSI4_VS3: 0x400144E6	DSI5_VS3: 0x400145E6
DSI6_VS3: 0x400146E6	DSI7_VS3: 0x400147E6
DSI8_VS3: 0x400148E6	DSI9_VS3: 0x400149E6
DSI12_VS3: 0x40014CE6	DSI13_VS3: 0x40014DE6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1211 DSI[0..15]_VS4

VS4

Reset: N/A

Register : Address

DSI0_VS4: 0x400140E8	DSI1_VS4: 0x400141E8
DSI2_VS4: 0x400142E8	DSI3_VS4: 0x400143E8
DSI4_VS4: 0x400144E8	DSI5_VS4: 0x400145E8
DSI6_VS4: 0x400146E8	DSI7_VS4: 0x400147E8
DSI8_VS4: 0x400148E8	DSI9_VS4: 0x400149E8
DSI12_VS4: 0x40014CE8	DSI13_VS4: 0x40014DE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1212 DSI[0..15]_VS5

VS5

Reset: N/A

Register : Address

DSI0_VS5: 0x400140EA	DSI1_VS5: 0x400141EA
DSI2_VS5: 0x400142EA	DSI3_VS5: 0x400143EA
DSI4_VS5: 0x400144EA	DSI5_VS5: 0x400145EA
DSI6_VS5: 0x400146EA	DSI7_VS5: 0x400147EA
DSI8_VS5: 0x400148EA	DSI9_VS5: 0x400149EA
DSI12_VS5: 0x40014CEA	DSI13_VS5: 0x40014DEA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1213 DSI[0..15]_VS6

VS6

Reset: N/A

Register : Address

DSI0_VS6: 0x400140EC	DSI1_VS6: 0x400141EC
DSI2_VS6: 0x400142EC	DSI3_VS6: 0x400143EC
DSI4_VS6: 0x400144EC	DSI5_VS6: 0x400145EC
DSI6_VS6: 0x400146EC	DSI7_VS6: 0x400147EC
DSI8_VS6: 0x400148EC	DSI9_VS6: 0x400149EC
DSI12_VS6: 0x40014CEC	DSI13_VS6: 0x40014DEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1214 DSI[0..15]_VS7

VS7

Reset: N/A

Register : Address

DSI0_VS7: 0x400140EE
DSI1_VS7: 0x400141EE
DSI2_VS7: 0x400142EE
DSI3_VS7: 0x400143EE
DSI4_VS7: 0x400144EE
DSI5_VS7: 0x400145EE
DSI6_VS7: 0x400146EE
DSI7_VS7: 0x400147EE
DSI8_VS7: 0x400148EE
DSI9_VS7: 0x400149EE
DSI12_VS7: 0x40014CEE
DSI13_VS7: 0x40014DEE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1215 BCTL[0..3]_MDCLK_EN

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_MDCLK_EN: 0x40015000 BCTL1_MDCLK_EN: 0x40015010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

digital clock enable

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-804.
6	DCEN6	Bank Clock Enable Control See Table 1-804.
5	DCEN5	Bank Clock Enable Control See Table 1-804.
4	DCEN4	Bank Clock Enable Control See Table 1-804.
3	DCEN3	Bank Clock Enable Control See Table 1-804.
2	DCEN2	Bank Clock Enable Control See Table 1-804.
1	DCEN1	Bank Clock Enable Control See Table 1-804.
0	DCEN0	Bank Clock Enable Control See Table 1-804.

Table 1-804. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

1.3.1216 BCTL[0..3]_MBCLK_EN

BCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_MBCLK_EN: 0x40015001 BCTL1_MBCLK_EN: 0x40015011

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						NC1	NC0	BCEN

bus clock enable

Bits	Name	Description
2	NC1	Spare register bit
1	NC0	Spare register bit
0	BCEN	Bank Clock Enable Control See Table 1-805.

Table 1-805. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

1.3.1217 BCTL[0..3]_WAIT_CFG

WAIT_CFG

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_WAIT_CFG: 0x40015002 BCTL1_WAIT_CFG: 0x40015012

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Name	WR_WRK_WAIT		RD_WRK_WAIT		WR_CFG_WAIT		RD_CFG_WAIT	

Wait State Configuration Register

Bits	Name	Description
7:6	WR_WRK_WAIT[1:0]	Wait States for Writing UDB Working Registers See Table 1-809.
5:4	RD_WRK_WAIT[1:0]	Wait States for Reading UDB Working Registers See Table 1-807.
3:2	WR_CFG_WAIT[1:0]	Wait States for Writing UDB Configuration See Table 1-808.
1:0	RD_CFG_WAIT[1:0]	Wait States for Reading UDB Configuration See Table 1-806.

Table 1-806. Bit field encoding: RD_CFG_WAIT_ENUM

Value	Name	Description
2'b00	FIVE_WAITS	5 wait states
2'b01	FOUR_WAITS	4 wait state
2'b10	THREE_WAITS	3 wait states
2'b11	ONE_WAITS	1 wait states

Table 1-807. Bit field encoding: RD_WRK_WAIT_ENUM

Value	Name	Description
2'b00	ONE_WAITS	1 wait states
2'b01	TWO_WAITS	2 wait state
2'b10	THREE_WAITS	3 wait states
2'b11	ZERO_WAITS	0 wait states

Table 1-808. Bit field encoding: WR_CFG_WAIT_ENUM

Value	Name	Description
2'b00	ONE_WAITS	1 wait state
2'b01	TWO_WAITS	2 wait states
2'b10	THREE_WAITS	3 wait states
2'b11	ZERO_WAITS	0 wait states

Table 1-809. Bit field encoding: WR_WRK_WAIT_ENUM

Value	Name	Description
2'b00	ONE_WAITS	1 wait states
2'b01	TWO_WAITS	2 wait state

1.3.1217 BCTL[0..3]_WAIT_CFG (continued)

Table 1-809. Bit field encoding: WR_WRK_WAIT_ENUM

2'b10	THREE_WAITS	3 wait states
2'b11	ZERO_WAITS	0 wait states

1.3.1218 BCTL[0..3]_BANK_CTL

BANK_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_BANK_CTL: 0x40015003 BCTL1_BANK_CTL: 0x40015013

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					GLBL_WR	DPARAM_TM	ROUTE_ENABLE	DIS_COR

Bank Control Register

Bits	Name	Description
3	GLBL_WR	Global Write Test Mode: The purpose of this bit is to accelerate configuration and working register writing for test purposes. When this bit is set, the bank is in global write mode. In this mode a set of UDBs or UDB channels are selected for writing in parallel based on the setting of the GUDB WR bits and GCH WR bits in the individual UDB. See Table 1-812.
2	DPARAM_TM	DPARAM Test Mode: The DP RAM (s8dparam_ram16x8) has two read ports, one connectred to the system bus (for configuration of the RAM), and one port that drives the DP control bits. When this bit is set, the DP RAM control port is connected to the system bus for reading (the system bus read port is tri-stated) See Table 1-811.
1	ROUTE_ENABLE	Route Enable: When this bit is a 0, all routing drivers are gated off to drive '0'. Also, all routing outputs are gated off to prevent high current states. After configuration, this bit may be enabled. See Table 1-813.
0	DIS_COR	Disable Clear On Read: The status registers have an automatic clear on read function to maintain firmware synchronization with UDB processing. When the system is stopped in debug mode, this bit can be used to prevent the statu from clearing on a debug read. It also prevents a read pop from the FIFO blocks. Only the top of FIFO can be read when this bit is set. See Table 1-810.

Table 1-810. Bit field encoding: COR_ENUM

Value	Name	Description
1'b0	ENABLE	Status register clear on read enabled (default)
1'b1	DISABLE	Status register clear on read disabled

Table 1-811. Bit field encoding: DPARAM_TM_ENUM

Value	Name	Description
1'b0	DISABLE	DPARAM test mode is disabled (default)
1'b1	ENABLE	DPARAM test mode is enabled

Table 1-812. Bit field encoding: GLBL_WR_ENUM

Value	Name	Description
1'b0	DISABLE	Global Write Test Mode is disabled (default)
1'b1	ENABLE	Global Write Test Mode enabled

1.3.1218 BCTL[0..3]_BANK_CTL (continued)

Table 1-813. Bit field encoding: ROUTE_ENABLE

Value	Name	Description
1'b0	DISABLE	Routing input drivers are gated off to '0' (default)
1'b1	ENABLE	Routing input drivers are enabled.

1.3.1219 BCTL[0..3]_DCLK_EN0

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN0: 0x40015008 BCTL1_DCLK_EN0: 0x40015018

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

digital clock enable

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-814.
6	DCEN6	Bank Clock Enable Control See Table 1-814.
5	DCEN5	Bank Clock Enable Control See Table 1-814.
4	DCEN4	Bank Clock Enable Control See Table 1-814.
3	DCEN3	Bank Clock Enable Control See Table 1-814.
2	DCEN2	Bank Clock Enable Control See Table 1-814.
1	DCEN1	Bank Clock Enable Control See Table 1-814.
0	DCEN0	Bank Clock Enable Control See Table 1-814.

Table 1-814. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

1.3.1220 BCTL[0..3]_BCLK_EN0

BCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_BCLK_EN0: 0x40015009 BCTL1_BCLK_EN0: 0x40015019

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				NC	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN

bus clock enable

Bits	Name	Description
4	NC	Spare register bit
3	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-816.
2	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When this bit is set, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes See Table 1-817.
1	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When this bit is set, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes See Table 1-818.
0	BCEN	Bank Clock Enable Control See Table 1-815.

Table 1-815. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

Table 1-816. Bit field encoding: DIS_ROUTE

Value	Name	Description
1'b0	ENABLE	The routing in this quadrant can be enabled with the bank route enable bit. (default)
1'b1	DISABLE	The routing in this quadrant is disabled and held in a benign state

Table 1-817. Bit field encoding: GCH_WR_HI

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for higher order address is disabled
1'b1	ENABLE	Global UDB channel configuration write for higher order address is enabled

1.3.1220 BCTL[0..3]_BCLK_EN0 (continued)

Table 1-818. Bit field encoding: GCH_WR_LO

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for lower order address is disabled
1'b1	ENABLE	Global UDB channel configuration write for lower order address is enabled

1.3.1221 BCTL[0..3]_DCLK_EN1

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN1: 0x4001500A BCTL1_DCLK_EN1: 0x4001501A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

digital clock enable

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-819.
6	DCEN6	Bank Clock Enable Control See Table 1-819.
5	DCEN5	Bank Clock Enable Control See Table 1-819.
4	DCEN4	Bank Clock Enable Control See Table 1-819.
3	DCEN3	Bank Clock Enable Control See Table 1-819.
2	DCEN2	Bank Clock Enable Control See Table 1-819.
1	DCEN1	Bank Clock Enable Control See Table 1-819.
0	DCEN0	Bank Clock Enable Control See Table 1-819.

Table 1-819. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

1.3.1222 BCTL[0..3]_BCLK_EN1

BCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_BCLK_EN1: 0x4001500B BCTL1_BCLK_EN1: 0x4001501B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				NC	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN

bus clock enable

Bits	Name	Description
4	NC	Spare register bit
3	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-821.
2	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When this bit is set, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes See Table 1-822.
1	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When this bit is set, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes See Table 1-823.
0	BCEN	Bank Clock Enable Control See Table 1-820.

Table 1-820. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

Table 1-821. Bit field encoding: DIS_ROUTE

Value	Name	Description
1'b0	ENABLE	The routing in this quadrant can be enabled with the bank route enable bit. (default)
1'b1	DISABLE	The routing in this quadrant is disabled and held in a benign state

Table 1-822. Bit field encoding: GCH_WR_HI

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for higher order address is disabled
1'b1	ENABLE	Global UDB channel configuration write for higher order address is enabled

1.3.1222 BCTL[0..3]_BCLK_EN1 (continued)

Table 1-823. Bit field encoding: GCH_WR_LO

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for lower order address is disabled
1'b1	ENABLE	Global UDB channel configuration write for lower order address is enabled

1.3.1223 BCTL[0..3]_DCLK_EN2

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN2: 0x4001500C BCTL1_DCLK_EN2: 0x4001501C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

digital clock enable

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-824.
6	DCEN6	Bank Clock Enable Control See Table 1-824.
5	DCEN5	Bank Clock Enable Control See Table 1-824.
4	DCEN4	Bank Clock Enable Control See Table 1-824.
3	DCEN3	Bank Clock Enable Control See Table 1-824.
2	DCEN2	Bank Clock Enable Control See Table 1-824.
1	DCEN1	Bank Clock Enable Control See Table 1-824.
0	DCEN0	Bank Clock Enable Control See Table 1-824.

Table 1-824. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

1.3.1224 BCTL[0..3]_BCLK_EN2

BCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_BCLK_EN2: 0x4001500D BCTL1_BCLK_EN2: 0x4001501D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				NC	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN

bus clock enable

Bits	Name	Description
4	NC	Spare register bit
3	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-826.
2	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When this bit is set, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes See Table 1-827.
1	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When this bit is set, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes See Table 1-828.
0	BCEN	Bank Clock Enable Control See Table 1-825.

Table 1-825. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

Table 1-826. Bit field encoding: DIS_ROUTE

Value	Name	Description
1'b0	ENABLE	The routing in this quadrant can be enabled with the bank route enable bit. (default)
1'b1	DISABLE	The routing in this quadrant is disabled and held in a benign state

Table 1-827. Bit field encoding: GCH_WR_HI

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for higher order address is disabled
1'b1	ENABLE	Global UDB channel configuration write for higher order address is enabled

1.3.1224 BCTL[0..3]_BCLK_EN2 (continued)

Table 1-828. Bit field encoding: GCH_WR_LO

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for lower order address is disabled
1'b1	ENABLE	Global UDB channel configuration write for lower order address is enabled

1.3.1225 BCTL[0..3]_DCLK_EN3

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN3: 0x4001500E BCTL1_DCLK_EN3: 0x4001501E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

digital clock enable

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-829.
6	DCEN6	Bank Clock Enable Control See Table 1-829.
5	DCEN5	Bank Clock Enable Control See Table 1-829.
4	DCEN4	Bank Clock Enable Control See Table 1-829.
3	DCEN3	Bank Clock Enable Control See Table 1-829.
2	DCEN2	Bank Clock Enable Control See Table 1-829.
1	DCEN1	Bank Clock Enable Control See Table 1-829.
0	DCEN0	Bank Clock Enable Control See Table 1-829.

Table 1-829. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

1.3.1226 BCTL[0..3]_BCLK_EN3

BCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_BCLK_EN3: 0x4001500F BCTL1_BCLK_EN3: 0x4001501F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Name				NC	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN

bus clock enable

Bits	Name	Description
4	NC	Spare register bit
3	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-831.
2	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When this bit is set, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes See Table 1-832.
1	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When this bit is set, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes See Table 1-833.
0	BCEN	Bank Clock Enable Control See Table 1-830.

Table 1-830. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled
1'b1	ENABLE	Digital Global clock is enabled

Table 1-831. Bit field encoding: DIS_ROUTE

Value	Name	Description
1'b0	ENABLE	The routing in this quadrant can be enabled with the bank route enable bit. (default)
1'b1	DISABLE	The routing in this quadrant is disabled and held in a benign state

Table 1-832. Bit field encoding: GCH_WR_HI

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for higher order address is disabled
1'b1	ENABLE	Global UDB channel configuration write for higher order address is enabled

1.3.1226 BCTL[0..3]_BCLK_EN3 (continued)

Table 1-833. Bit field encoding: GCH_WR_LO

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for lower order address is disabled
1'b1	ENABLE	Global UDB channel configuration write for lower order address is enabled

1.3.1227 IDMUX_IRQ_CTL[0..7]

Control Register IRQ_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IDMUX_IRQ_CTL0: 0x40015100
IDMUX_IRQ_CTL1: 0x40015101
IDMUX_IRQ_CTL2: 0x40015102
IDMUX_IRQ_CTL3: 0x40015103
IDMUX_IRQ_CTL4: 0x40015104
IDMUX_IRQ_CTL5: 0x40015105
IDMUX_IRQ_CTL6: 0x40015106
IDMUX_IRQ_CTL7: 0x40015107

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Name	ICTRL3		ICTRL2		ICTRL1		ICTRL0	

This register is used to configure the routing and processing of interrupts.

Bits	Name	Description
7:6	ICTRL3[1:0]	IRQ Control See Table 1-834.
5:4	ICTRL2[1:0]	IRQ Control See Table 1-834.
3:2	ICTRL1[1:0]	IRQ Control See Table 1-834.
1:0	ICTRL0[1:0]	IRQ Control See Table 1-834.

Table 1-834. Bit field encoding: irq_enum

Value	Name	Description
2'b00	Fixed Function	Fixed Function Interrupt.
2'b01	DMA	DMA Interrupt
2'b10	UDB	UDB Level Interrupt
2'b11	UDB EDGE	UDB Edge Detect Interrupt

1.3.1228 IDMUX_DRQ_CTL[0..5]

Configuration Register DRQ_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IDMUX_DRQ_CTL0: 0x40015110
IDMUX_DRQ_CTL1: 0x40015111
IDMUX_DRQ_CTL2: 0x40015112
IDMUX_DRQ_CTL3: 0x40015113
IDMUX_DRQ_CTL4: 0x40015114
IDMUX_DRQ_CTL5: 0x40015115

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Name	DCTRL3		DCTRL2		DCTRL1		DCTRL0	

This register is used to select between DMA requests (fixed function or udb).

Bits	Name	Description
7:6	DCTRL3[1:0]	DMA input type. See Table 1-835.
5:4	DCTRL2[1:0]	DMA input type. See Table 1-835.
3:2	DCTRL1[1:0]	DMA input type. See Table 1-835.
1:0	DCTRL0[1:0]	DMA input type. See Table 1-835.

Table 1-835. Bit field encoding: drq_enum

Value	Name	Description
2'b00	Fixed Function	Fixed Function DMA request.
2'b01	UDB	UDB Level DMA request
2'b10	UDB EDGE	UDB Edge Detect DMA request
2'b11	RESERVED	RESERVED

1.3.1229 P3BA_Y_START

Y_START

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_Y_START: 0x40050300

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R						
Name		y_start						

This register is used to store the Y address value of the target memory. It corresponds to the column address of the target memory on which the memory test begins. In case there is only one column in the memory, both y_start and the y_roll values have to be zero.

Bits	Name	Description
6:0	y_start[6:0]	This is the starting value of Y address.

1.3.1230 P3BA_YROLL

YROLL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_YROLL: 0x40050301

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R						
Name		y_roll						

This register is used to store the roll-over value of the Y address range for the target memory. It corresponds to the column address of the target memory, which value when reached by y_curr results in y_curr value rolling over to y_start or memory test being ended (refer to fast_x). The value depends on the physical map of the memory. In case there is only one column in the memory, both y_start and the y_roll values have to be zero.

Bits	Name	Description
6:0	y_roll[6:0]	This is the roll-over value for Y address.

1.3.1231 P3BA_YCFG

YCFG

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_YCFG: 0x40050302

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Name	y_sub	y_inc						

This register is used to store the increment/decrement step value for Y address and the direction of the increment. The y_inc corresponds to the data width of the memory (in bytes). In case there is only one column in the memory, the y_inc value has to be zero. The y_sub specifies if the y_curr has to be incremented by y_inc or decremented by y_inc. Care should be taken while setting this bit, so that the calculates y_curr always lies between y_start and y_roll.

Bits	Name	Description
7	y_sub	1'b0: y_curr is incremented by a value of y_inc. (y_sub can be 1'b0 only when y_roll >= y_start) 1'b1: y_curr is decremented by a value of y_inc. (y_sub can be 1'b0 only when y_roll <= y_start)
6:0	y_inc[6:0]	This is the increment/decrement step value for Y address.

1.3.1232 P3BA_X_START1

X_START1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_X_START1: 0x40050303

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	x_start1							

x_start is the starting value of X address and corresponds to the row address of the target memory on which the test begins. This register is used to store bits [7:0] of the x_start address of the target memory.

Bits	Name	Description
7:0	x_start1[7:0]	Bits (7:0) of x_start.

1.3.1233 P3BA_X_START2

X_START2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_X_START2: 0x40050304

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	x_start2							

This register is used to store bits [15:8] of the x_start address of the target memory.

Bits	Name	Description
7:0	x_start2[7:0]	Bits (15:8) of x_start.

1.3.1234 P3BA_XROLL1

XROLL1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_XROLL1: 0x40050305

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	x_roll1							

x_roll is the roll-over value of X address range for the target memory. It corresponds to the row address of the target memory, which value when reached by x_curr results in x_curr value rolling over to x_start or memory test being ended (refer to fast_x). The value depends on the physical map of the memory. This register is used to store bits [7:0] of the x_roll address of the target memory.

Bits	Name	Description
7:0	x_roll1[7:0]	Bits (7:0) of x_roll.

1.3.1235 P3BA_XROLL2

XROLL2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_XROLL2: 0x40050306

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	x_roll2							

This register is used to store bits [15:8] of the x_roll address of the target memory.

Bits	Name	Description
7:0	x_roll2[7:0]	Bits (15:8) of x_roll.

1.3.1236 P3BA_XINC

XINC

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_XINC: 0x40050307

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	x_inc							

This register is used to store the increment/decrement step value for Y address. The x_inc corresponds to the row address increment value of the target memory (in bytes).

Bits	Name	Description
7:0	x_inc[7:0]	This is the increment/decrement step value for X address. This depends on y_start and y_roll

1.3.1237 P3BA_XCFG

XCFG

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_XCFG: 0x40050308

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							fast_x	x_sub

This register is used to store the direction of the increment and the priority of increment. The x_sub specifies if the x_curr has to be incremented by y_inc or decremented by y_inc. Care should be taken while setting this bit, so that the calculated x_curr always lies between x_start and x_roll.

Bits	Name	Description
1	fast_x	This bit when set causes incrementing to occur primarily on x_curr (fast-x) instead of on y_curr (fast-y). See Table 1-836.
0	x_sub	1'b0: x_curr is incremented by a value of x_inc. (x_sub can be 1'b0 only when x_roll >= x_start) 1'b1: x_curr is decremented by a value of x_inc. (x_sub can be 1'b0 only when x_roll <= x_start)

Table 1-836. Bit field encoding: fast_x_enum

Value	Name	Description
1'b1	FAST_X	Fast X incrementing: x_curr increments/decrements for each sequence. y_curr increments/decrements when x_curr reaches x_roll. The memory test is terminated when both x_curr and y_curr reach the roll-over values.
1'b0	FAST_Y	Fast Y incrementing: y_curr increments/decrements for each sequence. x_curr increments/decrements when y_curr reaches y_roll. The memory test is terminated when both x_curr and y_curr reach the roll-over values.

1.3.1238 P3BA_OFFSETADDR1

OFFSETADDR1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_OFFSETADDR1: 0x40050309

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	offset_addr1							

The offset address (offset_addr) corresponds to the peripheral address of the target memory. This register is used to store bits (7:0) of the offset address.

Bits	Name	Description
7:0	offset_addr1[7:0]	Bits (7:0) of offset address.

1.3.1239 P3BA_OFFSETADDR2

OFFSETADDR2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_OFFSETADDR2: 0x4005030A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	offset_addr2							

This register is used to store bits (15:8) of the offset address.

Bits	Name	Description
7:0	offset_addr2[7:0]	Bits (15:8) of offset address.

1.3.1240 P3BA_OFFSETADDR3

OFFSETADDR3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_OFFSETADDR3: 0x4005030B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	offset_addr3							

This register is used to store bits (23:16) of the offset address.

Bits	Name	Description
7:0	offset_addr3[7:0]	Bits (23:16) of offset address.

1.3.1241 P3BA_ABSADDR1

ABSADDR1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_ABSADDR1: 0x4005030C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	abs_addr1							

The absolute address (abs_addr) corresponds to the complete address of a memory location in the target memory. Absolute address is generated by OR ing offset address (h), current X address (x) and current Y address (y) in the following manner hhhh_hhhh_hhhh_hhhh_0000_0000 0000_0000_xxxx_xxxx_xxxx_xxxx 0000_0000_0000_0000_0yyy_yyyy It can be seen that some of the bits overlap. In the overlapping bits, there should be no conflicting bits; only one of the address fields can have valid value and the other fields should have zero. For instance, in Leopard, while testing CAN memory the OR function would look like 0000_0000_1010_0000_0000_0000 0000_0000_0000_00xx_xxx0_0000 0000_0000_0000_0000_000y_yyyy In the above function, bits [23:12] corresponds to peripheral addressing, bits [9:2] corresponds to X address and bits [1:0] corresponds to Y address. There is no conflicting overlap. Similarly, for other memories there should be no conflicting overlaps. When read in debug mode this value corresponds to the address of the memory location on which the memory test was last done. This register is used to store bits (7:0) of the absolute address.

Bits	Name	Description
7:0	abs_addr1[7:0]	Bits (7:0) of the absolute address.

1.3.1242 P3BA_ABSADDR2

ABSADDR2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_ABSADDR2: 0x4005030D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	abs_addr2							

Register used to store bits (15:8) of the absolute address.

Bits	Name	Description
7:0	abs_addr2[7:0]	Bits (15:8) of the absolute address.

1.3.1243 P3BA_ABSADDR3

ABSADDR3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_ABSADDR3: 0x4005030E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	abs_addr3							

Register used to store bits (23:16) of the absolute address.

Bits	Name	Description
7:0	abs_addr3[7:0]	Bits (23:16) of the absolute address.

1.3.1244 P3BA_ABSADDR4

ABSADDR4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_ABSADDR4: 0x4005030F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	abs_addr4							

Register used to store bits (31:24) of the absolute address.

Bits	Name	Description
7:0	abs_addr4[7:0]	Bits (31:24) of the absolute address.

1.3.1245 P3BA_DATCFG1

DATCFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATCFG1: 0x40050310

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	data_invert_mask							

This register is used to store data inversion address mask. The data invert mask is an address pattern used to invert the data. The logic used to generate data invert signal is masked_addr = data_invert_mask[7:0] & mstr_haddr[7:0]; data_invert = ^(masked_addr); -- reduction XOR of masked_addr. Based on this data invert signal and the current opcode (regular or inverted), the data is either inverted or is used uninverted.

Bits	Name	Description
7:0	data_invert_mask[7:0]	The 8 bit data invert mask

1.3.1246 P3BA_DATCFG2

DATCFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATCFG2: 0x40050311

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:00		R/W:0
HW Access	NA					R		R
Name						data_pattern		data_ovr

This register contains the data override bit and data pattern. When a memory test is initiated, this bit is used either to replicate the data pattern into the data register or to override the data pattern and preserve the explicitly written contents of the data register The data pattern is the basic 2-bit pattern which, if data_ovr is not set, is replicated to generate data.

Bits	Name	Description
2:1	data_pattern[1:0]	Basic 2-bit data pattern.
0	data_ovr	1'b0: State machine enters INIT state and data pattern bits are replicated in the data_reg. 1'b1: State machine skips INIT state and the contents of the data_reg are preserved.

1.3.1247 P3BA_CMP_RSLT1

CMP_RSLT1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_CMP_RSLT1: 0x40050314

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	comp_rslt1							

The compare result (cmp_rslt) is the XOR'd result of registered hrdata and the expected data during master mode. The comparison is done only when a read operation is performed. This register contains bits (7:0) of the cmp_rslt.

Bits	Name	Description
7:0	comp_rslt1[7:0]	Bits(7:0) of the comp_rslt.

1.3.1248 P3BA_CMP_RSLT2

CMP_RSLT2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_CMP_RSLT2: 0x40050315

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	comp_rslt2							

This register contains bits (15:8) of the cmp_rslt.

Bits	Name	Description
7:0	comp_rslt2[7:0]	Bits(15:8) of the comp_rslt.

1.3.1249 P3BA_CMP_RSLT3

CMP_RSLT3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_CMP_RSLT3: 0x40050316

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	comp_rslt3							

This register contains bits (23:16) of the cmp_rslt.

Bits	Name	Description
7:0	comp_rslt3[7:0]	Bits(23:16) of the comp_rslt.

1.3.1250 P3BA_CMP_RSLT4

CMP_RSLT4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_CMP_RSLT4: 0x40050317

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	comp_rslt4							

This register contains bits (31:24) of the cmp_rslt.

Bits	Name	Description
7:0	comp_rslt4[7:0]	Bits(31:24) of the comp_rslt.

1.3.1251 P3BA_DATA_REG1

DATA_REG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATA_REG1: 0x40050318

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	data_reg1							

The data register (data_reg) stores the data that is used to write into the target memory. Data can directly be written into the register (and preserved during a memory test by setting data_ovr bit to 1'b1) or can be generated, when a memory test is initiated from the data_pattern, by setting data_ovr bit to 1'b0. This register contains bits (7:0) of the data_reg.

Bits	Name	Description
7:0	data_reg1[7:0]	Bits (7:0) of the data.

1.3.1252 P3BA_DATA_REG2

DATA_REG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATA_REG2: 0x40050319

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	data_reg2							

This register contains bits (15:8) of the data_reg.

Bits	Name	Description
7:0	data_reg2[7:0]	Bits (15:8) of the data.

1.3.1253 P3BA_DATA_REG3

DATA_REG3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATA_REG3: 0x4005031A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	data_reg3							

This register contains bits (23:16) of the data_reg.

Bits	Name	Description
7:0	data_reg3[7:0]	Bits (23:16) of the data.

1.3.1254 P3BA_DATA_REG4

DATA_REG4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_DATA_REG4: 0x4005031B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	data_reg4							

This register contains bits (31:24) of the data_reg.

Bits	Name	Description
7:0	data_reg4[7:0]	Bits (31:24) of the data.

1.3.1255 P3BA_EXP_DATA1

EXP_DATA1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_EXP_DATA1: 0x4005031C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	exp_data1							

The expected data (exp_data) is used to check if the data read from the target memory is correct. The expected data is generated from the data register and other factors including, mstr_hsize, bits24_true, data_invert_mask, abs_addr and opcode. This register contains bits (7:0) of exp_rslt.

Bits	Name	Description
7:0	exp_data1[7:0]	Bits (7:0) of the exp_data.

1.3.1256 P3BA_EXP_DATA2

EXP_DATA2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_EXP_DATA2: 0x4005031D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	exp_data2							

This register contains bits (15:8) of exp_rslt.

Bits	Name	Description
7:0	exp_data2[7:0]	Bits (15:8) of the exp_data.

1.3.1257 P3BA_EXP_DATA3

EXP_DATA3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_EXP_DATA3: 0x4005031E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	exp_data3							

This register contains bits (23:16) of exp_rslt.

Bits	Name	Description
7:0	exp_data3[7:0]	Bits (23:16) of the exp_data.

1.3.1258 P3BA_EXP_DATA4

EXP_DATA4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_EXP_DATA4: 0x4005031F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	exp_data4							

This register contains bits (31:24) of exp_rslt.

Bits	Name	Description
7:0	exp_data4[7:0]	Bits (31:24) of the exp_data.

1.3.1259 P3BA_MSTR_HRDATA1

MSTR_HRDATA1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_MSTR_HRDATA1: 0x40050320

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	mstr_hrdata1							

When a target memory location is read, the data is returned on the hrdata port on the master AHB interface. This data is registered as master hrdata (mstr_hrdata). This data is compared with exp_data to check if the read data is correct. This register contains bits (7:0) of the mstr_hrdata.

Bits	Name	Description
7:0	mstr_hrdata1[7:0]	Bits (7:0) of the mstr_hrdata.

1.3.1260 P3BA_MSTR_HRDATA2

MSTR_HRDATA2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_MSTR_HRDATA2: 0x40050321

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	mstr_hrdata2							

This register contains bits (15:8) of the mstr_hrdata.

Bits	Name	Description
7:0	mstr_hrdata2[7:0]	Bits (15:8) of the mstr_hrdata.

1.3.1261 P3BA_MSTR_HRDATA3

MSTR_HRDATA3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_MSTR_HRDATA3: 0x40050322

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	mstr_hrdata3							

This register contains bits (23:16) of the mstr_hrdata.

Bits	Name	Description
7:0	mstr_hrdata3[7:0]	Bits (23:16) of the mstr_hrdata.

1.3.1262 P3BA_MSTR_HRDATA4

MSTR_HRDATA4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_MSTR_HRDATA4: 0x40050323

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	mstr_hrdata4							

This register contains bits (31:24) of the mstr_hrdata.

Bits	Name	Description
7:0	mstr_hrdata4[7:0]	Bits (31:24) of the mstr_hrdata.

1.3.1263 P3BA_BIST_EN

BIST_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_BIST_EN: 0x40050324

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:1	R/W:0	R/W:0
HW Access	NA					R/W	R/W	R/W
Name						passing	init_compl	bist_go

This register is used to store the values for system control and initialization status bit. The bist_go bit, when set to 1'b1, initiates a memory test. When data_ovr bit is not set and when memory test is initiated, data initialization state is entered. During this state the data_reg is updated with data_pattern bits and the initialization complete (init_compl) bit is set. The passing bit is used to track the pass status of the memory test. Before starting a memory test the bit has to be set to 1'b1 by the software.

Bits	Name	Description
2	passing	This bit has to be set to 1'b1 before starting a memory test. During and at the end of a memory test if passing bit is 1'b0: A failure was encountered during the memory test. 1'b1: The memory test passed.
1	init_compl	1'b0: When data_ovr bit is set the init state is skipped. The init_compl bit is not set. 1'b1: When data_ovr bit is set the state machine enters init state, replicates data pattern bits in the data_reg and sets init_compl to 1'b1
0	bist_go	1'b0: The block is in slave mode. The slave AHB interface is active. The master AHB interface is inactive. 1'b1: The block enters master mode and a memory test in initiated. The master AHB interface is active. The slave AHB interface is inactive. The default bus master (a microcontroller) is stalled.

1.3.1264 P3BA_PHUB_MASTER_SSR

PHUB_MASTER_SSR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_PHUB_MASTER_SSR: 0x40050325

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:00	
HW Access	NA					R	R	
Name						bits24_true	mstr_hsize	

This register contains the mstr_hsize and bits24_true. The master AHB interface hsize (mstr_hsize) is used to specify the memory access data width. This should be equal to or less than the data width of the target memory. For example, the USB block has a data width of 16 bits then the Bist Assist block can perform a 16 bit memory access or an 8 bit memory access, but not a 32 bit memory access. The bits24_true is used to identify if the target memory is a 24 bit memory.

Bits	Name	Description
2	bits24_true	This bit is valid only when mstr_hsize is 2'b10. 1'b0: The target memory is a 32 bit memory. 1'b1: The target memory is a 24 bit memory. The MS byte of the data in all memory transactions are ignored
1:0	mstr_hsize[1:0]	This field is used to identify the size of the spoke for synchronization with PHUB.

1.3.1265 P3BA_SEQCFG1

SEQCFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_SEQCFG1: 0x40050326

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			R/W:000			R/W:1
HW Access	NA	R			R			R
Name		opcode_2			opcode_1			pre_address

This register is used to store the first two opcodes in the test sequence and the pre_address bit. The two opcodes will perform the first two operations in the state machine after the memory test is initiated. When the pre address bit is set, a single read is executed on the address corresponding to x_roll, y_roll and results ignored, immediately before executing the programmed sequence starting at the address corresponding to x_start, ystart. This provides full address transition coverage.

Bits	Name	Description
6:4	opcode_2[2:0]	second opcode See Table 1-837.
3:1	opcode_1[2:0]	first opcode See Table 1-837.
0	pre_address	1'b0: Pre address state is skipped. Sequence starts from address corresponding to x_address, y_address. 1'b1: Pre address state is entered and a single read on the address corresponding to x_roll, y_roll.

Table 1-837. Bit field encoding: opcode_enum

Value	Name	Description
3'b000	NOOP	Execute Wait State
3'b011	RDATA	Execute Read and compare with data
3'b100	RDATABAR	Execute Read and compare with inverted data
3'b001	WDATA	Execute Write with data
3'b010	WDATABAR	Execute Write with inverted data
3'b101	EXCLUDE	Do not execute anything. Skip opcode.

1.3.1266 P3BA_SEQCFG2

SEQCFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_SEQCFG2: 0x40050327

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:000			R/W:000		
HW Access	NA	R	R			R		
Name		bist_stop	opcode_4			opcode_3		

This register is used to store the last two opcodes in the test sequence and bist_stop bit. The two opcodes will perform the las two operations in the state machine after the memory test is initiated. The bit stop bit is used to enter the debug mode when a fail is encountered.

Bits	Name	Description
6	bist_stop	1'b0: The state machine does not stop when a fail is encountered. 1'b1: The state machine stops and enters debug mode when a fail is encountered.
5:3	opcode_4[2:0]	fourth opcode See Table 1-838.
2:0	opcode_3[2:0]	third opcode See Table 1-838.

Table 1-838. Bit field encoding: opcode_enum

Value	Name	Description
3'b000	NOOP	Execute Wait State
3'b011	RDATA	Execute Read and compare with data
3'b100	RDATABAR	Execute Read and compare with inverted data
3'b001	WDATA	Execute Write with data
3'b010	WDATABAR	Execute Write with inverted data
3'b101	EXCLUDE	Do not execute anything. Skip opcode.

1.3.1267 P3BA_Y_CURR

Y_CURR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_Y_CURR: 0x40050328

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R:0000000						
HW Access	NA	R/W						
Name		y_curr						

This register is used to store the current Y address value of the target memory. When read in debug mode it corresponds to the column address of the memory location on which the memory test was last done.

Bits	Name	Description
6:0	y_curr[6:0]	This is the current value of Y address. Counter

1.3.1268 P3BA_X_CURR1

X_CURR1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_X_CURR1: 0x40050329

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	x_curr1							

This register is used to store the current X address value of the target memory. When read in debug mode it corresponds to the row address of the memory location on which the memory test was last done. This register is used to store bits [7:0] of the current X address value of the target memory.

Bits	Name	Description
7:0	x_curr1[7:0]	Bits (7:0) of x_curr Counter

1.3.1269 P3BA_X_CURR2

X_CURR2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

P3BA_X_CURR2: 0x4005032A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	x_curr2							

Register is used to store bits [15:8] of the current X address value of the target memory.

Bits	Name	Description
7:0	x_curr2[7:0]	Bits (15:8) of x_curr Counter

1.3.1270 PANTHER_STCALIB_CFG

SYSTICK Calibration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_STCALIB_CFG: 0x40080000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	TENMS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	TENMS							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	TENMS							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:0	R/W:0	R:000000					
HW Access	R/W	R/W	R/W					
Name	NOREF	SKEW	RESERVED					

Note that this register is driven to the NVIC.SYSTICK_CAL register. This register is used to adjust the SYSTICK timer to be exactly 10ms. Note that software should only write to this register during boot and immediately after the clock frequency has been determined for the CPU and the SYSTICK timer reference input. See Chapter 14 of The Definitive Guide to the ARM Cortex-M3.

Bits	Name	Description
31	NOREF	NOREF is set to 1 when there is no reference clock. Software should use the CPU clock.
30	SKEW	When SKEW is set to 1, the calibration value is not exactly 10 milliseconds due to the clock frequency. The accuracy of the timer may not be suitable for Real-Time applications. IF the clock period is not an integral number of 10ms then this bit should be set.
29:24	RESERVED[5:0]	NA
23:0	TENMS[23:0]	Calibration value for the Ten Millisecond timer. This value is normally copied into the RELOAD register by software to achieve 10ms.

1.3.1271 PANTHER_WAITPIPE

Wait State Pipeline

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_WAITPIPE: 0x40080004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R:0	R/W:0	R/W:0	NA:0
HW Access	NA			R/W	R/W	R/W	R/W	NA
Name				CM3_TRACECLKIN_SRCSEL	RESERVED	CM3_SYSTCK_SRCSEL	NMI_SRCSEL	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This bit enables a set of pipelines that enable high Megahertz clock operation. The pipeline should be enabled when the CPU is clocking at or above ???TBD??? MHz. All transactions thru the PHUB will incurr a 1 cycle wait-state when the pipeline is enabled.

Bits	Name	Description
4	CM3_TRACECLKIN_SRCSEL	CM3 TRACECLKIN SOURCE SELECTION. 1= EXT Clock provided on SWD clock pin. 0= CPU clock divided by 2
3	RESERVED	NA
2	CM3_SYSTCK_SRCSEL	SYSTCK SOURCE SELECTION. 1= DSI cm3_dsi_stclksrc clock (connected to dsi_01_out_p_13). 0= 100KHz Slow Clock
1	NMI_SRCSEL	NMI SOURCE SELECTION. 1=Selects DSI_01_OUT_P_14 as NMI source. 0=Tied-off. Default tied-off.

1.3.1272 PANTHER_TRACE_CFG

Debug Trace Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_TRACE_CFG: 0x40080008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R/W	R/W
Name							TRACE_MODE	SWV_MODE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Enable the Serial Wire Viewer (SWV) mode. Only 1 of the following 2 modes should enabled at a time. If both modes are enabled, then the TRACE mode is output.

Bits	Name	Description
1	TRACE_MODE	Trace Mode. 1=Trace Mode enable. Trace Data is on GPIO pins P2.7-P2.4. TRACECLK is on P2.3. 0=Normal operation. Trace disabled.
0	SWV_MODE	SWV Mode. 1=SWV Mode enable. SWV Data is on GPIO pin P2.3. 0=Normal operation. SWV disabled.

1.3.1273 PANTHER_ETMFIFO

Embedded Trace Overflow Stall

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_ETMFIFO: 0x4008000C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R/W	R/W
Name							BOOT_CM3SYSRST_BYPASS	EMTOF-LOW

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Prevent the ETM FIFO from overflowing by stalling the CPU until the FIFO has enough room for more trace data.

Bits	Name	Description
1	BOOT_CM3SYSRST_BYPASS	0 --> no effect 1 --> bypasses the CM3 system reset during boot.
0	EMTOFLOW	The CM3 has built in Embedded Trace logic which compresses the trace data so it can be transferred in real-time. However, this compression can cause the FIFO in the ETM logic to overflow. When the ETM fifo fills, this bit can be used to either cause the CPU to stall until there is enough room for more data in the FIFO, or to simply loose data and not stall the CPU. 1=CPU will free-run even if the ETM FIFO is full. Trace data will be lost. 0=CPU will stall when the ETM FIFO is full.

1.3.1274 PANTHER_PVTCFG1

PVT Controller CFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_PVTCFG1: 0x40080010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								PVT_ENABLE1

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This configuration register is used for PVT controller bit fields. The only bit used right now is bit [0].

Bits	Name	Description
0	PVT_ENABLE1	This bit is used along with bit [0] of the PVTCFG2 register to provide the enable for the PVT to switch control of the VNWELL over to the VIDAC and remove the VNWELL short. This safety mechanism keeps SW from accidently enabling the analog mux. 1= If PVTCFG2 bit[0] = 1, this signal will switch the analog mux so the VNWELL can be controlled by the VIDAC output voltage. 0= The analug mux will keep the VNWELL connected to the existing short.

1.3.1275 PANTHER_PVTCFG2

PVT Controller CFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PANTHER_PVTCFG2: 0x40080014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								PVT_ENABLE2

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This configuration register is used for PVT controller bit fields. The only bit used right now is bit [0].

Bits	Name	Description
0	PVT_ENABLE2	This bit is used along with bit [0] of the PVTCFG1 register to provide the enable for the PVT to switch control of the VNWELL over to the VIDAC and remove the VNWELL short. This safety mechanism keeps SW from accidently enabling the analog mux. 1= If PVTCFG1 bit[0] = 1, this signal will switch the analog mux so the VNWELL can be controlled by the VIDAC output voltage. 0= The analug mux will keep the VNWELL connected to the existing short.

1.3.1276 EXTMEM_DATA[0..16777215]

DATA

Reset: N/A

Register : Address

EXTMEM_DATA: 0x60000000-0x60FFFFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	data							

(no description)

Bits	Name	Description
7:0	data[7:0]	(no description)

1.3.1277 ITM_TRACE_EN

ITM Trace Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_TRACE_EN: 0xE0000E00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	STIMENA							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	STIMENA							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	STIMENA							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	STIMENA							

Use the Trace Enable Register to generate trace data by writing to the corresponding stimulus port.

Bits	Name	Description
31:0	STIMENA[31:0]	Bit mask to enable tracing on ITM stimulus ports. One bit per stimulus port.

1.3.1278 ITM_TRACE_PRIVILEGE

ITM Trace Privilege Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_TRACE_PRIVILEGE: 0xE0000E40

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R/W			
Name					PRIVMASK			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the ITM Trace Privilege Register to enable an operating system to control which stimulus ports are accessible by user code.

Bits	Name	Description
3:0	PRIVMASK[3:0]	Bit mask to enable tracing on ITM stimulus ports: bit [0] = stimulus ports [7:0] bit [1] = stimulus ports [15:8] bit [2] = stimulus ports [23:16] bit [3] = stimulus ports [31:24]

1.3.1279 ITM_TRACE_CTRL

ITM Trace Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_TRACE_CTRL: 0xE0000E80

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R/W	R/W	R/W	R/W	R/W
Name				SWOENA	DWTENA	SYNCENA	TSENA	ITMENA

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R/W	
Name							TSPrescale	

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R/W	R/W						
Name	BUSY	ATBID						

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use this register to configure and control ITM transfers.

Bits	Name	Description
23	BUSY	Set when ITM events present and being drained
22:16	ATBID[6:0]	ATB ID for CoreSight system.
9:8	TSPrescale[1:0]	Timestamp prescaler: 0b00 = no prescaling 0b01 = divide by 4 0b10 = divide by 16 0b11 = divide by 64.
4	SWOENA	Enable SWV behavior - count on TPIUEMIT and TPIUBAUD.
3	DWTENA	Enables the DWT stimulus.
2	SYNCENA	Enables sync packets for TPIU.
1	TSENA	Enables differential timestamps. Differential timestamps are emitted when a packet is written to the FIFO with a non-zero timestamp counter, and when the timestamp counter overflows. Timestamps are emitted during idle times after a fixed number of cycles. This provides a time reference for packets and inter-packet gaps.

1.3.1279 ITM_TRACE_CTRL (continued)

0	ITMENA	Enable ITM. This is the master enable, and must be set before ITM Stimulus and Trace Enable registers can be written.

1.3.1280 ITM_INTEGRATION_WRITE

ITM Integration Write Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_INTEGRATION_WRITE: 0xE0000EF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							W:0
HW Access	NA							R/W
Name								ATVALIDM

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use this register to determine the behavior of the ATVALIDM bit.

Bits	Name	Description
0	ATVALIDM	When the integration mode is set: 0 = ATVALIDM clear 1 = ATVALIDM set.

1.3.1281 ITM_INTEGRATION_READ

ITM Integration Read Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_INTEGRATION_READ: 0xE0000EFC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R:0
HW Access	NA							R/W
Name								ATREADYM

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use this register to read the value of the ATREADYM bit.

Bits	Name	Description
0	ATREADYM	Value on ATREADYM

1.3.1282 ITM_INTEGRATION_MODE_CRTL

ITM Integration Mode Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_INTEGRATION_MODE_CRTL: 0xE0000F00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								INTEGRA-TION

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use this register to enable write accesses to the Control Register.

Bits	Name	Description
0	INTEGRATION	0 = ATVALIDM normal 1 = ATVALIDM driven from Integration Write Register

1.3.1283 ITM_LOCK_ACCESS

ITM Lock Access Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_LOCK_ACCESS: 0xE0000FB0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R/W							
Name	lock_access							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	W:00000000							
HW Access	R/W							
Name	lock_access							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	W:00000000							
HW Access	R/W							
Name	lock_access							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	W:00000000							
HW Access	R/W							
Name	lock_access							

Use this register to prevent write accesses to the Control Register.

Bits	Name	Description
31:0	lock_access[31:0]	A privileged write of 0xC5ACCE55 enables more write access to Control Register 0xE00::0xFFC. An invalid write removes write access.

1.3.1284 ITM_LOCK_STATUS

ITM Lock Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_LOCK_STATUS: 0xE0000FB4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R:0	R:0	R:0
HW Access	NA					R/W	R/W	R/W
Name						ByteAcc	Access	Present

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use this register to enable write accesses to the Control Register.

Bits	Name	Description
2	ByteAcc	You cannot implement 8-bit lock accesses.
1	Access	Write access to component is blocked. All writes are ignored, reads are permitted.
0	Present	Indicates that a lock mechanism exists for this component.

1.3.1285 ITM_PID4

ITM Peripheral Identification Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID4: 0xE0000FD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000100							
HW Access	R/W							
Name	PID4							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID4[7:0]	Peripheral Identification Register 4

1.3.1286 ITM_PID5

ITM Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID5: 0xE0000FD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID5							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID5[7:0]	Peripheral Identification Register 5

1.3.1287 ITM_PID6

ITM Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID6: 0xE0000FD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID6							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID6[7:0]	Peripheral Identification Register 6

1.3.1288 ITM_PID7

ITM Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID7: 0xE0000FDC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID7							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID7[7:0]	Peripheral Identification Register 7

1.3.1289 ITM_PID0

ITM Peripheral Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID0: 0xE0000FE0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000001							
HW Access	R/W							
Name	PID0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID0[7:0]	Peripheral Identification Register 0

1.3.1290 ITM_PID1

ITM Peripheral Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID1: 0xE0000FE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10110000							
HW Access	R/W							
Name	PID1							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID1[7:0]	Peripheral Identification Register 1

1.3.1291 ITM_PID2

ITM Peripheral Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID2: 0xE0000FE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00011011							
HW Access	R/W							
Name	PID2							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID2[7:0]	Peripheral Identification Register 2

1.3.1292 ITM_PID3

ITM Peripheral Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_PID3: 0xE0000FEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID3							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID3[7:0]	Peripheral Identification Register 3

1.3.1293 ITM_CID0

ITM Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_CID0: 0xE0000FF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00001101							
HW Access	R/W							
Name	CID0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID0[7:0]	Component Identification Register 0

1.3.1294 ITM_CID1

ITM Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_CID1: 0xE0000FF4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:11100000							
HW Access	R/W							
Name	CID1							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID1[7:0]	Component Identification Register 1

1.3.1295 ITM_CID2

ITM Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_CID2: 0xE0000FF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000101							
HW Access	R/W							
Name	CID2							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID2[7:0]	Component Identification Register 2

1.3.1296 ITM_CID3

ITM Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ITM_CID3: 0xE0000FFC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10110001							
HW Access	R/W							
Name	CID3							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID3[7:0]	Component Identification Register 3

1.3.1297 DWT_CTRL

DWT Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_CTRL: 0xE0001000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000			R/W:0000				R/W:0
HW Access	R/W			R/W				R/W
Name	POSTCNT			POSTPRESET				CYCCNTE-NA

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/W:0	R/W:00		R/W:0	R/W:0
HW Access	NA			R/W	R/W		R/W	R/W
Name				PCSAM-PLEENA	SYNCTAP		CYCTAP	POSTCNT

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name		CYCEVTEN	FOLDEVTE NA	LSUEVTE-NA	SLEEPE-VTENA	EXCEVTE-NA	CPIEVTE-NA	EXCTRCE-NA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:0100				NA:0000			
HW Access	R/W				NA			
Name	NUMCOMP							

Use the DWT Control Register to enable the DWT unit.

Bits	Name	Description
31:28	NUMCOMP[3:0]	Number of comparators field. This read-only field contains b0100 to indicate four comparators.
22	CYCEVTEN	Enables Cycle count event. Emits an event when the POSTCNT counter triggers it. See CYCTAP (bit [9]) and POSTPRESET, bits [4:1], for details. 1 = Cycle count events enabled 0 = Cycle count events disabled. This event is only emitted if PCSAMPLENA, bit [12], is disabled. PCSAMPLENA overrides the setting of this bit. Reset clears the CYCEVTENA bit.
21	FOLDEVTENA	Enables Folded instruction count event. Emits an event when DWT_FOLDCNT overflows (every 256 cycles of folded instructions). A folded instruction is one that does not incur even one cycle to execute. For example, an IT instruction is folded away and so does not use up one cycle. 1 = Folded instruction count events enabled. 0 = Folded instruction count events disabled. Reset clears the FOLDEVTENA bit.

1.3.1297 DWT_CTRL (continued)

20	LSUEVTENA	Enables LSU count event. Emits an event when DWT_LSUCNT overflows (every 256 cycles of LSU operation). LSU counts include all LSU costs after the initial cycle for the instruction. 1 = LSU count events enabled. 0 = LSU count events disabled. Reset clears the LSUEVTENA bit.
19	SLEEPEVTENA	Enables Sleep count event. Emits an event when DWT_SLEEPCNT overflows (every 256 cycles that the processor is sleeping). 1 = Sleep count events enabled. 0 = Sleep count events disabled. Reset clears the SLEEPEVTENA bit.
18	EXCEVTENA	Enables Interrupt overhead event. Emits an event when DWT_EXCCNT overflows (every 256 cycles of interrupt overhead). 1 = Interrupt overhead event enabled. 0 = Interrupt overhead event disabled. Reset clears the EXCEVTENA bit.
17	CPIEVTENA	Enables CPI count event. Emits an event when DWT_CPICNT overflows (every 256 cycles of multi-cycle instructions). 1 = CPI counter events enabled. 0 = CPI counter events disabled. Reset clears the CPIEVTENA bit.
16	EXCTRCENA	Enables Interrupt event tracing: 1 = interrupt event trace enabled 0 = interrupt event trace disabled. Reset clears the EXCEVTENA bit.
12	PCSAMPLEENA	Enables PC Sampling event. A PC sample event is emitted when the POSTCNT counter triggers it. See CYCTAP, bit [9], and POSTPRESET, bits [4:1], for details. Enabling this bit overrides CYCEVTENA (bit [20]). 1 = PC Sampling event enabled. 0 = PC Sampling event disabled. Reset clears the PCSAMPLENA bit.
11:10	SYNCTAP[1:0]	Feeds a synchronization pulse to the ITM SYNCENA control. The value selected here picks the rate (approximately 1/second or less) by selecting a tap on the DWT_CYCCNT register. To use synchronization (heartbeat and hot-connect synchronization), CYCCNTENA must be set to 1, SYNCTAP must be set to one of its values, and SYNCENA must be set to 1. 0b00 = Disabled. No synch counting. 0b01 = Tap at CYCCNT bit 24. 0b10 = Tap at CYCCNT bit 26. 0b11 = Tap at CYCCNT bit 28.
9	CYCTAP	Selects a tap on the DWT_CYCCNT register. These are spaced at bits [6] and [10]: CYCTAP = 0 selects bit [6] to tap CYCTAP = 1 selects bit [10] to tap. When the selected bit in the CYCCNT register changes from 0 to 1 or 1 to 0, it emits into the POSTCNT, bits [8:5], post-scalar counter. That counter then counts down. On a bit change when post-scalar is 0, it triggers an event for PC sampling or CYCEVTCNT.
8:5	POSTCNT[3:0]	Post-scalar counter for CYCTAP. When the selected tapped bit changes from 0 to 1 or 1 to 0, the post scalar counter is down-counted when not 0. If 0, it triggers an event for PCSAMPLENA or CYCEVTENA use. It also reloads with the value from POSTPRESET (bits [4:1]).

1.3.1297 DWT_CTRL (continued)

4:1	POSTPRESET[3:0]	Reload value for POSTCNT, bits [8:5], post-scalar counter. If this value is 0, events are triggered on each tap change (a power of 2, such as 1<<6 or 1<<10). If this field has a non-0 value, this forms a count-down value, to be reloaded into POSTCNT each time it reaches 0. For example, a value 1 in this register means an event is formed every other tap change.
0	CYCCNTENA	Enable the CYCCNT counter. If not enabled, the counter does not count and no event is generated for PS sampling or CYCCNTENA. In normal use, the debugger must initialize the CYCCNT counter to 0.

1.3.1298 DWT_CYCLE_COUNT

DWT Current PC Sampler Cycle Count Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_CYCLE_COUNT: 0xE0001004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	CYCCNT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	CYCCNT							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	CYCCNT							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	CYCCNT							

Use the DWT Current PC Sampler Cycle Count Register to count the number of core cycles. This count can measure elapsed execution time.

Bits	Name	Description
31:0	CYCCNT[31:0]	Current PC Sampler Cycle Counter count value. When enabled, this counter counts the number of core cycles, except when the core is halted. CYCCNT is a free running counter, counting upwards. It wraps around to 0 on overflow. The debugger must initialize this to 0 when first enabling.

1.3.1299 DWT_CPI_COUNT

DWT CPI Count Register

Reset: N/A

Register : Address

DWT_CPI_COUNT: 0xE0001008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CPICNT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT CPI Count Register to count the total number of instruction cycles beyond the first cycle.

Bits	Name	Description
7:0	CPICNT[7:0]	Current CPI counter value. Increments on the additional cycles (the first cycle is not counted) required to execute all instructions except those recorded by DWT_LSUCNT. This counter also increments on all instruction fetch stalls. If CPIEVTENA is set, an event is emitted when the counter overflows. Clears to 0 on enabling.

1.3.1300 DWT_EXC_OVHD_COUNT

DWT Exception Overhead Count Register

Reset: N/A

Register : Address

DWT_EXC_OVHD_COUNT: 0xE000100C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	EXCCNT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT Exception Overhead Count Register to count the total cycles spent in interrupt processing.

Bits	Name	Description
7:0	EXCCNT[7:0]	Current interrupt overhead counter value. Counts the total cycles spent in interrupt processing (for example entry stacking, return unstacking, pre-emption). An event is emitted on counter overflow (every 256 cycles). This counter initializes to 0 when enabled. Clears to 0 on enabling.

1.3.1301 DWT_SLEEP_COUNT

DWT Sleep Count Register

Reset: N/A

Register : Address

DWT_SLEEP_COUNT: 0xE0001010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SLEEPCNT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT Sleep Count Register to count the total number of cycles during which the processor is sleeping.

Bits	Name	Description
7:0	SLEEPCNT[7:0]	Sleep counter. Counts the number of cycles during which the processor is sleeping. An event is emitted on counter overflow (every 256 cycles). This counter initializes to 0 when enabled.

1.3.1302 DWT_LSU_COUNT

DWT LSU Count Register

Reset: N/A

Register : Address

DWT_LSU_COUNT: 0xE0001014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	LSUCNT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT LSU Count Register to count the total number of cycles during which the processor is processing an LSU operation beyond the first cycle.

Bits	Name	Description
7:0	LSUCNT[7:0]	LSU counter. This counts the total number of cycles that the processor is processing an LSU operation. The initial execution cost of the instruction is not counted. For example, an LDR that takes two cycles to complete increments this counter one cycle. Equivalently, an LDR that stalls for two cycles (and so takes four cycles), increments this counter three times. An event is emitted on counter overflow (every 256 cycles). Clears to 0 on enabling.

1.3.1303 DWT_FOLD_COUNT

DWT Fold Count Register

Reset: N/A

Register : Address

DWT_FOLD_COUNT: 0xE0001018

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	FOLDCNT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT Fold Count Register to count the total number of folded instructions. This counts 1 for each instruction that takes 0 cycles.

Bits	Name	Description
7:0	FOLDCNT[7:0]	This counts the total number folded instructions. This counter initializes to 0 when enabled.

1.3.1304 DWT_PC_SAMPLE

DWT Program Counter Sample Register

Reset: N/A

Register : Address

DWT_PC_SAMPLE: 0xE000101C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	EIASAMPLE							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	EIASAMPLE							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	EIASAMPLE							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	EIASAMPLE							

Use the DWT Program Counter Sample Register (PCSR) to enable coarse-grained software profiling using a debug agent, without changing the currently executing code. If the core is not in debug state, the value returned is the instruction address of a recently executed instruction. If the core is in debug state, the value returned is 0xFFFFFFFF.

Bits	Name	Description
31:0	EIASAMPLE[31:0]	Execution instruction address sample, or 0xFFFFFFFF if the core is halted.

1.3.1305 DWT_COMP_0

DWT Comparator Registers

Reset: N/A

Register : Address

DWT_COMP_0: 0xE0001020

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Use the DWT Comparator Registers 0-3 to write the values that trigger watchpoint events.

Bits	Name	Description
31:0	COMP[31:0]	Data value to compare against PC and the data address as given by DWT_FUNCTIONx. DWT_COMP0 can also compare against the value of the PC Sampler Counter (DWT_CYCCNT). DWT_COMP1 can also compare against data values so that data matching can be performed (DATAVMATCH).

1.3.1306 DWT_MASK_0

DWT Mask Registers

Reset: N/A

Register : Address

DWT_MASK_0: 0xE0001024

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:UUUU			
HW Access	NA				R/W			
Name					MASK			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT Mask Registers 0-3 to apply a mask to data addresses when matching against COMP.

Bits	Name	Description
3:0	MASK[3:0]	Mask on data address when matching against COMP. This is the size of the ignore mask. So, ~0< However, the actual comparison is slightly more complex to enable matching an address wherever it appears on a bus. So, if COMP is 3, this matches a word access of 0, because 3 would be within the word.

1.3.1307 DWT_FUNCTION_0

DWT Function registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_FUNCTION_0: 0xE0001028

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0000			
HW Access	R/W	NA	R/W	NA	R/W			
Name	CYC-MATCH		EMI-TRANGE		FUNCTION			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:0000				R/W:00		R/W:0	R/W:0
HW Access	R/W				R/W		R/W	R/W
Name	DATAVADDR0				DATAVSIZE		LNK1ENA	DATAV-MATCH

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R/W			
Name					DATAVADDR1			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								MATCHED

Use the DWT Function Registers 0-3 to control the operation of the comparator. Each comparator can: Match against either the PC or the data address. This is controlled by CYCMATCH. This function is only available for comparator 0 (DWT_COMP0). Perform data value comparisons if associated address comparators have performed an address match. This function is only available for comparator 1 (DWT_COMP1). Emit data or PC couples, trigger the ETM, or generate a watchpoint depending on the operation defined by FUNCTION.

Bits	Name	Description
24	MATCHED	This bit is set when the comparator matches, and indicates that the operation defined by FUNC-TION has occurred since this bit was last read. This bit is cleared on read.
19:16	DATAVADDR1[3:0]	Identity of a second linked address comparator for data value matching when DATAVMATCH == 1 and LNK1ENA == 1.
15:12	DATAVADDR0[3:0]	Identity of a linked address comparator for data value matching when DATAVMATCH == 1.
11:10	DATAVSIZE[1:0]	Defines the size of the data in the COMP register that is to be matched: 00 = byte 01 = halfword 10 = word 11 = Unpredictable.

1.3.1307 DWT_FUNCTION_0 (continued)

9	LNK1ENA	Read-only: 0 = DATAVADDR1 not supported 1 = DATAVADDR1 supported (enabled).
8	DATAVMATCH	This bit is only available in comparator 1. When DATAVMATCH is set, this comparator performs data value compares. The comparators given by DATAVADDR0 and DATAVADDR1provide the address for the data comparison. If DATAVMATCH is set in DWT_FUNCTION1, the FUNCTION setting for the comparators given by DATAVADDR0 and DATAVADDR1 are overridden and those comparators only provide the address match for the data comparison.
7	CYCMATCH	Only available in comparator 0. When set, this comparator compares against the clock cycle counter.
5	EMITRANGE	Emit range field. Reserved to permit emitting offset when range match occurs. Reset clears the EMITRANGE bit. PC sampling is not supported when EMITRANGE is enabled. EMITRANGE only applies for: FUNCTION = b0001, b0010, and b0011.
3:0	FUNCTION[3:0]	Function settings of the DWT Function Registers.

1.3.1308 DWT_COMP_1

DWT Comparator Registers

Reset: N/A

Register : Address

DWT_COMP_1: 0xE0001030

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Use the DWT Comparator Registers 0-3 to write the values that trigger watchpoint events.

Bits	Name	Description
31:0	COMP[31:0]	Data value to compare against PC and the data address as given by DWT_FUNCTIONx. DWT_COMP0 can also compare against the value of the PC Sampler Counter (DWT_CYCCNT). DWT_COMP1 can also compare against data values so that data matching can be performed (DATAVMATCH).

1.3.1309 DWT_MASK_1

DWT Mask Registers

Reset: N/A

Register : Address

DWT_MASK_1: 0xE0001034

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:UUUU			
HW Access	NA				R/W			
Name					MASK			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT Mask Registers 0-3 to apply a mask to data addresses when matching against COMP.

Bits	Name	Description
3:0	MASK[3:0]	Mask on data address when matching against COMP. This is the size of the ignore mask. So, ~0< However, the actual comparison is slightly more complex to enable matching an address wherever it appears on a bus. So, if COMP is 3, this matches a word access of 0, because 3 would be within the word.

1.3.1310 DWT_FUNCTION_1

DWT Function registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_FUNCTION_1: 0xE0001038

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0000			
HW Access	R/W	NA	R/W	NA	R/W			
Name	CYC-MATCH		EMI-TRANGE		FUNCTION			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:0000				R/W:00		R/W:0	R/W:0
HW Access	R/W				R/W		R/W	R/W
Name	DATAVADDR0				DATAVSIZE		LNK1ENA	DATAV-MATCH

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R/W			
Name					DATAVADDR1			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								MATCHED

Use the DWT Function Registers 0-3 to control the operation of the comparator. Each comparator can: Match against either the PC or the data address. This is controlled by CYCMATCH. This function is only available for comparator 0 (DWT_COMP0). Perform data value comparisons if associated address comparators have performed an address match. This function is only available for comparator 1 (DWT_COMP1). Emit data or PC couples, trigger the ETM, or generate a watchpoint depending on the operation defined by FUNCTION.

Bits	Name	Description
24	MATCHED	This bit is set when the comparator matches, and indicates that the operation defined by FUNCTION has occurred since this bit was last read. This bit is cleared on read.
19:16	DATAVADDR1[3:0]	Identity of a second linked address comparator for data value matching when DATAVMATCH == 1 and LNK1ENA == 1.
15:12	DATAVADDR0[3:0]	Identity of a linked address comparator for data value matching when DATAVMATCH == 1.
11:10	DATAVSIZE[1:0]	Defines the size of the data in the COMP register that is to be matched: 00 = byte 01 = halfword 10 = word 11 = Unpredictable.

1.3.1310 DWT_FUNCTION_1 (continued)

9	LNK1ENA	Read-only: 0 = DATAVADDR1 not supported 1 = DATAVADDR1 supported (enabled).
8	DATAVMATCH	This bit is only available in comparator 1. When DATAVMATCH is set, this comparator performs data value compares. The comparators given by DATAVADDR0 and DATAVADDR1provide the address for the data comparison. If DATAVMATCH is set in DWT_FUNCTION1, the FUNCTION setting for the comparators given by DATAVADDR0 and DATAVADDR1 are overridden and those comparators only provide the address match for the data comparison.
7	CYCMATCH	Only available in comparator 0. When set, this comparator compares against the clock cycle counter.
5	EMITRANGE	Emit range field. Reserved to permit emitting offset when range match occurs. Reset clears the EMITRANGE bit. PC sampling is not supported when EMITRANGE is enabled. EMITRANGE only applies for: FUNCTION = b0001, b0010, and b0011.
3:0	FUNCTION[3:0]	Function settings of the DWT Function Registers.

1.3.1311 DWT_COMP_2

DWT Comparator Registers

Reset: N/A

Register : Address

DWT_COMP_2: 0xE0001040

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Use the DWT Comparator Registers 0-3 to write the values that trigger watchpoint events.

Bits	Name	Description
31:0	COMP[31:0]	Data value to compare against PC and the data address as given by DWT_FUNCTIONx. DWT_COMP0 can also compare against the value of the PC Sampler Counter (DWT_CYCCNT). DWT_COMP1 can also compare against data values so that data matching can be performed (DATAVMATCH).

1.3.1312 DWT_MASK_2

DWT Mask Registers

Reset: N/A

Register : Address

DWT_MASK_2: 0xE0001044

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:UUUU			
HW Access	NA				R/W			
Name					MASK			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT Mask Registers 0-3 to apply a mask to data addresses when matching against COMP.

Bits	Name	Description
3:0	MASK[3:0]	Mask on data address when matching against COMP. This is the size of the ignore mask. So, ~0< However, the actual comparison is slightly more complex to enable matching an address wherever it appears on a bus. So, if COMP is 3, this matches a word access of 0, because 3 would be within the word.

1.3.1313 DWT_FUNCTION_2

DWT Function registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_FUNCTION_2: 0xE0001048

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0000			
HW Access	R/W	NA	R/W	NA	R/W			
Name	CYC-MATCH		EMI-TRANGE		FUNCTION			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:0000				R/W:00		R/W:0	R/W:0
HW Access	R/W				R/W		R/W	R/W
Name	DATAVADDR0				DATAVSIZE		LNK1ENA	DATAV-MATCH

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R/W			
Name					DATAVADDR1			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								MATCHED

Use the DWT Function Registers 0-3 to control the operation of the comparator. Each comparator can: Match against either the PC or the data address. This is controlled by CYCMATCH. This function is only available for comparator 0 (DWT_COMP0). Perform data value comparisons if associated address comparators have performed an address match. This function is only available for comparator 1 (DWT_COMP1). Emit data or PC couples, trigger the ETM, or generate a watchpoint depending on the operation defined by FUNCTION.

Bits	Name	Description
24	MATCHED	This bit is set when the comparator matches, and indicates that the operation defined by FUNC-TION has occurred since this bit was last read. This bit is cleared on read.
19:16	DATAVADDR1[3:0]	Identity of a second linked address comparator for data value matching when DATAVMATCH == 1 and LNK1ENA == 1.
15:12	DATAVADDR0[3:0]	Identity of a linked address comparator for data value matching when DATAVMATCH == 1.
11:10	DATAVSIZE[1:0]	Defines the size of the data in the COMP register that is to be matched: 00 = byte 01 = halfword 10 = word 11 = Unpredictable.

1.3.1313 DWT_FUNCTION_2 (continued)

9	LNK1ENA	Read-only: 0 = DATAVADDR1 not supported 1 = DATAVADDR1 supported (enabled).
8	DATAVMATCH	This bit is only available in comparator 1. When DATAVMATCH is set, this comparator performs data value compares. The comparators given by DATAVADDR0 and DATAVADDR1provide the address for the data comparison. If DATAVMATCH is set in DWT_FUNCTION1, the FUNCTION setting for the comparators given by DATAVADDR0 and DATAVADDR1 are overridden and those comparators only provide the address match for the data comparison.
7	CYCMATCH	Only available in comparator 0. When set, this comparator compares against the clock cycle counter.
5	EMITRANGE	Emit range field. Reserved to permit emitting offset when range match occurs. Reset clears the EMITRANGE bit. PC sampling is not supported when EMITRANGE is enabled. EMITRANGE only applies for: FUNCTION = b0001, b0010, and b0011.
3:0	FUNCTION[3:0]	Function settings of the DWT Function Registers.

1.3.1314 DWT_COMP_3

DWT Comparator Registers

Reset: N/A

Register : Address

DWT_COMP_3: 0xE0001050

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Use the DWT Comparator Registers 0-3 to write the values that trigger watchpoint events.

Bits	Name	Description
31:0	COMP[31:0]	Data value to compare against PC and the data address as given by DWT_FUNCTIONx. DWT_COMP0 can also compare against the value of the PC Sampler Counter (DWT_CYCCNT). DWT_COMP1 can also compare against data values so that data matching can be performed (DATAVMATCH).

1.3.1315 DWT_MASK_3

DWT Mask Registers

Reset: N/A

Register : Address

DWT_MASK_3: 0xE0001054

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:UUUU			
HW Access	NA				R/W			
Name					MASK			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the DWT Mask Registers 0-3 to apply a mask to data addresses when matching against COMP.

Bits	Name	Description
3:0	MASK[3:0]	Mask on data address when matching against COMP. This is the size of the ignore mask. So, ~0< However, the actual comparison is slightly more complex to enable matching an address wherever it appears on a bus. So, if COMP is 3, this matches a word access of 0, because 3 would be within the word.

1.3.1316 DWT_FUNCTION_3

DWT Function registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DWT_FUNCTION_3: 0xE0001058

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0000			
HW Access	R/W	NA	R/W	NA	R/W			
Name	CYC-MATCH		EMI-TRANGE		FUNCTION			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:0000				R/W:00		R/W:0	R/W:0
HW Access	R/W				R/W		R/W	R/W
Name	DATAVADDR0				DATAVSIZE		LNK1ENA	DATAV-MATCH

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R/W			
Name					DATAVADDR1			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Name								MATCHED

Use the DWT Function Registers 0-3 to control the operation of the comparator. Each comparator can: Match against either the PC or the data address. This is controlled by CYCMATCH. This function is only available for comparator 0 (DWT_COMP0). Perform data value comparisons if associated address comparators have performed an address match. This function is only available for comparator 1 (DWT_COMP1). Emit data or PC couples, trigger the ETM, or generate a watchpoint depending on the operation defined by FUNCTION.

Bits	Name	Description
24	MATCHED	This bit is set when the comparator matches, and indicates that the operation defined by FUNC-TION has occurred since this bit was last read. This bit is cleared on read.
19:16	DATAVADDR1[3:0]	Identity of a second linked address comparator for data value matching when DATAVMATCH == 1 and LNK1ENA == 1.
15:12	DATAVADDR0[3:0]	Identity of a linked address comparator for data value matching when DATAVMATCH == 1.
11:10	DATAVSIZE[1:0]	Defines the size of the data in the COMP register that is to be matched: 00 = byte 01 = halfword 10 = word 11 = Unpredictable.

1.3.1316 DWT_FUNCTION_3 (continued)

9	LNK1ENA	Read-only: 0 = DATAVADDR1 not supported 1 = DATAVADDR1 supported (enabled).
8	DATAVMATCH	This bit is only available in comparator 1. When DATAVMATCH is set, this comparator performs data value compares. The comparators given by DATAVADDR0 and DATAVADDR1provide the address for the data comparison. If DATAVMATCH is set in DWT_FUNCTION1, the FUNCTION setting for the comparators given by DATAVADDR0 and DATAVADDR1 are overridden and those comparators only provide the address match for the data comparison.
7	CYCMATCH	Only available in comparator 0. When set, this comparator compares against the clock cycle counter.
5	EMITRANGE	Emit range field. Reserved to permit emitting offset when range match occurs. Reset clears the EMITRANGE bit. PC sampling is not supported when EMITRANGE is enabled. EMITRANGE only applies for: FUNCTION = b0001, b0010, and b0011.
3:0	FUNCTION[3:0]	Function settings of the DWT Function Registers.

1.3.1317 FPB_CTRL

Flash Patch Control Register

Reset: Reset Signals Listed Below

Register : Address

FPB_CTRL: 0xE0002000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				NA:00		R/W:U	R/W:0
HW Access	R/W				NA		R/W	R/W
Name	NUM_CODE1						KEY	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:UUU			R/W:UUUU			
HW Access	NA	R/W			R/W			
Name		NUM_CODE2			NUM_LIT			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the Flash Patch Control Register to enable the flash patch block.

Bits	Name	Description
14:12	NUM_CODE2[2:0]	Number of full banks of code comparators, sixteen comparators per bank. Where less than sixteen code comparators are provided, the bank count is zero, and the number present indicated by NUM_CODE. This read only field contains 3'b000 to indicate 0 banks for Cortex-M3 processor.
11:8	NUM_LIT[3:0]	Number of literal slots field. This read only field contains b0010 to indicate that there are two literal slots.
7:4	NUM_CODE1[3:0]	Number of code slots field. This read only field contains b0110 to indicate that there are six code slots.
1	KEY	Key field. To write to the Flash Patch Control Register, you must write a 1 to this write-only bit.
0	ENABLE	Flash patch unit enable bit: 1 = flash patch unit enabled 0 = flash patch unit disabled. Reset clears the ENABLE bit. Note: If the TIEOFF_FPBEN define is uncommented in CM3Defs.v during implementation, it is not possible to set ENABLE.

1.3.1317 FPB_CTRL (continued)

Reset Table

resetsignal	field(s)
N/A	KEY, NUM_CODE1[3:0], NUM_LIT[3:0], NUM_CODE2[2:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1318 FPB_REMAP

Flash Patch Remap Register

Reset: N/A

Register : Address

FPB_REMAP: 0xE0002004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R/W			NA				
Name	REMAP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	REMAP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	REMAP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:000			R/W:UUUUU				
HW Access	NA			R/W				
Name				REMAP				

Use the Flash Patch Remap Register to provide the location in System space where a matched address is remapped. The REMAP address is 8-word aligned, with one word allocated to each of the eight FPB comparators.

Bits	Name	Description
28:5	REMAP[23:0]	Remap base address field.

1.3.1319 FPB_FP_COMP_0

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_0: 0xE0002008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUU						NA:0	R/W:0
HW Access	R/W						NA	R/W
Name	COMP							ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UU		NA:0	R/W:UUUUU				
HW Access	R/W		NA	R/W				
Name	REPLACE			COMP				

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

Bits	Name	Description
31:30	REPLACE[1:0]	This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting.
28:2	COMP[26:0]	Comparison address.
0	ENABLE	Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit.

1.3.1319 FPB_FP_COMP_0 (continued)

Reset Table

resetsignal	field(s)
N/A	COMP[26:0], REPLACE[1:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1320 FPB_FP_COMP_1

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_1: 0xE000200C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUU						NA:0	R/W:0
HW Access	R/W						NA	R/W
Name	COMP							ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UU		NA:0	R/W:UUUUU				
HW Access	R/W		NA	R/W				
Name	REPLACE			COMP				

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

Bits	Name	Description
31:30	REPLACE[1:0]	This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting.
28:2	COMP[26:0]	Comparison address.
0	ENABLE	Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit.

1.3.1320 FPB_FP_COMP_1 (continued)

Reset Table

resetsignal	field(s)
N/A	COMP[26:0], REPLACE[1:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1321 FPB_FP_COMP_2

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_2: 0xE0002010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUU						NA:0	R/W:0
HW Access	R/W						NA	R/W
Name	COMP							ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UU		NA:0	R/W:UUUUU				
HW Access	R/W		NA	R/W				
Name	REPLACE			COMP				

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

Bits	Name	Description
31:30	REPLACE[1:0]	This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting.
28:2	COMP[26:0]	Comparison address.
0	ENABLE	Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit.

1.3.1321 FPB_FP_COMP_2 (continued)

Reset Table

resetsignal	field(s)
N/A	COMP[26:0], REPLACE[1:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1322 FPB_FP_COMP_3

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_3: 0xE0002014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUU						NA:0	R/W:0
HW Access	R/W						NA	R/W
Name	COMP							ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UU		NA:0	R/W:UUUUU				
HW Access	R/W		NA	R/W				
Name	REPLACE			COMP				

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

Bits	Name	Description
31:30	REPLACE[1:0]	This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting.
28:2	COMP[26:0]	Comparison address.
0	ENABLE	Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit.

1.3.1322 FPB_FP_COMP_3 (continued)

Reset Table

resetsignal	field(s)
N/A	COMP[26:0], REPLACE[1:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1323 FPB_FP_COMP_4

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_4: 0xE0002018

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUU						NA:0	R/W:0
HW Access	R/W						NA	R/W
Name	COMP							ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UU		NA:0	R/W:UUUUU				
HW Access	R/W		NA	R/W				
Name	REPLACE			COMP				

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

Bits	Name	Description
31:30	REPLACE[1:0]	This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting.
28:2	COMP[26:0]	Comparison address.
0	ENABLE	Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit.

1.3.1323 FPB_FP_COMP_4 (continued)

Reset Table

resetsignal	field(s)
N/A	COMP[26:0], REPLACE[1:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1324 FPB_FP_COMP_5

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_5: 0xE000201C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUU						NA:0	R/W:0
HW Access	R/W						NA	R/W
Name	COMP							ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UU		NA:0	R/W:UUUUU				
HW Access	R/W		NA	R/W				
Name	REPLACE			COMP				

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

Bits	Name	Description
31:30	REPLACE[1:0]	This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting.
28:2	COMP[26:0]	Comparison address.
0	ENABLE	Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit.

1.3.1324 FPB_FP_COMP_5 (continued)

Reset Table

resetsignal	field(s)
N/A	COMP[26:0], REPLACE[1:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1325 FPB_FP_COMP_6

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_6: 0xE0002020

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUU						NA:0	R/W:0
HW Access	R/W						NA	R/W
Name	COMP							ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UU		NA:0	R/W:UUUUU				
HW Access	R/W		NA	R/W				
Name	REPLACE			COMP				

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

Bits	Name	Description
31:30	REPLACE[1:0]	This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting.
28:2	COMP[26:0]	Comparison address.
0	ENABLE	Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit.

1.3.1325 FPB_FP_COMP_6 (continued)

Reset Table

resetsignal	field(s)
N/A	COMP[26:0], REPLACE[1:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1326 FPB_FP_COMP_7

Flash Patch Comparator Registers

Reset: Reset Signals Listed Below

Register : Address

FPB_FP_COMP_7: 0xE0002024

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUU						NA:0	R/W:0
HW Access	R/W						NA	R/W
Name	COMP							ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UU		NA:0	R/W:UUUUU				
HW Access	R/W		NA	R/W				
Name	REPLACE			COMP				

Use the Flash Patch Comparator Registers to store the values to compare with the PC address.

Bits	Name	Description
31:30	REPLACE[1:0]	This selects what happens when the COMP address is matched. It is interpreted as: b00 = remap to remap address. See FP_REMAP b01 = set BKPT on lower halfword, upper is unaffected b10 = set BKPT on upper halfword, lower is unaffected b11 = set BKPT on both lower and upper halfwords. Settings other than b00 are only valid for instruction comparators. Literal comparators ignore non-b00 settings. Address remapping only takes place for the b00 setting.
28:2	COMP[26:0]	Comparison address.
0	ENABLE	Compare and remap enable for Flash Patch Comparator Register n: 1 = Flash Patch Comparator Register n compare and remap enabled 0 = Flash Patch Comparator Register n compare and remap disabled. The ENABLE bit of FP_CTRL must also be set to enable comparisons. Reset clears the ENABLE bit.

1.3.1326 FPB_FP_COMP_7 (continued)

Reset Table

resetsignal	field(s)
N/A	COMP[26:0], REPLACE[1:0]
System reset for retention flops [reset_all_retention]	ENABLE

1.3.1327 FPB_PID4

FPB Peripheral Identification Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID4: 0xE0002FD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000100							
HW Access	R/W							
Name	PID4							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID4[7:0]	Peripheral Identification Register 4

1.3.1328 FPB_PID5

FPB Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID5: 0xE0002FD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID5							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID5[7:0]	Peripheral Identification Register 5

1.3.1329 FPB_PID6

FPB Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID6: 0xE0002FD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID6							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID6[7:0]	Peripheral Identification Register 6

1.3.1330 FPB_PID7

FPB Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID7: 0xE0002FDC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID7							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID7[7:0]	Peripheral Identification Register 7

1.3.1331 FPB_PID0

FPB Peripheral Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID0: 0xE0002FE0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000001							
HW Access	R/W							
Name	PID0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID0[7:0]	Peripheral Identification Register 0

1.3.1332 FPB_PID1

FPB Peripheral Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID1: 0xE0002FE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10110000							
HW Access	R/W							
Name	PID1							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID1[7:0]	Peripheral Identification Register 1

1.3.1333 FPB_PID2

FPB Peripheral Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID2: 0xE0002FE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00011011							
HW Access	R/W							
Name	PID2							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID2[7:0]	Peripheral Identification Register 2

1.3.1334 FPB_PID3

FPB Peripheral Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_PID3: 0xE0002FEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID3							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID3[7:0]	Peripheral Identification Register 3

1.3.1335 FPB_CID0

FPB Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_CID0: 0xE0002FF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00001101							
HW Access	R/W							
Name	CID0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID0[7:0]	Component Identification Register 0

1.3.1336 FPB_CID1

FPB Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_CID1: 0xE0002FF4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:11100000							
HW Access	R/W							
Name	CID1							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID1[7:0]	Component Identification Register 1

1.3.1337 FPB_CID2

FPB Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_CID2: 0xE0002FF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000101							
HW Access	R/W							
Name	CID2							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID2[7:0]	Component Identification Register 2

1.3.1338 FPB_CID3

FPB Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FPB_CID3: 0xE0002FFC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10110001							
HW Access	R/W							
Name	CID3							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID3[7:0]	Component Identification Register 3

1.3.1339 NVIC_INT_CTL_TYPE

Interrupt Controller Type Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_INT_CTL_TYPE: 0xE000E004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:00000				
HW Access	NA			W				
Name				INTLINESNUM				

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Read the Interrupt Controller Type Register to see the number of interrupt lines that the NVIC supports.

Bits	Name	Description
4:0	INTLINESNUM[4:0]	Total number of interrupt lines in groups of 32: b00000 = 0...32 b00001 = 33...64 b00010 = 65...96 b00011 = 97...128 b00100 = 129...160 b00101 = 161...192 b00110 = 193...224 b00111 = 225...256

1.3.1340 NVIC_SYSTICK_CTL

SYSTICK Control and Status register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYSTICK_CTL: 0xE000E010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						CLKSRC	TICKINT	ENB

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							RC:0
HW Access	NA							R/W
Name								CNTFLAG

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

SYSTICK Ten milliSecond software timer control and status register.

Bits	Name	Description
16	CNTFLAG	CNTFLAG is set when the CURRENT value of the SYSTICK timer is zero. It is automatically cleared when read. Note that CNTFLAG is cleared when the debugger reads it only if the MasterType bit in the AHB-AP Control Register is set to 0. Otherwise the CNTGLAG is not changed by a debugger read.
2	CLKSRC	0=External Clock Source 1=CPU Clock Note that the External Clock Source must be at least 2.5 times slower than the CPU Clock or operation will be unpredictable. If no external clock source is provided, the input is held at 1 and the SYSTICK timer will count as the same as if the CPU Clock was used.
1	TICKINT	0=Disable the Systick Interrupt handler 1=Enable the Systick Interrupt Handler. When the CNTFLAG is set an interrupt will be generated if the TICKINT bit is enabled (1).
0	ENB	0=Disable the timer 1=Enable the SYSTICK Timer When the SYSTICK timer is enabled, the counter runs until it reaches 0. When it reaches 0, it will set the COUNTFLAG and load the RELOAD value into the counter and continue counting.

1.3.1341 NVIC_SYSTICK_RELOAD

SYSTICK Reload value

Reset: N/A

Register : Address

NVIC_SYSTICK_RELOAD: 0xE000E014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	RELOAD							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	RELOAD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Name	RELOAD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

RELOAD is copied into the CURRENT register when it counts down to 0. RELOAD is the number of clocks between each setting of the CNTFLAG in the SYSTICK_CTL register. Note that a value of 0 will not cause an interrupt or CNTFLAG to be set.

Bits	Name	Description
23:0	RELOAD[23:0]	Value loaded into the SYSTICK CURRENT value register when it counts down 0.

1.3.1342 NVIC_SYSTICK_CURRENT

SYSTICK Counter

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYSTICK_CURRENT: 0xE000E018

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	CURRENT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	CURRENT							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	CURRENT							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Current value of the SYSTICK Counter. Note that writing any value to this register will clear it to zero. Clearing to zero will set CNTFLAG and reload the counter with the RELOAD value.

Bits	Name	Description
23:0	CURRENT[23:0]	Current value of the SYSTICK Counter.

1.3.1343 NVIC_SYSTICK_CAL

SYSTICK Calibration register

Reset: N/A

Register : Address

NVIC_SYSTICK_CAL: 0xE000E01C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	TENMS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	TENMS							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	TENMS							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:U	R:U	NA:000000					
HW Access	R/W	R/W	NA					
Name	NOREF	SKEW						

Used to adjust the SYSTICK timer to be exactly 10ms. See Chapter 14 of The Definitive Guide to the ARM Cortex-M3.

Bits	Name	Description
31	NOREF	NOREF is set to 1 when there is no reference clock.
30	SKEW	When SKEW is set to 1, the calibration value is not exactly 10 milliseconds due to the clock frequency. The accuracy of the timer may not be suitable for Real-Time applications.
23:0	TENMS[23:0]	Calibration value for the Ten Millisecond timer.

1.3.1344 NVIC_SETENA0

Interrupt Enable Set 0-31

Reset: N/A

Register : Address

NVIC_SETENA0: 0xE000E100

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SETENA0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SETENA0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SETENA0							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SETENA0							

Set Enable external interrupts 0-31. Writing a 1 to any bit in this register sets the interrupt enable for the respective interrupt. Writing a 0 does nothing. To clear the bit, write a 1 to the Interrupt Clear enable register. Reading this register will read the current status of the interrupt enable. Setting and clearing the interrupt enables is done in 2 different registers to make is easier to set/clear individual bits. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
31:0	SETENA0[31:0]	Writing a 1 enables the respective interrupt. IE: bit 0 will enable IRQ0, Bit 1 will enable IRQ1 ... Bit 31 will enable IRQ31. Writing 0 has no effect.

1.3.1345 NVIC_CLRENA0

Interrupt Enable Clear 0-31

Reset: N/A

Register : Address

NVIC_CLRENA0: 0xE000E180

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CLRENA0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CLRENA0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CLRENA0							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CLRENA0							

Clear Enable external interrupts 0-31. Writing a 1 to any bit in this register clears the interrupt enable for the respective interrupt. Writing a 0 does nothing. Reading this register will read the current status of the interrupt enable. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
31:0	CLRENA0[31:0]	Writing a 1 disables the respective interrupt. IE: bit 0 will disable IRQ0, Bit 1 will disable IRQ1 ... Bit 31 will disable IRQ31. Writing 0 has no effect.

1.3.1346 NVIC_SETPEND0

Interrupt Pending Set 0-31

Reset: N/A

Register : Address

NVIC_SETPEND0: 0xE000E200

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SETPEND0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SETPEND0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SETPEND0							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	SETPEND0							

Set Pending external interrupts 0-31. Writing a 1 to any bit in this register sets the interrupt pending bit for the respective interrupt. Writing a 0 does nothing. Reading this register will read the current status of the interrupt pending bits. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
31:0	SETPEND0[31:0]	Writing a 1 sets the respective interrupt pending bit. IE: bit 0 will set IRQ0, Bit 1 will set IRQ1 ... Bit 31 will set IRQ31. Writing 0 has no effect.

1.3.1347 NVIC_CLRPEND0

Interrupt Pending Clear 0-31

Reset: N/A

Register : Address

NVIC_CLRPEND0: 0xE000E280

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CLRPEND0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CLRPEND0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CLRPEND0							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	CLRPEND0							

Clear Pending external interrupts 0-31. Writing a 1 to any bit in this register clears the interrupt pending bit for the respective interrupt. Writing a 0 does nothing. Reading this register will read the current status of the interrupt pending bits. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
31:0	CLRPEND0[31:0]	Writing a 1 clears the respective interrupt pending bit. IE: bit 0 will clear IRQ0, Bit 1 will clear IRQ1 ... Bit 31 will clear IRQ31. Writing 0 has no effect.

1.3.1348 NVIC_ACTIVE0

Active Interrupts 0-31

Reset: N/A

Register : Address

NVIC_ACTIVE0: 0xE000E300

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	ACTIVE0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	ACTIVE0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	ACTIVE0							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Name	ACTIVE0							

Each bit of this register corresponds to an interrupt 0-31. If the bit is a 1, then that interrupt it active. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
31:0	ACTIVE0[31:0]	Active interrupt register.

1.3.1349 NVIC_PRI_0

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_0: 0xE000E400

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1350 NVIC_PRI_1

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_1: 0xE000E401

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1351 NVIC_PRI_2

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_2: 0xE000E402

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1352 NVIC_PRI_3

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_3: 0xE000E403

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1353 NVIC_PRI_4

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_4: 0xE000E404

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1354 NVIC_PRI_5

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_5: 0xE000E405

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1355 NVIC_PRI_6

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_6: 0xE000E406

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1356 NVIC_PRI_7

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_7: 0xE000E407

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1357 NVIC_PRI_8

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_8: 0xE000E408

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1358 NVIC_PRI_9

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_9: 0xE000E409

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1359 NVIC_PRI_10

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_10: 0xE000E40A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1360 NVIC_PRI_11

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_11: 0xE000E40B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1361 NVIC_PRI_12

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_12: 0xE000E40C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1362 NVIC_PRI_13

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_13: 0xE000E40D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1363 NVIC_PRI_14

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_14: 0xE000E40E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1364 NVIC_PRI_15

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_15: 0xE000E40F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1365 NVIC_PRI_16

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_16: 0xE000E410

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1366 NVIC_PRI_17

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_17: 0xE000E411

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1367 NVIC_PRI_18

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_18: 0xE000E412

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1368 NVIC_PRI_19

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_19: 0xE000E413

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1369 NVIC_PRI_20

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_20: 0xE000E414

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1370 NVIC_PRI_21

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_21: 0xE000E415

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1371 NVIC_PRI_22

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_22: 0xE000E416

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1372 NVIC_PRI_23

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_23: 0xE000E417

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1373 NVIC_PRI_24

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_24: 0xE000E418

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1374 NVIC_PRI_25

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_25: 0xE000E419

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1375 NVIC_PRI_26

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_26: 0xE000E41A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1376 NVIC_PRI_27

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_27: 0xE000E41B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1377 NVIC_PRI_28

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_28: 0xE000E41C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1378 NVIC_PRI_29

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_29: 0xE000E41D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1379 NVIC_PRI_30

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_30: 0xE000E41E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1380 NVIC_PRI_31

Interrupt Priority 0-31

Reset: N/A

Register : Address

NVIC_PRI_31: 0xE000E41F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUU			NA:00000				
HW Access	R			NA				
Name	PRIORITY							

Interrupt priority for interrupts 0-31. See Chapter 8 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
7:5	PRIORITY[2:0]	There are 8 interrupt priorities. Each interrupt is assigned a single byte address for the priority register. The priority registers are stored with the Most Significant Bit (MSB) first. The priority value is stored in bits [7:5] of the byte.0 is the lowest priority and 7 is the highest.

1.3.1381 NVIC_CPUID_BASE

CPU ID Base Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_CPUID_BASE: 0xE000ED00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0011				R:0001			
HW Access	R/W				R/W			
Name	PARTNO				REVISION			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:11000010							
HW Access	R/W							
Name	PARTNO							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:0001				R:1111			
HW Access	R/W				R/W			
Name	VARIANT				Constant			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00100001							
HW Access	R/W							
Name	IMPLEMENTER							

Read the CPU ID Base Register to determine: o the ID number of the processor core o the version number of the processor core o the implementation details of the processor core.

Bits	Name	Description
31:24	IMPLEMENTER[7:0]	Implementer code. ARM is 0x41
23:20	VARIANT[3:0]	Implementation defined variant number.
19:16	Constant[3:0]	Reads as 0xF
15:4	PARTNO[11:0]	Number of processor within family: [11:10] b11 = Cortex family [9:8] b00 = version [7:6] b00 = reserved [5:4] b10 = M (v7-M) [3:0] X = family member. Cortex-M3 family is b0011.
3:0	REVISION[3:0]	Implementation defined revision number.

1.3.1382 NVIC_INTR_CTRL_STATE

Interrupt Control State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_INTR_CTRL_STATE: 0xE000ED04

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	VECTACTIVE							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0	NA:00		R:0
HW Access	R/W				R/W	NA		R/W
Name	VECTPENDING				RETTO-BASE			VECTAC-TIVE

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:0	R:0	R:000000					
HW Access	R/W	R/W	R/W					
Name	ISRPRE-EMPT	ISRPEND-ING	VECTPENDING					

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:000			R/W:0	W:0	R/W:0	W:0	NA:0
HW Access	NA			R/W	R/W	R/W	R/W	NA
Name				PENDS-VSET	PENDSV-CLR	PENDST-SET	PENDST-CLR	

Use the Interrupt Control State Register to: o set a pending Non-Maskable Interrupt (NMI) o set or clear a pending SVC o set or clear a pending SysTick o check for pending exceptions o check the vector number of the highest priority pended exception o check the vector number of the active exception.

Bits	Name	Description
28	PENDSVSET	Set pending pendSV bit: 1 = set pending pendSV 0 = do not set pending pendSV.
27	PENDSVCLR	Clear pending pendSV bit: 1 = clear pending pendSV 0 = do not clear pending pendSV.
26	PENDSTSET	Set a pending SysTick bit 1 = set pending SysTick 0 = do not set pending SysTick.

1.3.1382 NVIC_INTR_CTRL_STATE (continued)

25	PENDSTCLR	Clear pending SysTick bit: 1 = clear pending SysTick 0 = do not clear pending SysTick.
23	ISRPREEMPT	You must only use this at debug time. It indicates that a pending interrupt becomes active in the next running cycle. If C_MASKINTS is clear in the Debug Halting Control and Status Register, the interrupt is serviced.
22	ISRPENDING	Interrupt pending flag. Excludes NMI and Faults: 1 = interrupt pending 0 = interrupt not pending.
21:12	VECTPENDING[9:0]	Pending ISR number field. VECTPENDING contains the interrupt number of the highest priority pending ISR.
11	RETTOBASE	This bit is 1 when the set of all active exceptions minus the IPSR_current_exception yields the empty set.
8:0	VECTACTIVE[8:0]	Active ISR number field. VECTACTIVE contains the interrupt number of the currently running ISR, including NMI and Hard Fault. A shared handler can use VECTACTIVE to determine which interrupt invoked it. You can subtract 16 from the VECTACTIVE field to index into the Interrupt Clear/Set Enable, Interrupt Clear Pending/SetPending and Interrupt Priority Registers. IN-TISR[0] has vector number 16. Reset clears the VECTACTIVE field.

1.3.1383 NVIC_VECT_OFFSET

Interrupt Vector Table Offset

Reset: N/A

Register : Address

NVIC_VECT_OFFSET: 0xE000ED08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	NA:0000000						
HW Access	R/W	NA						
Name	TBLOFF							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	TBLOFF							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	TBLOFF							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00		R/W:U	R/W:UUUUU				
HW Access	NA		R/W	R/W				
Name			TBLBASE	TBLOFF				

Relocates the Interrupt Vector table (IVT) to SRAM. The default Interrupt Vector Table is at 0x0000_0000 (see description in FLASH). This register allows the Vector Table to be relocated so that the interrupt vectors can be changed by the application. Typically the Interrupt Vector Table is relocated to SRAM in Code Space (below 0x2000_0000) for maximum interrupt performance. Note that the IVT can be placed above 0x2000_0000 but you lose the parallelism of stacking registers and fetching the interrupt vector at the same time if the IVT is located above 0x2000_0000. Typically the IVT should be located at the bottom of SRAM in CODE space - 0x1ffn_0000 where n will depend on the amount of SRAM available. See Chapter 7 of The Definitive Guide to the ARM Cortex-M3 for more details.

Bits	Name	Description
29	TBLBASE	Bit 29 of the vector table offset: 0=Table Base in Code. 1=Table Base in RAM. Maximum interrupt performance is achieved when this bit is 0.
28:7	TBLOFF[21:0]	Offset of the Interrupt Vector Table. Note that this must be on a power-of-2 boundary large enough for the number of interrupt vectors (typically a 1K byte boundary).

1.3.1384 NVIC_APPLN_INTR

Application Interrupt and Reset Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_APPLN_INTR: 0xE000ED0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R/W	R/W	R/W
Name						SYSRESE-TREQ	VECTCL-RACTIVE	VECTRE-SET

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:0	NA:0000				R/W:000		
HW Access	R/W	NA				R/W		
Name	ENDIAN-ESS					PRIGROUP		

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	VECTKEY							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	VECTKEY							

Use the Application Interrupt and Reset Control Register to: o determine data endianness o clear all active state information for debug or to recover from a hard failure o execute a system reset o alter the priority grouping position (binary point).

Bits	Name	Description
31:16	VECTKEY[15:0]	Register key. Writing to this register requires 0x5FA in the VECTKEY field. Otherwise the write value is ignored.
15	ENDIANESS	Data endianness bit: 1 = big endian 0 = little endian. ENDIANESS is sampled from the BIGEND input port during reset. You cannot change ENDIANESS outside of reset.

1.3.1384 NVIC_APPLN_INTR (continued)

10:8	PRIGROUP[2:0]	Interrupt priority grouping field: PRIGROUP Split of pre-emption priority from subpriority 0 7.1 indicates seven bits of pre-emption priority, one bit of subpriority 1 6.2 indicates six bits of pre-emption priority, two bits of subpriority 2 5.3 indicates five bits of pre-emption priority, three bits of subpriority 3 4.4 indicates four bits of pre-emption priority, four bits of subpriority 4 3.5 indicates three bits of pre-emption priority, five bits of subpriority 5 2.6 indicates two bits of pre-emption priority, six bits of subpriority 6 1.7 indicates one bit of pre-emption priority, seven bits of subpriority 7 0.8 indicates no pre-emption priority, eight bits of subpriority. PRIGROUP field is a binary point position indicator for creating subpriorities for exceptions that share the same pre-emption level. It divides the PRI_n field in the Interrupt Priority Register into a pre-emption level and a subpriority level. The binary point is a left-of value. This means that the PRIGROUP value represents a point starting at the left of the Least Significant Bit (LSB). This is bit [0] of 7:0. The lowest value might not be 0 depending on the number of bits allocated for priorities, and implementation choices.
2	SYSRESETREQ	Causes a signal to be asserted to the outer system that indicates a reset is requested. Intended to force a large system reset of all major components except for debug. Setting this bit does not prevent Halting Debug from running.
1	VECTCLRACTIVE	Clear active vector bit: 1 = clear all state information for active NMI, fault, and interrupts 0 = do not clear. It is the responsibility of the application to reinitialize the stack. The VECTCLRACTIVE bit is for returning to a known state during debug. The VECTCLRACTIVE bit self-clears. IPSR is not cleared by this operation. So, if used by an application, it must only be used at the base level of activation, or within a system handler whose active bit can be set.
0	VECTRESET	System Reset bit. Resets the system, with the exception of debug components: 1 = reset system 0 = do not reset system. The VECTRESET bit self-clears. Reset clears the VECTRESET bit. For debugging, only write this bit when the core is halted.

1.3.1385 NVIC_SYSTEM_CONTROL

System Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYSTEM_CONTROL: 0xE000ED10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:0	R/W:0	R/W:0	NA:0
HW Access	NA			R/W	NA	R/W	R/W	NA
Name				SEVON-PEND		SLEEP-DEEP	SLEEPON-EXIT	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the System Control Register for power-management functions: o signal to the system when the processor can enter a low power state o control how the processor enters and exits low power states.

Bits	Name	Description
4	SEVONPEND	When enabled, this causes WFE to wake up when an interrupt moves from inactive to pended. Otherwise, WFE only wakes up from an event signal, external and SEV instruction generated. The event input, RXEV, is registered even when not waiting for an event, and so effects the next WFE.
2	SLEEPDEEP	Sleep deep bit: 1 = indicates to the system that Cortex-M3 clock can be stopped. Setting this bit causes the SLEEPDEEP port to be asserted when the processor can be stopped. 0 = not OK to turn off system clock.
1	SLEEPONEXIT	Sleep on exit when returning from Handler mode to Thread mode: 1 = sleep on ISR exit. 0 = do not sleep when returning to Thread mode. Enables interrupt driven applications to avoid returning to empty main application.

1.3.1386 NVIC_CFG_CONTROL

Configuration Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_CFG_CONTROL: 0xE000ED14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	NA:0	R/W:0	R/W:0
HW Access	NA			R/W	R/W	NA	R/W	R/W
Name				DIV_0_TRP	UNALIGN_ TRP		USERSET-MPEND	NONE-BASETHRD ENA

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R/W	R/W
Name							STKALIGN	BFHFN-MIGN

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the Configuration Control Register to: o enable NMI, Hard Fault and FAULTMASK to ignore bus fault o trap divide by zero, and unaligned accesses o enable user access to the Software Trigger Exception Register o control entry to Thread Mode.

Bits	Name	Description
9	STKALIGN	1 = on exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. 0 = only 4-byte alignment is guaranteed for the SP used prior to the exception on exception entry.
8	BFHFNMIGN	When enabled, this causes handlers running at priority -1 and -2 (Hard Fault, NMI, and FAULTMASK escalated handlers) to ignore Data Bus faults caused by load and store instructions. When disabled, these bus faults cause a lock-up. You must only use this enable with extreme caution. All data bus faults are ignored - you must only use it when the handler and its data are in absolutely safe memory. Its normal use is to probe system devices and bridges to detect control path problems and fix them.
4	DIV_0_TRP	Trap on Divide by 0. This enables faulting/halting when an attempt is made to divide by 0.

1.3.1386 NVIC_CFG_CONTROL (continued)

3	UNALIGN_TRP	Trap for unaligned access. This enables faulting/halting on any unaligned half or full word access. Unaligned load-store multiples always fault.
1	USERSETMPEND	If written as 1, enables user code to write the Software Trigger Interrupt register to trigger (pend) a Main exception, which is one associated with the Main stack pointer.
0	NONEBASETHRDENA	When 0, default, It is only possible to enter Thread mode when returning from the last exception. When set to 1, Thread mode can be entered from any level in Handler mode by controlled return value.

1.3.1387 NVIC_SYS_PRIO_HANDLER_4_7

System Handler Priority Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYS_PRIO_HANDLER_4_7: 0xE000ED18

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N1							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N2							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N3							

Use the three System Handler Priority Registers to prioritize the following system handlers: o memory manage o bus fault o usage fault o debug monitor o SVC o SysTick o PendSV. System handlers are a special class of exception handler that can have their priority set to any of the priority levels. Most can be masked on (enabled) or off (disabled). When disabled, the fault is always treated as a Hard Fault.

Bits	Name	Description
31:24	PRI_N3[7:0]	Priority of system handler 7, 11, and 15. Reserved, SVCall, and SysTick.
23:16	PRI_N2[7:0]	Priority of system handler 6, 10, and 14. Usage Fault, reserved, and PendSV.
15:8	PRI_N1[7:0]	Priority of system handler 5, 9, and 13, Bus Fault, reserved, and reserved.
7:0	PRI_N[7:0]	Priority of system handler 4, 8, and 12. Mem Manage, reserved, and Debug Monitor.

1.3.1388 NVIC_SYS_PRIO_HANDLER_8_11

System Handler Priority Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYS_PRIO_HANDLER_8_11: 0xE000ED1C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N1							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N2							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N3							

Use the three System Handler Priority Registers to prioritize the following system handlers: o memory manage o bus fault o usage fault o debug monitor o SVC o SysTick o PendSV. System handlers are a special class of exception handler that can have their priority set to any of the priority levels. Most can be masked on (enabled) or off (disabled). When disabled, the fault is always treated as a Hard Fault.

Bits	Name	Description
31:24	PRI_N3[7:0]	Priority of system handler 7, 11, and 15. Reserved, SVCall, and SysTick.
23:16	PRI_N2[7:0]	Priority of system handler 6, 10, and 14. Usage Fault, reserved, and PendSV.
15:8	PRI_N1[7:0]	Priority of system handler 5, 9, and 13, Bus Fault, reserved, and reserved.
7:0	PRI_N[7:0]	Priority of system handler 4, 8, and 12. Mem Manage, reserved, and Debug Monitor.

1.3.1389 NVIC_SYS_PRIO_HANDLER_12_15

System Handler Priority Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYS_PRIO_HANDLER_12_15: 0xE000ED20

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N1							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N2							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	PRI_N3							

Use the three System Handler Priority Registers to prioritize the following system handlers: o memory manage o bus fault o usage fault o debug monitor o SVC o SysTick o PendSV. System handlers are a special class of exception handler that can have their priority set to any of the priority levels. Most can be masked on (enabled) or off (disabled). When disabled, the fault is always treated as a Hard Fault.

Bits	Name	Description
31:24	PRI_N3[7:0]	Priority of system handler 7, 11, and 15. Reserved, SVCall, and SysTick.
23:16	PRI_N2[7:0]	Priority of system handler 6, 10, and 14. Usage Fault, reserved, and PendSV.
15:8	PRI_N1[7:0]	Priority of system handler 5, 9, and 13, Bus Fault, reserved, and reserved.
7:0	PRI_N[7:0]	Priority of system handler 4, 8, and 12. Mem Manage, reserved, and Debug Monitor.

1.3.1390 NVIC_SYS_HANDLER_CSR

System Handler Control and State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_SYS_HANDLER_CSR: 0xE000ED24

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:000			R/W:0	NA:0	R/W:0	R/W:0
HW Access	R/W	NA			R/W	NA	R/W	R/W
Name	SVCAL-LACT				USGFAULT-ACT		BUSFAULT-ACT	MEMFAUL-TACT

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	NA	R/W
Name	SVCALL-PENDED	BUSFAULT-PENDED	MEM-FAULT-PENDED	USGFAULT-PENDED	SYSTICK-ACT	PENDS-VACT		MONITO-RACT

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R/W	R/W	R/W
Name						USGFAULT-ENA	BUSFAULT-ENA	MEM-FAULTENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the System Handler Control and State Register to: o enable or disable the system handlers o determine the pending status of bus fault, mem manage fault, and SVC o determine the active status of the system handlers. o If a fault condition occurs while its fault handler is disabled, the fault escalates to a Hard Fault.

Bits	Name	Description
18	USGFAULTENA	Set to 0 to disable, else 1 for enabled.
17	BUSFAULTENA	Set to 0 to disable, else 1 for enabled.
16	MEMFAULTENA	Set to 0 to disable, else 1 for enabled.
15	SVCALLPENDED	Reads as 1 if SVCall is pended.
14	BUSFAULTPENDED	Reads as 1 if BusFault is pended.
13	MEMFAULTPENDED	Reads as 1 if MemManage is pended.
12	USGFAULTPENDED	Read as 1 if usage fault is pended.

1.3.1390 NVIC_SYS_HANDLER_CSR (continued)

11	SYSTICKACT	Reads as 1 if SysTick is active.
10	PENDSVACT	Reads as 1 if PendSV is active.
8	MONITORACT	Reads as 1 if the Monitor is active.
7	SVCALLACT	Reads as 1 if SVCall is active.
3	USGFAULTACT	Reads as 1 if UsageFault is active.
1	BUSFAULTACT	Reads as 1 if BusFault is active.
0	MEMFAULTACT	Reads as 1 if MemManage is active.

1.3.1391 NVIC_MEMMAN_FAULT_STATUS

Memory Manage Fault Status Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_MEMMAN_FAULT_STATUS: 0xE000ED28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	R/W:0	NA:0	R/W:0	R/W:0
HW Access	R/W	NA		R/W	R/W	NA	R/W	R/W
Name	MMARVAL-ID			MSTKERR	MUNSTK-ERR		DACCVIOL	IACCVIOL

The flags in the Memory Manage Fault Status Register indicate the cause of memory access faults.

Bits	Name	Description
7	MMARVALID	Memory Manage Address Register (MMAR) address valid flag: 1 = valid fault address in MMAR. A later-arriving fault, such as a bus fault, can clear a memory manage fault. 0 = no valid fault address in MMAR. If a MemManage fault occurs that is escalated to a Hard Fault because of priority, the Hard Fault handler must clear this bit. This prevents problems on return to a stacked active MemManage handler whose MMAR value has been overwritten.
4	MSTKERR	Stacking from exception has caused one or more access violations. The SP is still adjusted and the values in the context area on the stack might be incorrect. The MMAR is not written.
3	MUNSTKERR	Unstack from exception return has caused one or more access violations. This is chained to the handler, so that the original return stack is still present. SP is not adjusted from failing return and new save is not performed. The MMAR is not written.
1	DACCVIOL	Data access violation flag. Attempting to load or store at a location that does not permit the operation sets the DACCVIOL flag. The return PC points to the faulting instruction. This error loads MMAR with the address of the attempted access.
0	IACCVIOL	Instruction access violation flag. Attempting to fetch an instruction from a location that does not permit execution sets the IACCVIOL flag. This occurs on any access to an XN region, even when the MPU is disabled or not present. The return PC points to the faulting instruction. The MMAR is not written.

1.3.1392 NVIC_BUS_FAULT_STATUS

Bus Fault Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_BUS_FAULT_STATUS: 0xE000ED29

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R/W	NA		R/W	R/W	R/W	R/W	R/W
Name	BFARVALID			STKERR	UNSTKERR	IMPRECIS-ERR	PRECIS-ERR	IBUSERR

The flags in the Bus Fault Status Register indicate the cause of bus access faults.

Bits	Name	Description
7	BFARVALID	This bit is set if the Bus Fault Address Register (BFAR) contains a valid address. This is true after a bus fault where the address is known. Other faults can clear this bit, such as a MemManage fault occurring later. If a Bus fault occurs that is escalated to a Hard Fault because of priority, the Hard Fault handler must clear this bit. This prevents problems if returning to a stacked active Bus fault handler whose BFAR value has been overwritten.
4	STKERR	Stacking from exception has caused one or more bus faults. The SP is still adjusted and the values in the context area on the stack might be incorrect. The BFAR is not written.
3	UNSTKERR	Unstack from exception return has caused one or more bus faults. This is chained to the handler, so that the original return stack is still present. SP is not adjusted from failing return and new save is not performed. The BFAR is not written.
2	IMPRECISERR	Imprecise data bus error. It is a BusFault, but the Return PC is not related to the causing instruction. This is not a synchronous fault. So, if detected when the priority of the current activation is higher than the Bus Fault, it only pends. Bus fault activates when returning to a lower priority activation. If a precise fault occurs before returning to a lower priority exception, the handler detects both IMPRECISERR set and one of the precise fault status bits set at the same time. The BFAR is not written.
1	PRECISERR	Precise data bus error return.
0	IBUSERR	Instruction bus error flag: 1 = instruction bus error 0 = no instruction bus error. The IBUSERR flag is set by a prefetch error. The fault stops on the instruction, so if the error occurs under a branch shadow, no fault occurs. The BFAR is not written.

1.3.1393 NVIC_USAGE_FAULT_STATUS

Usage Fault Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_USAGE_FAULT_STATUS: 0xE000ED2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R/W	R/W	R/W	R/W
Name					NOCP	INVPC	INVSTATE	UNDEFIN-STR

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R/W	R/W
Name							DIVBYZE-RO	UN-ALIGNED

The flags in the Usage Fault Status Register indicate the following errors: o illegal combination of EPSR and instruction o illegal PC load o illegal processor state o instruction decode error o attempt to use a coprocessor instruction o illegal unaligned access.

Bits	Name	Description
9	DIVBYZERO	When DIV_0_TRP (see Configuration Control Register) is enabled and an SDIV or UDIV instruction is used with a divisor of 0, this fault occurs The instruction is executed and the return PC points to it. If DIV_0_TRP is not set, then the divide returns a quotient of 0.
8	UNALIGNED	When UNALIGN_TRP is enabled (see Configuration Control Register), and there is an attempt to make an unaligned memory access, then this fault occurs. Unaligned LDM/STM/LDRD/STRD instructions always fault irrespective of the setting of UNALIGN_TRP.
3	NOCP	Attempt to use a coprocessor instruction. The processor does not support coprocessor instructions.
2	INVPC	Attempt to load EXC_RETURN into PC illegally. Invalid instruction, invalid context, invalid value. The return PC points to the instruction that tried to set the PC.
1	INVSTATE	Invalid combination of EPSR and instruction, for reasons other than UNDEFINED instruction. Return PC points to faulting instruction, with the invalid state.
0	UNDEFINSTR	The UNDEFINSTR flag is set when the processor attempts to execute an undefined instruction. This is an instruction that the processor cannot decode. The return PC points to the undefined instruction.

1.3.1394 NVIC_HARD_FAULT_STATUS

Hard Fault Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_HARD_FAULT_STATUS: 0xE000ED2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	NA:0
HW Access	NA						R/W	NA
Name							VECTTB	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:0	R/W:0	NA:000000					
HW Access	R/W	R/W	NA					
Name	DEBUGEVT	FORCED						

Use the Hard Fault Status Register (HFSR) to obtain information about events that activate the Hard Fault handler.

Bits	Name	Description
31	DEBUGEVT	This bit is set if there is a fault related to debug. This is only possible when halting debug is not enabled. For monitor enabled debug, it only happens for BKPT when the current priority is higher than the monitor. When both halting and monitor debug are disabled, it only happens for debug events that are not ignored (minimally, BKPT). The Debug Fault Status Register is updated.
30	FORCED	Hard Fault activated because a Configurable Fault was received and cannot activate because of priority or because the Configurable Fault is disabled. The Hard Fault handler then has to read the other fault status registers to determine cause.
1	VECTTB	This bit is set if there is a fault because of vector table read on exception processing (Bus Fault). This case is always a Hard Fault. The return PC points to the pre-empted instruction.

1.3.1395 NVIC_DEBUG_FAULT_STATUS

Debug Fault Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NVIC_DEBUG_FAULT_STATUS: 0xE000ED30

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R/W	R/W	R/W	R/W	R/W
Name				EXTERNAL	VCATCH	DWTTRAP	BKPT	HALTED

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the Debug Fault Status Register to monitor: o external debug requests o vector catches o data watchpoint match o BKPT instruction execution o alt requests. Multiple flags in the Debug Fault Status Register can be set when multiple fault conditions occur. The register is read/write clear. This means that it can be read normally. Writing a 1 to a bit clears that bit.

Bits	Name	Description
4	EXTERNAL	External debug request flag: 1 = EDBGRQ signal asserted 0 = EDBGRQ signal not asserted. The processor stops on next instruction boundary.
3	VCATCH	Vector catch flag: 1 = vector catch occurred 0 = no vector catch occurred. When the VCATCH flag is set, a flag in one of the local fault status registers is also set to indicate the type of fault.
2	DWTTRAP	Data Watchpoint and Trace (DWT) flag: 1 = DWT match 0 = no DWT match. The processor stops at the current instruction or at the next instruction.

1.3.1395 NVIC_DEBUG_FAULT_STATUS (continued)

1	BKPT	BKPT flag: 1 = BKPT instruction execution 0 = no BKPT instruction execution. The BKPT flag is set by a BKPT instruction in flash patch code, and also by normal code. Return PC points to breakpoint containing instruction.
0	HALTED	Halt request flag: 1 = halt requested by NVIC, including step. The processor is halted on the next instruction. 0 = no halt request.

1.3.1396 NVIC_MEMMAN_FAULT_ADD

Memory Manage Fault Address Register

Reset: N/A

Register : Address

NVIC_MEMMAN_FAULT_ADD: 0xE000ED34

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	ADDRESS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	ADDRESS							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	ADDRESS							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	ADDRESS							

Use the Memory Manage Fault Address Register to read the address of the location that caused a Memory Manage Fault.

Bits	Name	Description
31:0	ADDRESS[31:0]	Mem Manage fault address field. ADDRESS is the data address of a faulted load or store attempt. When an unaligned access faults, the address is the actual address that faulted. Because an access can be split into multiple parts, each aligned, this address can be any offset in the range of the requested size. Flags in the Memory Manage Fault Status Register indicate the cause of the fault.

1.3.1397 NVIC_BUS_FAULT_ADD

Bus Fault Address Register

Reset: N/A

Register : Address

NVIC_BUS_FAULT_ADD: 0xE000ED38

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	ADDRESS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	ADDRESS							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	ADDRESS							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Name	ADDRESS							

Use the Bus Fault Address Register to read the address of the location that generated a Bus Fault.

Bits	Name	Description
31:0	ADDRESS[31:0]	Bus fault address field. ADDRESS is the data address of a faulted load or store attempt. When an unaligned access faults, the address is the address requested by the instruction, even if that is not the address that faulted. Flags in the Bus Fault Status Register indicate the cause of the fault.

1.3.1398 CORE_DBG_DBG_HLT_CS

Debug Halting Control and Status register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CORE_DBG_DBG_HLT_CS: 0xE000EDF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	NA	R	R	R	R
Name			C_SNAPSTALL		C_MASKINTSK	C_STEP	C_HALT	C_DEBUGEN

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					S_LOCKUP	S_SLEEP	S_HALT	S_REGRDYG

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Name							S_RESET_ST	S_RETIRE_ST

The purpose of the Debug Halting Control and Status Register (DHCSR) is to: o provide status information about the state of the processor o enable core debug o halt and step the processor. NOTE: Bits[31:16] have a seperate write path. Debug Key. 0xA05F must be written whenever this register is written. Reads back as status bits [25:16]. If not written as Key, the write operation is ignored and no bits are written into the register.

Bits	Name	Description
25	S_RESET_ST	Indicates that the core has been reset, or is now being reset, since the last time this bit was read. This a sticky bit that clears on read. So, reading twice and getting 1 then 0 means it was reset in the past. Reading twice and getting 1 both times means that it is being reset now (held in reset still).
24	S_RETIRE_ST	Indicates that an instruction has completed since last read. This is a sticky bit that clears on read. This determines if the core is stalled on a load/store or fetch.
19	S_LOCKUP	Reads as one if the core is running (not halted) and a lockup condition is present.
18	S_SLEEP	Indicates that the core is sleeping (WFI, WFE or SLEEP-ON-EXIT). Must use C_HALT to gain control or wait for interrupt to wake-up.

1.3.1398 CORE_DBG_DBG_HLT_CS (continued)

17	S_HALT	The core is in debug state when S_HALT is set.
16	S_REGRDYG	Register Read/Write on the Debug Core Register Selector register is available. Last transfer is complete.
5	C_SNAPSTALL	If the core is stalled on a load/store operation the stall ceases and the instruction is forced to complete. This enables Halting debug to gain control of the core. It can only be set if: C_DEBUGEN = 1 C_HALT = 1 The core reads S_RETIRE_ST as 0. This indicates that no instruction has advanced. This prevents misuse. The bus state is Unpredictable when this is used. S_RETIRE can detect core stalls on load/store operations.
3	C_MASKINTSK	Mask interrupts when stepping or running in halted debug. Does not affect NMI, which is not maskable. Must only be modified when the processor is halted (S_HALT == 1).
2	C_STEP	Steps the core in halted debug. When C_DEBUGEN = 0, this bit has no effect. Must only be modified when the processor is halted (S_HALT == 1).
1	C_HALT	Halts the core. This bit is set automatically when the core Halts. For example Breakpoint. This bit clears on core reset. This bit can only be written if C_DEBUGEN is 1, otherwise it is ignored. When setting this bit to 1, C_DEBUGEN must also be written to 1 in the same value (value[1:0] is 2'b11). The core can halt itself, but only if C_DEBUGEN is already 1 and only if it writes with b11).
0	C_DEBUGEN	Enables debug. This can only be written by AHB-AP and not by the core. It is ignored when written by the core, which cannot set or clear it. The core must write a 1 to it when writing C_HALT to halt itself.

1.3.1399 CORE_DBG_DBG_REG_SEL

Debug Core Register Selector Register

Reset: N/A

Register : Address

CORE_DBG_DBG_REG_SEL: 0xE000EDF4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			W:UUUUU				
HW Access	NA			R/W				
Name				REGSEL				

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							W:U
HW Access	NA							R/W
Name								REGWnR

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The purpose of the Debug Core Register Selector Register (DCRSR) is to select the processor register to transfer data to or from. This write-only register generates a handshake to the core to transfer data to or from Debug Core Register Data Register and the selected register. Until this core transaction is complete, bit[16], S_REGRDY, of the DHCSR is 0. NOTE: o Writes to this register in any size but word are Unpredictable. o PSR registers are fully accessible this way, whereas some read as 0 when using MSR instructions. o All bits can be written, but some combinations cause a fault when execution is resumed. o IT might be written and behaves as though in an IT block. o ICI can be written, though invalid values or when not used on an LDM/STM causes a fault, as would on return from exception. changing ICI from a value to 0 causes the underlying LDM/STM to start, not continue.

Bits	Name	Description
16	REGWnR	Write = 1 Read = 0

1.3.1399 CORE_DBG_DBG_REG_SEL (continued)

4:0	REGSEL[4:0]	5'b00000 = R0 5'b00001 = R1 ... 5'b01111 = DebugReturnAddress() 5'b10000 = xPSR/Flags, Execution Number, and state information 5'b10001 = MSP (Main SP) 5'b10010 = PSP (Process SP) 5'b10011 = RAZ/WI All unused values reserved

1.3.1400 CORE_DBG_DBG_REG_DATA

Debug Core Register Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CORE_DBG_DBG_REG_DATA: 0xE000EDF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	DATA							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	DATA							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	DATA							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Name	DATA							

The purpose of the Debug Core Register Data Register (DCRDR) is to hold data for reading and writing registers to and from the processor. This is the data value written to the register selected by the DCRSR. When the processor receives a request from the DCRS, this register is read or written by the processor using a normal load-store unit operation. If core register transfers are not being performed, software-based debug monitors can use this register for communication in non-halting debug.

Bits	Name	Description
31:0	DATA[31:0]	(no description)

1.3.1401 CORE_DBG_EXC_MON_CTL

Debug Exception and Monitor Control register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CORE_DBG_EXC_MON_CTL: 0xE000EDFC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	NA:000			R/W:0
HW Access	R	R	R	R	NA			R
Name	VC_STATERR	VC_CHKERR	VC_NOCPERRC	VC_MMERRM				VC_CORERESET

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Name						VC_HARDERRR	VC_INTERR	VC_BUSERR

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Name					MON_REQ	MON_STEP	MON_PEND	MON_EN

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								TRCENA

The purpose of the Debug Exception and Monitor Control Register (DEMCR) is: o Vector catching. That is, to cause debug entry when a specified vector is committed for execution. o Debug monitor control.

Bits	Name	Description
24	TRCENA	This bit must be set to 1 to enable use of the trace and debug blocks: o Data Watchpoint and Trace (DWT) o Instrumentation Trace Macrocell (ITM) o Embedded Trace Macrocell (ETM) o Trace Port Interface Unit (TPIU). This enables control of power usage unless tracing is required. The application can enable this, for ITM use, or use by a debugger.
19	MON_REQ	This enables the monitor to identify how it wakes up: 1 = woken up by MON_PEND 0 = woken up by debug exception.

1.3.1401 CORE_DBG_EXC_MON_CTL (continued)

18	MON_STEP	When MON_EN = 1, this steps the core. When MON_EN = 0, this bit is ignored. This is the equivalent to C_STEP. Interrupts are only stepped according to the priority of the monitor and settings of PRIMASK, FAULTMASK, or BASEPRI.
17	MON_PEND	Pend the monitor to activate when priority permits. This can wake up the monitor through the AHB-AP port. It is the equivalent to C_HALT for Monitor debug. This register does not reset on a system reset. It is only reset by a power-on reset. Software in the reset handler or later, or by the DAP must enable the debug monitor.
16	MON_EN	Enable the debug monitor. When enabled, the System handler priority register controls its priority level. If disabled, then all debug events go to Hard fault. C_DEBUGEN in the Debug Halting Control and Statue register overrides this bit. Vector catching is semi-synchronous. When a matching event is seen, a Halt is requested. Because the processor can only halt on an instruction boundary, it must wait until the next instruction boundary. As a result, it stops on the first instruction of the exception handler. However, two special cases exist when a vector catch has triggered: o If a fault is taken during vectoring, vector read or stack push error, the halt occurs on the corresponding fault handler, for the vector error or stack push. o If a late arriving interrupt comes in during vectoring, it is not taken. That is, an implementation that supports the late arrival optimization must suppress it in this case.
10	VC_HARDERRR	Debug trap on Hard Fault.
9	VC_INTERR	Debug Trap on interrupt/exception service errors. These are a subset of other faults and catches before BUSERR or HARDERR.
8	VC_BUSERR	Debug Trap on normal Bus error.
7	VC_STATERR	Debug trap on Usage Fault state errors.
6	VC_CHKERR	Debug trap on Usage Fault enabled checking errors.
5	VC_NOCPERRC	Debug trap on Usage Fault access to Coprocessor which is not present or marked as not present in CAR register.
4	VC_MMERRM	Debug trap on Memory Management faults.
0	VC_CORERESET	Reset Vector Catch. Halt running system if Core reset occurs.

1.3.1402 TPIU_SUPPORTED_SYNC_PRT_SZ

Supported Sync Port Sizes Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_SUPPORTED_SYNC_PRT_SZ: 0xE0040000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:1011			
HW Access	NA				R			
Name					SUPPORTED_SYNC_PRT_SZ			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register is read/write. Each bit location represents a single port size that is supported on the device, that is, 4, 2 or 1 in bit locations [3:0]. If the bit is set then that port size is permitted. By default the RTL is designed to support all port sizes, set to 0x0000000B. This register is constrained by the input tie-off MAXPORTSIZE. The external tie-off, MAXPORTSIZE, must be set during finalization of the ASIC to reflect the actual number of TRACEDATA signals wired to physical pins. This is to ensure that tools do not attempt to select a port width that an attached TPA cannot capture. The value on MAXPORTSIZE causes bits within the Supported Port Size register that represent wider widths to be clear, that is, unsupported.

Bits	Name	Description
3:0	SUPPORTED_SYNC_PRT_SZ[3:0]	Port size

1.3.1403 TPIU_CURRENT_SYNC_PRT_SZ

Current Sync Port Size Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_CURRENT_SYNC_PRT_SZ: 0xE0040004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0001			
HW Access	NA				R			
Name					CURRENT_SYNC_PRT_SZ			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register is read/write. The Current Sync Port Size Register has the same format as the Supported Sync Port Sizes Register but only one bit is set, and all others must be zero. Writing values with more than one bit set, or setting a bit that is not indicated as supported is not supported and causes Unpredictable behavior. It is more convenient to use the same format as the Supported Sync Port Sizes Register because it saves on having to decode the sizes later on in the device, and also maintains the format from the other register bank for checking for valid assignments. On reset this defaults to the smallest possible port size, 1 bit, and so reads as 0x00000001.

Bits	Name	Description
3:0	CURRENT_SYNC_PRT_SZ[3:0]	Port size

1.3.1404 TPIU_ASYNC_CLK_PRESCALER

Async Clock Prescaler Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ASYNC_CLK_PRESCALER: 0xE0040010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	PRESCALER							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R				
Name				PRESCALER				

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the Async Clock Prescaler Register to scale the baud rate of the asynchronous output.

Bits	Name	Description
12:0	PRESCALER[12:0]	Divisor for TRACECLKIN is Prescaler + 1.

1.3.1405 TPIU_PROTOCOL

Selected Pin Protocol Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_PROTOCOL: 0xE00400F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:01	
HW Access	NA						R	
Name							PROTOCOL	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the Selected Pin Protocol Register to select which protocol to use for trace output.l

Bits	Name	Description
1:0	PROTOCOL[1:0]	00 - TracePort mode 01 - SerialWire Output (Manchester). This is the reset value. 10 - SerialWire Output (NRZ) 11 - Reserved.

1.3.1406 TPIU_FORM_FLUSH_CTRL

Formatter and Flush Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_FORM_FLUSH_CTRL: 0xE0040304

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:1	R:0
HW Access	NA	R	R	R	NA		R	R
Name		FOnMan	FOnTrig	FOnFlIn			EnFCont	EnFTC

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	NA	R	R	R
Name			StopTrig	StopFI		TrigFI	TrigEVT	TrigIN

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Formatter and Flush Control Register.

Bits	Name	Description
13	StopTrig	Stop the formatter after a Trigger Event is observed.
12	StopFI	Stop the formatter after a flush completes.
10	TrigFI	Indicates a trigger on Flush completion.
9	TrigEVT	Indicate a trigger on a Trigger Event.
8	TrigIN	Indicate a trigger on TRIGIN being asserted.
6	FOnMan	Manually generate a flush of the system.
5	FOnTrig	Generate flush using Trigger event.
4	FOnFlIn	Generate flush using the FLUSHIN interface.
1	EnFCont	Continuous Formatting, no TRACECTL. This bit is set on reset.
0	EnFTC	Enable Formatting. Because TRACECTL is never present, this bit reads as zero.

1.3.1407 TPIU_ITATBCTR2

Integration Test Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ITATBCTR2: 0xE0040EF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								ATREADY1

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the Integration Test Registers to perform topology detection of the TPIU with other devices in a Cortex-M3 system. These registers enable direct control of outputs and the ability to read the value of inputs.

Bits	Name	Description
0	ATREADY1	This bit reads or sets the value of ATREADYS1 and ATREADYS2.

1.3.1408 TPIU_ITATBCTR0

Integration Test Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TPIU_ITATBCTR0: 0xE0040EF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								ATVALID1_2

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Use the Integration Test Registers to perform topology detection of the TPIU with other devices in a Cortex-M3 system. These registers enable direct control of outputs and the ability to read the value of inputs.

Bits	Name	Description
0	ATVALID1_2	This bit reads or sets the value of ATVALIDS1 OR-ed with ATVALIDS2.

1.3.1409 ETM_CTL

ETM Control register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CTL: 0xE0041000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:001			R/W:00		R/W:0	R/W:1
HW Access	R	R			R		R	R
Name	STALL_uP	PRT_SIZE			DataAccess		Moni-torCPRT	PD

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00		R/W:1	R/W:0	R/W:1	R/W:1	R/W:0	R/W:0
HW Access	R		R	R	R	R	R	R
Name	ContextIDsize		HLF_CLK	CycAcc_Trace	PRT_SEL	PROG	DBGRQ_CTL	BRNCH_OUT

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	R	R	R	R	R	R	R	
Name	DisableSoft-Wr	DisableReg-Wr	PRT_SIZE3	DataOnly-Mode	FilterCPRT	Suppress-Data	PRT_MODE	

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0000				R/W:000			R/W:0
HW Access	NA				R			R
Name					CoreSelect			InstrResAc-cCtrl

ETM control register controls general operation of the ETM, such as whether tracing is enabled.

Bits	Name	Description
27:25	CoreSelect[2:0]	If an ETM is shared between multiple cores, selects which core to trace. For the maximum value permitted, see bits [14:12] of the System Configuration Register bit assignments.To guarantee that the ETM is correctly synchronized to the new core, you must update these bits as follows: 1. Set bit [10] (ETM programming) and bit [0] (ETM power down) to b1. 2. Change the core select bits. 3. Clear bit [0] (ETM power down) to b0. 4 .Perform other programming required as normal. The ETM cannot be shared if JTAG access is supported.
24	InstrResAccCtrl	When this bit is set (b1), the Instrumentation resources can only be controlled when the processor is in a privileged mode. When this bit is clear (b0), the Instrumentation resources can be accessed in both privileged and User modes.

1.3.1409 ETM_CTL (continued)

23	DisableSoftWr	Register writes from software disabled. This bit can only be written by the debugger. This bit is not supported in all implementations. This bit reads back as zero if not supported.
22	DisableRegWr	Register writes from the debugger disabled. This bit can only be written by software. Typically a debugger can halt the processor to simulate software accesses. This means that, even if this bit is set, the debugger might be able to access the ETM registers. This bit is not supported in all implementations. This bit reads back as zero if not supported.
21	PRT_SIZE3	For ETMv3.0 and later use this in conjunction with bits [6:4].On an ETM reset this bit is 0.
20	DataOnlyMode	b0 = Instruction trace enabled. b1 = Instruction trace disabled. Data-only tracing is possible in this mode.
19	FilterCPRT	From ETMv3.0, this bit is used in conjunction with bit [1], the MonitorCPRT bit.
18	SuppressData	Used with bit [7] to suppress data
17:16	PRT_MODE[1:0]	These bits enable the trace port clocking mode to be set. On a TAP reset or ETM reset these bits are cleared to 0.
15:14	ContextIDsize[1:0]	b00 = no context ID tracing b01 = context ID bits [7:0] traced b10 = context ID bits [15:0] traced b11 = context ID bits [31:0] traced. Only the number of bytes specified is traced even if the new value is larger than this. From ETMv2.1, these bits read back as b0 if context ID tracing is not supported.
13	HLF_CLK	This bit controls whether trace is captured off both edges of TRACECLK or only the rising edge. On an ETM reset this bit is 0.
12	CycAcc_Trace	When set to b1, a precise cycle count of executed instructions can be extracted from the trace. In ETMv3, this is achieved by adding extra information into the trace, giving cycle counts even when TraceEnable is inactive.
11	PRT_SEL	This bit controls the external ETMEN pin. The possible values are: 0 ETMEN is LOW. 1 ETMEN is HIGH. This bit must be set by the trace software tools to ensure that trace output is enabled from this ETM. ETMEN can be used to enable the trace port pins to be shared with GPIO pins under the control of logic external to the ETM. On an ETM reset this bit is 0.
10	PROG	When set to 1, the ETM is being programmed. On an ETM reset this bit is set to b1.
9	DBGRQ_CTL	When set to 1 and the trigger event occurs, the DBGRQ output is asserted until DBGACK is observed. This enables the ARM processor to be forced into Debug state. On an ETM reset this bit is 0.
8	BRNCH_OUT	When set to 1 all branch addresses are output, even if the branch was because of a direct branch instruction. Setting this bit enables reconstruction of the program flow without having access to the memory image of the code being executed. On an ETM reset this bit is 0.
7	STALL_uP	The FIFOFULL output can be used to stall the processor to prevent overflow. This signal is only enabled when the stall processor bit is set to 1. When this bit is 0 the FIFOFULL output remains LOW at all times and the FIFO overflows if there are too many trace packets. On an ETM reset this bit is 0. If the FIFOFULL signal is not implemented then this bit reads as zero and ignores writes.

1.3.1409 ETM_CTL (continued)

6:4	PRT_SIZE[2:0]	The port size determines how many external pins are available to output the trace information. In ETMv1 and ETMv2 the port size is the number of bits in TRACEPKT. In ETMv3 the port size is the number of bits in TRACEDATA. This configuration determines how quickly the trace packets are extracted from the FIFO. From ETMv3 the port size field is 4 bits wide and bits [6:4] must be used in conjunction with bit [21], so that the port size encoding is given by bits [21, 6:4]. On an ETM reset these bits correspond to the lowest supported port width.
3:2	DataAccess[1:0]	b00 = no data tracing b01 = trace only the data portion of the access b10 = trace only the address portion of the access b11 = trace both the address and the data of the access. On an ETM reset these bits are b00.
1	MonitorCPRT	When b0, the CPRTs are not traced. When set to b1, the CPRTs are traced. On an ETM reset this bit is b0. From ETMv.3.0, this bit is used with bit [19].
0	PD	A pin controlled by this bit enables the ETM power to be controlled externally. The external pin is often ETMPWRDOWN or inverted as ETMPWRUP. This bit must be cleared by the trace software tools at the beginning of a debug session.When this bit is set to 1, the ETM must be powered down and disabled, and then operated in a low power mode with all clocks stopped. When this bit is set to 1, writes to some registers and fields might be ignored. You can always write to the following registers and fields: o ETM Control Register, bit [0] and bits [27:25] o Lock Access Register o Claim Tag Set Register o Claim Tag Clear Register o Operating System Lock Access Register. o When the ETM Control Register is written with this bit set to 1, bits other than bit [0] and bits [27:25] might be ignored. On an ETM reset this bit is set to 1.

1.3.1410 ETM_CFG_CODE

ETM Configuration code register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CFG_CODE: 0xE0041004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R				R			
Name	DATA_CMPS				ADD_CMPS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:000			R:00000				
HW Access	R			R				
Name	COUNTERS			MMD_INPUT				

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:0	R:000			R:000			R:0
HW Access	R	R			R			R
Name	FIFOFULL_LGC	EXT_OUT			EXT_IN			SEQ

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:0	NA:000			R:1	R:1	R:00	
HW Access	R	NA			R	R	R	
Name	ETM_ID				COPRC_SUPPORT	TRACE_START_STOP	CTXTID_CMP	

The ETM Configuration Code Register enables the debugger to read the IMPLEMENTATION DEFINED configuration of the ETM, giving the number of each type of resource. Where a value indicates the number of instances of a particular resource, zero indicates that there are no implemented resources of that resource type.

Bits	Name	Description
31	ETM_ID	When set to 1, this bit indicates that the ETM ID Register, 0x79, is present and defines the ETM architecture version in use. When set to 0, this bit indicates that the ETM ID Register is not present.
27	COPRC_SUPPORT	Coprocessor or memory-mapped access to registers supported.
26	TRACE_START_STOP	When set to 1, the trace start/stop block is present.
25:24	CTXTID_CMP[1:0]	Number of Context ID comparators.
23	FIFOFULL_LGC	When set to 1, the FIFOFULL logic is present. This bit is used in conjunction with bit [8] of the System Configuration Register, register 0x05, of the processor core connected to the ETM.
22:20	EXT_OUT[2:0]	Number of external outputs.
19:17	EXT_IN[2:0]	Number of external inputs.

1.3.1410 ETM_CFG_CODE (continued)

16	SEQ	When set to b1 the sequencer is present.
15:13	COUNTERS[2:0]	Number of counters.
12:8	MMD_INPUT[4:0]	Number of memory map decoder inputs.
7:4	DATA_CMPS[3:0]	Number of data value comparators.
3:0	ADD_CMPS[3:0]	Number of pairs of address comparators.

1.3.1411 ETM_TRIG_EVENT

Trigger Event Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_TRIG_EVENT: 0xE0041008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	W:0000000						
HW Access	R	R						
Name	RSRC_B	RSRC_A						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	W:00		W:000000					
HW Access	R		R					
Name	FCN		RSRC_B					

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							W:0
HW Access	NA							R
Name								FCN

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Trigger Event Register defines the event that controls the trigger.

Bits	Name	Description
16:14	FCN[2:0]	Fcn.
13:7	RSRC_B[6:0]	Resource B.
6:0	RSRC_A[6:0]	Resource A.

1.3.1412 ETM_STATUS

ETM Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_STATUS: 0xE0041010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R:0	R:0
HW Access	NA				R	R	R	R
Name					TRIG_BIT	TRACE_STATUS	PROG_BIT	OVERFLOW_FLAG

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The ETM Status Register provides information about the current status of the trace and trigger logic.

Bits	Name	Description
3	TRIG_BIT	Trigger bit. Set when the trigger occurs, and prevents the trigger from being output until the ETM is next programmed.
2	TRACE_STATUS	Holds the current status of the trace start/stop resource. If set to 1, it indicates that a trace on address has been matched, without a corresponding trace off address match.
1	PROG_BIT	The current effective value of the ETM Programming bit (ETM Control Register bit [10]). You must wait for this bit to go to 1 before you start to program the ETM. If you read other bits in the ETM Status Register while this bit is 0, some instructions might not have taken effect. It is recommended that you set the ETM Programming bit and wait for this bit to go to 1 before reading the overflow bit.In ETMv3.2 and later this bit remains 0 if there is any data in the FIFO. This ensures that the FIFO is empty before the ETM programming is changed.
0	OVERFLOW_FLAG	If set to 1, there is an overflow that has not yet been traced. This bit is cleared to 0 when either: o trace is restarted. o the ETM Power Down bit, bit [0] of the ETM Control Register, 0x00, is set to 1.

1.3.1413 ETM_SYS_CFG

System Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_SYS_CFG: 0xE0041014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R:000		
HW Access	NA					R		
Name						MAX_PRT_SIZE		

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R:000			R/W:0	R:0	R:0	R:0
HW Access	NA	R			R	R	R	R
Name		CORE_SUPPORT			PRT_MODE _SUPPORT	PRT_SIZE_ SUPPORT	MAX_PRT_ SIZE3	FIFOFULL_ SUPPORT

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:000000						R:0	NA:0
HW Access	NA						R	NA
Name							NO_FETCH _CMP	

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The System Configuration Register shows the ETM features supported by the ASIC. The contents of this register are based on inputs provided by the ASIC.

Bits	Name	Description
17	NO_FETCH_CMP	No Fetch comparisons. Address comparators are not capable of performing fetch-stage comparisons. Setting bits [2:0] of an Address Access Type Register to b000 (instruction fetch) causes the comparator to have UNPREDICTABLE behavior.
14:12	CORE_SUPPORT[2:0]	Number of supported cores minus 1. The value given here is the maximum value that can be written to bits [27:25] of the ETM Control Register, 0x00. These bits must be b000 if JTAG access is supported.
11	PRT_MODE_SUPPORT	Port mode supported. Set to 1 if the currently selected port mode is supported internally or externally.
10	PRT_SIZE_SUPPORT	Port size supported. Set to 1 if the currently selected port size is supported internally or externally for the currently selected port mode. Enables more complex port sizes to be supported.
9	MAX_PRT_SIZE3	Maximum port size[3]. This bit is used in conjunction with bits [2:0].

1.3.1413 ETM_SYS_CFG (continued)

8	FIFOFULL_SUPPORT	If set to 1, FIFOFULL is supported. This bit is used in conjunction with bit [23] of the ETM Configuration Register.
2:0	MAX_PRT_SIZE[2:0]	Maximum port size[2:0]. This bit is used in conjunction with bit [9]. The value given here is the maximum size supported by both the ETM and the ASIC. Smaller sizes might or might not be supported. Check bit [10] for precise details of supported modes.

1.3.1414 ETM_TRACE_ENB_EVENT

Trace Enable Event Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_TRACE_ENB_EVENT: 0xE0041020

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	W:0000000						
HW Access	R	R						
Name	RSRC_B	RSRC_A						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	W:00		W:000000					
HW Access	R		R					
Name	FCN		RSRC_B					

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							W:0
HW Access	NA							R
Name								FCN

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The TraceEnable Event Register defines the TraceEnable enabling event.

Bits	Name	Description
16:14	FCN[2:0]	Fcn.
13:7	RSRC_B[6:0]	Resource B.
6:0	RSRC_A[6:0]	Resource A.

1.3.1415 ETM_TRACE_EN_CTRL1

TraceEnable Control 1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_TRACE_EN_CTRL1: 0xE0041024

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Name	ADD_CMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	W:00000000							
HW Access	R							
Name	MMD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	W:00000000							
HW Access	R							
Name	MMD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:000000						W:0	W:0
HW Access	NA						R	R
Name							TRACE_CTRL_EN	EXC_INC_FLAG

The TraceEnable Control 1 Register: o enables the start/stop logic o determines whether the resources specified in the TraceEnable Control 1 and TraceEnable Control 2 Registers are used for include or exclude control o specifies the address range comparators used for include/exclude control o specifies the memory map decodes (MMDs) used for include/exclude control. o a write-only register, although in architecture versions 3.1 and later it is read/write when bit [11] of the Configuration Code Extension Register is set

Bits	Name	Description
25	TRACE_CTRL_EN	Trace start/stop enable. The possible values of this bit are: 0 Tracing is unaffected by the trace start/stop logic. 1 Tracing is controlled by the trace on and off addresses configured for the trace start/stop logic.
24	EXC_INC_FLAG	Include/exclude control. The possible values of this bit are: 0 Include. The specified resources indicate the regions where tracing can occur. When outside this region tracing is prevented. 1 Exclude. The resources, specified in bits [23:0] and in the TraceEnable Control 2 Register, indicate regions to be excluded from the trace. When outside an exclude region, tracing can occur.
23:8	MMD[15:0]	When a bit is set to 1, it selects memory map decode 16-1 for include/exclude control. For example, bit [8] set to 1 selects MMD 1.

1.3.1415 ETM_TRACE_EN_CTRL1 (continued)

7:0	ADD_CMP[7:0]	When a bit is set to 1, it selects address range comparator 8-1 for include/exclude control. For example, bit [0] set to 1 selects address range comparator 1.

1.3.1416 ETM_FIFOFULL_LEVEL

FIFOFULL Level Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_FIFOFULL_LEVEL: 0xE004102C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	FIFOFULL_LVL							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The FIFOFULL Level Register holds the level below which the FIFO is considered full, although its function varies for different ETM architectures. From ETMv3.0 the value in this register also controls the point at which data trace suppression occurs.

Bits	Name	Description
7:0	FIFOFULL_LVL[7:0]	The number of bytes left in the FIFO, below which the FIFOFULL or SuppressData signal is asserted. For example, setting this value to 15 causes data trace suppression or processor stalling, if enabled, when there are less than 15 free bytes in the FIFO.

1.3.1417 ETM_SYNC_FREQ

Synchronization Frequency Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_SYNC_FREQ: 0xE00411E0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	SyncFrequency							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0000				R/W:0100			
HW Access	NA				R			
Name					SyncFrequency			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Synchronization Frequency Register holds the trace synchronization frequency value.

Bits	Name	Description
11:0	SyncFrequency[11:0]	Synchronization frequency (default = 1024)

1.3.1418 ETM_ETM_ID

ETM ID Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_ETM_ID: 0xE00411E4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0010				R:0000			
HW Access	R				R			
Name	MinorETMArchVer				ImplRev			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0010			
HW Access	R				R			
Name	CoreFam				MajorETMArchVer			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:000			R:0	R:0	R:0	NA:0	R:0
HW Access	NA			R	R	R	NA	R
Name				BrPcktEnc	TrustZone-Supp	Thumb2Supp		LoadPC-First

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:01000001							
HW Access	R							
Name	ImplCode							

The ETM ID Register holds the ETM architecture variant, and precisely defines the programmer's model for the ETM.

Bits	Name	Description
31:24	ImplCode[7:0]	Implementor code. The following code is defined, all other values are reserved by ARM Limited: 0x41 = A (ARM Limited).
20	BrPcktEnc	Branch packet encoding implemented: If this bit is not set (b0), the ETM implements the original branch packet encoding. If this bit is set (b1), the ETM implements the alternative branch packet encoding.
19	TrustZoneSupp	TrustZone support. If this bit is not set (b0), then the ETM behaves as if the processor is in secure state at all times. If this bit is set (b1), the TrustZone architectural extensions are supported by the processor.
18	Thumb2Supp	Thumb-2 support. If this bit is not set (b0), BL and BLX immediate are traced as two instructions. Exceptions might occur between these instructions. If this bit is set (b1), the Thumb-2 architectural extensions are supported by the processor. Thumb 32-bit BL/BLX instructions are traced as one instruction.

1.3.1418 ETM_ETM_ID (continued)

16	LoadPCFirst	Load pc first. If this bit is set to b1, LSMs with the pc in the list load the pc first, followed by the other registers in the normal order. This can be decompressed by using the following procedure: 1. Calculate the number of items transferred by the LSM by looking at the code image. 2. As each item is read, assign an address equal to 4 greater than the previous one as normal. 3. When the number of items read equals the total number of items transferred, subtract (4 * number of items) from each address other than the first.
15:12	CoreFam[3:0]	Core family. The meaning of this field depends on the value of the Implementor Code.The following apply if Implementor code = A (ARM Limited), and are the only values that are defined. All other values are reserved by ARM Limited: b0000 = ARM7 core b0001 = ARM9 core b0010 = ARM10 core b0011 = ARM11 core b1111 = Defined elsewhere
11:8	MajorETMArchVer[3:0]	Major ETM architecture version number, see The ETM architecture version: b0000 = ETMv1 b0001 = ETMv2 b0010 = ETMv3
7:4	MinorETMArchVer[3:0]	Minor ETM architecture version number
3:0	ImplRev[3:0]	Implementation revision.

1.3.1419 ETM_CFG_CODE_EXT

Configuration Code Extension Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CFG_CODE_EXT: 0xE00411E8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000					R:000		
HW Access	R					R		
Name	SzExtInBus					NumExtInSel		

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:000			R:1	R:0	R:000		
HW Access	R			R	R	R		
Name	NumInstr			DataAddr-Supp	RegRead-able	SzExtInBus		

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00		R:0	R:0	R:0000			
HW Access	NA		R	R	R			
Name			EmbICEBe-hCtrl	TraceSSBlk	NumEmbICE			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Configuration Code Extension Register holds additional bits for ETM configuration code. This register describes the extended external inputs.

Bits	Name	Description
21	EmbICEBehCtrl	EmbeddedICE Behavior Control Register implemented. This bit is b1 if the register is implemented, and b0 if it is not implemented.
20	TraceSSBlk	Trace Start/Stop block can use EmbeddedICE watchpoint inputs. This bit is b1 if the Trace Start/Stop block can used these inputs, and is b0 otherwise.
19:16	NumEmbICE[3:0]	Number of EmbeddedICE watchpoint inputs implemented. This field can take any value from b0000 (0 inputs) to b1000 (8 inputs).
15:13	NumInstr[2:0]	Number of Instrumentation resources supported. The maximum value of this field is b100, for four Instrumentation resources.
12	DataAddrSupp	Set to b1 if data address comparisons are not supported.
11	RegReadable	Set to b1 if all registers are readable.
10:3	SzExtInBus[7:0]	Size of extended external input bus. This field must be 0 if bits [2:0] are 0.

1.3.1419 ETM_CFG_CODE_EXT (continued)

2:0	NumExtInSel[2:0]	Number of extended external input selectors.

1.3.1420 ETM_TR_SS_EMBICE_CTRL

Trace Start/Stop EmbeddedICE Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_TR_SS_EMBICE_CTRL: 0xE00411F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	StrtResSel							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	StpResSel							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Trace Start/Stop EmbeddedICE Control Register specifies the EmbeddedICE watchpoint comparator inputs that are used as trace start and stop resources.

Bits	Name	Description
23:16	StpResSel[7:0]	Stop resource selection. Setting a bit in this field to b1 selects the corresponding EmbeddedICE watchpoint input as a TraceEnable stop resource. Bit [16] corresponds to input 1, bit [17] to input 2, and this pattern continues up to bit [23] corresponding to input 8.
7:0	StrtResSel[7:0]	Start resource selection. Setting a bit in this field to b1 selects the corresponding EmbeddedICE watchpoint input as a TraceEnable start resource. Bit [0] corresponds to input 1, bit [1] to input 2, and this pattern continues up to bit [7] corresponding to input 8.

1.3.1421 ETM_CS_TRACE_ID

CoreSight Trace ID Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CS_TRACE_ID: 0xE0041200

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R						
Name		TraceID						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The CoreSight Trace ID Register defines the 7-bit Trace ID, for output to the trace bus.

Bits	Name	Description
6:0	TraceID[6:0]	Trace ID to output onto the trace bus. At reset this register is 0x00.

1.3.1422 ETM_OS_LOCK_ACCESS

OS Lock Access Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_OS_LOCK_ACCESS: 0xE0041300

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Name	LOCK_UNLOCK_ACCESS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	W:00000000							
HW Access	R							
Name	LOCK_UNLOCK_ACCESS							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	W:00000000							
HW Access	R							
Name	LOCK_UNLOCK_ACCESS							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	W:00000000							
HW Access	R							
Name	LOCK_UNLOCK_ACCESS							

The OS Lock Access Register (OSLAR) is used to lock and unlock access to ETM debug registers.

Bits	Name	Description
31:0	LOCK_UNLOCK_ACCESS[31:0]	Write 0xC5ACCE55 to this field to lock the ETM debug registers. Write any other value to this field to unlock the ETM debug registers.

1.3.1423 ETM_OS_LOCK_STATUS

OS Lock Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_OS_LOCK_STATUS: 0xE0041304

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R:1	R:0	R:0
HW Access	NA					W	W	W
Name						Access32	Locked	LockImpl

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The OS Lock Status Register (OSLSR) is used to find whether the ETM debug registers are locked. It can also be used to find whether ETM debug register locking is implemented on your ETM macrocell.

Bits	Name	Description
2	Access32	32-bit access bit. If ETM debug register locking is implemented then this bit is set (b1), to indicate that 32-bit access is required to write to the OS Lock Access Register to lock the ETM debug registers.
1	Locked	Locked bit: b0: ETM debug registers are not locked. b1: ETM debug registers are locked. Any access to these registers returns a slave-generated error response. The reset value of this field corresponds to the value on the DBGOSLOCKINIT pin.
0	LockImpl	ETM debug register locking implemented: b0: OS Lock and OS Save/Restore registers are not implemented. In this case, bits [31:0] of the OS Lock Status register reads as zero. b1: OS Lock and OS Save/Restore registers are implemented and it is possible to set the OS Lock for this macrocell, to lock the ETM debug registers. The reset value of this field is Implementation-defined.

1.3.1424 ETM_INT_MODE_CTRL

Integration Mode Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_INT_MODE_CTRL: 0xE0041F00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Name								EnIntTest

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Integration Mode Control Register is used to enable topology detection or to check integration testing.

Bits	Name	Description
0	EnIntTest	When set to b1, the device goes into an integration mode to enable Topology Detection or Integration Testing to be checked. At reset this bit is b0.

1.3.1425 ETM_CLM_TAG_SET

Claim Tag Set Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CLM_TAG_SET: 0xE0041FA0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:11111111							
HW Access	R							
Name	ClaimTagSet							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Claim Tag Set Register is used to set bits in the claim tag and find the number of bits supported by the claim tag.

Bits	Name	Description
7:0	ClaimTagSet[7:0]	On reads, returns 0xFF. On writes, a 1 in a bit position causes the corresponding bit in the claim tag value to be set.

1.3.1426 ETM_CLM_TAG_CLR

Claim Tag Clear Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CLM_TAG_CLR: 0xE0041FA4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Name	ClaimTagClear							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Claim Tag Clear Register is used to clear bits in the claim tag to b0, and to find the current value of the claim tag.

Bits	Name	Description
7:0	ClaimTagClear[7:0]	On reads, returns the current claim tag value. On writes, a 1 in a bit position causes the corresponding bit in the claim tag value to be cleared to b0.

1.3.1427 ETM_LOCK_ACCESS

Lock Access Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_LOCK_ACCESS: 0xE0041FB0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Name	LOCK_UNLOCK_ACCESS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	W:00000000							
HW Access	R							
Name	LOCK_UNLOCK_ACCESS							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	W:00000000							
HW Access	R							
Name	LOCK_UNLOCK_ACCESS							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	W:00000000							
HW Access	R							
Name	LOCK_UNLOCK_ACCESS							

The Lock Access Register (LAR or LOCKACCESS) is used to lock and unlock access to all other ETM registers.

Bits	Name	Description
31:0	LOCK_UNLOCK_ACCESS[31:0]	A write of 0xC5ACCE55 unlocks the ETM. A write of any other value locks the ETM. Writes to this register from an interface that ignores the lock registers are ignored.

1.3.1428 ETM_LOCK_STATUS

Lock Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_LOCK_STATUS: 0xE0041FB4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R:0	R:0	R:0
HW Access	NA					W	W	W
Name						Access32	Locked	LockImpl

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Lock Status Register has two uses: - If you read this register from any interface, you can check bit [0] to find out whether the lock registers are implemented for the interface you are using. - If you read this register from an interface for which lock registers are implemented, you can check bit [1] to find out whether the registers are currently locked.

Bits	Name	Description
2	Access32	Reads as b0. Indicates that the Lock Access Register is 32 bits.
1	Locked	Indicates if the ETM is locked: b1: Writes are ignored b0: Writes are permitted. If this register is accessed from an interface where the lock registers are ignored, this field reads as b0 regardless of whether the ETM is locked.
0	LockImpl	Indicates if the lock registers are implemented for this interface: b1: This access is from an interface that requires the ETM to be unlocked b0: This access is from an interface that ignores the lock registers.

1.3.1429 ETM_AUTH_STATUS

Authentication Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_AUTH_STATUS: 0xE0041FB8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00		R:00		R:00		R:00	
HW Access	W		W		R		W	
Name	NonInvSupp		SInvSupp		NSNonInvSupp		NSInvSupp	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Authentication Status Register reports the level of tracing currently permitted by the authentication signals provided to the ETM.

Bits	Name	Description
7:6	NonInvSupp[1:0]	Permission for secure non-invasive debug.
5:4	SInvSupp[1:0]	Reads as b00: Secure invasive debug not supported by the ETM.
3:2	NSNonInvSupp[1:0]	Permission for Non-secure non-invasive debug. This field is only implemented if the processor core implemented with the ETM supports the TrustZone security extensions. When this field is implemented the permitted values are: b10: Non-secure non-invasive debug disabled b11: Non-secure non-invasive debug enabled. This field is a logical OR of the NIDEN and DBGEN signals. It takes the value b11 when the OR is TRUE, and b10 when the OR is FALSE. If the core does not support the TrustZone extensions, bits [3:2] are reserved, read as b00.
1:0	NSInvSupp[1:0]	Reads as b00: Non-secure invasive debug not supported by the ETM.

1.3.1430 ETM_DEV_TYPE

Device Type Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_DEV_TYPE: 0xE0041FCC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0001				R:0011			
HW Access	R				R			
Name	SubType				MainType			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

The Device Type Register returns the CoreSight device type of the component.

Bits	Name	Description
7:4	SubType[3:0]	0x1 Sub type, processor trace.
3:0	MainType[3:0]	0x3 Main type, trace source.

1.3.1431 ETM_PID4

ETM Peripheral Identification Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID4: 0xE0041FD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000100							
HW Access	R/W							
Name	PID4							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID4[7:0]	Peripheral Identification Register 4

1.3.1432 ETM_PID5

ETM Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID5: 0xE0041FD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID5							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID5[7:0]	Peripheral Identification Register 5

1.3.1433 ETM_PID6

ETM Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID6: 0xE0041FD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID6							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID6[7:0]	Peripheral Identification Register 6

1.3.1434 ETM_PID7

ETM Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID7: 0xE0041FDC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID7							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID7[7:0]	Peripheral Identification Register 7

1.3.1435 ETM_PID0

ETM Peripheral Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID0: 0xE0041FE0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000001							
HW Access	R/W							
Name	PID0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID0[7:0]	Peripheral Identification Register 0

1.3.1436 ETM_PID1

ETM Peripheral Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID1: 0xE0041FE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10110000							
HW Access	R/W							
Name	PID1							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID1[7:0]	Peripheral Identification Register 1

1.3.1437 ETM_PID2

ETM Peripheral Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID2: 0xE0041FE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00011011							
HW Access	R/W							
Name	PID2							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID2[7:0]	Peripheral Identification Register 2

1.3.1438 ETM_PID3

ETM Peripheral Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_PID3: 0xE0041FEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID3							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	PID3[7:0]	Peripheral Identification Register 3

1.3.1439 ETM_CID0

ETM Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CID0: 0xE0041FF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00001101							
HW Access	R/W							
Name	CID0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID0[7:0]	Component Identification Register 0

1.3.1440 ETM_CID1

ETM Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CID1: 0xE0041FF4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:11100000							
HW Access	R/W							
Name	CID1							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID1[7:0]	Component Identification Register 1

1.3.1441 ETM_CID2

ETM Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CID2: 0xE0041FF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000101							
HW Access	R/W							
Name	CID2							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID2[7:0]	Component Identification Register 2

1.3.1442 ETM_CID3

ETM Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ETM_CID3: 0xE0041FFC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10110001							
HW Access	R/W							
Name	CID3							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Name								

This register mirrors the PID/CID contents of the ROM memory table

Bits	Name	Description
7:0	CID3[7:0]	Component Identification Register 3

1.3.1443 ROM_TABLE_NVIC

NVIC

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_NVIC: 0xE00FF000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000011							
HW Access	R							
Name	NVIC							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:11110000							
HW Access	R							
Name	NVIC							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:11110000							
HW Access	R							
Name	NVIC							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:11111111							
HW Access	R							
Name	NVIC							

(no description)

Bits	Name	Description
31:0	NVIC[31:0]	Points to the NVIC at 0xE000E000.

1.3.1444 ROM_TABLE_DWT

DWT

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_DWT: 0xE00FF004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000011							
HW Access	R							
Name	DWT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00100000							
HW Access	R							
Name	DWT							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:11110000							
HW Access	R							
Name	DWT							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:11111111							
HW Access	R							
Name	DWT							

(no description)

Bits	Name	Description
31:0	DWT[31:0]	DWT Points to the Data Watchpoint and Trace block at 0xE0001000.

1.3.1445 ROM_TABLE_FPB

FPB

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_FPB: 0xE00FF008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000011							
HW Access	R							
Name	FPB							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00110000							
HW Access	R							
Name	FPB							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:11110000							
HW Access	R							
Name	FPB							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:11111111							
HW Access	R							
Name	FPB							

(no description)

Bits	Name	Description
31:0	FPB[31:0]	FPB Points to the Flash Patch and Breakpoint block at 0xE0002000.

1.3.1446 ROM_TABLE_ITM

ITM

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_ITM: 0xE00FF00C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000011							
HW Access	R							
Name	ITM							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00010000							
HW Access	R							
Name	ITM							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:11110000							
HW Access	R							
Name	ITM							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:11111111							
HW Access	R							
Name	ITM							

(no description)

Bits	Name	Description
31:0	ITM[31:0]	Points to the Instrumentation Trace block at 0xE0000000.

1.3.1447 ROM_TABLE_TPIU

TPIU

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_TPIU: 0xE00FF010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000011							
HW Access	R							
Name	TPIU							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00010000							
HW Access	R							
Name	TPIU							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:11110100							
HW Access	R							
Name	TPIU							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:11111111							
HW Access	R							
Name	TPIU							

(no description)

Bits	Name	Description
31:0	TPIU[31:0]	Points to the TPIU. Value has bit [0] set to 1 if TPIU is fitted. TPIU is at 0xE0040000

1.3.1448 ROM_TABLE_ETM

ETM

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_ETM: 0xE00FF014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000011							
HW Access	R							
Name	ETM							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00100000							
HW Access	R							
Name	ETM							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:11110100							
HW Access	R							
Name	ETM							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:11111111							
HW Access	R							
Name	ETM							

(no description)

Bits	Name	Description
31:0	ETM[31:0]	Points to the ETM. Value has bit [0] set to 1 if ETM is fitted. ETM is at 0xE0041000.

1.3.1449 ROM_TABLE_END

END

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_END: 0xE00FF018

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Name	END							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R							
Name	END							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R							
Name	END							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R							
Name	END							

(no description)

Bits	Name	Description
31:0	END[31:0]	Marks the end of the ROM table. If CoreSight components are added, they are added starting from this location and the End marker is moved to the next location after the additional components.

1.3.1450 ROM_TABLE_MEMTYPE

MEMTYPE

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_MEMTYPE: 0xE00FFFCC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000001							
HW Access	R							
Name	MEMTYPE							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R							
Name	MEMTYPE							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R							
Name	MEMTYPE							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R							
Name	MEMTYPE							

(no description)

Bits	Name	Description
31:0	MEMTYPE[31:0]	Bits [31:1] RAZ. Bit [0] is set when the system memory map is accessible using the DAP. Bit [0] is clear when only debug resources are accessible using the DAP.

1.3.1451 ROM_TABLE_PID4

ROM Table Peripheral Identification Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID4: 0xE00FFFD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID4							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID4							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID4							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID4							

ROM Table Peripheral Identification Register 4

Bits	Name	Description
31:0	PID4[31:0]	Peripheral Identification Register 4

1.3.1452 ROM_TABLE_PID5

ROM Table Peripheral Identification Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID5: 0xE00FFFD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID5							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID5							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID5							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID5							

ROM Table Peripheral Identification Register 5

Bits	Name	Description
31:0	PID5[31:0]	Peripheral Identification Register 5

1.3.1453 ROM_TABLE_PID6

ROM Table Peripheral Identification Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID6: 0xE00FFFD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID6							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID6							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID6							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID6							

ROM Table Peripheral Identification Register 6

Bits	Name	Description
31:0	PID6[31:0]	Peripheral Identification Register 6

1.3.1454 ROM_TABLE_PID7

ROM Table Peripheral Identification Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID7: 0xE00FFFDC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID7							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID7							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID7							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID7							

ROM Table Peripheral Identification Register 7

Bits	Name	Description
31:0	PID7[31:0]	Peripheral Identification Register 7

1.3.1455 ROM_TABLE_PID0

ROM Table Peripheral Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID0: 0xE00FFFE0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID0							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID0							

ROM Table Peripheral Identification Register 0

Bits	Name	Description
31:0	PID0[31:0]	Peripheral Identification Register 0

1.3.1456 ROM_TABLE_PID1

ROM Table Peripheral Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID1: 0xE00FFFE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID1							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID1							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID1							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID1							

ROM Table Peripheral Identification Register 1

Bits	Name	Description
31:0	PID1[31:0]	Peripheral Identification Register 1

1.3.1457 ROM_TABLE_PID2

ROM Table Peripheral Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID2: 0xE00FFFE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID2							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID2							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID2							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID2							

ROM Table Peripheral Identification Register 2

Bits	Name	Description
31:0	PID2[31:0]	Peripheral Identification Register 2

1.3.1458 ROM_TABLE_PID3

ROM Table Peripheral Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_PID3: 0xE00FFFEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID3							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID3							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID3							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	PID3							

ROM Table Peripheral Identification Register 3

Bits	Name	Description
31:0	PID3[31:0]	Peripheral Identification Register 3

1.3.1459 ROM_TABLE_CID0

ROM Table Component Identification Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_CID0: 0xE00FFFF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00001101							
HW Access	R/W							
Name	CID0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID0							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID0							

ROM Table Component Identification Register 0

Bits	Name	Description
31:0	CID0[31:0]	Component Identification Register 0

1.3.1460 ROM_TABLE_CID1

ROM Table Component Identification Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_CID1: 0xE00FFFF4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00010000							
HW Access	R/W							
Name	CID1							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID1							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID1							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID1							

ROM Table Component Identification Register 1

Bits	Name	Description
31:0	CID1[31:0]	Component Identification Register 1

1.3.1461 ROM_TABLE_CID2

ROM Table Component Identification Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_CID2: 0xE00FFFF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000101							
HW Access	R/W							
Name	CID2							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID2							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID2							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID2							

ROM Table Component Identification Register 2

Bits	Name	Description
31:0	CID2[31:0]	Component Identification Register 2

1.3.1462 ROM_TABLE_CID3

ROM Table Component Identification Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ROM_TABLE_CID3: 0xE00FFFFC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10110001							
HW Access	R/W							
Name	CID3							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID3							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID3							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Name	CID3							

ROM Table Component Identification Register 3

Bits	Name	Description
31:0	CID3[31:0]	Component Identification Register 3

Revision History

Revision History

Document Title: CY8C55, CY8C54, CY8C53, CY8C52 PSoC® 5 REGISTERS TRM (TECHNICAL REFERENCE MANUAL) Document Number: 001-72718				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	3424459	10/28/2011	VVSK	Initial release
*A	3524248	02/14/2012	VVSK	Incorporated updates through 02/13/2012
*B	3637274	06/05/2012	VVSK	Incorporated updates through 06/04/2012