PCB Design of Signal Conditioning Circuit for MMC

Submitted by

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INTRODUCTION:

The signal conditioning circuit forms an important component in the data acquisition system. The output of the Hall Effect voltage and current transducers are in the range of +5 V. These are now converted to 0-3 V range to make it compatible to the analog channels of the Digital Signal Processor. The allowable input range for the DSP is 0-3 V. The input signals should not exceed this limit at any condition. This is achieved using an OPAMP (TL064) based signal conditioning circuit

THE WORKING PRINCIPLE:

The signal conditioning circuit consists of four stages. The first stage is a unity follower stage which offers very high impedance to the input signals so as to avoid loading effects on measured quantities. The signal of +5 V is given to the attenuator stage which has a gain of 0.3. Thus, output is in the range of +1.5 V with 180 degree phase shift. The level shifter stage adds A DC offset voltage of -1.5 V under the inverting mode to make the output signal with 0-3 V range. The precision rectifier stage prevents any excursion of negative voltage. A zener diode (ZD) with a cut-in voltage of 3.3 V is connected in reversed bias condition at the output stage to prevent any over-voltage.

CIRCUIT DIAGRAM:

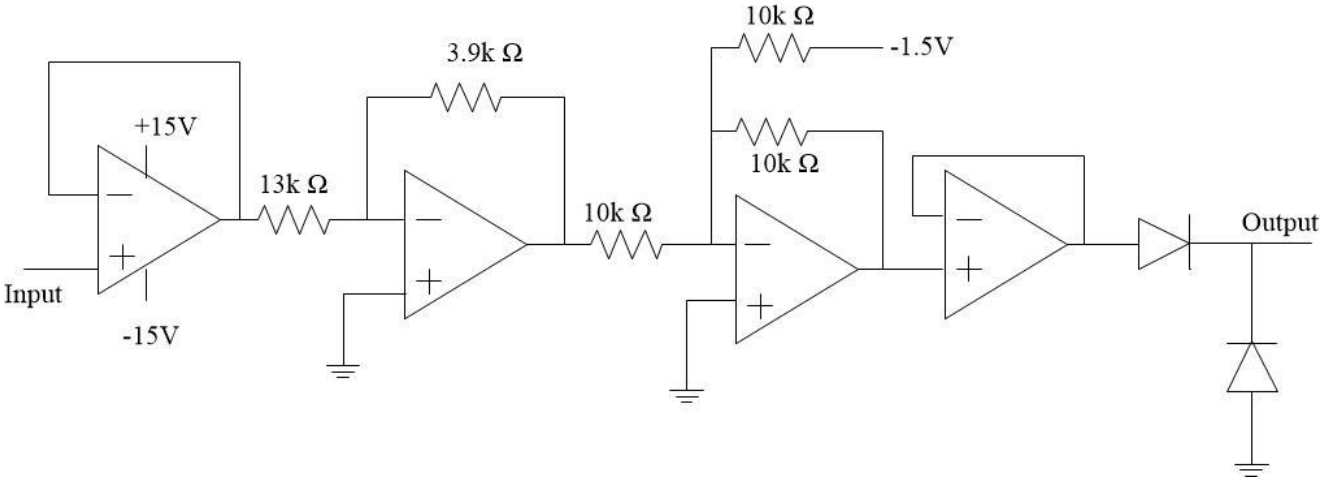

Fig.1 Signal conditioning ckt

Component Used:

For hardware we need 8 signal conditioning circuit

SR No.	Component	IC Name	Specification
1.	Op-Amp	TL064	Max Supply Voltage=36V, Tj=150^{0}C
2.	Voltage Regulator	LM337TS	Input-Output Voltage diff =40V(max), Tj= 40 to 150^{0}C
3.	Resistor	-	13k, 3.9k,10k
4.	Capacitor	-	0.1 micro fared (ceramic)
5.	Trimer Resister		20 Ohms 0.5W, 1/2W PC Pins Through Hole Trimmer Potentiometer Cermet 25 Turn Top Adjustment
6.	Diode	IN4004	Peak Reverse Repetitive Voltage =400V, Peak Forward Voltage=1V
7.	Zener Diode	IN4728	Voltage - Zener (Vz)=3.3V, Impedance=10ohm(max)

SIMULATION:

Software Used: LTspice

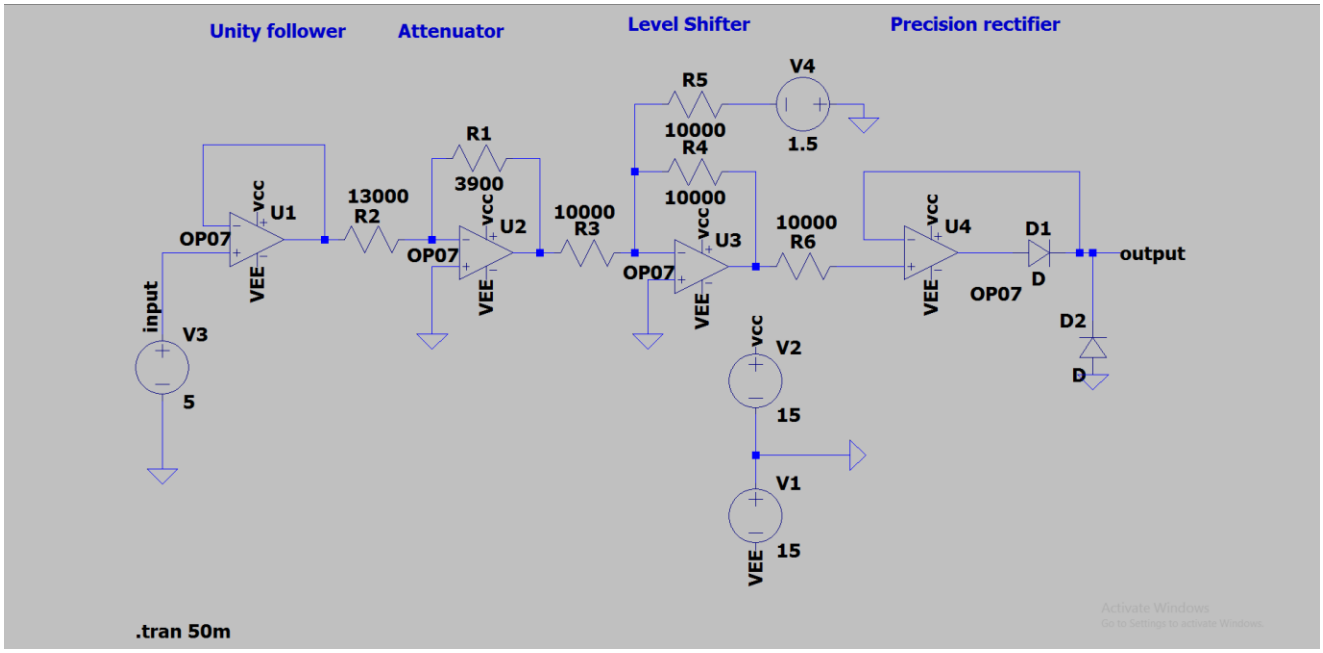

Fig.2 Simulation

Simulation result

1. **Output Voltage at different level**

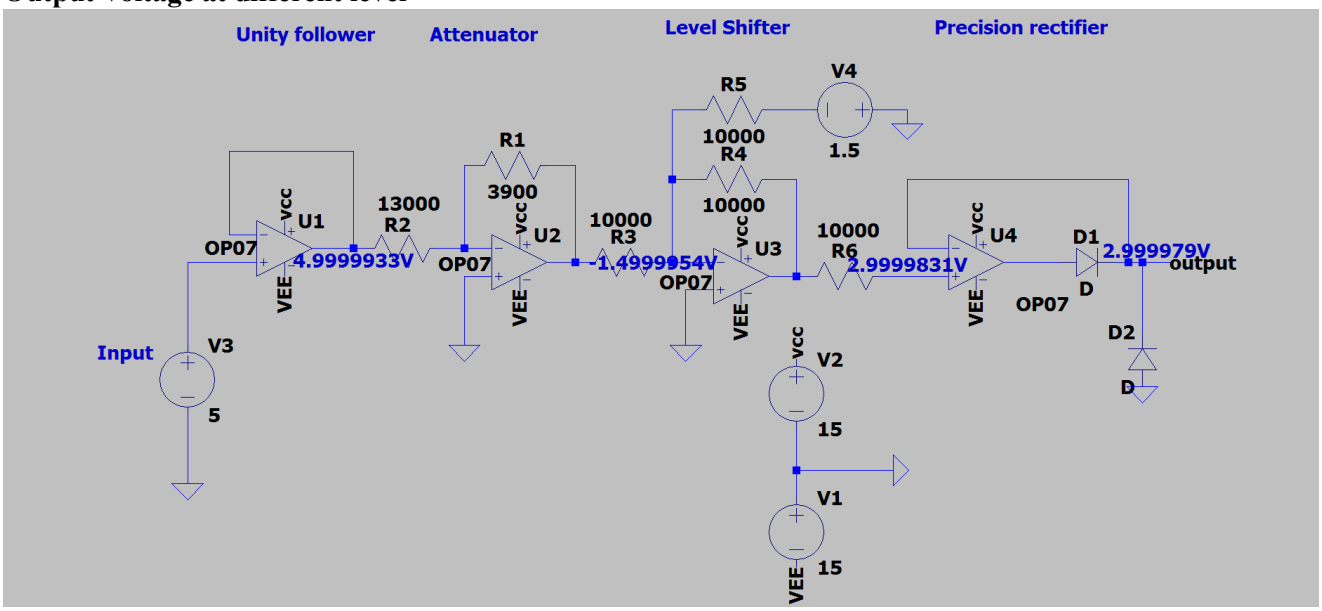

Fig.3 Simulation with output

2. **Output and Input voltage waveform**

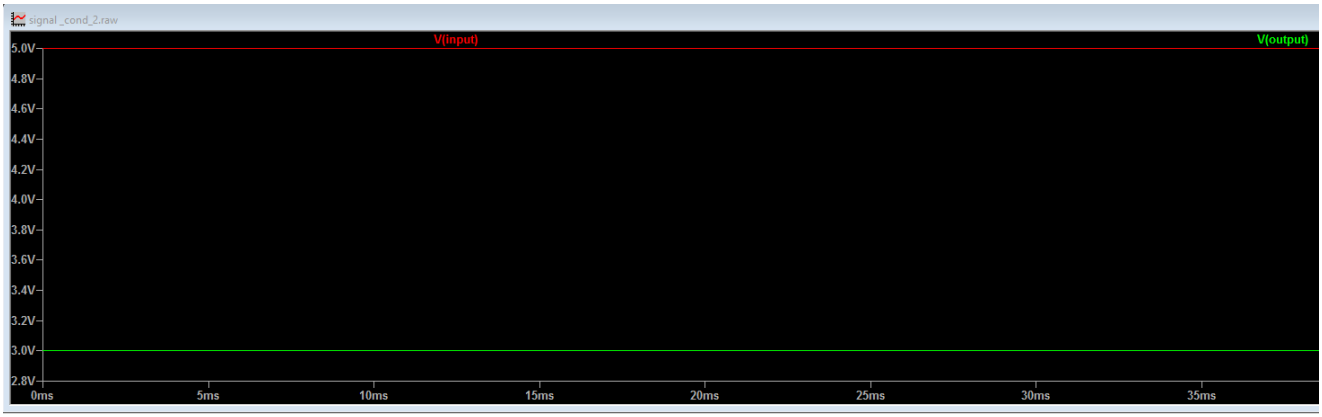

Fig.4. Output Voltage (green), Input Voltage (red)

PCB Design:

Software Used: Eagle

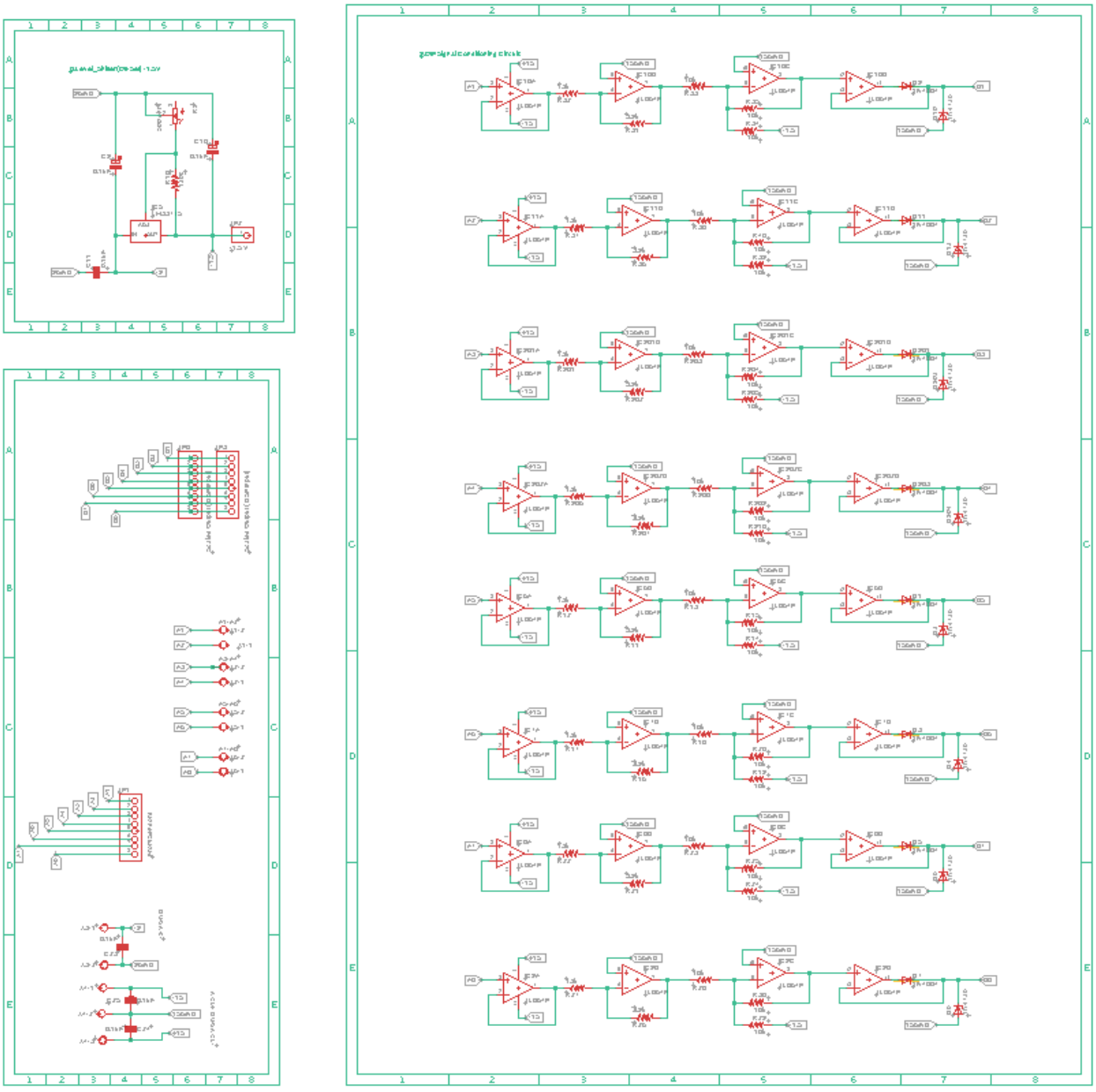

Fig.5. Schematic Diagram of signal conditioning circuit

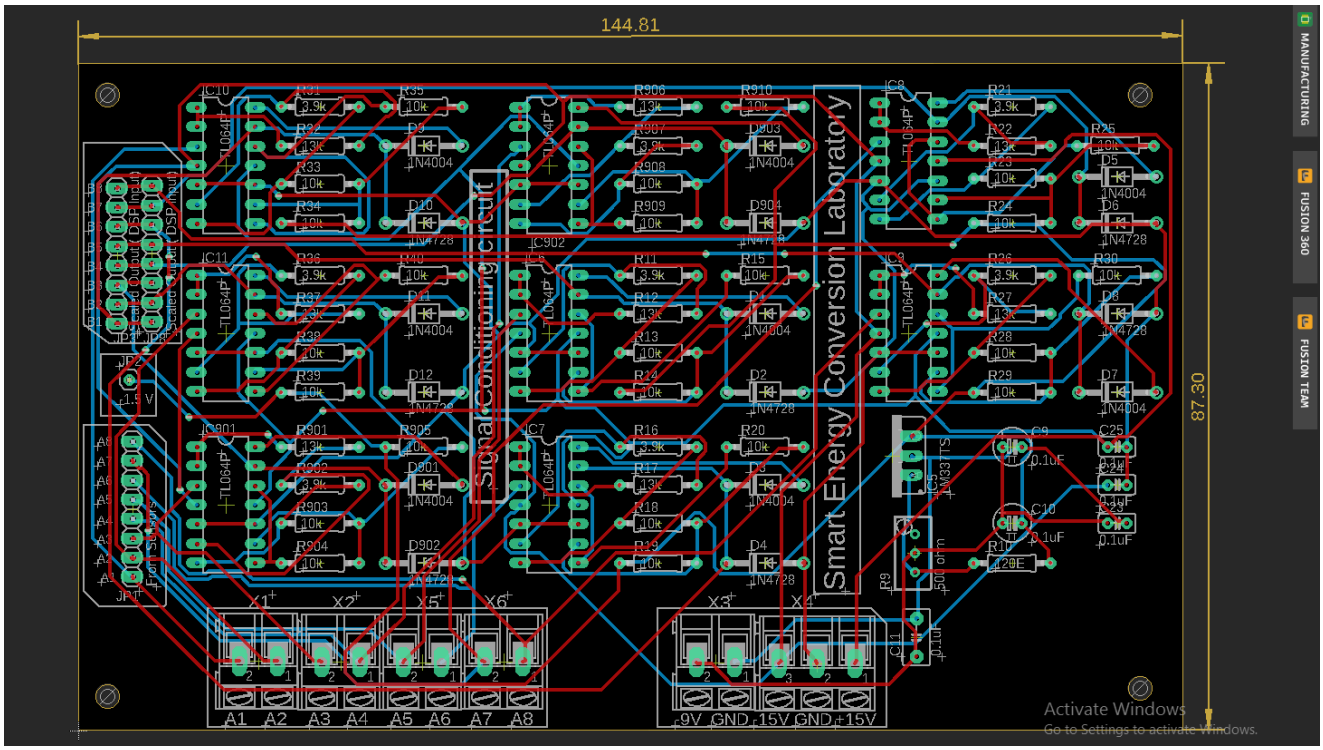

Fig.6. PCB Design of signal conditioning circuit

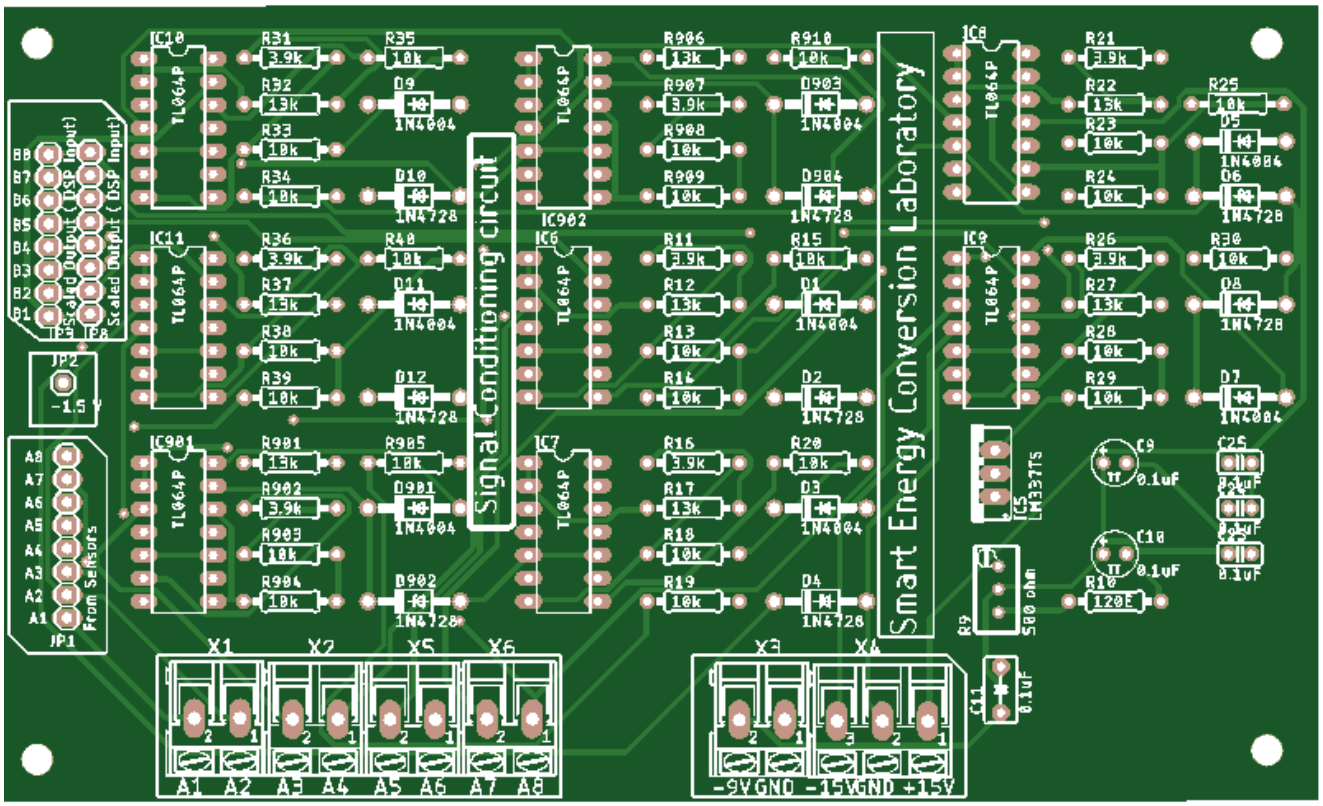

Fig.7. Gerber File (Top view)

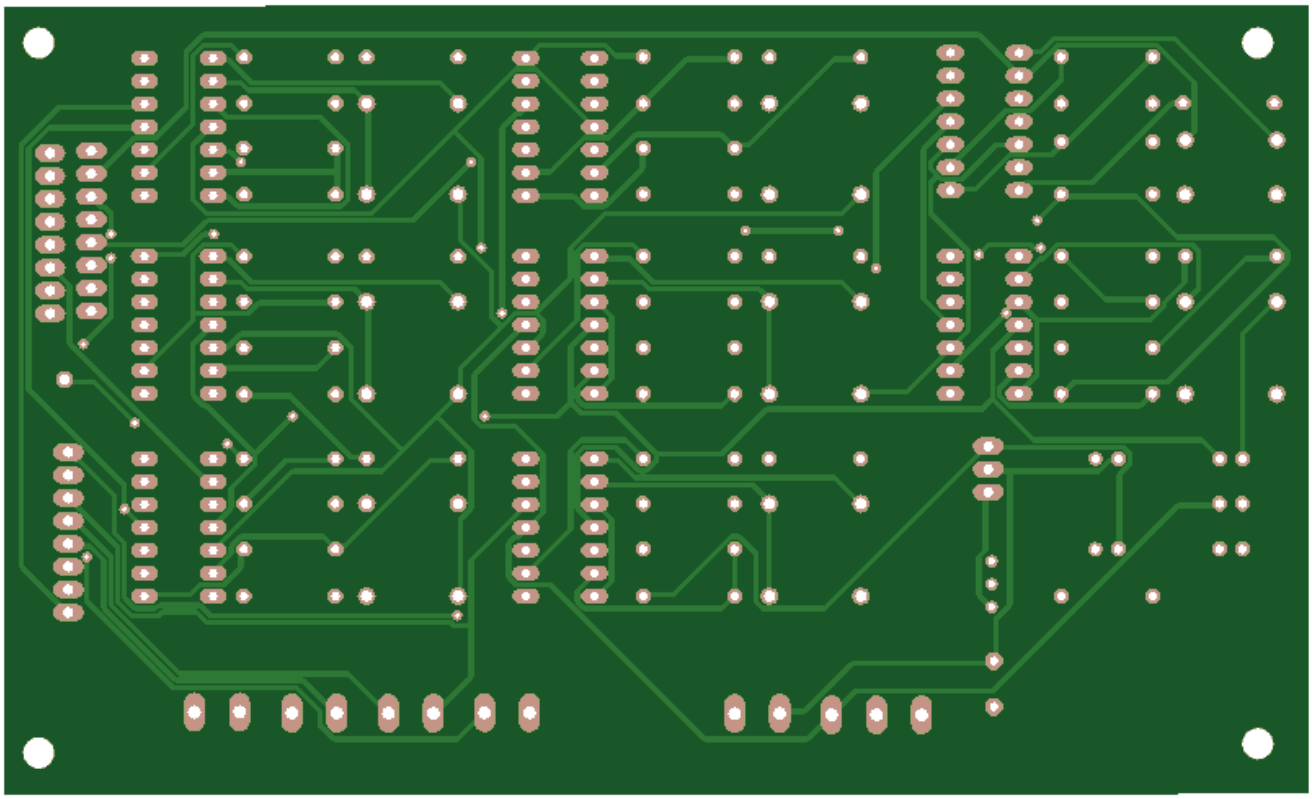

Fig.8 Gerber File (Bottom view)