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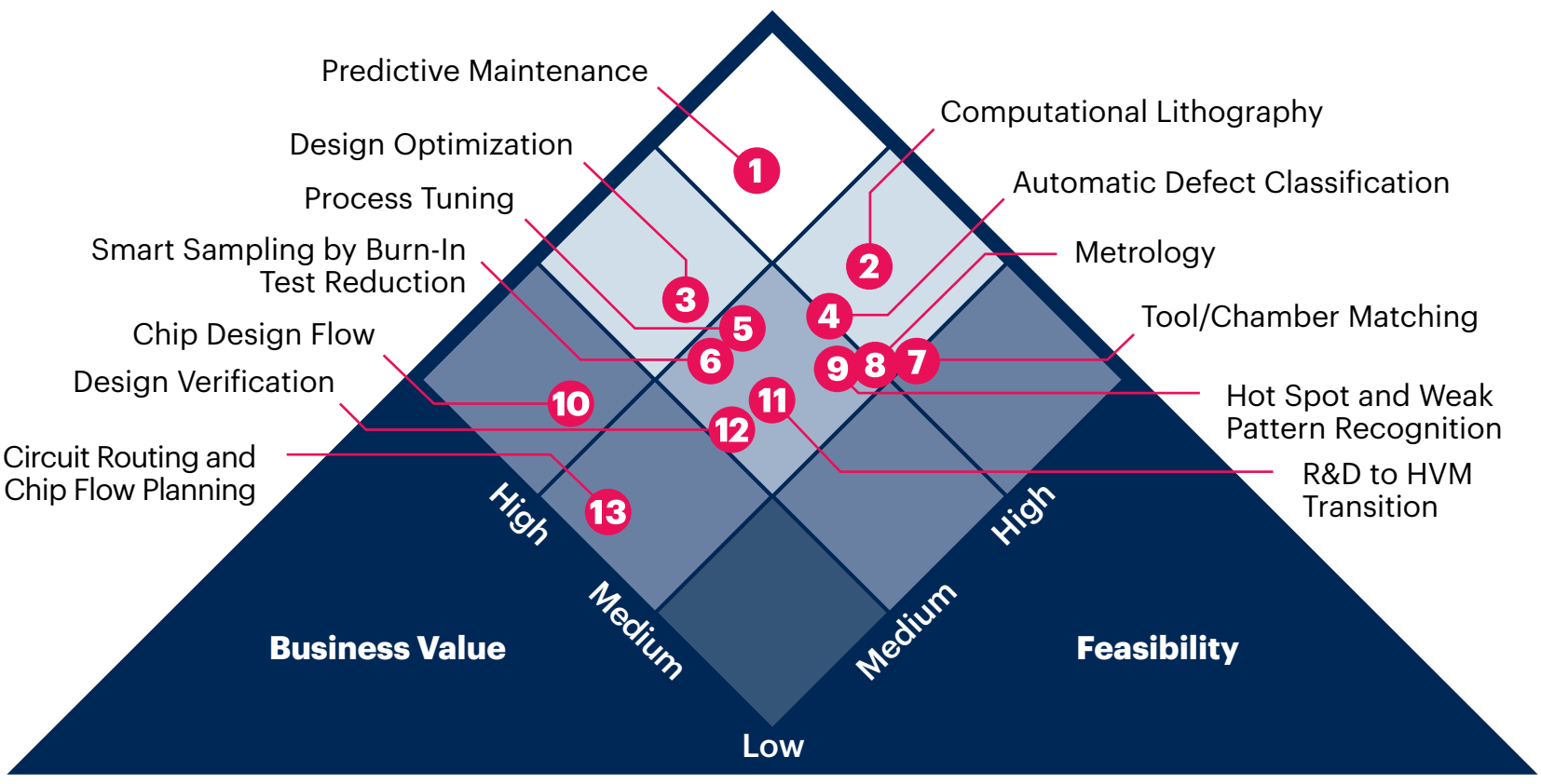
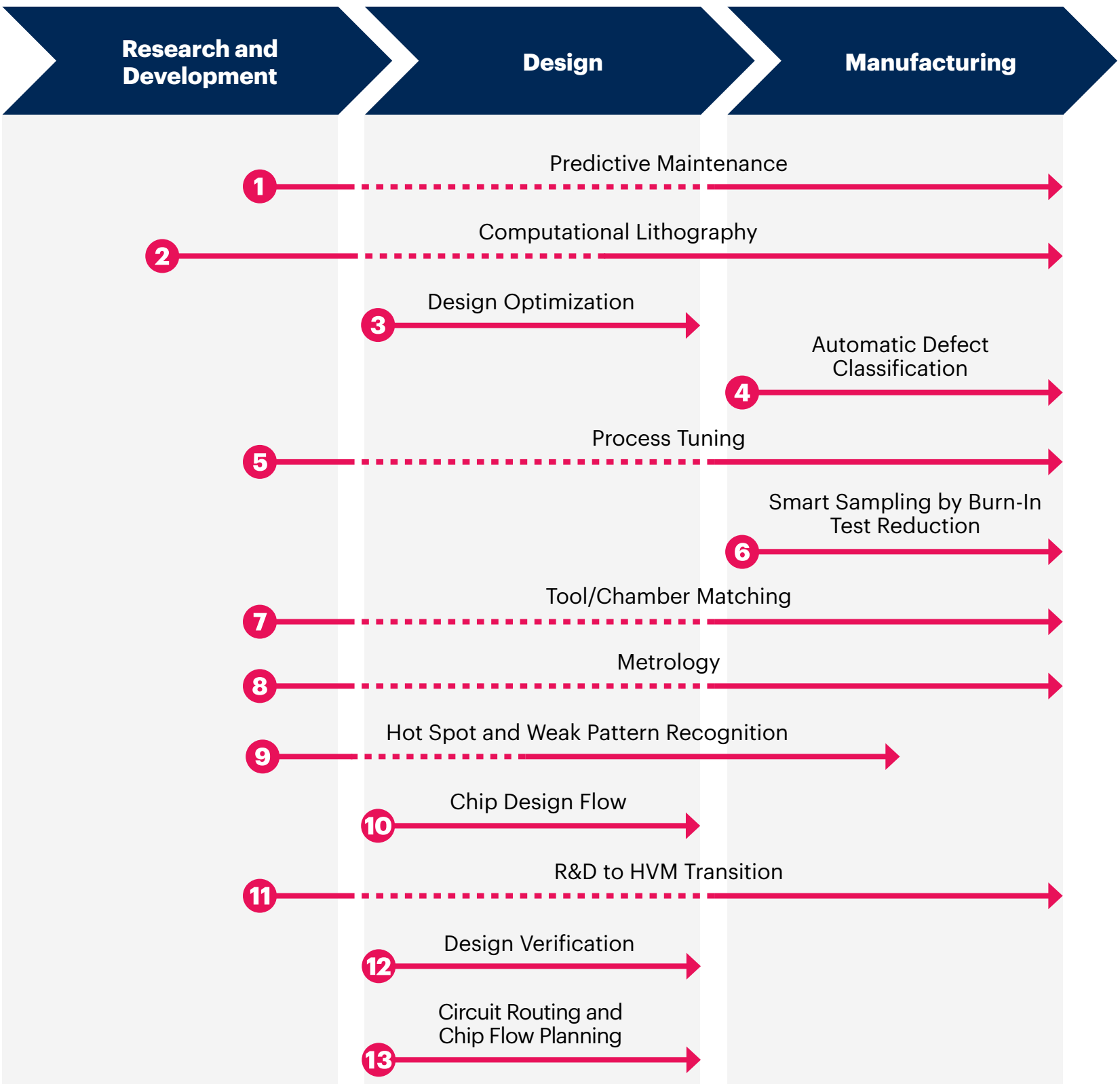
AI Use Case Prism for Chip Manufacturing and Design





Business case is intermittent and doesn't apply to the process spanning the dotted line

		Business Value				Feasibility	
		Cost Reduction[1]	Operational Efficiency[2]	Yield Improvement/ Quality[3]	Time to Market[4]	Technical Feasibility[5]	Organization Readiness[6]
1	Predictive Maintenance	●	●	◕	◑	●	◕
2	Computational Lithography	◑	◑	●	◕	●	◕
3	Design Optimization	◕	◕	●	◕	◕	◑
4	Automatic Defect Classification	◑	◕	◑	◑	●	◑
5	Process Tuning	◕	◕	◕	◕	◕	◑
6	Smart Sampling by Burn-In Test Reduction	◕	◕	◑	◕	◕	◑
7	Tool/Chamber Matching	◔	◑	◕	◔	●	◕
8	Metrology	◔	◕	◕	◔	◕	◕
9	Hot Spot and Weak Pattern Recognition	◑	◔	●	◑	◕	◕
10	Chip Design Flow	◕	●	◕	●	◔	◑
11	R&D to HVM Transition	◔	◕	◑	◕	◕	◑
12	Design Verification	◔	◕	◕	◕	◑	◑
13	Circuit Routing and Chip Flow Planning	◑	◕	◕	◕	◔	◔

[1] Includes reducing the overall costs from getting through the entire pipeline of chip design and manufacturing process.

[2] Improving efficiency of the entire process results in higher throughput, while maintaining standards/quality and reducing redundancy.

[3] Implies improving yield of the wafers, such that high percentage of fabricated chips perform at intended levels by reducing process and/or random defects

[4] Faster time to market implies how quickly products can be delivered to the customer, critical in technology sector to gain market share.

[5] Includes if available technologies are a good match for the complexity of the use cases, are available in the market and how mature they are.

[6] Includes stakeholder adoption issues, such as infrastructure, talent, management support, and cultural acceptance

○ None
◔ Low
◑ Medium
◕ High
● Very High

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