

EE 5319 Nanoelectric Device, Circuit, and System

Project 3

Physical Design

Name/Class ID	UTA ID	Contribution to the Project (%)
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1. Find the minimum core area which passes placement and routing without any errors.

The image shows the 'Specify Floorplan' dialog box in the Cadence Innovus environment. The 'Design Dimensions' tab is active, showing the 'Core Size by' section with 'Core Utilization' set to 0.892692 and 'Cell Utilization' set to 0.892692. The 'Dimension' section shows 'Width' and 'Height' both set to 49.4. The 'Core Margins by' section shows 'Core to IO Boundary' and 'Core to Die Boundary' both set to 4.94. The 'Die Size by' section shows 'Width' and 'Height' both set to 59.28. The 'Floorplan Origin at' is set to 'Lower Left Corner'. The 'Unit' is 'Micron'. The 'OK' button is highlighted.

The terminal window on the right shows the following output:

```
#CELL VIEW ictest,init has no DRC violation.
#Total number of DRC violations = 0
# number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1588.89 (MB), peak = 1695.69 (MB)
#CELL VIEW ictest,init has no DRC violation.
#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 6122 um.
#Total half perimeter of net bounding box = 5780 um.
#Total wire length on LAYER metal1 = 185 um.
#Total wire length on LAYER metal2 = 2566 um.
#Total wire length on LAYER metal3 = 2897 um.
#Total wire length on LAYER metal4 = 464 um.
#Total wire length on LAYER metal5 = 10 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3545
#Up-Via Summary (total 3545):
#-----
# metal1      1955
# metal2      1497
# metal3       91
# metal4        2
#-----
#              3545
```

The image shows the Cadence Innovus Implementation System 21.1.1 interface. The main window displays a floorplan layout with a grid of cells and various components. The 'Layout' tab is active. The 'Net' list on the left shows various nets and their connections. The 'Favorite' list on the right shows various objects and their status. The 'Instance' list on the right shows various instances and their status. The 'Module' list on the right shows various modules and their status. The 'Cell' list on the right shows various cells and their status. The 'Blockage' list on the right shows various blockages and their status. The 'Row' list on the right shows various rows and their status. The 'Floorplan' list on the right shows various floorplans and their status. The 'Partition' list on the right shows various partitions and their status. The 'Power' list on the right shows various power objects and their status. The 'Overlay' list on the right shows various overlays and their status. The 'Track' list on the right shows various tracks and their status. The 'Net' list on the right shows various nets and their status. The 'Route' list on the right shows various routes and their status. The 'Layer' list on the right shows various layers and their status. The 'Adaptive' list on the right shows various adaptive objects and their status. The 'Detail' list on the right shows various detail objects and their status. The 'Speed' list on the right shows various speed objects and their status. The 'Goto' list on the right shows various goto objects and their status. The status bar at the bottom shows '19.25350, 40.11900 Set: 0 Routed'.

DRC = 0 ; Errors = 0 after completion of routing.

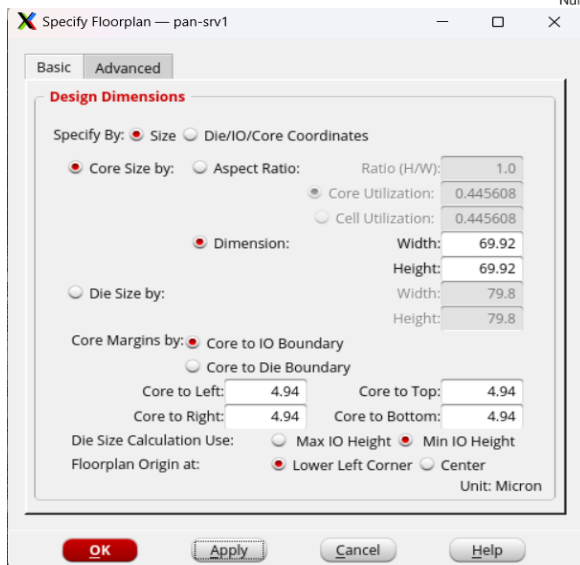
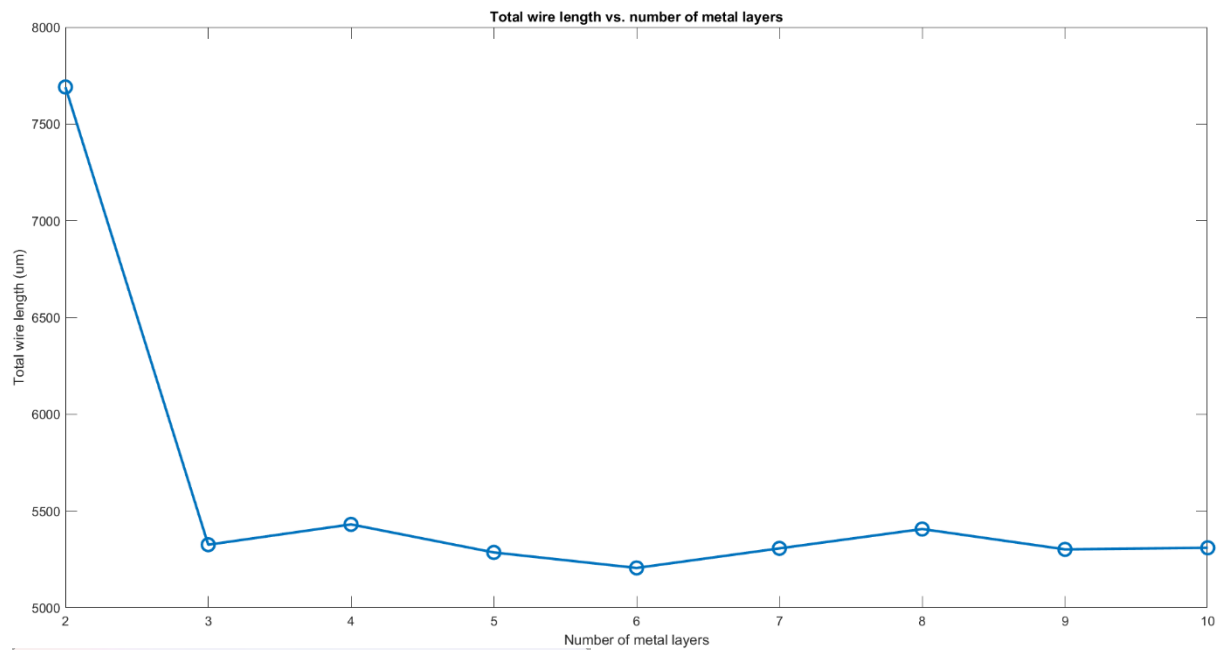
Minimum dimensions

Width = 49.4 um

Height = 49.4 um

Minimum core area = width * Height = 2440.36 um²

2. Fix the core area to 70×70 and investigate how the number of metal layers affects the total wire length and provide explanations. You may plot the total wire length vs. number of metal layers.



Metal layer	Total wire length(um)
2	7691
3	5326
4	5431
5	5286
6	5206
7	5307
8	5407
9	5302
10	5310

```
#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 5206 um.
#Total half perimeter of net bounding box = 4800 um.
#Total wire length on LAYER metal1 = 313 um.
#Total wire length on LAYER metal2 = 2819 um.
#Total wire length on LAYER metal3 = 2022 um.
#Total wire length on LAYER metal4 = 39 um.
#Total wire length on LAYER metal5 = 17 um.
#Total wire length on LAYER metal6 = 6 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3200
#Up-Via Summary (total 3200):
#
#-----
# metal1      1987
# metal2      1196
# metal3        13
# metal4         3
# metal5         1
#-----
#              3200
#
```

#ERROR (NRDB-164) The number of layers between bottom routing layer (1) and top routing layer (1) is less than 2. Nanoroute cannot route with less than two routing layers.

Hence we swept values of metal layers from 2-10

Key observation here is the maximum routing layer used was metal 6 even though we allowed until 10 metal layers , there was a drastic drop in the routing wire length when switched from metal 2 to metal 3
I.e., from 7691um to 5326um

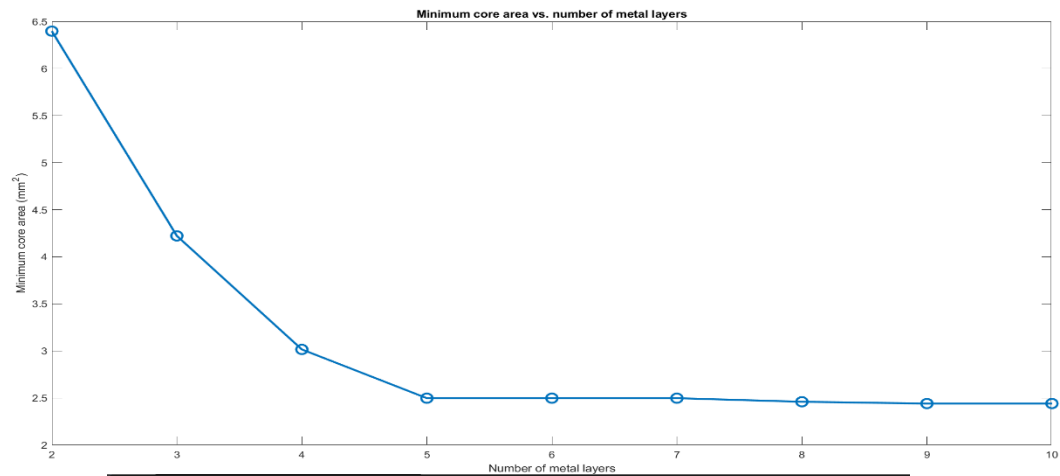
The Metal 6 gave us the minimum wire length of 5206um.

Conclusion:

As we go on routing vertically using higher metal layers there will be reduction of total wire length used, but this doesn't mean the wire length reduces as we keep on moving to higher metal layers at some point it will even increase this indicates there is optimum value for metal layer usage and wire length.

3. Vary the core area and investigate how the number of metal layers affects the minimum core area without DRC violations (i.e. when you see white cross on the layout, it means violation and the core area is too small and cannot route all interconnects). For example, you may first find what is the minimum core area when only using 2 metal layers, then find what is the minimum core area when increasing metal layers to 3, and then to 4, 5, and etc. At the end, you should be able to plot the minimum core area vs. number of metal layers and see if you can observe any trend and provide possible explanations for such a trend.

Metal layer	Minimum core area(mm ²)
2	6.398
3	4.222
4	3.015
5	2.497
6	2.497
7	2.497
8	2.459
9	2.440
10	2.440



```
#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 7972 um.
#Total half perimeter of net bounding box = 5399 um.
#Total wire length on LAYER metal1 = 2412 um.
#Total wire length on LAYER metal2 = 5559 um.
#Total wire length on LAYER metal3 = 0 um.
#Total wire length on LAYER metal4 = 0 um.
#Total wire length on LAYER metal5 = 0 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3276
#Up-Via Summary (total 3276):
#
#-----
# metal1      3244
# metal2       24
# metal3        4
# metal4        4
#-----
#              3276
```

Specify Floorplan — pan-srv1

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☐ Aspect Ratio: Ratio (H/W): 1.0

☐ Core Utilization: 0.340474

☐ Cell Utilization: 0.340474

☒ Dimension: Width: 79.99 Height: 79.99

☐ Die Size by: Width: 89.87 Height: 89.87

Core Margins by: ☒ Core to IO Boundary ☐ Core to Die Boundary

Core to Left: 4.94 Core to Top: 4.94

Core to Right: 4.94 Core to Bottom: 4.94

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

Unit: Micron

OK Apply Cancel Help

```

#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 5186 um.
#Total half perimeter of net bounding box = 4698 um.
#Total wire length on LAYER metal1 = 299 um.
#Total wire length on LAYER metal2 = 2848 um.
#Total wire length on LAYER metal3 = 2039 um.
#Total wire length on LAYER metal4 = 0 um.
#Total wire length on LAYER metal5 = 0 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3212
#Up-Via Summary (total 3212):
#
#-----
# metal1          1975
# metal2          1227
# metal3           5
# metal4           5
#-----
#                  3212
#
#detailRoute Statistics:
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = -0.32 (MB)
#Total memory = 1320.94 (MB)
#Peak memory = 1500.03 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 2.49 (MB)
#Total memory = 1316.96 (MB)
#Peak memory = 1500.03 (MB)
#Number of warnings = 0
#Total number of warnings = 23
#Number of fails = 0
#Total number of fails = 0

```

Specify Floorplan — pan-srv1

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☐ Aspect Ratio: Ratio (H/W):

☐ Core Utilization:

☐ Cell Utilization:

☒ Dimension: Width:

Height:

☐ Die Size by: Width:

Height:

Core Margins by: ☒ Core to IO Boundary

☐ Core to Die Boundary

Core to Left: Core to Top:

Core to Right: Core to Bottom:

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

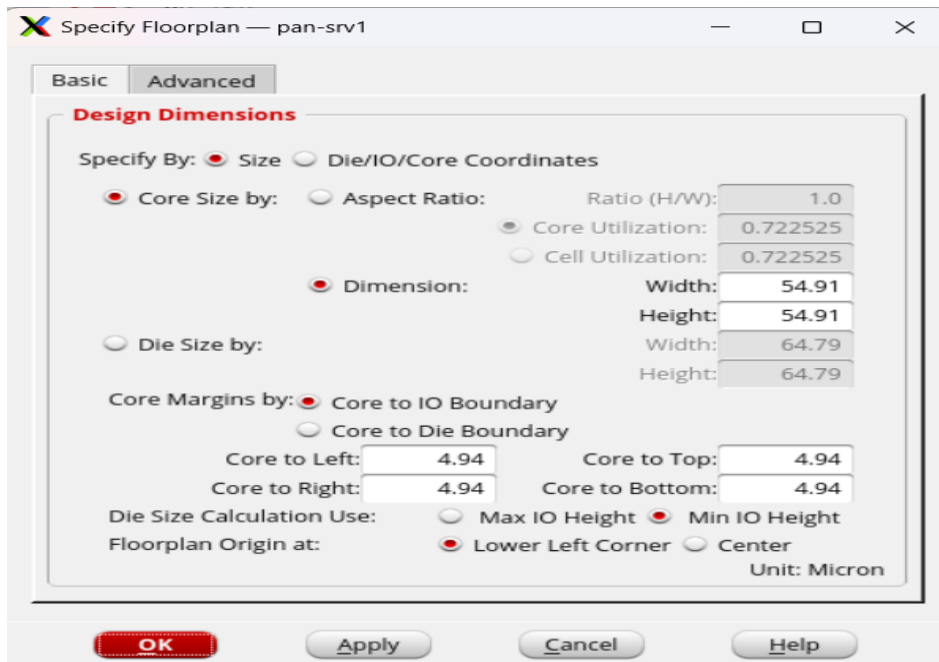
Floorplan Origin at: ☒ Lower Left Corner ☐ Center

Unit: Micron

OK Apply Cancel Help

m4

```
#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 4957 um.
#Total half perimeter of net bounding box = 4612 um.
#Total wire length on LAYER metal1 = 216 um.
#Total wire length on LAYER metal2 = 2597 um.
#Total wire length on LAYER metal3 = 2081 um.
#Total wire length on LAYER metal4 = 62 um.
#Total wire length on LAYER metal5 = 0 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3280
#Up-Via Summary (total 3280):
#
#-----
# metal1          1971
# metal2          1278
# metal3           27
# metal4           4
#-----
#                  3280
#
#detailRoute Statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = -0.17 (MB)
#Total memory = 1390.44 (MB)
#Peak memory = 1500.03 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 2.49 (MB)
#Total memory = 1387.06 (MB)
#Peak memory = 1500.03 (MB)
#Number of warnings = 0
#Total number of warnings = 32
#Number of fails = 0
#Total number of fails = 0
```



m5

```

#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 6262 um.
#Total half perimeter of net bounding box = 5854 um.
#Total wire length on LAYER metal1 = 162 um.
#Total wire length on LAYER metal2 = 2653 um.
#Total wire length on LAYER metal3 = 3061 um.
#Total wire length on LAYER metal4 = 350 um.
#Total wire length on LAYER metal5 = 37 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3555
#Up-Via Summary (total 3555):
#
#-----
# metal1          1960
# metal2          1460
# metal3           130
# metal4            3
# metal5            1
# metal6            1
#-----
#                  3555
#
#detailRoute Statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 0.57 (MB)
#Total memory = 1201.34 (MB)
#Peak memory = 1280.52 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 4.31 (MB)
#Total memory = 1197.64 (MB)
#Peak memory = 1280.52 (MB)
#Number of warnings = 1

```

Specify Floorplan — pan-srv1

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☐ Aspect Ratio: Ratio (H/W): 1.0

☐ Core Utilization: 0.872443

☐ Cell Utilization: 0.872443

☒ Dimension: Width: 49.97

Height: 49.97

☐ Die Size by: Width: 59.85

Height: 59.85

Core Margins by: ☒ Core to IO Boundary

☐ Core to Die Boundary

Core to Left: 4.94 Core to Top: 4.94

Core to Right: 4.94 Core to Bottom: 4.94

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

Unit: Micron

OK Apply Cancel Help


```

#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 5642 um.
#Total half perimeter of net bounding box = 5335 um.
#Total wire length on LAYER metal1 = 174 um.
#Total wire length on LAYER metal2 = 2551 um.
#Total wire length on LAYER metal3 = 2679 um.
#Total wire length on LAYER metal4 = 225 um.
#Total wire length on LAYER metal5 = 14 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3571
#Up-Via Summary (total 3571):
#
#-----
# metal1          1960
# metal2          1543
# metal3           66
# metal4           2
#-----
#              3571
#
#detailRoute Statistics:
#Cpu time = 00:00:03
#Elapsed time = 00:00:03
#Increased memory = 5.93 (MB)
#Total memory = 1368.20 (MB)
#Peak memory = 1483.38 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:03
#Elapsed time = 00:00:03
#Increased memory = 8.59 (MB)
#Total memory = 1363.68 (MB)
#Peak memory = 1483.38 (MB)
#Number of warnings = 1
#Total number of warnings = 23
#Number of fails = 0
#Total number of fails = 0

```

Specify Floorplan — pan-srv1

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☐ Aspect Ratio: Ratio (H/W): 1.0

☐ Core Utilization: 0.872443

☐ Cell Utilization: 0.872443

☒ Dimension: Width: 49.97

Height: 49.97

☐ Die Size by: Width: 59.85

Height: 59.85

Core Margins by: ☒ Core to IO Boundary

☐ Core to Die Boundary

Core to Left: 4.94 Core to Top: 4.94

Core to Right: 4.94 Core to Bottom: 4.94

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

Unit: Micron

OK Apply Cancel Help

```

#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 6288 um.
#Total half perimeter of net bounding box = 5854 um.
#Total wire length on LAYER metal1 = 169 um.
#Total wire length on LAYER metal2 = 2810 um.
#Total wire length on LAYER metal3 = 2945 um.
#Total wire length on LAYER metal4 = 346 um.
#Total wire length on LAYER metal5 = 16 um.
#Total wire length on LAYER metal6 = 1 um.
#Total wire length on LAYER metal7 = 1 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3600
#Up-Via Summary (total 3600):
#
#-----
# metal1          1968
# metal2          1522
# metal3           104
# metal4           4
# metal5           1
# metal6           1
#-----
#                    3600
#
#detailRoute Statistics:
#Cpu time = 00:00:03
#Elapsed time = 00:00:03
#Increased memory = 5.25 (MB)
#Total memory = 1470.73 (MB)
#Peak memory = 1580.14 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:03
#Elapsed time = 00:00:03
#Increased memory = 9.48 (MB)
#Total memory = 1467.19 (MB)
#Peak memory = 1580.14 (MB)
#Number of warnings = 1

```

M8

Specify Floorplan — pan-srv1

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☐ Aspect Ratio: Ratio (H/W): 1.0

☐ Core Utilization: 0.885865

☐ Cell Utilization: 0.885865

☒ Dimension: Width: 49.59

Height: 49.59

☐ Die Size by: Width: 59.47

Height: 59.47

Core Margins by: ☒ Core to IO Boundary

☐ Core to Die Boundary

Core to Left: 4.94 Core to Top: 4.94

Core to Right: 4.94 Core to Bottom: 4.94

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

Unit: Micron

OK Apply Cancel Help

```

#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 5723 um.
#Total half perimeter of net bounding box = 5360 um.
#Total wire length on LAYER metal1 = 166 um.
#Total wire length on LAYER metal2 = 2650 um.
#Total wire length on LAYER metal3 = 2590 um.
#Total wire length on LAYER metal4 = 281 um.
#Total wire length on LAYER metal5 = 27 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 9 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3487
#Up-Via Summary (total 3487):
#
#-----
# metal1      1955
# metal2      1432
# metal3       93
# metal4        5
# metal5        1
# metal6        1
#-----
#              3487
#
#detailRoute Statistics:
#Cpu time = 00:00:02
#Elapsed time = 00:00:02
#Increased memory = 3.18 (MB)
#Total memory = 1513.76 (MB)
#Peak memory = 1645.25 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:03
#Elapsed time = 00:00:03
#Increased memory = 7.42 (MB)
#Total memory = 1509.84 (MB)
#Peak memory = 1645.25 (MB)
#Number of warnings = 1

```

M9

Specify Floorplan — pan-srv1

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☐ Aspect Ratio: Ratio (H/W): 1.0

☒ Core Utilization: 0.892692

☐ Cell Utilization: 0.892692

☒ Dimension: Width: 49.4 Height: 49.4

☐ Die Size by: Width: 59.28 Height: 59.28

Core Margins by: ☒ Core to IO Boundary ☐ Core to Die Boundary

Core to Left: 4.94 Core to Top: 4.94

Core to Right: 4.94 Core to Bottom: 4.94

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

Unit: Micron

OK Apply Cancel Help

```

#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 5872 um.
#Total half perimeter of net bounding box = 5522 um.
#Total wire length on LAYER metal1 = 185 um.
#Total wire length on LAYER metal2 = 2601 um.
#Total wire length on LAYER metal3 = 2646 um.
#Total wire length on LAYER metal4 = 423 um.
#Total wire length on LAYER metal5 = 18 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3507
#Up-Via Summary (total 3507):
#
#-----
# metal1          1964
# metal2          1426
# metal3           114
# metal4           3
#-----
#                  3507
#

```

M10

```

#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 5659 um.
#Total half perimeter of net bounding box = 5325 um.
#Total wire length on LAYER metal1 = 173 um.
#Total wire length on LAYER metal2 = 2621 um.
#Total wire length on LAYER metal3 = 2599 um.
#Total wire length on LAYER metal4 = 252 um.
#Total wire length on LAYER metal5 = 13 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3504
#Up-Via Summary (total 3504):
#
#-----
# metal1          1970
# metal2          1446
# metal3           85
# metal4           3
#-----
#                  3504
#

```

Specify Floorplan — pan-srv1

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☐ Aspect Ratio: Ratio (H/W): 1.0

☒ Core Utilization: 0.892692

☐ Cell Utilization: 0.892692

☒ Dimension: Width: 49.4 Height: 49.4

☐ Die Size by: Width: 59.28 Height: 59.28

Core Margins by: ☒ Core to IO Boundary ☐ Core to Die Boundary

Core to Left: 4.94 Core to Top: 4.94

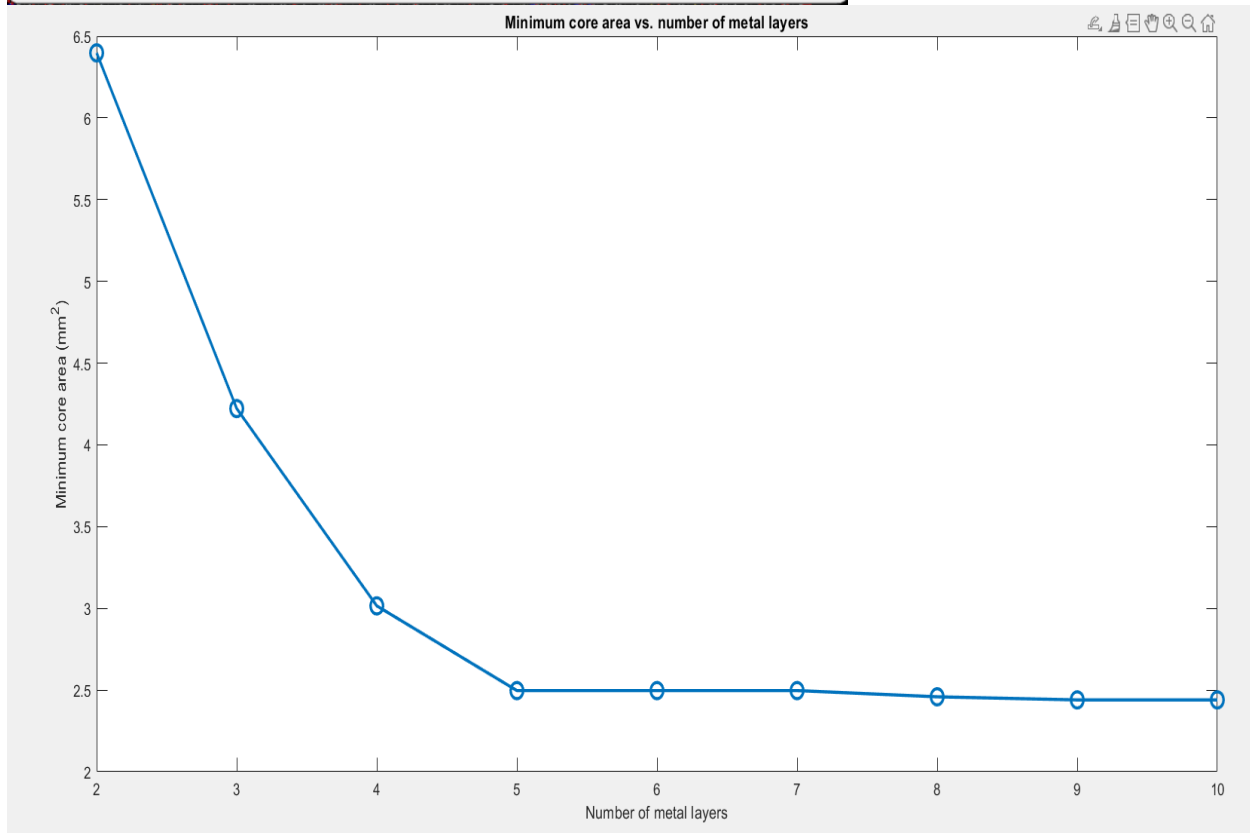
Core to Right: 4.94 Core to Bottom: 4.94

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

Unit: Micron

OK Apply Cancel Help



```
#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 7972 um.
#Total half perimeter of net bounding box = 5399 um.
#Total wire length on LAYER metal1 = 2412 um.
#Total wire length on LAYER metal2 = 5559 um.
#Total wire length on LAYER metal3 = 0 um.
#Total wire length on LAYER metal4 = 0 um.
#Total wire length on LAYER metal5 = 0 um.
#Total wire length on LAYER metal6 = 0 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 3276
#Up-Via Summary (total 3276):
#
#-----
# metal1          3244
# metal2           24
# metal3            4
# metal4            4
#-----
#                  3276
#
#detailRoute Statistics:
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 0.12 (MB)
#Total memory = 1278.71 (MB)
#Peak memory = 1403.29 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 3.51 (MB)
#Total memory = 1275.45 (MB)
#Peak memory = 1403.29 (MB)
#Number of warnings = 0
#Total number of warnings = 17
#Number of fails = 0
#Total number of fails = 0
```