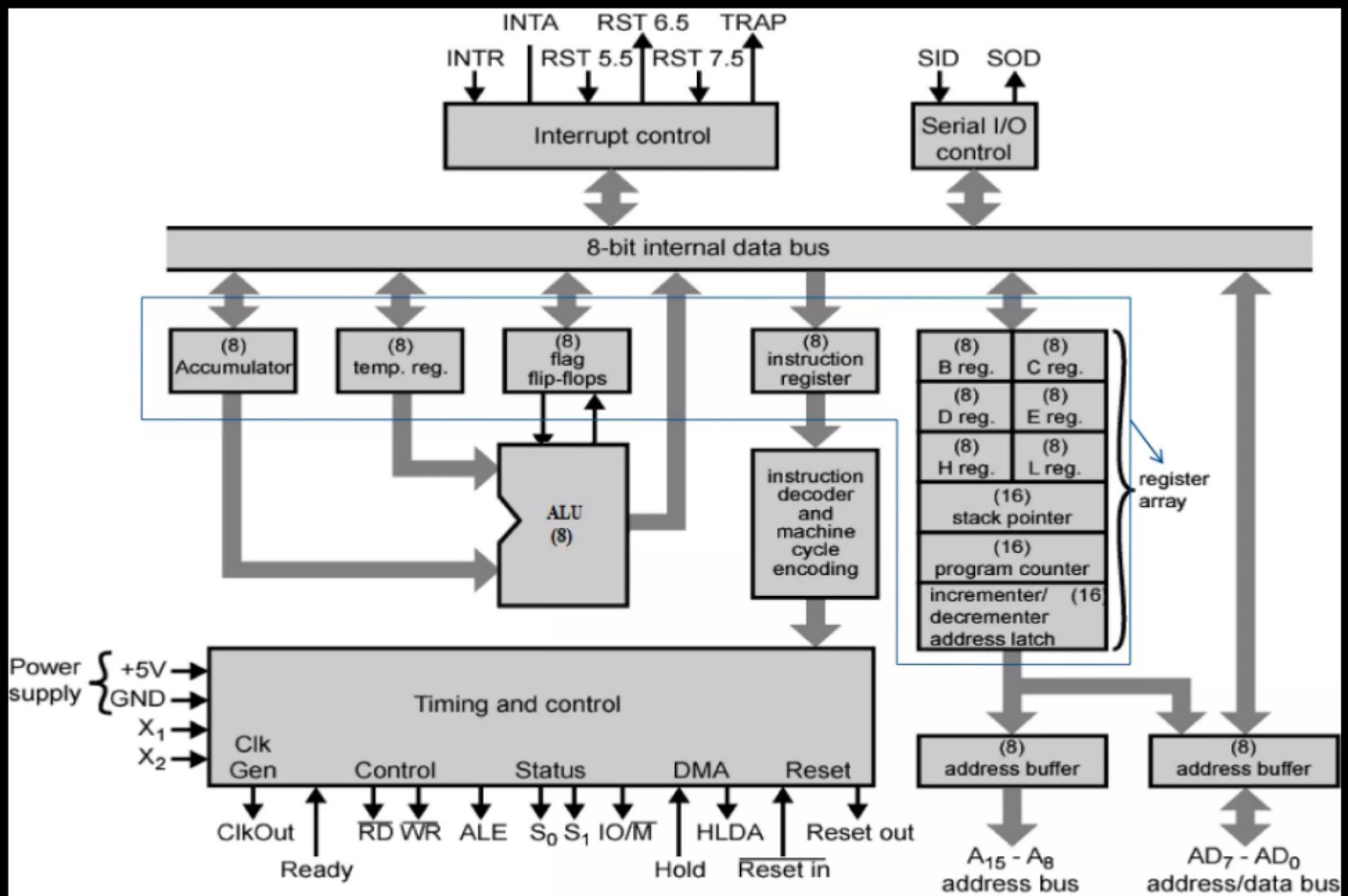


Chapter 2

Microprocessor Architecture & Pin diagram

Features of Microprocessor- 8085

- ✓ 8085 is developed by INTEL
- ✓ 8 bit microprocessor: can accept 8 bit data simultaneously
- ✓ Operates on single +5V D.C. supply.
- ✓ Designed using NMOS technology
- ✓ 6200 transistor on single chip
- ✓ It provides on chip clock generator, hence it does not require external clock generator.
- ✓ Operates on 3MHz clock frequency.
- ✓ 8bit multiplexed address/data bus, which reduce the number of pins.
- ✓ 16address lines, hence it can address $2^{16} = 64$ K bytes of memory
- ✓ It generates 8 bit I/O addresses, hence it can access $2^8 = 256$ I/O ports.
- ✓ 5 hardware interrupts i.e. TRAP, RST6.5, RST5.5, RST4.5, and INTR
- ✓ It provides DMA.



Internal Architecture (functional block diagram) of 8085

8085 Architecture.....cont...

8085 architecture consists of following blocks:

1. Register Array
2. ALU & Logical Group
3. Instruction decoder and machine cycle encoder, Timing and control circuitry
4. Interrupt control Group
5. Serial I/O control Group

8085 Architecture cont....

1. Registers Array : 14 register out of which 12 are 8 bit capacity and 2 of 16 bit. Classify into 4 types

(a) General purpose register: (user accessible)

- B,C,D,E,H,L are 8 bit register.(can be used singly)
- Can also be used for 16-bit register pairs- BC, DE & HL.
- Used to store the intermediate data and result
- H & L can be used as a data pointer(holds memory address)

(b) Special Purpose Register[A, Instruction Register and Flag]

(b.1) Accumulator (A): (user accessible)

- 8 bit register
- All the ALU operations are performed with reference to the contents of Accumulator.
- Result of an operation is stored in A.
- Store 8 bit data during I/O transfer

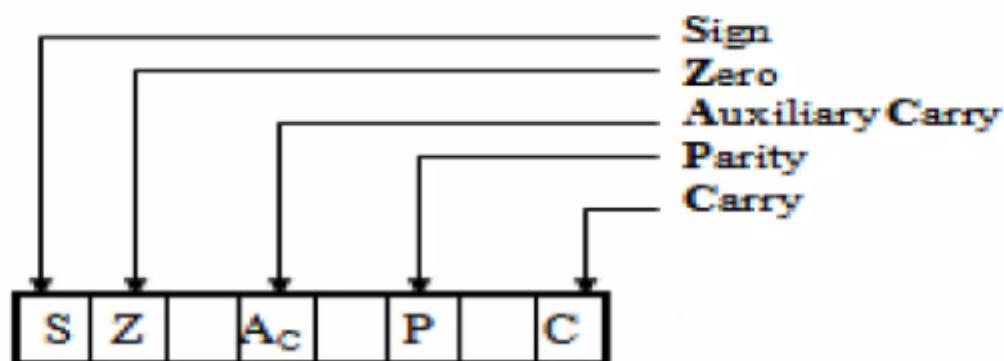
(b.2) Instruction Register: (user not accessible)

- When an instruction is fetched from memory, it is loaded in IR. Then transferred to the decoder for decoding.
- It is not programmable and can not be accessed through any instruction.

8085 Architecture cont....

(b.3) Flag Register(F): (user accessible)

- 8 bit Register
- Indicates the status of the ALU operation.
- ALU includes 5 flip flop, which are set or reset after an operation according to data conditions of the result in the accumulator.



(Flag Register)

Flag Register..... cont....

| Flag | Significance |
|----------------------|---|
| C or CY (Carry) | CY is set when an arithmetic operation generates a carry out, otherwise it is 0 (reset) |
| P (Parity) | $P = 1$; if the result of an ALU operation has an even number of 1's in A; $P = 0$; if number of 1 is odd. |
| AC (Auxiliary carry) | Similar to CY, AC= 1 if there is a carry from D ₃ to D ₄ Bit AC= 0 if there is a no carry from D ₃ to D ₄ Bit (not available for user) |
| Z(zero) | Z = 1; if result in A is 00H 0 otherwise |
| S(Sign) | S=1 if D ₇ bit of the A is 1(indicate the result is -ive) S= 0 if D ₇ bit of the A is 0(indicate the result is +ive) |

8085 Architecture cont....

(c) Temporary Register[W, Z, Temporary data register]

- Internally used by the MP(user not accessible)

(c.1) W and Z register:

- 8 bit capacity
- Used to hold temporary addresses during the execution of some instructions

(c.2) Temporary data register:

- 8 bit capacity
- Used to hold temporary data during ALU operations.

8085 Architecture cont....

(d) Pointer Register or special purpose [SP, PC]

(d.1) Stack Pointer(SP)

- 16 bit address which holds the address of the data present at the top of the stack memory
- It is a reserved area of the memory in the RAM to store and retrieve the temporary information.
- Also hold the content of PC when subroutines are used.
- When there is a subroutine call or on an interrupt. ie. pushing the return address on a jump, and retrieving it after the operation is complete to come back to its original location.

(d.3) Program Counter(PC)

- 16 bit address used for the execution of program
- Contain the address of the next instruction to be executed after fetching the instruction it is automatically incremented by 1.
- Not much use in programming, but as an indicator to user only.

8085 Architecture cont....

In addition to register MP contains some latches and buffer

- ✓ **Increment and decrement address latch**
 - 16 bit register
 - Used to increment or decrement the content of PC and SP
- ✓ **Address buffer**
 - 8 bit unidirectional buffer
 - Used to drive high order address bus(A8 to A15)
 - When it is not used under such as reset, hold and halt etc this buffer is used tristate high order address bus.
- ✓ **Data/Address buffer**
 - 8 bit bi-Directional buffer
 - Used to drive the low order address (A₀ to A₇) and data (D₀ to D₇) bus.
 - Under certain conditions such as reset, hold and halt etc this buffer is used tristate low order address bus.

8085 Architecture cont....

(2) ALU & Logical Group: it consists ALU, Accumulator, Temporary register and Flag Register.

(a) ALU

- Performs arithmetic and logical operations
- Stores result of arithmetic and logical operations in accumulator

(b) Accumulator

- General purpose register
- Stores one of the operand before any arithmetic and logical operations and result of operation is again stored back in Accumulator
- Store 8 bit data during I/O transfer

8085 Architecture cont....

(2) ALU & Logical Group.....cont.....

(c) Temporary Register

- 8 bit register
- During the arithmetic and logical operations one operand is available in A and other operand is always transferred to temporary register

For Eg.: ADD B – content of B is transferred into temporary register before actual addition

(d) Flag Register

- Five flag is connected to ALU
- After the ALU operation is performed the status of result will be stored in five flags.

8085 Architecture cont....

(3) Instruction decoder and machine cycle encoder, Timing and control circuitry

(a) Instruction decoder and machine cycle encoder :

- Decodes the op-code stored in the Instruction Register (IR) and establishes the sequence of events to follow.
- Encodes it and transfer to the timing & control unit to perform the execution of the instruction.

(b) Timing and control circuitry

- works as the brain of the CPU
- For proper sequence and synchronization of all the operations of MP, this unit generates all the timing and control signals necessary for communication between microprocessor and peripherals.

8085 Architecture cont....

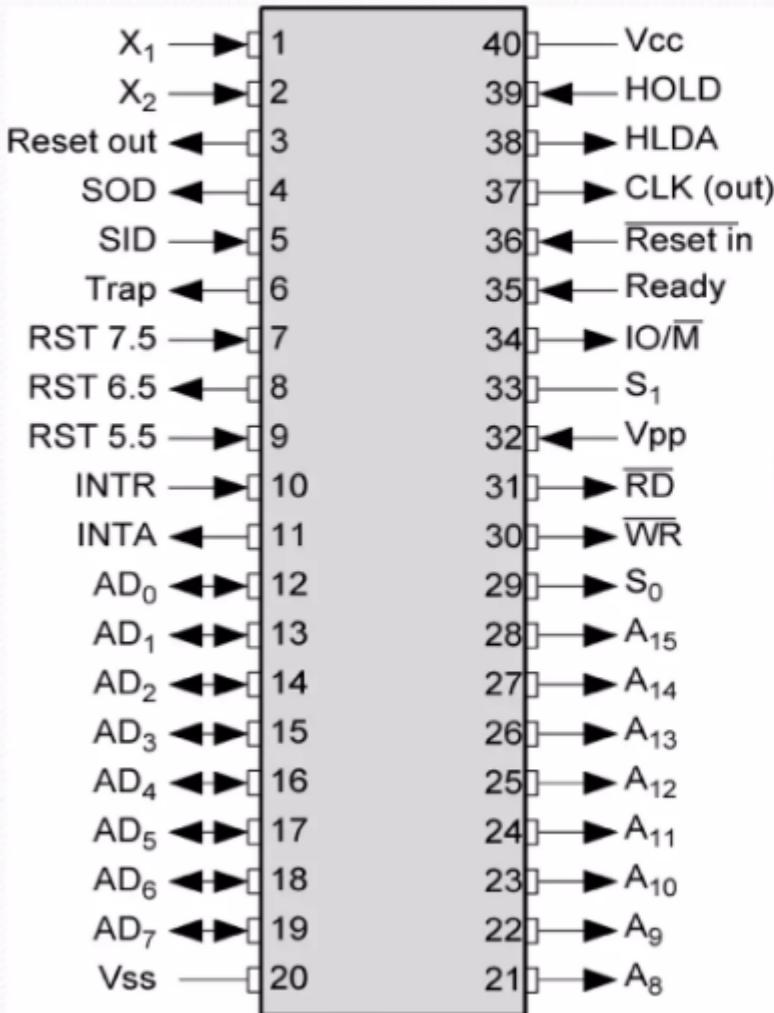
(4) Interrupt Control group

- **Interrupt:-** Occurrence of an external disturbance
- After servicing the interrupt, 8085 resumes its normal working sequence
- Transfer the control to special routines
- Five interrupts: - TRAP, RST_{7.5}, RST_{6.5}, RST_{5.5}, INTR
- In response to INTR, it generates INTA signal

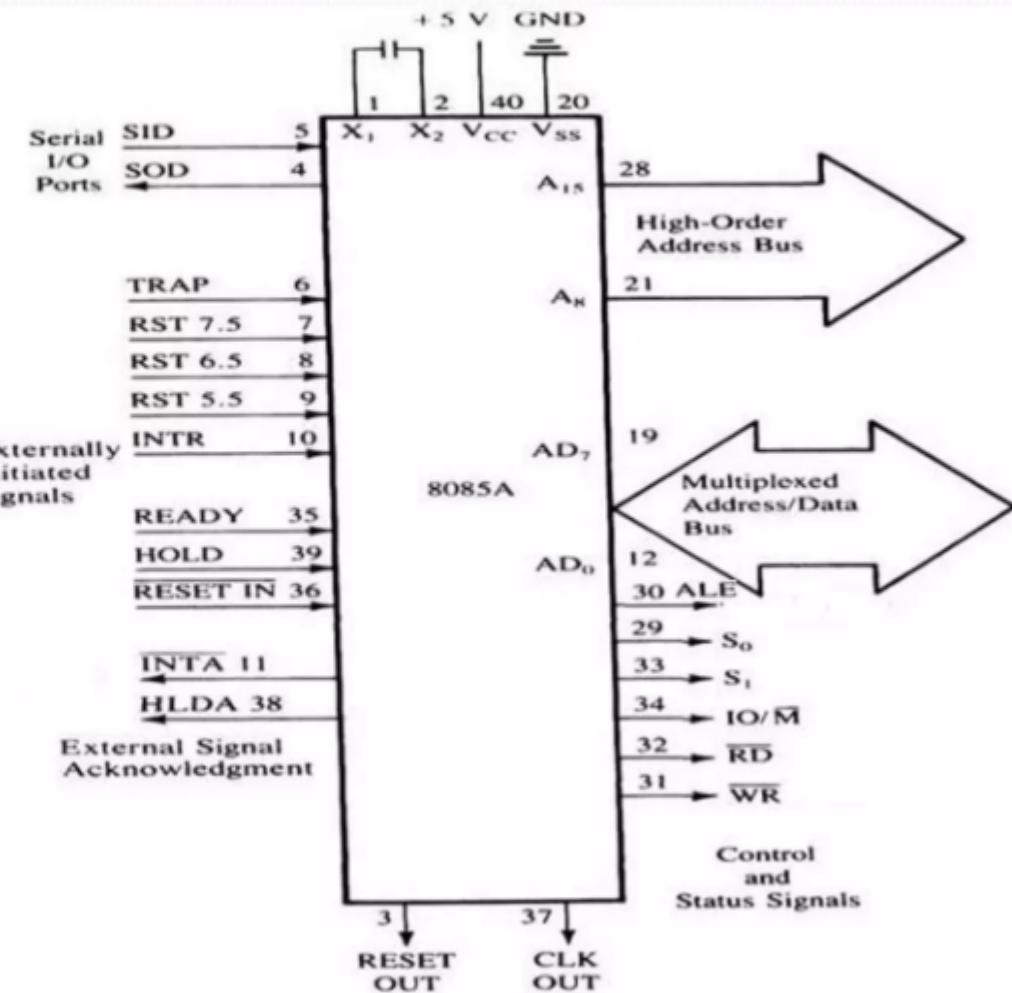
(5) Serial I/O control Group

- Data transfer red on Do- D₇ lines is parallel data
- But under some condition it is used serial data transfer
- Serial data is entered through SID(serial input data) input (received)
- Serial data is outputted on SOD(serial output data) input (send)

8085 Pin Diagram



Pin Configuration



Functional Pin diagram

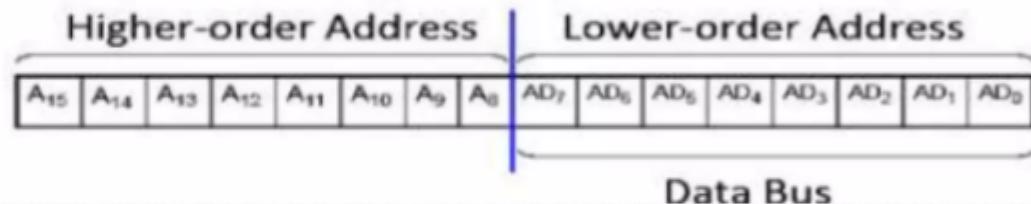
8085 Pin Description

- The 8085 is an 8-bit general purpose microprocessor that can address 64K Byte of memory.
- It has 40 pins and uses +5V for power. It can run at a maximum frequency of 3 MHz.
- The pins on the chip can be grouped into 6 groups:
 - Address Bus and Data Bus.
 - Status Signals.
 - Control signal
 - Interrupt signal
 - Power supply and Clock signal
 - Reset Signal
 - DMA request Signal
 - Serial I/O signal
 - Externally Initiated Signals.

The Address and Data Busses

□ Address Bus (Pin 21-28)

- 16 bit address lines A₀ to A₁₅
- The address bus has 8 signal lines A₈ – A₁₅ which are unidirectional.
- The other 8 address lines A₀ to A₇ are multiplexed (time shared) with the 8 data bits.



□ Data Bus (Pin 19-12)

- To save the number of pins lower order address pin are multiplexed with 8 bit data bus (bidirectional)
- So, the bits AD₀ – AD₇ are bi-directional and serve as A₀ – A₇ and D₀ – D₇ at the same time.
- During the execution of the instruction, these lines carry the address bits during the early part (T₁ state), then during the late parts(T₂ state) of the execution, they carry the 8 data bits.

Status Signals

Status Pins – ALE, S₁, S₀

1. ALE(Address Latch Enable): (Pin 30)

- Used to demultiplexed the address and data bus
- +ive going pulse generated when a new operation is started by uP.
- ALE = 1 when the AD0 – AD7 lines have an address
- ALE = 0 When it is low it indicates that the contents are data.
- This signal can be used to enable a latch to save the address bits from the AD lines.

2. S1 and S0 (Status Signal): (Pin 33 and 29)

- Status signals to specify the kind of operation being performed .
- Usually un-used in small systems.

| S ₁ | S ₀ | Operation |
|----------------|----------------|-----------|
| 0 | 0 | HALT |
| 0 | 1 | WRITE |
| 1 | 0 | READ |
| 1 | 1 | FETCH |

Control Signals

Control Pins – RD, WR, IO/M(active low)

1. RD: Read(Active low) (Pin 32)

- Read Memory or I/O device
- Indicated that data is to be read either from memory or I/P device and data bus is ready for accepting data from the memory or I/O device.

2. WR: Write(Active low) (Pin 31)

- Write Memory or I/O device
- Indicated that data on the data bus are to be written into selected memory or I/P device.

3. IO/M: (Input Output/Memory-Active low) (Pin 34)

- Signal specifies that the read/write operation relates to whether memory or I/O device.
- When (IO/M=1) the address on the address bus is for I/O device
- When (IO/M=0) the address on the address bus is for memory

| IO/M(active low) | RD | WR | Control Signal | Operation |
|------------------|----|----|----------------|-----------|
| 0 | 0 | 1 | MEMR | M/M Read |
| 0 | 1 | 0 | MEMW | M/M write |
| 1 | 0 | 1 | IOR | I/O Read |
| 1 | 1 | 0 | IOW | I/O Write |

Control and status Signals

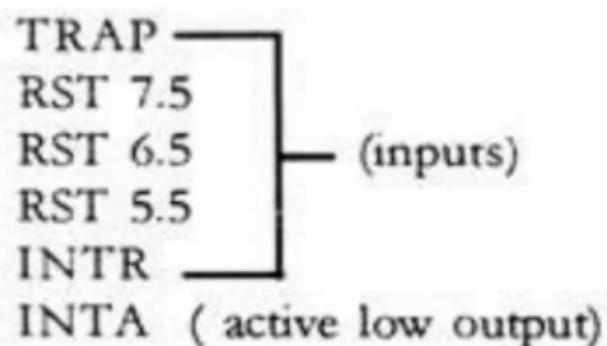
When S_0, S_1 is combined with IO/M(active low), we get status of machine cycle

| IO/M | S_1 | S_0 | OPERATION | Control Signal |
|------|-------|-------|-----------------------|---|
| 0 | 1 | 1 | Opcode fetch | $\overline{RD} = 0$ |
| 0 | 1 | 0 | Memory read | $\overline{RD} = 0$ |
| 0 | 0 | 1 | Memory write | $\overline{WR} = 0$ |
| 1 | 1 | 0 | I/O read | $\overline{RD} = 0$ |
| 1 | 0 | 1 | I/O write | $\overline{WR} = 0$ |
| 1 | 1 | 0 | Interrupt Acknowledge | $\overline{INTA} = 0$ |
| Z | 0 | 0 | Halt | |
| Z | X | X | Hold | |
| Z | X | X | Reset | $\overline{RD}, \overline{WR} = Z$ and $\overline{INTA} = 1$ |

Z= Tristate, X = don't care condition

Interrupts

- They are the signals initiated by an external device to request the microprocessor to do a particular task or work.
- There are five hardware interrupts called, (Pin 6-11)



- On receipt of an interrupt, the microprocessor acknowledges the interrupt by the active low INTA (Interrupt Acknowledge) signal.