

Chapter 4

Timing Diagram

Introduction

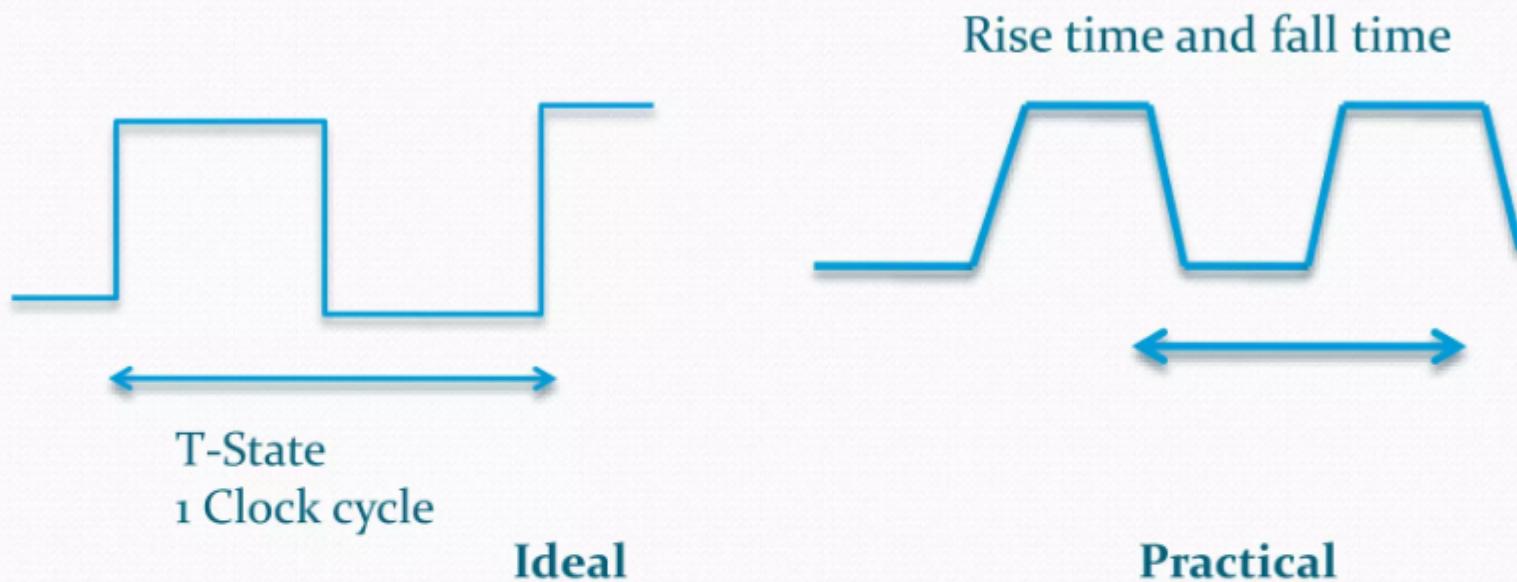
- It represents the execution time taken by each instruction in a graphical format.
- It is the graphical representation of initiation of read/write and transfer of data operations under the control of 3-status signals IO / M , S₁, and S₀. All the operation is performed with respect to CLK signal.
- The combination of these 3-status signals identify read or write operation and remain valid for the duration of the cycle.

Machine cycle	Status			Controls		
	IO / \overline{M}	S ₁	S ₀	\overline{RD}	\overline{WR}	INTA
Opcode Fetch (OF)	0	1	1	0	1	1
Memory Read	0	1	0	0	1	1
Memory Write	0	0	1	1	0	1
I/O Read (I/OR)	1	1	0	0	1	1
I/O Write (I/OW)	1	0	1	1	0	1
Acknowledge of INTR (INTA)	1	1	1	1	1	0
BUS Idle (BI) : DAD	0	1	0	1	1	1
ACK of RST, TRAP	1	1	1	1	1	1
HALT	Z	0	0	Z	Z	1
HOLD	Z	X	X	Z	Z	1

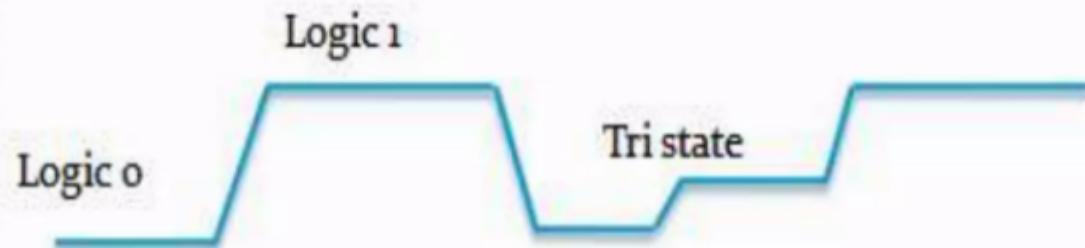
X ⇒ Unspecified, and Z ⇒ High impedance state

Machine cycle status and control signal

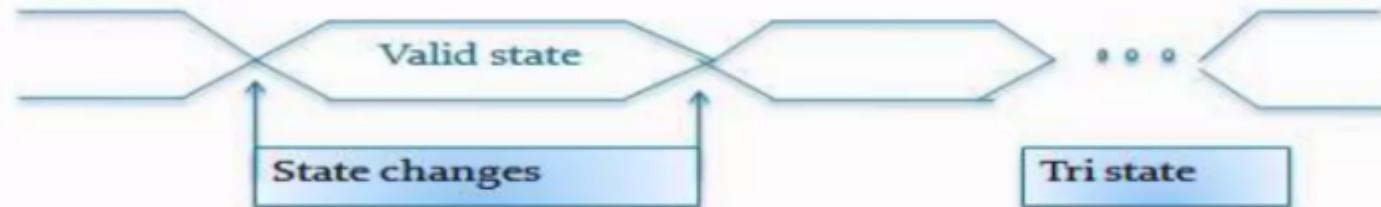
Clock Signal - The 8085 divides the clock frequency provided at x₁ and x₂ inputs by 2 which is called operating frequency.



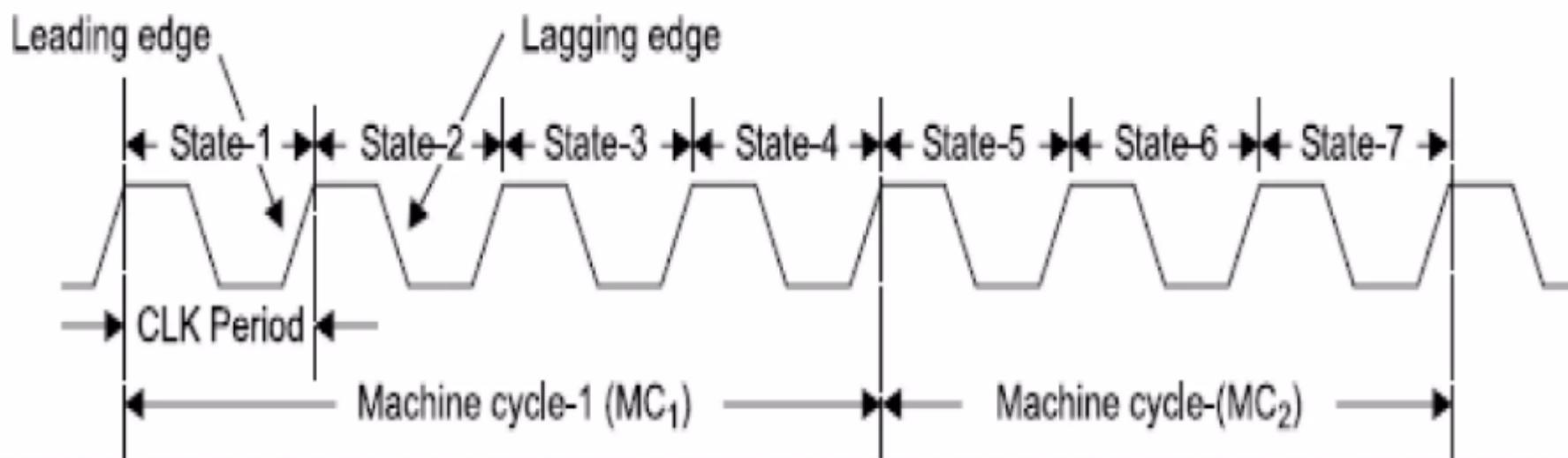
Single Signal - Single signal status is represented by a line. It may have status either logic 0 or logic 1 or tri-state



Group of signals - Group of signals is also called a bus. Eg:
Address bus, data bus



Machine cycle showing clock periods -



Cycles and States

From the above discussion, we can define terms that will become handy later on:

□ T-State:

- One subdivision of an operation performed in one clock period.
- Each T states is precisely equal to one clock period.
- An instruction's execution length is usually measured in a number of T-states.

□ Machine Cycle:

- The time required to complete one operation of accessing memory, I/O, or acknowledging an external request.
- This cycle may consist of 3 to 6 T-states.
- Various machine cycle in 8085 is
 - Opcode fetch
 - Memory read/write
 - Input read/write
 - Interrupt acknowledge
 - Halt/hold
 - Reset

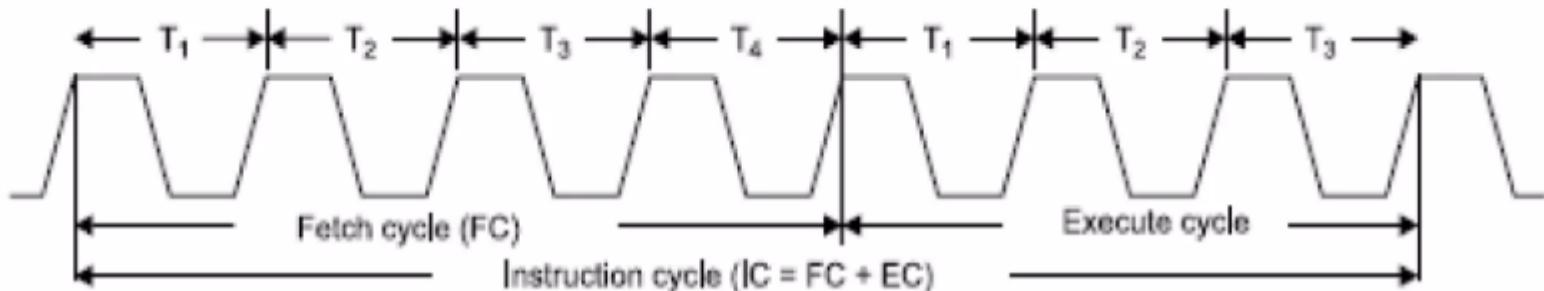
□ Instruction Cycle:

- The time required to complete the execution of an instruction.
- In the 8085, an instruction cycle may consist of 1 to 6 machine cycles.

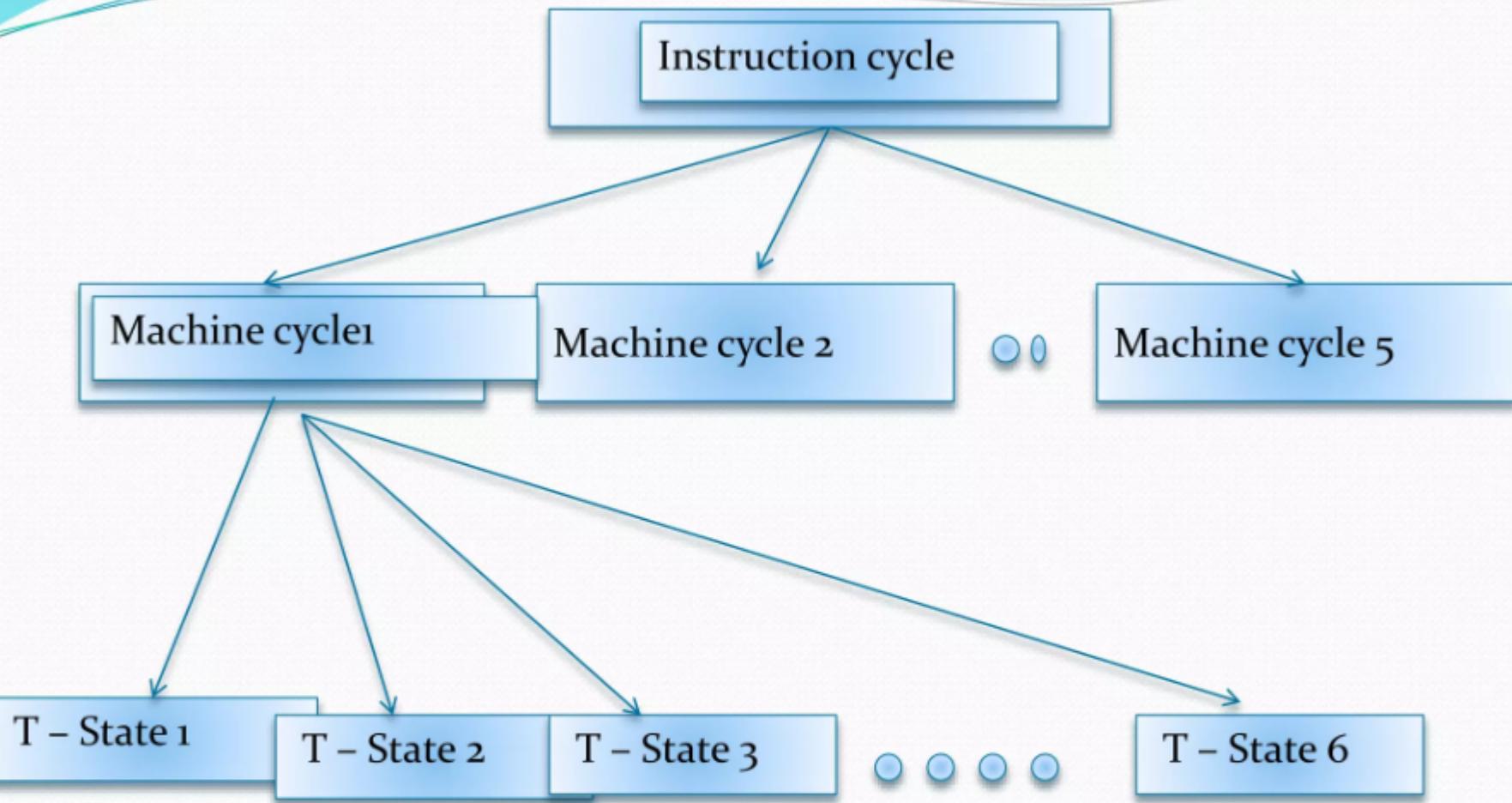
Processor Cycle

- The function of the microprocessor is divided into two cycle of the instruction
 - Fetch
 - Execute
- Number of instructions are stored in the memory in sequence.
- In the normal process of operation, the microprocessor fetches (receives or reads) and executes one instruction at a time in the sequence until it executes the halt (HLT) instruction.
- Thus, an instruction cycle is defined as the time required to fetch and execute an instruction.

$$\text{Instruction Cycle (IC)} = \text{Fetch cycle (FC)} + \text{Execute Cycle (EC)}$$



Processor Cycle



The 8085 microprocessor has 7 basic machine cycles.
They are

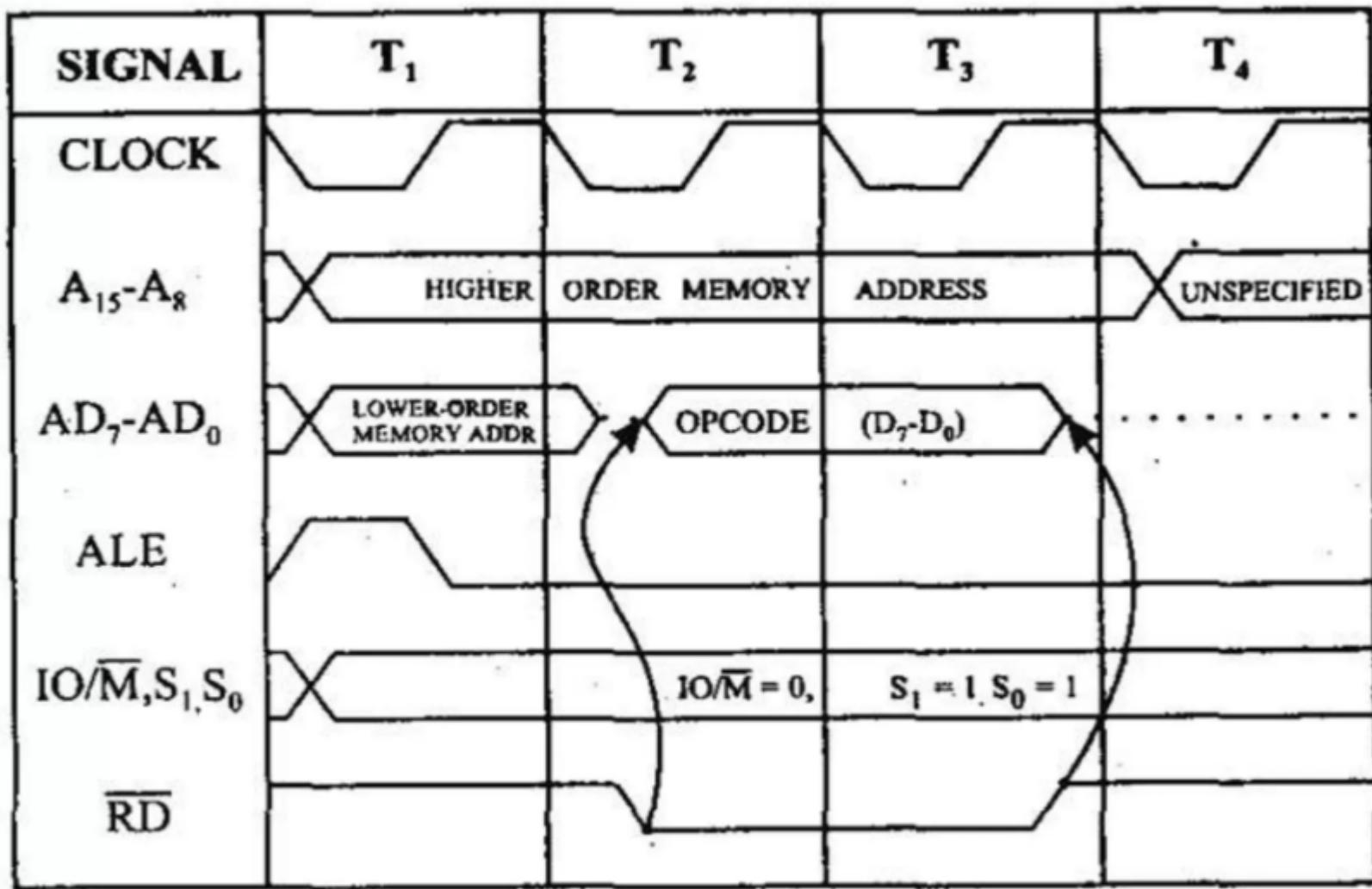
1. Opcode fetch cycle (4 T)
2. Memory read cycle or operand fetch(3 T)
3. Memory write cycle (3 T)
4. I/O read cycle (3 T)
5. I/O write cycle (3 T)
6. Interrupt Acknowledge
7. Bus Idle cycle

Opcode Fetch Machine Cycle

The first step of executing any instruction is the Opcode fetch cycle.

- ❑ In this cycle, the microprocessor brings in the instruction's Opcode from memory.
 - To differentiate this machine cycle from the very similar “memory read” cycle, the control & status signals are set as follows:
 - $\overline{IO/M} = 0$ (memory operation),
 - $S1$ and so are both 1. (opcode fetch)
- ❑ This machine cycle has four T-states.
 - The 8085 uses the first 3 T-states to fetch the opcode.
 - T₄ is used to decode and execute it.
- ❑ It is also possible for an instruction to have 6 T-states in an opcode fetch machine cycle.

Timing Diagram of Opcode Fetch



Timing Diagram for Opcode Fetch Machine Cycle

Timing: Transfer of byte from memory to MPU

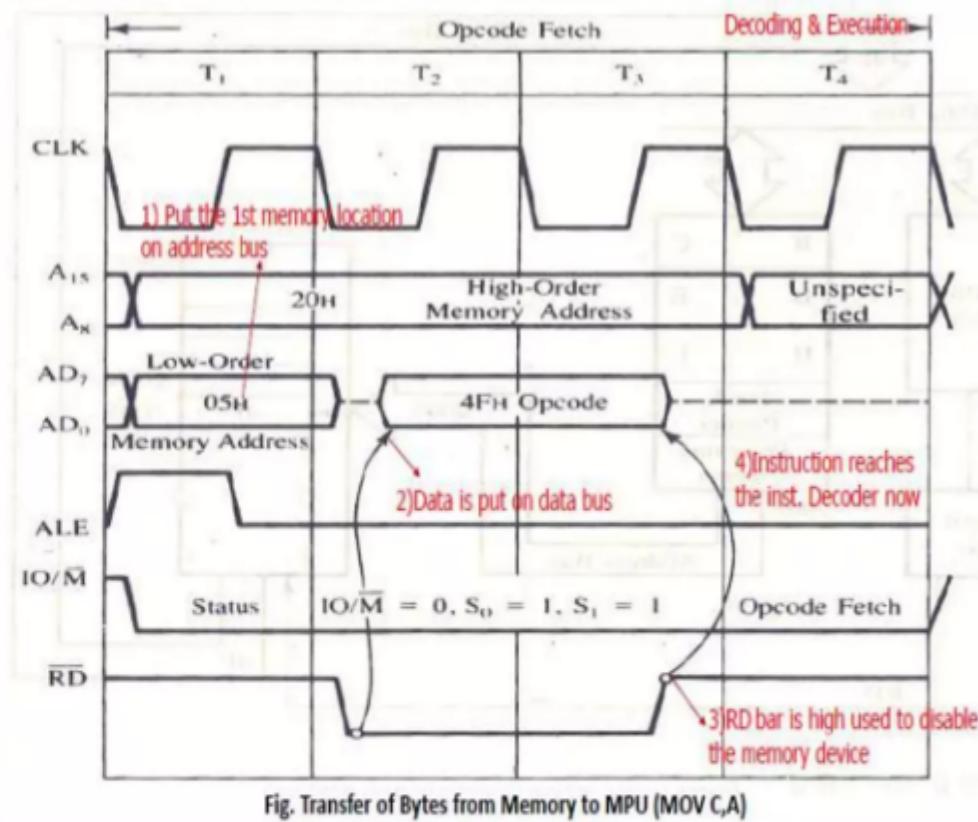
- How a data byte is transfer from memory to the MPU.
- It shows the five different group of signals with clock

Step 1: At T₁ higher order memory address 20H is placed on the A₁₅ – A₈ and the lower order memory address 05H is placed on the bus AD₇-AD₀, and ALE signal high. IO/M goes low(memory related signal).

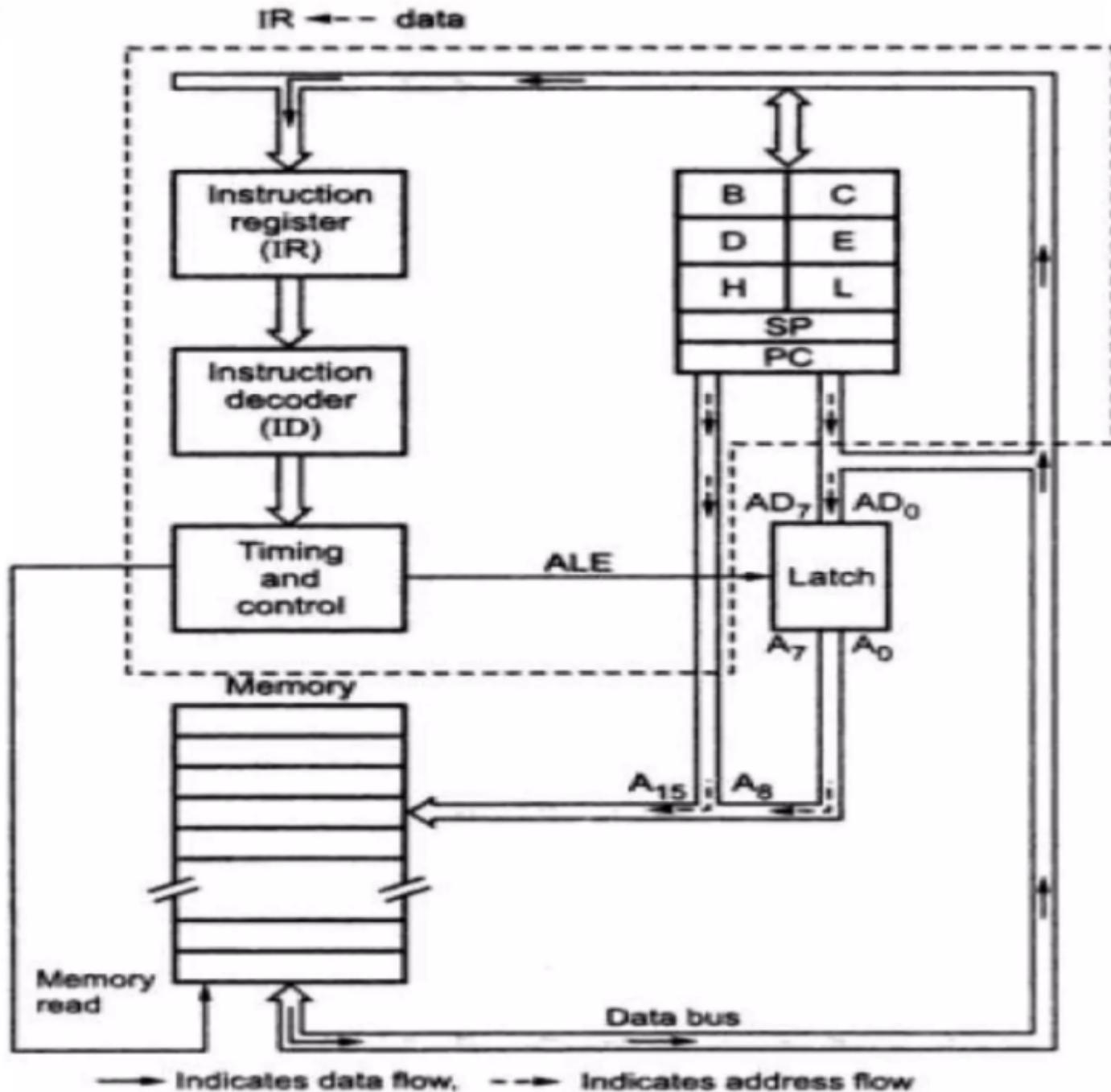
Step 2: During T₂ RD signal is sent out. RD is active during two clock periods.

Step 3 : During T₃, Memory is enabled then instruction byte 4FH is placed on the data bus and transferred to MPU. When RD goes high it causes the bus to go into high impedance state.

Step 4: During T₄, the machine code or byte is decoded by the instruction decoder and content of A is copied into register.



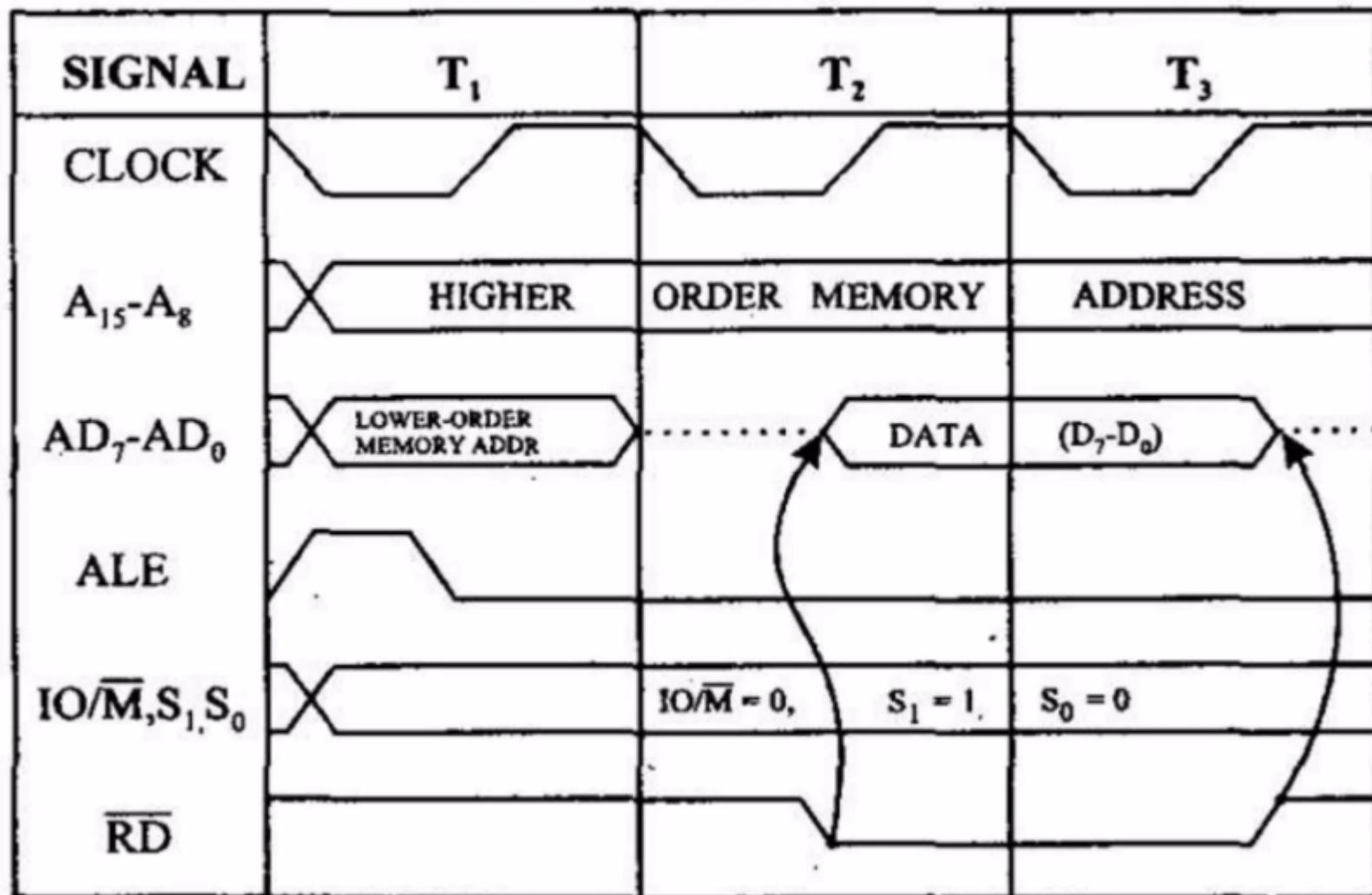
Data Flow form Memory to MP



Memory Read or Operand Fetch Machine Cycle

- This cycle is executed by the processor to read a data byte from memory or to fetch operand in a multi byte instruction. For ex. 2 or 3 byte instruction because in 1 byte instruction the machine code is an opcode; so operation is always an opcode fetch
- The instructions which have more than one byte word size will use the machine cycle after the opcode fetch machine cycle.
- The memory read machine cycle is exactly the same as the opcode fetch except:
 - **IO/M= 0(memory operation),**
 - **s₁ = 1 and s₀ = 0. (memory read)**
 - **WR = 1 & RD = 0**
 - It only has 3 T-states
- First cycle is opcode fetch cycle.
- So this cycle requires
 $4T(\text{opcode}) + 3T(\text{memory read}) = 7 \text{ T states to execute.}$

Timing Diagram of Memory Read Machine Cycle

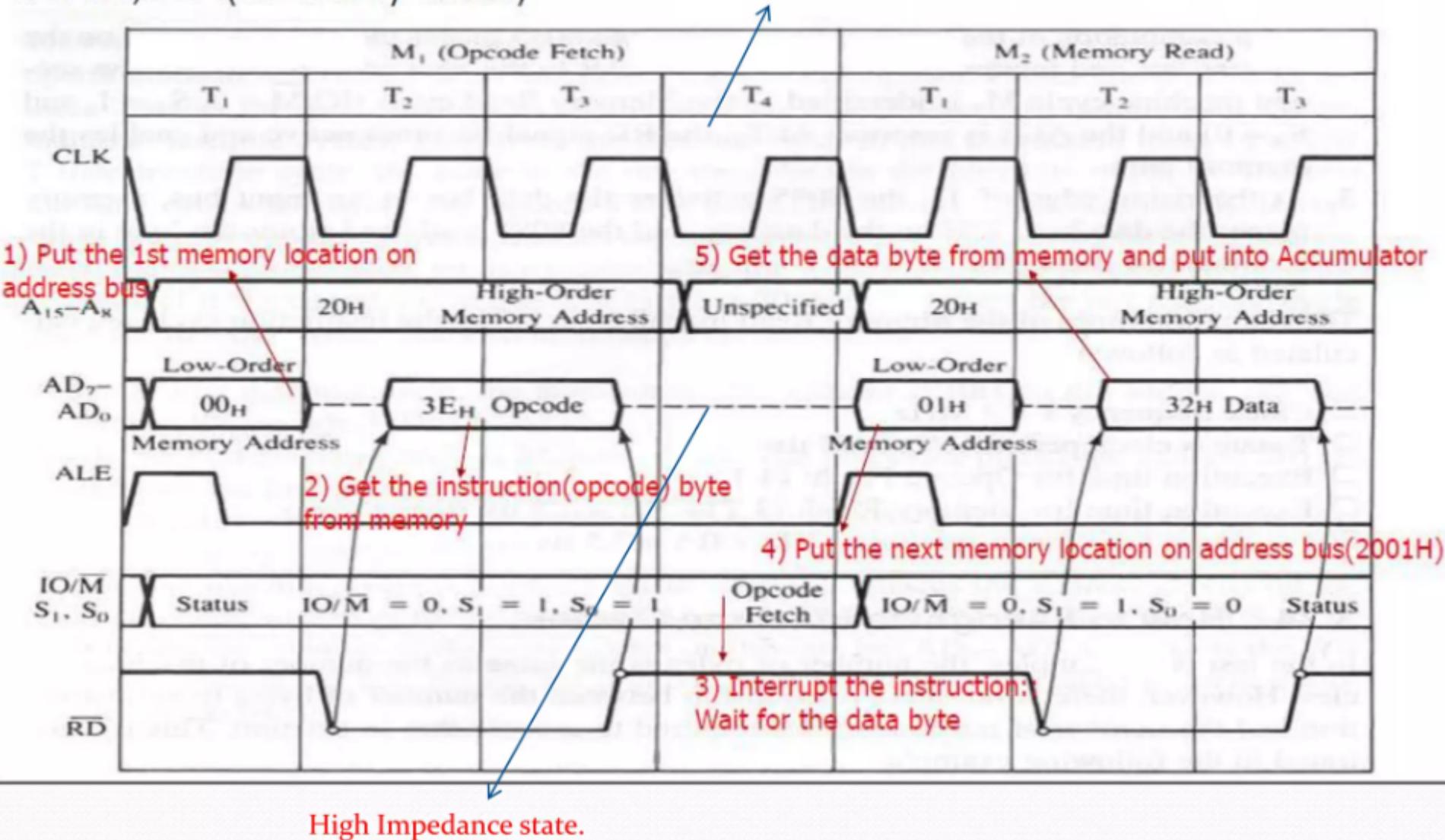


Timing for execution of the instruction MVI A, 32H

MVIA, 32H is 2 byte instruction, so hex code for MVI A is 3E.

MVI A,32H(Memory Read)

8085 decode the opcode and finds out a second byte need to be read



The execution times of the memory read machine cycle and the instruction cycle are calculated as

Clock Frequency $f = 2\text{MHz}$

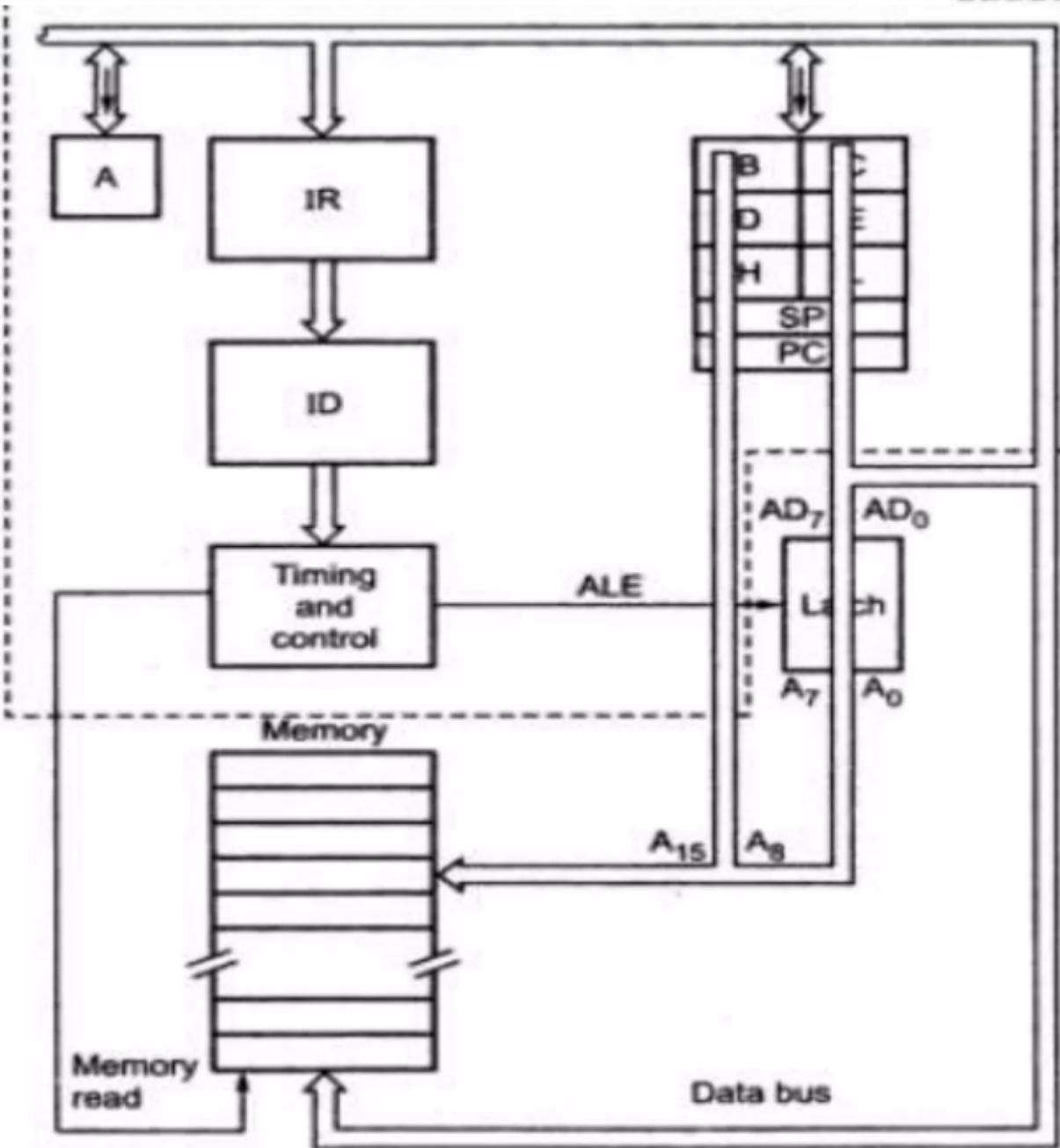
$T_{\text{state}} = \text{clock period } (1/f) = 0.5\mu\text{sec}$

Execution time for opcode fetch = $4T * 0.5 = 2\mu\text{sec}$

Execution time for Memory Read = $3T * 0.5 = 1.5\mu\text{sec}$

Execution time for Instruction = $7T * 0.5 = 3.5\mu\text{sec}$

Data Flow from Memory to MP

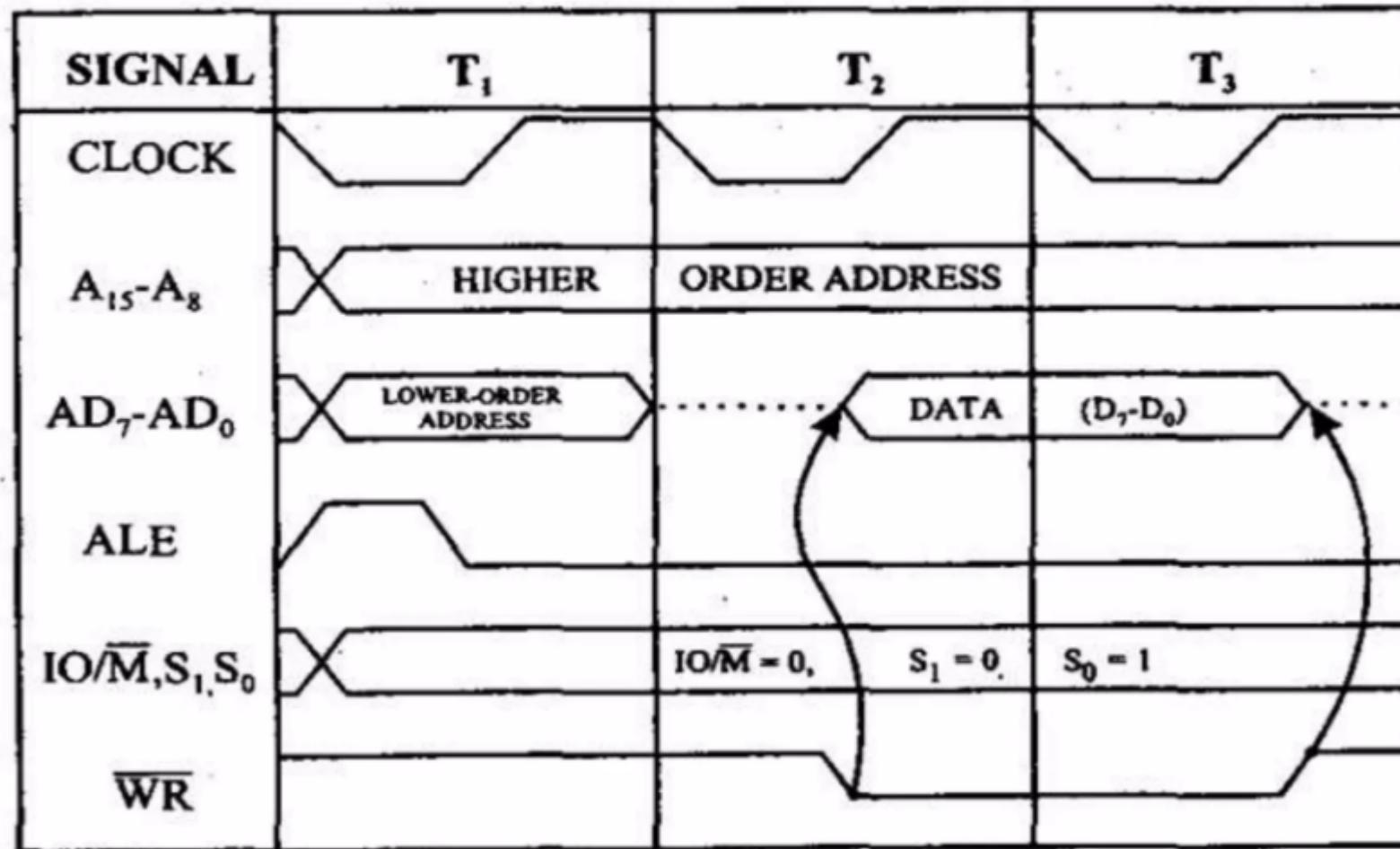


→ Indicates data flow, - - → Indicates address flow

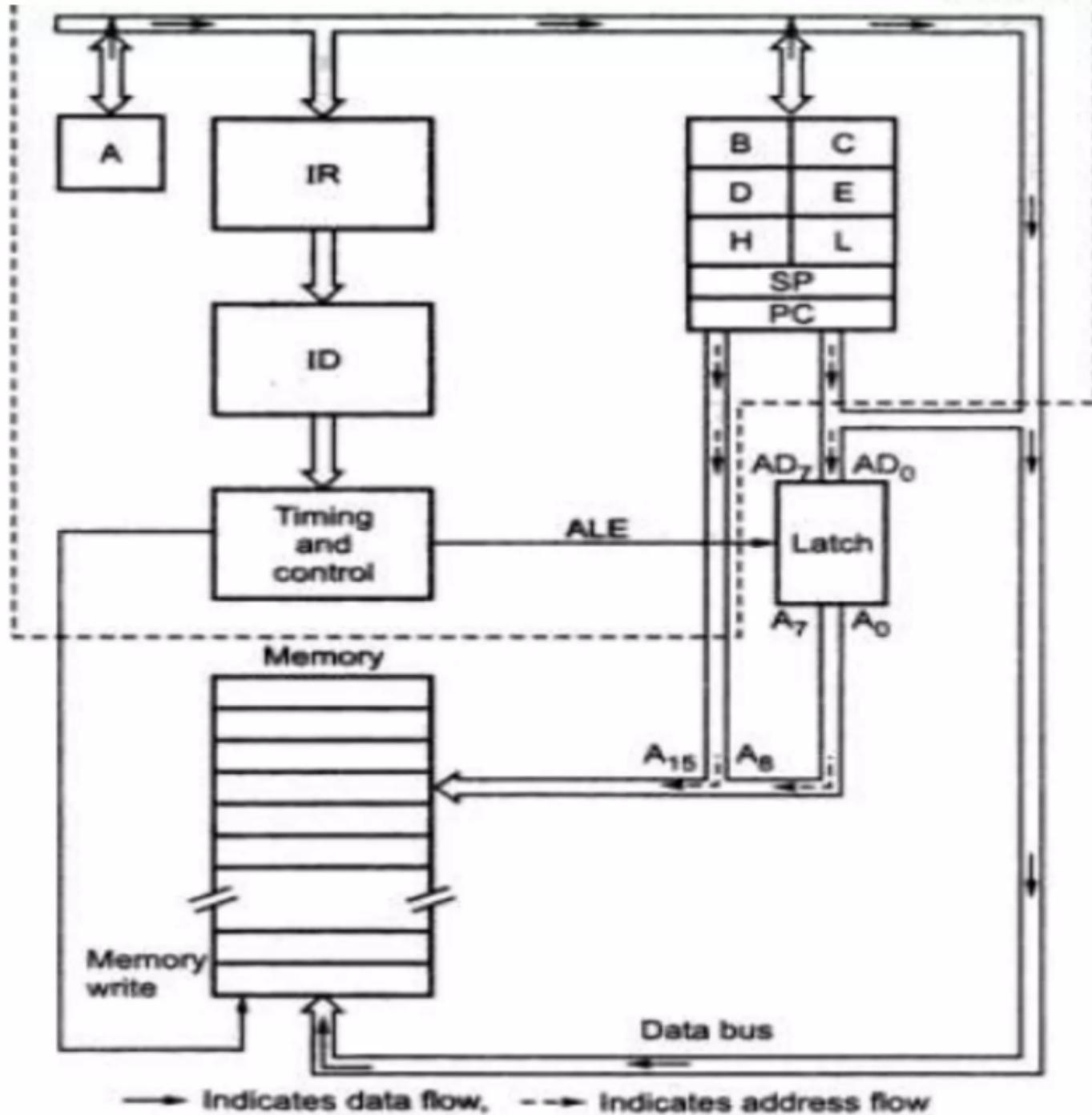
Memory Write Machine Cycle

- The memory write machine cycle is executed by the processor to write a data byte in a memory location.
- The memory write machine cycle is exactly the same as the memory read except:
 - **IO/M= 0 (memory operation),**
 - **S₁ = 0 and S₀ = 1. (memory read)**
 - **WR = 0 & RD = 1**
 - It only has 3 T-states
- First cycle is opcode fetch cycle.
- So this cycle requires
 $4T(\text{opcode}) + 3T(\text{memory write }) = 7 \text{ T states}$ to execute.

Timing Diagram of Memory write Machine Cycle



Data Flow from MPU to Memory



Input/ Output Read Machine Cycle

- Microprocessor executes this cycle to read content of I/O port or to read 8 bit data present on an input ports through data bus.
- The I/O read machine cycle is exactly the same as the memory read except:
 - $\text{IO/M} = 1$ (I/O operation),
 - $\underline{\text{SO}} = 0$ and $\underline{\text{SI}} = 1$. (read)
 - $\overline{\text{WR}} = 1$ & $\text{RD} = 0$
 - It only has 3 T-states
- This instruction reads the data from an input device and places the data byte in the accumulator.
- It accept the data from input device by using I/O read signal(IOR).