DIGITAL ELECTRONICS: ECE 213

Topic: Introduction to Counters and its Types

UNIT IV: COUNTERS AND REGISTERS

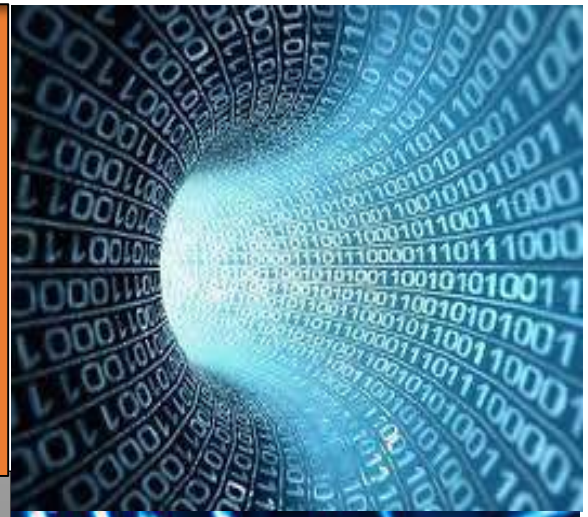
Lecture No.: 31

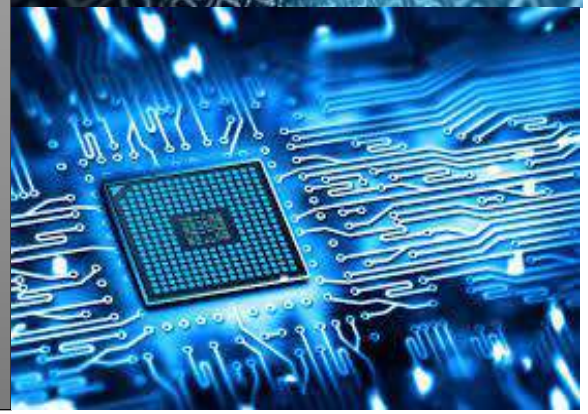
Prepared By: Irfan Ahmad Pindoo

Assistant Professor

VLSI Design, ECE

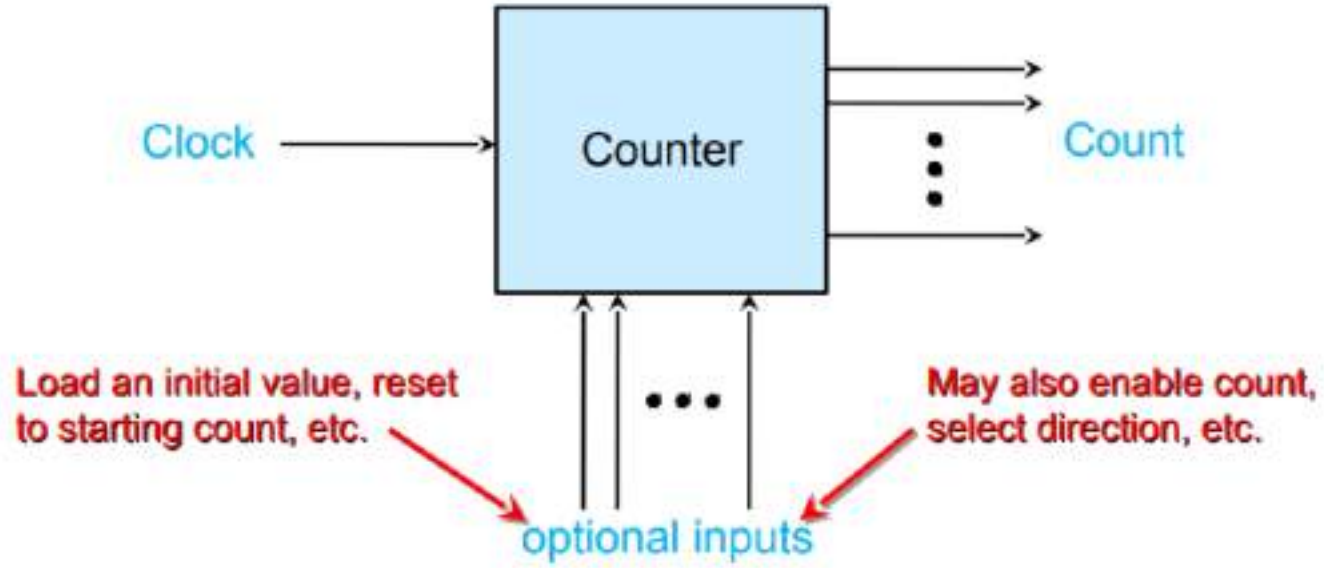
School of Computer Science and Engineering





Introduction to Counters

- A digital circuit which is used for a counting pulses is known as counter.
- Counter is a sequential circuit.
- Counter is the widest application of flip-flops.
- It is a group of flip-flops with a clock signal applied.

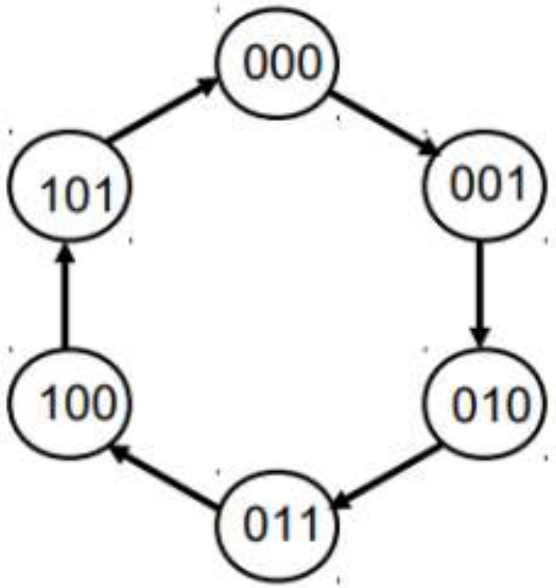


Applications of Counter

1. Frequency counters
2. Digital clock
3. Time measurement
4. A to D converter
5. Frequency divider circuits
6. Digital triangular wave generator.

Types of Counter

- Asynchronous
  - Ripple
- Synchronous
  - Clocked

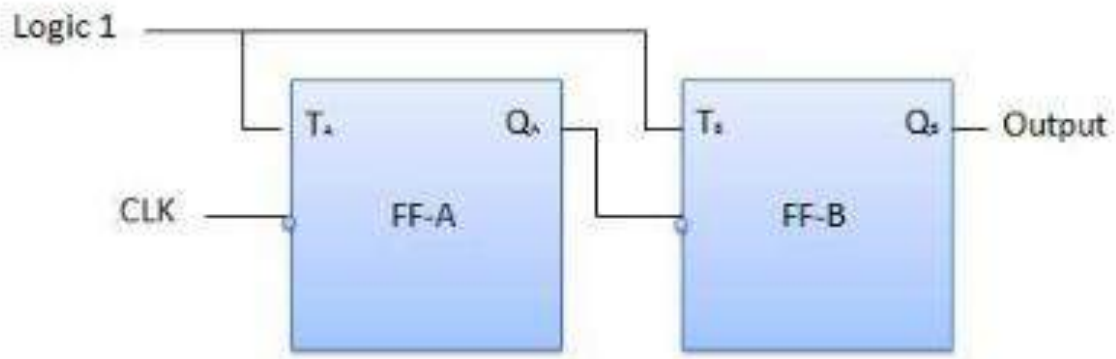


- Modulus
  - Binary
  - Decade
  - etc.
- Ring
- Johnson
  - Twisted ring
- Up/Down
- Linear Feedback Shift-Register Counter (LFSR)

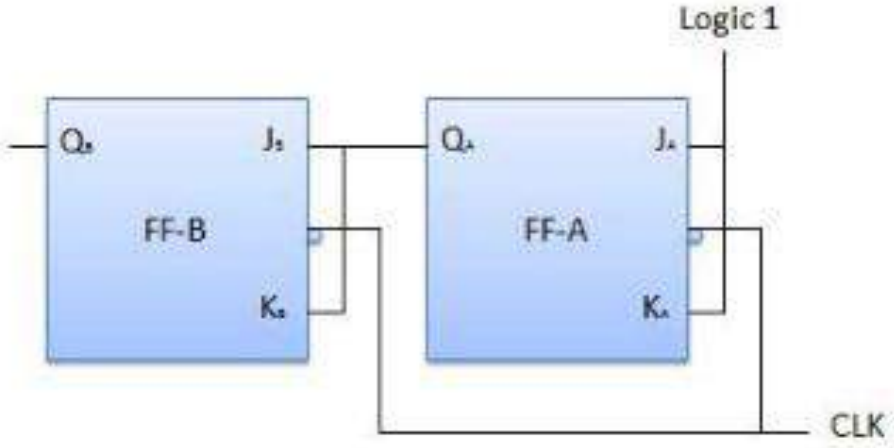
Synchronous and Asynchronous Counters

- In **Asynchronous Counter** is also known as Ripple Counter, different flip flops are triggered with different clock, not simultaneously.
- While in **Synchronous Counter**, all flip flops are triggered with same clock simultaneously.

Asynchronous Counter:



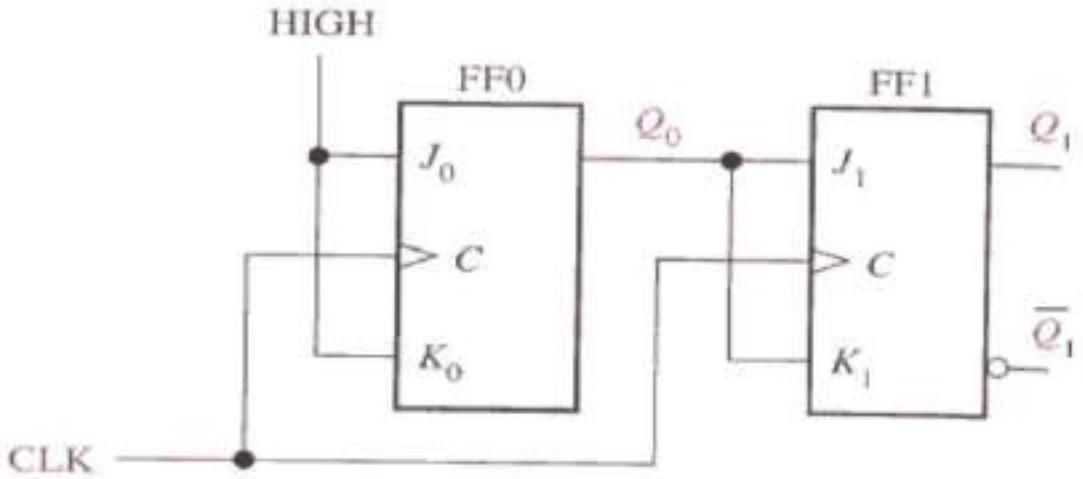
Synchronous Counter:



Quick Quiz (POLL)

The diagram given represents:

a) Master slave flip flop
b) Asynchronous counter
c) Synchronous counter
d) 2-bit ripple counter



C

Synchronous and Asynchronous Counters

Synchronous Counter	Asynchronous Counter
In synchronous counter, all flip flops are triggered with same clock simultaneously.	In asynchronous counter, different flip flops are triggered with different clock, not simultaneously.
Synchronous Counter designing as well implementation are complex due to increasing the number of states.	Asynchronous Counter designing as well as implementation is very easy.
Synchronous Counter will operate in any desired count sequence.	Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).
propagation delay is less.	There is high propagation delay.
Faster	Slower

Quick Quiz (POLL)

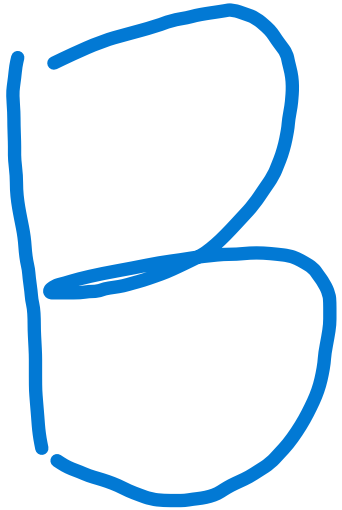
Identify the **wrong** statement?

a) Synchronous counters are faster.

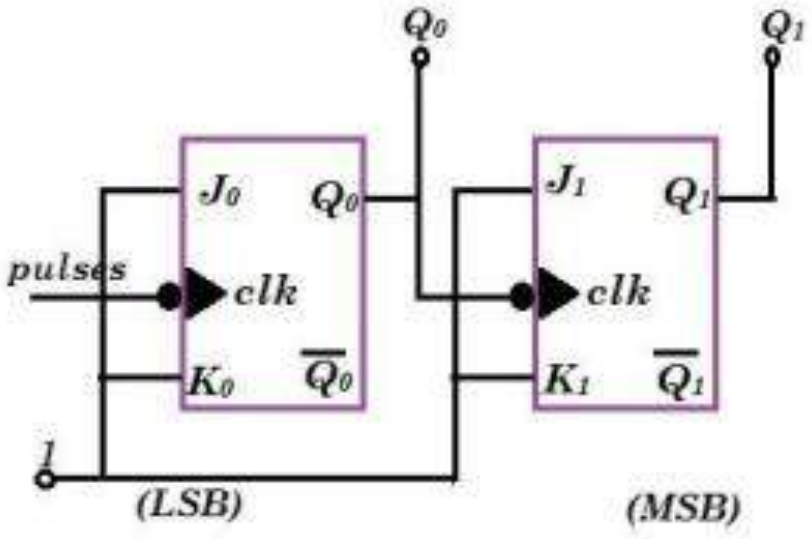
b) Synchronous counters have more propagation delay.

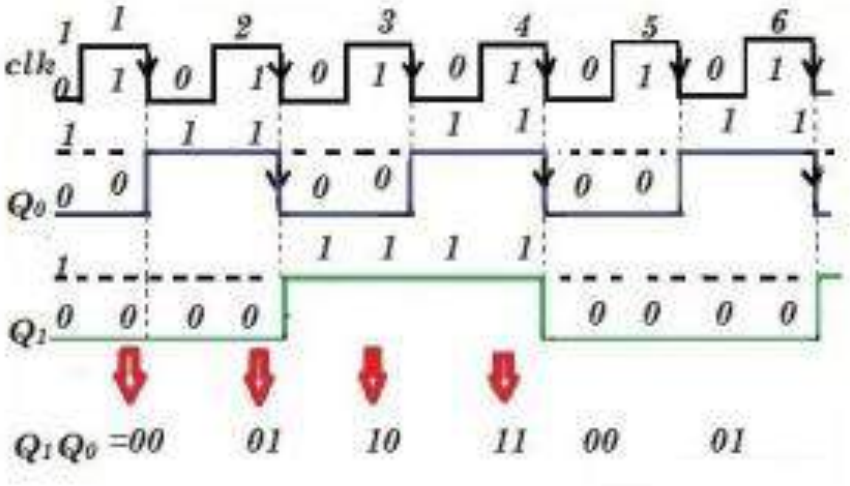
c) Asynchronous counters is also called as ripple counter.

d) All flip flops are clocked simultaneously in Synchrnous counters



Design of 2-bit Asynchronous UP Counter





Quick Quiz (POLL)

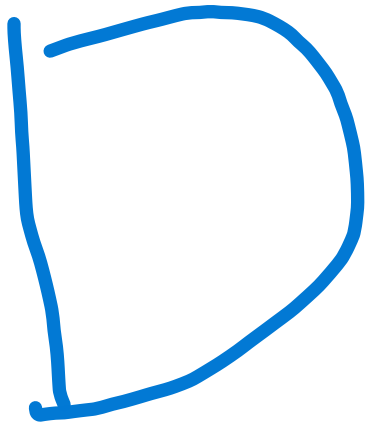
For a counter with two flip flops, how many maximum states are possible:

a) 1

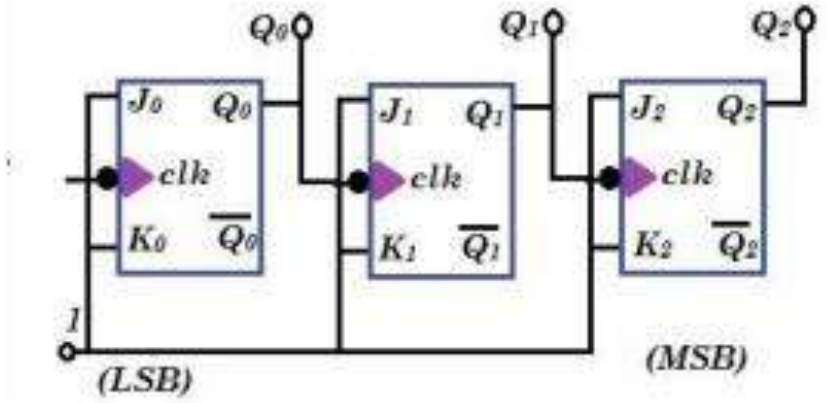
b) 2

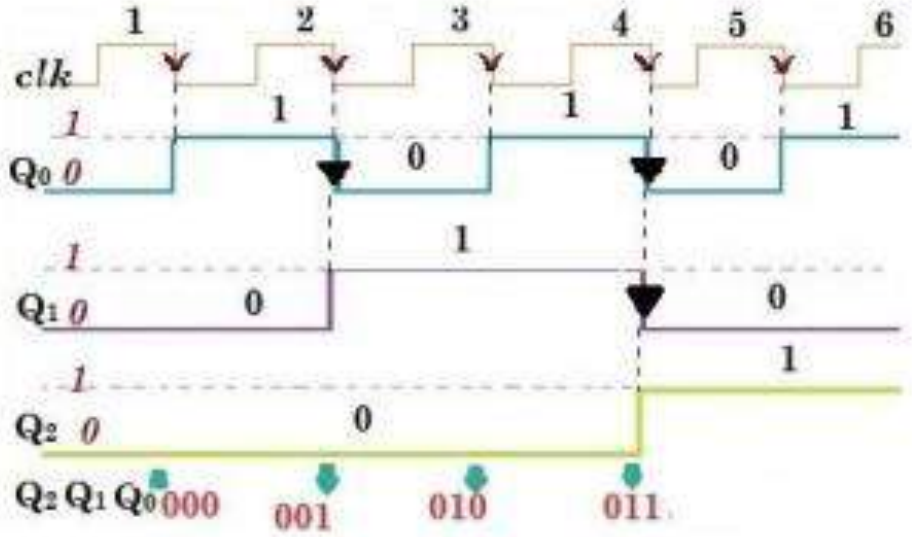
c) 3

d) 4



Design of 3-bit Asynchronous UP Counter





Design of Asynchronous Down Counter

One way is to take the output across Qbar in a down counter, instead of Q.

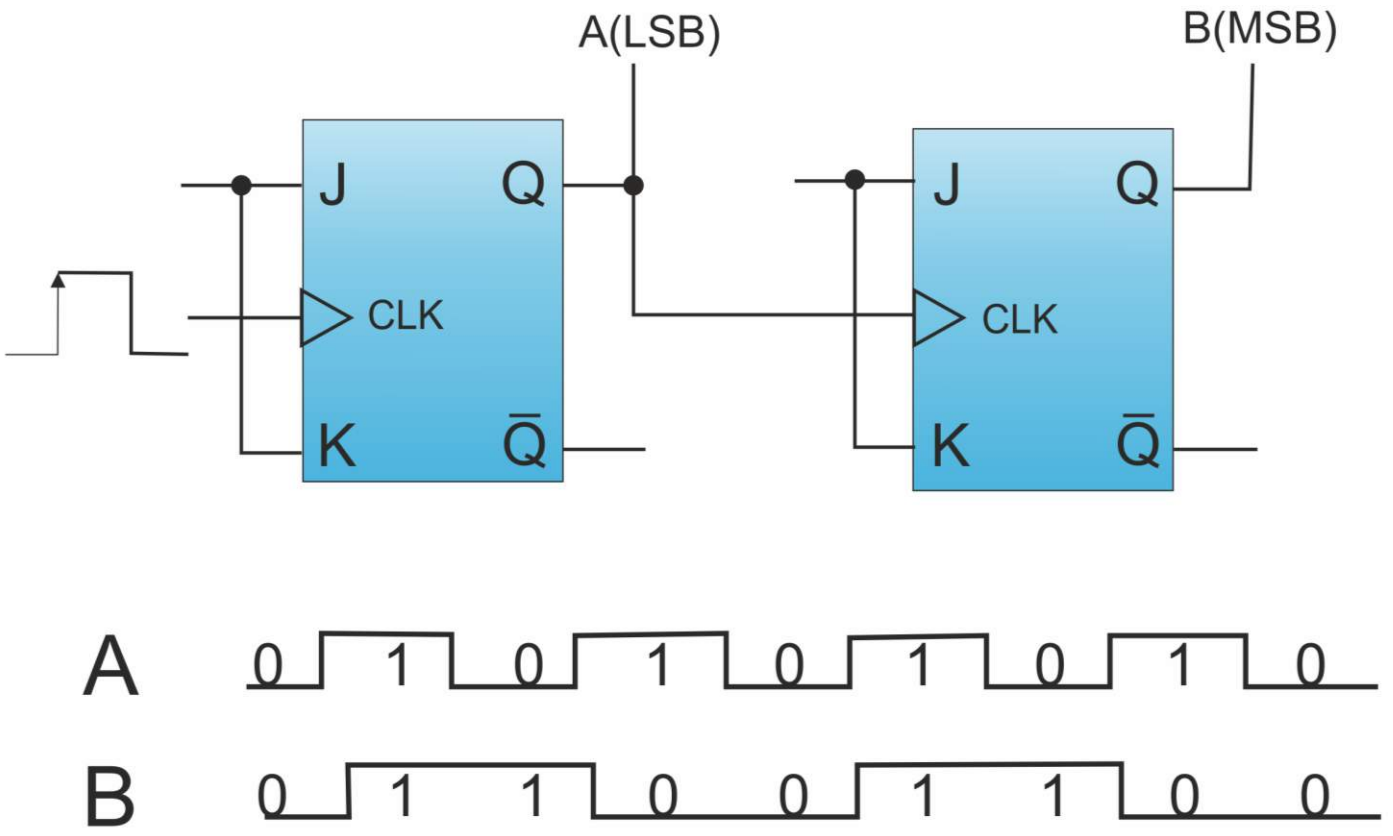
OR

An alternate way of making a down counter is to provide clock to n-1 flip flops via Qbar instead of Q, while taking outputs from Q only.

OR

Changing the clock pulse to positive edge triggering, while taking outputs from Q only.

Design of 2-bit Asynchronous Down Counter



DIGITAL ELECTRONICS: ECE 213

Topic: Introduction to Counters and its Types

UNIT IV: COUNTERS AND REGISTERS

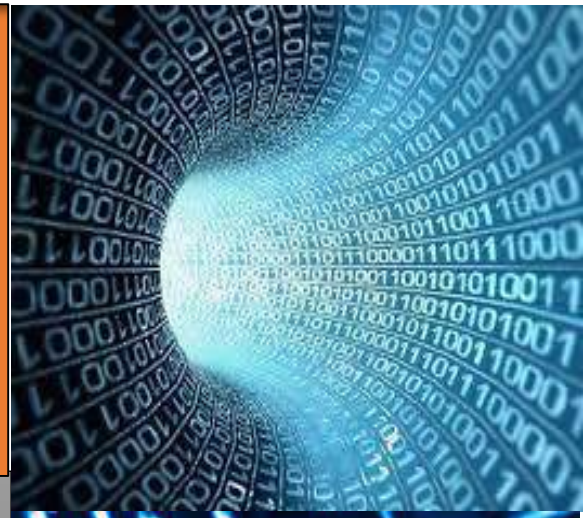
Lecture No.: 32

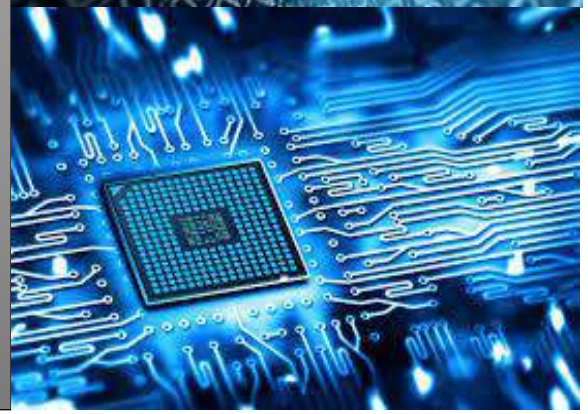
Prepared By: Irfan Ahmad Pindoo

Assistant Professor

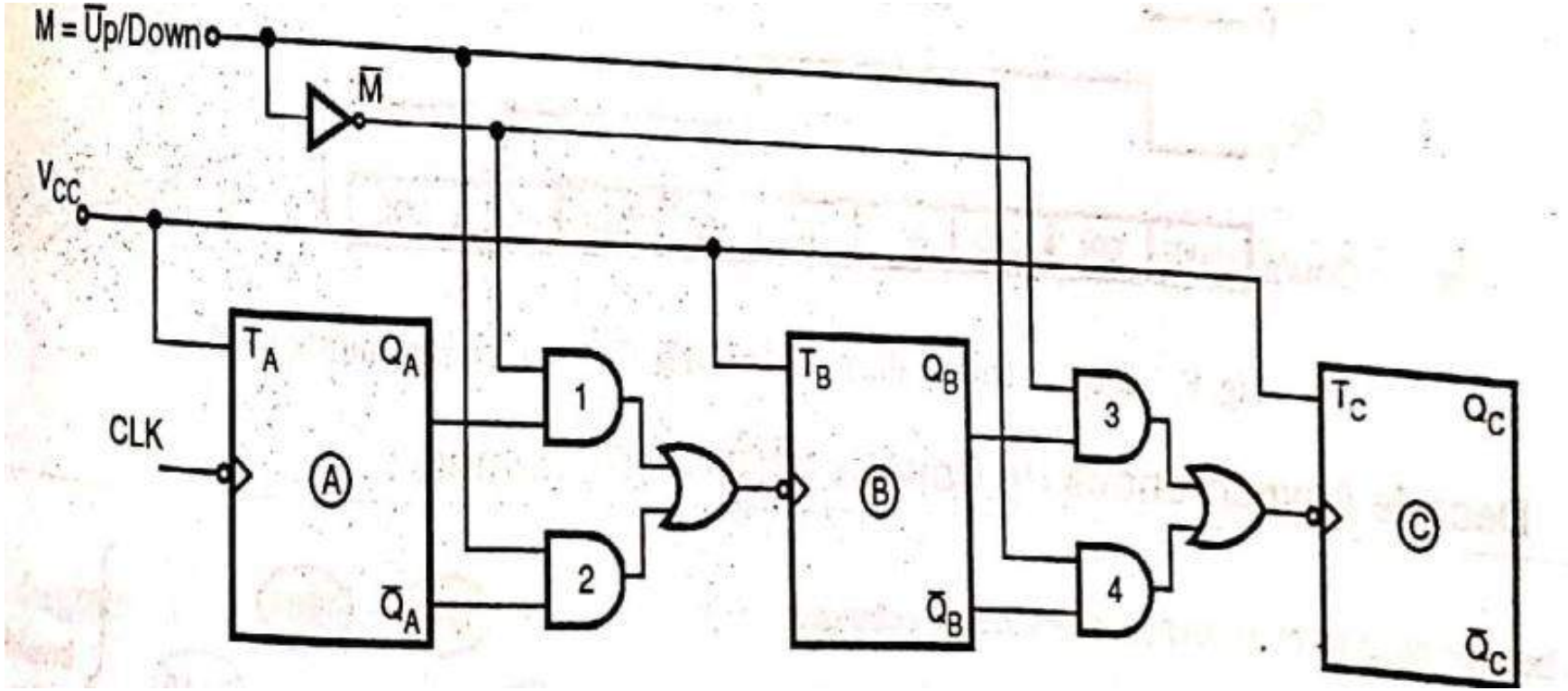
VLSI Design, ECE

School of Computer Science and Engineering





Design of 3-bit Asynchronous Up-Down Counter



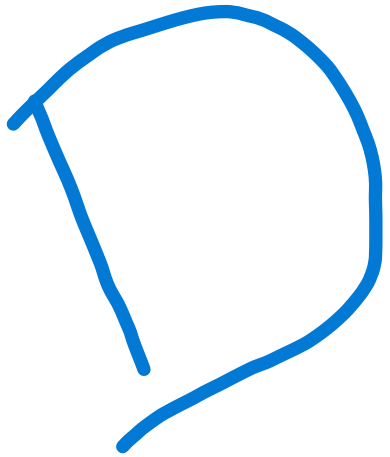
Design of Asynchronous Decade Counter

- An Asynchronous counter can have $2^n - 1$ possible counting states e.g. MOD-16 for a 4-bit counter, (0-15) making it ideal for use in Frequency Division applications.
- But it is also possible to use the basic asynchronous counter configuration to construct special counters with counting states less than their maximum output number. For example, modulo or MOD counters.
- This is achieved by forcing the counter to reset itself to zero at a predetermined value producing a type of asynchronous counter that has truncated sequences.
- Then an n-bit counter that counts up to its maximum modulus (2^n) is called a full sequence counter and a n-bit counter whose modulus is less than the maximum possible is called a truncated counter.

QUICK QUIZ (POLL)

Number of states in a 4-bit decade counter are?

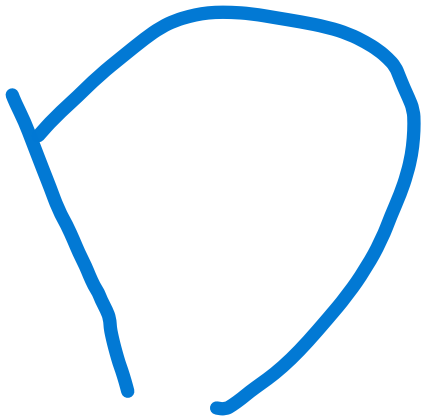
a) 4
b) 16
c) 11
d) 10



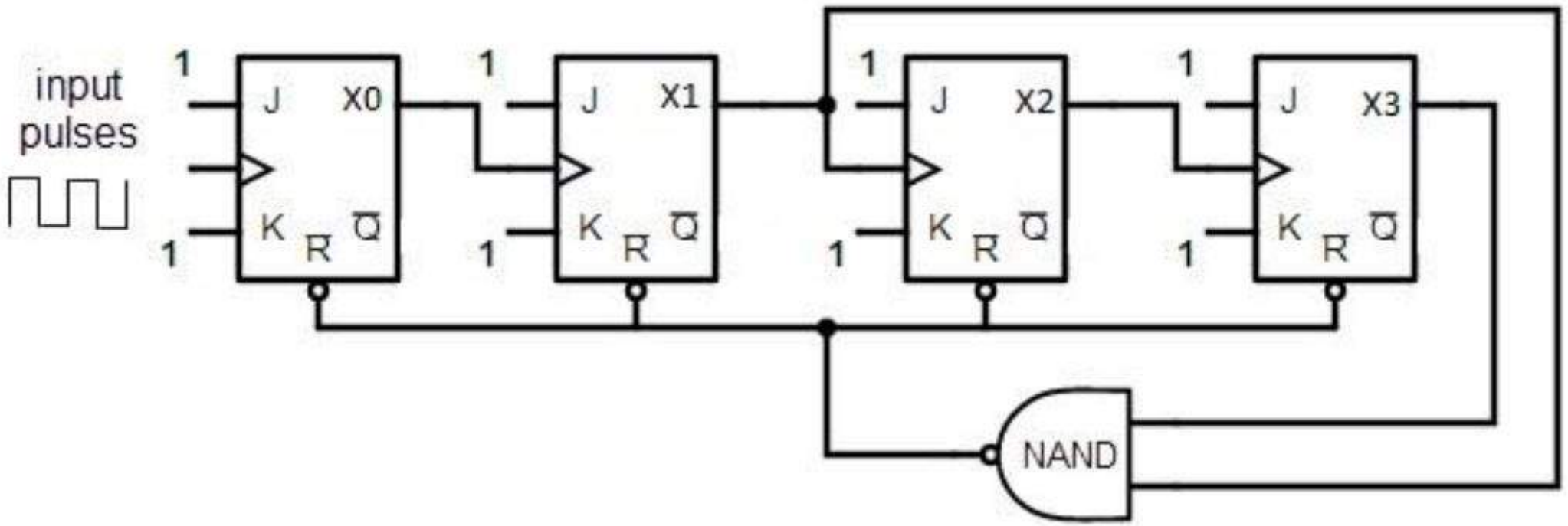
QUICK QUIZ (POLL)

If the given counter is Mod-12, it means, the number of states are?

a) 4
b) 16
c) 11
d) 12

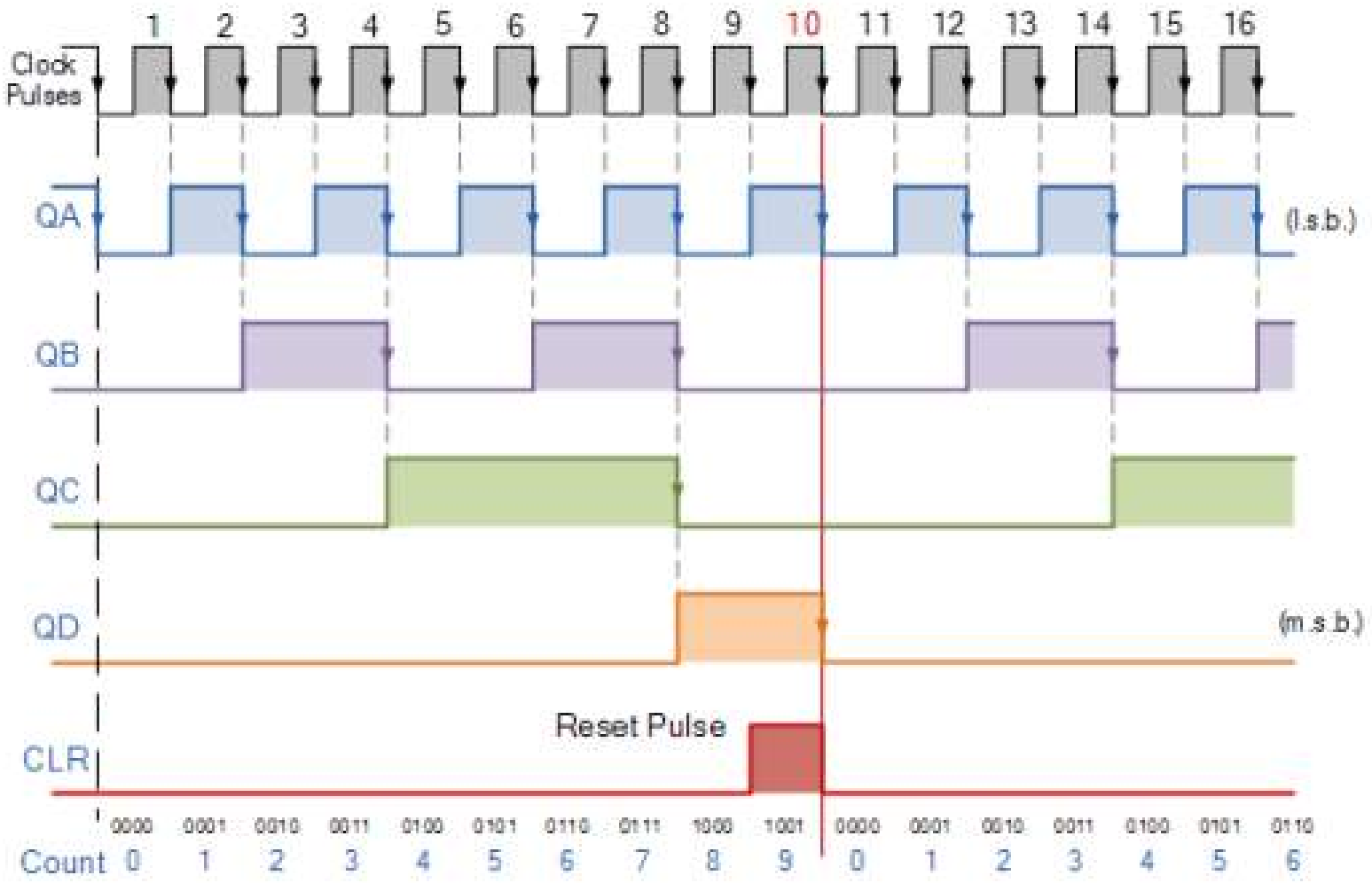


Design of Asynchronous Decade Counter



Design of Asynchronous Decade Counter

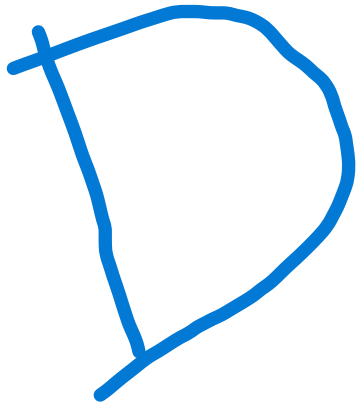
Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
0	0	0	0	0 (resets)



QUICK QUIZ (POLL)

For a decade counter, the outputs are reset at _____ condition of outputs?

a) 1011
b) 1100
c) 1001
d) 1010



DIGITAL ELECTRONICS: ECE 213

Topic: Introduction to Counters and its Types

UNIT IV: COUNTERS AND REGISTERS

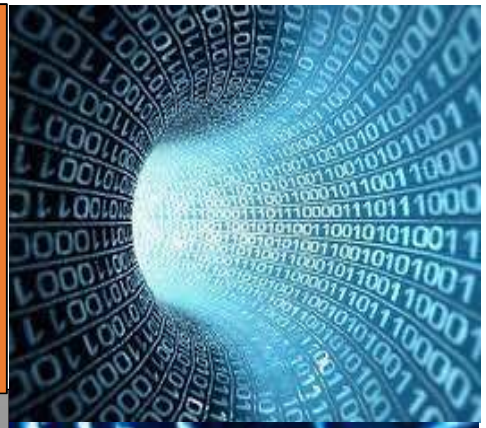
Lecture No.: 34

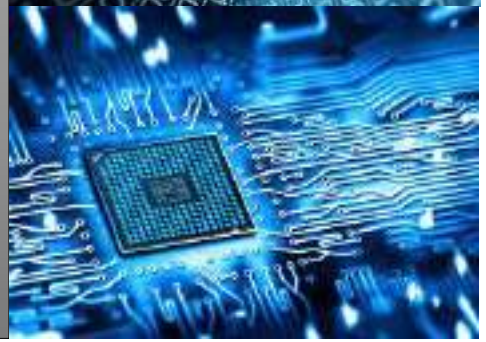
Prepared By: Irfan Ahmad Pindoo

Assistant Professor

VLSI Design, ECE

School of Computer Science and Engineering





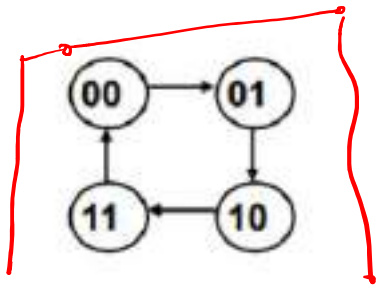
QUICK QUIZ (POLL)

The random sequence of counting is possible in

a) Ripple counter
b) Asynchronous counter
c) Synchronous counter
d) None of these

Design of 2-bit Synchronous UP Counter

0 → 1 → 2
7 → 6 → 5

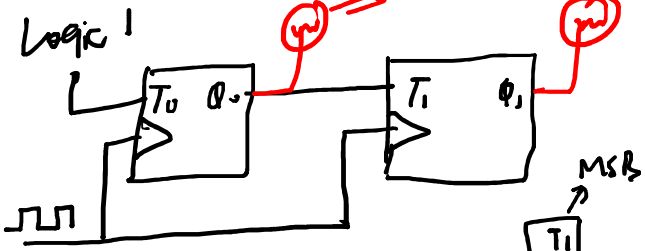


STATE TABLE:

Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

1. Create a state table.
2. Use k-map to get Eqns - $T_0 = 1$, $T_1 = Q_1\bar{Q}_0 + \bar{Q}_1 Q_0$, $T_1 = Q_0$
3. Create the design.

Design Logic



- Excitation Table

Q_0	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

XOR

MSB

T_1 T_0

0 0	0
0 1	1
1 0	1
1 1	0

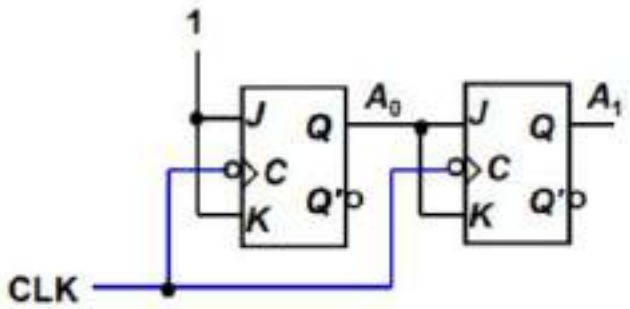
P.S		N.S		Flip Flops	
Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

Design of 2-bit Synchronous UP Counter

Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

$TA_1 = A_0$

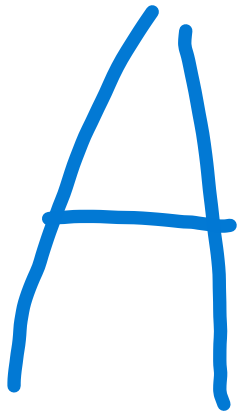
$TA_0 = 1$



QUICK QUIZ (POLL)

The table representing the present state, next state and the flip flop inputs is referred as:

a) State table
b) Excitation table
c) Characteristic table
d) Truth table



Design of 3-bit Synchronous UP Counter

→ 3 F/Fs [JK Flip Flops]

0 → 1 → 2 → 3 → 4 → 5 → 6 → 7 → 0

Step 1:- Create a State Table:-

Present State $Q_2\ Q_1\ Q_0$	Next State $Q_2^+\ Q_1^+\ Q_0^+$	Flip Flop Inputs $J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$
⇒ 0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	1 0 1	X 0	0 X	1 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	0 0 0	X 1	X 1	X 1

Step 2: K map

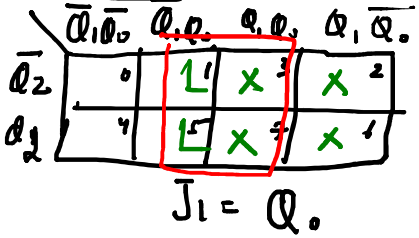
$J_0 = K_0 = 1$ = Logic 1.

$J_1 = K_1 = Q_0$

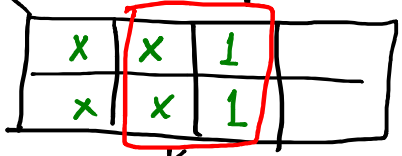
$J_2 = K_2 = Q_1 Q_0$

E-T

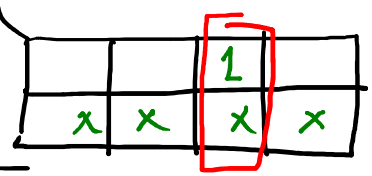
Q_1	Q_1^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



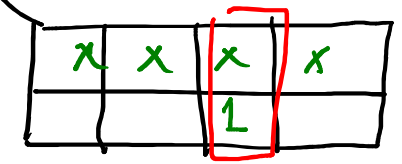
$J_1 = Q_0$



$K_1 = Q_0$

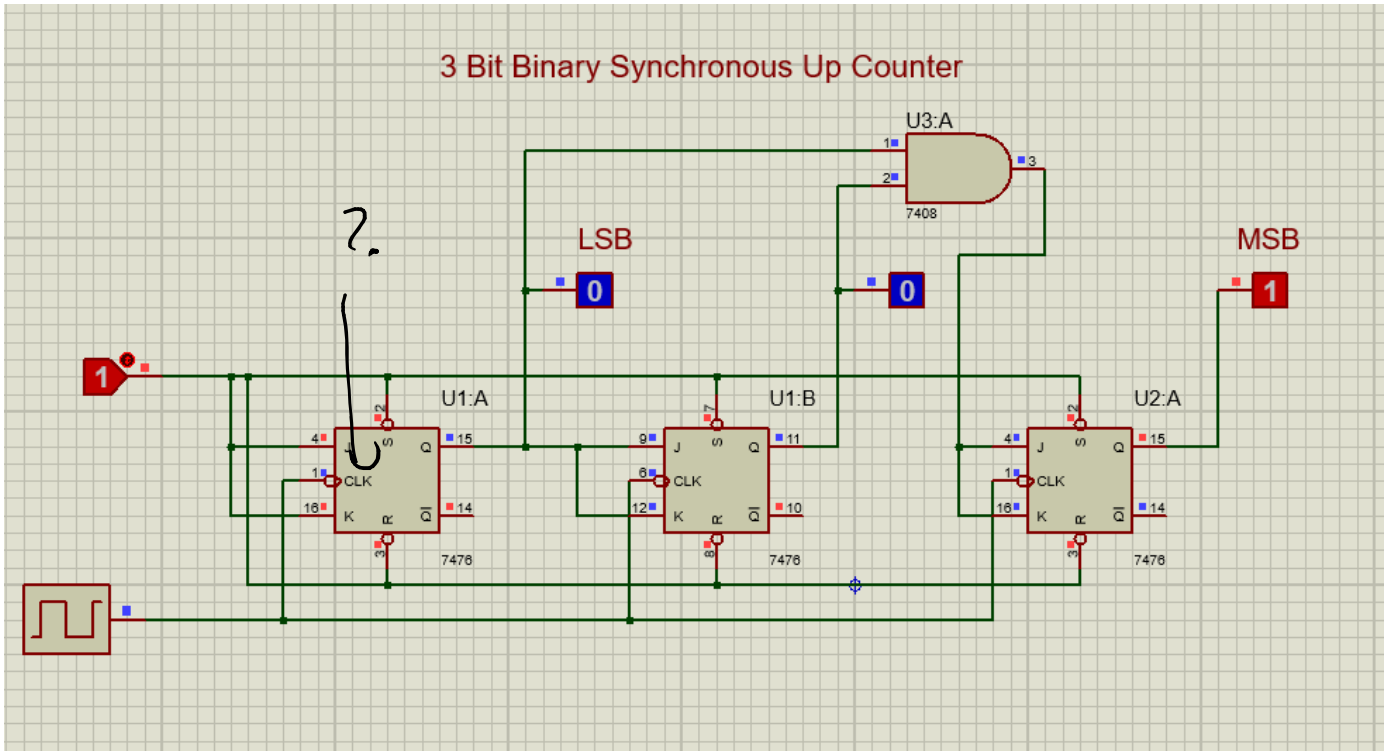


$J_2 = Q_1Q_0$



$K_2 = Q_1Q_0$

Design of 3-bit Synchronous UP Counter



QUICK QUIZ (POLL)

A counter circuit is usually constructed of _____

a) A number of latches connected in cascade form

b) A number of NAND gates connected in cascade form

c) A number of flip-flops connected in cascade

d) A number of NOR gates connected in cascade form

Design of 3-bit Synchronous Down Counter

1) design State table.
2) K-map
3) design

→ (JK F/F)

$J_2 = K_2 = \overline{Q_0}\,\overline{Q_1}$ $\quad J_1 = K_1 = \overline{Q_0}$

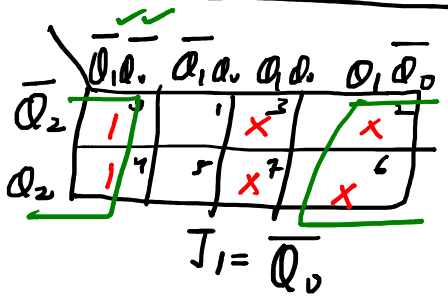
7 → 6 → 5 → 4 → 3 → 2 → 1 → 0

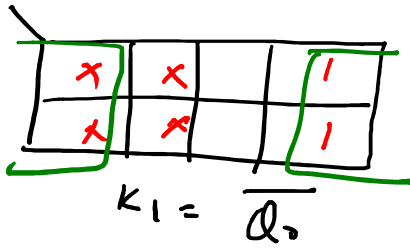
Present State			Next state			Flip Flop Inputs					
Q_2	Q_1	Q_0	$Q_2(t+1)$	$Q_1(t+1)$	$Q_0(t+1)$	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	1	1	1	1	X	1	X	1	X
7	1	1	1	1	0	X	0	X	0	X	1
6	1	1	1	0	1	X	0	X	1	1	X
5	1	0	1	1	0	X	0	0	X	X	1
4	1	0	0	0	1	X	1	1	X	1	X
3	0	1	1	0	1	0	X	X	0	X	1
2	0	1	0	0	0	0	X	X	1	1	X
1	0	0	1	0	0	0	X	0	X	X	1

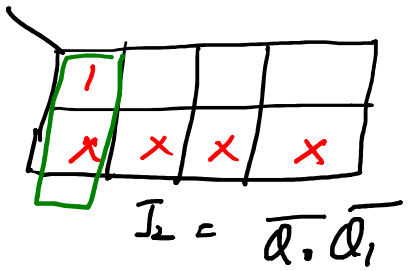
E.T

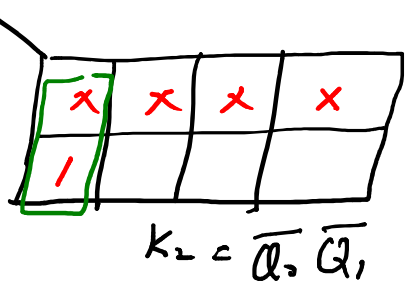
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(2) Step: $J_0 = K_0 = 1$

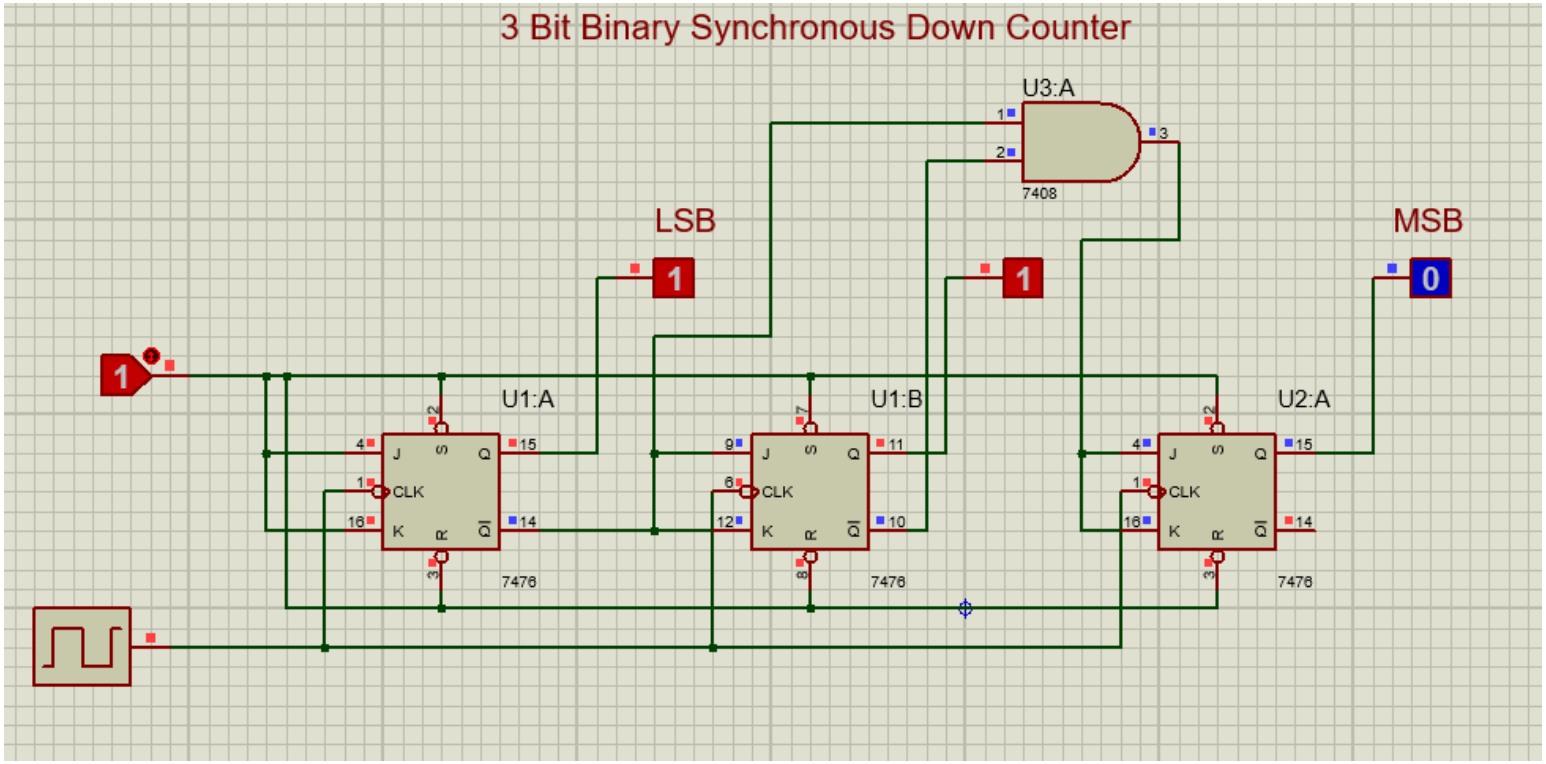








Design of 3-bit Synchronous Down Counter



DIGITAL ELECTRONICS: ECE 213

Topic: Introduction to Counters and its Types

UNIT IV: COUNTERS AND REGISTERS

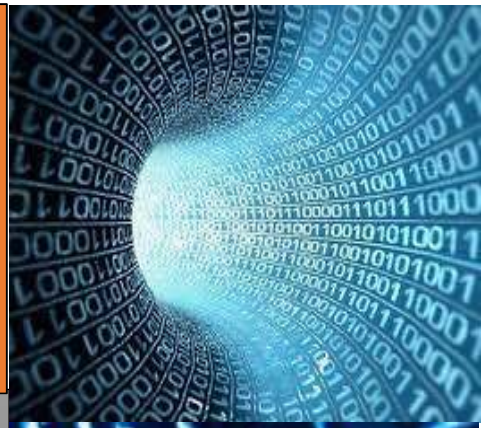
Lecture No.: 35

Prepared By: Irfan Ahmad Pindoo

Assistant Professor

VLSI Design, ECE

School of Computer Science and Engineering



Synchronous Counter with Random Sequence

3 bits = 3 F/F.

- Example: Design a counter with a sequence 4,7,3,0,2,4,..... Using JK FlipFlop?

1) State Table
2) K-maps:
3) Design.

Unused state → 1, 5, 6.
Used state → ✓

State Table:

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
4 → 1	0	0	1	1	1	X	0	1	X	1	X
7 1	1	1	0	1	1	X	1	X	0	X	0
3 0	1	1	0	0	0	0	X	X	1	X	1
0 0	0	0	0	1	0	0	X	1	X	0	X
2 0	1	0	1	0	0	1	X	X	1	0	X

K-map

	$\bar{Q}_1\bar{Q}_0$	$\bar{Q}_1 Q_0$	$Q_1 Q_0$	$Q_1\bar{Q}_0$
$\bar{Q}_2$	0	X 1	3	1
Q_2	X 4	X 5	X 7	X 6

$J_2 = Q_1\bar{Q}_0$

Yourself!

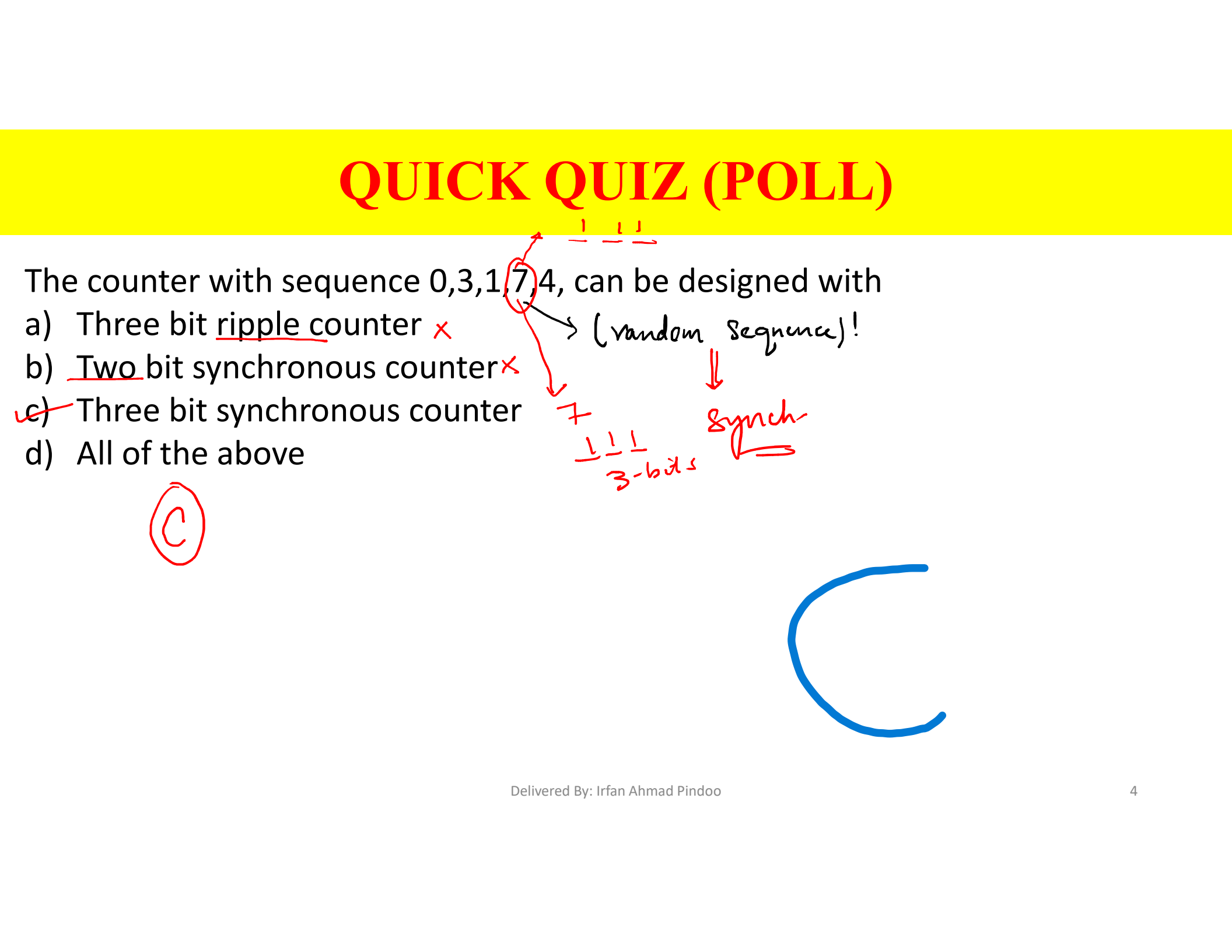
E.T

		J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

QUICK QUIZ (POLL)

The counter with sequence 0,3,1,7,4, can be designed with

a) Three bit ripple counter
b) Two bit synchronous counter
c) Three bit synchronous counter
d) All of the above

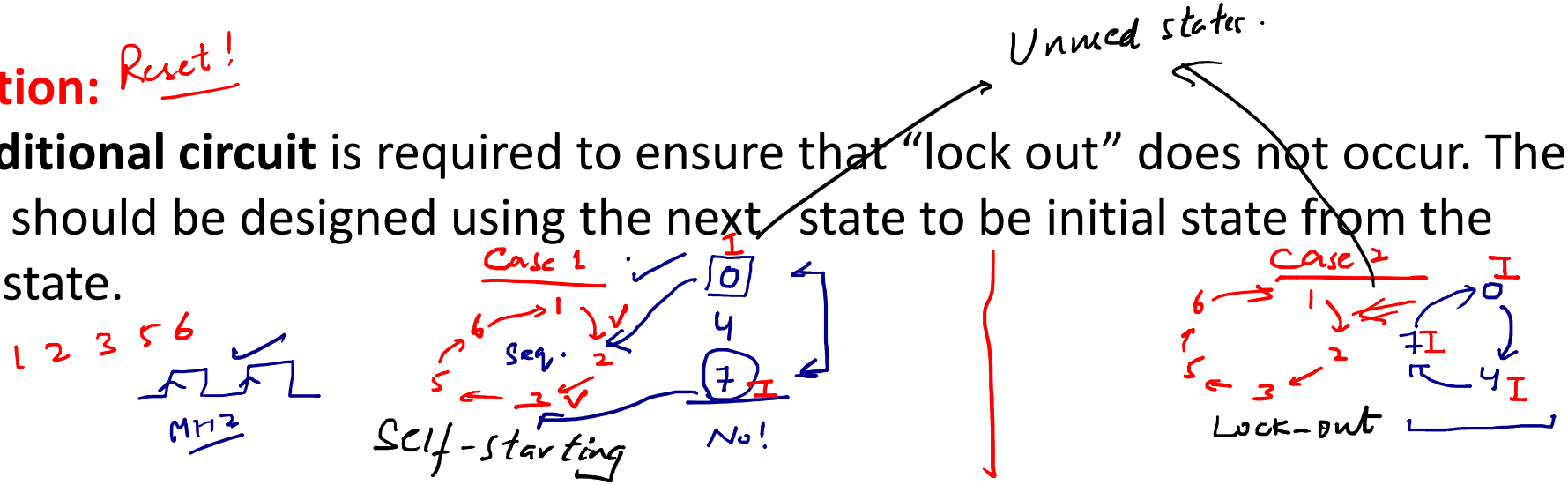


Lock Out condition in Synchronous Counters

- Sometimes a counter may find itself in some unused states.
- It happens when the next state of some unused state is again some unused one and if by chance the counter happens to find itself in some unused state and never arrives at in used state then this condition is called “Lock Out”.

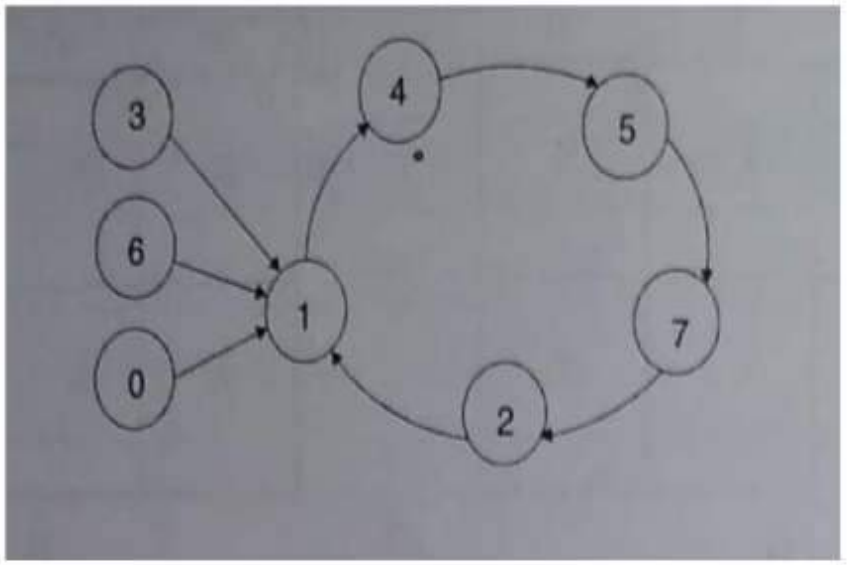
- **Solution:** Reset!

An **additional circuit** is required to ensure that “lock out” does not occur. The counter should be designed using the next state to be initial state from the unused state.



Lock Out condition in Synchronous Counters

- To avoid lock out condition the unused states are introduced in front of used states.
- From the given state diagram: 1,4,5,6 and 7 is the sequence and unused states are 0,3 and 6.



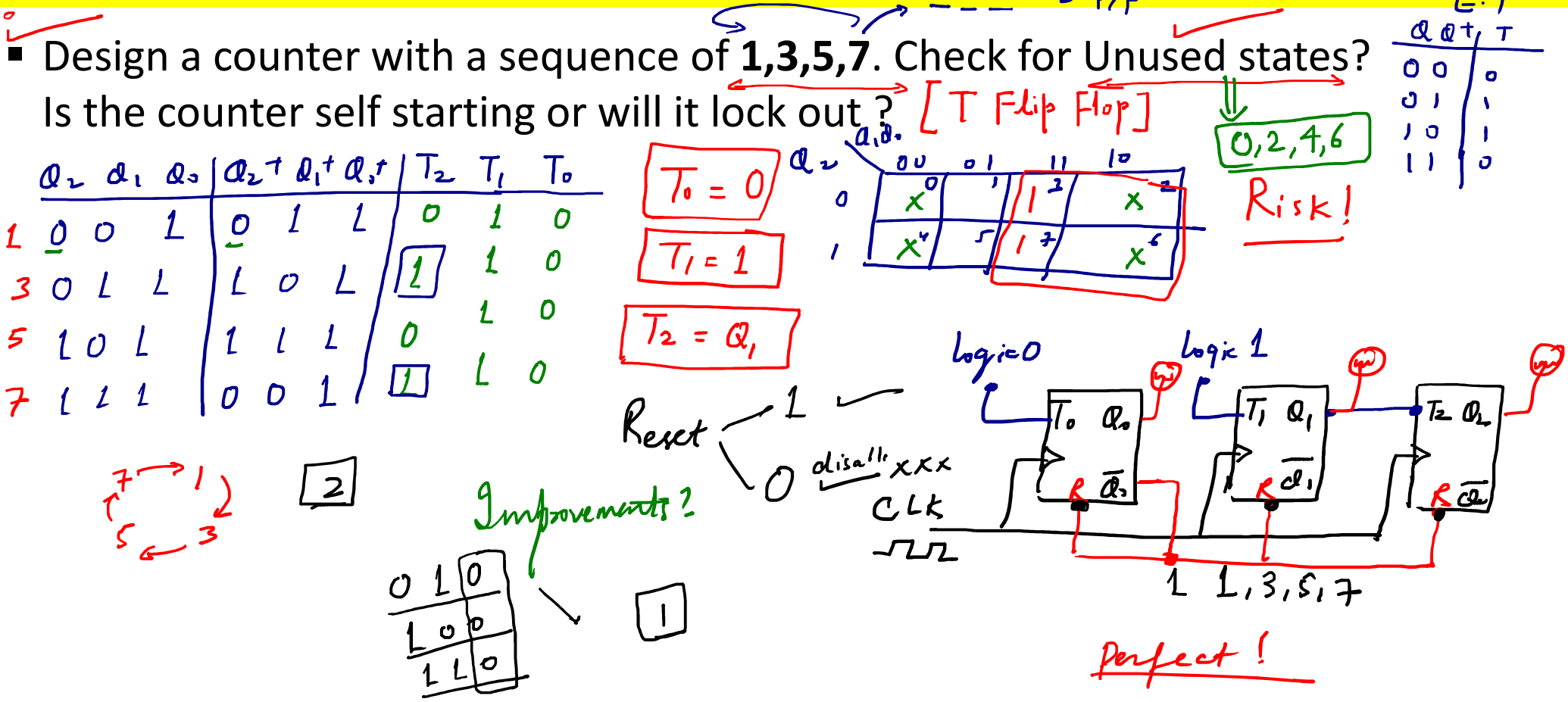
QUICK QUIZ (POLL)

Identify the correct statement?

a) In lock out condition, the counter rests at zero.
b) There is no lock out condition in synchronous counters.
c) In lock out condition, the counter does not return to its original sequence.
d) Both b and c

Lock Out condition in Synchronous Counters

- Design a counter with a sequence of **1,3,5,7**. Check for Unused states? Is the counter self starting or will it lock out ?



Lock Out condition in Synchronous Counters

- Design a counter with a sequence of **1,3,5,7**. Check for Unused states? Is the counter self starting or will it lock out?

Unused states: 0, 2, 4, 6

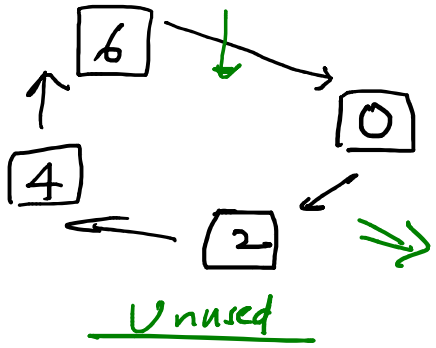
Checking for Unused States:-

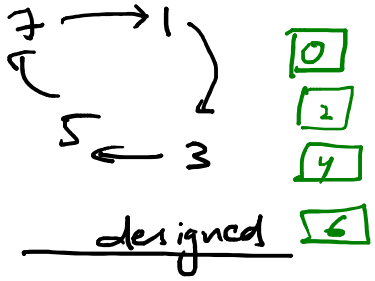
Q_2	Q_1	Q_0	T_2	T_1	T_0	Q_2^+	Q_1^+	Q_0^+
⇒ 0	0	0	0	1	0	0	1	0
0	1	0	1	1	0	1	0	0
→ 1	0	0	0	1	0	1	1	0
1	1	0	1	1	0	0	0	0

Charac-Table:-

T	Q	Q^+

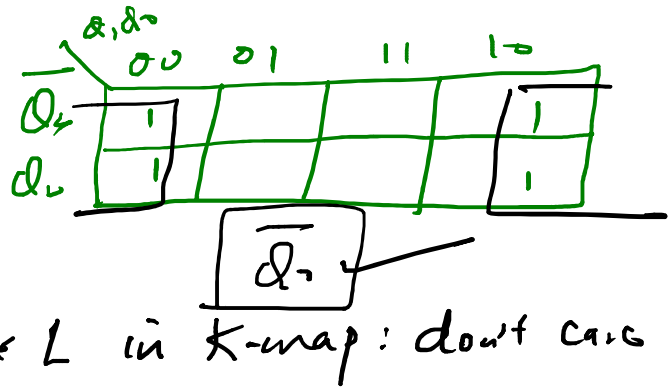
$Q^+ = T \oplus Q$ (XOR)





Lock Out condition in Synchronous Counters

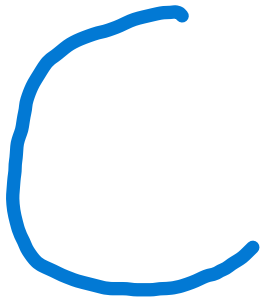
- Design a counter with a sequence of **1,3,5,7**. Check for Unused states? Is the counter self starting or will it lock out ?
- Modify the Design to eliminate lock out condition?



QUICK QUIZ (POLL)

Which of the following counting sequence will produce lock out condition for 3 bit synchronous counter design?

a) 0, 1, 2, 3,4,5,6,7
b) 1,2,5,7,6,3
c) 0,2,4,6
d) 7,3,6,5,1,0,4,2



DIGITAL ELECTRONICS: ECE 213

Topic: Introduction to Registers and its Types

UNIT V: COUNTERS AND REGISTERS

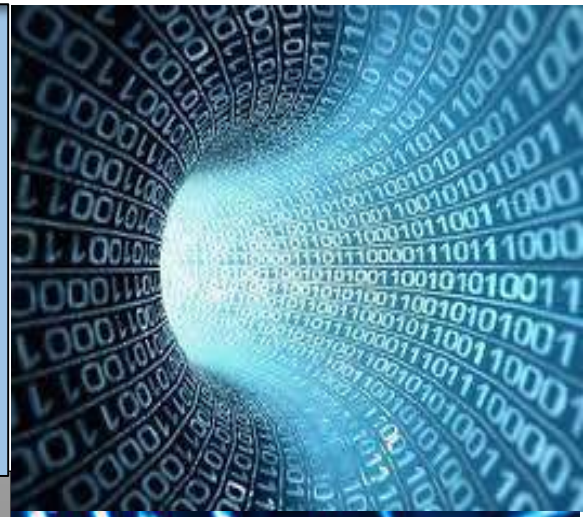
Lecture No.: 36

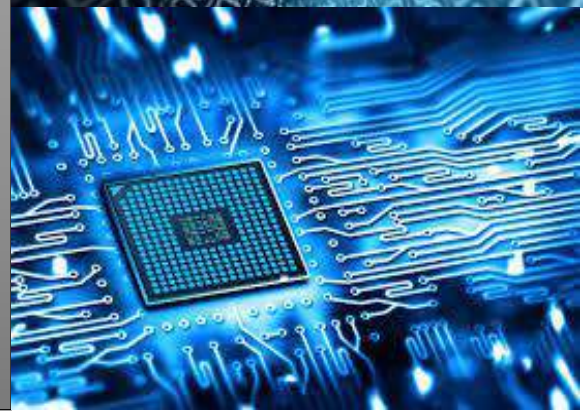
Prepared By: Irfan Ahmad Pindoo

Assistant Professor

VLSI Design, ECE

School of Computer Science and Engineering





Introduction to Registers

- A *register* is a group of flip-flops, each one of which shares a common clock and is capable of storing one bit of information.
- An *n*-bit register consists of a group of *n* flip-flops capable of storing *n* bits of binary information.
- In its broadest definition, a register consists of a group of flip-flops together with gates that affect their operation. The flip-flops hold the binary information, and the gates determine how the information is transferred into the register.

Applications of Registers

- Shift register is used as Parallel to serial converter, which converts the parallel data into serial data. It is utilized at the transmitter section after Analog to Digital Converter ADC block.

- Shift register is used as Serial to parallel converter, which converts the serial data into parallel data. It is utilized at the receiver section before Digital to Analog Converter DAC block.

- Shift register along with some additional gates generate the sequence of zeros and ones. Hence, it is used as sequence generator.

- Shift registers are also used as counters. There are two types of counters based on the type of output from right most D flip-flop is connected to the serial input. Those are Ring counter and Johnson Ring counter.

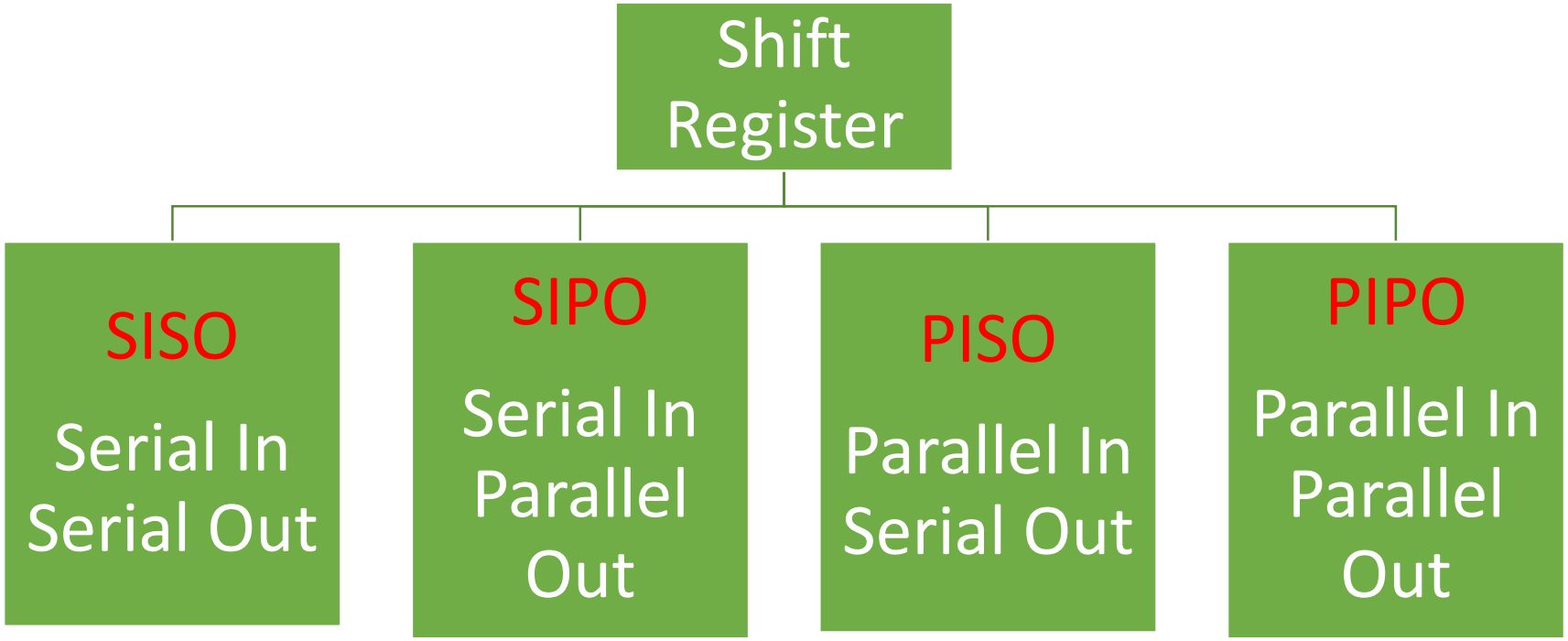
Shift Register and its Types

- Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format.

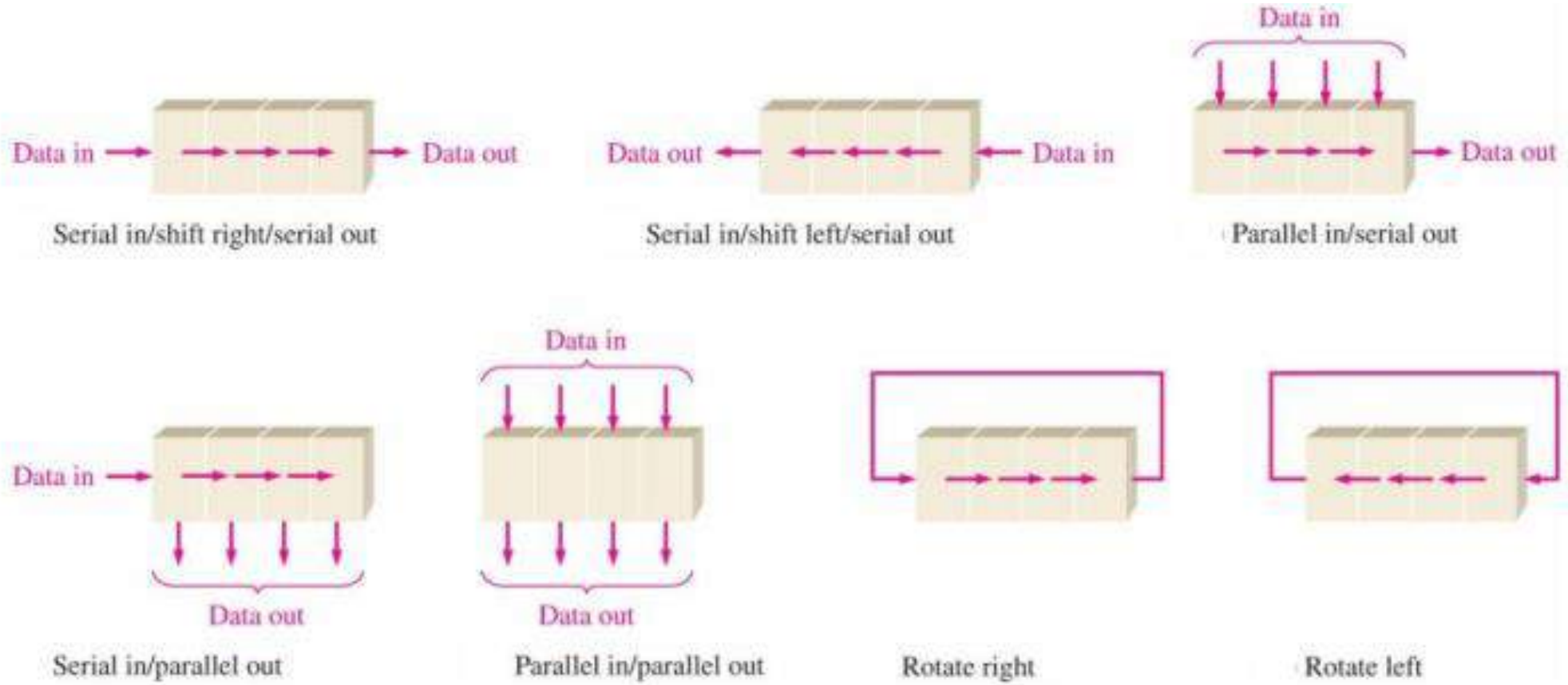
- The individual data latches that make up a single shift register are all driven by a common clock (CLK) signal making them synchronous devices.

- This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name Shift Register.

Shift Register and its Types



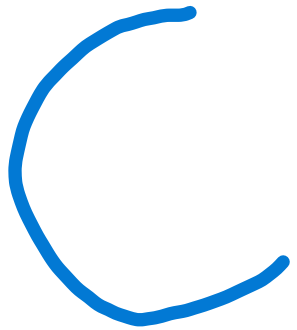
Shift Register and its Types



QUICK QUIZ (POLL)

Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.

a) 2
b) 3
c) 4
d) 5



QUICK QUIZ (POLL)

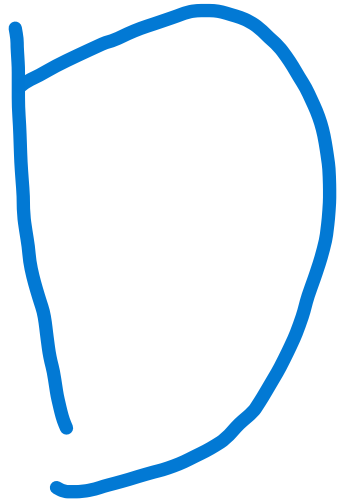
The full form of SIPO is _____

a) System-in Parallel-out

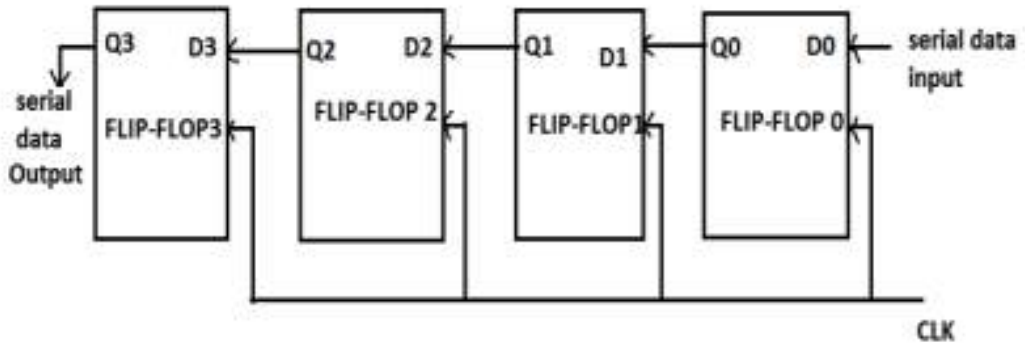
b) Parallel-in Serial-out

c) Serial-In Peripheral-Out

d) Serial In Parallel Out



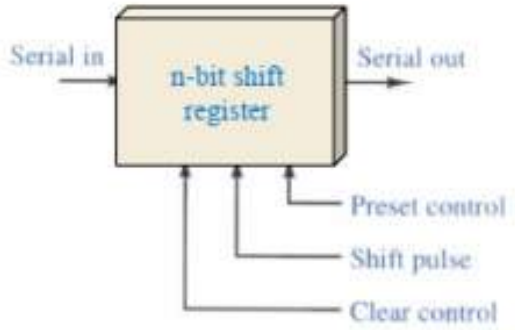
Serial In Serial Out (SISO) Shift Register

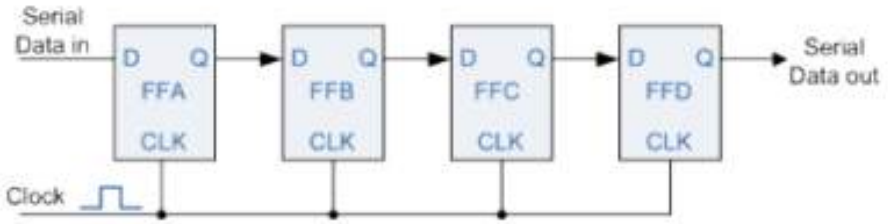


CLK	Q3	Q2=D3	Q1=D2	Q0=D1	SERIAL INPUT Din=D0
	0	0	0	0	
↓	0	0	0	1 ←	1
↓	0	0	1	1 ←	1
↓	0	1	1	1 ←	1
↓	1	1	1	1 ←	1

Serial In Serial Out (SISO) Shift Register

- Data bits come in one at a time and leave one at a time
- One Flip-Flop for each bit to be handled
- Movement can be left or right, but is usually only a single direction in a given register
- Asynchronous preset and clear inputs are used to set initial values





Serial In Serial Out (SISO) Shift Register

Timing Diagram

CLK	Q3	Q2=D3	Q1=D2	Q0=D1	SERIAL INPUT Din=D0
	0	0	0	0	
↓	0	0	0	1	1
↓	0	0	1	1	1
↓	0	1	1	1	1
↓	1	1	1	1	1

Practice Problem

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)

a) 1100
b) 0011
c) 0000
d) 1111

QUICK QUIZ (POLL)

With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in _____

a) 4 µs
b) 40 µs
c) 400 µs
d) 40 ms

B

Practice Problem

The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____

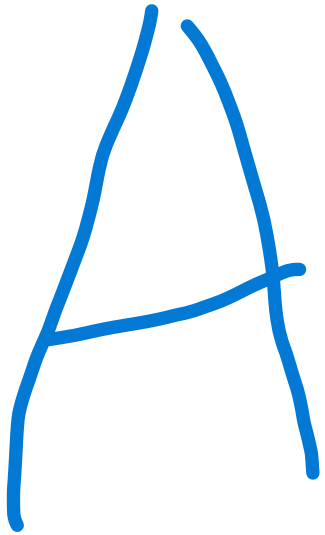
a) 01110
b) 00001
c) 00101
d) 00110

QUICK QUIZ (POLL)

A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains

_____

a) 0111
b) 1111
c) 0000
d) 1000



DIGITAL ELECTRONICS: ECE 213

Topic: Introduction to Registers and its Types

UNIT V: COUNTERS AND REGISTERS

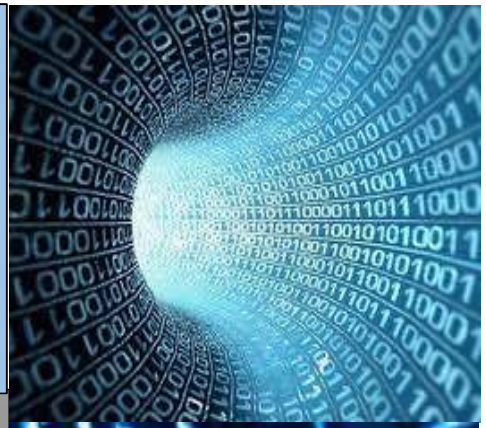
Lecture No.: 37

Prepared By: Irfan Ahmad Pindoo

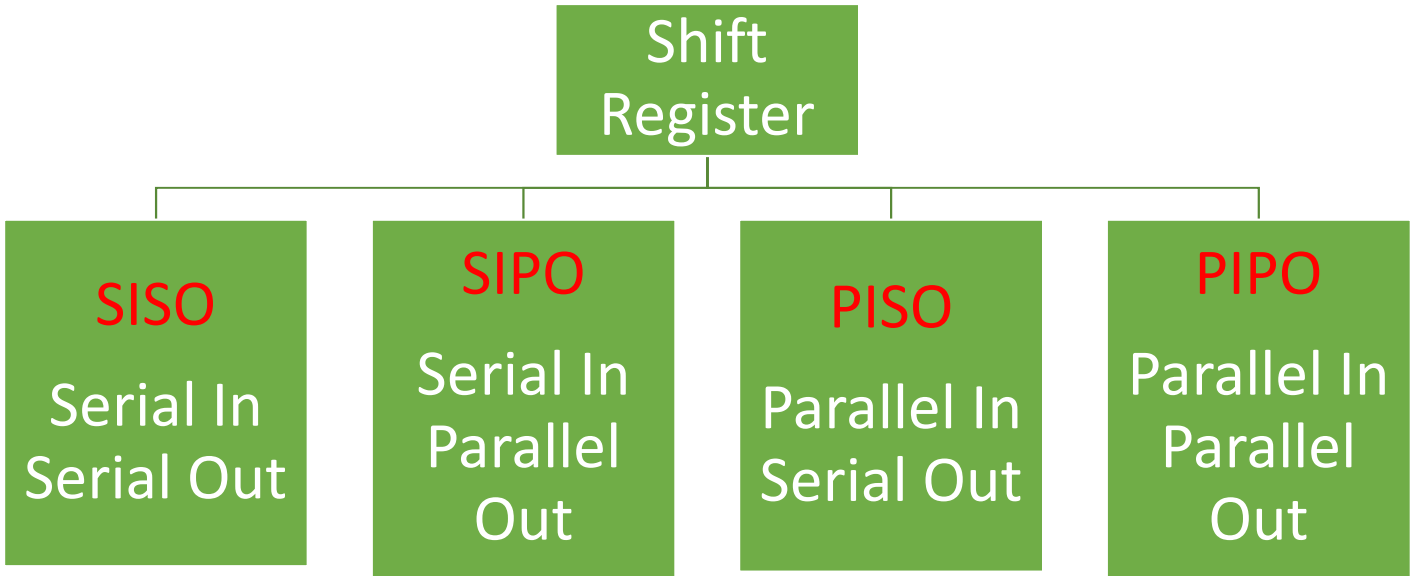
Assistant Professor

VLSI Design, ECE

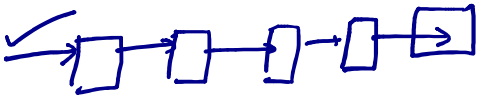
School of Computer Science and Engineering

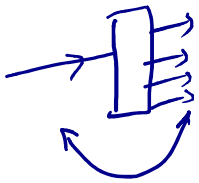


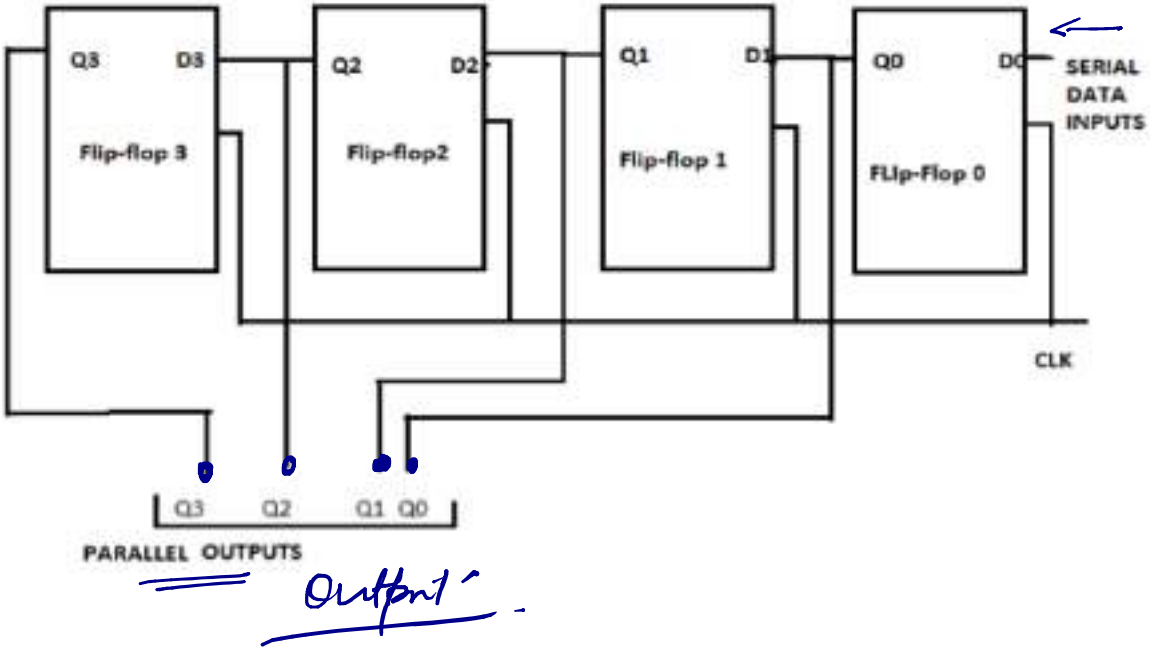
Shift Register and its Types



Serial In Parallel Out (SIPO) Shift Register







1011

enter data inside ffs: 4

my O/P :- 4

Output.

Parallel In Serial Out (PISO) Shift Register

- The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as Parallel-In Serial-Out shift register.

Parallel In Serial Out (PISO) Shift Register

loading the data

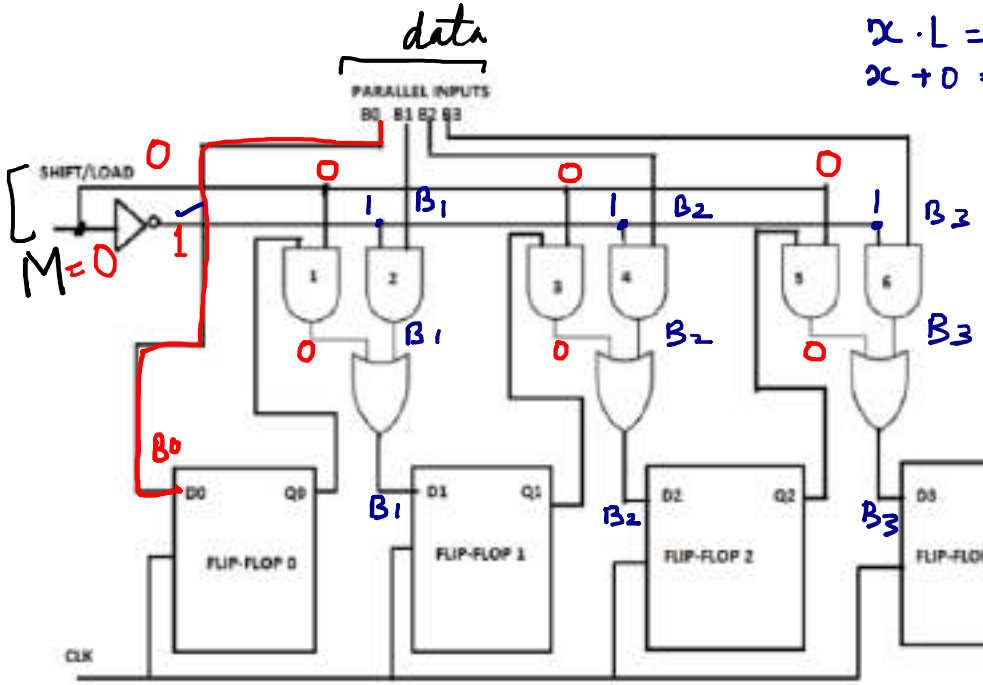
Load Operation: M=0

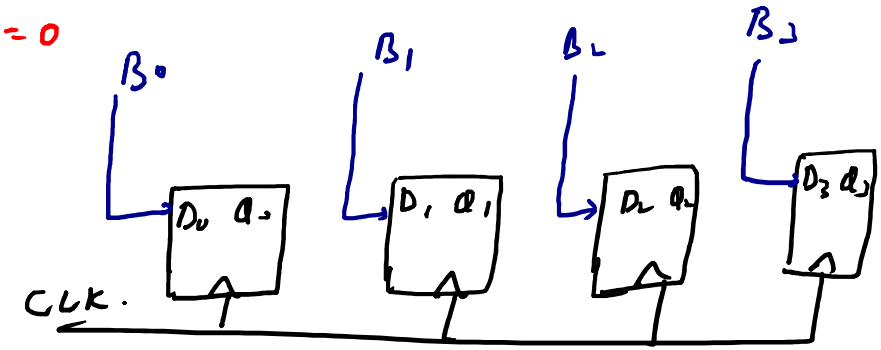
2, 4, 6 : data ✓ : ON, M = 0

1, 3, 5 : o/p = 0

x · 1 = x

x + 0 = x





loading ✓ Shifting ✗

Parallel In Serial Out (PISO) Shift Register

Shift Operation:

M = 1 :

Gates: 2, 4, 6 : turned-off

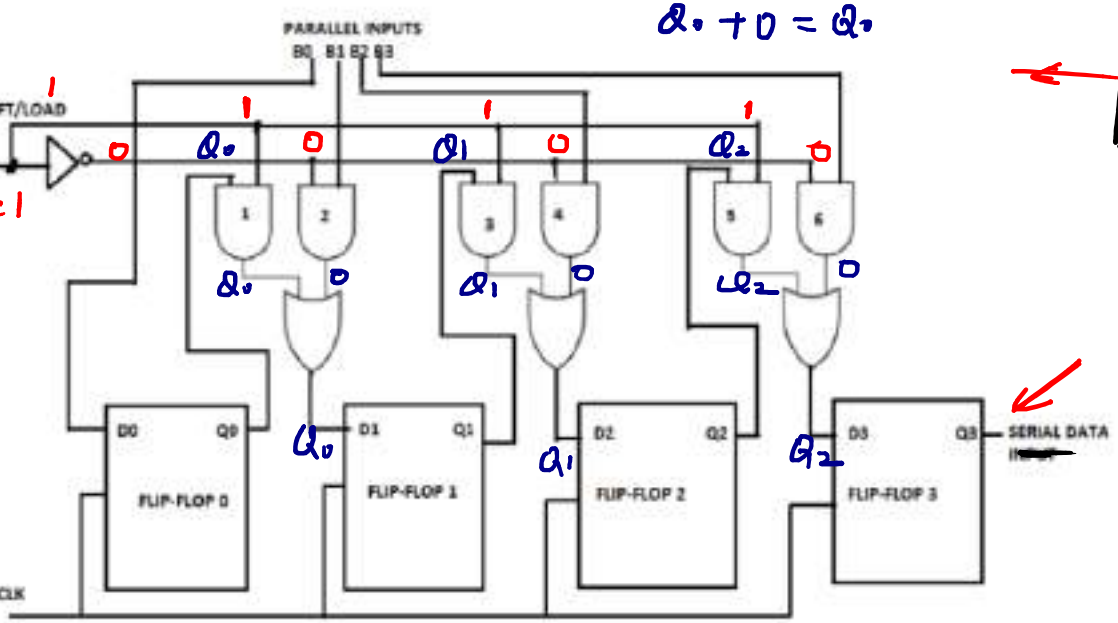
Gates: 1, 3, 5 : ON!

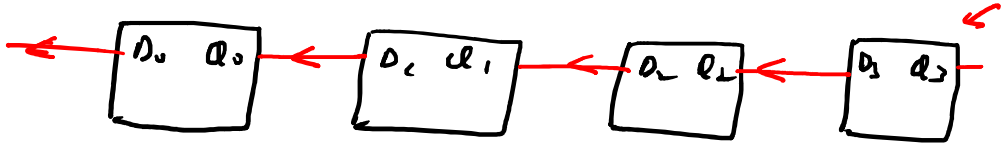
$Q_0 \cdot 1 = Q_0$

$Q_0 + 0 = Q_0$

Shifting ✓

Loading X.

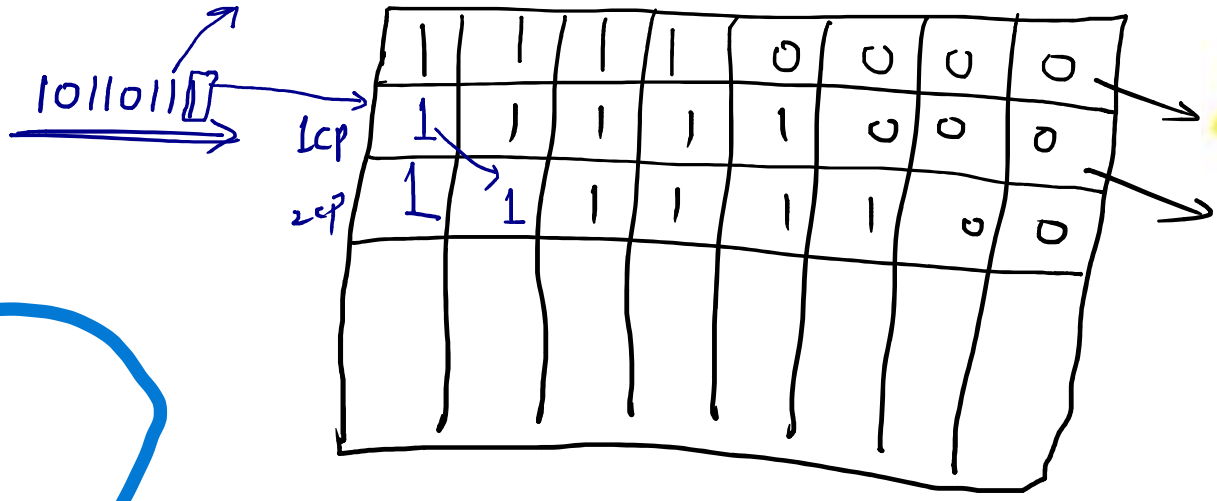


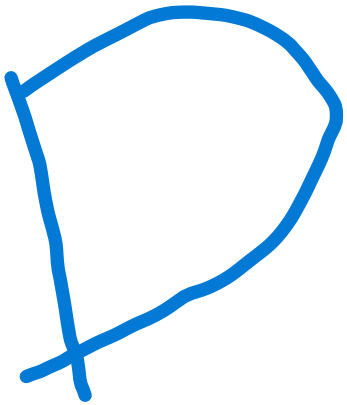


QUICK QUIZ (POLL)

The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains _____

a) 10111000
b) 10110111
c) 11110000
d) 11111100





QUICK QUIZ (POLL)

How can parallel data be taken out of a shift register simultaneously?

a) Use the Q output of the first FF ×

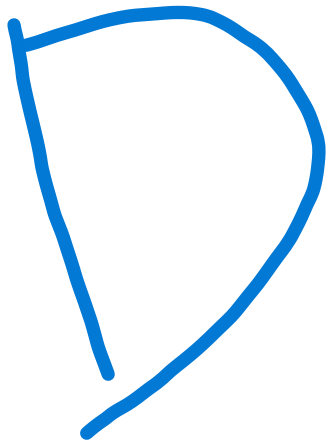
b) Use the Q output of the last FF ×

c) Tie all of the Q outputs together ×

d) Use the Q output of each FF ✓

Parallel out

× Shifting



DIGITAL ELECTRONICS: ECE 213

Topic: Introduction to Registers and its Types

UNIT V: COUNTERS AND REGISTERS

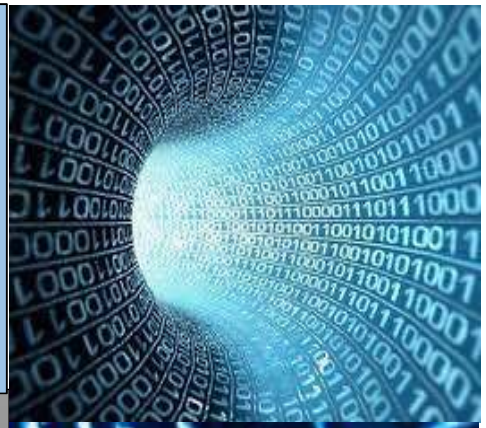
Lecture No.: 38

Prepared By: Irfan Ahmad Pindoo

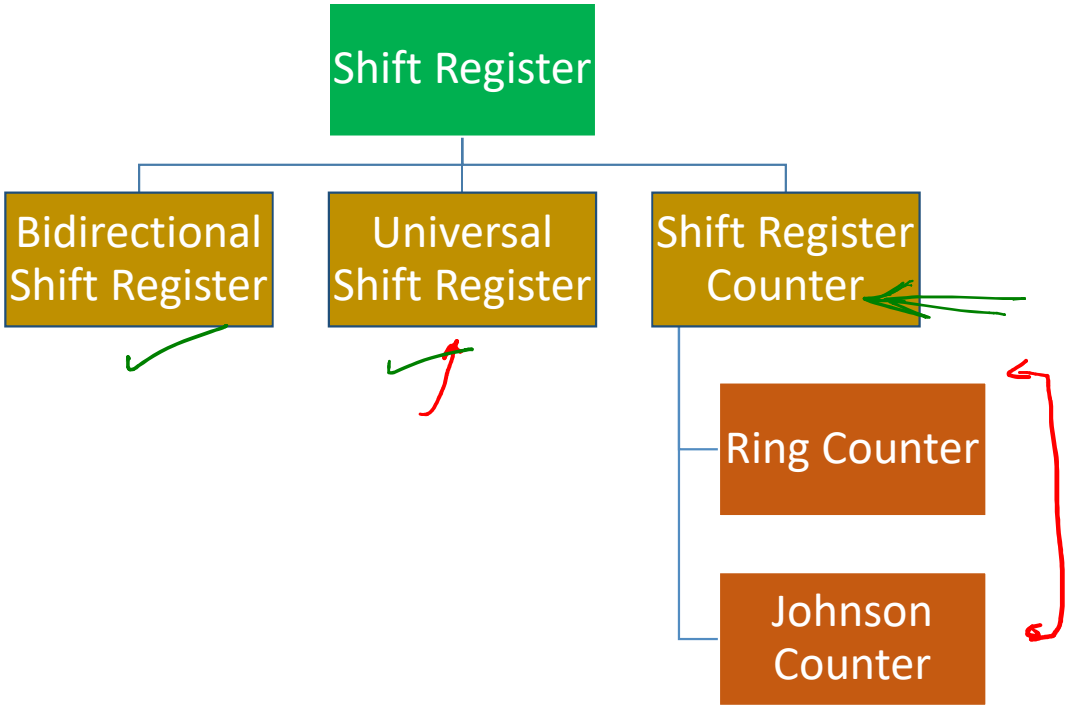
Assistant Professor

VLSI Design, ECE

School of Computer Science and Engineering



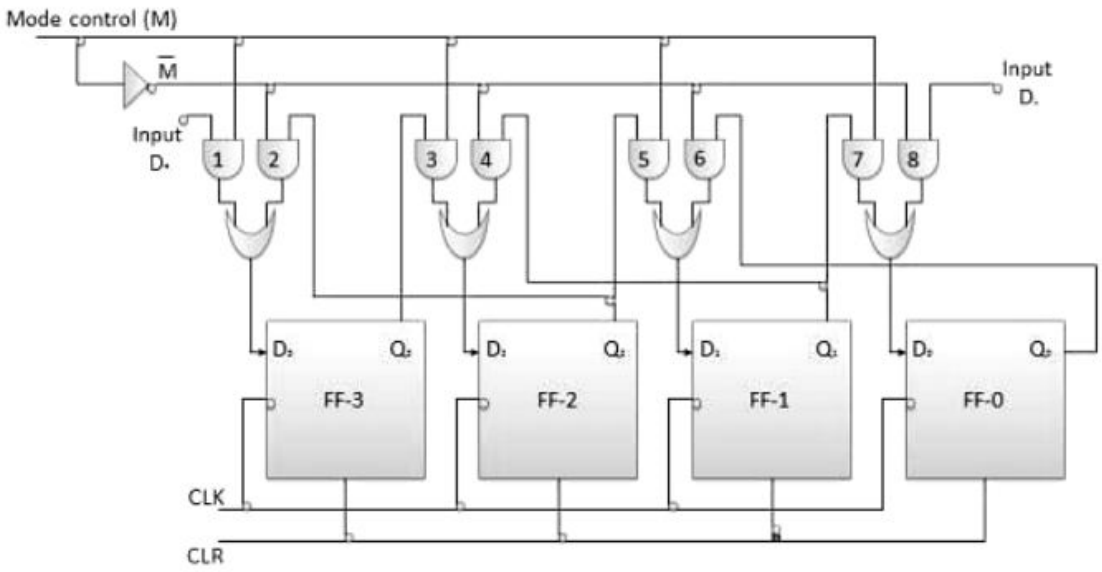
Shift Register Other Types



Bidirectional Shift Register

- Bidirectional shift registers are the storage devices which are capable of shifting the data either right or left depending on the mode selected.

- If the mode selected is 1(high), the data will be shifted towards the right direction and
- if the mode selected is 0(low), the data will be shifted towards the left direction.



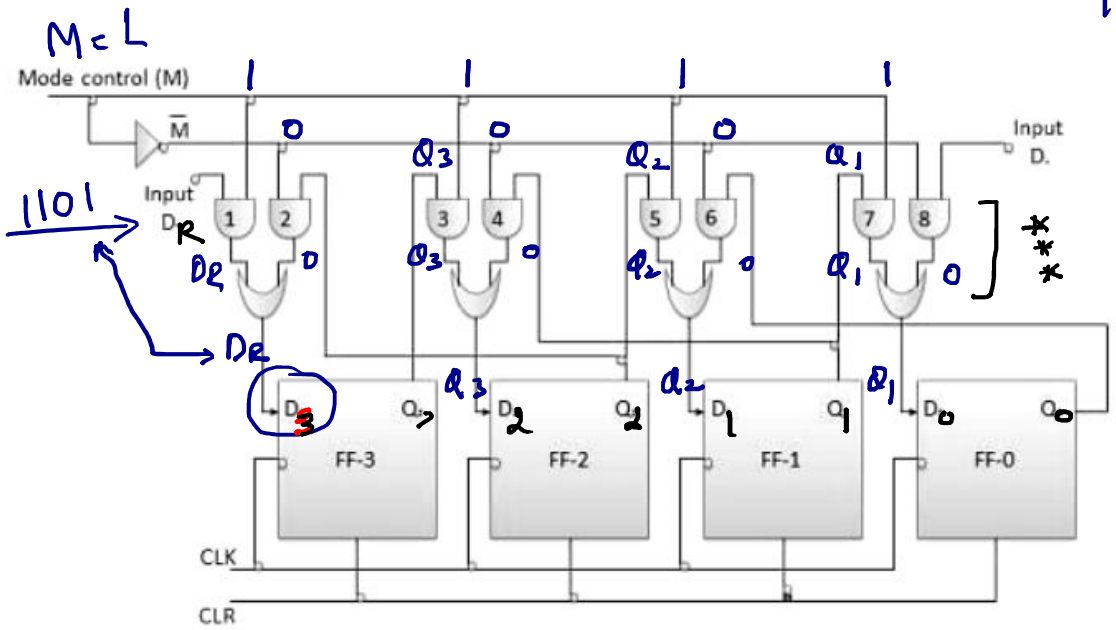
Bidirectional Shift Register

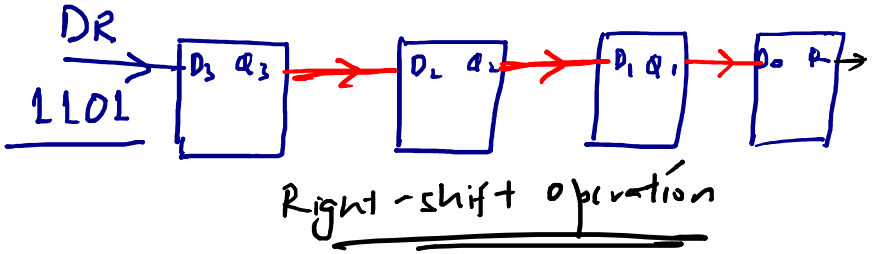
Right Shift Operation:

M = 1 :

Gates 2, 4, 6, 8 :- off

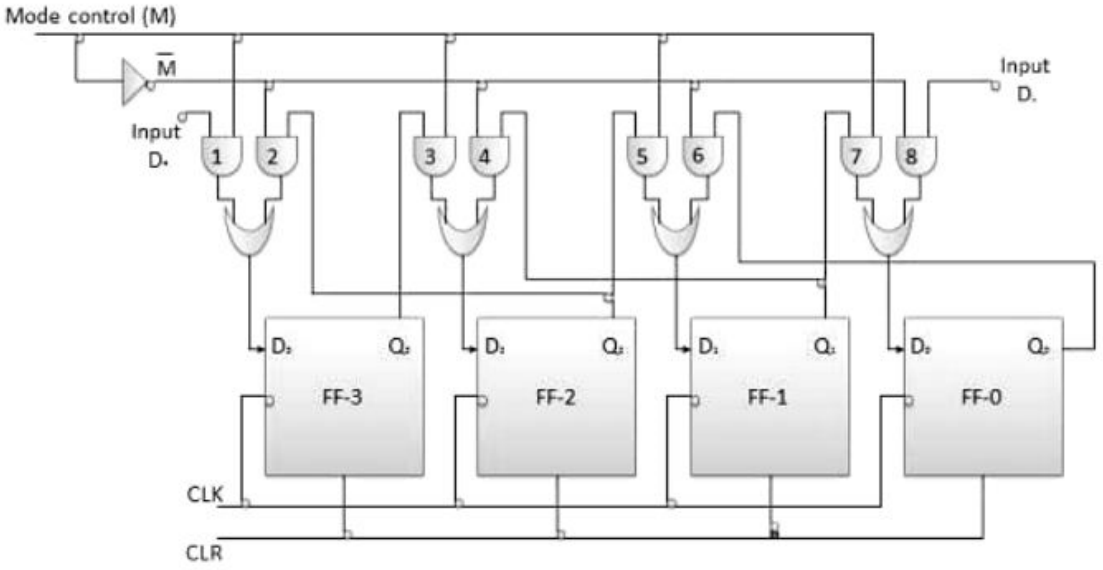
Gates 1, 3, 5, 7 :- on





Bidirectional Shift Register

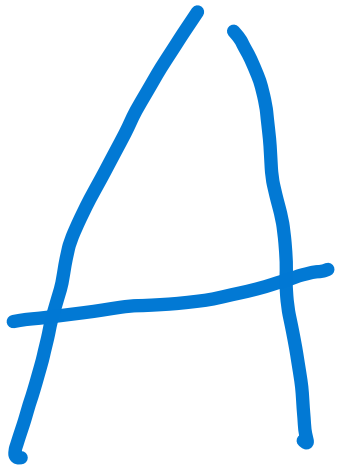
Left Shift Operation:



QUICK QUIZ (POLL)

For a bidirectional shift register discussed here, what will happen if the mode value selected is 1:

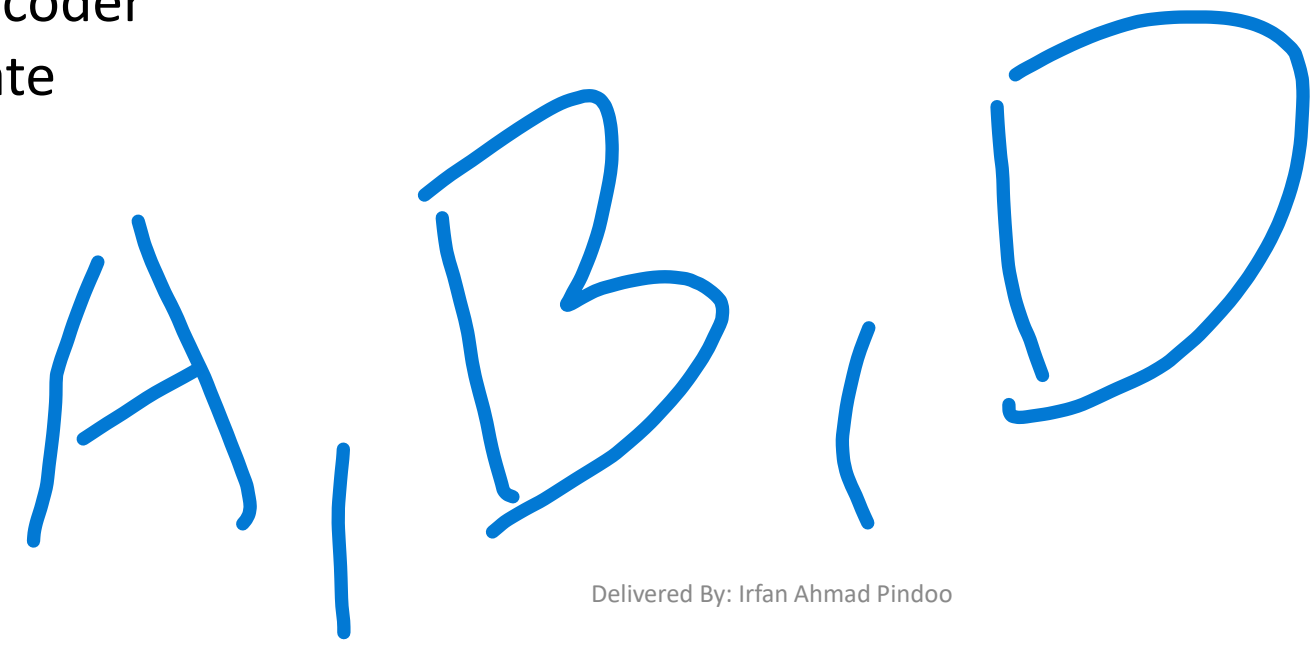
a) Data movement towards right.
b) Data movement towards right
c) NO change
d) Parallel loading



QUICK QUIZ (MSQ)

Which of the following combinational gates is required for the operation of bidirectional shift register?

- ❑ AND with OR gates
- ❑ 2X1 multiplexer
- ❑ 4X2 encoder
- ❑ XOR gate

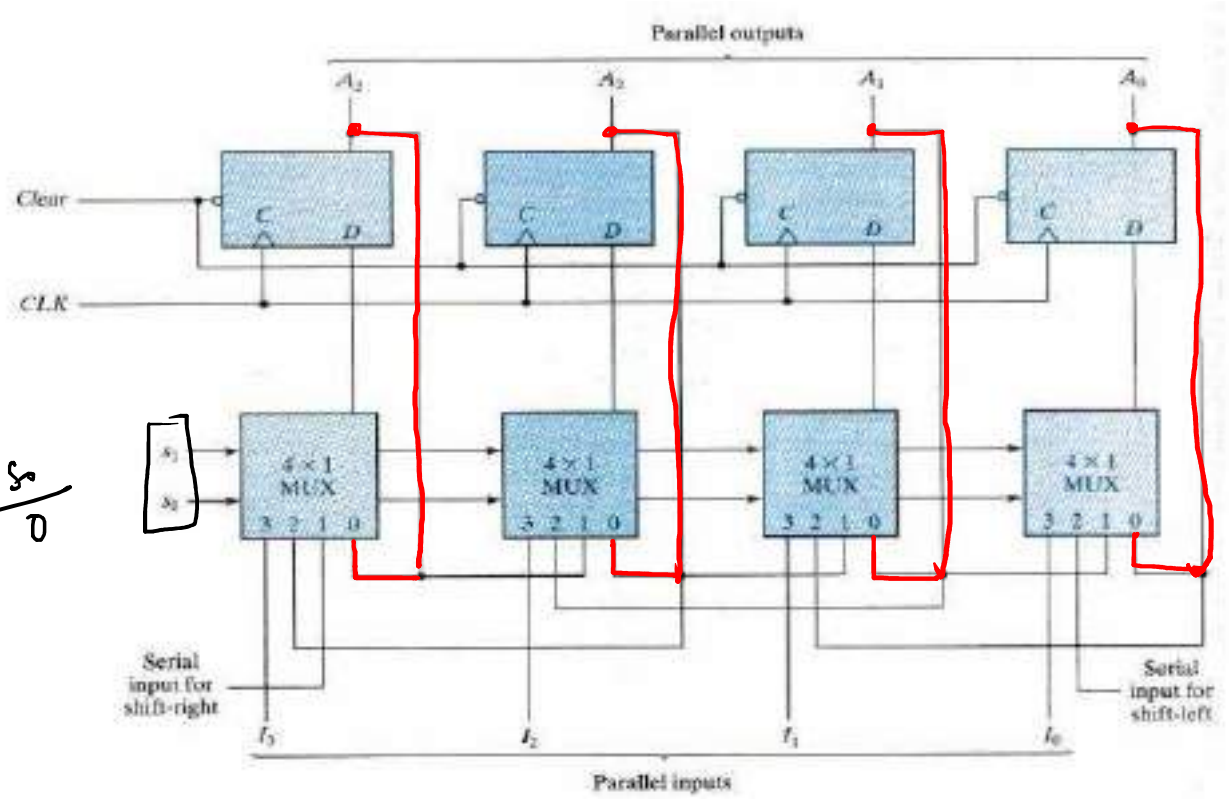


Universal Shift Register

- A register that can store the data and /shifts the data towards the right and left along with the parallel load capability is known as a universal shift register.
- It can be used to perform input/output operations in both serial and parallel modes.
- Unidirectional shift registers and bidirectional shift registers are combined together to get the design of the universal shift register.

Universal Shift Register

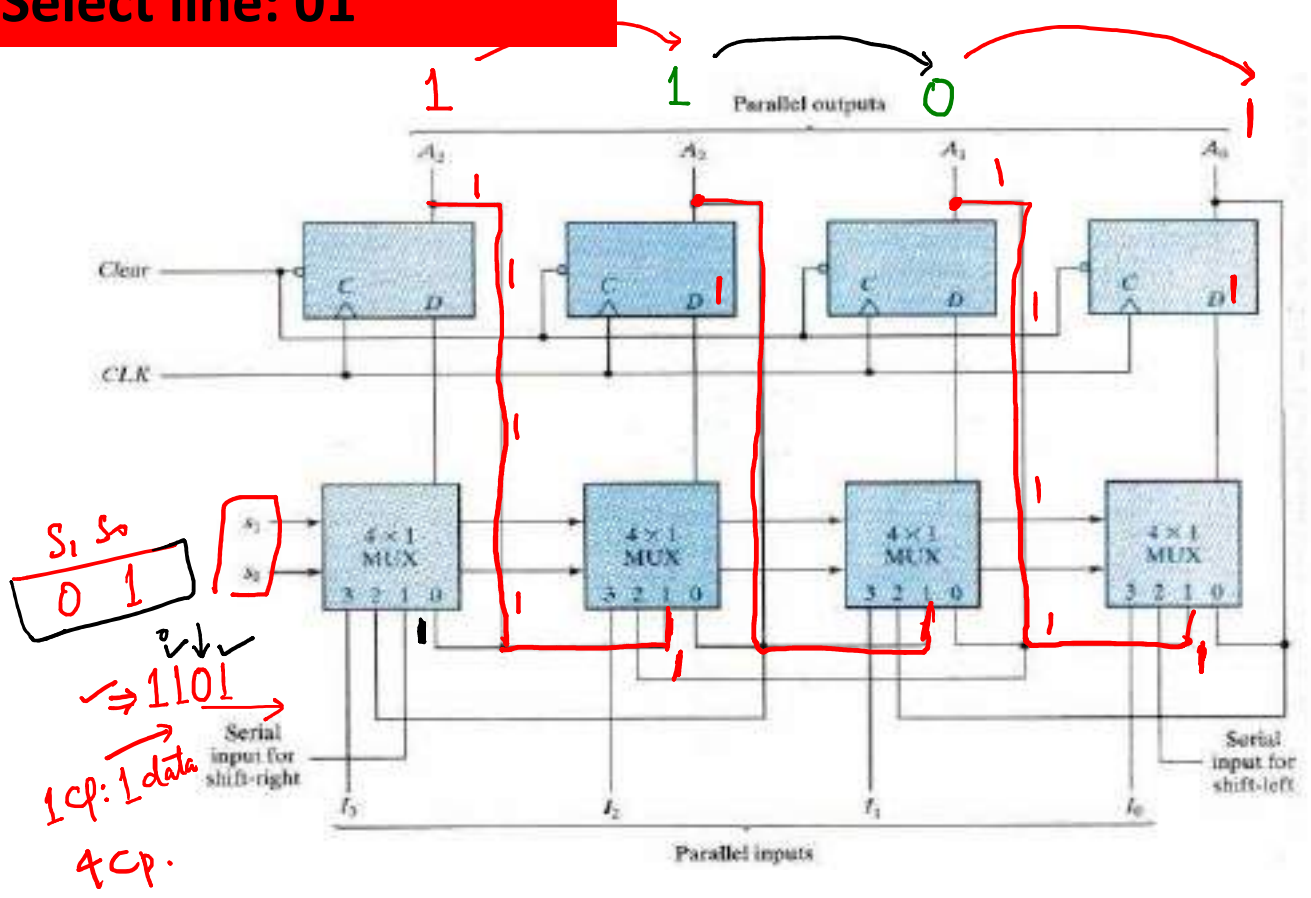
Select line: 00



S_0	S_1	Mode of operation
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Loading

Universal Shift Register

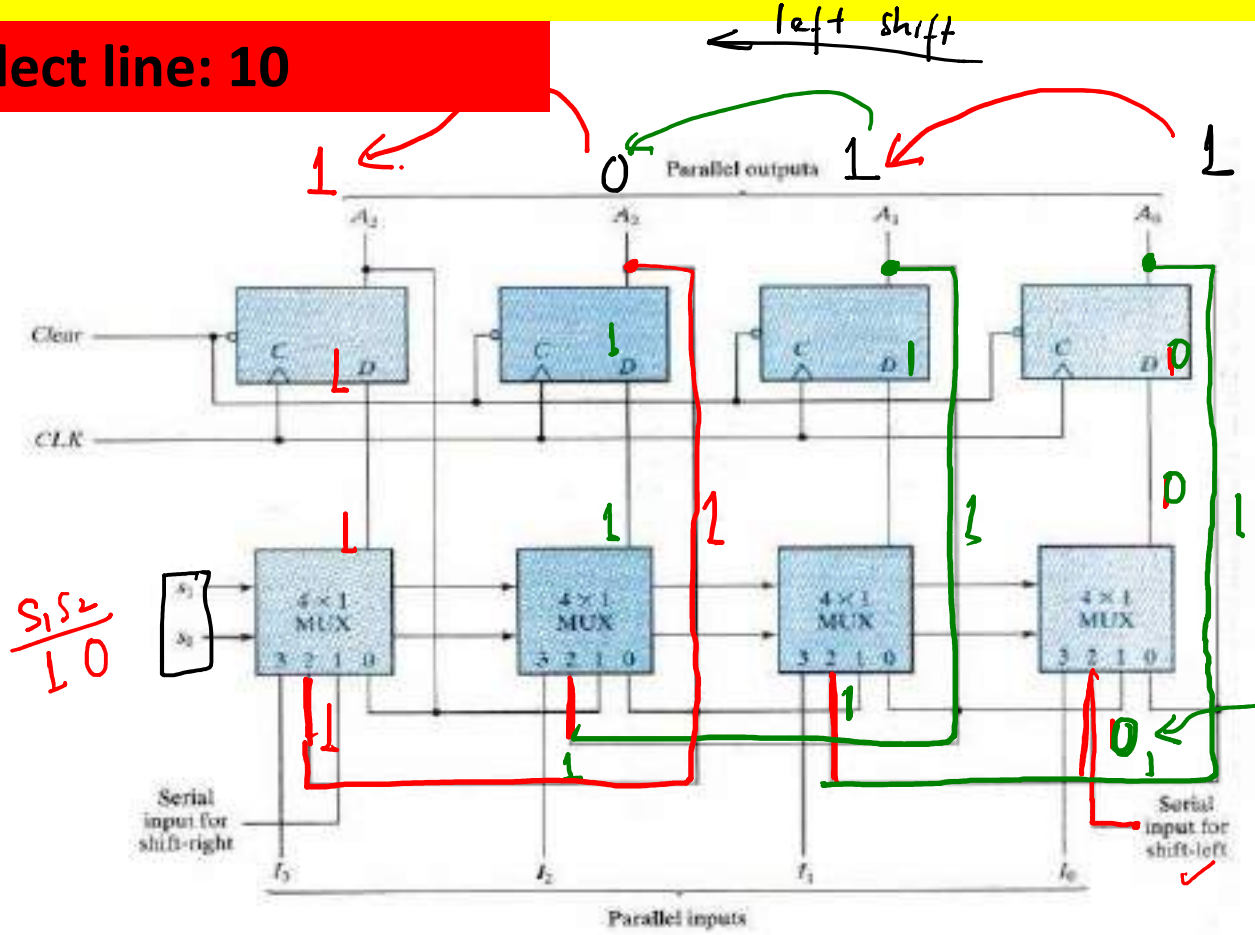
Select line: 01



S_0	S_1	Mode of operation
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Loading

Universal Shift Register

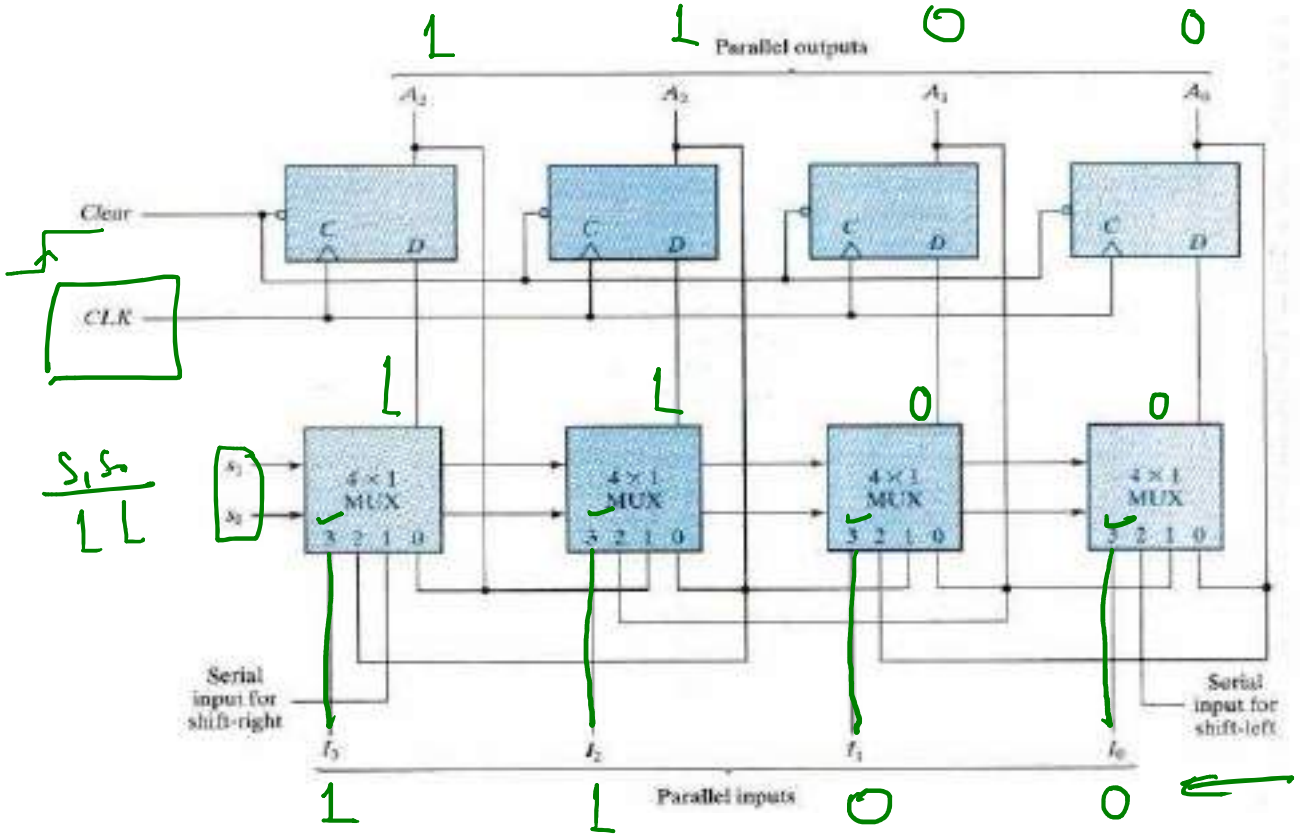
Select line: 10



S_1	S_0	Mode of operation
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Loading

Universal Shift Register

Select line: 11



S_0	S_1	Mode of operation
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Loading

QUICK QUIZ (POLL)

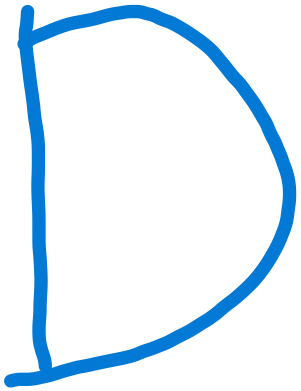
How can parallel data be taken out of a shift register simultaneously?

a) Use the Q output of the first FF

b) Use the Q output of the last FF

c) Tie all of the Q outputs together

d) Use the Q output of each FF



Universal Shift Register: Applications

- Used as a serial-to-serial converter
- Used as a parallel-to-parallel data converter
- Used as a serial-to-parallel data converter.
- Used in serial – to – serial data transfer
- Used in parallel data transfer.
- Used in micro-controllers for I/O expansion
- Used as a memory element in digital electronics like computers.
- Used in time delay applications
- Used as frequency counters, binary counters, and Digital clocks
- Used in data manipulation applications.

QUICK QUIZ (POLL)

A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?

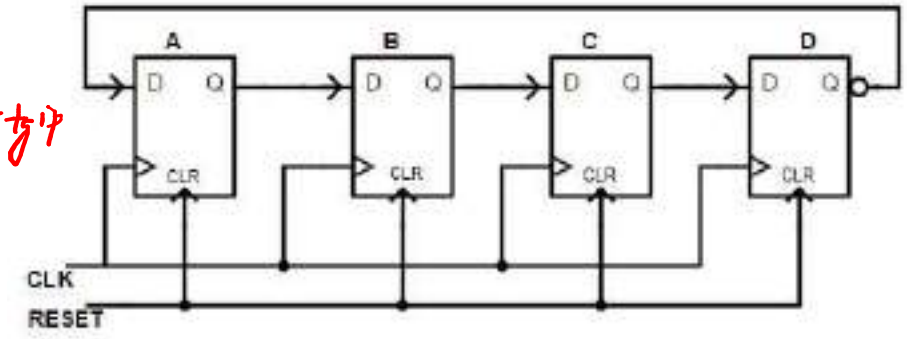
a) Tristate
b) End around
c) Universal
d) Conversion

C

Ring Counter

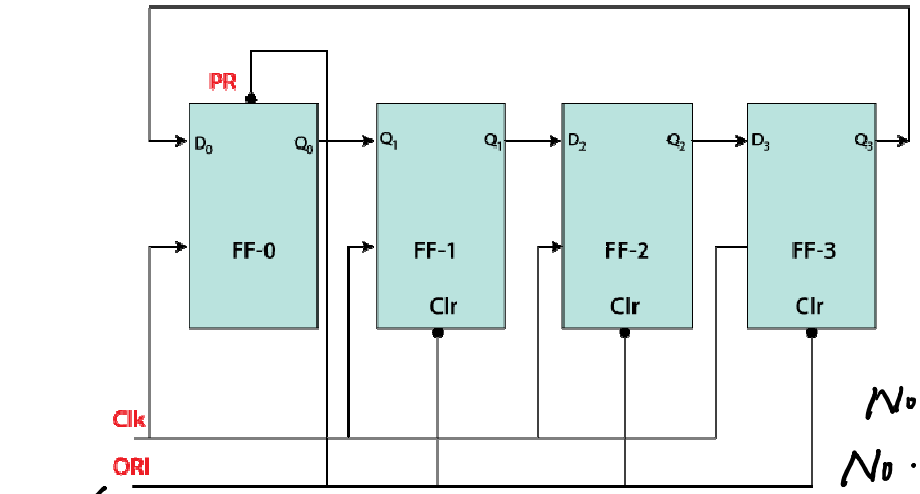
- If we apply a serial data signal to the input of a **Serial-in to Serial-out** Shift Register, the same sequence of data will exit from the last flip flop in the register chain.
- But what if we were to connect the **output of this shift register back to its input** so that the output from the last flip-flop, Q_D becomes the input of the first flip-flop, Q_A. We would then have a closed loop circuit that "recirculates" the same bit of DATA around a continuous loop for every state of its sequence, and this is the principal operation of a Ring Counter.

1) SISO Register
2) Shift Right
* feedback: Q last stage → 1st stage



Operation of Ring Counter

- Initial state: 0000
- We want to enter '1' in a Ring Counter
- ORI — enable: LOOD
  - disable: so that o/p ∝ I/ps. CLK.



Over riding Input

	Q_0	Q_1	Q_2	Q_3	
①	1	0	0	0	
②	0	1	0	0	1cp
③	0	0	1	0	2cp
④	0	0	0	1	3cp
	1	0	0	0	4cp

5cp

No. of Bits = N = N F/Fs

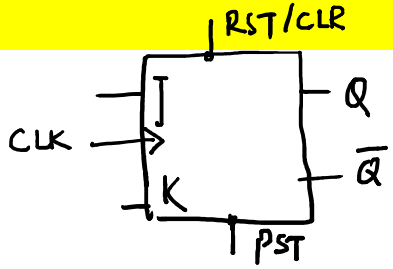
No. of states = N.

X Lot of Unused States: 12x

Counter

N F/Fs → 2^N

4 Bits → 4 FFs → 2^4 = 16 states



→ direct Inputs
→ ORI
→ Asynch. Inputs

func.: CLR → Q=0
PST → Q=1

irrespective of
CLK
I/P

QUICK QUIZ (POLL)

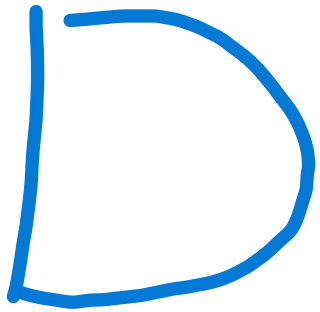
What is the preset condition for a ring shift counter?

a) All FFs set to 1

b) All FFs cleared to 0

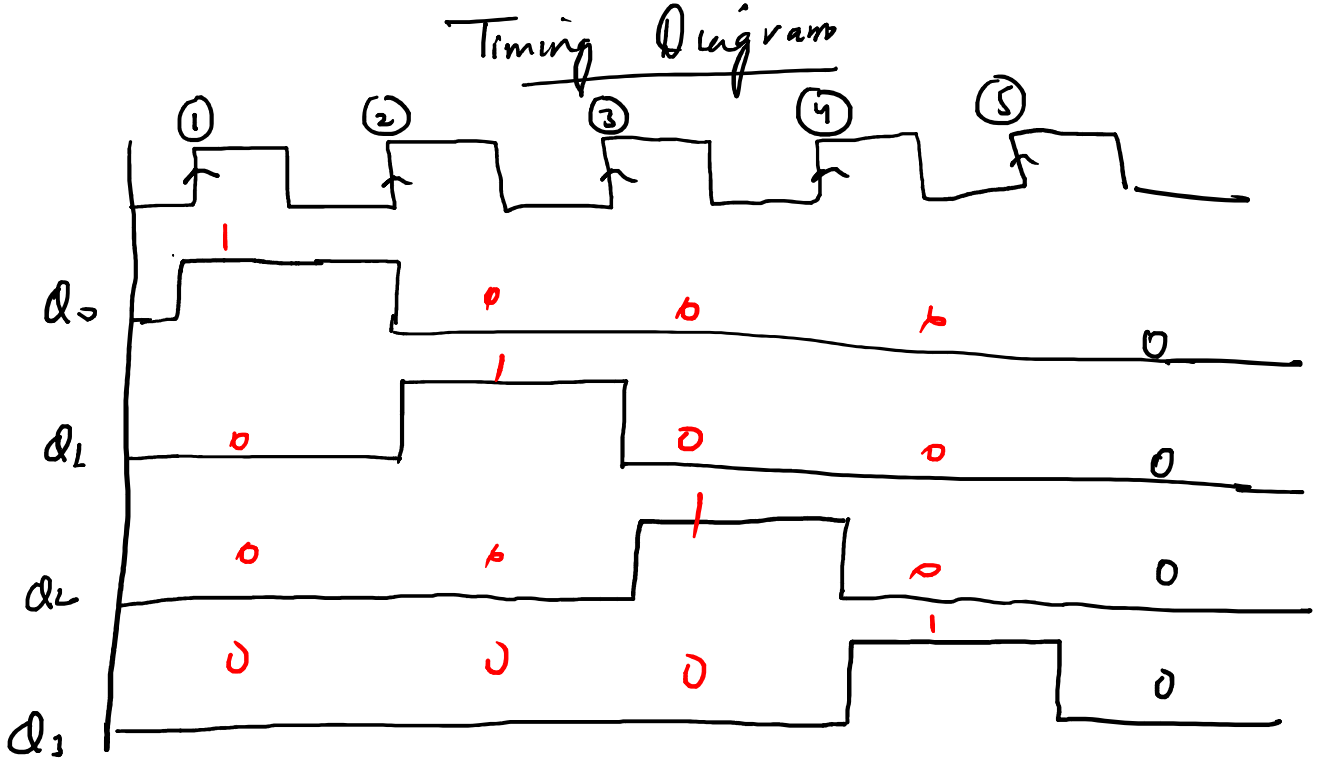
c) A single 0, the rest 1

d) A single 1, the rest 0



Timing Diagram of Ring Counter

	Q_0	Q_1	Q_2	Q_3
1 →	1	0	0	0
2 →	0	1	0	0
3 →	0	0	1	0
4 →	0	0	0	1



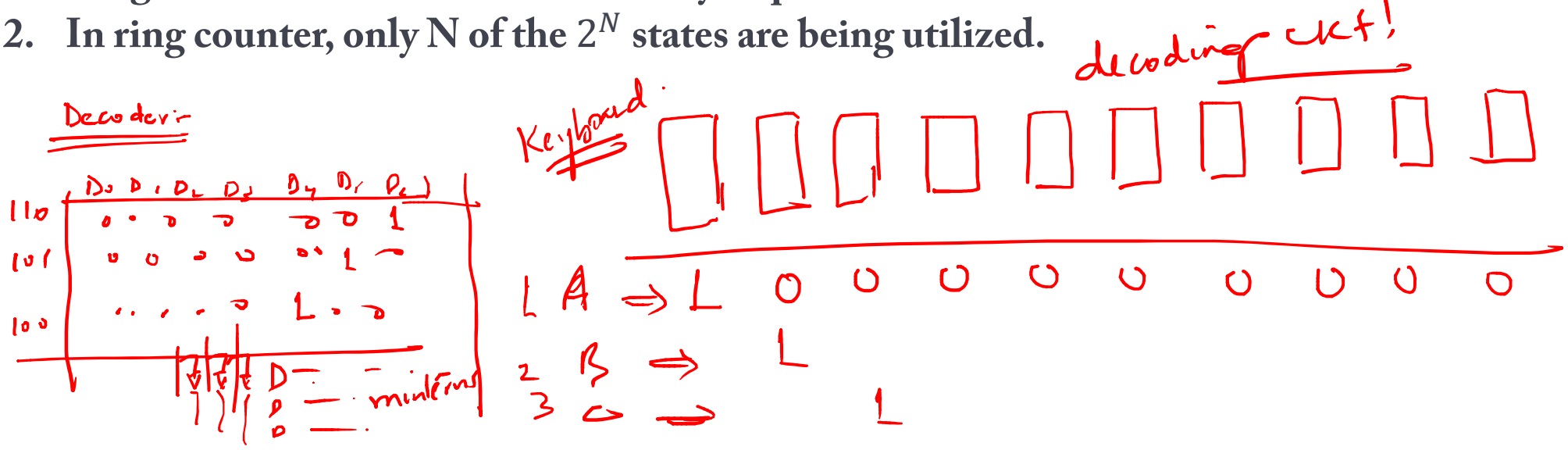
Ring Counter: Merits and Demerits

- **Merits:**

1. It doesn't need a decoder (i.e. It is a self decoding circuit)

- **Demerits:**

1. Ring counter doesn't count in a binary sequence.
2. In ring counter, only N of the 2^N states are being utilized.



QUICK QUIZ (POLL)

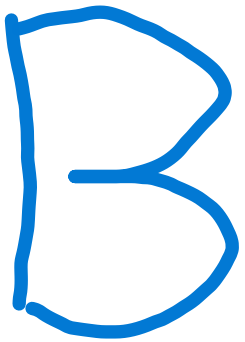
For 8 bits, the number of states in a Ring counter would be:

a) 256

b) 8

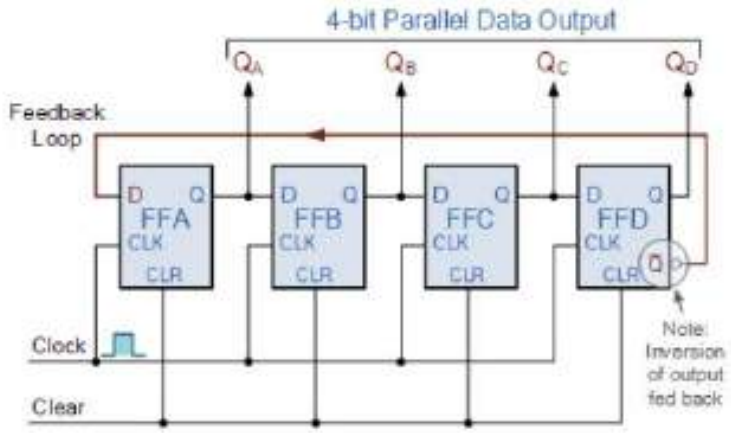
c) 16

d) 64



Johnson Counter

- The Johnson Ring Counter or "Twisted Ring Counters", is another shift register with feedback exactly the same as the standard Ring Counter above, except that this time the inverted output Q of the last flip-flop is now connected back to the input D of the first flip-flop •
- "n-stage" Johnson counter will circulate a single data bit giving sequence of 2n different states and can therefore be considered as a "mod-2n counter".



QUICK QUIZ (POLL)

Ring shift and Johnson counters are _____

a) Synchronous counters

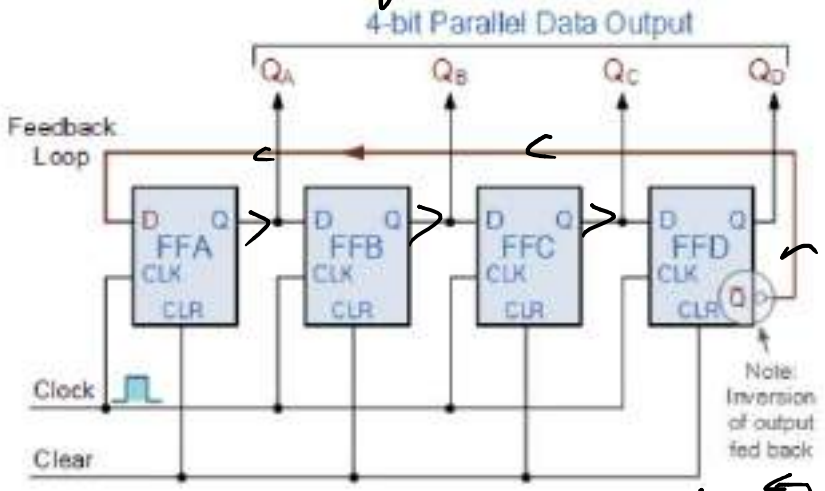
b) Asynchronous counters

c) True binary counters

d) Synchronous and true binary counters

Operation of Johnson Counter

* double the states as found on Ring Counter.



Q_A	Q_B	Q_C	Q_D	
0	0	0	0	
1	0	0	0	1 cp
1	1	0	0	2 cp
1	1	1	0	3 cp
1	1	1	1	4 cp
0	1	1	1	5 cp
0	0	1	1	6 cp
0	0	0	1	7 cp
0	0	0	0	8 cp
1	0	0	0	9 cp

N Bits → Counter : 2^N
Ring " : N
Johnson : $2N$

MCQ's.

Timing Diagram of Johnson Counter

q to ?

Yourself!

Clock Pulse No	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Johnson Counter: Merits and Demerits

- **Merits:**

1. It doesn't need a decoder (i.e. It is a self decoding circuit)
2. The Johnson counter has same number of flip flop but it can count twice the number of states the ring counter can count.

- **Demerits:**

1. Johnson counter doesn't count in a binary sequence.
2. In Johnson counter more number of states remain unutilized than the number of states being utilized.

5 Bits < 10 States (32 - 10) = 22 States

QUICK QUIZ (POLL)

For 5 bits, the number of states in a Johnson counter would be:

a) 32
b) 5
c) 10
d) 20

DIGITAL ELECTRONICS: ECE 213

Topic: PROBLEMS Based on Registers and Counters

UNIT : COUNTERS AND REGISTERS

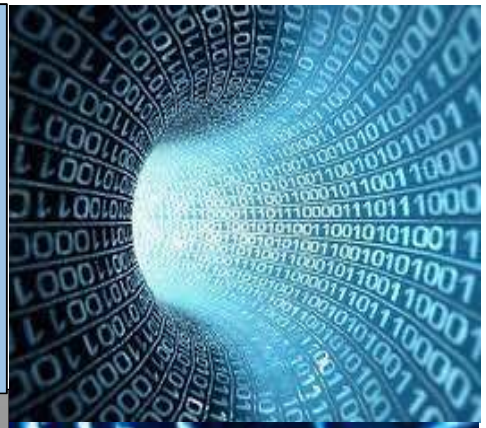
Lecture No.: 39 (Tutorial)

Prepared By: Irfan Ahmad Pindoo

Assistant Professor

VLSI Design, ECE

School of Computer Science and Engineering

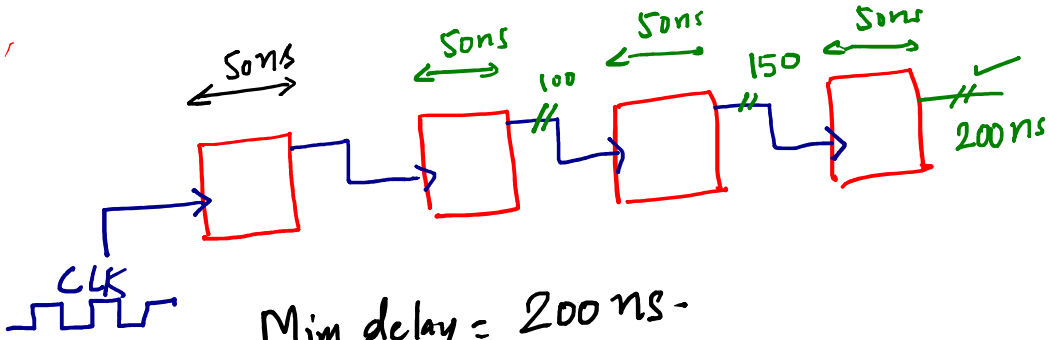


GATE Problem

A 4 bit modulo 16 ripple counter uses JK flip-flops. If the propagation delay of each FF is 50 ns. The max. clock frequency that can be used is equal to

a) 20 MHz
b) 10 MHz
c) 5 MHz
d) 4 MHz

ripple : Asynchronous.



Min delay = 200 ns.

$$freq = \frac{1}{\text{Time period}}$$

$$f = \frac{1}{T} = \frac{1}{200\,ns} = \frac{10^{+9}}{200}$$

$$= \frac{1000}{200} \times 10^{6} = 5 \times 10^{6}\ Hz.$$

$$= 5MHz$$

C

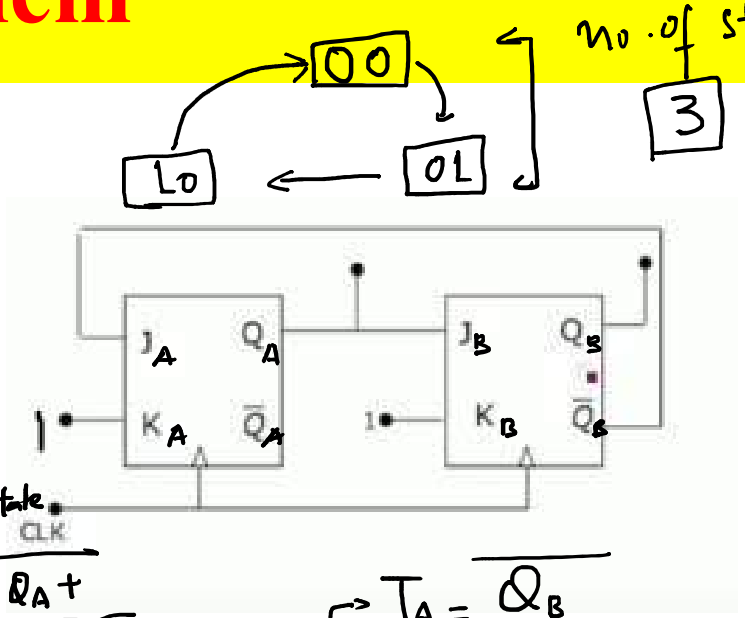
GATE Problem

Mod

The modulus of counter in the given figure is equal to

a) 1
b) 2
c) 3
d) 4

C



① Synchronous Design.

② Initial state: 00 (Reset)

③ State Table:-

Present state		Flip Flop Inputs				Next state	
Q_B	Q_A	J_B	K_B	J_A	K_A	Q_B+	Q_A+
0	0	0	1	1	1	0	1
0	1	1	1	1	1	1	0
1	0	0	1	0	1	0	0

$J_A = \overline{Q_B}$

$K_A = 1$

$J_B = Q_A$

$K_B = 1$

* Mod-3 counter

Mod-N

no. of states

Charac. Table of JK

J	K	Q
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

QUICK QUIZ (POLL)

GATE

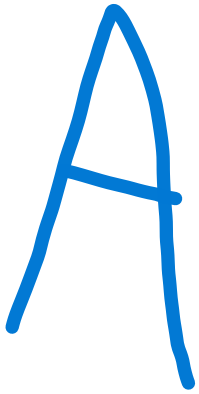
Synchronous counters are faster than ripple counters

a) faster A

b)slower

c) of same speed

d) none of these



GATE Problem

The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of counter is $Q_2\ Q_1\ Q_0 = 011$, then its next state ($Q_2\ Q_1\ Q_0$) will be

a) 010
b) 100
c) 111
d) 101

Asynch.

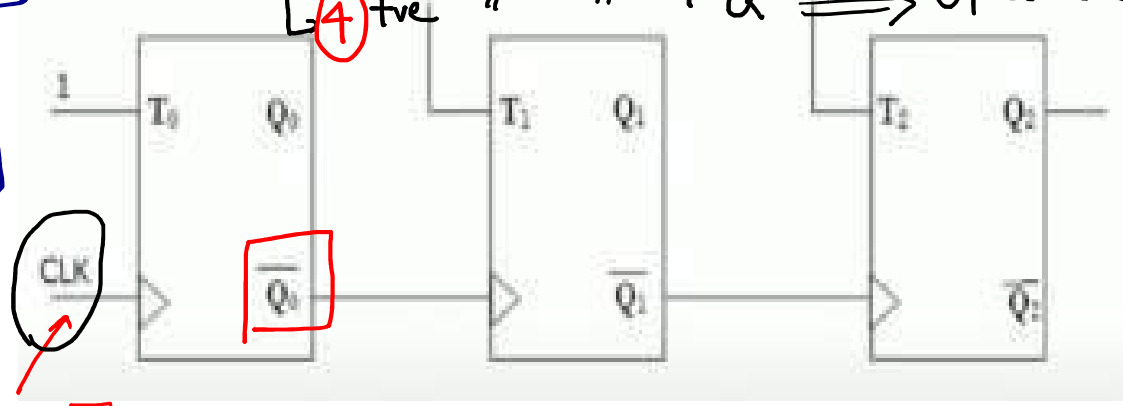
T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

Present state = $Q_2\ Q_1\ Q_0$ = 0 1 1

P.S ($Q_2\ Q_1\ Q_0$)	$T_2\ T_1\ T_0$	N.S ($Q_2^+\ Q_1^+\ Q_0^+$)
0 1 1	1 1 1	1 0 0

Next state

Trick:
- -ve edge trigg + Q ⇒ Up Counter
- -ve " " + $\bar{Q}$ ⇒ Down
- +ve " " + Q ⇒ Down
- (4) +ve " " + $\bar{Q}$ ⇒ Up Counter

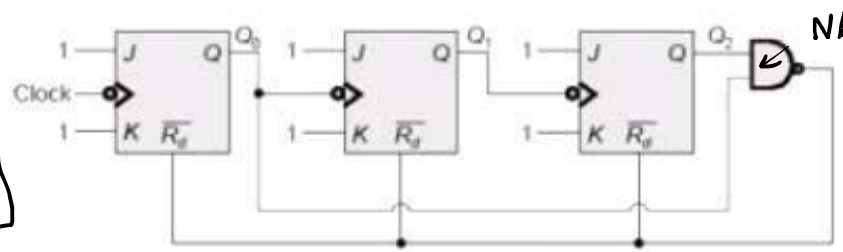


Positive Edge trigg.

B

GATE Problem

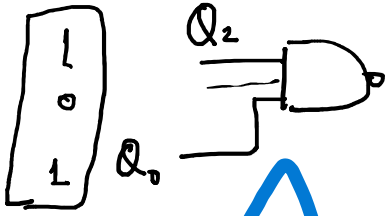
The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset ($\overline{R_d}$ input). The counter corresponding to this circuit is

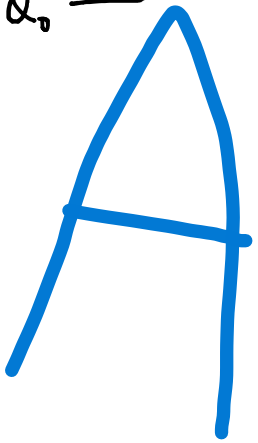


A

(A) a modulo-5 binary up counter
(B) a modulo-6 binary down counter
(C) a modulo-5 binary down counter
(D) a modulo-6 binary up counter

Mod 5
Mod 6





(1) Ripple / Asynch. Counter:

(2) -ve edge trigg.

(3) Q acting as a CLK next stage

-ve edge + Q ⟹ UP Counter

(4) Reset is done at:

$Q_2\ Q_1\ Q_0$ = L O L

X

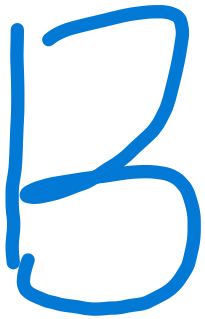
0, 1, 2, 3, 4

Mod-5 counter.

QUICK QUIZ (POLL)

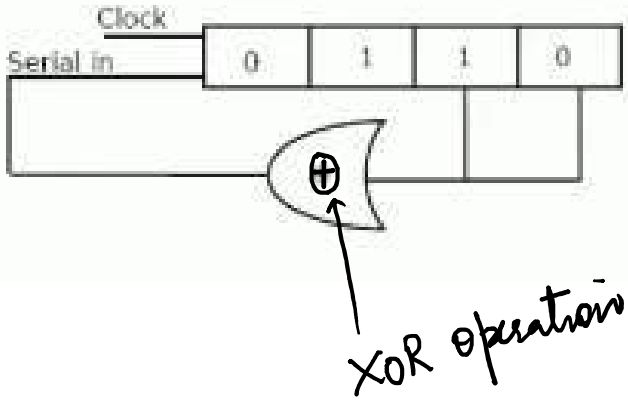
For a MOD-5 binary up counter, what would be the maximum value number displayed?

a) 5
b) 4
c) 7
d) 6



GATE Problem

The initial contents of the 4-bit serial-in-parallel-out, right-shift, Shift Register shown in figure, is 0110. After three clock pulses are applied, the contents of the Shift Register will be

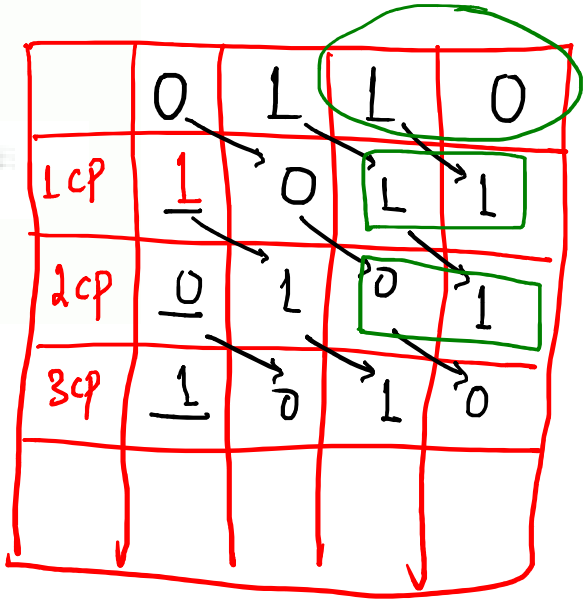


(a) 0 0 0 0 (b) 0 1 0 1

(c) 1 0 1 0 (d) 1 1 1 1

XOR operation

C



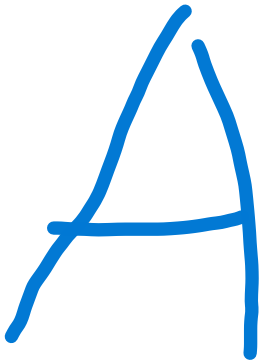
QUICK QUIZ (POLL)

GATE!

A pulse train can be delayed by a finite number of clock periods using a

a. Serial In Serial Out shift register slowest. (maxm no. of clock pulses).
b. Serial In Parallel Out shift register
c. Parallel In serial Out shift register
d. Parallel In parallel Out shift register

SISO vs PIPO



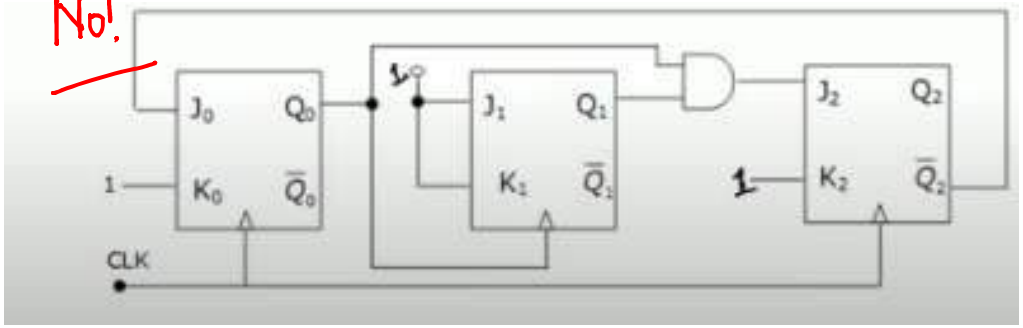
GATE Problem

MS 13

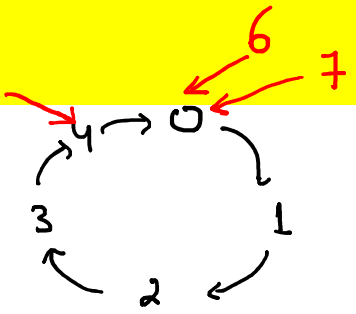
The mod-5 counter shown in Fig. counts through states $Q_2Q_1Q_0$ = 000, 001, 010, 011 and 100

(a) Will the counter lockout if it happen to be in any one of the unused states?

No!



$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0$



Unused: 5, 6, 7.

Lockout: If counter ∉ return to its original Counting sequence.

STATE TABLE:

Present state			Flip Flop Inputs						Next state		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2t	Q_1t	Q_0t
1	0	1	0	1	1	1	0	1	0	1	0
1	1	0	0	1	1	1	0	1	0	0	0
1	1	1	1	1	1	1	0	1	0	0	0

$J_1 = K_1 = K_2 = K_0 = 1$

$J_0 = \overline{Q_2}$

$J_2 = Q_1Q_0$