

Logisim: main of Half-Adder

File Edit Project Simulate Window Help

Wiring

Gates

NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter

Circuit: main

Circuit Name

main

Shared Label

Shared Label Faci...

East

Shared Label Font

SansSerif Plain 12

100%

RESULT:-

Hence the designing of the 2-bit half adder using logisim simulator has been implemented successfully.

32-BIT FULL ADDER USING LOGISIM SIMULATOR

EXP.NO: 12

AIM:

To design and implement 32-bit full adder by using logisim simulator.

TRUTH TABLE:-

Row	Inputs		Outputs			Comment
	x	y	C _{in}	C _{out}	s	
0	0	0	0	0	0	0 + 0 + 0 = 00 ₂
1	0	0	1	0	1	0 + 0 + 1 = 01 ₂