NANO LETTERS

Letter

pubs.acs.org/NanoLett

Improving Signal-to-Noise Performance for DNA Translocation in Solid-State Nanopores at MHz Bandwidths

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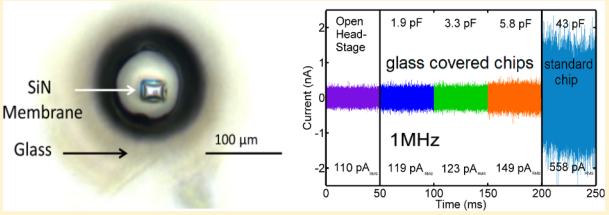
Supporting Information

ABSTRACT: DNA sequencing using solid-state nanopores is, in part, impeded by the relatively high noise and low bandwidth of the current state-of-the-art translocation measurements. In this Letter, we measure the ion current noise through sub 10 nm thick Si_3N_4 nanopores at bandwidths up to 1 MHz. At these bandwidths, the input-referred current noise is dominated by the amplifier's voltage noise acting across the total capacitance at the amplifier input. By reducing the nanopore chip capacitance to the 1−5 pF range by adding thick insulating layers to the chip surface, we are able to transition to a regime in which input-referred current noise (~117−150 pArms at 1 MHz in 1 M KCl solution) is dominated by the effects of the input capacitance of the amplifier itself. The signal-to-noise ratios (SNRs) reported here range from 15 to 20 at 1 MHz for dsDNA translocations through nanopores with diameters from 4 to 8 nm with applied voltages from 200 to 800 mV. Further advances in bandwidth and SNR will require new amplifier designs that reduce both input capacitance and input-referred amplifier noise.



KEYWORDS: *Nanopore, DNA, sequencing, TEM, silicon nitride, capacitance*

Recently, there has been significant progress in the use of both biological[1,2] and solid-state[3] nanopores for biomolecule detection. Nanopore measurements are made by driving a biomolecule through a nanopore and analyzing the temporary reduction in transmembrane ion current caused by the restriction of the available pore volume while the molecule translocates. Nanopore-based sequencing operates by measuring the distinct current reductions from individual DNA bases with different sizes as they translocate through the pore.[4,5] Biological nanopores have demonstrated de novo sequencing of small DNA segments,[4] using a molecular enzyme to lower translocation speed. DNA ratcheting through an α-hemolysin nanopore at speeds of 2.5−40 bases per second has been achieved using a similar technique.[6] Despite signal levels that are often more than an order of magnitude higher, solid-state nanopores without the benefit of enzyme ratcheting have only demonstrated differentiation between short (30 bases) homopolymers with thin silicon nitride (Si_3N_4) nanopores[5] at 500 kHz bandwidths. The typical DNA translocation speed of ~20 megabases per second in these experiment means that a 20-fold increase in the measurement speed (bandwidths in excess of 20 MHz) will be required to achieve single-base resolution.

The primary barrier to achieving free-running nanopore DNA sequencing is obtaining a high SNR at the required bandwidths—as higher bandwidth requirements increase noise and decrease SNR, making it impossible to discriminate between DNA bases. There are two distinct SNRs that are often referenced in the context of solid-state nanopores; each is associated with a different signal level. The first, $SNR_{ionic} = \Delta I_{ionic}/I_{rms}$, uses as the signal level the total change in the ion current (ΔI_{ionic}) when DNA passes through the nanopore (Figure 1d), where I_{rms} is the root-mean-square (rms) input-referred current noise of the nanopore. The second SNR metric, $SNR_{contrast} = \Delta I_{contrast}/I_{rms}$, uses as the signal level ($\Delta I_{contrast}$) the contrast between ion signals from different nucleotides (Figure 1d).

Increasing ΔI_{ionic} (and $\Delta I_{contrast}$) can be achieved by decreasing the thickness of nanopore sensors.[5,7] It has long been recognized that decreasing I_{rms} requires reducing the total capacitance of the nanopore device.[8−10] Above 10 kHz, the dominant noise is the interaction of the amplifier's voltage noise with the total capacitance at the input, which includes the chip capacitance (C_{chip}), the capacitance seen at the input of the amplifier (C_{amp}), and any interconnect capacitance from the amplifier to the nanopore (C_w).[1,2,11] In this case, I_{rms} at a bandwidth B is given by

$$I_{rms}(B) = \left(\frac{2\pi}{\sqrt{3}}\right) B^{2/3} (C_{chip} + C_w + C_{amp}) v_n \quad (1)$$

where v_n is the input-referred voltage noise of the amplifier and C_{chip} values typically range from ~50 pF[3,11] to 370 pF[4,5,12] in most nanopore measurements. C_{chip} can be further reduced by painting a thick silicone elastomer onto the chip surface.

Received: November 12, 2014

   dx.doi.org/10.1021/nl504345y | *Nano Lett.* XXXX, XXX, XXX−XXX

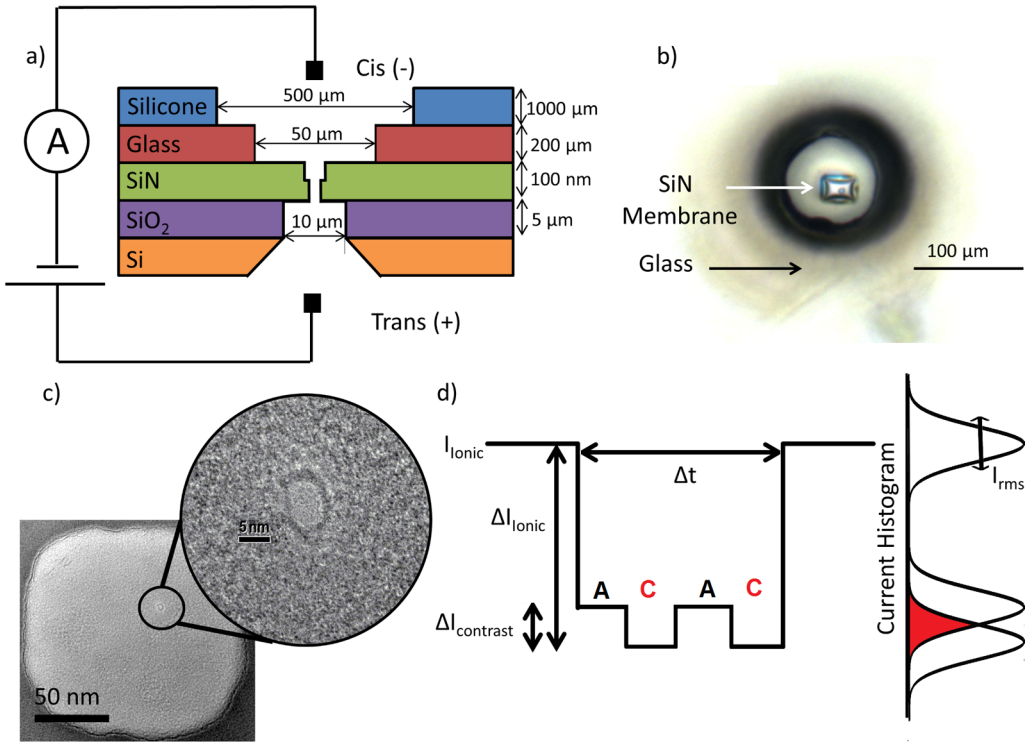


Figure 1. (a) Schematic of the stacked nanopore chip with dimensions indicated. A 500 μm thick silicon chip is covered with 5 μm of silicon dioxide onto which 100 nm of Si_3N_4 is deposited. The chips are etched to create a suspended Si_3N_4 membrane window with side length ranging from 10 to 40 μm. A reactive ion etch is then used to thin the portion of the membrane into which the pore will be drilled. A 100−200 μm thick glass layer, containing a 50 or 100 μm diameter laser-drilled hole, is placed on top of the Si_3N_4 using a micromanipulator setup and attached with an acrylic adhesive. Finally, a silicone elastomer is hand-painted on top of the glass and over the whole ~5 × 5 mm membrane-facing side of the chip, leaving an exposed glass area of less than 0.25 mm^2 around the nanopore. Finally a nanopore of diameter ~2−8 nm is drilled in the thinned region of the membrane using a focused TEM beam. This device is positioned to separate two chambers of 1 M KCl solution across which a bias of up to 1 V is applied. The ion conductance is then monitored using a voltage-clamp amplifier. (b) Optical image of the resulting nanopore chip with a glass hole diameter of 100 μm and Si_3N_4 membrane with a side length of 20 μm. (c) TEM image of a 7 nm diameter nanopore which was drilled into the thinned region of the Si_3N_4 membrane with the focused beam of the TEM. (d) A diagram of a model DNA translocation. As DNA passes through the nanopore, it blocks a considerable fraction of the nanopore volume and this DNA translocation event is characterized by its duration, Δt, and current reduction, ΔI. Different bases produce different residual currents, allowing for the determination of $\Delta I_{contrast}$, the difference between the current reductions of the different bases. Noise in the ionic current creates a broadened distribution in the current histograms.

Membrane capacitances as low as 6 pF[11] have been demonstrated by this method, achieving I_{rms} ~ 155 pA_{rms} over a 1 MHz bandwidth for a custom amplifier with v_n = 5 $nV/\sqrt{Hz}$. Other efforts to reduce C_{chip} included patterning insulators onto the chip surface[6,9,13] and transferring the Si_3N_4 membrane onto a PDMS substrate,[5,14] resulting in I_{rms} ~ 30 pArms measured at 10 kHz bandwidth[5,7,12] and I_{rms} ~ 15 pArms at 100 kHz, respectively.[8−10,15] The signal-to-noise ratio and signal amplitude have also been studied for DNA translocation through ~10 nm diameter glass nanocapillaries, yielding SNR ~ 25 at 10 kHz bandwidth.[16]

In this Letter, we exploit glass bonding to lower C_{chip} to ~1.5 pF for sub 10 nm thick silicon nitride nanopores, achieving SNR_{ionic} of up to 20 at 1 MHz bandwidth for a standalone amplifier with C_{amp} = 20 pF and v_n = 1 $nV/\sqrt{Hz}$. These nanopores are used to detect translocation of double-stranded DNA (dsDNA) in 1 M KCl solution. The lowest measured I_{rms} ~ 115 pA_{rms} at 1 MHz bandwidth is near the amplifier open-headstage limit of ~110 pA_{rms}, indicating that further improvements require new amplifier designs that reduce input capacitance, amplifier input-referred voltage noise, or both.

Figure 1a shows a schematic diagram of the Si_3N_4 chips used for making nanopores improved from the design described elsewhere.[17] Briefly, nanopores are formed in sub 10 nm thin regions of suspended 50 nm thick Si_3N_4 membranes with side lengths of ~10−40 μm. The membranes are supported by 5 μm of silicon dioxide[18] on 500 μm of n-type doped silicon. Figure 1b is the optical image of the nanopore chip with the top glass layer clearly visible. In this case, a 100 μm thick glass plate with a laser-drilled 50 μm diameter hole is bonded to the top surface of the pore substrate. A silicone elastomer is painted on top of the glass and over the whole membrane-facing side of the chip (~25 mm^2 area), leaving an exposed <0.25 mm^2 area around the nanopore. The glass placement and bonding procedure is described in the Methods. Figure 1c is a TEM image of one of these pores with diameter ~7 nm. We present ion current data from nanopore diameters from 4 to 8 nm.

The ion-current measurement setup is shown in Figure 1a. The nanopore chip separates two chambers of salt solution and voltage is applied across the nanopore while the ion conductance is monitored. When DNA passes through the nanopore, a significant fraction of the ionic current is blocked, presenting a measurable signal. Translocations are characterized by ΔI_{ionic} and Δt, corresponding to the change in ion current and the duration of the translocation event, respectively. Once translocations have been identified by their deviations from baseline current, the signal is plotted on a histogram. Figure 1d

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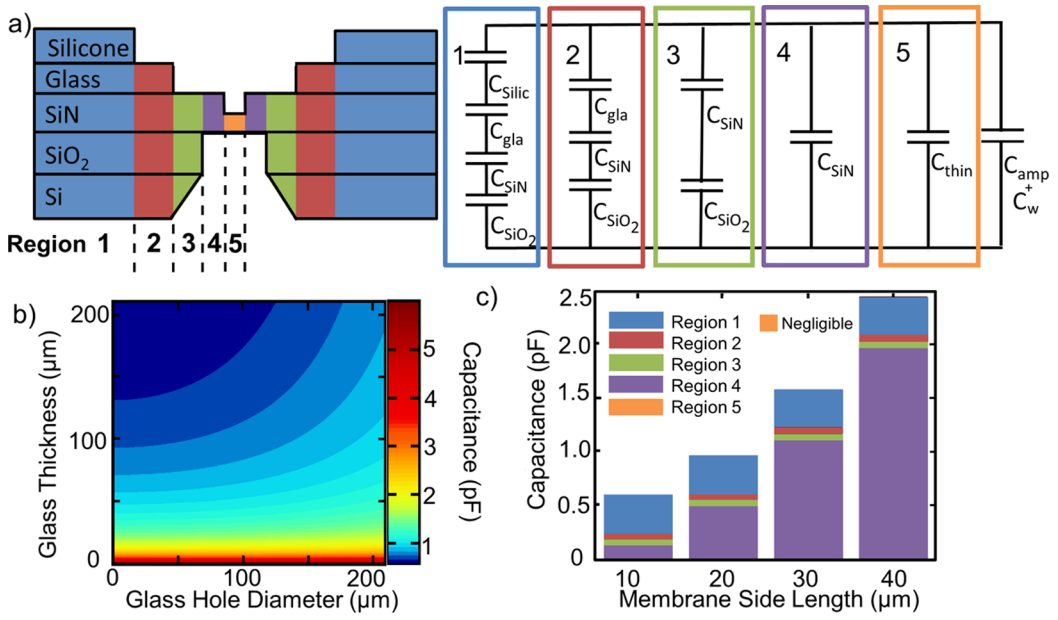

Figure 2. (a) Schematic diagram of chip structure composed of stacked layers of Si, SiO_2, Si_3N_4, glass, and silicone. Five regions (labeled 1−5) spanning the chip structure vertically and contributing to the capacitance are indicated by different colors (left). The corresponding capacitor circuit model, where C_{SiO2}, C_{SiN}, C_{gla}, C_{thin}, and C_{Silic} are capacitances of the individual layers (SiO_2, SiN, glass, thinned SiN and silicone) within each region, are shown. (b) Two-dimensional contour plot of chip capacitance as a function of glass thickness and glass hole diameter for a constant Si_3N_4 membrane side length of 10 μm. (c) Bar graph of chip capacitance for membrane side lengths of 10, 20, 30, and 40 μm, showing relative contributions from regions 1 to 5.

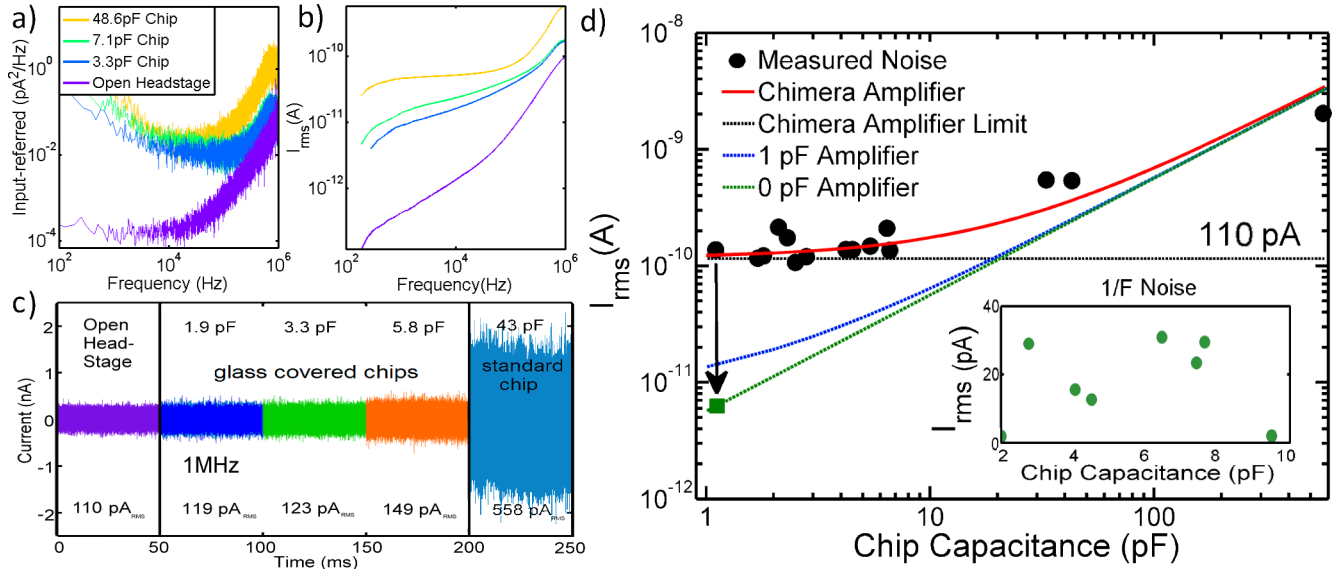

Figure 3. (a) Input-referred noise power spectral density (PSD) for two glass-passivated nanopore chips with membrane capacitances of 3.3 and 7.1 pF. The PSDs for an unpassivated chip (with C_{chip} = 48.6 pF) and the open-headstage amplifier are also shown. (b) I_{rms} calculated from the data in part a, as a function of signal bandwidth showing increase in noise proportional to capacitance at frequencies above 10^5 Hz. (c) Measured ion current temporal traces at a 1 MHz bandwidth for several glass-passivated chips with capacitances C_{chip} = 1.9, 3.3, and 5.8 pF. There are compared with an unpassivated chip (C_{chip} = 43 pF) and an open-headstage measurement. I_{rms} values are indicated. (d) I_{rms} at 1 MHz bandwidth is shown as a function of C_{chip}. Measured values (black circles) compare favorably with values predicted from eq 1 (red curve). The open-stage amplifier noise of 110 pA at 1 MHz is also indicated by a horizontal black dashed line. For comparison, the blue and green dashed lines show the expected I_{rms} vs C_{chip} for an assumed amplifier design with v_n = 1 nV/(Hz$^{1/2}$) and C_{amp} = 1 pF and an idealized case of C_{amp} = 0 pF, respectively. The inset shows I_{rms} at 1 kHz bandwidth (green circles). This low-frequency noise is independent of capacitance.

is a model of an idealized signal of a DNA molecule with two bases (e.g., ACAC) and demonstrates the process through which DNA translocations are analyzed. Figure 1d also illustrates the source of expected sequencing errors resulting from the signal overlap of current distributions corresponding to different bases, indicated in red. Insufficiently high $SNR_{contrast}$ can make it difficult to distinguish between bases, leading to significant base call errors.

The increase of the SNR can be achieved by lowering the chip capacitance. Figure 2a shows the schematic diagram of the

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chip structure and the corresponding constituent elements that contribute to chip capacitance. C_{chip} is estimated by decomposing the structure into sections of equal thickness that add in parallel to give the total chip capacitance. Each of these sections is then further decomposed into layers of different dielectrics (glass, Si_3N_4, silicone elastomer) that can be described as capacitors in series. The right panel in Figure 2a additionally includes C_{amp} and C_w (~0.4 pF from the short external wiring).

Figure 2b shows the calculated C_{chip} using the model in Figure 2a, as a function of the glass hole diameter and glass thickness for a fixed Si_3N_4 window size of 10 μm × 10 μm. Our experiment uses glass with thicknesses ranging from 100 to 200 μm and holes ranging from 50 to 100 μm. The smallest predicted C_{chip} is 0.60 pF for a glass thickness of 200 μm and a glass hole diameter of 50 μm. At this thickness and diameter for the bonded glass, capacitance contributions per section vary from 1.4×10^3 pF/m^2 for Region 1 (the thickest region) to 4.13×10^6 pF/m^2 for Region 5 (the thinnest region). The capacitance from Region 5 is negligible because of its small area, while Regions 1 (~58%) and 4 (~20%) contribute the most (Figure 2c). These calculated values of total chip capacitance are in good agreement with measured values. Chip capacitance is measured in a fluidic cell with the VC100 low-noise patch-clamp amplifier (Chimera Instruments, New York, NY) by applying triangular-wave voltages and measuring the resulting current response (see Supporting Information S1).

Figure 3a shows the input-referred power spectral density (PSD), $S_n(f)$, of the ion current noise as a function of bandwidth for two representative chips with C_{chip} of 3.3 pF and 7.1 pF, along with a chip without bonded glass which presents a capacitance of 48.6 pF. For comparison, we also show here the open-headstage noise spectrum. The PSDs have the form[19]

$$S_n(f) = a_{-1}f^{-1} + a_0 + a_1 f + a_2 C_T f^2 \quad (2)$$

where $C_T = C_{amp} + C_{chip} + C_W$. In the low-frequency regime (<1 kHz), the $1/f$ noise in the ionic conductance of the nanopore itself is dominant. Between 1 kHz and 20 kHz, the noise spectrum is dominated by the second term representing the white noise in the pore and amplifier. The third term is primarily attributed to dielectric losses in the membrane. The last term represents the amplifier's input-referred thermal noise v_n acting through C_T giving an f^2-dependence beyond 20 kHz ($S_n(f) = (2\pi f C_T v_n)^2$), which dominates high-bandwidth noise floors. Figure 3b shows the integrated I_{rms} as a function of bandwidth corresponding to data in Figure 3a. Figure 3c shows the ion current noise, I_{rms}, as a function of time measured through several nanopores drilled in glass covered chips with C_{chip} = 1.9 pF to 5.8 pF, compared to the open headstage current noise and a standard nanopore chip with C_{chip} = 43 pF. The open pore ion current through the nanopores was rescaled to zero for all pores. As shown, I_{rms} approaches the amplifier noise limit of 110 pA for C_{chip} < 10 pF as the internal capacitance of the amplifier (C_{amp} = 20 pF) starts to dominate.

Figure 3d shows I_{rms} at 1 MHz bandwidth as a function of C_{chip} for all of the nanopores measured. The red line in Figure 3d is I_{rms} calculated from eq 1 where C_{amp} = 20 pF, C_W = 0.4 pF, and v_n = 1 nV/(Hz$^{1/2}$), showing excellent agreement with the data. The open-headstage I_{rms} of 110 pA$_{rms}$ at 1 MHz bandwidth is also noted. Data in Figure 3d clearly show that we are now in a regime where noise is determined by C_{amp} (and v_n). Further reduction of C_{chip} at this stage will have a negligible effect on I_{rms}. The blue and green dashed lines show the expected performances (I_{rms} as a function of C_{chip}) for future amplifier designs with v_n = 1 nV/(Hz$^{1/2}$) and C_{amp} = 1 pF and an idealized case of C_{amp} = 0 pF, respectively. The inset of Figure 3d shows the integrated input-referred current noise integrated up to 1 kHz band, capturing the low frequency ($1/f$) contribution to the total noise. Even for chips with C_{chip} < 10 pF, this low-frequency noise is usually less than 20% of the total integrated noise to the 1 MHz band. Furthermore, this noise is completely independent of C_{chip}, being rather a function of nanopore cleanliness and hydrophilicity.[20]

Figure 4a and b shows translocation measurements of 15k-base-pair-long dsDNA through the *same* 4 nm diameter nanopore drilled in 40 nm thick Si_3N_4 membrane at applied bias of 800 mV in 1 M KCl. Data are shown *before* (Figure 4a, red trace) and *after* (Figure 4b, blue trace) C_{chip} was reduced by adding the bonded-glass insulating layer (C_{chip} = 47 pF before and C_{chip} = 4.9 pF after). The current traces are shown at both 1 MHz bandwidth (a 4M samples/s sampling rate is used) and filtered to 10 kHz bandwidth. The ~10-fold capacitance reduction results in a 3-fold reduction of high-frequency noise I_{rms}, from 615 to 183 pA at 1 MHz bandwidth. The corresponding SNR_{ionic} is 19 at 1 MHz. The I_{rms} in the low frequency range (10 kHz) is not influenced by the reduction in capacitance and remains the same in Figure 4a and b.

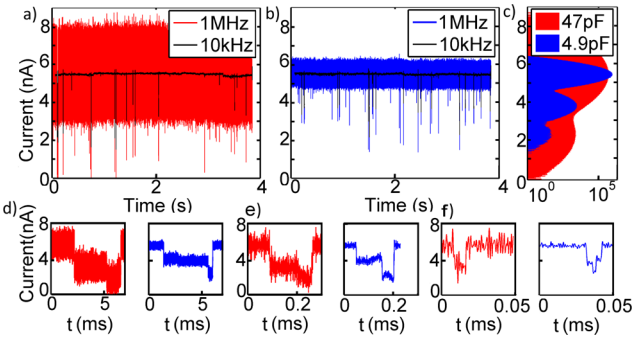

Figure 4. Comparison of 15 kbp dsDNA translocation results obtained from the *same* nanopore with diameter 4 nm, *before* and *after* capacitance reduction by glass passivation. (a) Ion current trace as a function of time before capacitance reduction (C_{chip} = 47 pF) at 1 MHz (red trace) and 10 kHz (black trace) measurement bandwidths. (b) Current trace of the pore after passivation (C_{chip} = 4.9 pF) at 1 MHz (4 MSs sampling rate) (blue trace) and 10 kHz (black trace) bandwidths. (c) All-points current histograms in red and blue correspond to the red and blue traces in parts a and b, respectively. The peak centered at ~5.5 nA, corresponding to the open pore current, is much broader in the red histogram, as expected. The blue histogram shows a structure with three peaks: the open pore current peak and two peaks corresponding to dsDNA molecules passing in both folded and unfolded states. (d) Example events of different duration, in the order of decreasing durations (5, 0.2, or 0.02 ms), for the two capacitances (red 47 pF, blue 4.9 pF). The events corresponding to the lower capacitance chip (blue) show less noise and a clearer separation of levels within the events.

The histograms of the current distributions at 1 MHz bandwidth for the two different values of chip capacitance are shown in Figure 4c. The open-pore baseline current is approximately ~5.5 nA for both measurements (before and after glass bonding). While the open pore current can drift over time and change when the pore is recleaned, in this particular case, it changes very little between the two measurements (<5%). In the 4.9 pF data set the noise is low enough at 1 MHz

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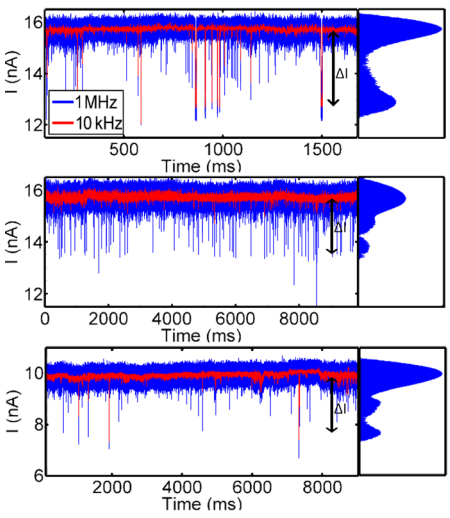
bandwidth to distinguish three distinct peaks, two of which correspond to events in which DNA molecules pass in both a folded and unfolded states. These two states are not distinguishable in the 47 pF data set. Figure 4d–f shows selected events with multilevel structure at 1 MHz bandwidth (47 pF in red, 4.9 pF in blue). The events have different approximate durations, 5 ms in Figure 4d, 200 μs in Figure 4e, and 20 μs in Figure 4f. In contrast with the 47 pF data set where the levels overlap (red events in Figure 4d–f) and are difficult to analyze with simple event-detection algorithms, in the 4.9 pF data set the levels are easily and clearly distinguishable (blue events), even for events as short as 5 μs.

Figure 5 shows ion current traces and associated current histograms for three additional nanopores measured under the



Pore Size	6 nm
Voltage	240 mV
ΔG	7 nS
C_{Chip}	5.4 pF
I_{rms} (1 MHz)	148 pA
SNR_{ionic} (1 MHz)	20

Pore Size	8 nm
Voltage	300 mV
ΔG	7 nS
C_{Chip}	1.7 pF
I_{rms} (1 MHz)	117 pA
SNR_{ionic} (1 MHz)	18

Pore Size	5 nm
Voltage	220 mV
ΔG	9 nS
C_{Chip}	4 pF
I_{rms} (1 MHz)	135 pA
SNR_{ionic} (1 MHz)	15

Figure 5. Ion current as a function of time during translocation of 15 kbp dsDNA molecules in 1 M KCl from three nanopores chips containing sub 10 nm thick Si_3N_4 nanopores. The nanopore diameters are between 5 and 8 nm, and nanopore chips are glass-passivated, leading to C_{chip} values between 1.7 and 5.4 pF. 1 MHz (blue trace) and 10 kHz (red trace) bandwidth measurements are shown. Corresponding all-points current histograms are shown at 1 MHz bandwidth. Specific nanopore diameter, applied voltage, resulting I_{rms}, and SNR_{ionic} at 1 MHz are indicated in the table. SNR_{ionic} ranges from 15 to 20 for dsDNA at 1 MHz.

same conditions as those in Figure 4. Nanopore diameters are approximately 6 nm, 5 nm, and 8 nm with applied voltages of 240 mV, 300 mV, and 220 mV, respectively. The measured I_{rms} for each case is approximately 148 pA, 117 pA, and 135 pA at 1 MHz for chip capacitances $C_{chip} \sim 5.4$ pF, 1.7 pF, and 4 pF, respectively. Signal conductances during dsDNA translocation ranged from $\Delta G = 7$ to 9 nS, comparable to the best values obtained previously.[5] The calculated SNR_{ionic} ranges from 15 to 20 at 1 MHz, enabling detection of shallow events at 1 MHz bandwidth that would otherwise be missed in unpassivated chips with $C_{chip} \sim 50$ pF.

Nanopore sequencing will require the ability to distinguish the current signatures of individual DNA bases as they pass through a nanopore. One method to estimate these expected current differences is to translocate homopolymer DNA of different bases, each consisting of a single nucleotide species, and measure the resulting differences in their current signals. Consequently, it is interesting to examine the requirements on the total input capacitance ($C_T = C_{amp} + C_W + C_{chip}$) and amplifier input-referred noise (v_n) to be able to achieve homopolymer differentiation at 1 MHz. Recent literature has shown that thin, silicon-nitride nanopores give a difference in ion current between different ssDNA homopolymers of between 200 and 900 pA.[5] The error rate in distinguishing between different bases, assuming a Gaussian noise distribution, is given by $1 - erf((SNR_{contrast})/(2\sqrt{2}))$. Using a 1% error rate and $\Delta I_{contrast} = 200$ pA, I_{rms} would have to be reduced to less than 40 pArms. At $v_n = 1$ nV/(Hz$^{1/2}$), this requires C_T to be reduced to 7.5 pF. This estimate may be extended to find the capacitance required at 20 MHz, which would be required for sequencing at 10 Mbases per second. To achieve the same I_{rms} (at the same v_n) at this higher bandwidth requires C_T to be reduced to 0.1 pF (from eq 1).

In conclusion, by applying glass bonding, we have reduced the capacitance of Si_3N_4 nanopore membranes to as low as 1.5 pF, allowing input-referred ion current noise to reach amplifier-determined limit of ~115 pA_{rms} at 1 MHz bandwidth. Translocation measurements of dsDNA molecules in 1 M KCl, through sub 10 nm thick Si_3N_4 nanopores of diameter 4–8 nm, and applied bias of 200–800 mV, show SNR_{ionic} of 15–20 at 1 MHz at these noise levels. We demonstrate that reducing chip and amplifier capacitances will be essential to further bandwidth enhancements of nanopore measurements. Improved measurement capabilities have the potential to complement or displace approaches which slow down translocation in DNA sequencing applications paving the way for human genome sequencing in sub 1 h timeframes.

Materials and Methods. Nanopore chips are built on a 5 × 5 mm substrate of Si onto which a layer of SiO_2 is deposited. A further layer of Si_3N_4 is then added. After the photolithography steps are complete, the device is cleaned in boiling piranha solution and repeatedly rinsed with water. C2-950 PMMA is then spun onto the membrane side of the chip, which is then patterned with electron beam lithography and etched with CHF_3, before being cleaned in piranha again.

A 100 or 200 μm thick glass piece with a laser-drilled pore is also cleaned in piranha before being attached to a micromanipulator tip using a vacuum. This micromanipulator is then used to align the hole in the glass with the membrane of the nanopore chip. Once the alignment is complete, a small quantity of cyanoacrylate adhesive is placed onto the exposed surface of the nanopore device, such that the flow of the liquid leads it into contact with the edge of the glass as shown in Figure S4. The adhesive is drawn underneath the glass by interfacial forces, forming a watertight seal without covering the membrane.

The chips were then placed in the TEM, where nanopores with diameters ranging from 2 to 10 nm were drilled using the focused electron beam. We estimate a 10% error in determining the nanopore diameter; this error takes into account the fact that the shape of the nanopores is more precisely described as an ellipse, rather than a circle. The reported diameter is the average of the major and minor diameters. The resultant chips were cleaned using an oxygen and hydrogen plasma for 60–120 s to promote hydrophilicity. Chips are attached to a Teflon cell using a silicone elastomer (Kwik-cast, World Precision Instruments) painted on top of the glass and over the whole membrane-facing side of the chip (~25 mm^2 area), leaving an exposed <0.25 mm^2 area around the nanopore.

The cell has two chambers of 1 M KCL/1 mM EDTA solution buffered to a pH of 8 using 10 mM TrisHCl. Our cell allows for fluid volume of 10–50 μL. Bias voltages of ~200–

dx.doi.org/10.1021/nl504345y | Nano Lett. XXXX, XXX, XXX–XXX

800 mV are applied across the nanopore using Ag/AgCl electrodes. Experiments were conducted using a VC100 voltage-lamp amplifier (Chimera Instruments, New York, NY), to apply the bias voltage and measure the ion current through the nanopore. The amplifier applies a fourth order Bessel low-pass filter at 1 MHz. Signals are sampled at 4−6 MS/s. The measured signals are then analyzed in MATLAB (MathWorks, Natick, MA).

■ ASSOCIATED CONTENT

Supporting Information

Estimations of chip capacitance from geometrical considerations and from the measured power spectral density, measurement of chip capacitance and illustration of the glass bonding procedure. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by NIH Grants R21HG004767 and R01HG006879. We gratefully acknowledge use of the TEM in the NSF-MRSEC electron microscopy facility. We thank Andrew Sharo, Matthew Puster, Dr. Kimberly Venta, and Prof. Jacob Rosenstein for their help and useful discussions.

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