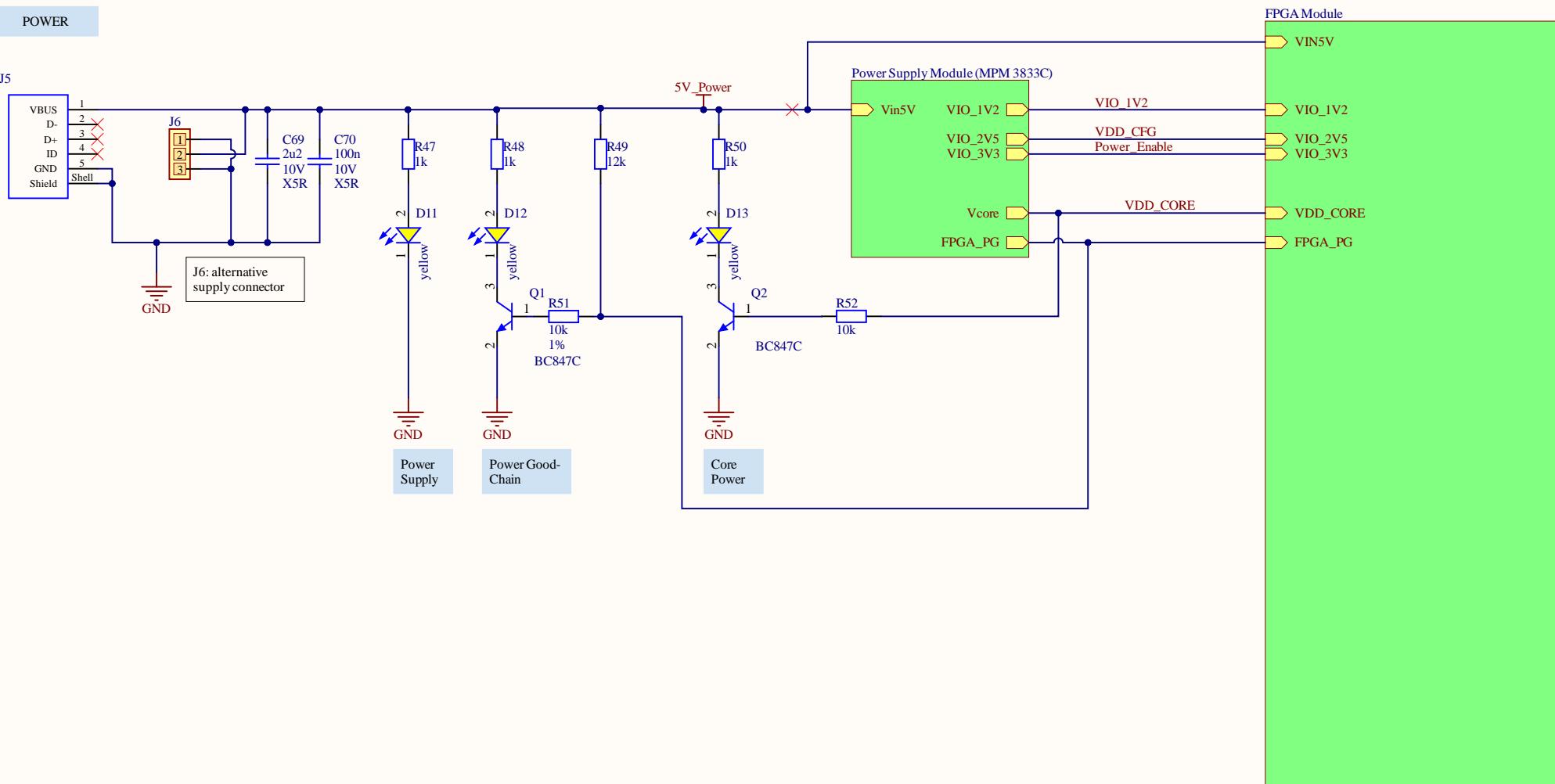


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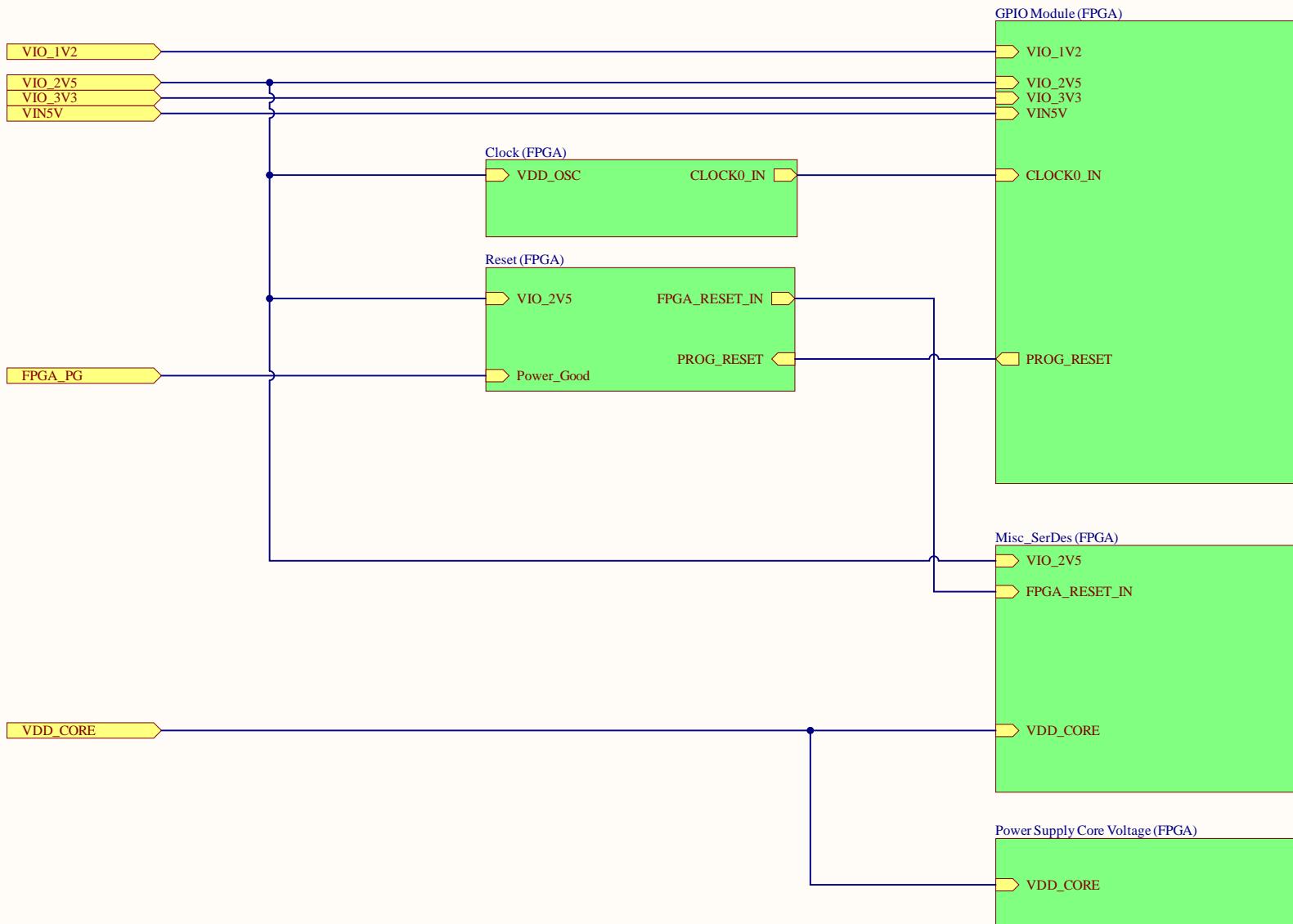
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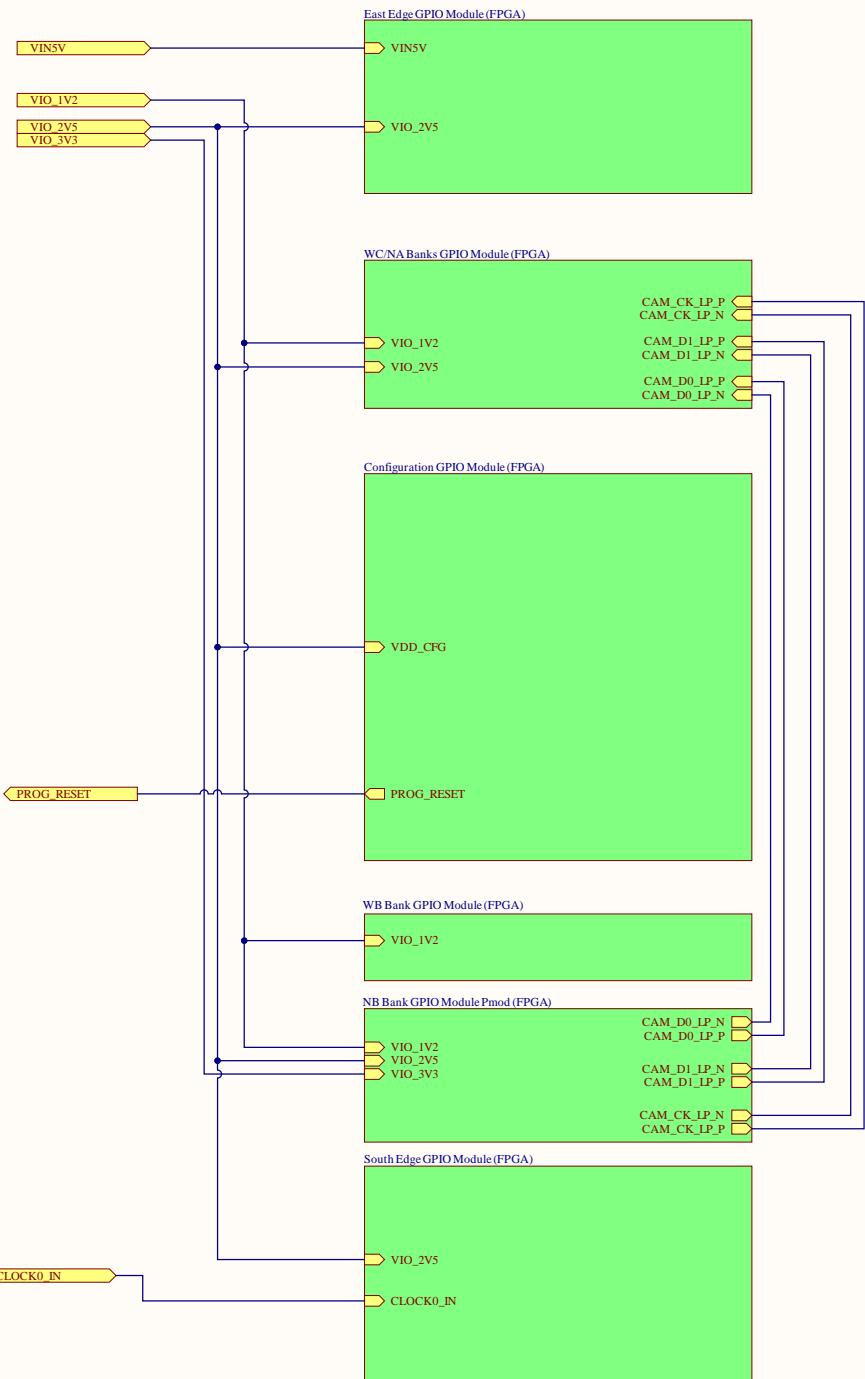
D

D

A

A



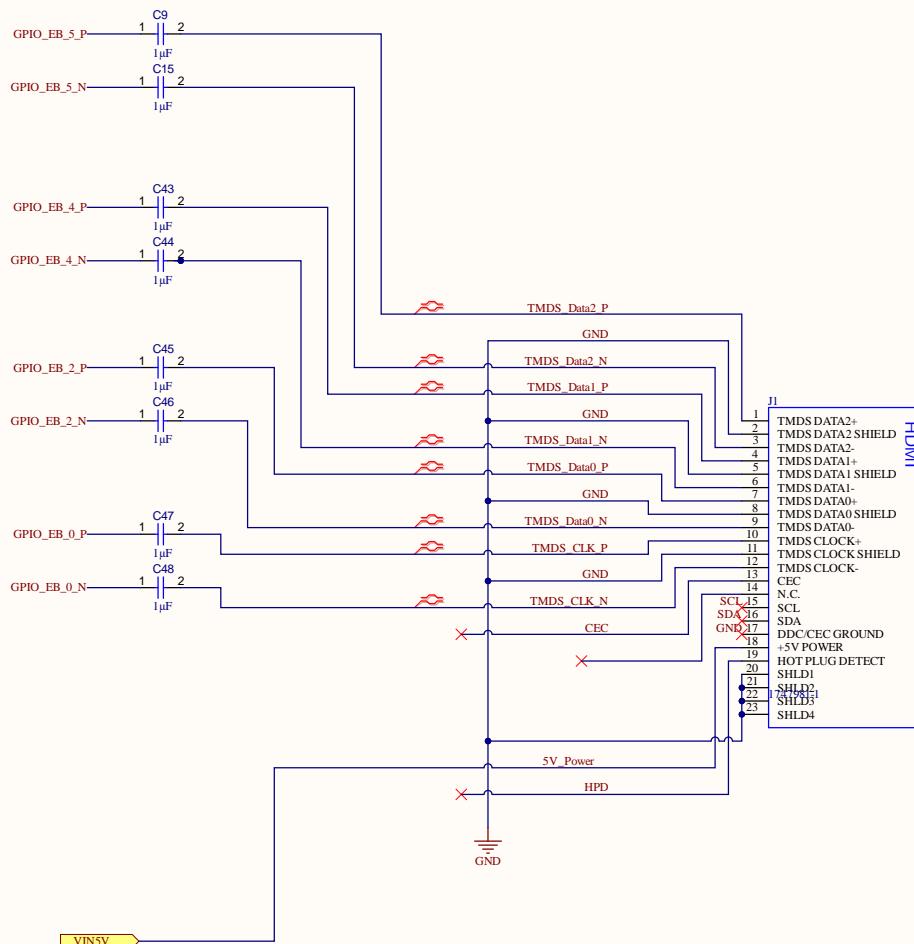
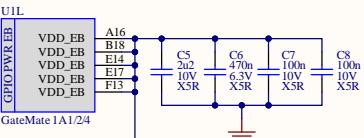
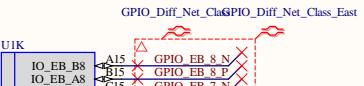
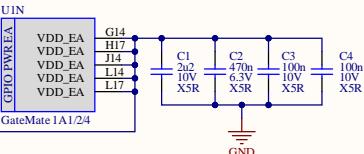
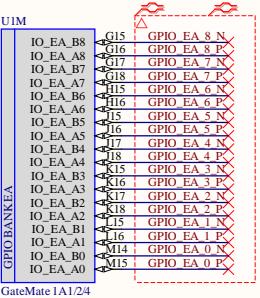


Project:	GateMate CCGM1A1 (BGA324) Evaluation Board	Revision:	3.1B
Title:	GPIO Module (FPGA)		
Size:	A3	Author:	CCAG
File:	FPGA_GPIO.SchDoc	Date:	08.07.2024

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Germany



GPIO_Diff_Net_Class GPIO_Diff_Net_Class_East



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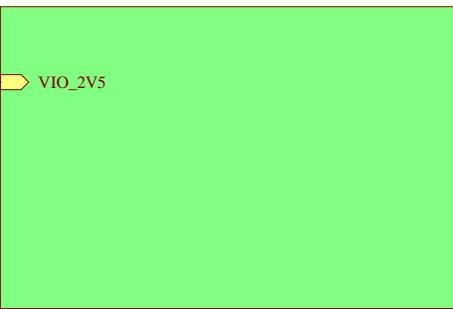
C

C

D

D

SA Bank GPIO Module (FPGA)



SB Bank GPIO Module (FPGA)



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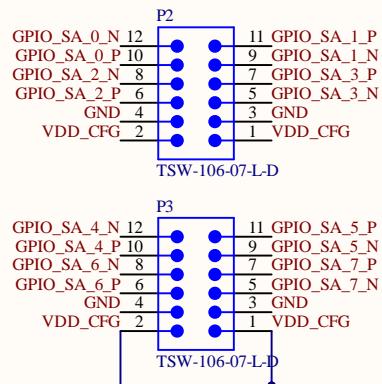
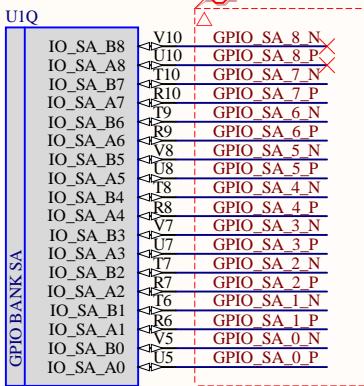
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C

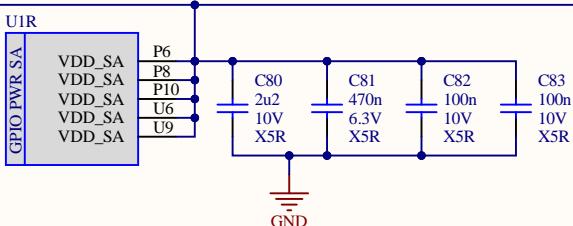
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GPIO_Diff_Net_Class



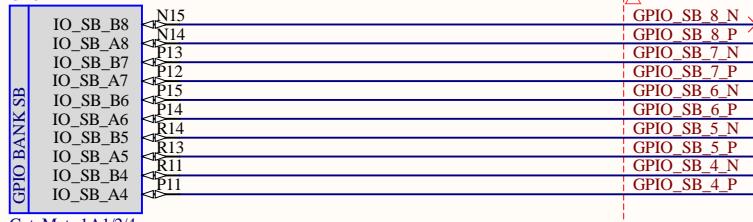
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A

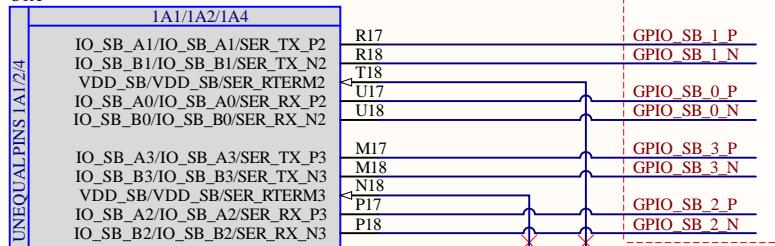
CLOCK0_IN

UI0



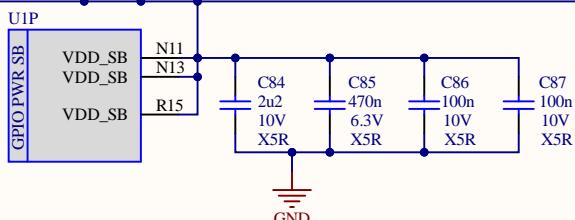
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UIX

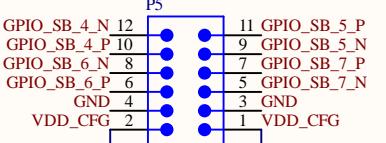
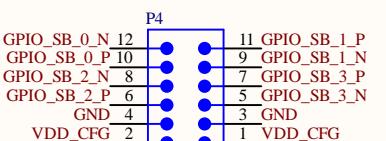


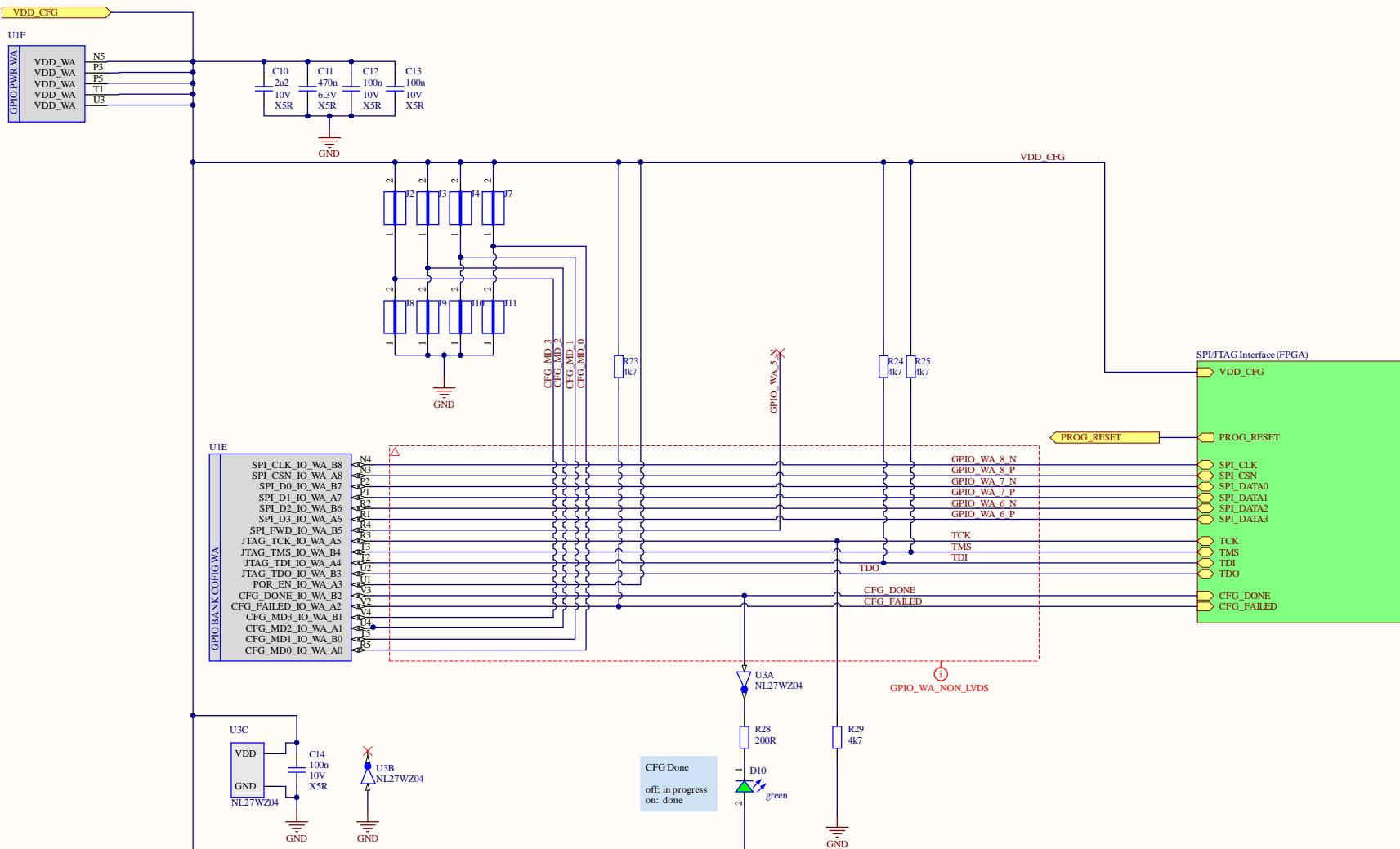
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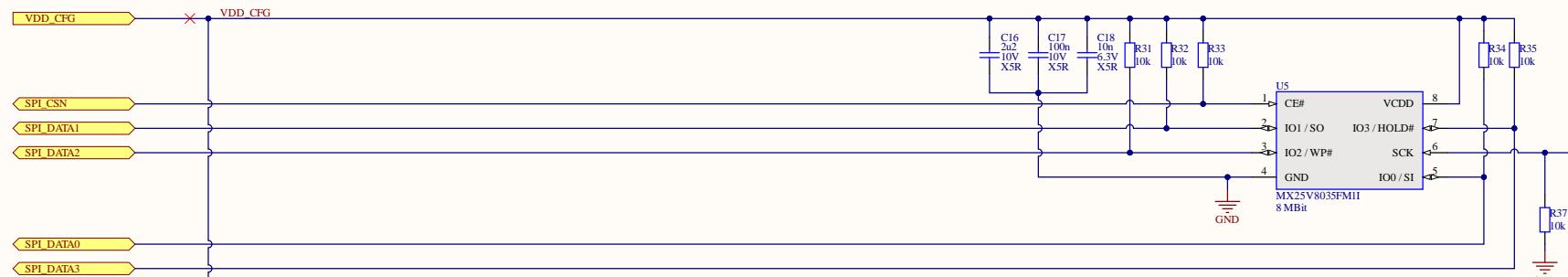


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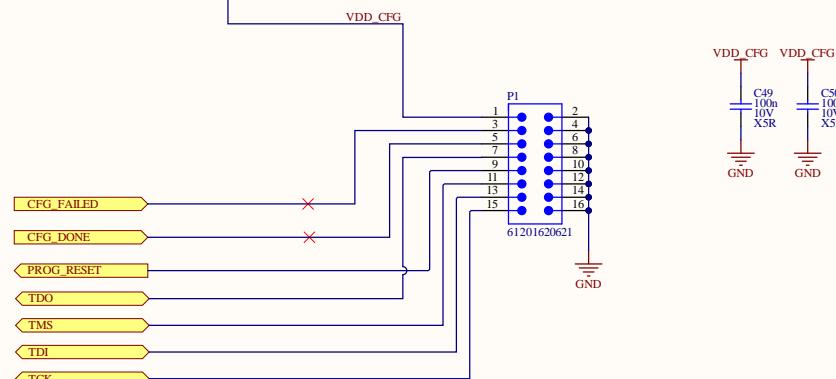




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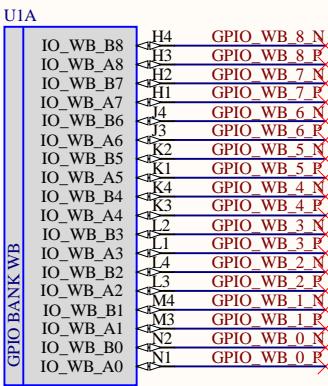
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Title:	SPI/JTAG Interface (FPGA)		
Size:	A3	Author:	CCAG
File:	FPGA_SPI_JTAG.SchDoc	Date:	08.07.2024
		Sheet	9 of 21

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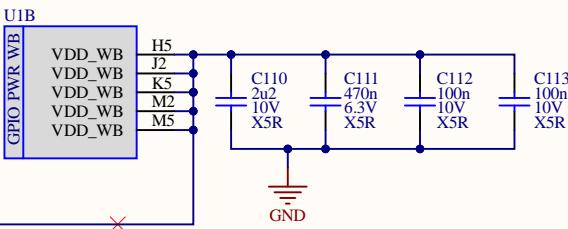
A

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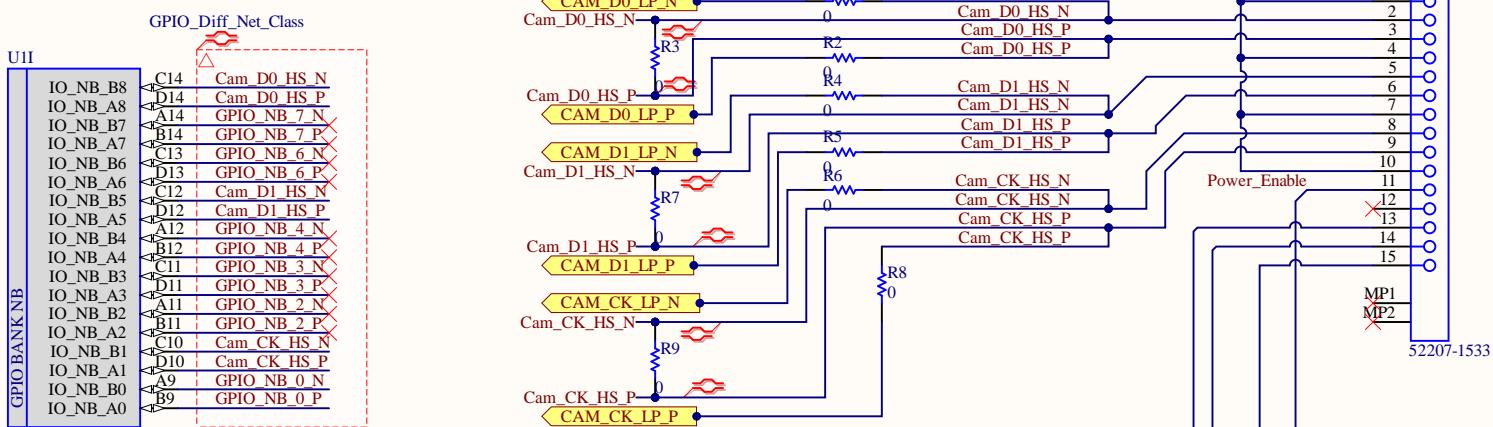
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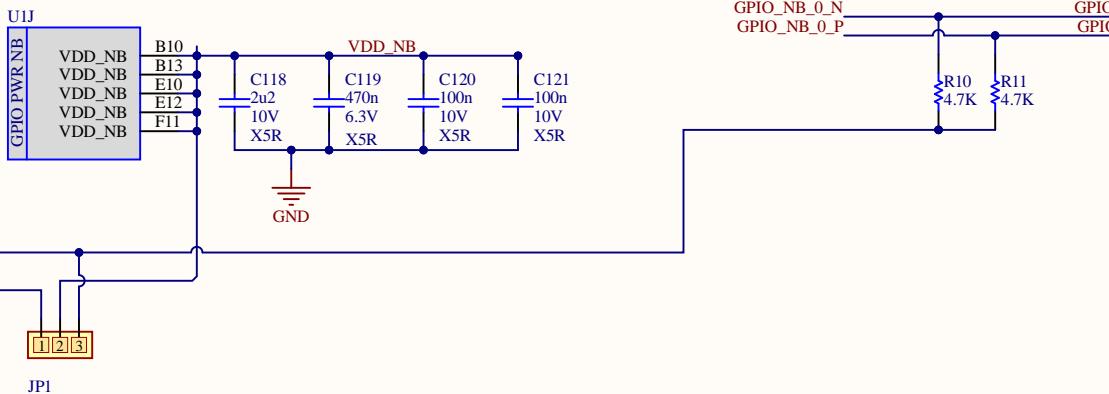
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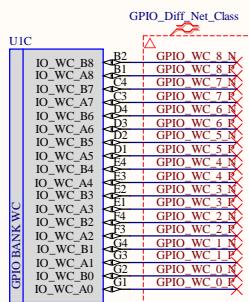
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C

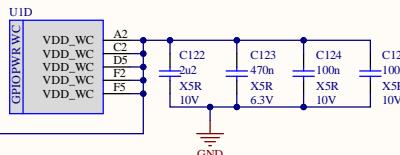
Project:	GateMate CCGM1A1 (BGA324) Evaluation Board	Revision:	3.1B
Title:	NB Bank GPIO Module Pmod (FPGA)		
Size:	A4	Author:	CCAG
Date:	08.07.2024	Sheet:	13 of 21
File:	FPGA_GPIO_NB.SchDoc	Cologne Chip AG Eintrachtstr. 113 50668 Cologne Germany	



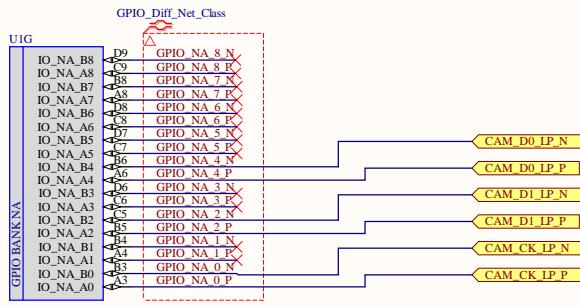
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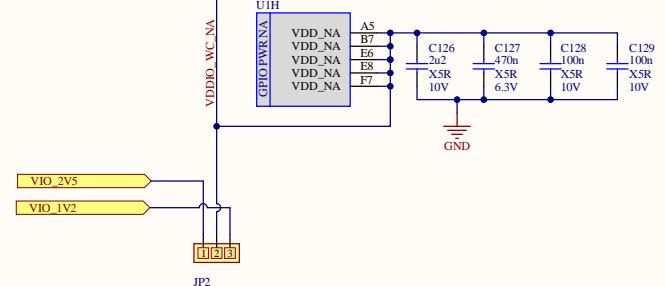
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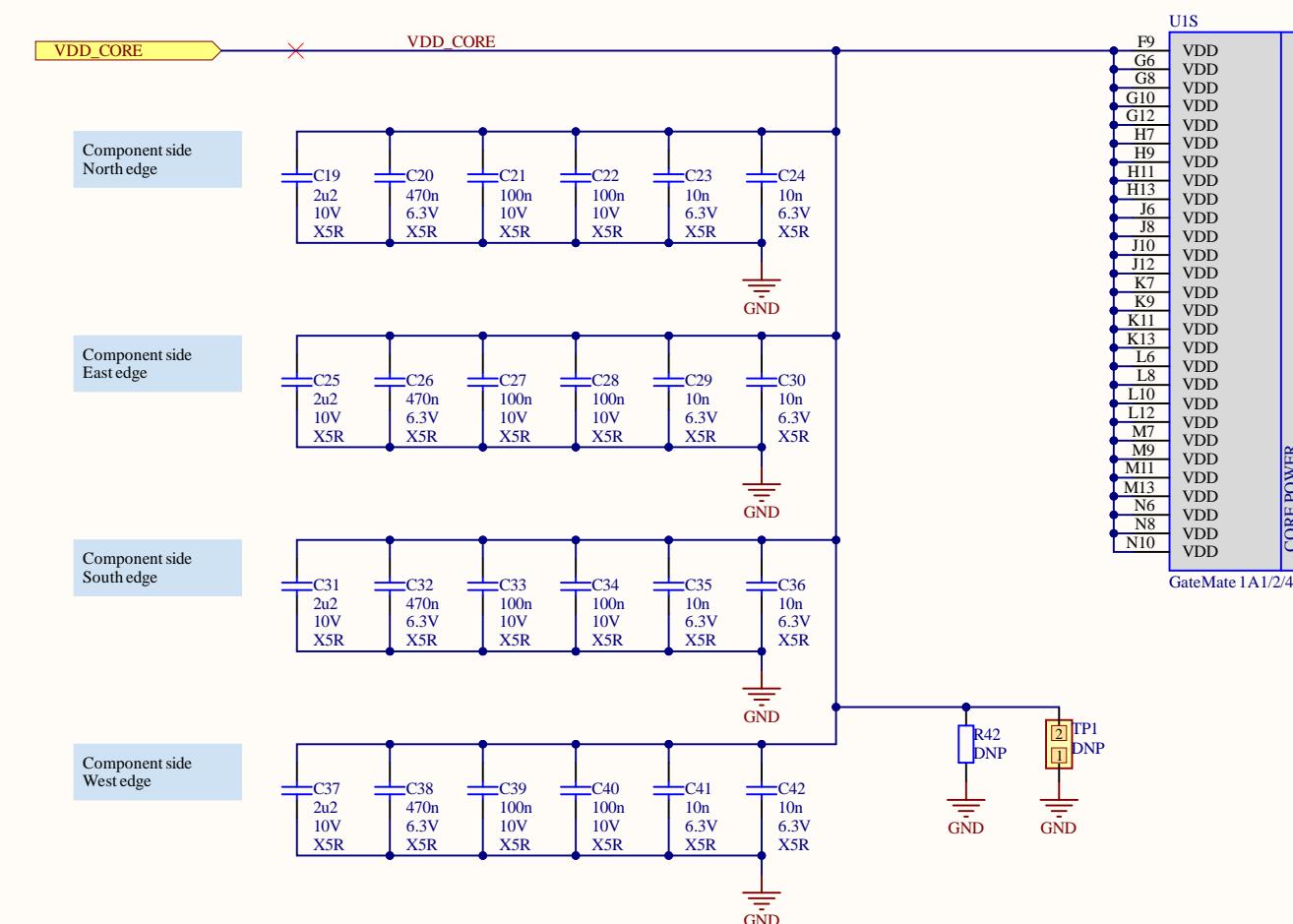


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Project:	GateMate CCGM1A1 (BGA324) Evaluation Board	Revision:	3.1B
Title:	WC/NA Banks GPIO Module (FPGA)		
Size:	A3	Author:	CCAG
File:	FPGA_GPIO_WC_NA.SchDoc	Date:	08.07.2024
		Sheet	15 of 21

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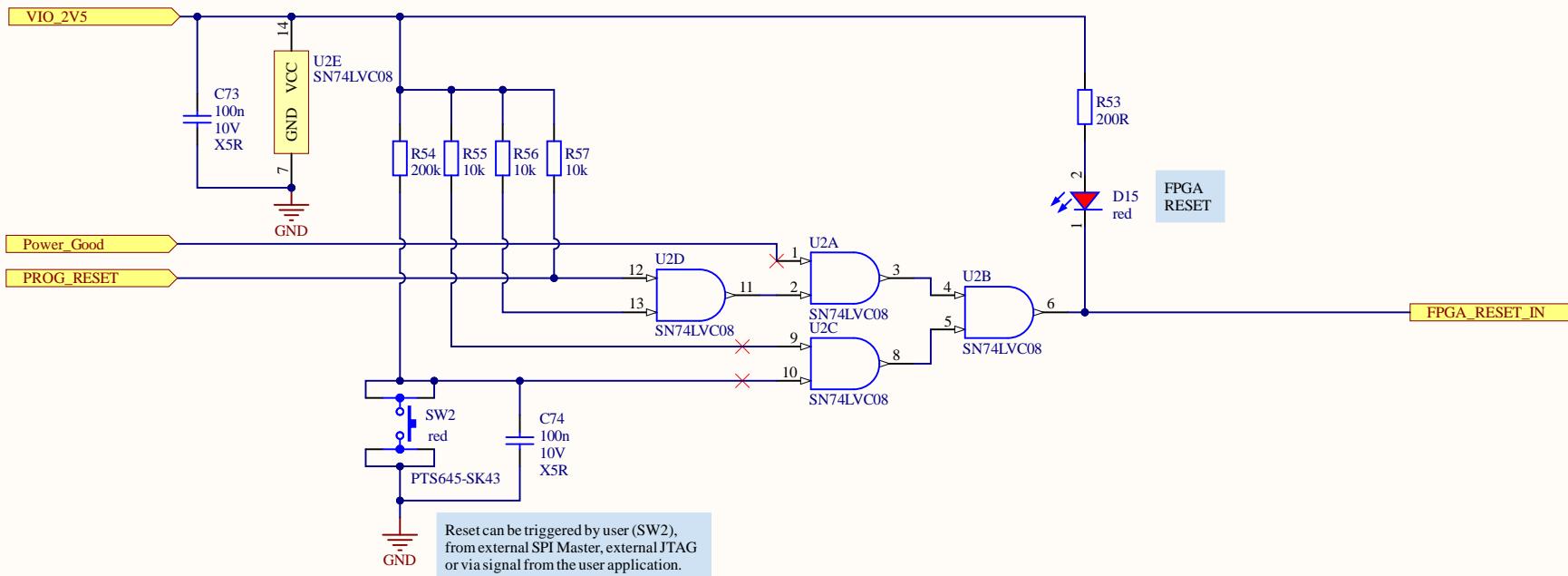
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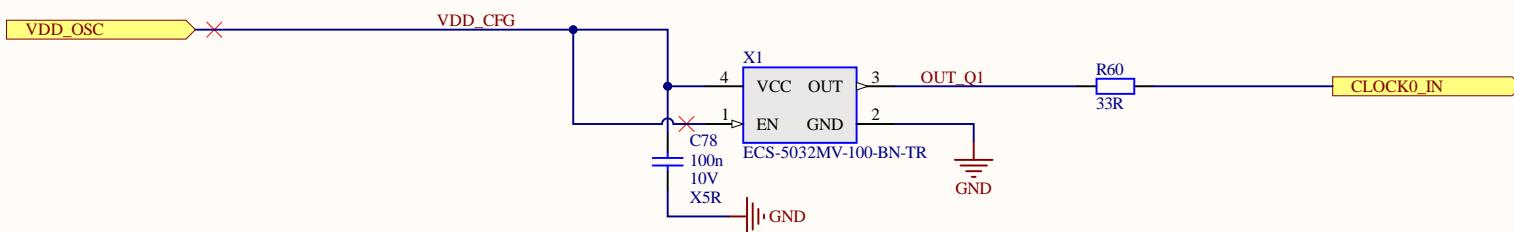
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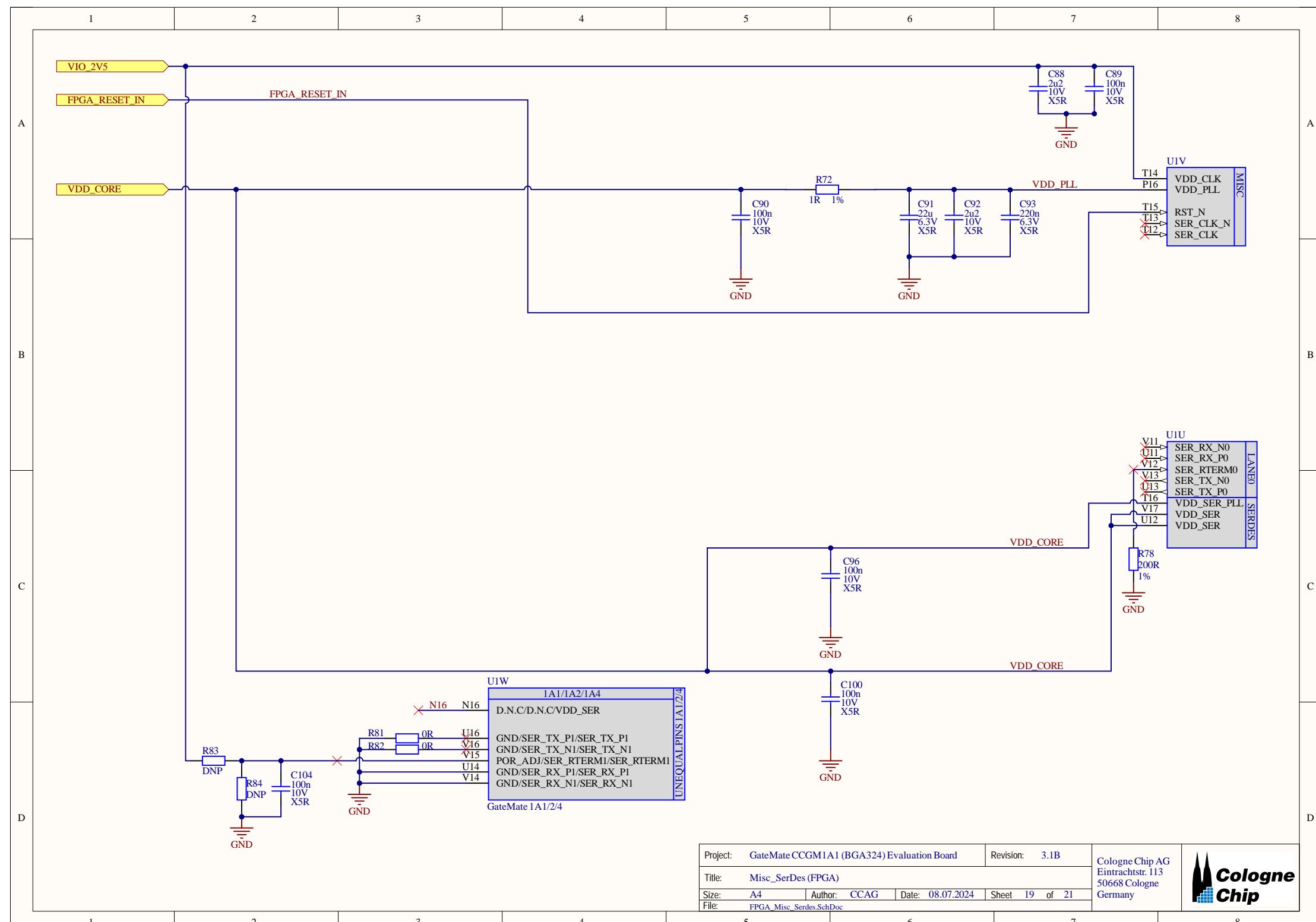
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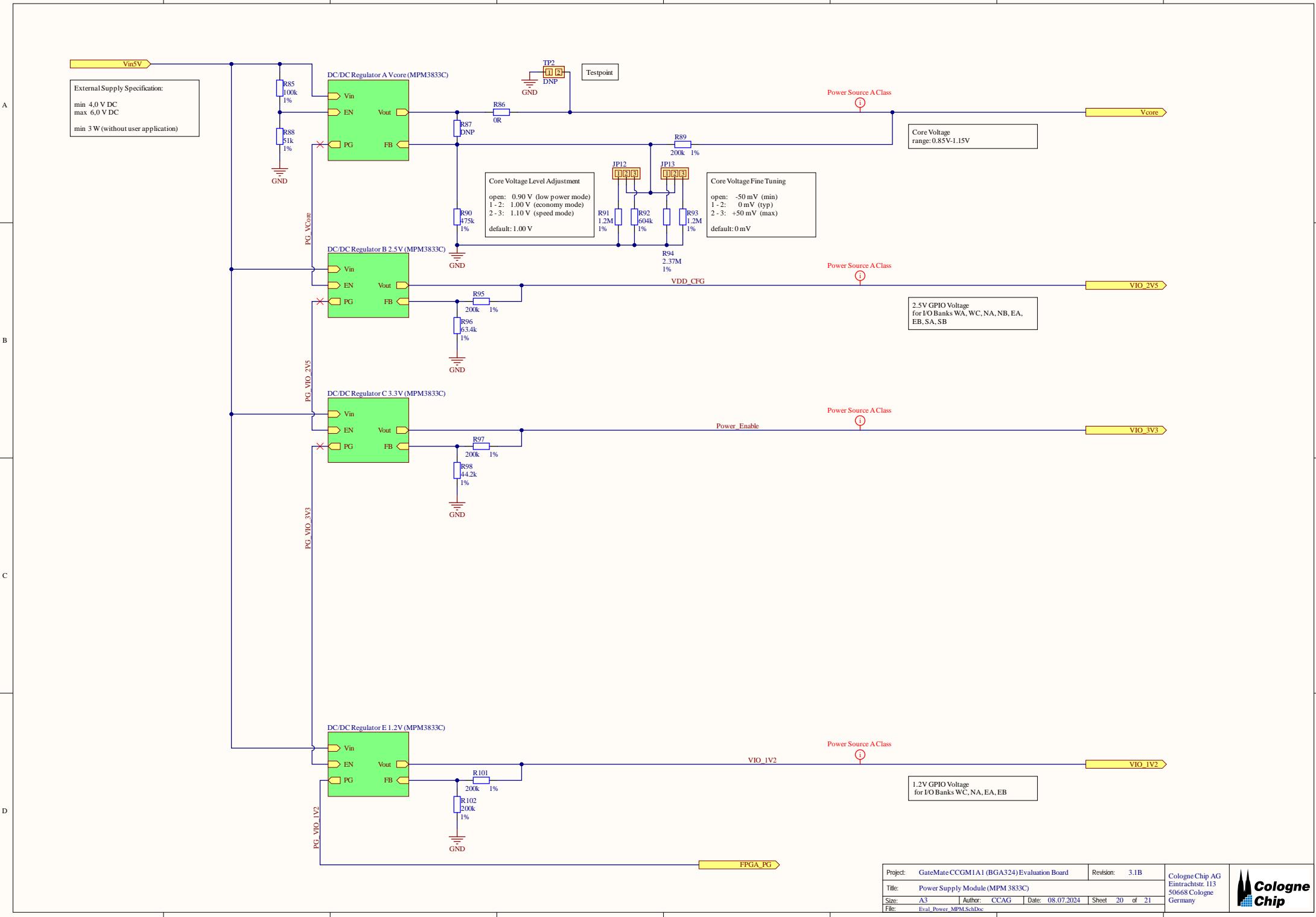
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Project:	GateMate CCGM1A1 (BGA324) Evaluation Board	Revision:	3.1B	Cologne Chip AG Eintrachtstr. 113 50668 Cologne Germany
Title:	Clock (FPGA)			
Size:	A4	Author:	CCAG	
Date:	08.07.2024	Sheet:	18 of 21	
File:	FPGA_Clock.SchDoc			





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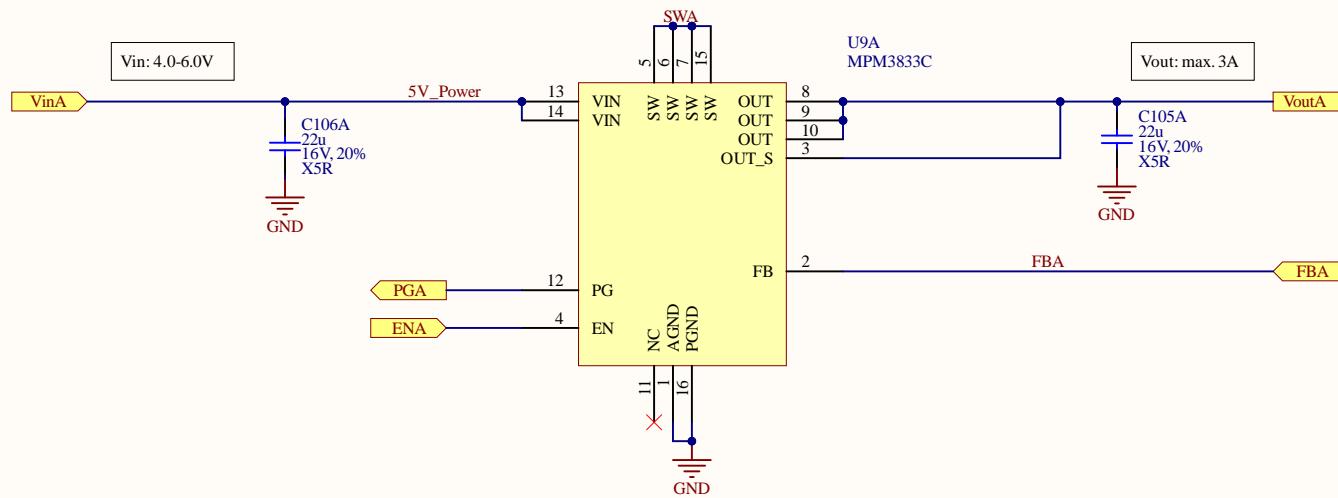
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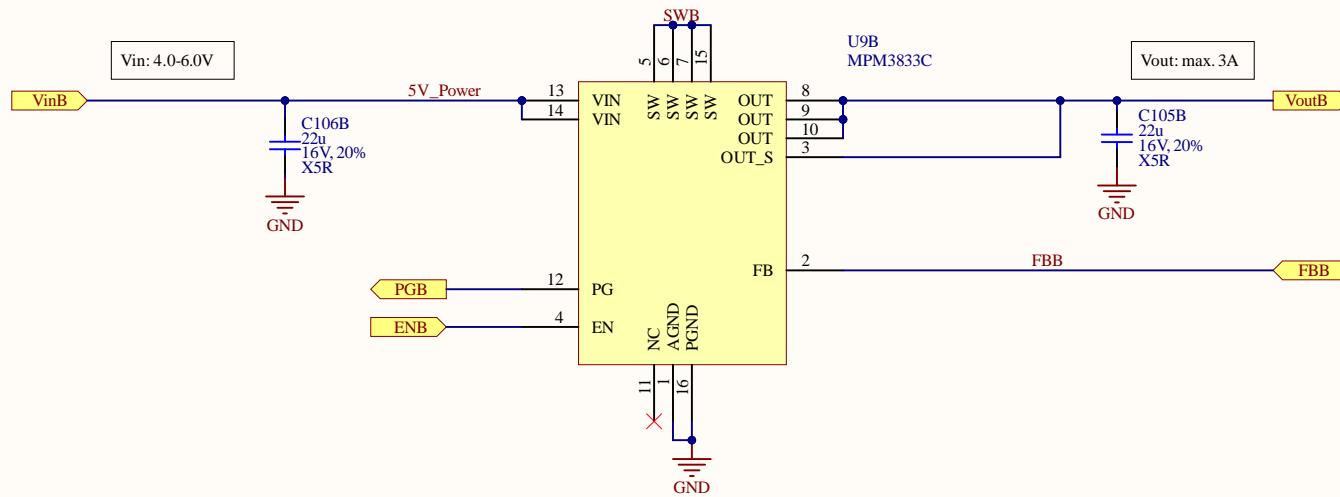
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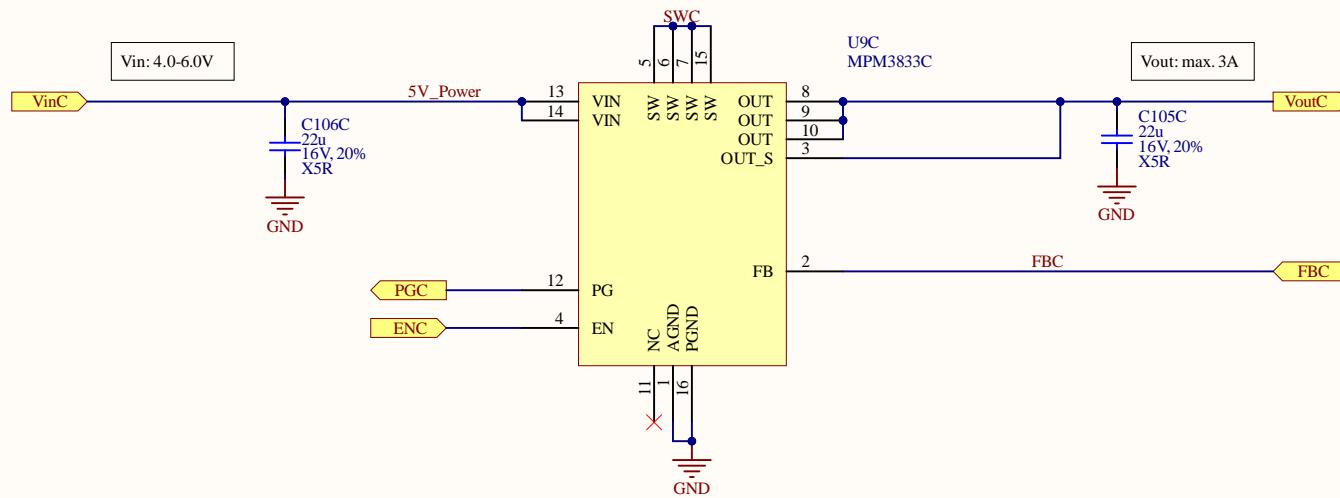
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