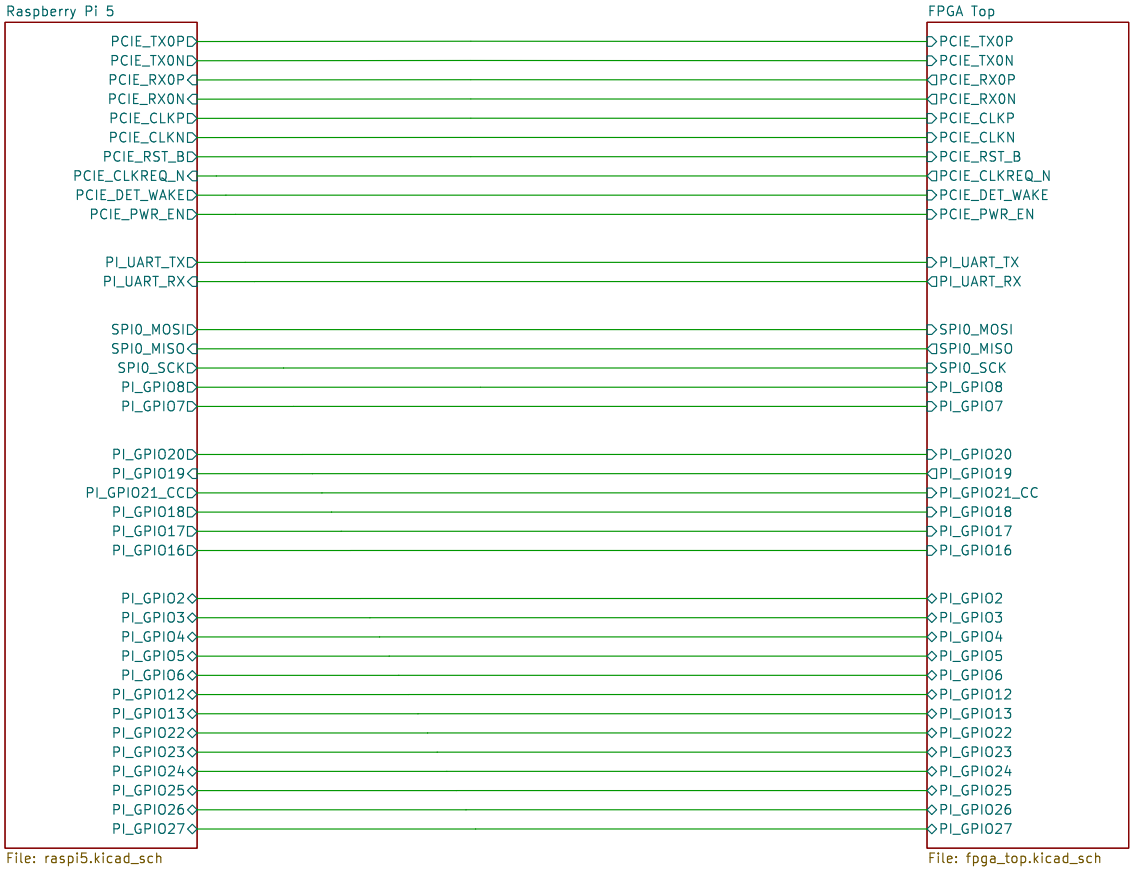

https://www.george-smart.co.uk
https://github.com/m1geo/Pi5-Artix-FPGA-Hat
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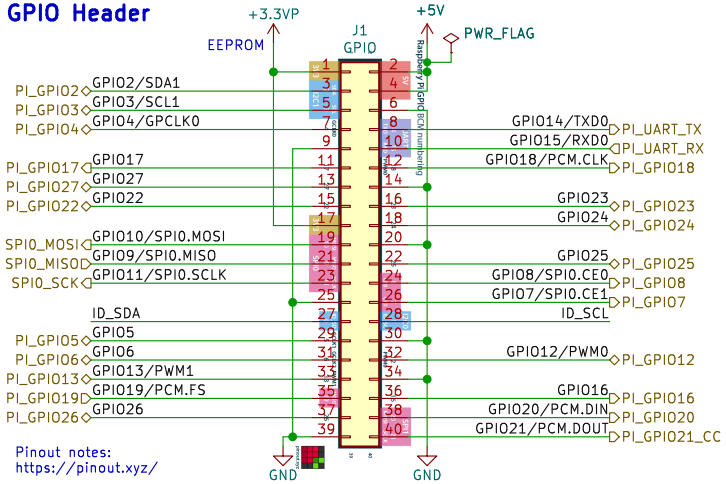
Sheet: /
File: Pi5-Artix50T-Hat.kicad_sch

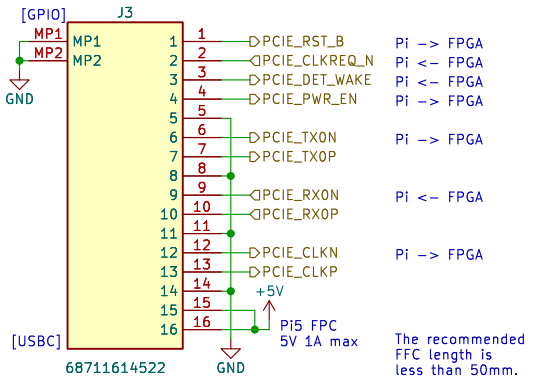
Title: Pi 5 - Artix XC7A50T - PCIe FPGA Hat

Size: A4	Date: 2024-03-24	**Rev: 1.1**
KiCad E.D.A. 8.0.1		Id: 1/9

GPIO Header



PCIe Header



Datasheet:
https://datasheets.raspberrypi.com/pcie/pcie-connector-standard.pdf

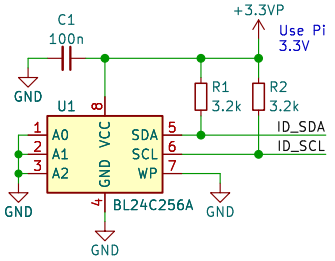
HAT EEPROM

ID_SD and ID_SC PINS:
These pins are reserved for HAT ID EEPROM.

At boot time this I2C interface will be interrogated to look for an EEPROM that identifes the attached board and allows automagic setup of the GPIOs (and optionally, Linux drivers).

Bridging JP1 enables write protection.

DO NOT USE these pins for anything other than attaching an I2C ID EEPROM. Leave unconnected if ID EEPROM not required.



Details: https://github.com/raspberrypi/hats

https://www.george-smart.co.uk
https://github.com/m1geo/Pi5-Artix-FPGA-Hat
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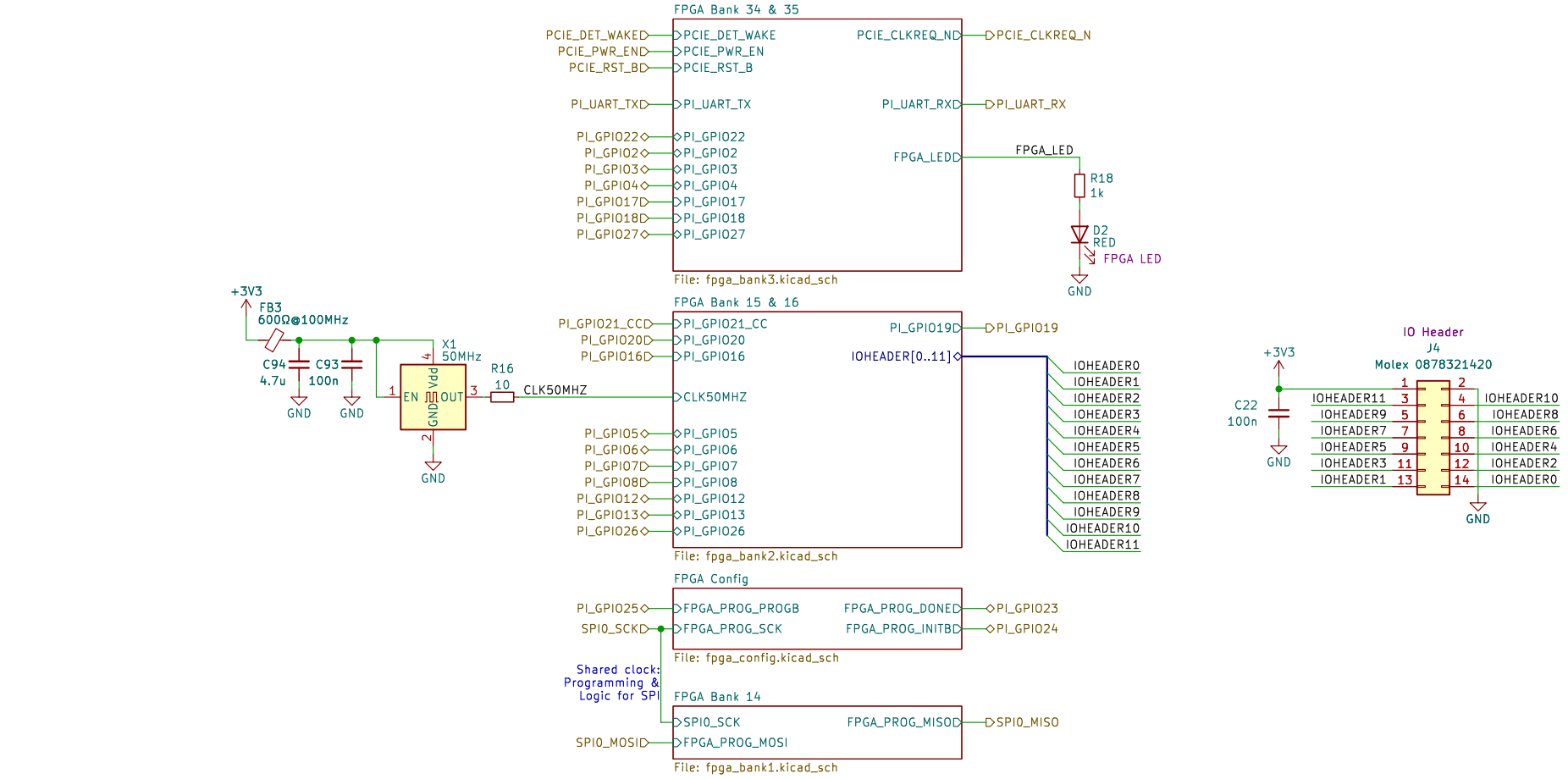
Sheet: /Raspberry Pi 5/
File: raspi5.kicad_sch

Title: Raspberry Pi 5 – GPIO & PCIe Headers

Size: A4	Date: 2024-03-24	**Rev: 1.1**
KiCad E.D.A. 8.0.1		Id: 2/9



https://www.george-smart.co.uk
https://github.com/m1geo/Pi5-Artix-FPGA-Hat
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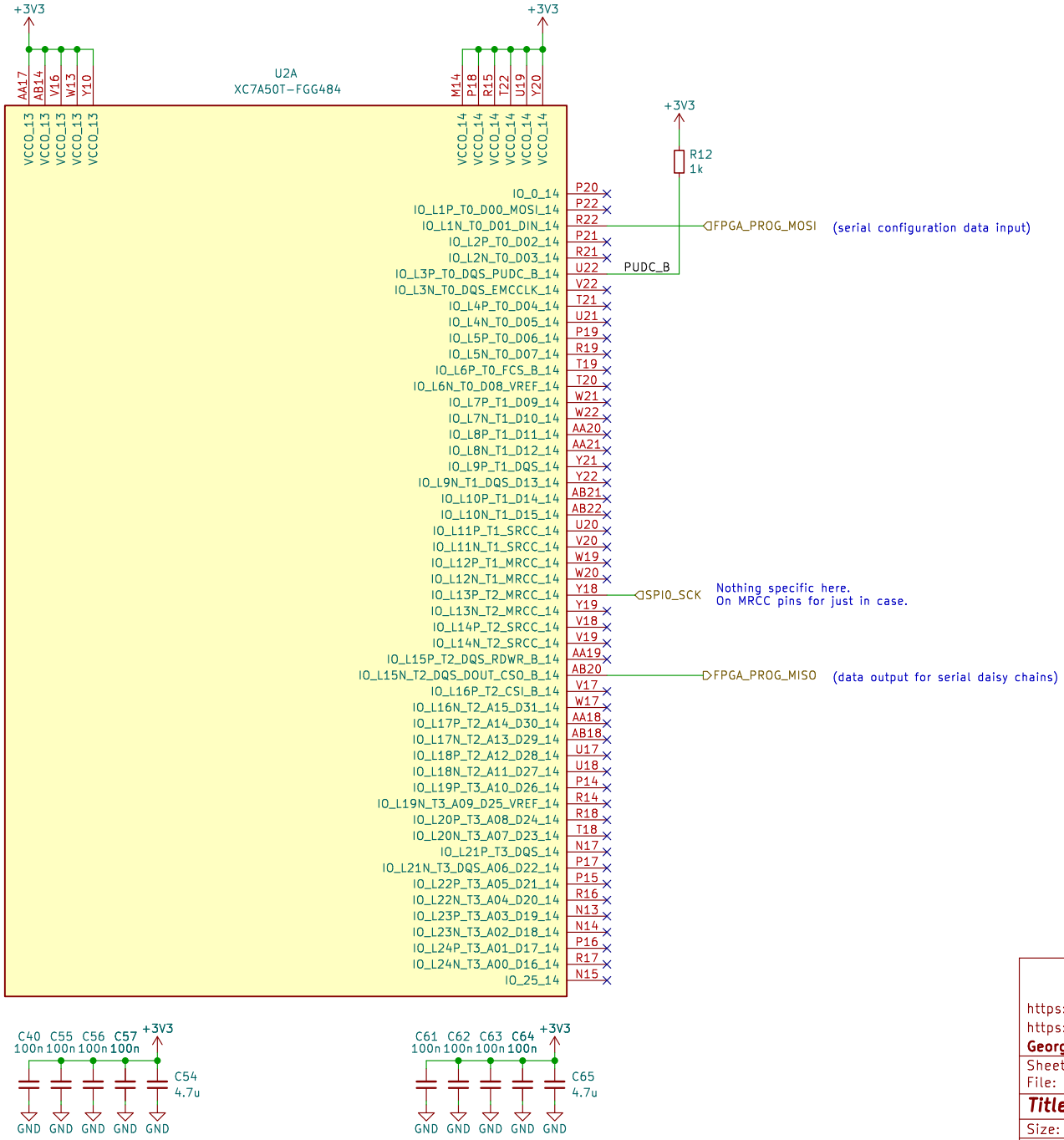
Sheet: /FPGA Top/
File: fpga_top.kicad_sch

Title: FPGA Top Sheet

Size: A4	Date: 2024-03-24	**Rev: 1.1**
KiCad E.D.A. 8.0.1		Id: 3/9



Pin Name	Bank	Slave Serial
CFGBVS	0	CFGBVS
M[2:0]	0	M[2:0]=111
TCK	0	TCK
TMS	0	TMS
TDI	0	TDI
TDO	0	TDO
PROGRAM_B	0	PROGRAM_B
INIT_B	0	INIT_B
DONE	0	DONE
CCLK	0	CCLK
PUDC_B(1)	14	PUDC_B(1)
EMCCLK(2)	14	–
CSI_B	14	–
DOUT_CSO_B(3)(4)	14	[DOUT](3)
RDWR_B	14	–
FCS_B	14	–
D00_MOSI	14	–
D01_DIN	14	DIN
D02	14	–
D03	14	–
D[04-07]	14	–
D[08-15]	14	–
A[00-15]_D[16-31]	14	–
A[16-28]	15	–
FOE_B	15	–
FWE_B	15	–
ADV_B	15	–
RS0, RS1(5)	15	RS0, RS1(5)

https://www.george-smart.co.uk
https://github.com/m1geo/Pi5-Artix-FPGA-Hat
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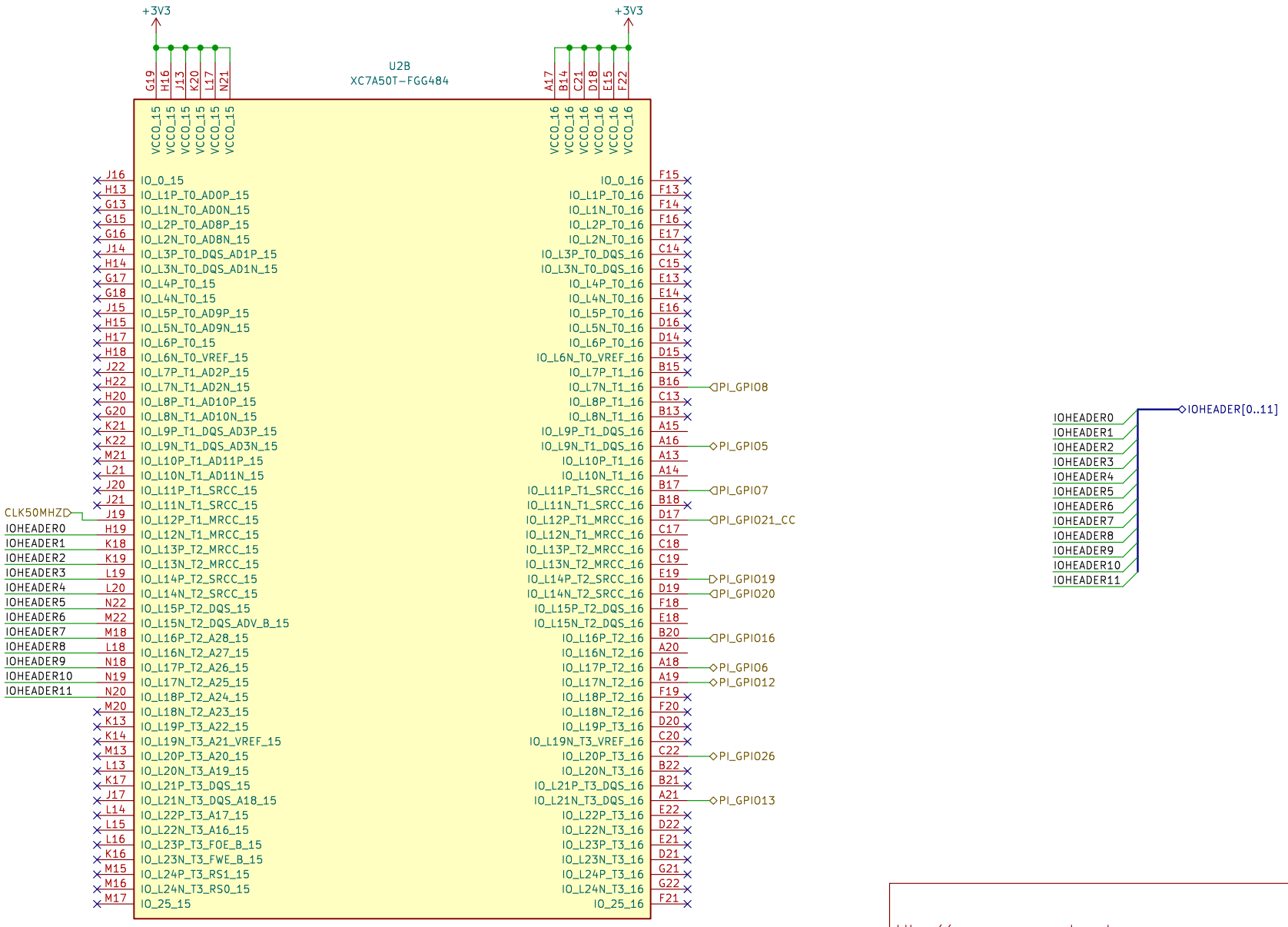
Sheet: /FPGA Top/FPGA Bank 14/
File: fpga_bank1.kicad_sch

Title: FPGA Bank 14

Size: A4	Date: 2024-03-24	**Rev: 1.1**
KiCad E.D.A. 8.0.1		Id: 4/9



https://www.george-smart.co.uk
https://github.com/m1geo/Pi5-Artix-FPGA-Hat
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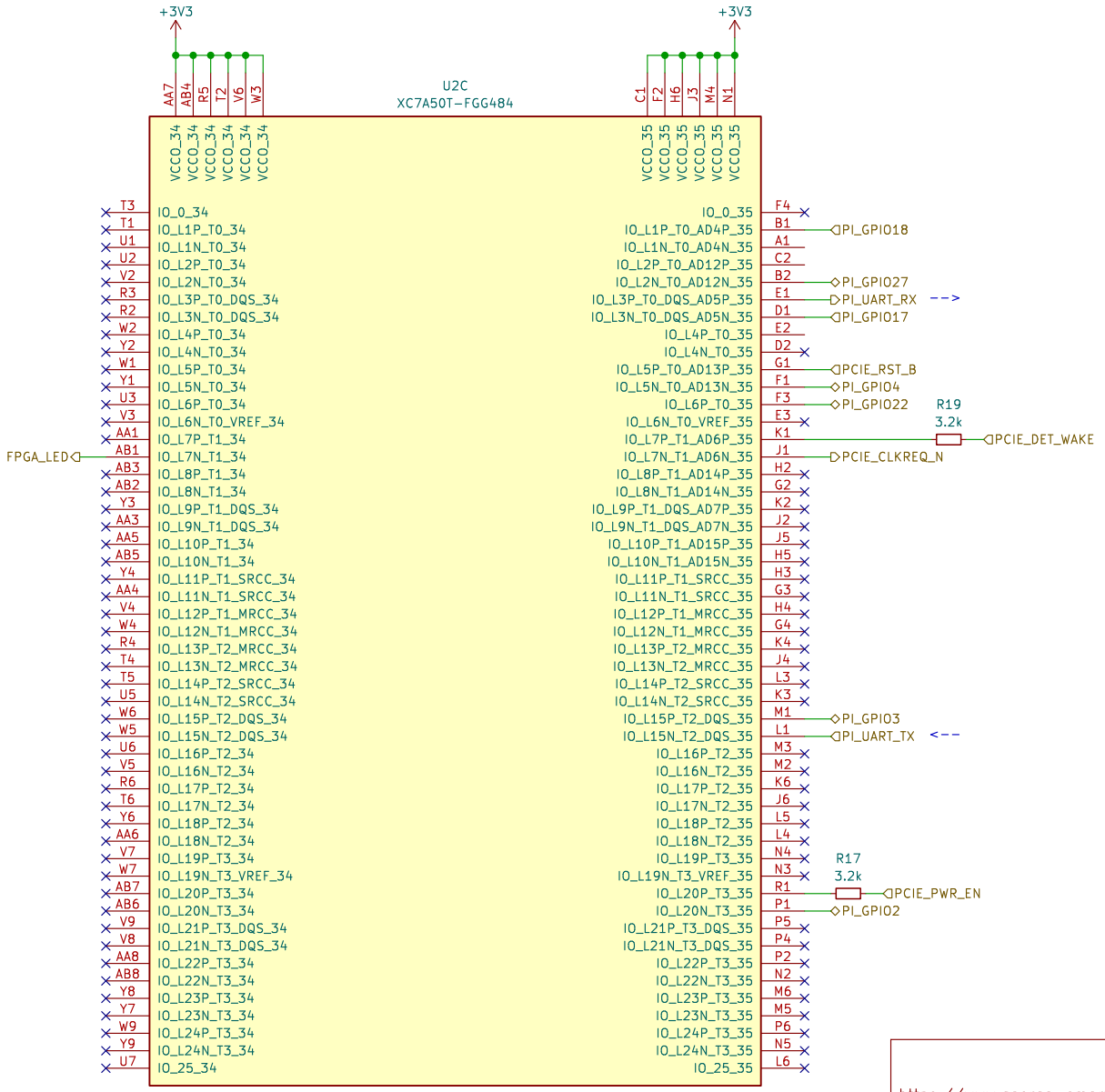
Sheet: /FPGA Top/FPGA Bank 15 & 16/
File: fpga_bank2.kicad_sch

Title: FPGA Banks 15 & 16

Size: A4	Date: 2024-03-24	**Rev: 1.1**
KiCad E.D.A. 8.0.1		Id: 5/9



https://www.george-smart.co.uk
https://github.com/m1geo/Pi5-Artix-FPGA-Hat
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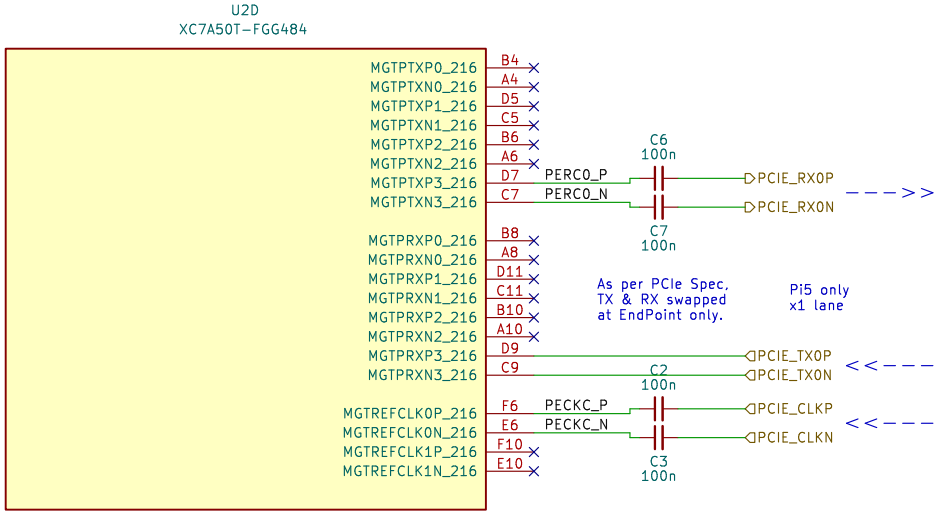
Sheet: /FPGA Top/FPGA Bank 34 & 35/
File: fpga_bank3.kicad_sch

Title: FPGA Banks 34 & 35

Size: A4	Date: 2024-03-24	**Rev: 1.1**
KiCad E.D.A. 8.0.1		Id: 6/9

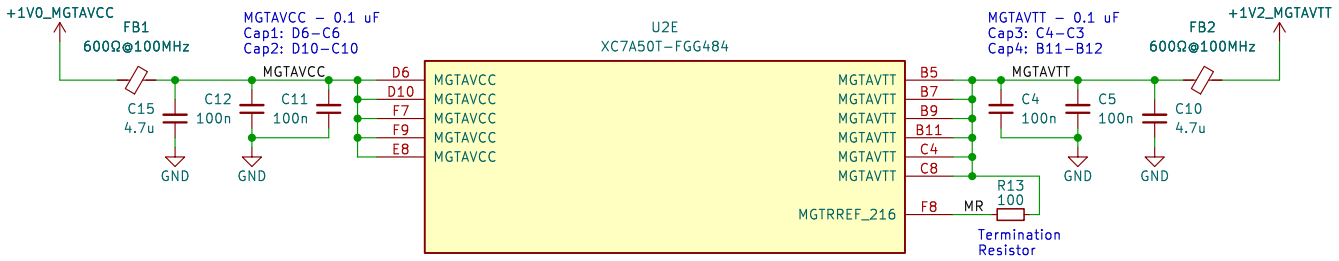
Table 4-12: **Artix-7 Recommended GT Locations**

Device	Package	Integrated Block Location	Lane	X1	X2	X4	X8
XC7A200T	FBG484, FBG676, FFG1156, SBG484, FBV484, FBV676, FFV1156, SBV484	X0Y0	Lane 0	X0Y7	X0Y7	X0Y7	Not Supported
			Lane 1		X0Y6	X0Y6	
XC7A100T	FGG484, FGG676		Lane 2			X0Y5	
XC7A75T	FGG484, FGG676		Lane 3			X0Y4	
XC7A35T ×	FGG484, CPG236, CSG325	X0Y0	Lane 0	X0Y3	X0Y3	X0Y3	Not Supported
			Lane 1		X0Y2	X0Y2	
			Lane 2			X0Y1	
XC7A50T	FGG484, CPG236, CSG325		Lane 3			X0Y0	



Test build:

C7	pci_exp_txn[0]	MGTPTXN3_216
C9	pci_exp_rxn[0]	MGTPRXN3_216
D7	pci_exp_txp[0]	MGTPTXP3_216
D9	pci_exp_rxp[0]	MGTPRXP3_216
E6	sys_clk_n	MGTREFCLK0N_216
F6	sys_clk_p	MGTREFCLK0P_216



Each supply ($V_{MGTAVCC}$ and $V_{MGTAVTT}$) needs:
1x 4.7uF
2x 100nF
Recommended 0401 between pads on back
see UG482 for details

Series 7 MGT Datasheets:

https://docs.xilinx.com/v/u/en-US/ug482_7Series_GTP_Transceivers
pg054-7series-pcie-en-us-3.3

https://www.george-smart.co.uk
https://github.com/m1geo/Pi5-Artix-FPGA-Hat
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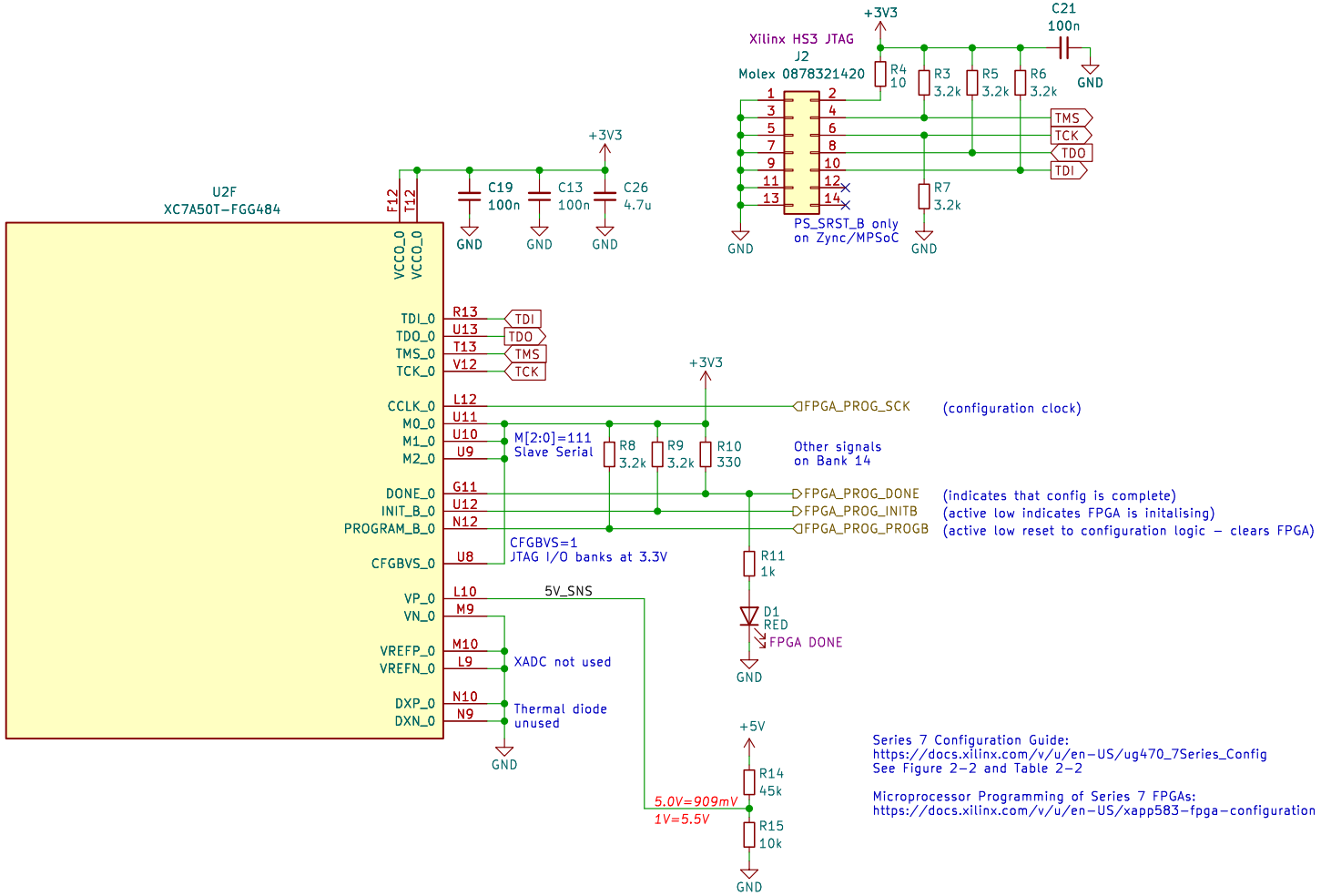
Sheet: /FPGA Top/FPGA Bank 216 (MGT)/
File: fpga_bank4.kicad_sch

Title: FPGA Bank 216 (MGT/PCIe)

Size: A4	Date: 2024-03-24	**Rev: 1.1**
KiCad E.D.A. 8.0.1		Id: 7/9



Series 7 Configuration Guide:
https://docs.xilinx.com/v/u/en-US/ug470_7Series_Config
See Figure 2-2 and Table 2-2

Microprocessor Programming of Series 7 FPGAs:
https://docs.xilinx.com/v/u/en-US/xapp583-fpga-configuration

Pin Name	Bank	Slave Serial
CFGBVS	0	CFGBVS
M[2:0]	0	M[2:0]=111
TCK	0	TCK
TMS	0	TMS
TDI	0	TDI
TDO	0	TDO
PROGRAM_B	0	PROGRAM_B
INIT_B	0	INIT_B
DONE	0	DONE
CCLK	0	CCLK
PUDC_B(1)	14	PUDC_B(1)
EMCCLK(2)	14	–
CSI_B	14	–
DOUT_CSO_B(3)(4)	14	[DOUT](3)
RDWR_B	14	–
FCS_B	14	–
D00_MOSI	14	–
D01_DIN	14	DIN
D02	14	–
D03	14	–
D[04-07]	14	–
D[08-15]	14	–
A[00-15]_D[16-31]	14	–
A[16-28]	15	–
FOE_B	15	–
FWE_B	15	–
ADV_B	15	–
RS0, RS1(5)	15	RS0, RS1(5)

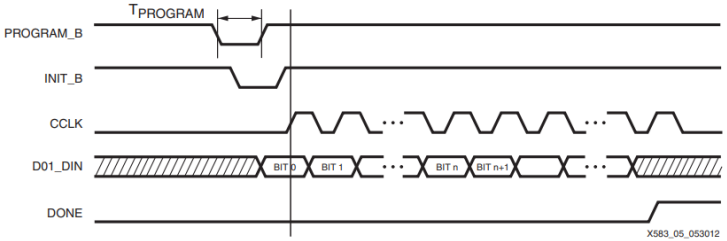


Figure 5: **Serial Configuration Clocking Sequence**

Programming Pseudocode
1) Pulse PROGRAM_B
2) Check INIT_B = 0
3) Wait for INIT_B = 1
4) Send config bitstream
5) Check INIT_B = 1 (if low, config failed)
6) Send clock for special startup conditions
7) Check DONE = 1 (if low, startup timeout)
8) Supply 8 further clock cycles (see XAPP583)

FPGA reprogramming can be restarted by repeating (1)

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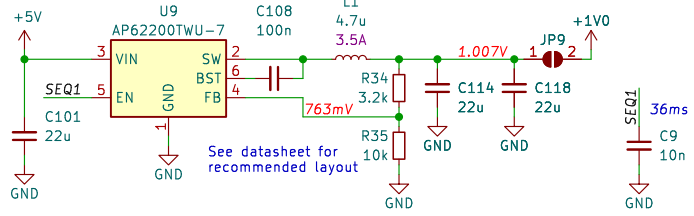
Sheet: /FPGA Top/FPGA Config/
File: fpga_config.kicad_sch

Title: FPGA Bank 0 (Config)

Size: A4	Date: 2024-03-24	**Rev: 1.1**
KiCad E.D.A. 8.0.1		Id: 8/9

VCCINT + VCCBRAM (1.0V)

Seq-#1

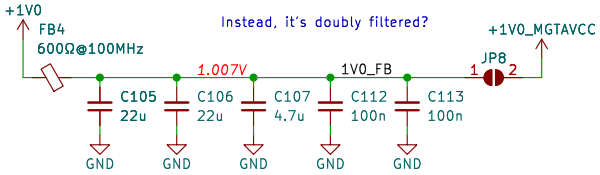


VMGTAVCC (1.0V)

Seq-#1

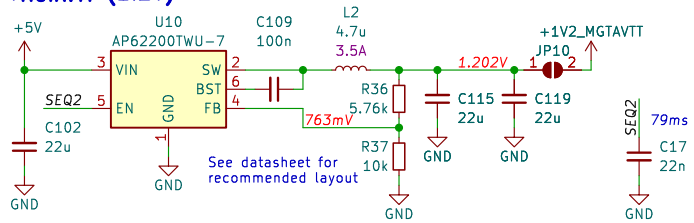
This should be a separate LDO according to the datasheet.

Instead, it's doubly filtered?



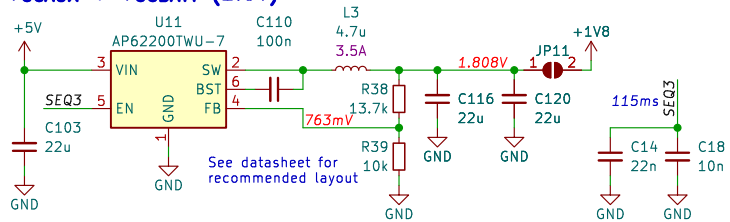
VMGTAVTT (1.2V)

Seq-#2



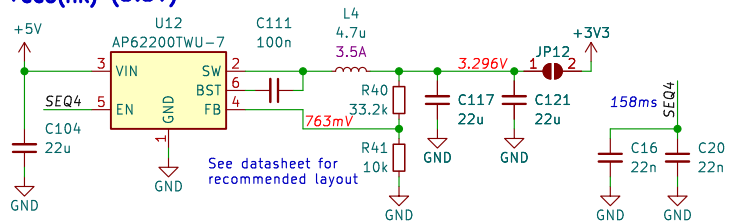
VCCAUX + VCCBATT (1.8V)

Seq-#3

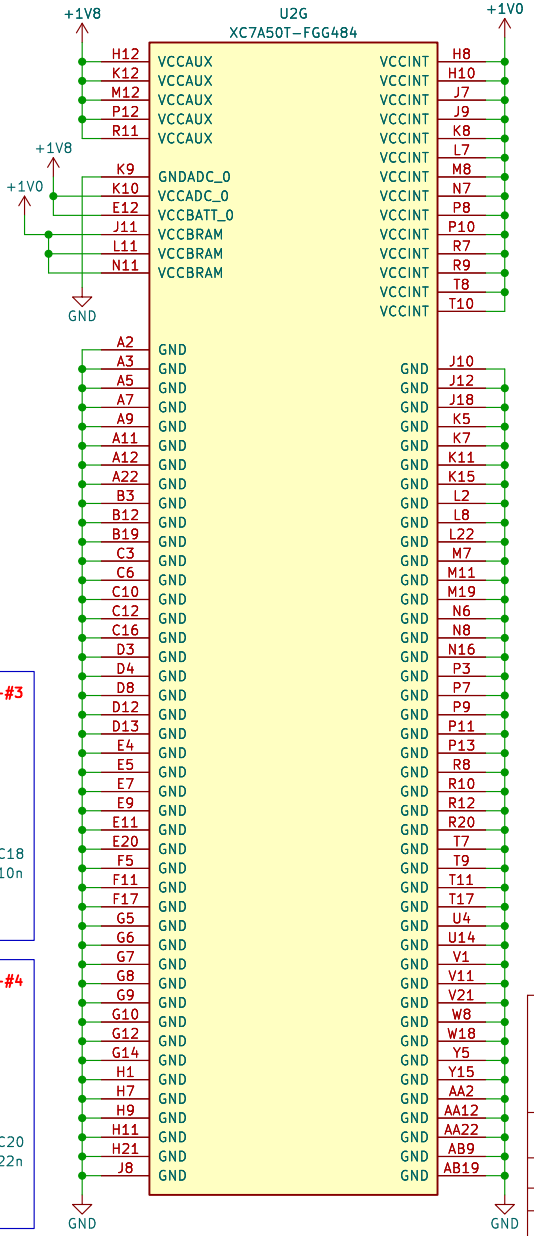


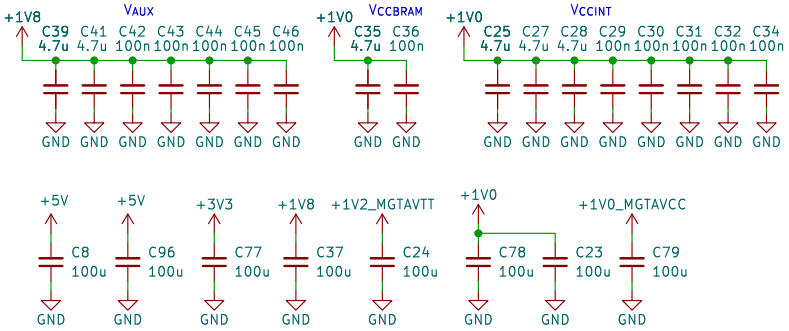
VCCO(HR) (3.3V)

Seq-#4



Seq #1 : 1.0V : 350mA : VCCINT + VCCBRAM + VMGTAVCC
Seq #2 : 1.2V : 150mA : VMGTAVTT
Seq #3 : 1.8V : 50mA? : VCCAUX + VCCBATT
Seq #4 : 3.3V : 500mA : VCCO(HR)





Power planning – see UG483 – supplies within ±5%
VCCINT = 1.0V (>120mA) [link to VCCBRAM]
VCCBRAM = 1.0V (>60mA) [link to VCCINT]
VCCAUX = 1.8V (>40mA)
VCCBATT = 1.8V [link to VCCAUX]
VCCO(HR) = 3.3V (>40mA/bank) [LVCMOS33]

VMGTAVCC = 1.0V (>140mA)
VMGTAVTT = 1.2V (>140mA)
Decouple with 1x4.7uF & 2x0.1uF ceramic 0402/0201 per group.

MGT supplies should not share with non-MGT signals.

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT.

The voltage difference between VCCO and VCCAUX must not exceed 2.625V for longer than TVCCO2VCCAUX (min 300ms).

AP62200T:
*Cd[nF] = 0.278 * td[ms]*
Cd[nF] / 0.278 = td[ms]

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https://github.com/m1geo/Pi5-Artix-FPGA-Hat
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Sheet: /FPGA Top/FPGA Power/
File: fpga_power.kicad_sch

Title: FPGA Power Supplies & Core Decoupling

Size: A4	Date: 2024-03-24	Rev: 1.1
KiCad E.D.A. 8.0.1		Id: 9/9